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The objective of this thesis is to contribute to the development of p-type materials for transparent electronics applications. Thin films of α-$BaCu_2S_2$, a p-type semi-transparent semiconductor, are fabricated and characterized. α-$BaCu_2S_2$ has a transmittance of 60% to 80 % in the visible portion of the electromagnetic spectrum. The mobility, conductivity, and carrier concentration of α-$BaCu_2S_2$ are 3.5 cm^2/V-s, 17 S/cm, and 10^{19} cm^{-3}, respectively. The potential use of $BaCu_2S_2$ in thin-film solar cells is described. A number of p-channel transparent thin-film transistors (p-TTFTs) based on $BaCu_2S_2$, NiO, NiO:Li, and $CuScO_2$ are fabricated and characterized. None of these p-TTFTs are operational. The key issues in these transistors are as follows. $BaCu_2S_2$ p-TTFTs exhibit excessively large gate leakage current caused by the interaction of $BaCu_2S_2$ with the gate insulator. In undoped NiO p-TTFTs and in $CuScO_2$ p-TTFTs, the injected carriers are trapped in the transistor channel layer thin film. $CuScO_2$ p-TTFTs also suffer from gate leakage due to interaction of $CuScO_2$ with the gate insulator. In this work it is found that having Cu containing materials in contact with gate insulators leads to enhanced gate leakage current. In NiO:Li p-TTFTs, the bulk channel layer is too conductive to modulate with the transistor gate; thus, the transistors do not work. Information obtained from the characterization of these p-TTFTs is used to identify and explore important considerations in making a functional p-TTFT. These considerations include efficient injecting contacts to wide-bandgap p-type insu-

lators, and the conductivity of materials used for the transistor channel in p-TTFTs. The topic of injecting contacts to wide-bandgap insulators and the topic of channel layer conductivity are explored and quantified.

p-Type Transparent Electronics

by

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Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Melinda Marie Valencia, Author

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P-TYPE TRANSPARENT ELECTRONICS

1. INTRODUCTION

The field of transparent electronics is just emerging. In recent years, a number of transparent semiconductors have been developed and characterized. These include both n-type and p-type semiconductors. With further research these transparent semiconductors may be used to form complex transparent electronic devices, circuits, and systems. At this stage of development, the primary focus is on the demonstration of discrete transparent devices and clarification of the chemistry and physics of their fabrication and operation. Various device issues remain to be resolved, however, with respect to the wide-bandgap materials used in transparent devices. Many of these considerations are not addressed in device theories currently utilized in the assessment of devices fabricated with more traditional narrow to moderate bandgap semiconductors. This thesis addresses two of these issues, injecting contacts and carrier conductivity/trapping in wide-bandgap insulating materials.

Recently there have been several reports in the literature of successful n-channel transparent thin-film transistors (n-TTFTs). The goal of this thesis research was to fabricate and characterize an operational p-channel transparent thin-film transistor (p-TTFT). Although an operational p-TTFT is not demonstrated in this work, analysis of the p-TTFTs fabricated leads to insight into injecting contacts and channel conductivity/trapping, topics which are believed to be of fundamental importance for the realization of an operational p-TTFT.

Semi-transparent p-type $BaCu_2S_2$ films produced in this thesis research have application in the area of solar cells. Improvements to solar cells are continually being sought, as solar cells have the potential to provide low-cost, environmentally friendly energy on a large scale. In this thesis the current state-of-the-art of $Cu(In,Ga)Se_2$ solar cells are

described, followed by a discussion of a new double heterojunction p-i-n thin-film solar cell design that may incorporate $BaCu_2S_2$ as a p-layer.

This thesis is organized as follows. Chapter 2 presents technical background information useful to the understanding of research presented in this thesis, as well as a review of relevant literature. Chapter 3 describes the experimental techniques used in this work. Chapter 4 contains work on $BaCu_2S_2$ thin films and the use of $BaCu_2S_2$ in thin-film solar cell applications. Chapter 5 describes the fabrication and characterization of a number of p-TTFTs. Chapter 6 presents conclusions and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

This chapter presents technical background material and a literature review of topics relevant to this thesis. Transparent conductors are discussed. The fabrication and operation of thin-film transistors are presented. Materials issues particular to the channel layer of thin-film transistors are examined. Transparent thin-film transistors reported in the literature are summarized. Metal-semiconductor contacts are discussed with the purpose of elucidating injecting contacts.

2.1 Transparent Conductors

Transparent conductors are materials that possess both good electrical conductivity and transparency in the visible portion of the electromagnetic spectrum. A wide bandgap ($\sim>$ 3 eV) is needed for visible transparency. Both n-type and p-type transparent conductors continue to be developed.

2.1.1 n-Type Transparent Conductors

n-type transparent conducting oxides (n-TCOs) have been used for many years in applications requiring both conductivity and optical transparency. Some TCO applications include transparent electrodes for flat-panel displays, thermal management for window glass, and electrochromic windows. [1] Some of the commonly used n-TCOs are shown in Table 2.1.

2.1.2 p-Type Transparent Conductors

There has been a recent push to develop p-type transparent conductors (p-TCs) in order to open up a new range of applications for transparent electronics that includes p-n junctions and complementary circuits. Several p-type transparent conductors have been developed recently (Table 2.2). The electrical performance (conductivity, mobility) of these materials does not approach that of the n-type transparent conductors. This

Table 2.1: Properties of common n-type transparent conducting oxides. Trans.: optical transmittance in the visible region; σ: conductivity; μ: mobility; n: carrier concentration; E_g: optical band gap.

Material	Trans. %	σ (S/cm)	n (cm^{-3})	μ (cm^2/V-s)	E_g (eV)
Cd_2SnO_4 [2]	88-90	$\sim 10^4$	$\sim 10^{21}$	30-50	2.9-3.1
$CuInO_2$:Sn [3]	50-80	3.8×10^{-3}			3.9
In_2O_3:Sn [2]	90	$\sim 10^4$	10^{21}	15-40	$\sim$3.8
SnO_{2-x} [2]	80-90	100-300	10^{19}-10^{20}	5-30	3.9-4.3
ZnO_{1-x} [2]	80-90	$\sim 10^4$	10^{19}-10^{21}	$\sim$20	3.2
ZnO:Al [2],[4]	80-85	$\sim 10^4$	$\sim 10^{19}$-10^{20}	$\sim$20	3.2
ZnO:F [5]	85	100	10^{20}	$\sim$5	3.2
$ZnSnO_3$ [6]	80	$\sim$200	10^{20}	10	3.5

is expected, to some degree, due to the stronger localization of carriers in p-type versus n-type materials. This localization leads to a lower mobility. The specific p-type transparent semiconductors used in the research described in this thesis ($CuScO_2$, $BaCu_2S_2$, NiO) are discussed in more detail below. Also, $CuInO_2$ is discussed because it is a transparent conductor that has been successfully doped both n-type and p-type.

2.1.3 $CuInO_2$

$CuInO_2$ is a particularly interesting transparent conductor because it has been successfully doped both n-type and p-type. [3] Devices created with homojunctions are in general more desirable from the standpoint of device operation and process integration. $CuInO_2$ is doped n-type by the replacement of In^{3+} with Sn^{4+}, and p-type by the replacement of In^{3+} with Ca^{2+}. Neither n-$CuInO_2$ nor p-$CuInO_2$ is particularly conductive, 3.8 mS/cm and 2.8 mS/cm respectively. Transmittance in the visible region is

Table 2.2: Properties of p-type transparent conductors. Trans.: optical transmittance in the visible region; σ: conductivity; μ: mobility; p: carrier concentration; E_g: optical band gap.

Material	Trans. %	σ (S/cm)	p (cm^{-3})	μ (cm^2/Vs)	E_g (eV)
$AgCoO_2$ [7]	40-60	0.2			4.15
$BaCu_2S_2$ [8]	60-80	17	10^{19}	3.5	2.3
BaCuSF:K [9]		82			3.2
BaCuSeF:K [9]		43			3.0
$CuAlO_2$ [10]	70-80	0.3	2.7×10^{19}	0.13	3.5
$CuCrO_2$:Mg [7],[11]	30	220		<0.3	3.1
$CuGaO_2$ [12]	70-85	6.3×10^{-2}	1.7×10^{18}	0.23	3.6
$CuGa_{0.5}Fe_{0.5}O_2$ [7]	50-70	1			3.4
$CuInO_2$:Ca [3]	50-80	2.8×10^{-3}			3.9
$CuNi_{2/3}Sb_{1/3}O_2$:Sn [7]	60	5.0×10^{-2}			3.4
$CuScO_{2+x1}$ [7],[13] $CuScO_{2+x2}$ [7],[13] (x2>x1)	70 15	$\sim 5.0 \times 10^{-2}$ 20			3.3 3.3
$CuYO_2$:Ca [14]	40-50	1	$\sim 10^{19}$	<1	3.6
In_2O_3 80% [15],[16] $+Ag_2O$ 20%	34	4.4×10^{-2}		8.2	3.8-4.0
LaCuOS:Sr [17],[18]	60-70	20			3.1
LaCuOSe [19]		24	2×10^{19}	8.0	2.8
LaCuOSe:Mg [19]		140	2.2×10^{20}	4.0	2.8
NiO_{1+x} [20]	40	0.14	1.3×10^{19}		3.6-4.0
NiO:Li [21]	80	1.4			3.6-4.0
$SrCu_2O_2$ [22]	70-80	4.8×10^{-2}	6.1×10^{17}	0.46	3.3

50% to 80% . The bandgap is about 3.9 eV. Although $CuInO_2$ does not have impressive performance, it demonstrates the idea that one transparent material can support conduction of both electrons and holes. A transparent p-n junction has been made from bipolar $CuInO_2$. [23]

2.1.4 $CuScO_2$

$CuScO_2$ is a p-TCO of the delafossite crystal structure with a bandgap of 3.3 eV. [13] Stoichiometric $CuScO_2$ is an insulator. It is rendered conductive by oxygen intercalation. $CuScO_{2+x}$ has a rather frustrating trade off in that as films become more conductive through oxygen intercalation, they also become dark optically. The film color goes from nicely transparent to brown. The best conductivity is about 20 S/cm with a very low transmittance of about 15% in the visible portion of the electromagnetic spectrum. The best visible transmittance is about 70% with a conductivity of 50 mS/cm. This decrease in optical transparency with increasing conductivity is seen in other delafossites. The band structure of delafossites is such that the valence band maximum is at a low symmetry point. This means that some intra-valence band optical absorption is quantum mechanically allowed. This intra-valence band optical absorption is the cause of the decrease in optical transparency in delafossites. [24] [25]

2.1.5 NiO:Li

NiO has the rocksalt crystal structure with a bandgap of 3.6 eV [21] and an electron affinity of 1.4 eV. [26] Increased conductivity can be induced in NiO by acceptor doping. This can be accomplished intrinsically by the introduction of interstitial oxygen or Ni vacancies; or extrinsically via monovalent cation substitution. Typically, Li^+ is employed for monovalent cation substitution acceptor doping. [21] Other monovalent substitutional cations such as Na^+ can be used to dope NiO. [27] In principle, pentavalent substitutional anions such as N and P could also be used for NiO p-type doping, although this does not appear to have been reported in the literature. A conductivity of 1.4 S/cm with

80% transparency has been achieved in NiO:Li. Conduction in NiO may be described by a model known as correlated barrier hopping. [28] Correlated barrier hopping refers to charge carriers moving between defect centers by thermal excitation over the potential barrier separating the centers. This kind of conduction involves thermal activation of the mobility of the charge carriers, as opposed to the more familiar case of thermal excitation of carrier concentration, e.g., valence band holes from acceptor levels.

2.1.6 $BaCu_2S_2$

$BaCu_2S_2$ is a semi-transparent p-type conductor developed at OSU with a bandgap of 2.3 eV. [8] It is orange in color with 60% to 80% transparency in the visible portion of the electromagnetic spectrum. The conductivity is 17 S/cm, with a mobility of 3.5 cm^2/V-s and a hole concentration of 10^{19} cm^{-3}. $BaCu_2S_2$ is discussed further in Chapter 4.

2.1.7 Chemical Design of p-TCs

As researchers first sought to make p-TCs, oxides were the main focus. This is because n-TCs are oxide-based and thus oxide-based p-TCs would be most compatible, from a materials and processing standpoint, with well-known n-TCOs. From Table 2.2 it is seen that most of the oxide p-TCs contain Cu or Ag. [29] There are several reasons for this choice. First, these cations have closed d shells (e.g., Cu^{2+}, Ag^{+}, In^{+}, Sn^{2+}). This avoids the introduction of color into the material due to d-d transitions. Second, the energy level of the outer d shell of these cations is close to the $2p$ energy level of oxygen ions. It is shown experimentally that Ag and Cu are the best p-TC cation candidates because their d energy levels are closest to the O $2p$ energy level. [29] The metal d levels and oxygen $2p$ energy levels overlap, forming a mixed d - p valence band edge. This mixture means that the bonds are fairly covalent. Thus, localization of holes seen in ionically bonded materials which possess an O $2p$-derived valence band maximum is lessened in a more covalent p-d hybrid-derived valence band maximum

material, resulting in more hole delocalization. This leads to improved hole mobility and a larger conductivity.

This basic idea of cation/anion valence orbital overlap has been extended to utilize other chalcogens. p-TCs based on S, Se, and Te are being developed. [8],[30] p-TCs based on oxygen-sulfur (OS) and oxygen-selenium (OSe) mixtures have also been investigated. [12],[18],[19] Greater covalency in the metal d band and chalcogen p valence band overlap of these materials is expected because of the smaller electronegativity difference between, for example, Cu and S as compared to Cu and O. The hole mobility is expected to increase in oxysulfides and oxyselenides compared to oxides due to this increased covalency. [19]

Another idea that has been applied to p-TCs is the addition of F in an attempt to widen the band gap of some candidate p-TCs. [30] For example, $BaCu_2S_2$ has desirable electrical properties, but is not quite transparent in the visible portion of the electromagnetic spectrum (band gap of 2.3 eV). Thus, BaCuSF is an attempt to retain the desirable attributes of $BaCu_2S_2$ while improving transparency. [9] The addition of F widens the band gap because the high electronegativity of F pulls down the energy of the valence band, creating a wider gap. [30]

2.2 Thin-Film Transistors

This section describes the structure, fabrication and operation of thin-film transistors (TFTs). Materials issues related to the semiconductor channel region are discussed. Finally, transparent thin-film transistors (TTFTs) reported to date in the literature are summarized.

2.2.1 Thin-Film Transistor Structure and Fabrication

A TFT is built up from multiple amorphous or polycrystalline thin-film layers. Figure 2.1 shows examples of how a TFT might be constructed. The substrate is not necessarily a part of the device as with process technologies using bulk crystalline material as the starting point for devices (e.g., Si CMOS technology).

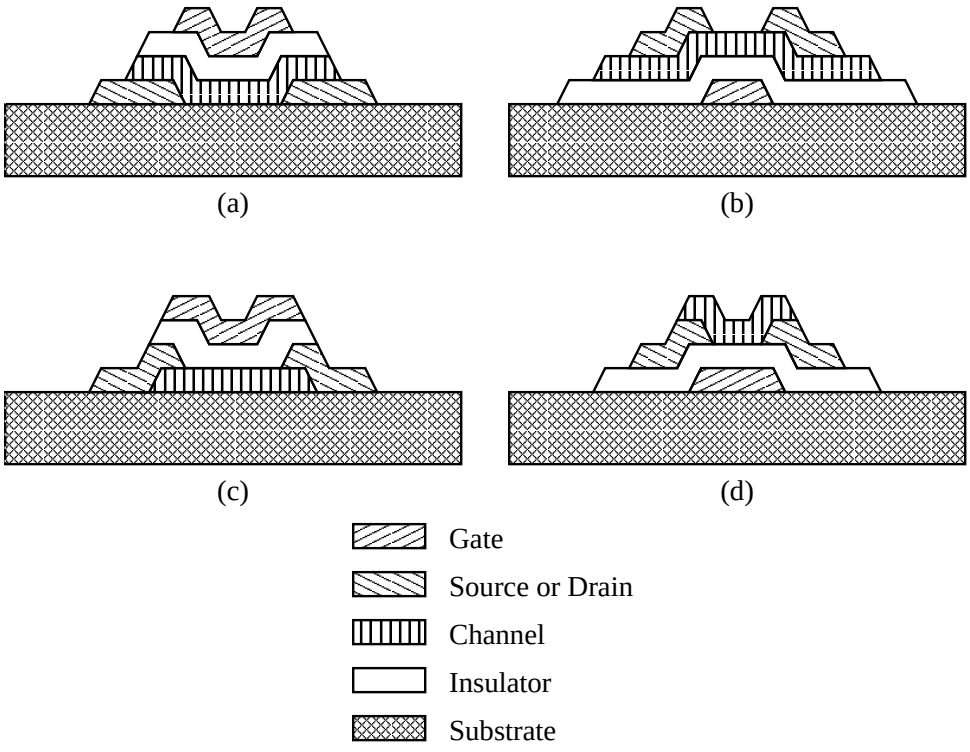


Figure 2.1: Four TFT structures: (a) staggered top-gate, (b) staggered bottom-gate, (c) co-planar top-gate, and (d) co-planar bottom-gate

Thin-film layers generally have inferior electrical properties compared to bulk crystal due to a larger number of defects. Undesirable surface effects are very influential on the operation of thin-film devices compared to bulk devices. [31] This is because the films are so thin that surface effects may extend across the entire film layer. Also, both top and bottom surfaces are influential to the operation of a thin-film device compared to the presence of only a single surface for a bulk device. The performance of TFTs is poor compared to single crystal devices because the carriers must traverse polycrystalline material. More carrier scattering occurs in a polycrystalline layer compared to a single crystal. This leads to a smaller carrier mobility.

2.2.2 TFT Operation

The TFT is a majority carrier field-effect transistor. There are no p-n junctions involved in the device operation. Operation is described for a p-channel TFT. A negative DC voltage is applied to the gate. A negative voltage is applied to the drain with respect to the source. Majority carrier holes injected into the channel material from the source and holes from the channel material itself are attracted to the interface of the channel layer with the gate insulator, forming a conduction channel. The carriers in the conduction channel are swept through the channel and collected at the drain. The more negative the gate voltage, the more carriers are attracted to the gate insulator/channel interface, and the transistor current is greater. Current increases with source to drain voltage at a given gate voltage until channel pinch-off occurs. At still greater source to drain voltages the transistor current saturates. For an enhancement-mode device (desirable), the channel conductance at zero gate voltage is zero and must be enhanced by applying a negative gate voltage. For a depletion-mode device (less desirable), there is channel conductance at zero gate voltage. The conductance may then be increased by applying a negative gate voltage or decreased by applying a positive gate voltage. A depletion-mode device is less desirable because it requires power to keep it in the off state. [31]

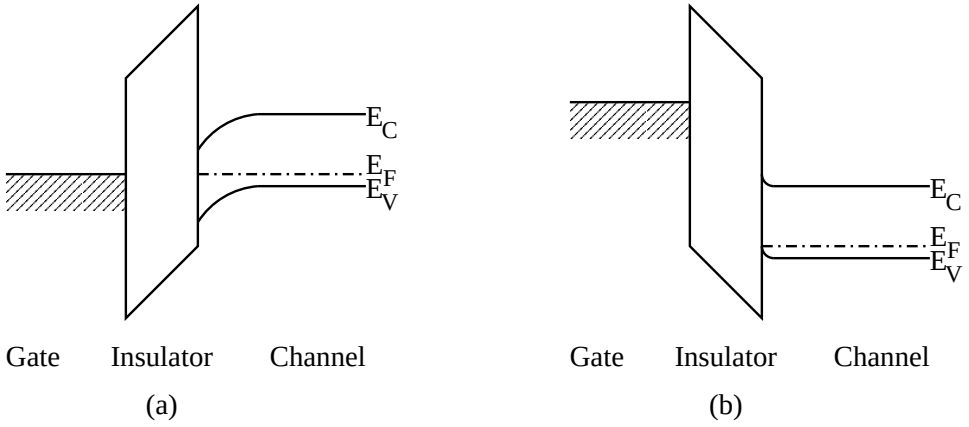


Figure 2.2: Energy band diagrams for TFT gate region where $\phi_m < \phi_s$: (a) equilibrium and (b) under positive bias.

Energy band diagrams helpful to the understanding of TFT operation may be drawn for two regions of the TFT. The first is the gate region, showing the interaction of the gate metal, gate insulator, and semiconductor. The second is the semiconductor/contact interface at either the source or the drain. Figure 2.2(a) is an equilibrium energy band diagram for the gate region of a p-channel TFT where the gate material has a work function smaller than the ionization potential of the semiconductor (as is the case for the transistors developed in this work). At zero gate bias, the semiconductor/insulator interface is depleted of holes, as may be seen by the larger separation of the Fermi level from the valence band at the surface as compared to in the bulk. As a negative gate bias is applied, the energy band diagram is that depicted in Fig. 2.2(b). The band bending has reversed, and the semiconductor/insulator interface has an accumulation of holes (a channel has formed), as may be seen by the smaller separation of the Fermi level from the valence band at the surface as compared to in the bulk. For energy band diagrams depicting the semiconductor-source/drain contact interface, see the discussion in Sec. 2.3.

2.2.3 TFT Channel Semiconductor Issues

The most desirable channel material for an ideal TFT (i.e., no interface states, no bulk traps) is a near-insulator. [31] With an ideal near-insulator, all conduction is due to injected charge forming a very thin channel layer at the semiconductor / gate insulator interface. There is no bulk leakage current. When the gate voltage is removed, the channel disappears and the conductance reduces to zero. However, in real TFT channel semiconductor thin-film layers, there are interface states and bulk traps that affect the operation of the TFT.

2.2.3.1 Interface States and Bulk Traps

Tickle [31] gives an equation to calculate the maximum number of carriers that may be injected or removed from the channel semiconductor by the gate capacitor,

$$n_{max} = \frac{\xi_{breakdown}\epsilon_{ins}}{q}, \tag{2.1}$$

where $\xi_{breakdown}$ is the electric field at which the gate insulator breaks down, ϵ_{ins} is the dielectric constant of the insulator, and q is the electronic charge constant.

n_{max} is approximately 10^{12} cm^{-2} to 10^{14} cm^{-2} for typical dielectric constants and dielectric breakdown fields on the order of a MV/cm. If the density of interface states or bulk traps is greater than n_{max}, the gate is incapable of increasing the channel mobile carrier concentration to a useful level, since all of the injected carriers are trapped in interface states or bulk traps. If the channel semiconductor has a large enough carrier concentration, these carriers can fill the interface states and bulk traps and gate modulation of the mobile carrier concentration in the channel may be possible. If the semiconductor is insulating to begin with, there are few semiconductor carriers to fill the interface states and bulk traps and gate modulation is not possible. [31]

2.2.3.2 Channel Conductivity

The ideal material for the channel semiconductor in a TFT is a near-insulator. If the channel semiconductor is too conductive, the conductivity of the channel is not ap-

preciably affected by application of a gate bias. As defined in Sec. 2.2.3.1, the maximum number of carriers that may be injected or removed from the channel semiconductor by the gate capacitor is n_{max}. The initial number of carriers in the channel under the gate is given by $N_{ch}t_{ch}$, where N_{ch} is the carrier concentration in the channel and t_{ch} is the channel thickness. If $N_{ch}t_{ch} > n_{max}$, the gate is not capable of appreciably changing the conductivity of the channel. In this case the possible increase in or variation of channel conductivity due to the modulation of the gate capacitor is insignificant compared to the existing bulk channel conductivity. The gate is only capable of decreasing the channel conductance by the application of a positive gate bias. This reverse bias increases the depletion region width in the semiconductor, eventually closing off the channel. Decreasing channel layer thin film thickness can help with this issue. Decreasing the channel layer thin film thickness decreases the initial bulk concentration of carriers in the channel, $N_{ch}t_{ch}$. In turn the value of n_{max} required to significantly increase the channel conductivity decreases.

In order to modulate the channel conductivity, the charge induced by the gate must be greater than the carrier charge in the channel that is present in the semiconductor under equilibrium. This consideration can be expressed quantitatively as [32],

$$V_g C_{ins} > q p_{chan} t_{chan}, \tag{2.2}$$

where V_g is the applied gate voltage, C_{ins} is the gate capacitance, q is the electronic charge constant, 1.6 x 10^{-19} C, p_{chan} is the bulk carrier concentration in the channel, and t_{chan} is the channel thickness. The threshold voltage (the minimum gate voltage required to form a conduction channel under the gate), V_t, may be obtained from this equation by solving for V_g,

$$V_t = \frac{q p_{chan} t_{chan}}{C_{ins}}. \tag{2.3}$$

The constraint on carrier concentration explicit in this equation is necessary but not sufficient to ensure successful operation of a TFT. If the induced carrier concentration in the thin-film transistor channel is too small, the interface states and bulk traps may

not be completely filled. In that case, the gate is incapable of controlling the TFT regardless of gate voltage, as described in Sec. 2.2.3.1.

2.2.4 Transparent Thin-Film Transistors (TTFTs)

Transparent thin-film transistors (TTFTs) described in the literature to date are all n-channel devices. Several n-channel TTFTs (n-TTFTs) based on ZnO have been reported.

The first report of a partially transparent n-TTFT was made in 1995 by Seager et al. [33] These n-TTFTs use In_2O_3 for the channel layer. Lead zirconate titanate is used as a ferroelectric insulator. These devices are developed as nonvolatile memory devices, hence the use of the ferroelectric insulator. Transparency is not a concern in this research. These devices are not truly transparent because they are fabricated on Si, using a Pt gate electrode and Pt source and drain contacts. The devices are bottom-gate, staggered TFTs. No traditional transistor characterization is reported for these devices, as they are intended as memory cells.

Another partially transparent n-TTFT was reported by Prins et al. in 1997. [34] Sb-doped SnO_2 is used for the channel semiconductor. Lead zirconate titanate is used as a ferroelectric insulator. A non-transparent $SrRuO_3$ gate is used. The devices are bottom-gate, co-planar TFTs. The devices are intended as transparent, thin-film memory field-effect transistors. No traditional transistor characterization is reported for these devices.

In 2003, several ZnO based n-TTFTs were reported. Matsuda et al. [35] made several different devices, of which one is truly transparent. The other devices are made on Si substrates which serve as the gate electrode. The transparent devices are made on glass, with a bottom-gate, staggered structure. ITO is used for the gate contact. A layered gate insulator of SiO_2 and SiN_4 is used. ZnO is used for the channel layer. Zn-doped In_2O_3 (IZO) is used for the source and drain contacts. It is reported that the SiN_4 layer in the gate insulator greatly reduced gate leakage current compared to

SiO_2 alone. Properties of the SiO_2 layer seem to be degraded by the deposition of ZnO onto it. The non-transparent devices have a drain current on-off ratio of $\sim 10^5$. The threshold voltage and channel mobility of non-transparent devices are 2.5 V and 0.031 cm^2/V-s or -1.0 V and 0.97 cm^2/V-s, depending on structure. Transparent devices are depletion-mode devices. They do not have good saturation characteristics. No value for channel mobility is reported for the transparent devices. The transparent devices have 80% optical transmission.

In 2003, Hoffman et al. reported n-TTFTs using ZnO for the channel material and Sn-doped In_2O_3 (ITO) for the source and drain contacts. [36] A bottom-gate, staggered structure is employed for this n-TTFT. The gate insulator is a superlattice of alternating layers of Al_2O_3 and TiO_2 (known as ATO). The gate contact is ITO. The transistors are made on glass. The transistors, including substrate, have an optical transmission of $\sim$75% in the visible portion of the electromagnetic spectrum. The threshold voltage reported is $\sim$10 V to 20 V and channel mobility $\sim$0.3 to 2.5 cm^2/V-s. The drain current on-to-off ratio is $\sim 10^7$. The transistors are enhancement-mode devices.

Another partially transparent n-TTFT based on ZnO was reported in 2003 by Carcia et al. [37] These transistors cannot be considered truly transparent because they are fabricated on Si, and because the transistors use non-transparent Ti-Au source and drain electrodes. The Si serves as the gate, and thermal SiO_2 as the gate insulator. The on-off drain current ratio for these devices is $\sim 10^6$. The channel mobility is $\sim$2 cm^2/V-s. The threshold voltage is 0 V.

2.3 Semiconductor Contacts

An important issue to understand in wide bandgap semiconductor devices is injecting contacts. A metal or highly conductive semiconductor may be applied to a semiconductor for the purpose of making an electrical contact that interfaces with an outside circuit. This topic is discussed in the context of a p-type semiconductor. Ideal metal-semiconductor contact theory is discussed first, followed by non-ideal theory.

2.3.1 Ideal Metal-Semiconductor Contacts

In ideal metal-semiconductor contact theory, a metal-semiconductor junction may form an Ohmic contact or a Schottky barrier. See Ref. [38], Chapter 14, and Ref. [39], Chapter 5, for a thorough discussion of metal-semiconductor contacts. The determining factor in whether a metal-semiconductor contact is a Schottky barrier or an Ohmic contact is the relative value of the metal work function, ϕ_m, and the semiconductor work function, ϕ_s (see Fig. 2.3(a)). For a p-type semiconductor, if $\phi_m > \phi_s$, the contact is ohmic (Fig. 2.3(b)). For an Ohmic contact, holes are able to flow freely under either a forward bias (positive bias to the p-type semiconductor) or a reverse bias (positive bias to the metal) from either the metal to the semiconductor, or from the semiconductor to the metal. If $\phi_m < \phi_s$, the metal-semiconductor contact forms a Schottky barrier (Fig. 2.3(c)). The Schottky barrier height for holes, ϕ_{Bp}, is given by

$$\phi_{Bp} = \frac{E_g}{q} - (\phi_m - \chi_s), \tag{2.4}$$

where E_g is the semiconductor bandgap and χ_s is the semiconductor electron affinity. For a Schottky barrier, holes are able to flow from the semiconductor to the metal under a forward bias. Under a reverse bias, there is a barrier to hole flow. For TTFT applications, it is desirable that metal-semiconductor contacts be Ohmic in character to ensure that the source and drain contacts have a low contact resistance regardless of bias conditions in the device. If the contact resistance is small, most of the applied drain-source voltage drops across the channel, as desired. A Schottky barrier contact has a high resistance.

In an ideal contact, charge balance across the metal-semiconductor interface can be expressed as

$$Q_m + Q_{sc} = 0, \tag{2.5}$$

where Q_m is the charge per unit area associated with the metal and Q_{sc} is the charge per unit area associated with the semiconductor.

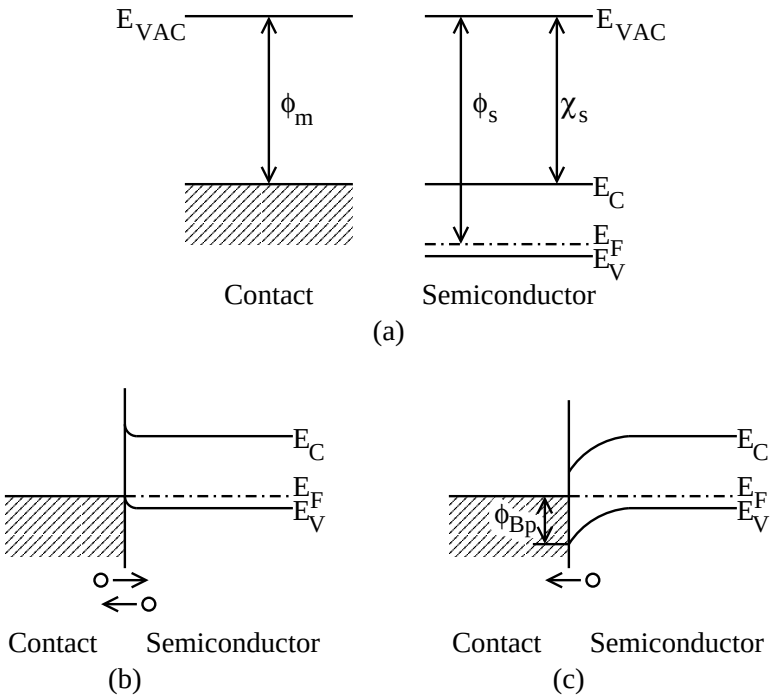


Figure 2.3: Metal-semiconductor contacts: (a) before contact is formed, (b) Ohmic contact, and (c) Schottky barrier contact. ϕ_m is the metal contact work function, ϕ_s is the semiconductor work function, and χ_s is the semiconductor electron affinity.

2.3.2 Non-Ideal Metal-Semiconductor Contacts

Regardless of the metal-semiconductor work function alignment, if there is a large density of interface states, the Fermi level at the semiconductor surface may be pinned at a given energy level in the band gap. For a non-ideal contact, charge balance across the metal-semiconductor interface can be expressed as

$$Q_m + Q_{sc} + Q_{ss} = 0, \tag{2.6}$$

where Q_{ss} is the charge per unit area associated with the interface states. If $Q_{ss} \gg Q_m$, Q_{sc}+$Q_{ss} \approx 0$ and the Fermi level is determined entirely by the interface states. Figure 2.4 illustrates how Fermi-level pinning can change the nature of a contact from an Ohmic contact to a Schottky barrier. In Fig. 2.4(a), an Ohmic metal-semiconductor contact is shown. In Fig. 2.4(b), the same contact is shown with the Fermi level pinned in the middle of the bandgap. The contact has become a Schottky barrier due to Fermi-level pin-

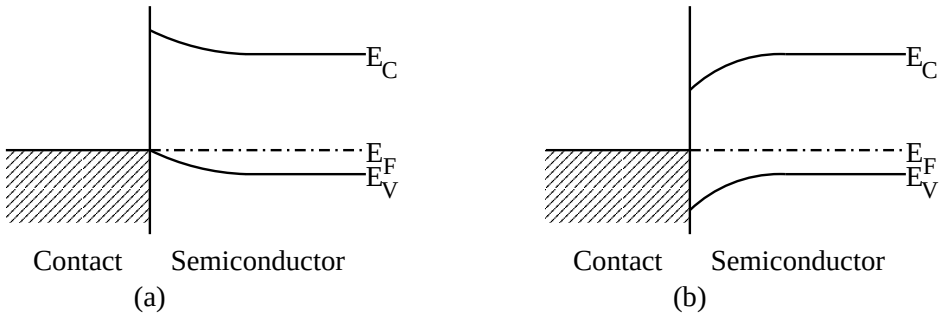


Figure 2.4: Metal-semiconductor contact (a) without Fermi-level pinning and (b) with the Fermi level pinned at the middle of the bandgap.

ning. In practice, Fermi-level pinning is present to some degree in metal-semiconductor contacts.

A pinning parameter, S, can be calculated to determine the degree of pinning in a barrier. S varies between 0 and 1, with 0 indicating strong pinning and 1 indicating no pinning. An empirical formula for S is given by [40]

$$S = \frac{1}{1 + 0.1(\epsilon_\infty - 1)^2}, \tag{2.7}$$

where ϵ_∞ is the high-frequency dielectric constant of the semiconductor. Using S, a more accurate calculation of the barrier height for holes, ϕ_{Bp}, can be made from [40]

$$\phi_{Bp} = (E_g + \chi_s - \phi_{CNL}) - S(\phi_m - \phi_{CNL}), \tag{2.8}$$

where ϕ_{CNL} is the charge neutrality level of the interface states measured from the vacuum level. ϕ_{CNL} is the energy below which interface states are filled and above which interface states are empty for a neutral surface. [40] If $S = 1$ (no pinning), the ideal Schottky barrier height is obtained,

$$\phi_{Bp} = E_g + \chi_s - \phi_m. \tag{2.9}$$

If $S = 0$ (strongly pinned), the Schottky barrier height is given as

$$\phi_{Bp} = E_g + \chi_s - \phi_{CNL}. \tag{2.10}$$

Returning to Eq. 2.8, it is evident that for a given metal with a known workfunction, ϕ_m, the non-ideal Schottky barrier height may be estimated if the bandgap, electron affinity, Fermi-level pinning factor, and charge neutrality level are known for the constituent material. The bandgap, E_g, of most common materials is known or can be estimated from optical absorption measurements. [41] Although the electron affinity, χ_s, is also known for many materials, this is a more difficult property to accurately determine. Thus, values of χ_s for a given material are often inconsistent, as reported in the literature. Photoemission measurements are commonly used to estimate χ_s, but a great deal of care must be taken to properly prepare the surface and perform such an experiment in order to unambiguously establish χ_s. In contrast, the pinning parameter, S, is easily determined from Eq. 2.7, if ϵ_∞ is known. Typically, ϵ_∞ is calculated as the square of the optical index of refraction. Finally, the charge neutrality level, ϕ_{CNL}, must be known in order to employ Eq. 2.8 to calculate the non-ideal Schottky barrier height.

Values of ϕ_{CNL} are determined by calculating the band structure of a material using a technique such as the tight binding method, then extracting ϕ_{CNL}. [40],[42] Values of the charge neutrality level, CNL, (measured from the top of the valence band) have been tabulated for only a limited number of materials. Some tabulated values of ϕ_{CNL} for wide-bandgap oxides can be found in Ref. [40]. Values of CNL for some III-V compounds, II-VI compounds, and a few other materials can be found in Ref. [42]. Van de Walle and Neugebauer [43] claim that ϕ_{CNL} (as measured from the vacuum level) is the same for all materials, and is approximately 4.5 eV. Van de Walle and Neugebauer claim that this value of 4.5 eV corresponds to the energy level where hydrogen, in a host material, transitions from donor to acceptor behavior. They term this the universal hydrogen level, $\epsilon(+/-)$.

In an effort to test the viability of this concept of a universal charge neutrality level, Table 2.3 is constructed. Table 2.3 shows materials with values for electron affinity, bandgap, and calculated charge neutrality level relative to the valence band. The value

of ϕ_{CNL} (measured from the vacuum level) is calculated from

$$\phi_{CNL} = \chi + E_g - CNL, \tag{2.11}$$

where χ is the electron affinity, and E_g is the bandgap. The difference from the universal hydrogen level at 4.5 eV, $\epsilon(+/-)$, is also shown in the table. It is noted in the construction of this table that there is often considerable disagreement among references for the values of electron affinity. This disagreement is due to the complicated nature of the surface photoemission measurements used to determine electron affinity. Surface conditions (orientation, cleanliness) can significantly affect the measurement results. This should be taken into account when considering this table. As seen from Table 2.3, the universal hydrogen/CNL level proposed by Van de Walle and Neugebauer seems to be in reasonable agreement with the materials assessed (in the tabulated examples, the error is typically less than 10%). Although the existence of a universal charge neutrality level is a new idea that has not been fully debated, calculations appearing later in this thesis employ this assumption that $\phi_{CNL} = \epsilon(+/-) = 4.5$ eV.

In terms of forming an Ohmic contact, a way to circumvent the problem of Fermi-level pinning creating a Schottky barrier is to dope the semiconductor surface heavily so that a tunneling contact is formed (see Ref. [38], Chapter 14). For heavy surface doping, there is strong band bending at the semiconductor surface, creating a barrier so narrow that carriers can tunnel through, forming an Ohmic contact (see Fig. 2.5).

2.3.3 Injecting Contacts

Ohmic contacts are typically discussed in the context of narrow or moderate bandgap semiconductors, which have bandgaps less than ∼1.5-2.0 eV. Ohmic contacts are characterized by bulk-limited transport, not injection-limited transport which is applicable when the metal contact cannot adequately supply the required number of carriers to maintain the space charge neutrality condition required to sustain bulk-limited transport. Moreover, Ohmic contacts to narrow/moderate bandgap materials produce

Table 2.3: ϕ_{CNL} for various materials and comparison to $\epsilon(+/-)$. χ is the electron affinity, E_g is the bandgap, CNL is the charge neutrality level measured from the valence band, ϕ_{CNL} is the charge neutrality level measured from the vacuum level, and $\epsilon(+/-)$ is the proposed universal hydrogen level at 4.5 eV of Van de Walle and Neugebauer.

Material	χ (eV)	E_g (eV)	CNL (eV)	ϕ_{CNL} (eV)	$\phi_{CNL} - \epsilon_{(+/-)}$(eV)	Error (%)
Al_2O_3	1.0 [40]	8.8 [40]	5.5 [40]	4.3	-0.2	-4.4
AlN	1.9 [44]	6.0 [45]	2.97 [42]	4.93	0.43	9.6
$BaTiO_3$	3.9 [46]	3.3 [46]	2.6 [46]	4.6	0.1	2.2
CdS	4.0 [47]	2.4 [47]	1.93 [42]	4.47	-0.03	-0.7
CdTe	1.4 [48]	4.3 [48]	1.12 [42]	4.58	0.08	1.8
GaAs	4.07 [39]	1.42 [39]	0.52 [42]	4.97	0.47	9.4
GaN	3.3 [49]	3.2 [50]	2.37 [42]	4.13	-0.37	-8.2
GaSb	4.06 [50]	0.73 [50]	0.16 [42]	4.63	0.13	2.8
Ge	4.0 [39]	0.66 [39]	-0.28 [42]	4.94	0.44	8.9
HfO_2	2.5 [46]	5.8 [46]	3.7 [46]	4.6	0.1	2.2
InP	4.35 [50]	1.35 [50]	0.86 [42]	4.84	0.34	7.0
$LaAlO_3$	2.5 [46]	5.6 [46]	3.8 [46]	4.3	-0.02	-4.4
La_2O_3	2 [46]	5.5 [51]	2.4 [46]	5.1	0.6	10.7
$PbZrO_3$	3.2 [46]	3.7 [46]	2.6 [46]	4.3	-0.2	-4.4
Si	4.05 [39]	1.1 [39]	0.3 [42]	4.85	0.35	7.2
$SrTiO_3$	3.9 [40]	3.3 [40]	2.6 [40]	4.6	0.1	2.2
Ta_2O_5	3.3 [46]	4.4 [46]	3.3 [46]	4.4	-0.1	-2.2
TiO_2	3.9 [40]	3.05 [40]	2.2 [40]	4.75	0.25	5.3
Y_2O_3	2 [40]	5.6 [52]	2.4 [40]	5.2	0.7	12.5
ZnS	3.0 [53]	3.68 [54]	2.05 [42]	4.63	0.13	2.4

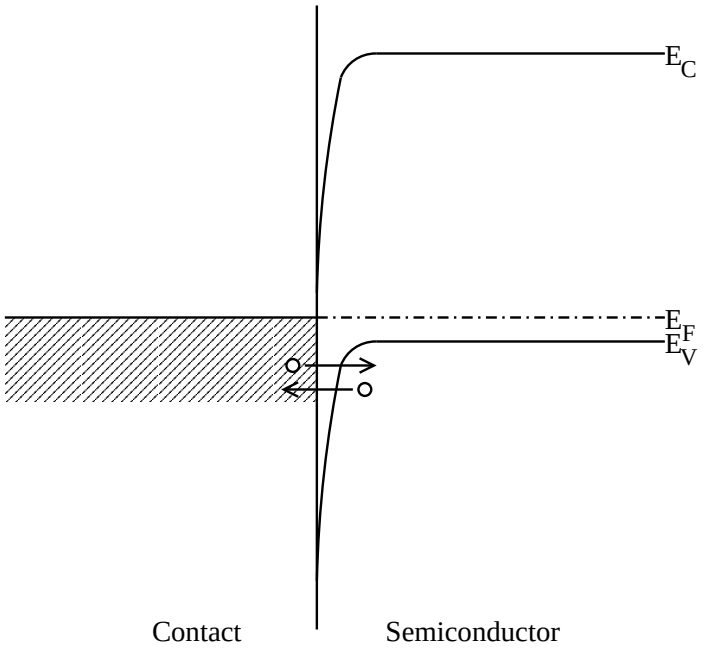


Figure 2.5: Energy band diagram depicting tunneling through a Schottky barrier for a metal-semiconductor contact with the semiconductor surface heavily doped.

linear current-voltage characteristics with a large slope (signifying small resistance). The contact resistance is small compared to the bulk resistance of the semiconductor. [39]

Figure 2.6 depicts a lumped-parameter resistor model for a wide-bandgap, insulating semiconductor with contacts. R_c represents a voltage-dependent contact resistance. R_{sp} represents a voltage-dependent spreading resistance. R_b represents the bulk resistance of the semiconductor. $R_{measured}$ is given by [55]

$$R_{measured} = 2R_c + 2R_{sp} + R_b. \tag{2.12}$$

$R_{measured}$ is found experimentally by passing a current through the semiconductor and measuring the voltage across the contacts, $R_{measured} = V/I$. In wide-bandgap, insulating semiconductors (such as used in TTFTs), linear current-voltage characteristics such as that expected for an Ohmic contact may be obtained even when contact injection is extremely poor, since the bulk semiconductor resistance is much larger than the contact resistance.

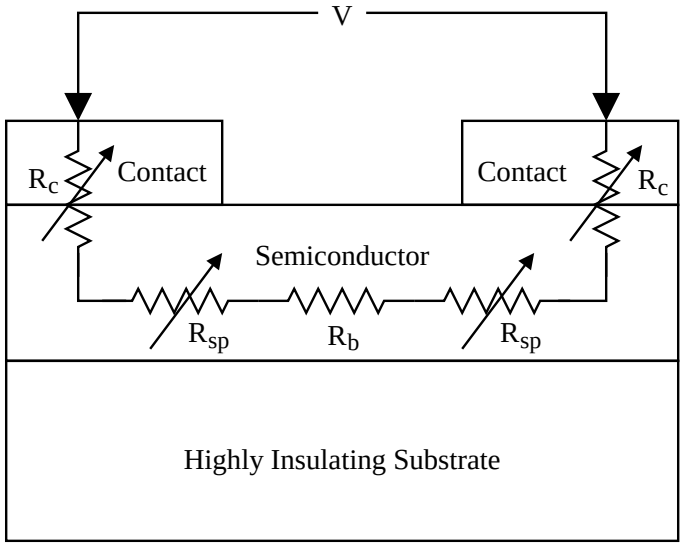


Figure 2.6: Contacts to a semiconductor showing contact resistance R_c, spreading resistance R_{sp}, and bulk semiconductor resistance R_b.

To illustrate this point, an example is given comparing the bulk resistance of narrow-bandgap Si to that of wide-bandgap ZnS. Bulk resistance is given by

$$R_b = \frac{\rho L}{A}, \tag{2.13}$$

where ρ is the semiconductor resistivity, L is the length of the semiconductor, and A is the cross-sectional area of the semiconductor. For both semiconductors, L is chosen as 0.1 cm, and A is chosen as 10^{-5} cm^2. For n-type Si with a carrier concentration of 10^{17} cm^{-3}, $\rho \sim 10^{-1}$ Ω-cm. [38] For ZnS, $\rho \sim 10^{10}$ Ω-cm. [56] Calculating R_b gives $R_{b,Si} = 10^3$ Ω and $R_{b,ZnS} = 10^{14}$ Ω. If the voltage-dependent, non-linear contact resistance is greater than 10^3 Ω in this example, current-voltage characteristics from the Si sample will be non-linear due to the dominance of the non-linear contact resistance. In contrast, the current-voltage characteristics for the ZnS sample will always be linear due to the dominance of the linear bulk resistance.

Because the contact issue outlined above for wide-bandgap semiconductors prevents standard contact characterization, a contact to a wide-bandgap insulating semi-

conductor is best characterized by how it functions as a source/drain contact in a TFT. If a contact material is successful in providing carriers to a wide-bandgap, insulating semiconductor TFT channel, that contact may be termed an injecting contact.

2.4 Conclusions

This chapter presents background information useful for understanding the research results presented in this thesis. Properties of n-type and p-type transparent conductors are tabulated and discussed, including the chemical design of p-type transparent conductors. The fabrication and operation of TFTs is explained. Materials issues related to using a wide-bandgap semiconductor as the channel layer in a TFT are discussed. Reports of TTFTs in the literature are summarized. Contacts to semiconductors are discussed, with an emphasis on Fermi-level pinning and contacts to wide-bandgap semiconductors.

3. EXPERIMENTAL TECHNIQUE

Experimental techniques used in this thesis research are discussed in this chapter. Several thin-film processing and thin-film characterization techniques are described. Finally, transistor characterization is discussed.

3.1 Thin-film Processing

This section describes thin-film deposition and post-deposition processing methods. Radio-frequency and direct-current sputtering are discussed. Plasma-enhanced chemical vapor deposition is explained. Thermal evaporation is examined. Rapid thermal processing of thin-films is described.

3.1.1 RF Sputtering

$BaCu_2S_2$ films used in this work are deposited by RF sputtering, using a CPA RF magnetron sputtering system. A solid source material is attached to the sputter power source. A thin film substrate is placed opposite the sputter source. A gas flow is set up in the deposition chamber, and an RF power source is applied to create a glow discharge plasma. The energy from the power source is coupled to charged species in the plasma (a small number of electrons and positive ions). The electrons gain most of the energy because of their much lighter mass as compared to the ions. These electrons and ions accelerate rapidly and undergo collisions. Many types of collisions occur. Collisions of an electron with an atom resulting in the promotion into an excited state and subsequent relaxation of an electron in the atom lead to the colored glow of a plasma. As excited electrons relax, they emit photons of a characteristic color in the visible region of the electromagnetic spectrum. Some of the collisions result in the creation of more ion/electron pairs. It is ions and electrons in the plasma that lead to sputtering. The ions and electrons are accelerated in opposite directions by the electric field from the power supply. A net negative charge builds up on each electrode because electrons are

faster than positive ions. As positive ions approach the sputter target they accelerate tremendously due to the electric field/net negative charge on the surface. When ions strike the target surface, they knock atoms off the target surface. Some of these atoms reach the substrate and produce the desired thin film. The substrate may be heated during deposition to improve crystallinity, giving energy to atoms landing on the substrate to help them find lattice positions. See Ref. [57] for more information on RF sputtering.

3.1.2 DC Ion Beam Sputtering

NiO and Ni films used in this work are deposited by DC ion beam sputtering using a Veeco 6-inch ion beam sputtering system. This sputter tool uses a DC power source. A heated cathode filament emits electrons which are accelerated in a magnetic field. These electrons strike gas atoms, creating a glow discharge plasma. The plasma is confined to a can that sits above the target/substrate chamber. A large DC potential is applied from the plasma can to the target/substrate chamber ($\sim$750 V). Positive gas ions are accelerated down into the target/substrate chamber. These ions pass through collimating grids on the way to the chamber. The ions strike the target surface and knock atoms out of the target. These target atoms deposit in the chamber, some of them onto the substrate. The sputter tool also has a hot neutralizer filament near the target that emits electrons in order to neutralize positive ion charge. This filament is used to prevent charge buildup on the target, reducing current and heating through the target. See Ref. [57] for more information on DC sputtering.

3.1.3 Plasma-Enhanced Chemical Vapor Deposition

SiO_2 gate insulator films used in this work are deposited by plasma-enhanced chemical vapor deposition (PECVD) using a Semi Group PECVD system. SiH_4 and N_2O gases flow into the reaction chamber. The chamber is heated to 300 °C. A radio frequency power supply creates a plasma in the chamber. The gases react and form SiO_2 on the hot substrate. See Ref. [57] for more information on PECVD.

3.1.4 Thermal Evaporation

Au and Zn films used in this work are deposited by thermal evaporation. In thermal evaporation, a thin film is deposited by heating the source material in a container using an electrical current. When sufficiently heated, the source material evaporates, depositing on the sample substrate. See Ref. [58] for more information on thermal evaporation.

3.1.5 Rapid Thermal Processing

Rapid thermal processing (RTP) is used to improve the crystallinity of deposited thin films. Rapid thermal processing involves rapidly increasing the temperature of a film to the desired temperature, exposing the film to this elevated temperature for a short time, and finally rapidly decreasing the film temperature back to room temperature. RTP gives atoms the energy to move into lattice positions. Rapid heating and cooling minimizes interdiffusion between film layers. During the anneal, gas flows through the chamber. Argon or nitrogen gases are used to prevent the film from reacting with the ambient air, minimizing oxidation and other unwanted reactions. Oxygen gas may be used to further oxidize a film or to prevent the loss of oxygen from the film. See Ref. [57] for more information on RTP.

3.2 Thin-film Characterization

This section covers techniques used to characterize electrical and optical properties of thin films. Hall measurements are described. Optical transmittance characterization is discussed. The hot-point probe measurement is explained.

3.2.1 Hall Measurements

Hall measurements in conjunction with resistivity measurements can be used to determine Hall mobility, carrier concentration, and resistivity of a material. The Hall effect describes the motion of a carrier in an applied magnetic field, B. When a carrier moves in a perpendicular direction to an applied magnetic field (current I), the Lorentz

force acts on the carrier in a direction perpendicular to both the magnetic field and the direction of carrier motion. The Lorentz force affects the direction of carrier motion, deflecting carriers from their original path. This creates a potential drop (the Hall voltage, V_H) across the sample that does not exist without the magnetic field. The Hall voltage can be measured and the carrier concentration p in the material determined from

$$p = \frac{IB}{qtV_H}, \tag{3.1}$$

where t is the sample thickness. [55]

The material resistivity may be determined using the van der Pauw technique. In this technique the sheet resistance of the material R_s is measured. The material resistivity may then be found from

$$\rho = R_s t. \tag{3.2}$$

Once the Hall voltage and material resistivity are known, the Hall mobility of a material may be calculated from [55]

$$\mu_H = \frac{V_H}{R_s IB}. \tag{3.3}$$

For a more thorough discussion of Hall measurements, see Ref. [55].

3.2.2 Optical Transmittance and Optical Bandgap Measurements

Optical transmittance is used in this work to measure the transparency of thin films and to determine the optical bandgap of materials. For the optical bandgap measurement, the absorption spectrum is needed. The absorption spectrum, A, is obtained from the transmittance spectrum, T, from $A = 1 - T$. Next, the optical absorption coefficient, α, is determined from

$$\alpha = \frac{1}{t} \ln \left[\frac{1}{1 - A} \right] \tag{3.4}$$

where t is the film thickness. A and in turn α are functions of photon energy, hν. Plots of $(\alpha h\nu)^2$ versus $h\nu$ and $(\alpha h\nu)^{1/2}$ versus $h\nu$ are made, as indicated in Fig. 3.1. The linear portion of the plot of $(\alpha h\nu)^2$ versus $h\nu$ may be extrapolated to the $h\nu$ axis for an

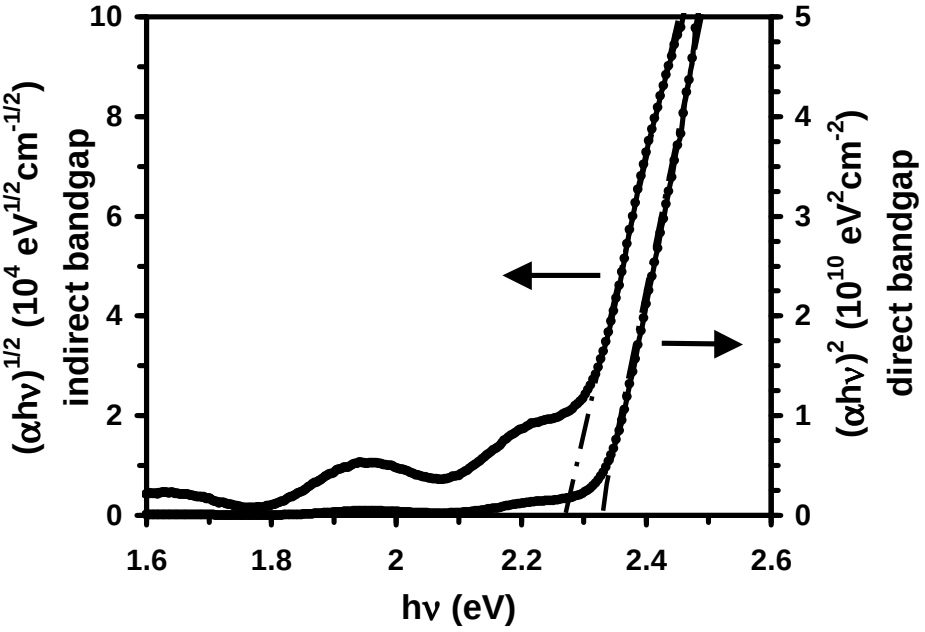


Figure 3.1: $(\alpha h\nu)^{1/2}$ versus $h\nu$ and $(\alpha h\nu)^2$ versus $h\nu$ plots for determining the optical indirect and direct bandgaps of a material.

estimate of the direct bandgap. The linear portion of the plot of $(\alpha h\nu)^{1/2}$ versus $h\nu$ may be extrapolated to the $h\nu$ axis for an estimate of the indirect bandgap. See Ref. [41] for a thorough explanation of this technique.

3.2.3 Hot Point Probe

The hot point probe is a quick method to determine if a semiconductor or thin film is n-type or p-type. The setup requires a heated probe and an unheated probe connected to an ammeter. The two probes are placed on the sample surface. Carriers near the hot probe gain thermal energy from the heat and move away from the hot probe, leaving a net charge near the probe. For a p-type material, negative charge exists near the hot probe. For an n-type material, the charge is positive. This charge separation results in a voltage and thus a current, which is detected by the ammeter. The sign of the current indicates whether the semiconductor is n-type or p-type. [38]

3.3 Device Characterization

TFTs may be characterized by commonly quoted properties and figures of merit. These include current-voltage plots, threshold voltage, transconductance, output conductance, and effective mobility.

3.3.1 Current-Voltage Measurements

A family of DC drain current versus drain voltage curves at various gate voltage values is commonly created to characterize a transistor. Current-voltage measurements made in this work are obtained using an HP 4140B picoammeter.

3.3.2 Mobility and Threshold Voltage Extraction

Mobility and threshold voltage can be estimated from a plot of I_d versus V_{ds} at a given V_{gs}. In the triode region of TFT operation ($V_{ds} < V_{dsat}$), the estimated mobility is called the effective mobility, μ_{eff}. μ_{eff} is a function of the electric field from source to drain. In the saturation region of TFT operation ($V_{ds} > V_{dsat}$), the estimated mobility is called the saturation mobility, μ_{sat}, and is different from μ_{eff}. μ_{sat} is different because in saturation carriers must pass through the pinch-off region, which has different properties than the rest of the channel. μ_{eff} is a better estimate of the mobility. [55] In practice, μ_{eff} and μ_{sat} are similar in value. The method for estimating μ_{eff} and threshold voltage, V_t, is described first for the triode region of TFT operation and secondly for the saturation region of TFT operation.

The ideal drain current equation in the triode region for a TFT is given by

$$I_d = \mu_{eff} C_{ins} \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right], \tag{3.5}$$

where μ_{eff} is the effective channel mobility, C_{ins} is the gate capacitance, W is the channel width, L is the channel length, V_{gs} is the applied gate-to-source voltage, V_{ds} is the applied drain-to-source voltage, and V_t is the threshold voltage for the formation of the channel. The truly linear regime of TFT operation occurs when $V_{gs} - V_t \gg V_{ds}$, and

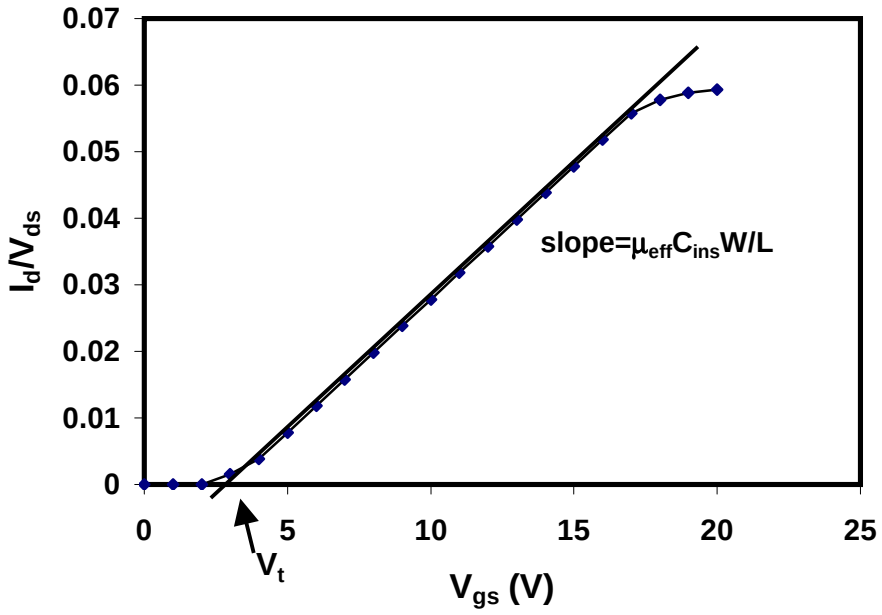


Figure 3.2: I_d/V_{ds} versus V_{gs} plot for TFT mobility and threshold voltage extraction in the triode region.

the squared term can be neglected,

$$I_d = \mu_{eff} C_{ins} \frac{W}{L} (V_{gs} - V_t) V_{ds}. \tag{3.6}$$

From a plot of I_d/V_{ds} versus V_{gs} the threshold voltage and effective mobility can be estimated. Such a plot has a slope of $\mu_{eff} C_{ins} \frac{W}{L}$, resulting in,

$$\mu_{eff} = \frac{slope}{C_{ins} \frac{W}{L}}. \tag{3.7}$$

Additionally, as shown in Fig. 3.2, V_t is estimated as the x-axis intercept of the linearly extrapolated portion of the I_d/V_{ds} versus V_{gs} curve.

The ideal drain current equation in the saturation region (square law theory) for a TFT is

$$I_d = C_{ins} \mu_{sat} \frac{W}{2L} (V_{gs} - V_t)^2. \tag{3.8}$$

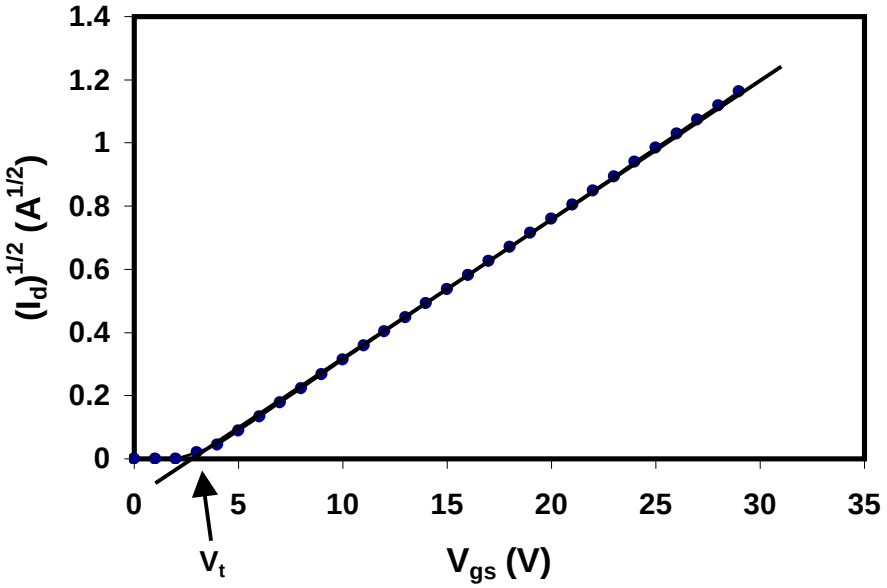


Figure 3.3: $I_d^{1/2}$ versus V_{gs} plot for TFT mobility and threshold voltage extraction in the saturation region.

From a plot of $I_d^{1/2}$ versus V_{gs}, the threshold voltage and saturation mobility can be estimated. The plot yields a slope of $(\mu_{sat} C_{ins} \frac{W}{2L})^{1/2}$, resulting in,

$$\mu_{sat} = \frac{slope^2}{2C_{ins}\frac{W}{L}}. \tag{3.9}$$

Also, as shown in Fig. 3.3, V_t is estimated as the x-axis intercept of the linearly extrapolated portion of the $I_d^{1/2}$ versus V_{gs} curve.

3.3.3 Transconductance and Output Conductance

Other common figures of merit for a TFT are transconductance and output conductance. Transconductance specifies the gain of the output current of the TFT with respect to the input voltage. The magnitude of the output conductance in the saturation region gives an indication of how well the TFT saturates. Mobility can also be estimated from the measured transconductance or output conductance.

Transconductance, g_m, is defined as the change in output current for a change in input voltage at a constant drain voltage,

$$g_m = \left.\frac{dI_d}{dV_{gs}}\right|_{V_{ds}=const}. \tag{3.10}$$

In the linear region Eq. 3.6 may be differentiated with respect to V_{gs} to obtain

$$g_m = \mu_{FE} C_{ins} \frac{W}{L} V_{ds}, \tag{3.11}$$

where μ_{FE} is the field effect mobility. [55] μ_{FE} is generally less than μ_{eff} because the dependence of mobility on the electric field is neglected in the derivation of g_m. μ_{FE} may be found, using the measured linear region transconductance, from

$$\mu_{FE} = \frac{g_m}{C_{ins}\frac{W}{L}V_{ds}}. \tag{3.12}$$

In the saturation region, Eq. 3.8 may be differentiated with respect to V_{gs}, which yields

$$g_m = \mu_{sat} C_{ins} \frac{W}{L}(V_{gs} - V_t). \tag{3.13}$$

μ_{sat} may be found, using the measured saturation region transconductance, from

$$\mu_{sat} = \frac{g_m}{C_{ins}\frac{W}{L}(V_{gs} - V_t)}. \tag{3.14}$$

Output conductance, g_d, is defined as the change in output current for a change in output voltage at a constant gate voltage,

$$g_d = \left.\frac{dI_d}{dV_{ds}}\right|_{V_{gs}=const}. \tag{3.15}$$

In the linear region, Eq. 3.6 may be differentiated with respect to V_{ds}, resulting in

$$g_d = \mu_{eff} C_{ins} \frac{W}{L}(V_{gs} - V_t). \tag{3.16}$$

μ_{eff} may be found, using the measured linear region output conductance, from

$$\mu_{eff} = \frac{g_d}{C_{ins}\frac{W}{L}(V_{gs} - V_t)}. \tag{3.17}$$

In the saturation region, Eq. 3.8 may be differentiated with respect to V_{ds}, obtaining (ideally),

$$g_d = 0. \tag{3.18}$$

In actuality, g_d is non-zero. A g_d of zero implies a saturated I_d versus V_{ds} curve with zero slope. Real devices exhibit some finite slope due to conduction in the bulk portion of the TFT channel or due to channel length modulation. To account for this non-ideality, channel length modulation is included in expression for I_d,

$$I_d = C_{ins}\mu_{sat}\frac{W}{2L}(V_{gs} - V_t)^2(1 + \lambda V_{ds}), \tag{3.19}$$

where λ is known as the body effect parameter. For the non-ideal case in saturation, g_d is obtained by differentiating Eq. 3.19 with respect to V_{ds},

$$g_d = \lambda C_{ins}\mu_{sat}\frac{W}{2L}(V_{gs} - V_t)^2. \tag{3.20}$$

In this section several methods have been described to calculate various transistor mobilities. These mobilities should be similar in value. μ_{eff} can be obtained from either the linear region I_d versus V_{ds} curves or from a measured value of the linear region output conductance. μ_{sat} can be found from the measured saturation region transconductance. μ_{FE} may be found from the measured linear region transconductance.

3.4 Conclusions

This chapter covers experimental techniques used in this research. Various thin-film deposition and processing methods are explained. Thin-film characterization techniques are reviewed. Finally, TFT characterization is described.

4. BARIUM COPPER SULFIDE THIN FILMS

This chapter describes work on $BaCu_2S_2$ thin films. Deposition, processing and characterization of $BaCu_2S_2$ films are discussed. Cu(In,Ga)Se_2 solar cells are described. A new p-i-n solar cell and the potential use of $BaCu_2S_2$ in this new cell are explained.

4.1 $BaCu_2S_2$ Thin-film Processing and Characterization

RF-sputtered $BaCu_2S_2$ thin films are developed as a candidate p-type transparent semiconductor. [8] To synthesize $BaCu_2S_2$, $BaCO_3$ and CuS powders are mixed and placed in H_2S at 650°C for 1 hour, then cooled to room temperature under flowing Ar gas. The resulting $BaCu_2S_2$ powder is pressed and sintered at 775°C into a 2" sputter target. $BaCu_2S_2$ targets used in this research were prepared by Sangmoon Park and Cheol-Hee Park, both in the Department of Chemistry at Oregon State University. Both α (orthorhombic crystal structure) and β (tetragonal crystal structure) $BaCu_2S_2$ films are fabricated in this work. α and β-$BaCu_2S_2$ are confirmed to be p-type by hot-point probe.

α-$BaCu_2S_2$ films are sputtered in 80 sccm of Ar/He (60% / 40%) at 35 mTorr at a substrate temperature of ~300°C, and an RF power of 45 W. A subsequent 5 minute rapid-thermal anneal is performed at 300°C in Ar. The resulting α-$BaCu_2S_2$ thin films are orange in color. X-ray diffraction (XRD) is used to confirm that the films are α-$BaCu_2S_2$. Figure 4.1 (top plot) shows an XRD pattern from a Siemens D-500 x-ray diffractometer for a α-$BaCu_2S_2$ thin film produced in this work. Figure 4.1 (bottom plot) shows an XRD pattern for α-$BaCu_2S_2$ powder taken from the ICSD XRD pattern database. Good match of the two patterns is observed, confirming that the thin film is α-$BaCu_2S_2$.

Optical transmission in the visible portion of the electromagnetic spectrum is 60% to 80%. The optical transmission spectrum of α-$BaCu_2S_2$ is illustrated in Fig. 4.2. The optical direct band gap for α-$BaCu_2S_2$ is estimated at 2.3 eV by using an $(\alpha h\nu)^2$

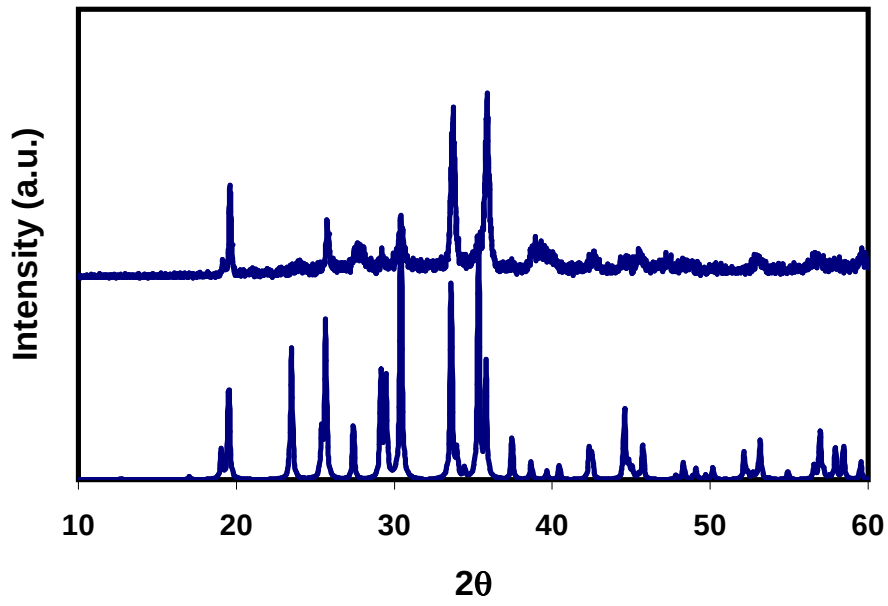


Figure 4.1: Top: XRD pattern for an α-$BaCu_2S_2$ thin-film fabricated in this work. Bottom: XRD pattern from the ICSD x-ray pattern database for α-$BaCu_2S_2$ powder.

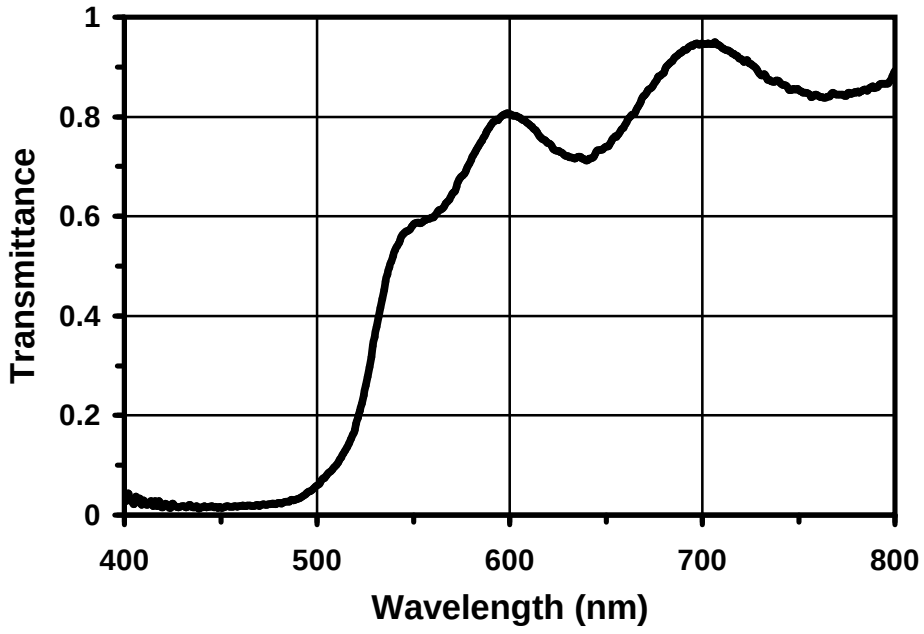


Figure 4.2: α-$BaCu_2S_2$ transmittance in the visible portion of the electromagnetic spectrum for a 430 nm-thick thin film.

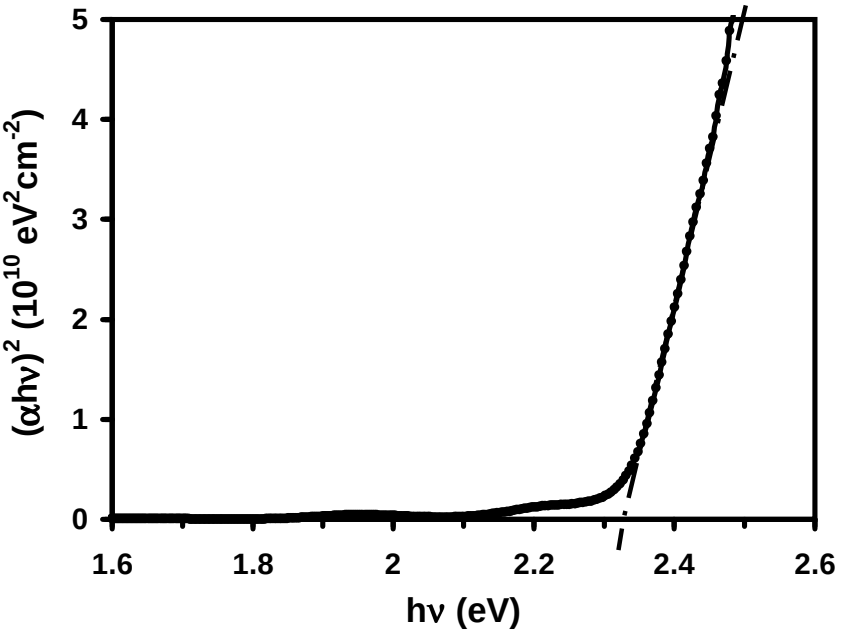


Figure 4.3: α-$BaCu_2S_2$ direct bandgap estimate from plot of $(\alpha h\nu)^2$ versus $h\nu$ for a 430 nm-thick thin film.

absorption edge plot as shown in Fig. 4.3. Hall measurements give a conductivity of ∼17 S/cm and a Hall mobility of 3.5 cm^2/V-s.

β-$BaCu_2S_2$ thin films are sputtered using the same parameters as α-$BaCu_2S_2$ except the substrate temperature is increased to ∼400°C during deposition. The as-deposited films are orange α-$BaCu_2S_2$. The films convert to β-$BaCu_2S_2$ during rapid thermal annealing. Rapid thermal annealing at 650°C in Ar for 5 minutes turns these films green. X-ray diffraction is used to confirm the films are β-$BaCu_2S_2$. Figure 4.4 (top plot) shows an XRD pattern from a Siemens D-500 x-ray diffractometer for a β-$BaCu_2S_2$ thin film produced in this work. Figure 4.4 (bottom plot) shows an XRD pattern for β-$BaCu_2S_2$ powder taken from the ICSD XRD pattern database. Good match of the two patterns is observed, confirming that the thin film is β-$BaCu_2S_2$.

Figure 4.5 is an optical transmittance plot for β-$BaCu_2S_2$. Optical transmittance in the visible portion of the electromagnetic spectrum is 10% to 50%. The optical direct

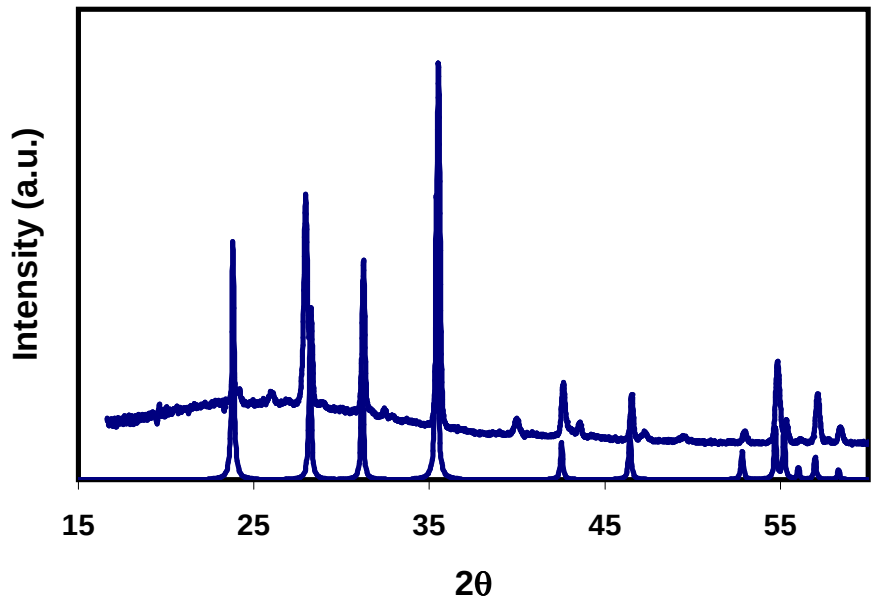


Figure 4.4: Top: XRD pattern for a β-$BaCu_2S_2$ thin-film fabricated in this work. Bottom: XRD pattern from the ICSD x-ray pattern database for β-$BaCu_2S_2$ powder.

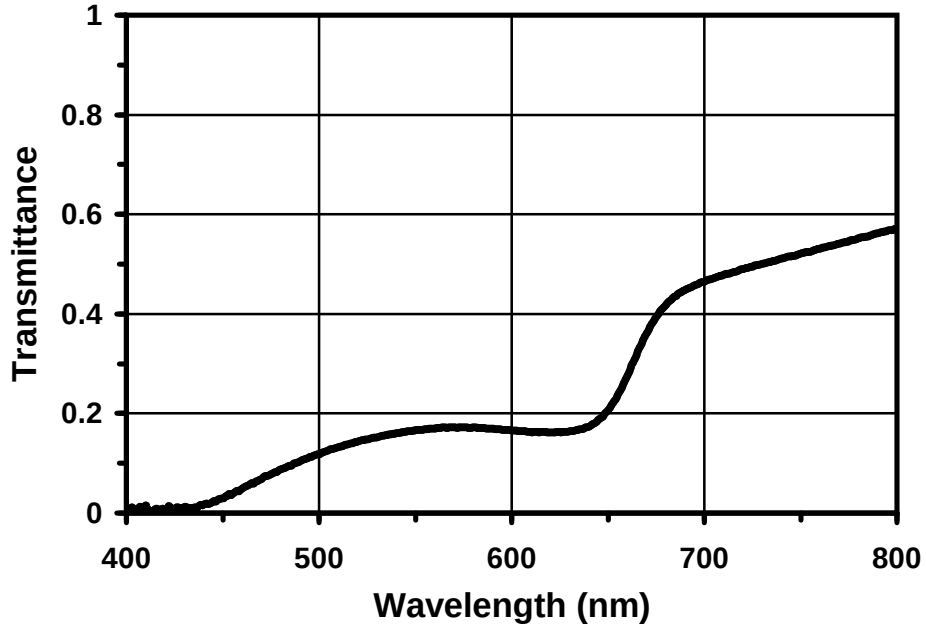


Figure 4.5: β-$BaCu_2S_2$ transmittance in the visible portion of the electromagnetic spectrum for a 450 nm-thick thin film.

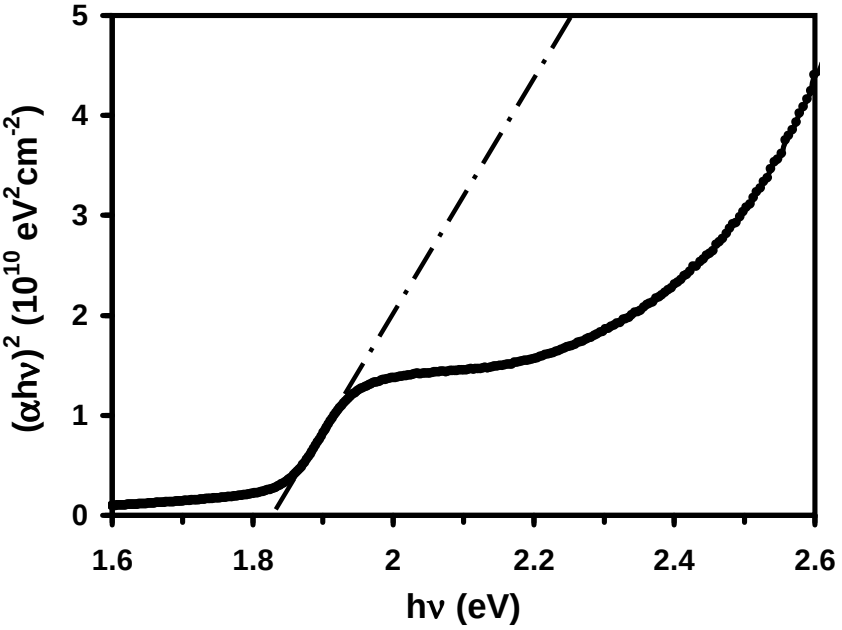


Figure 4.6: β-$BaCu_2S_2$ direct bandgap estimate from plot of $(\alpha h\nu)^2$ versus $h\nu$ for a 450 nm-thick thin film.

band gap for β-$BaCu_2S_2$ is estimated at 1.8 eV by using an $(\alpha h\nu)^2$ absorption edge plot (Fig. 4.6). The conductivity of the β-$BaCu_2S_2$ thin film is 8 S/cm.

4.2 $BaCu_2S_2$ as a p-Type Layer in Thin-film Solar Cells

Improvements to solar cells are continually being sought, as solar cells have the potential to provide low-cost, environmentally friendly energy on a large scale. Improvements in both efficiency and materials are sought. Desirable materials are inexpensive, long-lasting and non-toxic. This section describes the current state of the art of Cu(In,Ga)Se_2 solar cells, followed by discussion of a new p-i-n solar cell design that may incorporate $BaCu_2S_2$.

4.2.1 Cu(In,Ga)Se_2 Solar Cells

The current record thin-film solar cell efficiency is 18.8% for Cu(In,Ga)Se_2 solar cells fabricated by the National Renewable Energy Labratory (NREL). [59] The structure

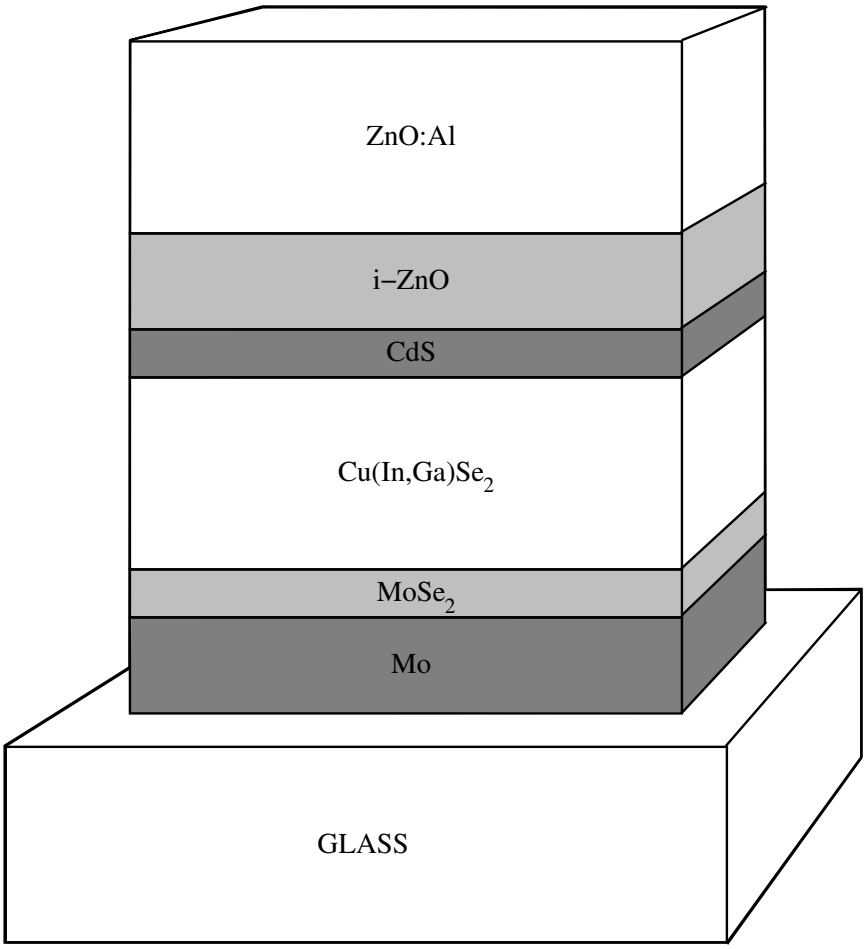


Figure 4.7: Thin-film $Cu(In,Ga)Se_2$ solar cell structure.

of these cells is as shown in Fig. 4.7. A glass substrate is used for the cells. Mo is the back electrode. Cu(In,Ga)Se_2 (an alloy of ∼80% $CuInSe_2$ and ∼20% $CuGaSe_2$) is the absorber layer. Cu(In,Ga)Se_2 has a bandgap of ∼ 1.2 eV [59], and is thus able to absorb much of the solar spectrum. Na diffuses from the glass substrate through the Mo electrode layer and into the absorber layer during absorber growth. The Na produces better quality and more conductive Cu(In,Ga)Se_2 films. Na diffusion from the glass substrate was originally unintentional, but it has become purposeful since the benefits of Na were understood. During the deposition of the Cu(In,Ga)Se_2 absorber layer, a thin layer of $MoSe_2$ forms at the Mo surface. CdS is a buffer layer between the Cu(In,Ga)Se_2 absorber and the ZnO 'window'. Intrinsic ZnO (i-ZnO) and Al-doped ZnO layers form the 'window' and top electrode of the solar cell. The ZnO layer is called a window as ZnO has a bandgap of 3.2 eV and is therefore transparent over most of the solar spectrum.

The cell works as illustrated by the energy band diagram shown in Fig. 4.8 (after Rau et al. [59]). Solar radiation passes through the ZnO window and CdS buffer layer. Electron-hole pairs are generated in the Cu(In,Ga)Se_2 absorber layer. The generated electrons and holes are separated by the solar cell and collected at the electrodes. As can be seen in Fig. 4.8, the $MoSe_2$ layer serves as an electron 'reflector' by presenting an energy barrier to minority carrier electrons. This reflector reduces recombination at the Mo electrode, thus improving collection efficiency.

The fill factor of a solar cell is a measure of its quality as a power source. The fill factor is an often quoted figure of merit for a solar cell, and so is explained here. As illustrated in Fig. 4.9, to find the fill factor (FF), the open circuit voltage (V_{oc}), short circuit current (I_{sc}), and maximum power (P_{max}) are measured for the solar cell. I_{sc} is the photocurrent for the illuminated solar cell when operated using a short circuit as a load. V_{oc} is the measured diode voltage for the illuminated solar cell when the load is an open circuit. The fill factor is ideally one. It is degraded in a real solar cell by losses due to series and shunt resistances in the cell. As illustrated in Fig. 4.9, an ideal solar cell has rectangular current-voltage curves. A real solar cell has current-voltage curves like

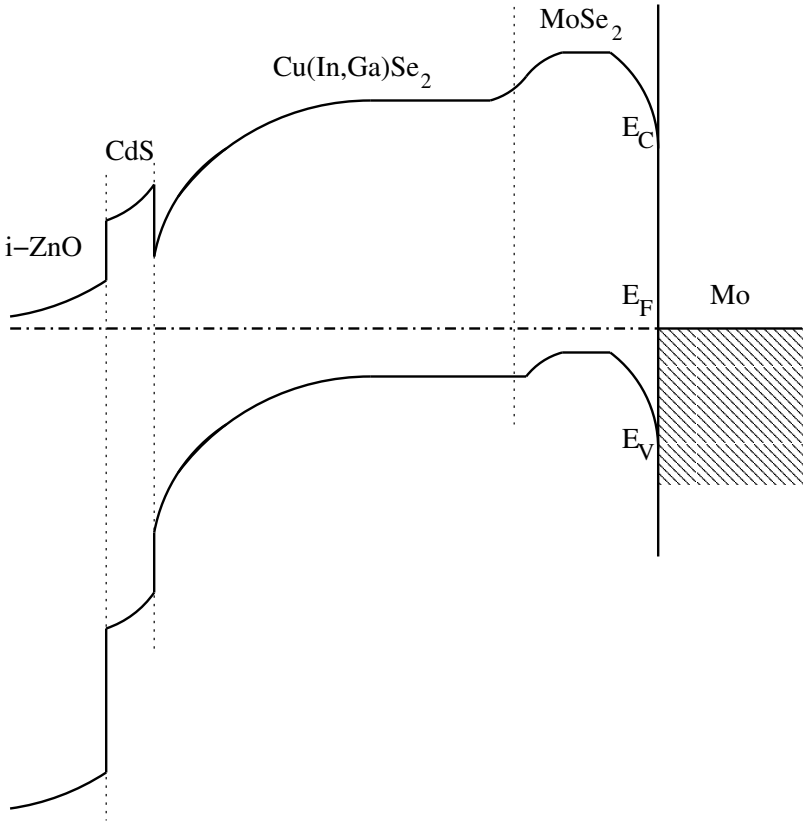


Figure 4.8: Equilibrium energy band diagram for a $Cu(In,Ga)Se_2$ thin-film solar cell.

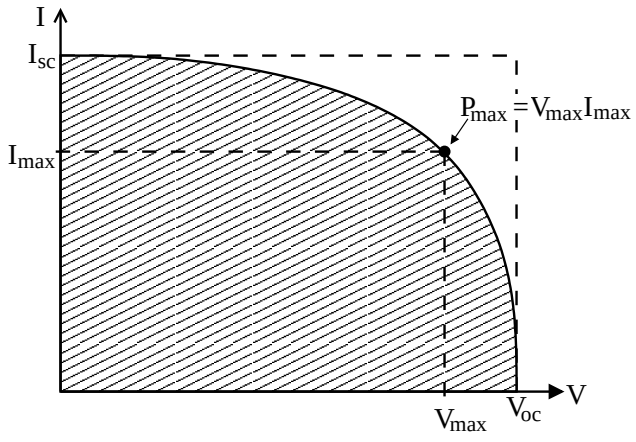


Figure 4.9: Current-voltage plot illustrating the meaning of the fill factor for a solar cell.

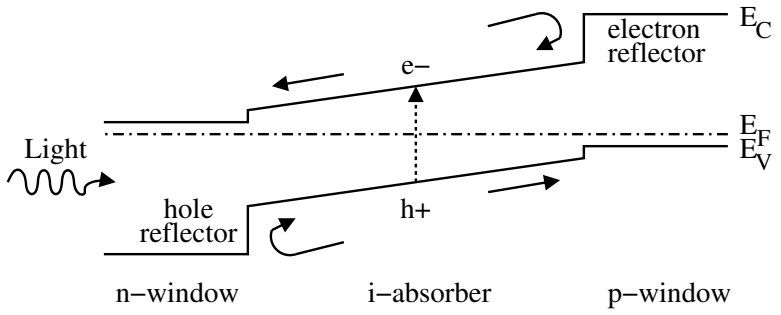


Figure 4.10: Energy band diagram for a next-generation pin solar cell.

the curved plot in Fig. 4.9. The fill factor is the fraction of the ideal rectangular current-voltage plot filled by the real curved current-voltage plot. The fill factor is calculated from [60]

$$FF = \frac{P_{max}}{I_{sc}V_{oc}}. \tag{4.1}$$

For the previously mentioned record-efficiency thin-film solar cell made at NREL, FF= 78.6%, $I_{sc} = 35.2$ mA/cm^2, and $V_{oc} = 678$ mV. [59]

4.2.2 A Next-Generation Solar Cell

For next-generation photovoltaic applications, an innovative thin-film solar cell design is proposed. [61] The proposed solar cell is a p-i-n, double-heterojunction thin-film cell. The p and n films are both wide bandgap window layers, and the insulating film is a narrower bandgap absorber layer. This solar cell operates as illustrated by the energy band diagram shown in Fig. 4.10 (after Wager and Keszler [61]). Solar radiation passes through the window layer. Electron-hole pairs are generated in the absorber layer. The generated carriers are separated by the solar cell and collected at the electrodes. The heterojunction band discontinuities act as reflectors for the minority carriers, preventing unwanted recombination at the electrodes and allowing carriers to be separated and collected efficiently by the cell. This design incorporates the concept of engineered reflectors for both electrodes in a solar cell.

A direct bandgap material is chosen for the absorber layer for efficient electron-hole pair generation. The absorber layer is selected to be lightly p-type since the photo-generated holes have a smaller mobility than the photo-generated electrons and are less efficiently collected. The light p-doping in the absorber layer in conjunction with the Fermi level positions of the p and n window layers results in the creation of a drift field in the absorber layer, which helps extract photo-generated carriers. Light doping of the absorber layer maximizes the minority carrier lifetime, reducing recombination losses. Materials containing copper are selected for the window and absorber layers in the proposed solar cells. This is a consequence of the fact that p-type behavior is found in many copper-containing compounds.

$BaCu_2S_2$ is being considered as the p-window layer in these proposed thin-film solar cells. Some other materials being considered for the p-window are $CuM^{III}X_2$ and $M^{II}Cu_2X_2$, where M^{II} is a divalent cation, M^{III} is a trivalent cation, and X is S, Se, or Te. Some of the materials being considered for the n-window are CuS-compounds, CuSe-compounds, and CuTe-compounds. Some potential i-absorber layers are CuS, $CuM^{II}X_2$, $CuM^{II}X_2$, Cu_2Te, and $Cu(In,Ga)Se_2$.

Development of solar cells using $BaCu_2S_2$ as the p-window has just begun. Samples of $BaCu_2S_2$ deposited onto SnO_2 were sent to the National Renewable Energy Laboratory (NREL) for further solar cell device development. At NREL, the basic properties of $BaCu_2S_2$ were investigated. Properties such as bandgap and mobility are found to be desirable for solar cell applications. Another desirable attribute of $BaCu_2S_2$ for solar cells is the fact that it has a direct bandgap. $BaCu_2S_2$ is also processed at low temperatures (300°C), which is desirable from a process integration standpoint. The fact that $BaCu_2S_2$ is copper-based makes $BaCu_2S_2$ compatible with materials already in use at NREL, such as $Cu(In,Ga)Se_2$. At NREL, $CuGaSe_2$ was deposited onto one sample, followed by an electrode to complete the $SnO_2/BaCu_2S_2/CuGaSe_2$ solar cell. [62] This device did not work. There are still process integration issues to overcome, and more devices will be fabricated and tested in the near future.

4.3 Conclusions

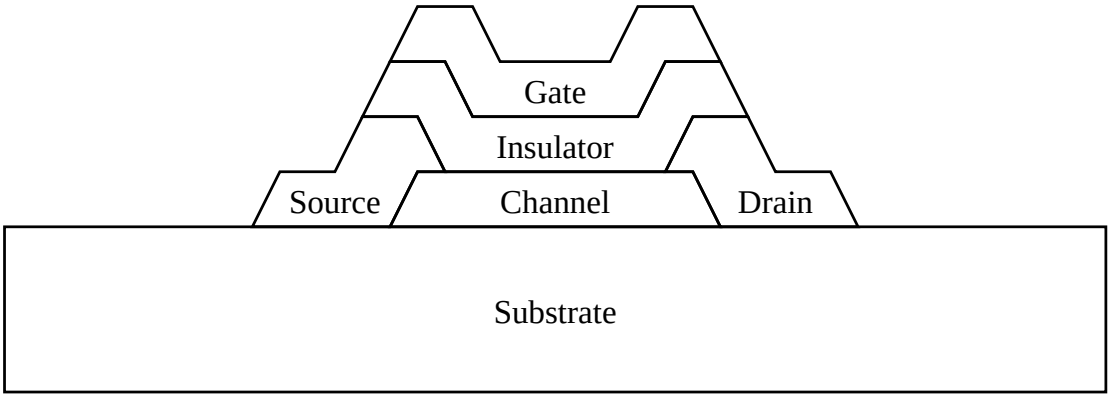
This chapter describes the processing and characterization of $BaCu_2S_2$ p-type transparent conducting thin films. The current world-record efficiency $Cu(In,Ga)Se_2$ solar cells are described. Finally, a next-generation p-i-n solar cell and the potential use of $BaCu_2S_2$ in this new cell are explained.

5. P-CHANNEL TRANSPARENT THIN-FILM TRANSISTORS

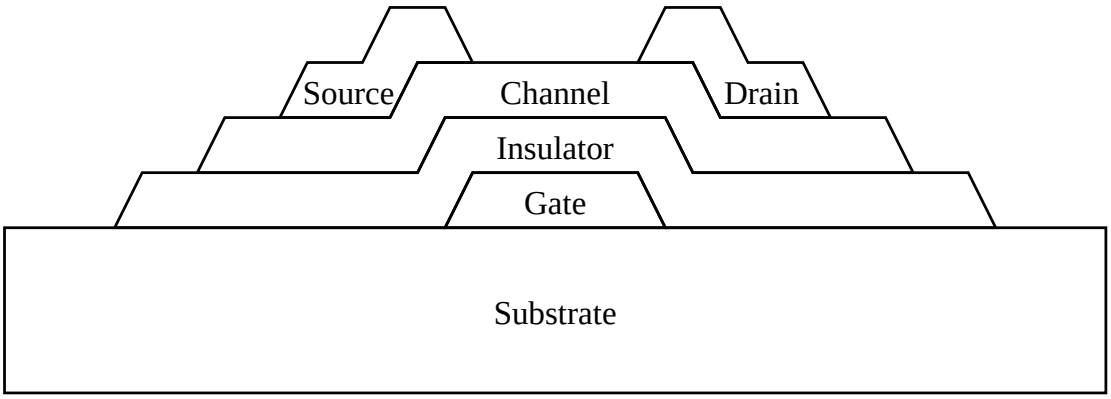
This chapter describes work on the development of p-channel transparent thin-film transistors (p-TTFTs). No successful p-TTFTs or p-TFTs have been realized to date. Important considerations for the realization of p-TTFTs that have become apparent through this thesis research include injecting contacts, semiconductor channel conductivity, and insulator integrity. Insulator integrity is particularly an issue with p-TTFTs fabricated with Cu-containing compounds. Also included in this chapter is a section on SPICE modeling of p-TTFTs. SPICE modeling is found to be useful in the formulation of physical explanations for the p-TTFT current-voltage characteristics obtained from experiment.

The p-TTFTs discussed in this chapter are metal-insulator-semiconductor field effect transistors (MISFETs). The conductivity of a FET is modulated by an electric field (field effect). In the case of the MISFET, the electric field is generated by a metal-insulator-semiconductor capacitor. Figure 5.1 shows the p-TTFT structures used in this work. p-TTFT devices are defined using shadow masks for the different film layers. Figure 5.2 shows the shadow mask geometries used to fabricate p-TTFTs.

Three p-type channel-layer materials are investigated in this work: $CuScO_2$, NiO, and $BaCu_2S_2$. Gate materials used are Al and In_2O_3:Sn (ITO). Gate insulators used are SiO_2 and a superlattice of alternating layers of Al_2O_3 and TiO_2 (known as ATO). All of the structures fabricated and tested are listed in Table 5.1. Because non-transparent gate and source/drain contacts are used in some of these devices, those devices are best referred to as p-TFTs rather than p-TTFTs, which is appropriate only for a device with all transparent layers. However, since fabrication of an operational p-TTFT is the ultimate objective of this work, all of the devices discussed in this chapter are denoted p-TTFTs, regardless of whether or not transparent contacts are employed.



(a)



(b)

Figure 5.1: (a) p-TTFT co-planar top-gate structure, and (b) p-TTFT staggered bottom-gate structure.

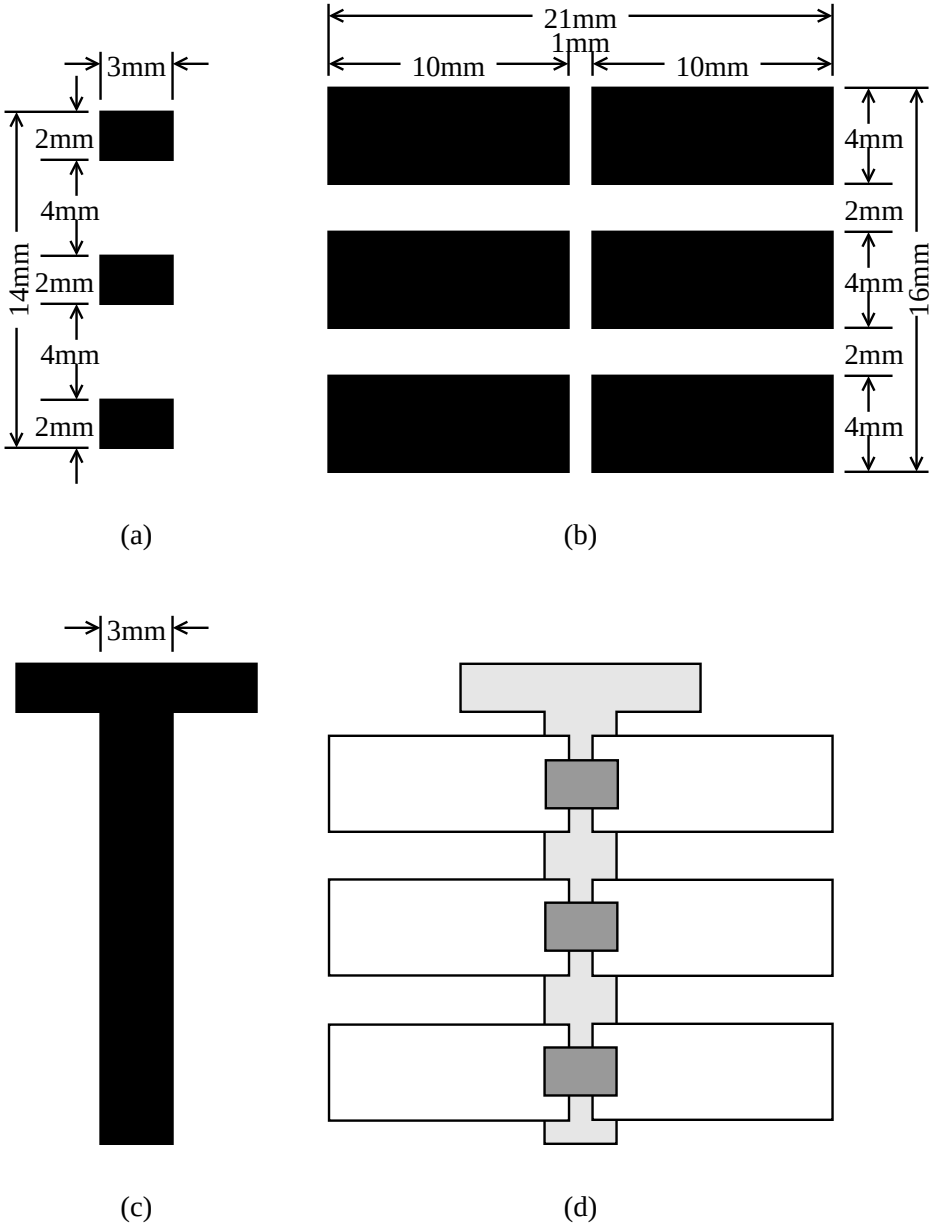


Figure 5.2: Shadow masks used to fabricate p-TTFTs: (a) is the channel mask, (b) is the source/drain mask, (c) is the gate mask, and (d) illustrates how the masks integrate.

Table 5.1: p-TTFT structures studied. CTG is co-planar top-gate structure and SBG is staggered bottom-gate structure.

Device No.	Channel	Gate	Insulator	Source/Drain Contacts	Type	No.TFTs Made
1	$BaCu_2S_2$:Zn	Al	SiO_2	$BaCu_2S_2$	CTG	15
2	$BaCu_2S_2$:Zn	ITO	ATO	$BaCu_2S_2$	SBG	18
3	$CuScO_2$	Al	SiO_2	Au	CTG	16
4	NiO	Al	SiO_2	Au	CTG	6
5	NiO	ITO	ATO	Ni	SBG	12
6	NiO:Li	Al	SiO_2	Ni	CTG	12
7	NiO:Li	ITO	ATO	Ni	SBG	18
8	NiO:Li	ITO	ATO	$La_{0.5}Sr_{0.5}CoO_3$	SBG	6

5.1 $BaCu_2S_2$:Zn p-TTFTs

p-TTFTs are made using Zn-doped $BaCu_2S_2$ as the the channel layer and undoped $BaCu_2S_2$ for the source and drain contacts (p-TTFT Device Nos. 1 and 2, Table 5.1). Using $BaCu_2S_2$ as the source and drain contacts to a $BaCu_2S_2$:Zn channel should provide injecting contacts since the contacts are made using the same material as the channel. Zn doping decreases the conductivity of $BaCu_2S_2$. [30] Zn-doping of $BaCu_2S_2$ is discussed further below.

5.1.1 Fabrication of $BaCu_2S_2$:Zn p-TTFTs

Device geometries are defined during processing using shadow masks. For bottom-gate devices, the following processing procedure is employed, using a glass slide pre-coated with ITO/ATO films. The 200 nm ITO film serves as the gate. The 220 nm thick ATO is the gate insulator. A 120 nm-thick $BaCu_2S_2$ channel layer is deposited

by RF sputtering (width 2 mm, length 1 mm). 20 nm of Zn is thermally evaporated onto the unannealed $BaCu_2S_2$ layer using shadow mask (a), Fig. 5.2. The $BaCu_2S_2$ source and drain are then deposited. The devices are then annealed at 300°C in Ar. This anneal serves both to crystallize the $BaCu_2S_2$ layer and to drive in the Zn. At this point, the bottom-gate devices are finished. For top-gate devices, the processing is accomplished using a plain glass substrate. The $BaCu_2S_2$ channel, Zn doping, and $BaCu_2S_2$ source/drain contacts are processed in the same manner as for bottom-gate devices. After source/drain deposition and annealing, a SiO_2 gate insulator layer ∼250 nm thick is deposited by PECVD, followed by a 100 nm thick Al gate deposited by thermal evaporation.

5.1.2 Discussion of $BaCu_2S_2$:Zn p-TTFTs

Zn-doping lowers the conductivity of $BaCu_2S_2$. Substitution of Zn^{2+} onto a Cu^+ site decreases the conductivity. The conductivity of $BaCu_2S_2$ is decreased from ∼17 S/cm to $\sim 10^{-2}$ S/cm as a consequence of the Zn doping. This decrease in conductivity is required for proper p-TTFT operation because undoped $BaCu_2S_2$ is too conductive to allow conductivity modulation of the channel at reasonable gate voltages (see Sec. 2.2.3.2). That a decrease in conductivity is necessary can be illustrated by calculating the threshold voltage, V_t, for an undoped $BaCu_2S_2$ p-TTFT with a very thin channel layer (20 nm). For example,

$$V_t = \frac{qp_{chan}t_{chan}}{C_{ins}} = \frac{qp_{chan}t_{chan}}{\epsilon_{ins}\epsilon_0}t_{ins}, \tag{5.1}$$

where $q = 1.6 \times 10^{-19}$ C, $p_{chan} = 10^{19}$ cm^{-3}, $t_{chan} = 20$ nm, $\epsilon_{ins} = 10$ for ATO, $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm, and $t_{ins} = 220$ nm. The resulting value of V_t is 80 V. A threshold voltage of 80 V is too large to be practical.

The threshold voltage calculation is repeated for a $BaCu_2S_2$:Zn p-TTFT with a 120 nm thick channel layer to illustrate that the Zn-doping is expected to yield a reasonable threshold voltage for $BaCu_2S_2$ p-TTFTs. Eq. 5.1 is used with $p_{chan} = 10^{16}$

cm^{-3}, t_{chan} = 120 nm, and all other values held constant. The resulting value of V_t is 0.4 V, a reasonable threshold voltage.

p-TTFTs are tested using an HP 4140B picoammeter. No meaningful current-voltage characteristics could be obtained for $BaCu_2S_2$ p-TTFTs due to a large gate leakage current for each and every device. The gate leakage is large enough to overrun the current limit of the ammeter, i.e., the gate leakage is greater than 1 mA. A few devices had gates that were intact to begin with. However, the gates of these devices broke down at an applied gate voltage of 20 V or less.

The large gate leakage in the $BaCu_2S_2$ p-TTFTs may be due to interaction between $BaCu_2S_2$ and the insulator layer, causing degradation of the insulator. Cu migration from the $BaCu_2S_2$ into the gate insulator seems likely, though the annealing temperature is quite low at 300°C. The gate leakage problem needs to be addressed before any further progress can be made with $BaCu_2S_2$ p-TTFTs. For a top-gate device, a double insulator stack using Si_3N_4 and SiO_2, with Si_3N_4 next to the $BaCu_2S_2$ layer would be worth trying, in order to determine if the Si_3N_4 acts as an effective diffusion barrier between the $BaCu_2S_2$ and SiO_2. This technique was used successfully by Masuda et al. for ZnO TTFTs. [35] Si_3N_4 could also be deposited on top of the ATO film in a bottom-gate device.

5.2 NiO p-TTFTs

p-TTFTs are first fabricated using undoped NiO as the channel material and Au or Ni as the source/drain contacts (p-TTFT Device Nos. 4 and 5, Table 5.1). Both co-planar top-gate and staggered bottom-gate devices are fabricated. The top-gate devices use Au source/drain contacts, and the bottom-gate devices use Ni source/drain contacts. Au or Ni contacts on NiO are expected to be injecting because the workfunctions of Au and Ni are close in energy to the valence band edge of NiO. The valence band edge of NiO is ∼5.0 eV. [26] The workfunction of Au is ∼5.1 eV. [63] The workfunction of Ni is ∼5.15 eV. [63] Ni and Au as contacts to NiO are discussed further below.

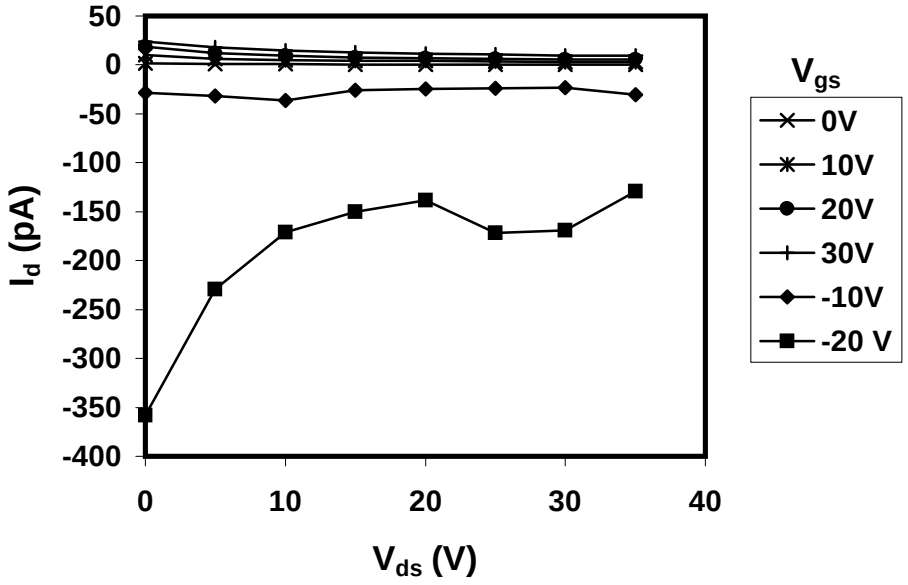


Figure 5.3: I_d versus V_{ds} curves for a p-TTFT with a NiO channel, Au source/drain contacts, ATO gate insulator and ITO gate.

5.2.1 Fabrication of NiO p-TTFTs

Devices are processed using shadow masks (Fig. 5.2). For bottom-gate devices, the 100 nm-thick NiO channel (width 2 mm, length 1 mm) is first deposited by ion-beam sputtering onto a glass slide pre-coated with ITO and ATO films. The NiO film is transparent and slightly green-gray in color. Next, the NiO film is rapid thermal annealed at 600°C in O_2 for 5 minutes. Source and drain contacts are then deposited (∼100 nm of either Au or Ni). Au is deposited by thermal evaporation. Ni is deposited by ion-beam sputtering. At this point bottom-gate devices are complete. Top-gate devices are made on plain Corning 1737 glass substrates. The processing for the NiO channel and for the source/drain contacts is the same as for bottom-gate devices. Next, ∼250 nm of SiO_2 is deposited by PECVD as the gate insulator, followed by an Al gate.

5.2.2 Discussion of NiO p-TTFTs

Typical I_d versus V_{ds} curves for undoped NiO p-TTFTs are shown in Fig. 5.3. These curves are very similar for devices made with either ATO or PECVD SiO_2 gate

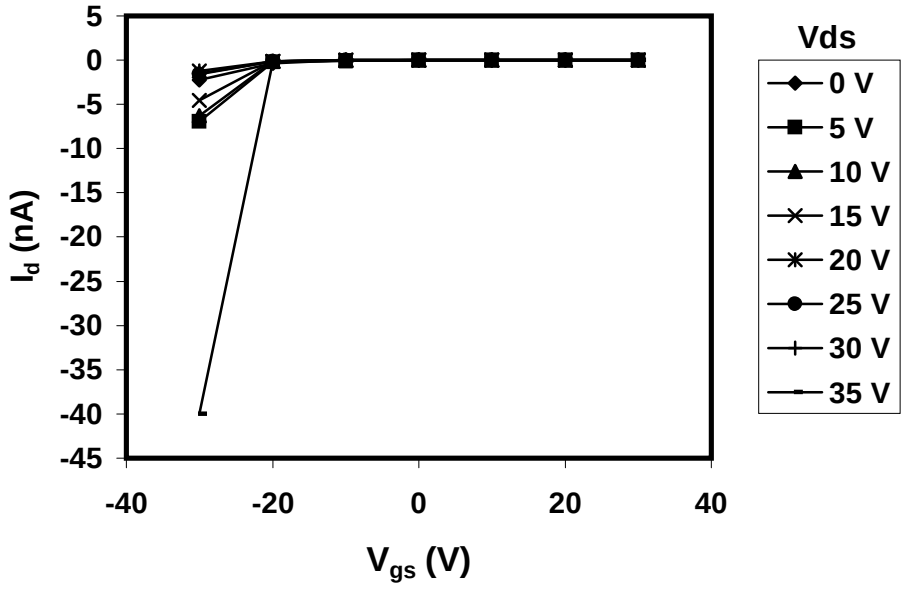


Figure 5.4: I_d versus V_{gs} curves for a p-TTFT with a NiO channel, Au source/drain contacts, ATO gate insulator, and ITO gate.

insulators. Three important conclusions arise from an assessment of Fig. 5.3. First, no transistor action is evident. Second, the I_d versus V_{ds} curves are determined by the gate leakage characteristics of this undoped NiO p-TTFT, and the gate leakage is very small. Third, the gate leakage is rectifying with respect to V_{gs}; a larger gate leakage current flows with a negative gate voltage polarity.

The rectifying nature of the gate leakage is also evident in Fig. 5.4, which is a plot of I_d versus V_{gs} at various values of V_{ds}. Again, this plot shows that the gate leakage current is rectifying, with greater current for negative gate voltages. This enhanced leakage current with negative gate voltage polarity may be because electron injection from the gate contact through the gate insulator is more effective for a negative gate bias than hole injection for a positive gate bias. Alternatively, a larger negative gate voltage leakage current could be ascribed to hole injection from the channel, through the gate insulator, to the gate contact. This hole injection from the channel, although possible, seems less likely since these NiO p-TTFTs provide no evidence for p-type behavior in the channel.

From Fig. 5.4, the gate leakage current density near the leakage threshold may be calculated. At $|V_{gs}| \sim 25$ V, $|I_d| \sim 1$ nA. The insulator thickness is 200 nm. The insulator area is 2 mm by 3 mm. The insulator field (assuming all of the applied voltage drops across the gate insulator) is equal to ~ 1.25 MV/cm. The near threshold gate leakage current density is equal to ~ 17 nA cm^{-2}. This gate leakage current is quite small, about an order of magnitude greater than that found experimentally for high-quality ATO capacitors. [64]

One possible reason for why the undoped NiO p-TTFTs did not work is that the source contacts are non-injecting. A barrier height analysis is performed below to further explore this possibility. Another possible reason is that the undoped NiO channel is too insulating, and injected carriers are trapped in interface states and bulk traps. An estimation of the fraction of trapped carriers is performed below to explore this possibility.

A possible reason for why these undoped NiO p-TTFTs did not operate is due to poor hole injection from the source contact. Hole injection in undoped NiO p-TTFTs is now considered quantitatively. The hole injection barrier height for Ni or Au contacts on NiO is calculated as follows. The pinning factor, S, is calculated according to Eq. 2.7, which is repeated here for convenience,

$$S = \frac{1}{1 + 0.1(\epsilon_\infty - 1)^2}, \tag{5.2}$$

where ϵ_∞ is the high-frequency dielectric constant of a material. For NiO, $\epsilon_\infty = 5$, [65] and S is calculated to be 0.38. S ranges from 0 to 1, with 0 indicating strong pinning and 1 indicating no pinning. The value of S for NiO is intermediate, though closer to pinned. S is then used to calculate the barrier height using Eq. 2.8, which is repeated here for convenience,

$$\phi_{Bp} = (E_g + \chi_s - \phi_{CNL}) - S(\phi_m - \phi_{CNL}), \tag{5.3}$$

where ϕ_{CNL} is the charge neutrality level of the interface states measured from the vacuum level. For a NiO/Au contact, $E_g \sim 3.5$ eV, $\chi_s = 1.4$ eV, $\phi_{CNL} = 4.5$ eV (using

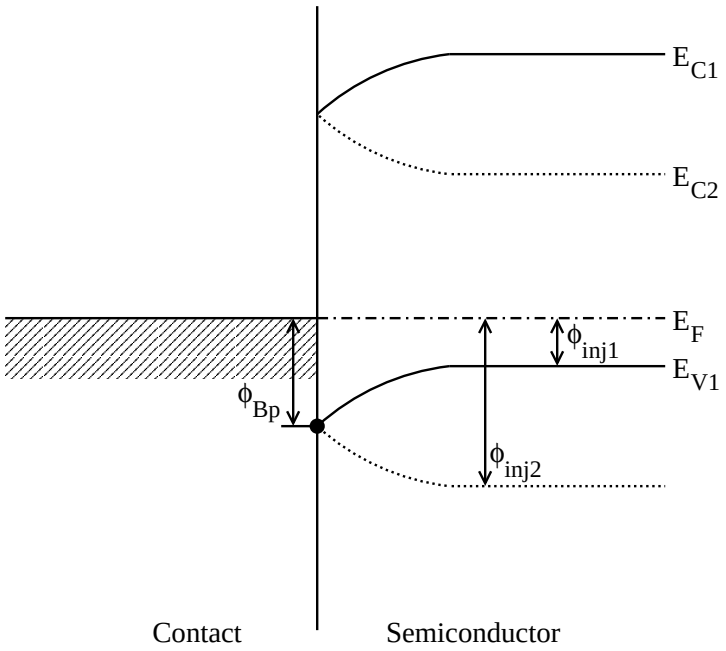


Figure 5.5: Equilibrium energy band diagram for a metal-semiconductor contact illustrating the change in hole injection barrier with semiconductor carrier concentration.

the universal charge neutrality level of Van de Walle and Neugebauer, see Sec. 2.3.2), and $\phi_m = 5.1$ eV. Using these values gives $\phi_{Bp} = 0.17$ eV. This is not a large barrier and, thus, would be expected to lead to a sufficient level of hole injection, as discussed below, so that injection-limited behavior for these NiO p-TTFTs would seem to be unlikely.

However, this calculated value of ϕ_{Bp} does not provide the whole picture for hole injection in insulating NiO, as evident from the energy band diagram shown in Fig. 5.5. Figure 5.5 illustrates how the carrier injection barrier height, ϕ_{inj}, in a metal-semiconductor contact may be larger than the Schottky barrier height, ϕ_{Bp}, depending on the location of the Fermi level in the semiconductor bulk. The location of the Fermi level, in turn, depends on the carrier concentration in the semiconductor. Two situations are indicated. For heavy p-type doping (i.e. $\phi_{inj1} < \phi_{Bp}$), the metal-semiconductor hole injection barrier is established by ϕ_{Bp}. For light p-type doping (i.e. $\phi_{inj2} > \phi_{Bp}$), the metal-semiconductor hole injection barrier is established approximately by ϕ_{inj2}. ϕ_{inj} is

given by

$$\phi_{inj} = (E_F - E_V)\Big|_{bulk}, \tag{5.4}$$

where $(E_F - E_V)\Big|_{bulk}$ refers to the Fermi level with respect to the valence band maximum in the semiconductor bulk. Note that the actual hole injection barrier is somewhat ambiguous when $\phi_{inj} > \phi_{Bp}$, as illustrated in Fig. 5.6 which shows an energy band diagram under bias for a condition of hole injection. The important point to note from Fig 5.6 is that when $\phi_{inj} > \phi_{Bp}$, the semiconductor is quite insulating such that most of the voltage will be dropped across the bulk portion of the semiconductor, rather than strongly modulating the hole injection barrier, as expected in a normal Schottky barrier contact. Thus, the metal-semiconductor hole injection barrier is expected to be $\sim \phi_{inj2}$, as indicated in Fig. 5.6. An example of this behavior where $\phi_{inj} > \phi_{Bp}$ may be found in the discussion of Baritt diodes in Ref. [39]. Other examples may be found in explanations of space charge limited current in insulators, Ref. [66] and Ref. [67].

Next, ϕ_{inj} is estimated. First, to find $(E_F - E_V)\Big|_{bulk}$, the density of states, N_V, is calculated from [39]

$$N_V = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2}, \tag{5.5}$$

where m^* is the density of states effective mass, k is the Boltzmann constant, T is temperature in K, and h is Planck's constant. For undoped NiO, $m^* = 1.82 \times 10^{-30}$ kg (i.e., $\frac{m^*}{m_0} = 2$) [65], $k = 1.83 \times 10^{-23}$ J/K, $T = 300$ K, and $h = 6.626 \times 10^{-34}$ J-s. Using these values, $N_V = 7 \times 10^{19}$ cm^{-3}. $(E_F - E_V)$ may now be calculated from [39]

$$\phi_{inj} = E_F - E_V = -kT \ln\left(\frac{p}{N_V}\right), \tag{5.6}$$

where $kT = 0.0259$ eV, $p = 10^{12}$ cm^{-3}, and $N_V = 7 \times 10^{19}$ cm^{-3}. Using these values, $\phi_{inj} = 0.47$ eV, a larger barrier to hole injection than when ϕ_{Bp} is assumed to constitute the hole injection barrier. It is possible that this barrier could be inhibiting hole injection, causing the failure of the NiO p-TTFTs.

A calculation is now made to assess whether this barrier is too large to allow for adequate hole injection. Assuming that the source contact needs to supply 10 μA of

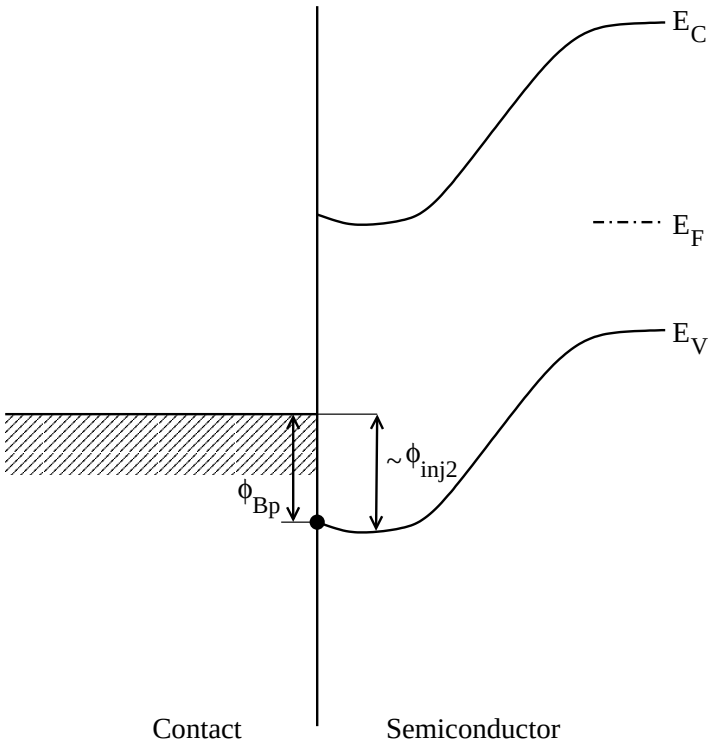


Figure 5.6: Energy band diagram for a metal-semiconductor contact illustrating the hole injection barrier under bias when $\phi_{inj} > \phi_{Bp}$ and there is the condition of hole injection.

current to the transistor channel, the current density required is given by

$$J_{req} = \frac{I_{req}}{A}, \tag{5.7}$$

where $I_{req} = 10$ μA and A is the source area, 0.02 cm^2. Using these values, $J_{req} = 0.5$ mA cm^{-2}. Assuming that hole injection is accomplished by thermionic emission over a barrier, [39]

$$J_{req} = A^* T^2 \exp\left(- \frac{q\phi_{Bp}}{kT} \right), \tag{5.8}$$

where A* is the Richardson constant ($\sim 120\frac{m^*}{m_0}$). $\frac{m^*}{m_0}$ is assumed to be equal to 1. Solving Eq. 5.8 for the barrier height ϕ_{Bp} gives

$$\phi_{Bp} = \frac{kT}{q} \ln \left[\frac{A^* T^2}{J_{req}} \right]. \tag{5.9}$$

Using the values given above, $\phi_{Bp} = 0.62$ eV. This value of ϕ_{Bp} provides an estimate of the maximum barrier height allowable to supply a current of 10 μA from the source to

the channel of the p-TTFT. Comparing this value to the value for ϕ_{inj}, 0.47 eV, it is seen that the barrier height should allow adequate carrier injection into the transistor.

As mentioned previously, another possibility that explains why the undoped NiO p-TTFTs do not work is that the undoped NiO channel is too insulating, and injected carriers are trapped in bulk traps and interface states. Undoped stoichiometric NiO has a very high resistivity, on the order of 10^{12} Ω-cm. The I_d versus V_{ds} curve trend shown in Fig. 5.3 is dominated by gate leakage current, the magnitude of which provides an upper limit on the possible, but undetectable, gate-modulated transistor current present in this device. This transistor current upper limit implies a corresponding upper limit in the channel mobility, which is estimated as follows.

An upper limit on mobility, μ_{UL}, is estimated from the current-voltage characteristics in Fig. 5.3. Equation 5.17 is used with $I_d = 100$ pA, $C_{ins} = 44.3$ nF/cm^2 (using the dielectric constant of ATO, 10, and an insulator thickness of 220 nm), $\frac{W}{L} = 2$, $V_{gs} = 20$ V, $V_t = 5$ V, and $V_{ds} = 20$ V. These values yield a mobility of $\sim 4 \times 10^{-6}$ cm^2/V-s. This is a very small value. Note that this is not the actual mobility, but only an upper limit, established by the magnitude of the gate leakage current. μ_{UL} is used in subsequent calculations, but it should be recognized that μ_{UL} is only a rough, upper-limit estimate.

The channel carrier concentration (p_{chan}) can be estimated using the upper limit mobility calculated (μ_{UL}) and the estimated resistivity (ρ) of the channel layer of 10^{12} Ω-cm, from

$$p_{chan} = \frac{1}{q\mu\rho}. \tag{5.10}$$

This leads to $p_{chan} \sim 10^{12}$ cm^{-3}. Using this value for p_{chan}, other quantities may be estimated, including the fraction of carriers available for transistor operation (i.e., the fraction not trapped), and a revised value for the barrier to hole injection.

The fraction of carriers available for transistor operation is given by

$$\frac{p_{chan}}{p_t + p_{chan}} = \frac{\mu_{UL}}{\mu_{est}}, \tag{5.11}$$

where μ_{est} is a "reasonable" estimated mobility for a channel material without traps and p_t is the number of trapped carriers. Assuming a value for μ_{est} of 0.1 cm^2/V-s and $\mu_{UL} = 4 \times 10^{-6}$ cm^2/V-s as found above, the fraction of carriers available for transistor operation is estimated to be 4×10^{-5}. This is a very small value, indicating that if holes are indeed being injected into the channel, most of these injected holes are trapped, leaving very few available for transistor operation. This seems to be the most likely reason why these undoped NiO p-TTFTs do not operate. The effects of poor injection and carrier trapping are discussed further in Sec. 5.4 in the context of a SPICE model of insulating channel p-TTFT behavior.

As a result of the realization that undoped NiO is too insulating to function as a p-TTFT channel, Li-doped NiO is explored as a p-TTFT channel material. Li-doping increases the conductivity of the NiO channel layer and lowers the additional barrier to carrier injection due to the reduced separation in energy between the Fermi level and the valence band.

5.2.3 Fabrication of NiO:Li p-TTFTs

p-TTFTs are fabricated using Li-doped NiO as the channel material and Ni or $La_{0.5}Sr_{0.5}CoO_3$ as the source and drain contacts (p-TTFT Device Nos. 6-8, Table 5.1). $La_{0.5}Sr_{0.5}CoO_3$ is expected to be an injecting contact to NiO because the workfunction of $La_{0.5}Sr_{0.5}CoO_3$ ($\sim$4.65 eV [68]) is close in energy to the valence band edge of NiO ($\sim$5.0 eV [26]).

Devices are processed using shadow masks (Fig. 5.2). For bottom gate devices, a $\sim$100 nm thick NiO channel (width 2 mm, length 1 mm) is first deposited by ion beam sputtering onto a glass slide pre-coated with ITO and ATO films. This NiO film is then soaked for 4 to 6 hours in either a 1% or 5% solution of LiOH in H_2O. After soaking, the NiO film is rinsed in deionized H_2O and annealed in a furnace at 250°C for 2 hours. After annealing, the films are again rinsed in deionized H_2O. Next, the films are rapid thermal annealed at 600°C in O_2 for 5 minutes. Source and drain contacts

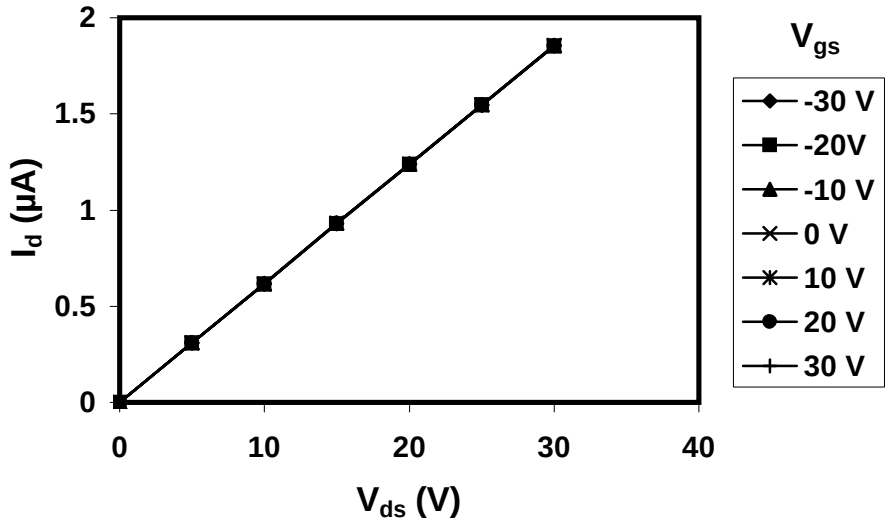


Figure 5.7: I_d versus V_{ds} curves for a p-TTFT with a NiO:Li channel, Ni source/drain contacts, ATO gate insulator, and ITO gate.

are then deposited ($\sim$ 100 nm of Ni or $La_{0.5}Sr_{0.5}CoO_3$). Ni is deposited by ion beam sputtering, and $La_{0.5}Sr_{0.5}CoO_3$ is deposited by RF sputtering. Bottom-gate devices are now complete. Top-gate devices are fabricated on plain Corning 1737 glass. The processing for the NiO:Li channel layer and for the source/drain contacts is the same as for the bottom-gate devices. Next, $\sim$250 nm of SiO_2 is deposited by PECVD for the gate insulator, followed by an Al gate.

5.2.4 Discussion of NiO:Li p-TTFTs

Typical I_d versus V_{ds} curves for NiO:Li p-TTFTs with Ni contacts are shown in Fig. 5.7. There is very little difference in curves obtained for devices using either ATO or PECVD SiO_2 for the gate insulator. No gate control is evident for these devices. An explanation for the lack of gate control in NiO p-TTFTs is that the NiO:Li channel layer is too conductive and the gate cannot modulate the conductivity (see Sec. 2.2.3.2). Varying the LiOH solution concentration or soak time in the ranges tested (1% or 5% solution, 4 to 6 hours soaking time) did not cause variability in the NiO:Li conductivity.

Perhaps a shorter soaking time would yield less conductive NiO:Li. Another possibility is to use an alternative method to induce p-type conductivity in NiO.

The following calculations are carried out in order to estimate the threshold voltage for these NiO:Li p-TTFTs. The carrier concentration in the NiO:Li channel layer can be estimated from the linear current-voltage characteristics of the NiO:Li p-TTFT. A resistance can be determined from the inverse slope of the current-voltage characteristics,

$$R = \frac{V_{ds}}{I_d} \tag{5.12}$$

where V_{ds}/I_d is the inverse slope of the linear current-voltage characteristics in Fig. 5.7. The slope is 6.2 $\times 10^{-8}$ Ω^{-1}, and $R = 1.6 \times 10^7$ Ω. A fundamental equation for bulk resistance is

$$R = \frac{\rho L}{A}, \tag{5.13}$$

where ρ is the channel layer semiconductor resistivity, L is the channel length, and A is the channel cross-sectional area. A fundamental equation for resistivity, ρ, is

$$\rho = \frac{1}{q\mu_p p_{chan}}, \tag{5.14}$$

where $q = 1.6 \times 10^{-19}$ C, μ_p is the channel mobility, and p is the carrier concentration in the channel semiconductor. Substituting Eq. 5.13 into Eq. 5.14 and rearranging gives,

$$p_{chan} = \frac{L}{q\mu_p RA}, \tag{5.15}$$

where L = 0.1 cm, W = 0.2 cm, $\mu_p \simeq 0.1$ cm^2/V-s (an estimate), $R = 1.6 \times 10^7$ Ω, and $A = 2 \times 10^{-6}$ cm^2. Using these values yields $p_{chan} = 2 \times 10^{17}$ cm^{-3}.

The threshold voltage may then be estimated using [69]

$$V_t = q p_{chan} t_{chan} \frac{t_{ins}}{\epsilon_{ins}\epsilon_0}, \tag{5.16}$$

where $p_{chan} = 2 \times 10^{17}$ cm^{-3}; $t_{chan} = 100$ nm; $\epsilon_{ins} = 10$, $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm; and $t_{ins} = 220$ nm. Using these values gives $V_t \simeq 8$ V. This is a very reasonable value for threshold voltage. According to this calculation, these NiO:Li p-TTFTs should work,

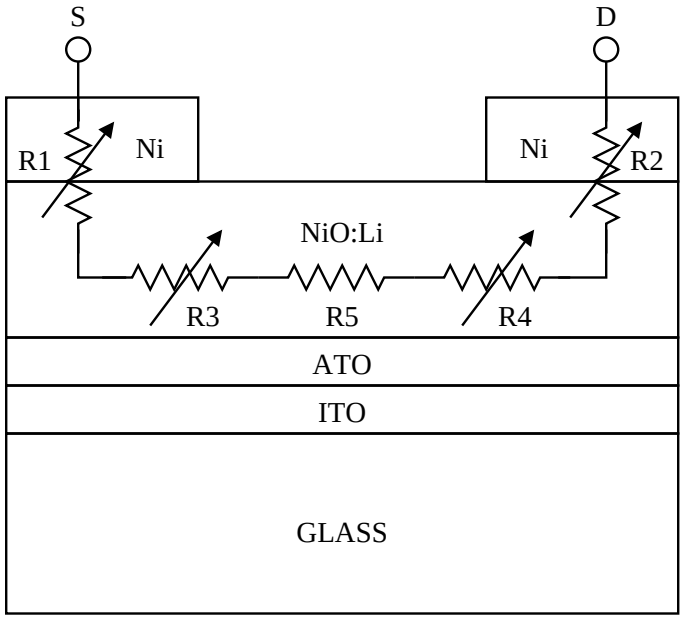


Figure 5.8: Contact and channel resistance model for a NiO:Li p-TTFT.

although it must be kept in mind that the mobility is estimated for this calculation of V_t. If the mobility is an order of magnitude less, 0.01 cm^2/V-s, then V_t would be an order of magnitude greater, 80 V. This calculation underscores the importance of the channel mobility in establishing the p-TTFT properties and performance.

To further demonstrate that an overly conductive channel layer can lead to the linear current-voltage characteristics seen in these devices, a lumped-parameter resistor model of a NiO:Li p-TTFT is shown in Fig. 5.8. This model shows a NiO:Li p-TTFT with contact and semiconductor resistances. R1 and R2 represent voltage-dependent contact resistances, modeling the imperfect nature of the source and drain contacts to the channel semiconductor. R3 and R4 represent voltage-dependent resistance of the channel due to conductivity modulation by the gate. R5 represents the intrinsic linear resistance of the channel. Since the current-voltage curves obtained for NiO:Li p-TTFTs are linear, it is reasonable to conclude that the intrinsic linear channel resistance is dominating these devices. The effects of an overly-conducting channel are discussed further in Sec. 5.4 in the context of a SPICE model of p-TTFT behavior.

5.3 $CuScO_2$ p-TTFTs

In this attempt at a p-TTFT, p-type, insulating $CuScO_2$ is used as the channel material, Au is used for the source and drain contacts, the gate insulator is SiO_2, and the gate is Al (p-TTFT Device No. 3, Table 5.1). $CuScO_2$ films used in this research were prepared by Matt Price in the Department of Physics and by Ben Nielsen in the Department of Materials Science at Oregon State University. Au as a contact to $CuScO_2$ is expected to be injecting because the workfunction of Au (5.1 eV) [63] is similar to the presumed valence band edge of $CuScO_2$. The valence band edge of $CuScO_2$ is expected to be in the range of 5 eV to 5.5 eV. This is based on the fact that Benko and Koffyberg found the valence band edges of $CuYO_2$ and $CuAlO_2$ to be 5.3 eV and 5.2 eV, respectively, which they assert is in the 5.0-5.5 eV range typical for oxides such as NiO, CuO, and Cu_2O whose valence band maxima are derived from metal $3d$ atomic states. [70]

5.3.1 Fabrication of $CuScO_2$ p-TTFTs

Devices are defined using shadow masks (Fig. 5.2). The 100 nm-thick $CuScO_2$ channel layer (width 2 mm, length 1 mm) is deposited by RF sputtering in 35 sccm of Ar and 0.5 sccm of O_2 at 90 W and 350°C. The films are annealed, first in O_2 at 850 °C and then in Ar at 900°C. The resistance of the channel layer is so large as to be unmeasurable with a multimeter (>40 MΩ). Au source and drain contacts are deposited by thermal evaporation. A ∼250 nm SiO_2 gate insulator is deposited by PECVD. Finally, an Al gate is deposited by thermal evaporation.

5.3.2 Discussion of $CuScO_2$ p-TTFTs

Current-voltage characteristics (Fig. 5.9) are obtained for $CuScO_2$ p-TTFTs using an HP 4140B picoammeter. These curves are similar to those obtained for undoped NiO p-TTFTs (Fig. 5.3). This similarity in behavior indicates that gate leakage current dominates $CuScO_2$ p-TTFT current-voltage characteristics, as it did in undoped NiO p-

TTFTs. I_d changes with gate voltage, but not with drain voltage. Thus, any transistor behavior that may be present is overwhelmed by the gate leakage current. The magnitude of current generated by the field effect would need to be increased to be greater than the gate leakage current to see any transistor behavior. This magnitude of the leakage current, about 1 μA, is likely too large to make a viable p-TTFT. A sample calculation may be made to determine how large of a transistor mobility is needed to produce a transistor current larger than 1 μA. Equation 3.6, the linear triode region current equation for a TFT, can be solved for mobility, μ_{eff}, as

$$\mu_{eff} = \frac{I_d}{C_{ins}\frac{W}{L}(V_{gs} - V_t)V_{ds}}. \tag{5.17}$$

The following values are used in this equation: $I_d = 1\mu$A, $C_{ins} = 17.3$ nF/cm^2 (using the dielectric constant of SiO_2, 3.9, and an insulator thickness of 200 nm), $\frac{W}{L} = 2$, $V_{gs} = 20$ V, $V_t = 5$ V, and $V_{ds} = 20$ V. These values yield a mobility of 0.1 cm^2/V-s. This is the minimum mobility required to obtain a transistor current at the (typical) values of V_{gs} and V_{ds} used in the equation. A mobility of 0.1 cm^2/V-s is large for an insulating p-type transparent material. The value calculated also puts an upper limit of 0.1 cm^2/V-s on the value of μ_{eff} for the $CuScO_2$ transistor. It is interesting to note that the PECVD SiO_2 which performed so poorly as a gate insulator in these $CuScO_2$ p-TTFTs performed much better in NiO p-TTFTs. Typical gate leakage currents for NiO p-TTFTs with PECVD SiO_2 gate insulators are on the order of 10^{-11} A to 10^{-10} A. Recall that $BaCu_2S_2$ p-TTFTs also had large gate leakage currents, even larger than $CuScO_2$ p-TTFTs. As discussed in Sec. 5.1.2 in the context of $BaCu_2S_2$ p-TTFTs, there may be interaction occurring between the channel layer and the gate insulator in both $BaCu_2S_2$ and $CuScO_2$ p-TTFTs. It seems likely that the Cu in these compounds is degrading the gate insulator, particularly since the same gate insulator performs much better in NiO p-TTFTs.

Note from Fig. 5.9 that there is more gate leakage current when the gate is negatively biased compared to a positive gate bias. This is is also the case for undoped NiO

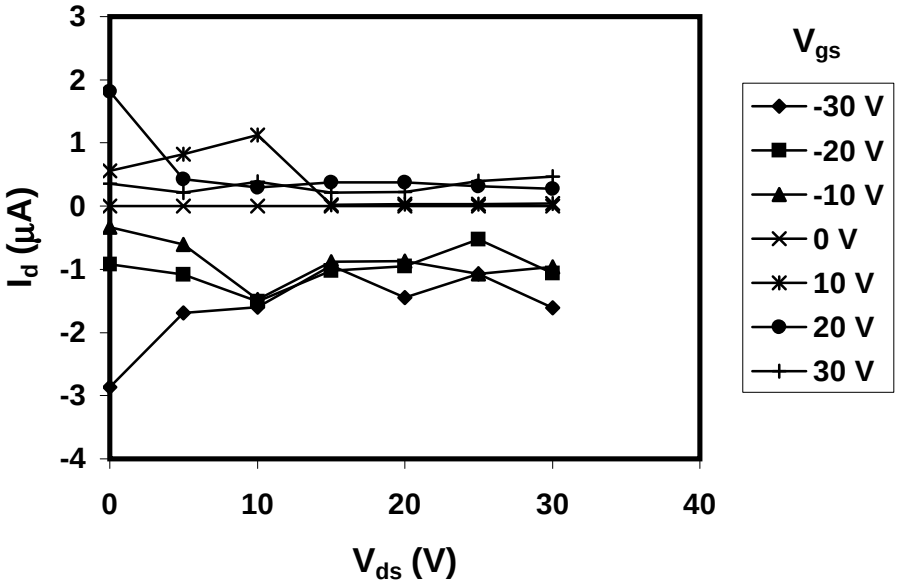


Figure 5.9: I_d versus V_{ds} curves for a p-TTFT with a $CuScO_2$ channel, Au source/drain contacts, SiO_2 gate insulator, and Al gate.

p-TTFTs. As discussed for undoped NiO p-TTFTs, this suggests that electron injection from the gate contact into the gate insulator is more effective for a negative gate bias than hole injection for a positive gate bias. Alternatively, a larger negative gate voltage leakage current could be ascribed to hole injection from the channel, through the gate insulator, to the gate contact. This hole injection from the channel, although possible, seems less likely since these $CuScO_2$ p-TTFTs provide no evidence for p-type behavior in the channel.

$CuScO_2$ is selected as a candidate p-TTFT channel material because it is a p-type insulator. Initially in this thesis research it was thought that lower carrier concentration in the p-TTFT semiconductor would be better, since according to Eq. 5.1 it would result in a low threshold voltage. The $CuScO_2$ p-TTFTs made in this work exhibited no transistor behavior, however, leading to a reassessment of this situation. It is possible that the $CuScO_2$ p-TTFTs do not work because injected carriers are being trapped in interface states and/or bulk traps, as discussed in Sec. 2.2.3.1. Another possibility for the failure of the $CuScO_2$ p-TTFTs is that the Au source and drain contacts may not be

injecting. This could be due to improper metal/semiconductor workfunction differences or Fermi-level pinning.

Hole injection in $CuScO_2$ p-TTFTs is now considered quantitatively. The hole injection barrier height for Ni or Au contacts on $CuScO_2$ is calculated as follows. The index of refraction for $CuScO_2$ is 2.1. [71] The high-frequency dielectric constant is calculated as the square of the index of refraction and is 4.41. The pinning factor, S, is calculated according to Eq. 5.2, and is equal to 0.46. Recall that S ranges from 0 to 1, with 0 indicating strong pinning and 1 indicating no pinning. The value of S for $CuScO_2$ is intermediate. S is then used to calculate the barrier height using Eq. 5.3, where $E_g + \chi_s \sim 5.25$ eV [26], $\phi_{CNL} = 4.5$ eV (using the universal charge neutrality level of Van de Walle and Neugebauer, see Sec. 2.3.2), and $\phi_m = 5.1$ eV. Using these values gives $\phi_{Bp} \sim 0.47$ eV. This is a fairly large barrier and may inhibit hole injection. The density of states for $CuScO_2$ is unavailable, and so it is not possible to perform a modified barrier calculation taking into account the location of the Fermi level in the bulk of $CuScO_2$ as was done for undoped NiO.

This calculation of ϕ_{Bp} does not conclusively determine if the failure of $CuScO_2$ p-TTFTs is due to poor injection. Carrier trapping in the insulating $CuScO_2$ channel is still considered a likely reason why these $CuScO_2$ p-TTFTs do not work. The effects of poor injection and carrier trapping are discussed further in Sec. 5.4 in the context of a SPICE model of insulating channel p-TTFT behavior.

5.4 SPICE Model of p-TTFT behavior

SPICE modeling (Fig. 5.10) is applied in this section to test the physical explanations for the current-voltage characteristics of $CuScO_2$, undoped NiO, and NiO:Li p-TTFTs. The model involves the use of a voltage-controlled current source to model $I_d(V_{ds},V_{gs})$ with parasitic resistors and capacitors between the terminals. C_{gd} and C_{gs} represent the gate capacitance. R_{gs} and R_{gd} represent leakage paths through the gate insulator to the source and drain terminals. Ideally, R_{gs} and R_{gd} are infinite in magni-

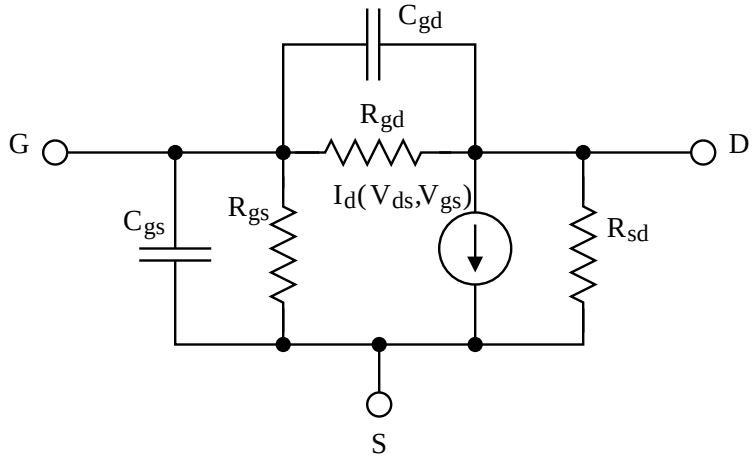


Figure 5.10: SPICE model for a TTFT.

tude, so that there is no gate leakage current. R_{sd} represents the channel conductivity. Ideally, R_{sd} is also infinite so that the only current that flows between the source and drain is due to the field effect, represented by $I_d(V_{ds},V_{gs})$. SPICE code used in these simulations is presented in Appendix A.

5.4.1 $CuScO_2$ and Undoped NiO p-TTFT Simulation

For the case of $CuScO_2$ and undoped NiO, the current-voltage characteristics obtained from experiment (Fig. 5.9 and Fig. 5.3) are dominated by the gate leakage current. The transistor field-effect current is so small (either due to the trapping nature of the channel or due to poor hole injection from the source to the channel) that the gate leakage current dominates. In the SPICE model, a small transistor field-effect current is represented by a small value of the transistor mobility. In the first SPICE simulation, shown in Fig. 5.11, the mobility is set to 10^{-3} cm^2/V-s. Figure 5.11 shows I_d versus V_{ds} curves at various values of V_{gs} from SPICE simulations for $CuScO_2$/undoped NiO p-TTFTs whose characteristics are dominated by gate leakage current. R_{sd} is kept at a large value (1 GΩ) in this simulation to represent the highly insulating channel layer. It is seen from Fig. 5.11 that simulation of poor mobility leads to I_d versus V_{ds} curves similar

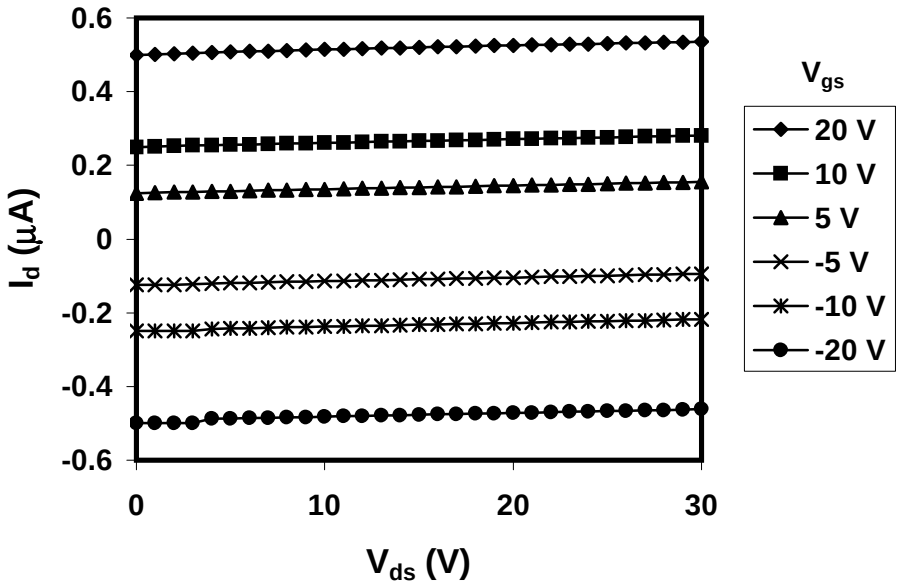


Figure 5.11: SPICE-generated I_d versus V_{ds} curves at various values of V_{gs} for a $CuScO_2$ or undoped NiO p-TTFT which is dominated by gate leakage current. In this simulation, $R_{sd} = 1$ GΩ, R_{gs} and $R_{gd} = 40$ MΩ, C_{gs} and $C_{gd} = 1$ pF, mobility $\mu = 0.001$ cm^2/V-s, $C_{ox} = 0.17$ F/cm (for SiO_2 gate insulator), and $V_t = 2$ V.

to those obtained from experiment (Fig. 5.3 and Fig. 5.9). A second SPICE simulation is performed in which the mobility is varied. Figure 5.12 shows I_d versus V_{ds} curves at $V_{gs} = 10$ V with channel mobility varying. From Fig. 5.12 it is seen that higher mobility leads to a familiar saturated I_d versus V_{ds} curve, while low mobility leads to a flat I_d versus V_{ds} curve like those obtained from experimental results on $CuScO_2$ and undoped NiO p-TTFTs. Note that the above pinch-off portions of the I_{ds} versus V_{ds} curves do not show strong saturation for which the slope of the I_{ds} versus V_{ds} curve is equal to zero because R_{sd} is not close enough to infinity. This underscores the need to reduce the conductance of the bulk portion of the channel in order to achieve the desired transistor behavior. These trends are almost self-evident when the SPICE model shown in Fig. 5.10 is considered, since the source-drain current arises from a parallel combination of the transistor field-effect current and the output resistance of the channel.

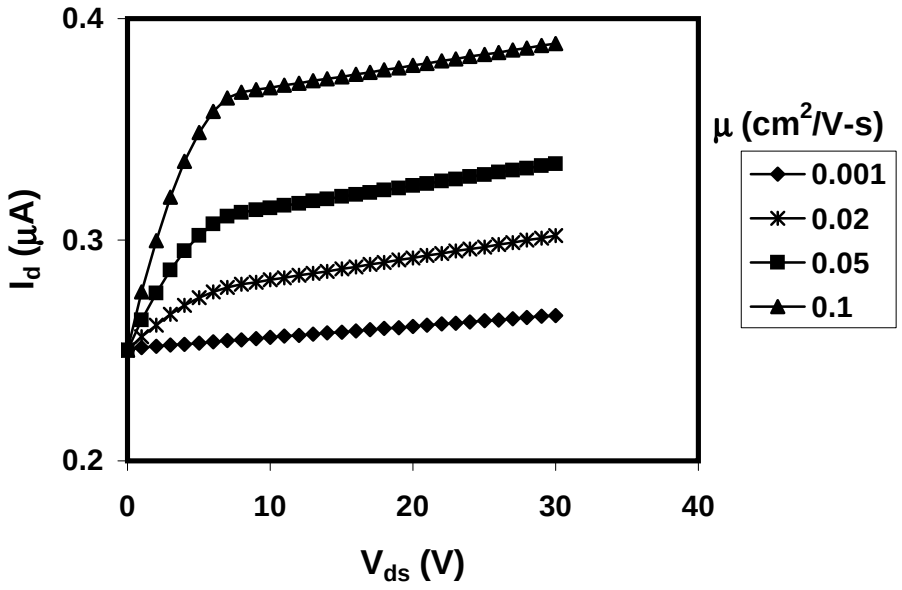


Figure 5.12: SPICE-generated I_d versus V_{ds} curves at a fixed $V_{gs} = 10$ V with channel mobility varying for a $CuScO_2$ p-TTFT. In this simulation, $R_{sd} = 1$ GΩ, R_{gs} and $R_{gd} = 40$ MΩ, C_{gs} and $C_{gd} = 1$ pF, $V_{gs} = 10$ V, $C_{ox} = 0.17$ F/cm (for SiO_2 gate insulator), and $V_t = 2$ V.

5.4.2 NiO:Li Simulation

For the case of NiO:Li, the current-voltage characteristics obtained from experiment (Fig. 5.7) are due to an overly conductive NiO:Li channel layer. In the SPICE model, this is represented by a smaller value for R_{sd}. Figure 5.13 shows the results of a SPICE simulation using various values for R_{sd} in the model. R_{gs} and R_{gd} are kept very large (1 GΩ) to simulate a gate with small leakage current. It is seen from Fig. 5.13 that as the channel conductivity increases (R_{sd} gets smaller), the transistor behavior seen from $I_d(V_{ds},V_{gs})$ when R_{sd} is large becomes masked by the large current through R_{sd} from the overly conductive channel layer.

5.5 Conclusions

This chapter describes work on the development of p-channel transparent thin-film transistors (p-TTFTs). Four materials are investigated for the channel layer of

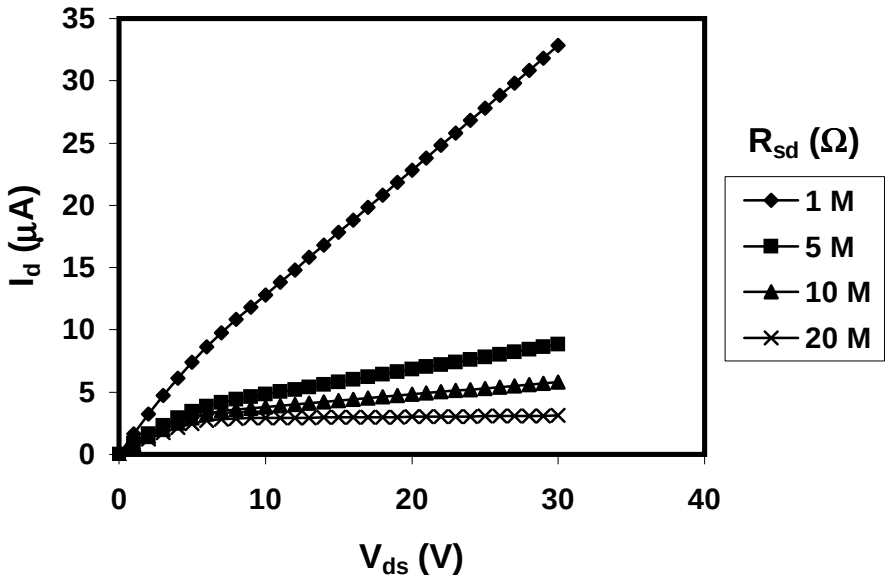


Figure 5.13: SPICE-generated I_d versus V_{ds} curves at a fixed V_{gs} with channel semiconductor resistance varying for a NiO:Li p-TTFT. In this simulation, R_{gs} and $R_{gd} = 1$ GΩ, C_{gs} and $C_{gd} = 1$ pF, mobility $\mu = 1$ cm^2/V-s, $V_{gs} = 10$ V, $C_{ox} = 0.44$ F/cm (for ATO gate insulator), and $V_t = 2$ V.

a p-TTFT: $BaCu_2S_2$:Zn, undoped NiO, NiO:Li, and $CuScO_2$. Although no successful devices are fabricated, some important considerations for the realization of p-TTFTs are elucidated. These considerations include injecting contacts, semiconductor channel conductivity, and insulator integrity. SPICE modeling of p-TTFTs is used successfully to test the physical explanations for p-TTFT current-voltage characteristics obtained in this research.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

One goal of this research is to investigate new p-type transparent conductors (p-TCs). p-TC $BaCuS_2$ thin films developed in this thesis research exhibit good conductivity and transparency over part of the visible portion of the electromagnetic spectrum. The properties of $BaCuS_2S_2$ make it a promising candidate material for $Cu(In,Ga)Se_2$ thin-film solar cells. $BaCu_2S_2$ may also prove to be an effective p-window layer in next-generation double heterojunction p-i-n thin-film solar cells.

A second goal is to explore p-type transparent thin-film transistors (p-TTFTs). Several p-TTFT structures are fabricated and tested in this work based on $BaCu_2S_2$, NiO, and $CuScO_2$. None of the devices work, but much progress has been made in the understanding of key issues surrounding p-TTFTs. The delicate balance in conductivity requirements of the channel layer semiconductor are better understood. The requirements for injecting contacts are clarified. It is hoped that the consideration and application of these ideas will lead to an operational p-TTFT in the near future.

6.2 Recommendations for Future Work

The research described in this thesis leaves several avenues to be explored. This section indicates potential directions to further this research.

6.2.1 Solar Cells

The use of $BaCu_2S_2$ in solar cells should continue to be investigated. $BaCu_2S_2$ is a promising candidate for use in $Cu(In,Ga)Se_2$ solar cells. The National Renewable Energy Laboratory is exploring this use of $BaCu_2S_2$. $BaCu_2S_2$ also has use as a p-window layer in new p-i-n solar cells being developed. This use of $BaCu_2S_2$ should be pursued. Aside

from $BaCu_2S_2$, other novel Cu-based materials should be explored for use in double heterojunction p-i-n thin-film solar cells.

6.2.2 p-TTFTs

Research described in this thesis on p-TTFTs should be continued. Use of the insights with regard to channel semiconductor conductivity and injecting contacts gained through this thesis research will help progress in this area. NiO p-TTFTs should continued to be pursued. Improper NiO channel conductivity seems to be the reason why NiO p-TTFTs fabricated in this research do not work. With dopants, the channel conductivity can be modified to an appropriate level. This will hopefully lead to an operational NiO p-TTFT. Additionally, Hall measurements should be made for NiO:Li thin films. $CuScO_2$ p-TTFTs should be explored further only if a controllable doping method is found, since the undoped $CuScO_2$ channel films used in this work were too insulating to produce a working p-TTFT. Further development is needed in the area of transparent injecting contacts for use in p-TTFTs. All of the contacts used in this thesis research were opaque. Using opaque contacts to prove the concept of a p-TTFT is acceptable, but transparent contacts are eventually needed. These contacts need to have large workfunctions (> 5 eV) to form injecting contacts to the p-type wide-bandgap semicondcutors used as channel layers in p-TTFTs. A further issue to explore is the isolation of gate insulators from Cu-containing compounds. In this thesis research there were large gate leakage currents in p-TTFTs made with $BaCu_2S_2$ and with $CuScO_2$, but not with NiO. The Cu in these compounds may be damaging the gate insulator. Barrier layers such as Si_3N_4 may be useful in preventing the degradation of gate insulators.

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APPENDIX

SPICE CODE

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SPICE MODEL FOR P-TTFTS TRIODE REGION
.OPTION POST NOMOD INGOLD=1
*ELEMENTS
RGD G D 100MEG
RGS G S 100MEG
RSD D S 1G
CGD G D 1p
CGS G S 1p
*TRANSISTOR CURRENT SOURCE
*I=MOBILITY*COX*W/L*[VGS-VT-(VDS/2)]*VDS
G1 D S CUR='1*0.44e-7*2*(V(G)-2-(V(D)/2))*V(D)'
*SOURCES
VGS G 0 10
VDS D 0 8
VSS S 0 0
*ANALYSIS
.DC VDD 0 8 1
.PLOT DC I(VSS)
.PRINT DC I(VSS)
.END
```

SPICE MODEL FOR P-TTFTS SATURATION REGION

```
.OPTION POST NOMOD INGOLD=1
*ELEMENTS
RGD G D 100MEG
RGS G S 100MEG
RSD D S 1G
CGD G D 1p
CGS G S 1p
*TRANSISTOR CURRENT SOURCE
*I=MOBILITY*COX*W/2L*(VGS-VT)2̂
G1 D S CUR='1*0.44e-7*1*(V(G)-2)*(V(G)-2)'
*SOURCES
VGS G 0 10
VDS D 0 8
VSS S 0 0
*ANALYSIS
.DC VDD 0 8 1
.PLOT DC I(VSS)
.PRINT DC I(VSS)
.END
```