AN ABSTRACT OF THE THESIS OF

Brian Ross McFarlane for the degree of Master of Science in
Electrical and Computer Engineering presented on September 24, 2008.
Title: Amorphous Oxide Semiconductors in Circuit Applications

Abstract approved: _____

John F. Wager

The focus of this thesis is the investigation of thin-film transistors (TFTs) based on amorphous oxide semiconductors (AOSs) in two circuit applications. To date, circuits implemented with AOS-based TFTs have been primarily enhancement-enhancement inverters, ring oscillators based on these inverters operating at peak frequencies up to ∼400 kHz, and two-transistor one-capacitor pixel driving circuits for use with organic light-emitting diodes (OLEDS). The first application investigated herein is AC/DC rectification using two circuit configurations based on staggered bottom-gate TFTs employing indium gallium oxide (IGO) as the active channel layer; a traditional full bridge rectifier with diode-tied transistors and a cross-tied full-wave rectifier are demonstrated, which is analogous to what has been reported previously using p-type organic TFTs. Both circuit configurations are found to operate successfully up to at least 20 MHz; this is believed to be the highest reported operating frequency to date for circuits based on amorphous oxide semiconductors. Output voltages at one megahertz are 9 V and ∼10.5 V, respectively, when driven with a differential 7.07 V_{rms} sine wave. This performance is superior to that of previously reported organic-based rectifiers.

The second AOS-based TFT circuit application investigated is an enhancement-depletion (E-D) inverter based on heterogeneous channel materials. Simulation results using models based on a depletion-mode indium zinc oxide (IZO) TFT and an enhancement-mode IGO TFT result in a gain of ∼15. Gains of other oxide-based inverters have been limited to less than 2; the large gain of the E-D inverter makes it well suited for digital logic applications. Deposition parameters for the IGO and IZO active layers are optimized to match the models used in simulation by fabricating TFTs on thermally oxidized silicon and patterned via shadow masks. Integrated IGO-based TFTs exhibit a similar turn-on voltage and decreased mobility compared to the shadow masked TFTs. However, the integrated IZO-based TFTs fabricated to date are found to be conductive and exhibit

no gate modulation. Due to the conductive nature of the load, the fabricated E-D inverter shows no significant output voltage variation. This discrepancy in performance between the integrated and shadow-masked IZO devices is attributed to processing complications.

Amorphous Oxide Semiconductors in Circuit Applications

by

Brian Ross McFarlane

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented September 24, 2008
Commencement June 2009

Master of Science thesis of Brian Ross McFarlane presented on September 24, 2008

APPROVED:

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Brian Ross McFarlane, Author

ACKNOWLEDGMENTS

First and foremost, I would like thank my parents and friends for their unwavering support. They provide the inspiration needed to be successful and are constant sources of stability and genuine happiness, the combination of which has allowed me to remain sane and confident.

I would like to thank my adviser, Dr. Wager, for providing the opportunity and support for working on this project. His willingness to meet on short notice to discuss technical issues has been greatly appreciated, and his patience and thoroughness when exploring new problems never ceases to amaze.

A great deal of credit is deserved by the past and present senior members of the research group. Notably, I would like to thank Hai Chiang, David Hong, Rick Presley, and Eric Sundholm for providing the training necessary to be successful in the lab and numerous helpful technical discussions. Rick and Eric also performed the in-house deposition of the PECVD silicon dioxide used for some initial results with the rectifiers and for the entirety of the enhancement-depletion inverter experiment, for which I am grateful. I would also like to acknowledge Chris Tasker; he keeps the lab running and is always focused on enabling graduate students to perform their research.

Many thanks are also owed to Peter Kurahashi of the Oregon State University Analog and Mixed Signal (AMS) group. His insight into circuits, experience with the analytical tools available in the AMS lab, and familiarity with the Cadence software package has saved countless hours of work and frustration. His genuine enthusiasm for the task at hand and positive nature have made working with him an enjoyable and enlightening experience.

I would also like to thank Tim Emery of the Hewlett-Packard Company and Greg Herman of Sharp Labs of America for their continued support of our endeavors here at Oregon State University. Both Tim and Greg arranged for the deposition of PECVD SiO_2 on very short notice at their respective facilities while our in-house tool was down for extended maintenance. Without these resources, progress could not have been made on the development and fabrication of the integrated circuits reported herein.

Finally, I would like to thank all of my fellow group members and lab mates for making my tenure here a pleasurable one. In addition to the previously mentioned individuals, this includes Daniel Heineck, Richard Schafer, Ken Hoshino, and Bill Cowell of Dr. Wager's group and Stephen Meyers, Jeremy Anderson, Chris Knutson, and Kai Jiang of Dr. Keszler's group.

This work was funded by the Hewlett-Packard Company and the Defense Advanced Research Projects Agency (MEMS/NEMS: Science and Technology Fundamentals).

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1. INTRODUCTION

As the ability to shrink integrated semiconductor devices down to dimensions measurable by the number of atoms involved, the amount of computing power relative to the required physical size and electrical power consumption for an integrated circuit has skyrocketed. A consequence of this phenomenon is that electronics are now ubiquitous in our society and the general public has come to expect a level of sophistication and capability from common electronics that would have seemed preposterous only a decade ago. It is currently possible to buy cell phones that have high-resolution full-color screens, five megapixel cameras, internet browsers, wireless audio streaming to headsets or cars, touch screens that can recognize multiple inputs simultaneously, and thicknesses that are measured in millimeters. Consumer television screens are pushing to larger sizes, higher resolutions, and higher contrast ratios while simultaneously decreasing thickness down to inches. Finally, an increasingly large number of people are finding themselves unlocking doors at their offices and on their cars without ever inserting a key.

One common theme that runs through all of these examples of electronic devices is that they rely on circuitry that is implemented in silicon. While this is undoubtedly the most mature technology available, there are several applications for which conventional single-crystal silicon is ill-suited: it is not flexible, it is not transparent, processing it is expensive, and it does not scale well to large area applications. Amorphous oxide semiconductors, which are transparent in the visible portion of the electromagnetic spectrum, represent a new class of materials that have the potential to be used in applications in which single-crystal silicon is an inappropriate choice. This may create new, novel markets such as transparent or highly flexible displays.

The focus of this thesis involves the design, simulation, and fabrication of both a rectifying circuit and an enhancement-depletion (E-D) inverter using amorphous oxide semiconductors. To date, oxide-based semiconductors have primarily been integrated as enhancement-enhancement inverters configured as ring oscillators. The rectifier represents another way to benchmark the practicality of using this nascent technology in a circuit application. In addition, a rectifier serves as a very practical component in power conditioning which could be used in a multiplicity of future applications, such as harvesting power from wireless transmissions, which could be the case if used

with a radio-frequency identification (RFID) transponder. For an NMOS oxide-based inverter, a depletion load is the most ideal load currently available. An (E-D) inverter is expected to demonstrate an improved gain compared to previously reported enhancement-enhancement inverters; this larger gain makes an E-D inverter an attractive choice for future digital logic applications.

The structure of this thesis is as follows. Chapter 2 contains a review of pertinent literature and provides the basic background information necessary to establish a context for discussing the experimental results. Chapter 3 details the necessary processing steps, tools, and techniques used to fabricate discrete devices and circuits, in addition to a discussion of relevant device and circuit characterization methods. Chapter 4 details fabrication and characterization of the rectifying circuits. Chapter 5 discuses the simulation results, integration, and electrical characterization of an enhancement-depletion inverter. Finally, Chapter 6 provides conclusions and paths for future work.

2. LITERATURE REVIEW

This chapter presents background information on thin-film transistors (TFTs) and transparent electronics to provide the reader with the historical context and necessary technical background to understand the work contained within this thesis. A summary of reports of amorphous oxide semiconductor based TFTs in the literature is presented in addition to a sampling of the most common circuit applications for TFTs. Finally, the performance of an alternating-current to direct-current (AC/DC) rectifier implemented with organic-based TFTs is presented for comparison to the results obtained in this body of work.

2.1 Thin-Film Transistors

The concept of a TFT can be traced back to patent applications filed in 1925 and 1926 by Lilienfeld. [1] While the most technically correct name for these devices is "thin-film insulated-gate field-effect transistors" the simpler term "thin-film transistor" was used by Weimer to describe the first successful vacuum-deposited field-effect device fabricated in 1961. [2] It is now common practice to refer to these devices as TFTs, with the insulated-gate and field-effect nature being implied even if unstated.

2.1.1 Thin-Film Transistor Structure

Thin-film transistors are similar in operation and structure to metal-oxide-semiconductor field-effect transistors (MOSFETs) which are widely used in single-crystal silicon applications such as memory cells and microprocessors. Like MOSFETs, TFTs are three-terminal devices with a source terminal for injecting carriers, a drain terminal for extracting carriers, and a gate terminal for modulating the conductivity of the channel. They are fabricated by subsequent deposition of conducting, insulating, and semiconducting thin films onto an insulating substrate. The ability to use an insulating substrate, such as glass or plastic, has three benefits compared to using a semiconducting substrate. First is the substantially lower material cost and second is that the insulating material inherently eliminates problems such as parasitic capacitances and latch-up which are either unavoidable or require additional isolation when using a semiconducting substrate. [2] Finally, since the semiconducting layer, where the conducting channel is induced during device operation, is deposited onto rather than built into the substrate, there is more freedom in the way in which the device can be structured.

Figure 2.1 illustrates the four most common arrangements of the thin film layers constituting a TFT. [3, 4] TFTs are classified as either coplanar or staggered, and these terms refer to whether

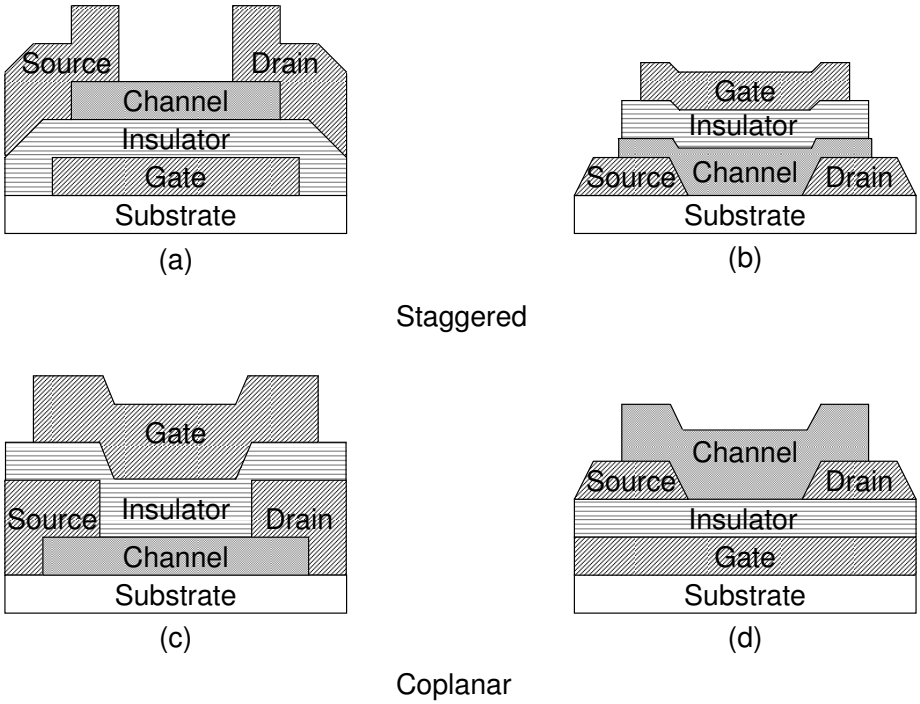


Figure 2.1: The four most common TFT structures. Defining features include whether the structure is staggered or coplanar and the location of the gate. If the gate insulator is on the same side of the channel material as the source and drain contacts, then the structure is said to be coplanar as illustrated in (c) and (d). If the gate insulator is on the opposite side of the channel material as the source and drain contacts, then the structure is in a staggered arrangement as illustrated in (a) and (b). Structures that have the gate electrode on top of the stack are said to be top-gated while structures that have their gate electrodes on the bottom are referred to as bottom-gated or inverted.

or not the gate capacitor is on the same or opposite side of the channel material as the source/drain terminals, respectively. In a coplanar device, the source and drain contacts are in direct contact with the induced channel while in a staggered structure the induced channel occurs on the opposite side of the deposited channel material compared to where the source and drain contacts are located. Thus, injected carriers need to first travel vertically to reach the induced channel before they can be transported across the length of the channel. [5] Staggered structures are often used in conjunction with amorphous-silicon (a-Si) TFTs because it is easier to ensure sufficient overlap between the source and drain contacts and the induced channel layer, thus minimizing series resistance which would otherwise degrade TFT performance. [3]

The other fundamental structural permutation is the location of the gate capacitor in relation to the channel layer. TFTs can either have a top-gate, where the gate electrode is above the channel

and on top of the device, or a back-gate where the gate electrode is underneath the channel. The latter is also referred to as an inverted structure. The staggered back-gate structure is the most widely used in liquid crystal display (LCD) panels [3] and also in many research groups investigating novel materials. If a heavily-doped silicon wafer with a thermally grown silicon dioxide dielectric (which is widely available) is used to fabricate a TFT, the Si/SiO_2 layers act as the metal and insulator of the back-side gate capacitor structure and all that is required to complete the device is deposition of the channel layer and source/drain contacts. If patterning is accomplished using shadow-masking, this is a simple two deposition process which can facilitate rapid exploration of a material's electrical properties.

2.1.2 Thin-Film Transistor Operation

To understand the operation of a TFT, it is helpful to first examine the metal-insulator-semiconductor stack in three different scenarios: zero, negative, and positive applied gate biases. Figure 2.2 illustrates the band bending in an unipolar n-type semiconductor and the relative shift of the metal Fermi level compared to the semiconductor Fermi level under these three conditions. With no applied bias, as depicted in Fig. 2.2(a), the system is in equilibrium or a flat-band state and ideally there is no impact on the carrier concentration at the semiconductor-insulator interface. When a negative bias is applied to the gate, delocalized majority carrier electrons in the semiconductor are repelled and there is a depletion of majority carriers at the semiconductor-insulator interface, as depicted by the positive curvature of the bands in Fig. 2.2(b). However, when a positive bias is applied to the gate, delocalized electrons are attracted towards the interface and this creates an accumulation layer of free majority carriers. It is this accumulation layer that is referred to as the induced channel in a TFT and it is what allows for conduction between source and drain terminals.

If the gate is positively biased, so as to induce a channel, and the source and drain terminals are now also considered, current flow along the channel can be achieved by applying a positive voltage to the drain to extract electrons in the channel while keeping the source grounded. According to the square-law model of TFT behavior [6], when the applied drain voltage V_{DS}, is less than the pinch-off voltage, V_{DSAT}, the drain current I_D is in the pre-saturation regime and is described as

$$I_D = \frac{W}{L}\mu C_G[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^2}{2}] \tag{2.1}$$

where C_G is the gate capacitance, the turn-on voltage V_{ON} is defined as the smallest applied gate voltage that causes a non-negligible increase in drain current for a given drain voltage, W and L are

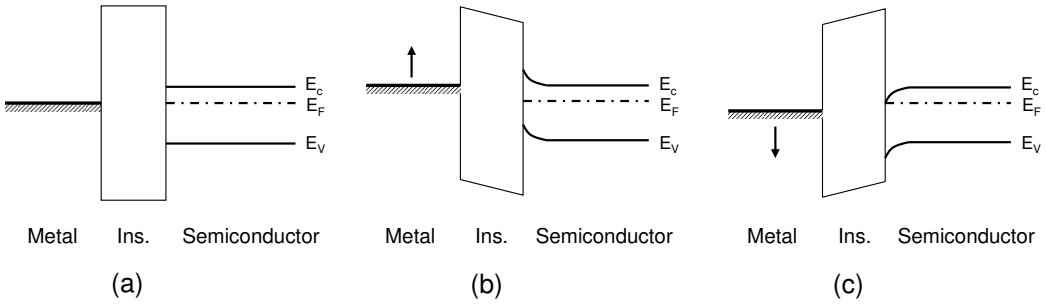


Figure 2.2: Energy band diagrams for a metal-insulator-semiconductor capacitor, assuming a unipolar n-type semiconductor under three gate bias conditions: (a) no bias, (b) negative bias, and (c) positive bias. With no bias on the gate, Fermi levels are aligned and there is no band bending. When a negative bias is applied, the metal Fermi level moves up relative to the semiconductor and the delocalized majority carriers (electrons) are repelled away from the semiconductor-insulator interface. This results in positive localized charge remaining near the interface, and hence positive curvature of the bands. When there is a positive voltage applied to the gate, the metal Fermi level moves down relative to the semiconductor and free electrons are attracted to the interface, forming an accumulation layer of electrons where conduction can occur. This results in the negative curvature in the bands.

the TFT's width and length, and μ is the mobility. A more thorough description of the electrical parameters V_{ON} and μ is provided in Chapter 3.

As the drain voltage increases and exceeds $V_{DSAT} \equiv V_{GS}$-V_{ON}, the drain current ideally becomes independent of the drain voltage and is said to be in the saturation regime where I_D is given by

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_G(V_{GS} - V_{ON})^2. \tag{2.2}$$

If $V_{GS} < V_{ON}$ or if V_{DS} is negative, then the TFT is said to be operating in the cutoff regime and it is assumed, according to the simplistic square-law model, that $I_D = 0$. These three equations for I_D and V_{DSAT} constitute the square-law model and allow the drain current to be modeled for any given combination of drain and gate voltages.

Thin-film transistors are also classified by the sign of V_{ON}. If V_{ON} is positive for an n-channel TFT, then no current flows when there is zero applied bias to the gate (i.e. the device is normally off) and the device is referred to as an enhancement-mode device. If V_{ON} is negative, then there is a sufficiently high carrier concentration in the channel that even with no applied bias to the gate, conduction between the source and drain can occur (i.e. the device is normally on). In this case, a negative gate voltage is required to turn the TFT off and the transistor is referred to as a depletion-mode device. Enhancement-mode TFTs are generally preferred in circuit applications

because of their normally off nature and lower power consumption, but depletion-mode devices can be useful in certain circuit applications, e.g., as active loads.

2.2 Transparent Electronics

The phenomenon of a material being both optically transparent and electrically conductive was first observed in 1907 with a cadmium oxide film. However, it was not until the 1940s that transparent conducting oxides (TCOs), specifically tin oxide (SnO_2), found widespread use as electric defrosters for airplane windscreens. [7] Since then, TCOs have been used for their optical properties as infrared-reflecting coatings in a variety of markets including energy-conserving low emissivity windows, eye glasses, and oven windows. Utilizing both their optical and electrical properties simultaneously, TCOs have been an enabling technology for flat-panel liquid crystal displays and solar cells when employed as front electrodes. [8]

One common theme among these aforementioned markets is that all of these applications use TCOs in a passive manner. If a material set can be found that is transparent and exhibits semiconducting properties, then a paradigm shift can occur and active transparent devices, namely transistors, can be made. This would enable complex and entirely transparent circuits to be investigated. This material set has two special requirements: a large enough band gap to be optically transparent (i.e. $E_{GAP} > 3.1$ eV) and a well controlled and low carrier concentration. [9]

2.2.1 Oxide-Based Transparent Semiconductors

The first two material sets to be explored in active devices that meet these criteria are tin oxide (SnO_2) and zinc oxide (ZnO). The first reports of TFTs fabricated with these materials as the channel layers date back to 1964 and 1968, respectively, but these initial reports either do not include the electrical characteristics or perform so poorly that their classification as a transistor is questionable. [6] In 1996 there was a report of a ferroelectric transparent TFT based on an antimony-doped SnO_2 channel with a ferroelectric $Pb(Zr,Ti)O_3$ insulator. A mobility of 5 $cm^2V^{-1}s^{-1}$ is reported in addition to an I_D-V_{GS} transfer curve when the gate material is $SrRuO_3$, an opaque material. The claim is made that heavily-doped SnO_2 was used also implemented as the gate electrode to realize a fully transparent structure, but no supporting electrical measurements, parameters, or evidence is otherwise presented with regards to this claim. [10] While the primary interest of this paper seems to be the all thin-film construction of the device and the ferromagnetic nature of the hysteresis, this appears to be the first successful realization of a transparent TFT (TTFT) in the literature.

In February of 2003, three groups published results of TFTs based on ZnO. [11, 12, 13] All three groups presented successful transistor operation while two groups realized a TTFT. [11, 12] Deposition methods included ion beam sputtering, rf magnetron sputtering, and pulsed laser deposition. All groups saw I_{on}/I_{off} ratios $> 10^5$, mobilities on the order of 1 $cm^2V^{-1}s^{-1}$, and drain currents in the tens of microamps. Bulk zinc oxide is a crystalline material with an hexagonal wurtzite structure that typically takes on a c-axis orientation; it cannot be deposited in an amorphous form, thus the reported films are all polycrystalline and conduction is limited by grain boundaries. This simultaneous successful demonstration of TFTs based on oxide semiconductors marks the beginning of a renewed interest in the development of invisible circuits with the most desirable applications arguably being either a fully transparent display or a display that is novelly thin.

At this point a brief discussion of the value of and technologies that dominate the current display market is relevant. The popularity of conventional cathode-ray tube (CRT) displays, which had been the backbone of the display industry since its inception, has been overtaken in the last decade by numerous flat-panel display (FPD) technologies, including liquid crystal displays (LCDs) and plasma display panels (PDPs). This shift in the market is mostly attributed to a desire to increase the viewing area of displays and the voluminous nature of CRT displays; as the display area of a CRT increases, so must the volume of the entire display. Of the two main FPD technologies, LCDs currently offer the most attractive mix of value and performance. In 2001 alone, shipments from LCD manufacturers were valued at more than 20 billion dollars. [14]

Current state-of-the-art LCDs are based on active-matrix-addressed LCDs which rely on TFTs to determine the state of each pixel over the entire area of the display. The substrates for these displays are glass panels with dimensions up to 195 cm x 225 cm. Due to these large areas, the semiconducting layer needs to be able to be deposited in a highly scalable manner to accommodate these dimensions and an amorphous material is preferred in order to achieve uniformity and reproducibility in transistor performance across the entire substrate. The current industry-standard is to use hydrogenated amorphous silicon (a-Si:H) as the semiconductor. While from a materials performance perspective this does not seem to be an optimal choice, the decision is due more to economics and the large amounts of experience and investment in working with single-crystal silicon and its integration challenges. [3] One of the biggest detriments of a-Si:H is the substantial degradation in mobility when compared to its single-crystal counterpart; in a-Si:H best-case mobilities are on the order of 1 $cm^2V^{-1}s^{-1}$, a full two orders of magnitude less than what is typical for single-crystal silicon. With such a low mobility, these a-Si:H TFTs are unable to drive

large currents while maintaining a high packing density and are thus used almost exclusively as voltage switches in display applications.

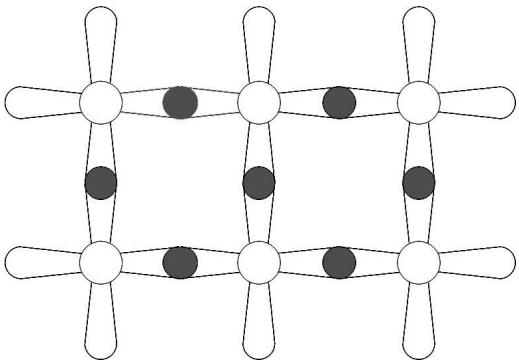
2.2.2 Amorphous Oxide Semiconductors

Based on potential FPD market applications and also on previous findings related to grain-boundary-limited conduction in zinc oxide films, it seems that there is at least a third criteria for an ideal transparent semiconductor: it should be amorphous. As an added benefit, if the material could have relatively high mobility (as compared to a-Si:H) then more complex applications could be realized.

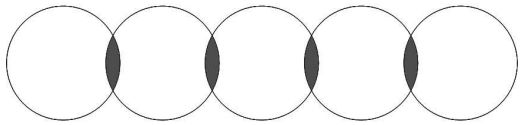
In 1996, Hosono *et al.* proposed a hypothesis for finding amorphous wide band-gap oxide semiconductors that should exhibit improved mobilities over amorphous covalent semiconductors such as silicon. [15] The key observation is that in semiconductors like silicon, the bottom of the conduction band is derived from highly-directional sp^3 hybrid orbitals of the Si atoms and the mobility is directly affected by the amount of overlap of these orbitals between neighboring Si atoms. In oxide-based semiconductors the conduction band is based on the cation (i.e. the metal atom's) valence shell, and if the appropriate cation is chosen, then the valence shell consists of large spherical s orbitals.

Figure 2.3 illustrates the implications of this observation on crystalline and amorphous arrangements of both material sets. It is apparent that when the covalent semiconductor is amorphous the predictability and amount of overlapping electron orbitals between neighboring atoms suffers dramatically compared to the crystalline state; this results in the electrons in the amorphous material relying on a hopping mechanism to be transported from site to site; hence the large reduction in mobility. In an oxide-based semiconductor, the large isotropic spherical orbitals allow for a substantial amount of overlap between neighboring atoms regardless of variations in their bonding angles. Hence there is substantially less difference in the mobility between the crystalline and amorphous states.

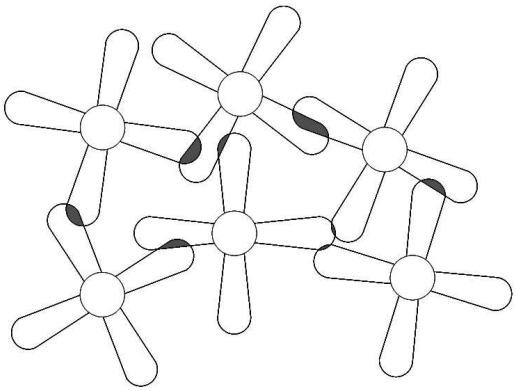
The specific criteria for cation selection proposed by Hosono *et al.* is to use heavy metal cations (HMCs) that have an electronic configuration of $(n\text{-}1)d^{10}ns^0$, where $4 \leq n \leq 6$. [16] This restricts the choice of cation to a rectangle in the periodic table consisting of the following 15 elements: copper, zinc, gallium, germanium, arsenic, silver, cadmium, indium, tin, antimony, gold, mercury, thallium, lead, and bismuth. In addition to targeting these specific atoms, it was also suggested that "double oxides" are preferable to single oxides to ensure the formation of an amorphous film. To support the hypothesis of finding new, high-mobility amorphous films three double oxides were formed: a-$AgSbO_3$, a-Cd_2PbO_4, and a-Cd_2GeO_4. All three films were reported



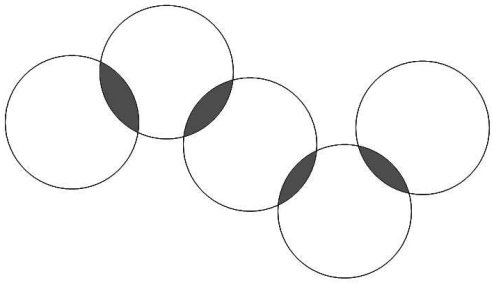
(a) Crystalline Covalent Semiconductor



(b) Crystalline Heavy-Metal Cation Semiconductor



(c) Amorphous Covalent Semiconductor



(d) Amorphous Heavy-Metal Cation Semiconductor

Figure 2.3: Comparison of atomic orbital overlap for covalent semiconductors versus amorphous oxide semiconductors (AOSs) in both amorphous and single crystalline configurations. The conduction band of covalent semiconductors is derived from highly directional sp^3 hybrid orbitals while the conduction band in AOSs is derived from large isotropic s orbitals. The amount of overlap between neighboring atomic orbitals has a direct impact on the mobility of a material; hence when a covalent semiconductor is in an amorphous state there is a substantial decrease in carrier mobility when compared to the crystalline material. In AOSs, the overlap is relatively unchanged between the two states. Thus, the mobility of the two material configurations is comparable.

to be amorphous and to have a mobilities of approximately 10 $cm^2V^{-1}s^{-1}$. This paper effectively marks the beginning of a newly recognized class of materials, henceforth referred to as amorphous oxide semiconductors (AOSs). After the success of the single oxide ZnO TFTs in 2003, the interest in multi-oxide semiconductors grew rapidly and the first successful AOS TFTs and TTFTs were quickly realized.

2.3 Previous Reports of AOS-based TFTs

In the last 4 years there has been a large amount of work published in the area of AOS-based TFTs. The purpose of this section is to report the most interesting and relevant findings in regard to transistor performance and stability, since these metrics are an integral part of the research reported herein. The organization of this section is by material, proceeding in chronological order (by year) to illustrate the evolution of this field. Materials examined include indium gallium zinc oxide, zinc tin oxide, indium gallium oxide, indium zinc oxide, and zinc indium tin oxide.

2.3.1 Indium Gallium Zinc Oxide

In 2004, Nomura and Hosono *et al.* reported transparent flexible TFTs based on amorphous indium gallium zinc oxide (IGZO). [17] The IGZO films are deposited by pulsed laser deposition (PLD) in an oxygen atmosphere with varying oxygen pressure P_{O_2}. The deposited IGZO films have a composition of In : Ga : Zn = 1.1 : 1.1 : 0.9. Based on Hall measurements, the carrier concentration varies from $<10^{14}$ cm^{-3} to $\sim10^{20}$ cm^{-3} when P_{O_2} is varied from $\sim$7 to 0.1 Pa.

Top gate TTFT structures are fabricated on flexible and transparent substrates of 200 μm thick polyethylene terephthalate (PET). The gate insulator is 140 nm thick yttrium oxide (Y_2O_3) while the source, drain, and gate electrodes are an indium oxide film doped with 10% tin (this type of film is commonly referred to as indium tin oxide, ITO). All films in this structure are deposited by PLD at room temperature and patterned using photolithography and lift-off techniques. The I_D-V_{DS} characteristics of these TTFTs exhibit pinch off and hard current saturation. A saturation mobility $\mu_{sat} = \sim$8.3 $cm^2V^{-1}s^{-1}$ and a field-effect mobility $\mu_{FE} = \sim$5.6 $cm^2V^{-1}s^{-1}$ are reported. Transfer curves show an off current of $\sim10^{-7}$ A, an on-to-off ratio of $\sim10^3$, a positive threshold voltage V_T = 1.6 V, and small hysteresis of 0.1 - 0.5 V which is attributed to interface states. The TTFTs are also measured while bent with a surface curvature radius R of 30 mm. There is a slight decrease in the drain saturation current, but the measured characteristics are otherwise unchanged.

In 2006, Yabuta *et al.*, in conjunction with Nomura and Hosono, reported the fabrication of radio frequency (rf) magnetron sputtered IGZO TFTs with no intentional heating during process-

ing. [18] A staggered top-gate structure is utilized with the gold/titanium stack comprising the source/drain contacts first being deposited via electron-beam (e-beam) evaporation. The channel is then sputtered from a ceramic target to a thickness of 50 nm in an argon/oxygen atmosphere of varying ratios with a total pressure of 0.53 Pa. The final film composition is In : Ga : Zn = 1 : 0.9 : 0.6, which is similar to, but more indium rich, than the film deposited by PLD. Yttrium oxide is used as the insulator and is also sputter deposited to a target thickness of 140 nm. The top gate contact is the same e-beam evaporated gold/titanium stack as the source/drain contacts. Contacts are patterned using shadow masks while the remainder of the TFT stack is patterned using photolithography and and lift-off techniques. Sticker-type temperature indicators are used to monitor substrate temperatures during sputtering; a temperature of 40 °C is reached during the IGZO deposition and a peak temperature of 140 °C is reached during the insulator deposition.

Device performance is an improvement over the previously reported PLD deposited IGZO TFTs. A field-effect mobility of 12 $cm^2V^{-1}s^{-1}$ with a threshold voltage of 1.4 V and on-to-off current ratios as high as 1×10^8 are reported. The effect of oxygen partial pressure is also reported, with devices fabricated at P_{O_2} = 0.016 Pa having conductivities greater than 10^{-3} S·cm^{-1} and exhibiting poor transistor performance. When the O_2 pressure is increased to between 0.017 and 0.020 Pa, working transistors are fabricated with conductivities less than 10^{-4} S·cm^{-1}.

In 2007, Iwasaki *et al.* reported on the optimization of IGZO TFTs from a compositional perspective. [19] Staggered bottom-gate TFTs are fabricated on 3-inch n-type silicon wafers with a layer of thermally grown silicon dioxide by co-sputtering zinc oxide (ZnO), gallium oxide(Ga_2O_3), and indium oxide (In_2O_3) until a channel thickness of 50 nm is achieved. The devices are finished with an Au/Ti stack for the source/drain contacts. By compositionally grading the IGZO film across the substrate, the impact of the different cations on the electrical performance can be examined by measuring transistors at different locations on the wafer. Based on channel dimensions, the compositional variation in the channel is estimated to be less than 0.2%.

Several important trends are observed. For an approximately constant zinc ratio of 31-34 atomic percent, an increase in the indium to gallium ratio ($\frac{In}{In+Ga}$) corresponds to an increase in μ_{sat} while $I_{on/off}$ decreases (due to a higher off current) and a negative shift in V_{th} is observed. TFTs with zinc-rich channels show an improved subthreshold swing. By correlating a ternary map of the three cations with transistor performance and electrical conductivity, good transistors seem to correspond to films that have conductivities between 10 and 10^{-3} S·cm^{-1} and have a composition that is located between the indium-rich (high conductivity) and gallium-rich (low conductivity) areas of the ternary map. This optimum area, which corresponds to small positive

threshold voltages, shifts towards the In-rich portion of the map as the oxygen pressure used during the channel deposition increases.

Mobility is observed to be strongly related to the indium content of the film. This illustrates the importance of large s orbital overlap for achieving high mobilities in amorphous films and is seen as support for Hosono's hypothesis about the conduction mechanism (indium has a 5s valence shell). At higher oxygen deposition pressures, the addition of gallium appears to compensate for the carrier generation due to large amounts of indium in the film. It is suggested that the gallium is suppressing the formation of oxygen vacancies. This suppression is important in regard to being able to control the carrier concentration while still having a large amount of indium to maintain good semiconductor properties. Based on its impact to the subthreshold swing, the contribution of zinc is hypothesized to either modulate shallow tail states below the conduction band or to reduce the interface states at the semioncductor/insulator interface.

The best TFT performance is achieved with a compositional ratio of In : Ga : Zn = 37 : 13 : 50. This ratio corresponds to a saturation mobility of 12 $cm^2V^{-1}s^{-1}$, a threshold voltage of 3 V, and an on-to-off ratio of 7×10^7. The caveat is provided that the optimum composition for a specific application should be chosen after further study of long-term stability, process margins, and device specifications.

Suresh *et al.* fabricated bottom-gated a-IGZO TTFTs in 2007 via room temperature PLD onto commercially available glass/ITO/aluminum titanium oxide (ATO) substrates. [20, 21] ATO is an atomic layer deposited superlattice of of AlO_X and TiO_X that is found to have an average capacitance of 55 $nF{\cdot}cm^{-2}$ for a 220 nm thick film. [20] All electrodes are ITO, with the source/drain electrodes being deposited at room temperature by PLD. The channel thickness is 50 nm, with the entire structure exhibiting roughly 80% transmittance in the optical spectrum. The IGZO TTFTs exhibit hard saturation, a saturation mobility of 11 $cm^2V^{-1}s^{-1}$, a threshold voltage of 2 V, and an on-to-off ratio of 5×10^7. There is no mention of film composition, total deposition pressure or patterning techniques; shadow masking is assumed since the claim is made that the TFTs are never intentionally exposed to a temperature above that of the ambient room level.

Several variables are explored including channel thickness, insulator choice, and oxygen pressure during deposition. Thicker channels (75 nm) were found to shift the threshold voltage negative in addition to decreasing the subthreshold slope. The use of a silicon nitride as an insulator is found to also lower the threshold voltage and mobility while negatively impacting the subthreshold slope and introducing hysteresis in the transfer curve. When the oxygen partial pressure is increased from 25 mTorr to 40 mTorr, there is a substantial decrease in carrier concentration that is concomitant with a positive shift in the threshold voltage. In a separate work from the same group, the

conductivity of the channel is seen to decrease over 4 orders of magnitude when the oxygen partial pressure is varied from 0 to 40 mTorr. [22] The decrease in carrier concentration is attributed to a decrease in oxygen vacancies with increasing oxygen partial pressure; this leaves more shallow interface traps unoccupied when there is zero applied gate bias which, in turn, raises the turn-on voltage and threshold voltage, assuming a relatively rigid shift in the transfer curve (i.e. no change in the subthreshold characteristic of the transistor).

The effect of a constant gate bias is also explored by this group. [22, 23] After the initial transfer characteristic is measured, the gate electrode is stressed at 30 V for 500 seconds, immediately after which a second transfer curve is measured. This stressing results in a rigid and positive shift in the threshold voltage. Since the subthreshold slope and saturation mobility remain effectively unchanged, it is hypothesized that no new defect states are created by the stressing but that the positive shift is caused by the trapping of the mobile electrons at the semiconductor/insulator interface. This fixed localized negative charge effectively serves to screen the applied positive gate voltage, thus requiring more applied gate bias after stressing to generate the same amount of accumulation and thus current flow in the channel. A linear relationship between the threshold voltage shift and the logarithmic scale of the stressing time is observed, in addition to a recovery of the threshold voltage to its initial value after 6 hours. A negative gate bias is found to have no effect on the threshold voltage; this is consistent with the trap filling hypothesis.

Noh *et al.* explored improving device performance at low voltages by implementing a high dielectric constant oxide/organic polymer double-layer insulator. [24] The channel and source/drain electrodes (ITO) are both sputter deposited (the channel at room temperature). ITO-coated glass is used as the substrate, and the bilayer insulator is deposited onto the substrate to form a staggered bottom-gate structure. The high-k oxide used is an SiO_2-CeO_2 composite (with a 65%-35% ratio and a measured relative dielectric constant k = 9.9) that is deposited by e-beam while the polymer is poly(4-vinylphenol) (PVP) that is deposited by spin coating. The PVP has a final thickness of 55 nm and is used to attempt to mediate large leakage currents that are typically associated with high-k materials deposited at low temperatures. [25]

Without the PVP layer, the gate leakage of a 300 nm oxide layer is $\sim 10^{-5}$ A/cm^2 at 5 V, which is too high for use as a gate insulator. It was also found that using thermally evaporated gold for the source/drain contacts lowers the leakage current by roughly one order of magnitude compared to the sputtered ITO; thus it is inferred that some damage is occurring during the sputter deposition. With the use of the PVP layer, the leakage current is reduced to $<10^{-8}$ A/cm^2 even with the sputtered contacts. The total capacitance of the 355 nm double-insulator stack is low at 20.8 nF/cm^2, due to the low capacitance of the PVP layer. Despite the disappointing capacitance,

the PVP did serve to planarize the surface between the insulator and the semiconductor and was found to be pinhole-free and conformal.

The TFTs exhibit low voltage operation with hard saturation occurring at a 5 V bias on the drain for up to 5 V on the gate. A low field-effect mobility of 0.97 $cm^2V^{-1}s^{-1}$ with a turn-on voltage of 1.7 V is observed in addition to an on-to-off ratio of 2.9×10^4. The channel material was initially sputtered from a single $InGaZO_4$ polycrystalline ceramic target; however there was negligible field-effect modulation, likely due to a high carrier concentration. The sputtered film was found to be indium-rich with a composition of In : Ga : Zn = 75.1 : 7.9 : 17.1, which is substantially different than the target composition. To decrease the indium concentration, the final channel material with reported electrical parameters was co-sputtered using the $InGaZnO_4$ and a ZnO target resulting in a final film composition of In : Ga : Zn = 57.5 : 5.9 : 36.5.

The effect of adsorbed oxygen on IGZO TFTs is explored by Kang *et al.* [26] Bottom-gate inverted TFTs are built on silicon substrates with a 100 nm thick layer of silicon dioxide by sputtering molybdenum for the gate contact, followed by 200 nm of PECVD silicon nitride deposited at 250 °C for the insulator with IGZO (referred to as GIZO by this group) deposited by rf magnetron sputtering to a thickness of 90 nm in an 98/2 argon/oxygen atmosphere at a total deposition pressure of 7 mTorr. Titanium/platinum bilayer source/drain electrodes are formed by liftoff. The completed stack is furnace annealed in a nitrogen atmosphere for an hour at 350 °C.

Two experiments are performed; first a transfer curve of the IGZO transistors are measured in air at room pressure. A vacuum is then applied and the transfer curve is measured at reduced pressures (as low as 8.5×10^{-6} Torr). After reaching the lowest pressure, oxygen is then added to the chamber to raise the pressure back up to atmosphere with measurements being made at varying intervals. The primary electrical parameter monitored is the turn-on voltage. The transistors are found to initially have a V_{ON} of approximately -7 V. As the pressure is decreased, the turn-on voltage also monotonically decreases, reaching a value of -54 V at the lowest pressure. In addition to the more negative turn-on, there is also an order of magnitude increase in the off current. When oxygen is introduced, the off current and turn-on voltage gradually increased back to their initial values under atmospheric conditions.

This shift in V_{ON} is attributed to the formation of a depletion region at the exposed IGZO surface due to adsorbed oxygen and the lack thereof under vacuum. A similar effect is seen in ZnO and is attributed to physisorbed O_2 sitting on the surface in a metastable state. When a conduction band electron is captured, the oxygen is chemisorbed and tightly bound to the surface in a stable state. The process is described as $O_{2_{(surface)}} + e^-_{(conduction\ band)} \rightarrow O^-_{2_{(adsorbed)}}$ and results in establishing the depletion region at the exposed surface. [26, 27] When this exposed-surface

depletion is removed by vacuum or other excitation, resulting in the desorption of oxygen, there is a decrease in the bulk resistance of the material (the cross-sectional area has effectively increased) and an increase in free carrier concentration from the release of the conduction band electrons is observed. Hence a negative shift in V_{ON} is expected.

The variation of the turn-on voltage is modeled using the Freundlich model of the form $ln(V_{on}^{P}) = constant + (1/n)ln(P)$, where n is constant and P is the oxygen pressure. [26] There is a good fit between experimental and modeled results; however the extrapolated V_{ON} at a pressure of 150 Torr, which is equivalent to the oxygen pressure of air at atmospheric pressure, is -10 V instead of -7 V. This difference is attributed to other adsorbed species that are present in air, namely water. In addition, carrier concentration is also measured and is found to vary from 1.25×10^{20} cm^{-3} at the lowest oxygen pressure to 1.6×10^{19} cm^{-3} at the highest. Based on the modeling work and reversible nature of the adsorption phenomenon, it is suggested that an IGZO TFT can be used as oxygen or pressure sensors.

In 2007 Hayashi *et al.* reported on the fabrication of 96 TFTs in a 1 inch by 1 inch square with a pitch of 1 millimeter between transistors to investigate uniformity. The 96 TFT array is fabricated on thermally oxidized silicon by rf magnetron sputtering the IGZO layer and patterning it with photolithography and wet etching. The gate/insulator/channel stack is annealed at 300 °C for 20 minutes in air. A Ti/Au stack is deposited via electron beam and patterned with lift-off to finish the staggered bottom gate device. Two of the 96 transistors failed because an error in the final lift-off process when defining the top contact. The remaining 94 devices exhibited virtually identical transfer curves. Electrical performance includes an average saturation mobility of 14.55 $cm^2V^{-1}s^{-1}$ with a standard deviation (σ) of 0.11 $cm^2V^{-1}s^{-1}$, a threshold voltage of 2.25 V with a σ of 0.13 V, an average subthreshold swing of 0.197 V/decade with a σ of 0.006 V/decade, and an average V_{ON} of -0.37 V with a σ of 0.13 V. The demonstration of uniformity is critical for the consideration of using AOS based TFTs in display applications.

Kumomi *et al.* explored the impact of several variables on TFT performance including the structure, oxygen partial pressure during deposition, and choice of materials for the gate insulator. [28] In every case, the IGZO layer is sputtered at room temperature in an argon/oxygen atmosphere. It is again reported that it is possible to control the electrical conductivity of the sputtered film by varying the oxygen partial pressure; the conductivity decreases monotonically with increasing oxygen partial pressure.

Three different insulators are explored: sputter deposited Y_2O_3 (140 nm, k = 14), thermally grown SiO_2 (100 nm, k = 3.9) and sputter deposited SiO_2 (100 nm, k = ~3.9). The Y_2O_3 film tends to grow conformally where it is deposited, but because of its columnar structure and polycrystalline

nature, its surface becomes rough. The implication of this is that a top gate transistor, where the insulator is deposited onto the semiconductor, yields a smoother semiconductor/insulator interface where the channel will be induced than a bottom gate transistor where the semiconductor is deposited onto the insulator. This roughness exhibits itself as a decrease in saturation mobility between these two structures from 12 $cm^2V^{-1}s^{-1}$ to 3.9 $cm^2V^{-1}s^{-1}$. The turn-on voltage and subthreshold swing are constant between the structures at 1.4 V and 0.2 V/decade, respectively.

The thermally grown SiO_2 is the smoothest surface among available materials. Hence, the bottom gate structure that the Si/SiO_2 stack lends itself to yields improved mobilities with a saturation mobility of 13.4 $cm^2V^{-1}s^{-1}$ but the lower capacitance causes a less ideal threshold voltage of 3.7 V, in addition to a smaller subthreshold slope of 0.47 V/decade. Inverse-staggered transistors using sputtered SiO_2 have similar device performance with a much lower saturation mobility of 4.8 $cm^2V^{-1}s^{-1}$. However it is not clear if a difference in interface roughness is responsible in this trend or if another mechanism is at play.

The effect the composition of the IGZO film has on the electrical properties is also investigated. Three targets (ZnO, In_2O_3, and Ga_2O_3) are co-sputtered with independent power sources to create IGZO films with varying cation ratios. Key findings are that when the composition ratios of zinc exceed >0.65, the phase of the film moves from amorphous to polycrystalline. Gallium-rich films are the most resistive, with a sharp change when increasing the indium content and a moderate change when increasing the zinc content. The less conductive films result in lower μ_{sat} values. Gallium-free films, however, are found to be too unstable with resistivity values changing just after deposition. Thus, the incorporation of gallium in the material appears to be an effective way to stabilize the carrier concentration. It is suggested by Nomura *et al.* that the gallium compensates for for oxygen vacancy formation because the gallium ions form stronger chemical bonds with the oxygen than zinc or indium ions. [17]

Kim *et al.* also fabricated staggered inverted IGZO TFTs at room temperature via rf sputtering. [29] Based on the observation that ZnO-based materials are susceptible to damage during both wet and dry etches, their primary concern is that patterning of other layers (i.e. source/drain contacts) via any form of etching may adversely affect transistor performance. To investigate this, TFTs were fabricated with and without an etch-stop layer (ESL) above the channel.

The TFT stack consists of a glass substrate coated with SiO_2 with 200 nm of lithographically patterned MoW on top of the SiO_2 as the gate contact, 200 nm of PECVD deposited SiN_x as the gate insulator, and 50 nm of rf magnetron sputter deposited IGZO for the channel. The sputtering ambient had a 65/35 Ar/O_2 ratio and the deposited film had atomic ratios of In:Ga:Zn = 2.2:2.2:1.0. After patterning the IGZO via photolithography and wet etching, an ESL layer of SiO_x is deposited

via PECVD and patterned with dry etching using an Ar/CHF_3 chemistry. A final layer of MoW is sputtered, defined via photolithography, and dry etched using an SF_6/O_2 chemistry. The samples are then subjected to a 1 hour anneal at 350 °C.

TFTs with the ESL exhibit large field effect mobilities of 35.8 $cm^2V^{-1}s^{-1}$, a V_T of 5.9 V, an on-to-off ratio of 4.9×10^6, and a subthreshold swing S of 0.59 V/decade. TFTs without the ESL exhibited a degradation in performance with μ_{FE} = 5 $cm^2V^{-1}s^{-1}$ and S = 3.5 V/decade. This result is attributed to traps formed at the backside of the IGZO material created by the plasma during the source/drain etching.

The choice of materials for the ESL is also shown to be critical. Initially SiN_x, which is used as an etch-stop for a-Si:H TFTs, was implemented and found to remove the effect of gate modulation on drain current; i.e. the transistors performed more like resistors. The explanation provided is that hydrogen present during the deposition of the SiN_x film is incorporated into the channel and acts like a dopant, thus increasing the carrier concentration. The IGZO TFTs with the SiN_x ESL are estimated to have a carrier concentration of 3.7×10^{19}; thus SiO_x is used as the ESL instead.

In addition to the ESL, the impact of channel length on μ_{FE} is also explored. Transistors with a 50 μm long channel exhibit a peak μ_{FE} of 35.8 $cm^2V^{-1}s^{-1}$ while TFTs with a length of 10 μm exhibit a peak μ_{FE} of 14.8 $cm^2V^{-1}s^{-1}$. It is proposed that the IGZO TFTs are contact-limited at short channel lengths and that the diminution of the field-effect mobility arises from parasitic source/drain resistances (R_{SD}) that alter the potential distribution across the channel. Thus, field-effect mobilities extracted without considering R_{SD} underestimate the true field-effect mobility. This effect is more pronounced in short channel devices since the resistance of the channel is decreased relative to R_{SD}.

Using the relationship [29]

$$\mu_{FE} \approx \mu_0 \frac{L}{L + \mu_0 W C_i R_{SD}(V_{GS} - V_T)} \tag{2.3}$$

and curve-fitting to experimental data for TFTs of varying lengths, R_{SD} and the true mobility are determined to be 101 kΩ (width-normalized to 101 Ω·cm) and 37.9 $cm^2V^{-1}s^{-1}$, respectively. $R_{SD}W$ is also determined by plotting the width-normalized device-on resistance $R_{on}W$ in the pre-saturation regime (V_{DS} = 5.1 V) versus transistor length L and extrapolating back to the y-intercept (corresponding to L = 0 μm). This yields an $R_{SD}W$ = 113 Ω·cm for a gate bias of 25 V which corresponds well to the curve-fit data. It is also found that R_{SD} is a function of gate voltage with different gate biases corresponding to different $R_{SD}W$ values. However, the amount

of change in $R_{SD}W$ values for a given change in V_{GS} decreases at higher applied biases; an effect that is also reported for organic transistors that exhibit large contact resistances.

The same group later reported in 2008 on the use IGZO TFTs with an SiO_x etch stop layer to drive a 12.1-inch active-matrix organic light-emitting-diode (AMOLED) display. [30, 31] Another material, photo-acryl, was investigated for the ESL but was found to also degrade device performance and stability. With the SiO_x ESL, the TFTs exhibit $\mu_{FE} = 8.2$ cm^{2}V^{-1}s^{-1}, $V_{T,sat} =$ 1.1 V, an on-to-off current ratio $>1\times10^7$, and a subthreshold swing S = 0.58 V/decade. Of specific interest to display applications is the amount of variation between neighboring devices; this is referred to as short-range uniformity (SRU) with the distance between adjacent transistors in the AMOLED being $\sim$150 μm. The average and standard deviation of μ_{FE} of nine nearby transistors are found to be 7.81 cm^{2}V^{-1}s^{-1} and 0.055 cm^{2}V^{-1}s^{-1}, respectively, while the standard deviation of V_T is less than 0.01 V.

In 2008, Lim *et al.* reported on IGZO TTFTs fabricated by rf sputtering at room temperature onto a glass substrate. [32] Rf magnetron sputtered amorphous indium zinc oxide (IZO) is used for all the contacts while 100 nm of sputter deposited HfO_2 is used for the gate dielectric. The channel layer is sputtered to a thickness of 50 nm in a pure Ar environment with a pressure of 10 mTorr. Variation of the rf power from 75 to 200 W is used to control the carrier concentration and electrical properties of the resulting TFTs as opposed to varying oxygen/argon ratios during the deposition. At a deposition power of 140 W, the IGZO has a carrier concentration of 6.5×10^{17} cm^{-3}. The motivation for this is that sputtering in pure argon is claimed to improve long-term stability.

The channel layer exhibits optical transparency >80%, including the reflection and absorption due to the glass substrate. TTFTs exhibit an on-to-off ratio of 10^5, a subthreshold swing of 0.25 V/decade, a threshold voltage of 0.44 V, and a saturation mobility of 7.18 cm^{2}V^{-1}s^{-1}. The effects of aging and biasing on the saturation mobility and threshold voltage are also explored. Devices are measured at t = 0, then maintained at the room ambient for 500 hours without electrical excitation, followed by 500 hours of continuous measurement. There is virtually no change between the values measured at t = 0 and t = 500 hours; thus there appear to be minimal aging effects. In the subsequent 500 hours of measuring, the mobility remained almost constant showing slight random variation within experimental error while the threshold voltage slowly increased. At the end of the 500 hour measurement period, the threshold voltage had only changed by 460 mV.

Lim *et al.* also published similar results for a different insulator material using the same channel and source/drain deposition parameters and experimental procedures later in 2008. [33] Using a PECVD deposited silicon nitride (SiN_X) at 70 °C for the gate insulator instead of the

sputter deposited HfO_2, the TTFTs exhibit an on-to-off ratio of $\sim 10^5$, a subthreshold swing of $\sim$0.5 V/decade, a threshold voltage of $\sim$2.1 V, and a saturation mobility of $\sim$17 $cm^2V^{-1}s^{-1}$. The impact of sputtering power on film resistivity shows a step-function like decrease from $\sim 10^3$ Ω-cm at powers less than 125 W to $\sim$1 Ω-cm for powers greater than 150 W. The higher sputtering powers are thought to yield films with increased density due to higher kinetic energy neutrals arriving at the film surface; this improved film quality is likely to correlate with the decrease in resistivity. Stability of these devices after 500 hours of stressing the drain at a bias of 6 V is reported, with no noticeable trends or changes in both the saturation mobility and the threshold voltage over the duration of the experiment.

Jeong *et al.* examined the effect of channel deposition pressure when fabricating an IGZO TFT via rf magnetron sputtering. [34] TFTs are bottom-gate structures, fabricated on top of an Si/SiO_2 substrate. Molybdenum-Tungsten (MoW) is sputtered to form the gate electrode; 200 nm of SiN_X is deposited by PECVD at a temperature of 330 °C to form the insulator. The IGZO channel is sputtered from a single $In_2Ga_2ZnO_7$ polycrystalline ceramic target at a power density of 1.4 W/cm^2 in an Ar/O_2 ambient with a ratio of 65/35 and varying pressures. Indium zinc oxide is used to form the source/drain contacts; the channel and source/drain are patterned via shadow masking techniques. Completed TFTs are subjected to a 350 °C anneal in an N_2 atmosphere.

A reference transistor with the channel sputtered at 5 mTorr had $\mu_{FE} = \sim 11.4$ $cm^2V^{-1}s^{-1}$, $V_T = \sim 2.9$ V, $I_{on/off} = 1\times 10^7$, and a subthreshold swing S of 0.87 V/decade. A significant improvement is seen when channel deposition pressure is decreased first to 3 mTorr and ultimately to 1 mTorr, with the best device exhibiting $\mu_{FE} = \sim 21.8$ $cm^2V^{-1}s^{-1}$, $V_T = \sim 0.83$ V, $I_{on/off} = 6.8\times 10^7$, and S = 0.17 V/decade.

Density, roughness, and cation composition of the films were analyzed for each pressure; there is no apparent variation in the composition of the films. The density of the IGZO films is found to increase monotonically with decreasing chamber pressure; the reference sample has a density of 5.50 g/cm^3 while the best-case device has a density of 6.27 g/cm^3. It is hypothesized that the lower pressure in the chamber leads to less scattering of the sputtered species, thus leading to an increased amount of energy in the deposited molecules which should increase the adatom mobility on the surface. Hence the improvement in device performance is tentatively attributed to the densification of the IGZO film.

The improvement in S is investigated in more detail. The subthreshold swing is typically an indicator of trap density (N_t), which includes the bulk trap density (N_{bulk}) and the interface trap density (D_{it}). To determine which of these quantities the lower deposition pressure is affecting, a bilayer stack is used where an IGZO film with a thickness X nm is first deposited at 1 mTorr onto

the insulator to form the same interface as seen in the best case device with a second IGZO film of thickness 50-X nm being deposited onto the first at a pressure of 5 mTorr. If an improvement at the interface is the primary cause for the smaller S values, then the bilayer TFTs should theoretically also exhibit the same improvement. S values for the bilayer device range from 0.53-0.59 V/decade, which is substantially different than S = 0.17 V/decade observed with the best-case TFT whose channel is deposited entirely at 1 mTorr. This is indicative that an improvement in N_{bulk} is responsible for the lower S values, and this is again attributed to a densification of the IGZO films when sputtered at lower pressures.

Chiang *et al.* reported on the processing effects on TFT performance and stability in 2008. [35] Transistors are bottom-gate inverted structures fabricated on thermally grown silicon/silicon dioxide substrates with the IGZO being deposited by rf magnetron sputtering from a 3-inch target. Oxygen partial pressure, sputtering power, anneal temperature, and deposition time (channel thickness) are all varied. A baseline device is fabricated at an rf power of 75 W in pure argon at a processing pressure of 5 mTorr with a 175 °C post deposition anneal. The reference device shows exemplary transistor performance with hard saturation, indicating that the channel is fully depleted, and saturation currents on the order of 1 mA. The primary electrical characteristics of this reference device are $\mu_{inc} = \sim 17$ cm^{2}V^{-1}s^{-1}, $V_{ON} = \sim 0$ V, S = 0.6 V/decade, and an on-to-off ratio $>10^7$.

Sample transistors are annealed between 200 °C and 800 °C in 100 °C steps; transistors that are not annealed do not exhibit an appreciable field-effect and are omitted. The percent of oxygen in the atmosphere is varied between 0, 5 and 10 % while the rf power is varied between 75, 100, and 125 W. Incremental mobility increases with increasing anneal temperature up through 500 °C, at which point there is a plateau. Above 600 °C, there is a slight decrease in mobility. The increase in mobility is ascribed to an improvement in either the semiconductor/insulator interface or in the local atomic arrangement and improved bonding with increasing annealing temperature. The decrease is associated with crystallization (i.e., grain boundary-limited transport) or phase segregation in the IGZO layer.

For temperatures <500 °C, decreasing the oxygen partial pressure leads to an increase in μ_{inc} and there is a negative shift in V_{ON} when there is no oxygen present (there is little difference in V_{ON} between 5 and 10 % oxygen). Above 500 °C the anneal dominates and mobility and V_{ON} trends converge, regardless of oxygen partial pressure.

Increasing rf power tends to decrease V_{ON} and increase mobilities for annealing temperatures below 400 °C. These trends are attributed to a larger carrier concentration at higher sputtering powers. With increasing power there are likely higher energy neutrals reaching the substrate

which subsequently raise the adatom mobility, allowing for increased local bonding order in the semiconductor and, thus, fewer bulk states are created and the free carrier concentration increases. This larger carrier concentration is concomitant with a zero-gate bias Fermi level shift towards the conduction band which results in a larger fraction of the remaining interface or bulk traps being filled at zero bias. Hence, the mobility is increased while the turn-on voltage becomes more negative.

Two types of stability are also explored; shelf life and bias stress. For the shelf life experiment, transistors with different channel thicknesses (10, 25, and 50 nm) are fabricated and subjected to a 175 °C post deposition anneal in N_2 and the transfer curve is measured at week 0. The TFTs are left unconnected in the dark for a period of 18 weeks with the transfer characteristic being measured periodically to monitor the turn-on voltage. Thicker devices exhibit less variation over the duration of the experiment and never exhibit more than a 0.5 V shift in the turn-on. The 25 nm device exhibited a constant shift of ∼1.5 V after 7 weeks, while the 10 nm transistor exhibited an increasing shift for the first 12 weeks, with a peak shift of >5.5 V.

Bias stability is tested by holding the gate and drain terminals at a bias of 30 V for 1,000 minutes and constantly monitoring the drain current. These TFTs are sputtered at 125 W with varying oxygen partial pressures (from 0.2 mTorr to 0.0 mTorr in increments of 0.05 mTorr) to control V_{ON} in a total Ar/O_2 pressure of 5 mTorr. These TFTs are subjected to a 300 °C post-deposition anneal in air. Turn-on voltages are found to be 8, 5, 4, 3, and 0 V. It is observed that bias stress stability greatly improves as the turn-on decreases towards 0 V. This is not a surprising trend since devices with large positive V_{ON}s are dominated by traps either at the interface or in the bulk. The TFT with the second best performance sees a degradation in current by more than 60% compared to its initial value. The device with a $V_{ON} = 0$ is extremely stable and shows negligible current degradation over the duration of the experiment.

2.3.2 Zinc Tin Oxide

In 2005 Chiang *et al.* reported the first TTFT based on an amorphous zinc tin oxide (ZTO) channel material. The channel was deposited from a ceramic target using radio-frequency (rf) magnetron sputtering in an argon and oxygen ambient atmosphere onto a glass substrate that was provided with a 200 nm sputtered indium tin oxide (ITO) layer beneath a 220 nm atomic layer deposited ATO insulator. The substrate was heated to 175 °C during the deposition and the entire stack was annealed after the channel layer deposition to 300 °C or 600 °C. To complete the devices, indium tin oxide (ITO) source and drain contacts were also sputtered. Patterning of channels and

the source/drain contacts was accomplished with shadow masks. Two molar ratios of ZnO:SnO_2 were explored, 2:1 and 1:1.

The average transmittance in the visible portion of the electromagnetic spectrum is 84% for the entire structure, including the substrate, which accounts for absorption and reflection losses. Electrical performance was excellent with qualitatively ideal I_D vs V_{DS} curves for various gate voltages (i.e. hard sauration is observed in all cases); current drive is in the miliamp range and large spacings are present between the different gate voltages, indicating a large transconductance. Field-effect mobility ranges between 20-50 $cm^2V^{-1}s^{-1}$ along with a turn-on voltage that varies between -5 V and 5 V for roughly 50 discrete devices. The drain current on-to-off current ratio is greater than 10^7, with the off-current being determined by the gate leakage current.

Little variation in electrical performance was seen between the different stoichiometries. The 300 °C anneal resulted in a moderate loss in channel mobilities ($\sim$15 $cm^2V^{-1}s^{-1}$ versus $\sim$25 $cm^2V^{-1}s^{-1}$ for the 600 °C anneal for two transistors). The improvement in performance with increasing anneal temperatures is attributed to improved local order, as opposed to long-range crystallinity since the x-ray diffraction (XRD) patterns are nearly identical between the two films. No hysteresis is reported. [16]

In 2005, Hong *et al.* successfully fabricated ZTO TFTs using reactive magnetron sputtering with a zinc/tin metal target. [36] The channel material is deposited onto a silicon/silicon dioxide substrate and subjected to two post-deposition anneal temperatures (300 °C and 500 °C); there is no intentional heating during deposition. The devices are completed with aluminum top contacts and all patterning is accomplished with shadow masks. Sputtering is done in an argon/oxygen environment with a total pressure of 30 mTorr while oxygen partial pressures are varied from 0.5 to 1.2 mTorr. Transistors fabricated via rf sputtering exhibit incremental and average mobilities of 11 $cm^2V^{-1}s^{-1}$ and 6 $cm^2V^{-1}s^{-1}$, respectively, for the 300 °C anneal and 32 $cm^2V^{-1}s^{-1}$ and 25 $cm^2V^{-1}s^{-1}$, respectively, for the transistors annealed to 500 °C. The turn-on voltage for the lower temperature anneal is 2 V while there is a -4 volt shift in the turn-on for the higher anneal temperature ($V_{ON,500^\circ C}$ = -2 V). Drain current on-to-off ratios of $\sim 10^7$ are observed regardless of the anneal temperature.

An optimal value of oxygen partial pressure is found at 0.8 mTorr; this corresponds to a peak incremental mobility value for both annealing conditions. Sputtering with a direct current (DC) power source is also reported and shows similar electrical performance; the optimum oxygen partial pressure is found to be slightly higher for the DC sputter at 0.9 mTorr. Sputtering at an overall pressure of 5 mTorr was explored and yielded higher mobilities, but turn-on voltages were always less than -20 V for both annealing conditions. This is attributed to a more metallic film

(i.e. not fully oxidized) being deposited at lower pressure, resulting in a higher conductivity and more resistor-like behavior.

Hong and Wager also explored the passivation of ZTO TFTs in 2005. [37] Staggered inverted TFTs are passivated by thermally evaporating silicon dioxide over the exposed channel material. The channel is deposited by rf magnetron sputtering from a ceramic target to a thickness of 80 nm onto a silicon substrate with a layer of thermally grown silicon dioxide. Sputtered ITO is used as the source and drain contacts with all patterning being accomplished with shadow masking. The unpassivated transistor is then annealed to 600 °C.

Unpassivated control transistors perform well with a peak μ_{inc} of 20 $cm^2V^{-1}s^{-1}$ and exhibit hard saturation. Transistors that have their channel region passivated, however, initially show markedly different results. These TFTs exhibit substantial current flow with no bias on the gate (i.e. they are depletion-mode devices) and they do not exhibit hard saturation. Performance as a transistor is so poor that these devices are better classified as nonlinear gate-controlled resistors. If a second anneal is performed on the passivated devices, the original performance of the unpassivated transistors is restored.

This drastic change in performance is attributed to the previously discussed adsorbed oxygen-induced depletion layer at the exposed surface of the bottom-gate TFT structure. [26, 27] When the surface is initially passivated, the depletion layer is eliminated. It is suggested that, depending on the passivation material used (several others besides silicon dioxide are briefly explored), an accumulation layer may even be formed at the surface. Either of these scenarios will cause in an increase in the conductivity of the channel between the source and drain terminals, resulting in a negative shift in the turn-on voltage, less gate-modulation of the current, and the inability to fully deplete the channel of carriers, resulting in a lack of hard saturation. The exact mechanism that restores proper transistor operation after the second anneal is not described, but it is likely due to a re-establishing of the depletion layer either through a thermally activated chemical reaction or inter-diffusion of the passivation layer and channel material which again allows for the conduction band electron capture.

Transistors are also passivated successfully utilizing calcium fluoride, germanium oxide, strontium fluoride, and antimony oxide with results similar to using silicon dioxide . A nickel oxide film results in a reduced peak incremental mobility while zinc sulfide and cesium oxide passivation layers eliminate channel conduction completely. For successful passivation layers, it is possible to utilize a single anneal step after the passivation layer is deposited, but this results in a lower channel mobility than the two-anneal process.

Jackson *et al.* reported ZTO TFTs on flexible substrates in 2005 and 2006. [38, 39] The substrate is stainless steel-backed polyimide, onto which an aluminum gate electrode is sputtered. Silicon oxynitride is used as the dielectric layer and is deposited via plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. Up through this point, processing is accomplished using roll-to-roll fabrication; the rolls are then cut into 10 mm x 50 mm strips for further processing. The channel layer is sputter-deposited to a target thickness of 50 nm with no substrate heating; the stack is later annealed to 250 °C. A source/drain contact layer is then deposited using either aluminum or ITO, followed by a final contact pad deposition of of gold or aluminum. The channel and source/drain layers are patterned with shadow masks.

When using Al as the source/drain contact layer, the transistors exhibit current crowding in the I_{DS} versus V_{DS} curves, i.e. the current trends for different gate voltages converge at a positive V_{DS} value, instead of zero. This is attributed to a contact resistance problem and the positive voltage where the currents converge correlates to an amount of voltage dropped across the contacts that is required in order to turn them on. When using ITO as the source/drain contact, this problem is not observed.

Electrical performance approaches that of TFTs fabricated on rigid substrates. The drain current on-to-off ratio approaches 10^6 and the incremental mobility μ_{INC} is 13 $cm^2V^{-1}s^{-1}$. The subthreshold slope is poor at 1.6 V/decade, but the dielectric used is also relatively thick at 375 nm. The only problematic electrical parameter is a very negative threshold voltage of -8.8 V; it is suggested that varying the makeup of the insulator will allow this parameter to be optimized. Qualitatively, these transistors also do not exhibit hard saturation.

Hoffman further explored the effects of channel stoichiometry and post-deposition anneal temperature on the electrical characteristics of ZTO TFTs. [40] Staggered bottom-gate TFTs are fabricated via rf sputter deposition of the channel material onto a thermally oxidized silicon substrate and ITO is employed for the source/drain contacts. All patterning is accomplished with shadow masks. Five different ceramic targets are used to deposit the channel with varying $\frac{Zn}{Zn+Sn}$ ratios of 0.0, 0.33, 0.5, 0.67, and 1.0 in a constant Ar/O_2 atmosphere. There is good correlation between the sputtered films and the target composition, as determined with wavelength dispersive spectrometry, with the fractional composition targets resulting in films that have ratios of 0.29, 0.46, and 0.68. Transfer curves in the linear regime are provided for transistors of each composition, annealed to 600 °C, while V_{ON} and μ_{INC} are monitored as the key electrical parameters of interest.

The transistor not containing any zinc (corresponding to the ratio 0.0) was unable to be depleted at any applied gate voltage, thus it never turned off. Transistors with higher zinc concentrations exhibit less hysteresis and increasingly less-negative V_{ON} values with the 0.67 ratio having

a V_{ON} = ~0 V. When the zinc ratio is 0.5, the best mobilities are observed with $\mu_{INC,PEAK}$ = ~30 $cm^2V^{-1}s^{-1}$ while the extreme compositions (0.0 and 1.0) exhibited the worst mobilities, with $\mu_{INC,PEAK}$ = ~10 $cm^2V^{-1}s^{-1}$ and ~5 $cm^2V^{-1}s^{-1}$, respectively.

The effect of increasing anneal temperature is found to increase mobilities, up to 600 °C, above which a decrease is seen for all the ratios with the exception of the pure zinc oxide film. Hence the decrease is likely associated with crystallization or phase segregation of the amorphous multi-component films, which clearly does not affect the polycrystalline ZnO film. V_{ON} decreases (or becomes more negative for values less than 0 V) up through 400-500 °C. This is attributed to improving the material quality and thus decreasing the trap density; with fewer traps there are more free carriers at any given gate voltage, thus it is easier for the accumulation layer to form. High mobilities and a V_{ON} = ~0 V are demonstrated to be possible concurrently.

In 2006, Görn *et al.* reported the application of a ZTO TFT in conjunction with an organic light-emitting diode (OLED) to create a transparent smart pixel. [41] The OLED is built vertically upon the TFT and uses the drain electrode of the transistor as the cathode for the diode. The ZTO channel layer is deposited via oxygen-plasma-assisted pulsed-laser-deposition (PA PLD). This technique relies upon the availability of radical oxygen species to prevent oxygen deficiencies in the film and hence unintentional doping. No post-deposition anneal is employed, keeping the maximum processing temperature to 150 °C. The TFT has an average transmittance of greater than 80% in the optical portion of the spectrum. Threshold voltages are reported to vary between -1 V and 1 V and no hysteresis was observed in the transfer curves. A saturated field-effect mobility of 11 $cm^2V^{-1}s^{-1}$ and a drain current on-to-off ratio of 10^5 is also observed.

In 2007, Görn *et al.* also reported on the stability of ZTO-based TFTs processed with different compositions and processing temperatures under gate bias stress tests. [42] The deposition method of the channel was again AP-PLD and the substrate temperature was varied between 250 and 450 °C during the channel deposition. Aluminum-doped zinc oxide (AZO) was used for the source and drain contacts while the same glass/ITO/ATO substrate employed by Chiang and Suresh is used as the metal and insulator of the gate capacitor stack. Patterning was accomplished with standard photolithographic techniques. To ensure that the bias stressing was the dominate mechanism at play for those experiments, the measurements were taken in a dark box. The stressing is accomplished by holding the gate terminal at 10 V for 60,000 seconds and measuring the transfer curve before and after. The two parameters used to monitor the effect of the bias stress are the change in threshold voltage, ΔV_T, and the change in the saturation mobility, $\Delta\mu_{SAT}$.

The most surprising finding of this work is that not only the magnitude but also the sign of ΔV_T changes with varying concentrations of zinc in the film. ΔV_T varies between -1.4 V and 1.5 V

for all samples; transistors with less than 36% or more than 65% zinc exhibit positive, rigid shifts in the transfer curve while transistors with near equal ratios of zinc and tin are found to exhibit negative shifts with a concomitant decrease in subthreshold slope; i.e. the shape of the transfer curve also changes. The positive threshold shift is attributed to defects in the dielectric that act as traps while the negative shift is assumed to be due to either the semiconductor/insulator interface or deep states created in the bulk of the material; no solid findings are presented to support these hypotheses which are based on mechanisms observed in a-Si. There is no apparent correlation between the change in threshold voltage and the change in saturation mobility; $\Delta\mu_{SAT}$ typically changes less than 10%. The most stable transistors have an atomic ratio of 36:64 Zn:Sn. After the removal of the applied stress there is a gradual recovery of all parameters to their original values.

In addition, this group also reported on the influence of visible light on ZTO TFTs. [43] The channel layer is deposited with PA-PLD with varying amounts of substrate heating and zinc concentrations. The target thickness for the channel is 60-80 nm. For the experimental procedure, light-emitting diodes (LEDs) of various wavelengths in the visible spectrum (628, 525, 470, and 425 nm) with spectral widths no broader than 30 nm are used to illuminate the transistors in a dark box. When exposed to the light source, three effects were observed: a decrease in V_T and μ_{SAT} and a simultaneous increase in the off current. After several hours of illumination, a steady state is reached. When the light source is removed, the TFTs immediately begin to recover to their initial values with a full recovery observed in 20 hours. Shorter wavelengths and higher intensities had the largest impact on device performance. The dominant processing parameter for improved stability is the processing temperature; transistors processed at 450 °C showed less than a 3 V shift in V_T while devices processed at 250 °C exhibited more than a 15 V shift. The zinc content of the film is reported to be a second order effect, but zinc concentrations of less than 35% are not explored.

In 2008, McDowell *et al.* also explored the effect of channel composition on the electrical performance of ZTO TFTs. [44] Instead of using different targets with different compositions, co-sputtering of a ZnO and an SnO_2 is employed, along with a rotating substrate holder, to grade the ZTO film between 85% Sn/ 15% Zn on one side of the substrate to 5% Sn/ 95% Zn on the other, varying approximately linearly as a function of position. Aluminium is vacuum deposited to form the source/drain contacts and shadow masking is used to define the channel and source/drain regions.

The primary electrical parameters that are monitored are saturation mobility and threshold voltage, compared to incremental mobility and the turn-on voltage in previous work. Two peaks in mobility are observed at zinc fractions of 0.25 and 0.8 (corresponding to mobilities of

$\sim$12 $cm^2V^{-1}s^{-1}$) with a trough between them centered at a zinc ratio of 0.5 (and mobilities $\sim$4 $cm^2V^{-1}s^{-1}$). This data suggests that films with a 1:1 or 2:1 ratio of Zn:Sn are non-optimal; this is contrary to what is reported previously by Hoffman. These differences are ascribed to run-to-run variation, since Hoffman's work required the different stoichiometries to be deposited during different depositions from different targets and, more importantly, to the different mobility metrics that are reported. The substantially lower mobility values are also partly attributed to the use of aluminum contacts in this work opposed to ITO. Besides this discrepancy in reported optimal ratios for peak mobilities, the two studies otherwise generally agree in regard to threshold/turn-on voltage and subthreshold trends. It is also seen in this work that ZTO films with zinc ratios $\leq$ 0.33 exhibit a photosensitivity which changes the drain current on-to-off current ratio as much as 10^5 for samples measured in both light and dark environments.

2.3.3 Other Materials

There are two reports in the literature of indium gallium oxide (IGO) as the active layer in a TFT, both from the same group. Chiang *et al.* report on the fabrication of staggered bottom-gate TFTs on Si/SiO_2 substrates using rf magnetron sputtering with a 5 mTorr processing pressure for the channel deposition. [45] Sputtered ITO is employed for the source and drain contacts; all patterning is accomplished with shadow masking. Channel composition, oxygen partial pressure during channel deposition, and anneal temperature are all explored.

Increasing indium concentration, anneal temperature, or decreasing oxygen partial pressure all tend to increase the mobility (up to the crystallization temperature of $\sim$600 °C) and decrease the turn-on voltage, as seen previously with other materials. Two types of mobility are reported, incremental and average. A peak μ_{INC} of 27 $cm^2V^{-1}s^{-1}$ with a corresponding V_{ON} of -14 V is reported for a 600 °C anneal, along with results more optimized for practical applications (i.e., enhancement-mode devices with a positive turn-on) with $\mu_{INC} = \sim$19 $cm^2V^{-1}s^{-1}$ and $V_{ON} = 2$ V. Average mobilities are slightly lower in magnitude than incremental mobilities but are found to provide good agreement to experimental results when used to model the current flow through the device. Drain current on-to-off ratios are typically $\sim 10^6$.

Presley *et al.* report on the integration of staggered bottom-gate IGO-based TFTs for use in inverters and ring oscillators, the performance of which is discussed in Sec. 2.4.2. [46] Commercially available Corning 1737 glass slides with 200 nm of sputter deposited ITO are used as the substrate and gate electrodes. One hundred nanometers of PECVD SiO_2 is used for the insulator, onto which the IGO is rf magnetron sputtered in a 90/10 Ar/O_2 environment at 5 mTorr. Sputter-deposited ITO source/drain top contacts complete the devices. The top contacts are defined with

photolithography and lift-off while the other layers are also patterned photolithographically and etched. A turn-on of ∼2 V and a drain current on-to-off ratio of $\sim 10^4$ are reported. A lower peak incremental mobility of ∼7 $cm^2V^{-1}s^{-1}$ is seen compared to Chiang's ∼19 $cm^2V^{-1}s^{-1}$ for similar conditions. The difference is attributed primarily to the use of a different insulator and, to a lesser extent, the non-idealities associated with photolithography. The lower on-to-off ratio is due to a much higher off current when using the PECVD SiO_2; 10^{-7} A compared to $\sim 10^{-10}$ A when using thermal SiO_2.

In 2005 DeHuff *et al.* demonstrated the viability of zinc indium oxide (ZIO), a material often used as a transparent conductor, as the channel layer in a TFT. [47] Transistors fabricated with two different processing conditions are reported; a 600 °C post-deposition anneal with a 91/9 Ar/O_2 flow ratio (33 sccm total flow) and a 300 °C post-deposition anneal with a 96/4 Ar/O_2 flow ratio (47 sccm total flow). Staggered bottom-gate TFTs are fabricated on glass/ITO/ATO substrates. The channel is deposited to a thickness of ∼85 nm by rf magnetron sputtering from a ceramic target with a 2:1 molar ratio of $ZnO:In_2O_3$; sputtered ITO source/drain contacts finish the transistors. X-ray diffraction data confirm that the 600 °C samples are polycrystalline while those annealed to 500 °C and below remain amorphous.

The TFTs subjected to a 600 °C anneal exhibit qualitatively ideal transistor characteristics such as a large transconductance and hard saturation, but are depletion-mode devices with V_{ON} = -12 V. Peak incremental mobilities range from 45-55 $cm^2V^{-1}s^{-1}$ with maximum average mobilities of 25-35 $cm^2V^{-1}s^{-1}$. The subthreshold swing is 800 mV/decade.

The TFTs subjected to a 300 °C anneal are enhancement mode with $V_{ON} = 6$ V and exhibit hard saturation but with a crowding in the output curves (decreasing spacing between saturated currents in the I_D vs V_{DS} plot) between large V_{GS} values. Performance is also reduced with peak incremental mobilities ranging from 10-30 $cm^2V^{-1}s^{-1}$ with maximum average mobilities of 5-20 $cm^2V^{-1}s^{-1}$, however the subthreshold swing is improved 300 mV/decade. The change in performance is attributed to the change in state from polycrystalline to amorphous; this changes the deep trap characteristics while the different temperatures also likely modify the semiconductor/insulator interface to different extents. Transistors successfully fabricated at room temperature (i.e., no intentional post-deposition anneal) are also reported but with decreased performance in general; peak incremental mobilities are ∼8 $cm^2V^{-1}s^{-1}$.

Yaglioglu *et al.* reported on the room temperature fabrication of a staggered bottom-gate TFT using IZO as both the active channel and the source/drain contacts in 2006. [48] Thermally oxidized silicon substrates are used for the gate contact and insulator while the channel and contacts are patterned via photolithographic liftoff techniques. The IZO is rf magnetron sputtered in

different argon/oxygen ratios to control the carrier concentration (a 90/10 Ar/O_2 ratio is used for the channel and a pure argon atmosphere is used for the contacts). The channel layer is notably thin at 10 nm.

The transistors are depletion mode with V_T = -3.2±0.9 V, exhibit a saturation mobility of 20.4±1.9 $cm^2V^{-1}s^{-1}$ with a subthreshold swing of 1.2 V/decade. Off-currents are on the order of 10^{-11} A with drain current on-to-off ratios of $\sim 10^8$. Carrier concentration of the contacts and channel are 3.3×10^{20} cm^{-3} and 2.1×10^{17} cm^{-3} respectively.

In 2007 Wang *et al.* also reported on room temperature fabrication of IZO TFTs using a top gate co-planar structure with 95 nm or 50 nm of PECVD SiO_2 for the insulator. [49] Devices are depletion mode with a threshold voltage of -6.5 V and a field-effect mobility of $\sim$4.5 $cm^2V^{-1}s^{-1}$. Subthreshold slopes of 1.9 V/decade and 0.87 V/decade are reported for the thinner and thicker insulator, respectively, despite this being counter-intuitive. A drain current on-to-off ratio of $\sim 10^5$ and an off current of $\sim 10^{-10}$ A are observed for both insulator thicknesses, despite the PECVD insulator deposition being performed without any intentional heating.

Song *et al.* also report on the fabrication of a room temperature TFT in 2007 that utilizes rf magnetron sputtered IZO for both the contacts and channel. [50] The effect of oxygen partial pressure on carrier concentration is investigated more thoroughly. The Ar/O_2 ratio is varied from 100:1 to 1000:1 while the carrier concentration changes from $\sim 10^{14}$ to $\sim 10^{20}$, respectively. The contacts are deposited in pure argon to a thickness of 100 nm and have a carrier concentration of 3×10^{20} cm^{-3} while the channel is deposited to a thickness of 60 nm in a 125:1 ratio, resulting in a carrier concentration of 2×10^{15} cm^{-3}. Room-temperature sputtered AlO_X onto the gate electrode serves as the insulator to create a staggered bottom-gate device.

Transistors have $\sim$80% transmittance in the optical portion of the electromagnetic spectrum. The subthreshold slope is poor at 2.2 V/decade, which could be indicative of poor dielectric quality, but the drain current on-to-off ratio is good at $\sim 10^6$ with gate leakage currents less than 10^{-10} A. The threshold voltage is 1.1 V, while V_{ON} is roughly -5 V. A small Hall mobility of 4.2 $cm^2V^{-1}s^{-1}$ for bulk IZO films is reported along with a field-effect mobility of only 0.53 $cm^2V^{-1}s^{-1}$. A peak saturation current of only 1.41 μA is seen at a bias of V_{GS} = 5 V and V_{DS} = 10 V, but the I_D versus V_{DS} curves exhibit hard saturation.

Barquinha *et al.* explored the impact of channel layer thickness on the electrical properties of IZO-based TFTs. [51] Staggered bottom gate TFTs are fabricated on glass/ATO/ITO substrates using rf magnetron sputtered IZO for both the source/drain and channel layers. The active layer thickness is varied from 15 to 60 nm. All the fabricated TFTs are claimed to be enhancement

mode because V_T is positive, but there is some ambiguity to this claim since some of the thicker transistors exhibit a negative V_{ON}.

All the main electrical parameters used to characterize a TFT are shown to improve by using a thinner active layer. These parameters include the drain current on-to-off ratio, μ_{FE}, and subthreshold swing. The threshold voltage is shifted increasingly positive with decreasing channel layer thickness; while not necessarily an improvement this provides a means for engineering this parameter.

The changes in device performance are ascribed to three main physical phenomena that occur with increasing channel thickness; a decrease in the bulk resistance of the film, an increase in the absolute number of free carriers available in the channel, and a decrease in the influence of the back interface (opposite the induced channel). The decrease in bulk resistivity leads to a higher off current, which thus decreases the on-to-off ratio. Increasing the number of carriers in the channel makes it easier to create the accumulation layer while also increasing the number of occupied interface states at zero bias that would otherwise capture the accumulated electrons forming the channel; thus V_{ON} becomes increasingly negative with increasing semiconductor thickness. Mobility is found to decrease with increasing thickness, which may seem counter-intuitive, but this is likely a function of the transistor structure. All the injected and extracted carriers need to be transported vertically through the bulk of the channel, so as the thickness of the channel increases the resistance of this path also increases. It is also suggested that increasing thickness results in a higher number of positively charged ions in the bulk of the channel. This increases the amount of scattering a carrier sees and thus negatively impacts the mobility.

The influence of the back interface is observed through the change in subthreshold swing; increasing channel thicknesses results in increased subthreshold slopes. It is hypothesized that, in thinner channels, the probability of charges initially induced in the semiconductor being trapped at either the front or back surface of the channel is very high because of a smaller number of absolute initial carriers and the shallow nature of the traps. Hence, it takes more induced charge to satisfy all the surface state defects before a noticeable increase in current can occur. Once the surface traps are satisfied, though, the next available induced charge will cause an abrupt increase in current. In this scenario, interface traps play the largest role in influencing the subthreshold characteristics. In thicker channels, these surface imperfections are satisfied at lower applied biases, because of the increased number of free carriers at zero bias, and it is also hypothesized that the influence from the back side is decreased both because of the increased distance and also an increased amount of defects in the bulk. These defects are likely distributed over deeper energies than the surface states, thus the change in current is less abrupt, resulting in an increase in the subthreshold slope.

Grover *et al.* fabricated staggered bottom-gate TFTs using zinc indium tin oxide (ZITO) as the channel layer on silicon/silicon dioxide substrates. The channel is rf magnetron sputtered while thermally evaporated aluminum is used to form the source/drain contacts. All patterning is accomplished via shadow masking. The ZITO layer is transparent in the visible spectrum with an ∼85% transmission through a ZITO film on a glass substrate, including losses for absorption and reflection. The film remains amorphous through post-deposition anneal temperatures up to 600 °C.

Transistors exposed to a 200 °C anneal are depletion mode with V_{ON} = ∼-11 V. Clockwise hysteresis is observed and attributed to the continuous filling of traps by accumulated channel electrons. The drain current on-to-off ratio is $\sim 10^7$ with incremental mobility and average mobility of approximately 15 $cm^2V^{-1}s^{-1}$ and 6 $cm^2V^{-1}s^{-1}$, respectively. A study of low temperature anneals from 100 °C to 300 °C show that mobility increases and V_{ON} becomes more negative with increasing temperature; a V_{ON} greater than zero is not reported, even at the lowest temperature anneal. These changes in electrical parameters with temperature are again attributed to an increase in short-range order.

2.4 Circuit Applications for Amorphous Oxide Semiconductors

While the majority of work regarding amorphous oxide semiconductors has focused on the development of discrete TFTs, there have been several efforts in the last two years to create integrated circuits. Inverters are the simplest circuit to implement and can be cascaded together to create a ring oscillator. In this section a brief tutorial of inverter operation is provided as it is directly relevant to the work contained herein in addition to reports of AOS-based integrated circuits (ICs). These ICs include: inverters, ring oscillators (ROs), and pixel drivers for display applications. The performance of an alternating-current to direct-current (AC/DC) rectifier implemented with p-type organic TFTs (OTFTs) is also discussed for comparison to results presented in this thesis using AOS-based TFTs to implement a similar circuit.

2.4.1 Inverter Operation

Inverters consist of a single control transistor operating as a switch that is in series with a load. Their function is to provide an output that is the digital opposite of the input signal; i.e., if the input is a high signal the output will be a low signal. Figure 2.4 illustrates a standard voltage transfer characteristic (VTC) for an inverter. If the input voltage to the control transistor is less than the turn-on voltage of the transistor, negligible current flows in the inverter and there is little to no voltage drop across the load, resulting in a high output signal (V_{OH}). Once the input

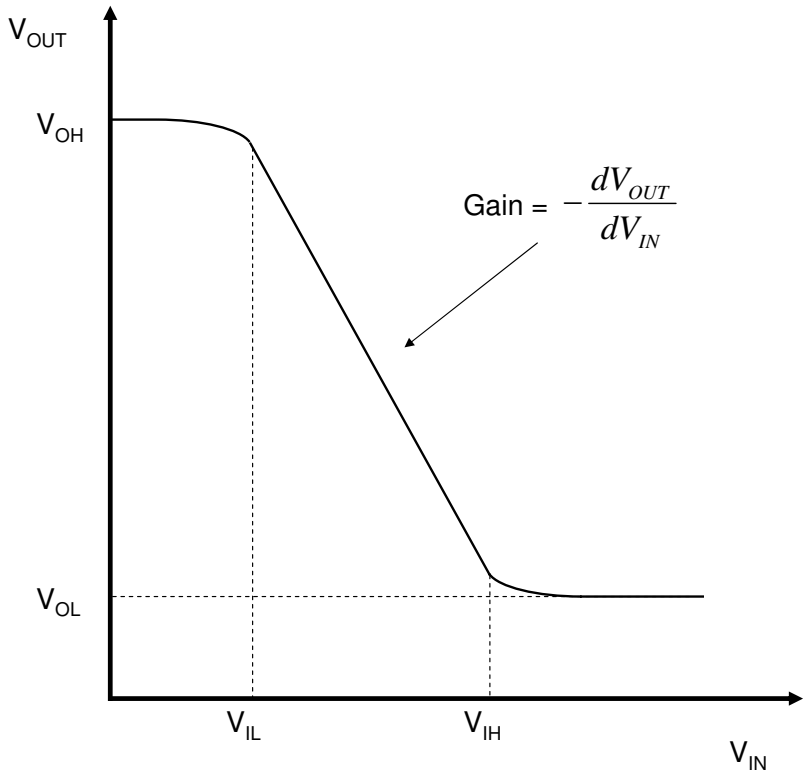


Figure 2.4: A representative voltage transfer characteristic (VTC) for an inverter. At input voltages below V_{IL}, the control transistor is off and negligible current flows through the inverter, hence the output voltage is at a relatively constant high level, V_{OH}. As the input voltage increases beyond V_{IL}, the control transistor turns on allowing increasing current to flow through the inverter causing a concomitant increase in the voltage drop across the load. Once the input exceeds V_{IH}, the inverter has reached a steady state in both the current and output voltage. The gain of an inverter is defined as the maximum change in output voltage with respect to a change in the input voltage; this corresponds to the slope of the VTC between V_{IL} and V_{IH}. It is typically quoted as a positive number, hence the negative sign.

voltage exceeds the turn-on voltage (V_{IL} on the representative VTC), appreciable current starts to flow through both the control and the load device, resulting in an increasingly large voltage drop across the load. Hence, as the input voltage is increased, the current through the control transistor increases while there is a concomitant decrease in the output voltage. Eventually a steady state is reached, depending on the nature of the load, and the current through the inverter and the output voltage saturates as seen for voltages larger than V_{IH} in Fig. 2.4.

The simplest load is a resistor, but there are two major drawbacks to this approach. First is power consumption when current is flowing and second is the physical area required to implement a resistor on-chip. Larger resistances are desirable because they lead to a higher gain, where the gain of an inverter is defined as the change in output voltage with respect to the change in input voltage,

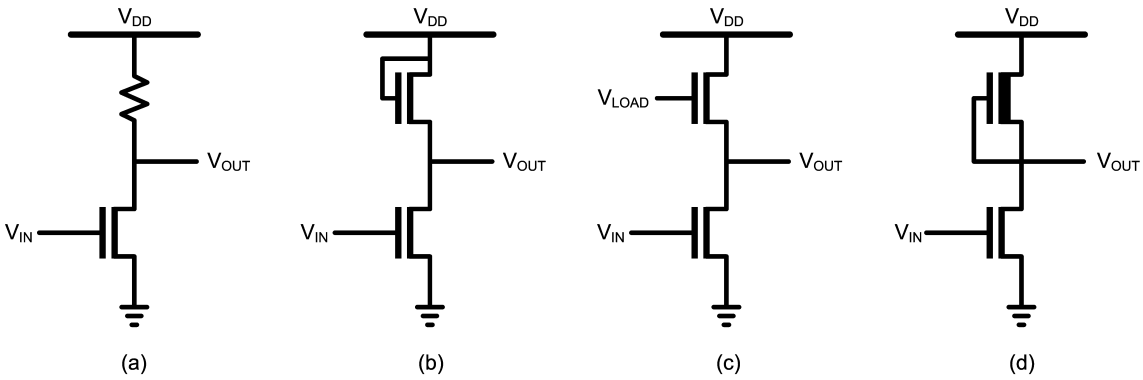


Figure 2.5: The four most commonly implemented inverter structures for NMOS technology. The differentiating factor between these structures is the load. The simplest scenario is a resistive load as depicted in (a). An active load is preferred, however, because a transistor requires far less area to fabricate. (b) and (c) depict an enhancement-mode NMOS transistor as the load operating in the saturation (b) and pre-saturation (c) regimes. A depletion-mode load is depicted in (d); the normally-on nature of the device allows the gate to be tied to the source.

$\frac{dV_{OUT}}{dV_{IN}}$. Larger resistances, though, require larger areas. In the beginning of large scale integration of ICs on silicon in the early 1970s, it would have taken approximately 18 times as much area to implement a 20 kΩ resistor as the control transistor; with decreasing transistor sizes this would surely be a much larger penalty with modern technology. [52] An alternative to a resistive load is to use another transistor as the load or as another switch; this alleviates both of the problems of resistive loads. It is currently standard practice to use complimentary-MOS (CMOS) transistors to effectively implement two switches controlled by a single input, one to pull the output up (the PMOS transistor) and one to pull the output down (the NMOS transistor). However, in a unipolar technology such as the present state of AOS-based TFTs, this is not possible.

Thus, a transistor load of the same polarity as the control transistor must be used. The load is classified by whether it is a depletion- or enhancement-mode device and, if it is enhancement, whether it is operating in the saturation or pre-saturation regime. Figure 2.5 illustrates the four most common loading possibilities. There are pitfalls to using enhancement-mode transistors in either case. If a saturation transistor is used, the gate is tied to the drain as seen in Fig. 2.5(b) and V_{OH} is reduced to V_{DD}-V_T, compared to the ideal maximum high output of V_{DD} when using a resistive load. If a pre-saturation load is used, it requires an independent voltage source to bias the gate of the load to ensure operation in this regime. This results in additional complexity and more chip area for interconnects and possibly signal conditioning.

The most ideal same-polarity load is a depletion load. [53] Its default on-state allows the gate to be tied to the source, as illustrated in Fig. 2.5(d), while allowing conduction to occur until V_{OUT} reaches the rail voltage, V_{DD}. In crystalline silicon technology, the body effect becomes very

critical when examining the load transistor, since its source is not tied to ground but rather to the output terminal. However, the body effect does not play a role for TFTs. To date, all reports of inverters based on AOSs in the literature use enhancement-mode loads.

A ring oscillator is formed by cascading an odd number of inverters together and tying the output of the final inverter back to the input of the first. Since an odd number of inverters are used, the polarity of the output of the final stage is always opposite the input of the first, resulting in an indefinite oscillation (assuming that the gain of each inverter stage is greater than 1). The dynamic response of an inverter is not instantaneous; there is always some finite delay as the control gates switch polarity and the output of each stage changes from low to high or vice versa. A ring oscillator is a convenient way of determining the propagation delay, t_p, of an inverter stage. The overall oscillation frequency is equivalent to $1/2Nt_p$, where N is the number of inverter stages (typically 5 or more). This oscillation frequency is of interest because it is one way of determining a technology's dynamic performance capability.

2.4.2 Previous Reports of AOS-Based Circuits

In 2006, Presley *et al.* reported on the first transparent ring oscillator based on IGO TTFTs. [46] The details of fabrication are discussed in Sec. 2.3.3. The VTC for an inverter shows a high output voltage level ∼4 volts below the applied V_{DD} voltage, due to the use of the enhancement load. The gain of the inverter is plotted versus V_{DD} and is shown to increase somewhat with increasing voltage and to saturate at a value of ∼1.5. The gain is a function of the current drive between the load and control transistors; thus voltage-dependent mobility, relative transistor sizing, and biasing conditions all affect the gain.

The oscillation frequency for a 5 stage ring oscillator is found to vary approximately linearly with increasing V_{DD} up to a maximum of ∼9.5 kHz at an applied bias of 80 V. With a 30 V bias, the output peak-to-peak voltage is ∼8 V with an oscillation frequency of ∼2.2 kHz. Simulations of the circuit using the gate voltage dependent average mobility show good agreement with the actual oscillation frequency, whereas if the incremental mobility is used in the simulation the oscillation frequency is over-estimated by a factor of 4. It is also noted that any parasitic capacitances in the circuit negatively affects the output frequency. For this design, large gate-source/gate-drain overlaps of 200 μm are used for ease of fabrication, resulting in ∼141.7 nF/cm of parasitic capacitance per TTFT. The channel length of the transistors is directly related to the switching speed and is also large at 60 μm. There is clearly room for improvement by decreasing dimensions. Thus, these results should be viewed as proof-of-concept for the integration of AOS-based circuits rather than performance benchmarks for them.

In 2007, Ofuji *et al.* [54] and Hayashi *et al.* [55] reported on the fabrication of a 5 stage ring oscillator based on IGZO TFTs operating as enhancement-mode transistors. A trilayer of Ti/Au/Ti is first deposited onto a glass substrate and patterned with lift-off to form the gate electrode. Both an SiO_2 and IGZO layer are rf magnetron sputtered over the gate and patterned photolithographically with wet etching to form the insulator and channel, respectively. The stack is then annealed to 300 °C for 20 minutes in air. The staggered devices are finished with Au/Ti top contacts deposited by e-beam and patterned by lift off. Channel lengths are 10 μm with gate-source/drain overlaps of only 5 μm.

The single inverter stage has a gain of 1.7, which is less than expected based on the geometrical ratios of the load and drive transistors. This difference is attributed to the voltage dependence of the mobilities; the load has a higher V_{GS} value than the control transistor, thus its mobility is expected to be higher. The actual gain agrees well with the square root of the effective beta ratio, which takes into account differences in mobility. The five stage ring oscillator begins to oscillate with the supply voltage as low as ∼1 V. Increasing the supply voltage linearly increases the output voltage swing while simultaneously decreasing the propagation delay per stage. With a supply voltage of $V_{DD} = 18$ V, the oscillation frequency is 410 kHz (corresponding to a propagation delay of 0.24 μsec/stage) with an output voltage swing of 7.5 volts peak-to-peak. Limited circuit simulation is performed using level 1 NMOS models. The output voltage range is correctly reproduced. However, the oscillation frequency varies to as much as twice as what is actually measured.

Hayashi *et al.* also briefly report on OLED cells driven by a two-transistor one-capacitor (2Tr-1C) circuit which is illustrated in Fig. 2.6. The fabrication is identical to that of the ring oscillator with the exception of a 200 °C anneal in air for 1 hour as opposed to the 20 minute anneal at 300 °C. The OLED cell is monolithically integrated with the backplane circuit. No discrete device performance is provided, but successful illumination of the OLED is reported,

Kim *et al.* [31] and Jeong *et al.* [30] of Samsung SDI have reported a full-color display driven by an IGZO backplane using 2Tr-1C circuitry. Discrete device fabrication and performance are discussed previously in Sec. 2.3.1. The display is a full-color 12.1 inch WXGA (1280x768 pixels) AMOLED display. There are 123 pixels per inch (ppi) with a reported sub-pixel pitch of 69x207 μm^2. LG has also reported an AMOLED display driven by an IGZO backplane, but the size was limited to 3.5 inch with a resolution of 176x144 pixels (QCIF). The reported display from Samsung is the largest and highest resolution of any AMOLED driven by amorphous oxide backplane circuitry to date.

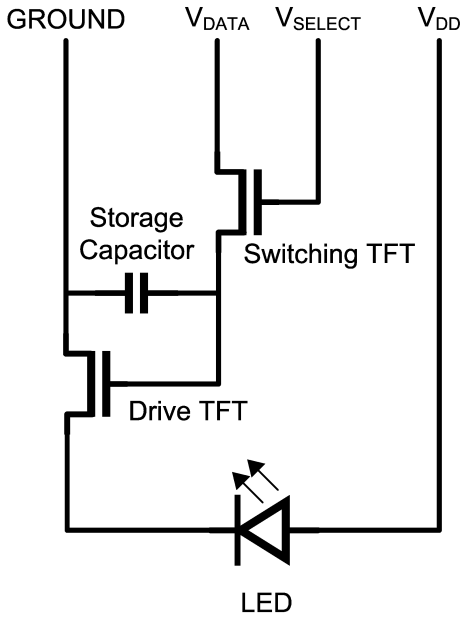


Figure 2.6: A two-transistor, 1 capacitor (2Tr-1C) pixel driving circuit. To date, this is the only circuit configuration implemented using amorphous oxide semiconductors which is not related to inverters.

2.4.3 AC/DC Rectification Using OTFTs

Rotzoll *et al.* report on AC/DC rectification at radio frequencies (13.56 MHz) using OTFTs with the intent that this rectification could be implemented in an RFID tag. [56] A direct comparison to these results is reported herein in an effort to demonstrate the superiority of AOS-based TFTs in high-speed applications. A thorough discussion of the switch-tied circuit design used is provided in Sec. 4.1.

Coplanar bottom-gate TFTs are fabricated on a polyethylene naphthalate (PEN) substrate. Gold is deposited and etched to form the gate contact. The dielectric, poly(4-vinylphenol) PVP, is spun onto the substrate, patterned, and etched to form vias. A second layer of gold is deposited and patterned using liftoff to form the source/drain contacts and fill the vias. A dielectric surface treatment is performed, followed by a thermal sublimation of the pentacene semiconductor to form the channel and complete the device. There is no intentional *in-situ* or post-deposition annealing. Steady-state parameters of the OTFT include a linear mobility of 0.296 $cm^2V^{-1}s^{-1}$, a saturation mobility of 0.356 $cm^2V^{-1}s^{-1}$, and a threshold voltage of 2 V indicating depletion mode operation (OTFTs are p-type whereas AOS-based TFTs are thus far exclusively n-type; thus a negative threshold is expected for enhancement-mode operation). The on-to-off drain current ratio is 2.4×10^2 when calculated between V_{GS} = 0 V and V_{GS} = -20 V. If the gate is biased to +10

V, the ratio improves to 1.26 $\times 10^5$. There is noticeable hysteresis between forward and backward voltage sweeps on the transfer curve.

It is asserted that the unity-gain bandwidth frequency for OTFTs is ∼1 MHz. [56] Thus, it has been assumed that operation of circuits based on OTFTs in this regime of frequency is not possible. It is proposed in this paper that, at such high frequencies, the transistors can operate successfully in a nonquasistatic (NQS) mode. To understand this terminology, it is helpful to imagine what occurs in a field-effect transistor when biases are first applied in terms of carrier transport and measured currents. Assuming an appropriate bias on all the terminals to turn the transistor on, charges are injected from the source and then transported across the channel length through the accumulation layer. Before this initially injected charge traverses the length of the device, a drain current cannot be measured. This initial time period is referred to as the turn-on delay, τ_d, and is expressed in terms of the mobility, lateral electric field E, and channel length L as $\tau_d = \mathrm{L}/\mu\mathrm{E}$. After the fastest carriers arrive, there is a gradual buildup in drain current as the channel carrier density reaches its equilibrium value and the drain current reaches a steady state. NQS operation happens when the excitation changes slower than τ_d, thus allowing measurable current to flow, but also changes too rapidly for equilibrium to be established. In order to have successful operation at 13.56 MHz, it is suggested that τ_d must be less than 18.4 ns; this is the time between a zero and peak value for a sine wave at this frequency. For the OTFTs reported, the turn-on delay is calculated to be 13.8 ns.

The switch-tied rectifying circuit was driven by a floating differential sine wave created by a sinusoidal waveform generator passing through a balancing transformer. The rectifier input and output were monitored with an oscilloscope and a digital voltmeter. The value of the load resistance is varied while three different frequencies are explored; 1 MHz, 5 MHz, and 14 MHz. The resistance of the probes used for the oscilloscope is not provided. The output voltage is normalized to a 10 V_{RMS} input.

There is a substantial degradation in output voltage between the three frequencies. At a load resistance of ∼0.75 Ω, the output voltage changes from ∼6.75 V, ∼5.25 V, and ∼2.00 V for the frequencies of 1, 5, and 14 MHz, respectively. To further explore the effect of frequency on the output, a constant load of 10 MΩ is applied to the output while the frequency is swept from 0 to 20 MHz. The output decreases in a roughly linear manner from a peak of ∼8 V at 0 MHz to ∼1 V at 20 MHz. Despite this degradation in performance at higher frequencies, the voltage efficiencies obtained are deemed adequate for implementing an RFID tag using organic technology.

2.5 Conclusions

This chapter provides a brief historical context to show the evolution of two branches of technology, the TFT and transparent electronics, and their merger in amorphous oxide semiconductors. Brief tutorials on transistor and inverter operation are presented, as both topics are of direct relevance to the work contained herein and the results presented in the literature review. Performance of transistors based on different material sets and experimental techniques are reported in addition to all known circuit implementations of amorphous oxide semiconductors. Finally, a brief summary of an AC/DC rectifier implemented using organic TFTs is provided for direct comparison to the results presented in this thesis.

3. EXPERIMENTAL TECHNIQUES

This chapter discusses fabrication techniques employed to create the circuits presented in this thesis. In addition, discrete TFT electrical characterization methods, drain current modeling and simulation, and nomenclature for describing alternating-current signals are discussed.

3.1 Thin-Film Transistor Fabrication

Processes used in semiconductor fabrication can be broadly classified into two categories; they are either additive (depositions) or subtractive (etches). Further classification can be accomplished by determining whether the driving mechanism of a process is purely physical, chemical, or some combination of the two. Examples of both physical and chemical deposition are present in this work, in addition to chemical (wet) etching. Patterning via shadow masks and photolithography are also discussed.

3.1.1 Physical Vapor Deposition

3.1.1.1 Thermal Evaporation

Thermal evaporation is used to deposit materials with relatively low melting points under high vacuum. Solid source material is placed in a conductive filament or boat and subsequently heated by passing large currents through the source holder. Evaporation occurs when the source material melts and subsequently evaporates or directly sublimes. This method is used for depositing aluminum as the top source/drain contacts for staggered bottom-gate TFTs in this work.

3.1.1.2 Sputtering

Sputtering is a process by which atoms are ejected from a target when it is struck by energetic particles; the ejected atoms are subsequently deposited onto the substrate. The process takes place in low- to medium-vacuum (1 to 50 mTorr) ranges with energetic ions generated by a plasma glow-discharge. The plasma is created by applying a bias across the target and the substrate, which are initially electrically isolated. This results in the entire potential difference being dropped across the space between electrodes, which typically contains argon gas. Any free electrons in the chamber are accelerated by the applied electric field between the target and substrate and gain kinetic energy; the amount of energy gained by the carriers is dependent upon the mean free path length, which is defined as the average distance between collisions. At low kinetic energies, any collisions between electrons and Ar atoms are elastic, resulting in little energy being exchanged between the electron and the Ar atom. If electrons gain sufficient energy before colliding with an Ar atom, however, then

the collision is inelastic and the kinetic energy of the free electron results in either the excitation or ionization of an Ar atom. If an Ar atom becomes excited, when it relaxes it releases a photon in the visible spectrum. If an Ar atom becomes ionized, there are now two free electrons being accelerated by the applied bias. These two processes are responsible for creating the glow and sustaining the plasma.

Once an Ar atom becomes ionized, it now also experiences an accelerating force due to the electric field and becomes accelerated towards the target. Due to the general motion of argon ions and elastic collisions, neutral Ar atoms are also propelled toward the target. If the impinging argon species have an appropriate amount of kinetic energy when they strike the target, they can cause surface atoms of the target to be dislodged and ejected towards the substrate. It is possible for sputtered molecules to also undergo scattering events, resulting in a decreased energy when they deposit onto the substrate, typically resulting in a poorer quality film. In an effort to minimize scattering events of sputtered species, the target-to-substrate distance is typically maintained at 5-10 cm.

Several variations are possible for the sputtering process. The process described above assumes use of a dc bias applied across the target and substrate, however a radio frequency (rf) alternating signal can also be applied. Dc sputtering yields higher deposition rates and requires less expensive equipment than rf sputtering but has the drawback that insulating targets cannot be sputtered. Whenever a positively charged ion impinges onto a target surface it captures an electron; if the target is a conductor, this captured electron is easily replaced by electrical conduction. If a target is insulating, however, the charge on the surface of the target cannot be easily replenished and the surface of the target develops a positive charge. This results in a decreasing potential difference between the anode and cathode, eventually leading to extinction of the plasma. Rf sputtering avoids this problem by varying the polarity of the bias at the target; any positive charges accumulated during the first half of the applied rf signal are replaced with electrons during the second half. Since electrons have much less mass than the positively charged Ar^+ ions, they respond much more rapidly to the change in polarity. Hence during two equally long bias periods of opposite polarity, more negative charge accumulates on the surface than positive charge. This results in a negative self-bias being established at the insulating target surface which allows for positive ions to always be attracted towards the target.

Magnetron sputtering is another sputtering variation. The inclusion of a magnetic field near the target results in an increase in the percentage of free electrons causing ionization collisions near to the target. This allows for the glow-discharge to be maintained at a lower pressure (e.g., $\sim$1 mTorr versus $\sim$20 mTorr). The lower pressure results in a longer mean free path for the sputtered

species. While the magnetic field has a strong effect on the motion of the electrons, it leaves the path of Ar^+ ions effectively unchanged because of their relatively large mass. Magnetron sources are the dominant source configuration because of these benefits. A more thorough discussion of plasma theory and sputtering physics can be found in Wolf and Tauber, Volume 1. [57]

Sputtering has many advantages over thermal evaporation. The two most prominent are the scalability of the target size, which results in improved uniformity over large areas, and the compositional control. The composition of the deposited film usually matches the composition of the target material, making it ideal for multi-component systems such as amorphous oxide semiconductors. Rf magnetron sputtering is employed in this work to deposit the active layer of the thin-film transistors from ceramic targets. Processing pressure is kept constant at 5 mTorr, but other processing parameters including power and oxygen partial pressure are varied to optimize the TFT electrical performance.

3.1.2 Chemical Vapor Deposition

Unlike physical vapor deposition (PVD) methods where the source material is the same as the deposited material, chemical vapor deposition (CVD) processes rely on chemical reactions at the substrate surface between two or more species, typically in the gas phase, to generate the desired material. There are three main types of CVD reactors; atmospheric, low-pressure, and plasma-enhanced (PE). In this work, PECVD reactors are used. The plasma generation works as described for sputtering (except with different gases) and the purpose is not to accelerate ions for the purpose of bombardment but rather to increase the energy of the reactive species. Using the plasma for this purpose allows reactions to take place at lower temperatures. This is the key benefit of PECVD.

In silicon industrial applications, CVD is used primarily to deposit SiO_2, silicon nitride, and polysilicon thin films. PECVD SiO_2 is utilized in this work as the gate dielectric for TFTs in integrated circuits. The deposition of silicon dioxide is accomplished using two different primary chemical precursors: silane (SiH_4) or TEOS (tetraethyl orthosilicate, $Si(OC_2H_5)_4$). The respective chemical reactions for the two precursors are

$$SiH_4(gas) + 2N_2O(gas) \xrightarrow{200-400^\circ C, rf} SiO_2(solid) + 2N_2(gas) + 2H_2(gas) \tag{3.1}$$

and

$$Si(OC_2H_5)_4(liquid) + O_2(gas) \xrightarrow{250-425^\circ C, rf} SiO_2(solid) + \text{ by-products } (gas). \tag{3.2}$$

Silane is pyrophoric, meaning that it combusts spontaneously when in contact with air. TEOS is a fairly inert material, i.e., a liquid at room temperature, and is thus preferred for safety reasons. TEOS vapor can be supplied to the reaction chamber either through a bubbler using nitrogen as a carrier gas or through a direct liquid injection system. Both precursors have been explored in this work (based on tool availability at Oregon State University, Hewlett Packard, and Sharp Labs of America) and have shown similar results. However, all the results presented in later chapters are based on use of the silane precursor. The PECVD reactor at Oregon State University is a SEMI Group PECVD cold wall reactor that uses silane to deposit the SiO_2. The walls of the chamber are actively cooled in order to reduce deposition onto chamber walls; this sidewall deposition could possibly flake off and lead to contamination of the deposited film.

3.1.3 Etching

Etching is a process of removing a material from the substrate. This removal can be accomplished by purely chemical means in a wet solution, by physical means such as ion bombardment (effectively sputtering the material off the substrate), by a dry chemical reaction in a plasma, or by a combination of the physical bombardment and dry chemical reaction in a process referred to as reactive ion etching (RIE). Defining characteristics of an etch are its selectivity and shape profile. Selectivity is defined as the ratio of how quickly it removes the desired material compared to other materials present (i.e., the materials underneath what is being etched). A high selectivity is desired to reduce problems that may be encountered when over-etching of the desired material occurs. The shape of the etch profile is dependent on whether it is wet or dry and also the material properties of what is being etched. A wet etch removes amorphous material equally in all directions, resulting in an isotropic shape. Dry etches remove more material vertically than horizontally, thus these are anisotropic.

Wet etching is used exclusively in this work. The gate electrode (ITO) and channel material (IGO) are both etched with solutions of hydrochloric acid (HCL). The ITO is more difficult to remove and is etched in undiluted HCl ($\sim$12 M) for at least 4 minutes. The IGO is etched in a 4:1 solution of deionized water (DI) to undiluted HCl for 80 seconds. The SiO_2 layer is etched in a buffered hydrofluoric acid solution, also referred to as a buffered oxide etch (BOE). The etch rate for the BOE for thermally grown SiO_2 is $\sim$100 nm/minute. It is expected that a PECVD deposited oxide is less dense and etches faster. Due to the geometry of the staggered bottom-gate TFTs used, there is good selectivity between the different etches; i.e., the HF has little to no effect on the ITO when opening vias to the gate layer and diluted HCl has no effect on the SiO_2 when

patterning the active channel. The top contact layer is patterned via liftoff, as discussed in Sec. 3.1.4.1.

3.1.4 Patterning

To successfully fabricate devices and integrated circuits, the deposition and/or etching of different layers must be accomplished selectively. There are two types of patterning methods that are commonly used to accomplish this; shadow masking and photolithography. Shadow masking is only relevant for selectively patterning a deposition; a mask with the pattern to be transferred is physically held against the substrate during deposition. There are several problems associated with this technique. The physical contact can potentially damage the substrate through unintentional scratching or stressing while the deposited features are typically thinner at their edges than the at their centers. This non-uniform thickness is a result of shadowing from edges of the features on the physical mask and depends on the angle at which the deposited material is incident. In addition to thickness non-uniformity, there is also a physical limitation on the minimum feature size that can be created on the shadow mask; this minimum feature size is typically much larger than the channel lengths desired for circuit applications. The benefits to using shadow masks are their throughput and the lack of chemical etching. Hence, for rapid material development based on dc characteristics (i.e., I_D versus V_{DS} or V_{GS} plots) shadow masks are preferred. In this work, shadow masking is used to optimize sputtering conditions for channel material deposition.

3.1.4.1 Photolithography

Photolithography creates a mask directly on a substrate by exposing a photo-active polymer to a high-intensity ultraviolet (UV) light source through a mask. The general process flow for photolithography using a positive photoresist is:

1. Substrate coating: The photoresist is dispensed as a liquid onto the substrate. The substrate is then spun at high speeds (∼4,000 revolutions per minute) to achieve an even dispersion of the photoresist.

2. Prebake: The substrate and photoresist are exposed to moderate temperatures (80-100 °C) in an oven or on a hotplate to remove solvents from the remaining film, readying it for light exposure.

3. Mask alignment and exposure: The photoresist-coated substrate and mask are brought into close proximity and patterns on the mask and substrate are aligned. Once the alignment is satisfactory, the mask and substrate are brought into contact and a high-intensity ultra-

violet light source is illuminated through the mask. A physical change occurs in the bonding properties of the photoresist where it is exposed to light, making it easier to remove.

4. Development: The coated substrate is rinsed with a developer solution that is specific to the photoresist used. This solution removes the photoresist that has been exposed to the UV light.

5. Hard bake: The developed photoresist and substrate are again heated to harden the patterned photoresist.

6. Pattern transfer: The pattern in the photoresist is transferred to the substrate, either by chemical etching, as previously discussed, or by lift-off, which is discussed in the following.

7. Photoresist removal: The photoresist is removed from the substrate by either acetone, a specific photoresist stripper, or by an oxygen plasma clean referred to as an ash. An ash cannot be used when performing lift-off.

As mentioned previously, the above steps are relevant for a positive photoresist. This terminology arises from the nature of the development: where the mask is dark, the photoresist remains. Hence, after the photoresist is developed the pattern remaining is the same as what is on the mask. In a negative photoresist, the exposure to light has the opposite effect and makes the exposed areas resistant to removal. Thus, the developer removes the photoresist that was not exposed to the light and the remaining pattern is the opposite of the mask. Figure 3.1 illustrates this difference in the resulting patterns. It is possible to achieve the same pattern using the two different types of resist if the polarity of the mask is flipped; i.e., a positive mask (one that is mostly transparent with shaded features) with a positive photoresist gives the same pattern as a negative mask (one that is mostly shaded with open features) with a negative photoresist.

While photolithography is mostly used for the selective etching of materials, as depicted in Fig. 3.1, it can also be used for selective deposition by a process known as lift-off, as depicted in Fig. 3.2. By depositing and patterning the photoresist prior to the blanket deposition of a film, the locations where the material is to be deposited onto the substrate are explicitly controlled. Assuming that the thickness of the deposited film is thinner than the photoresist, unwanted regions can be removed along with the photoresist. This process is useful when etching is not an option either because of a material's robustness or a lack of selectivity between two materials.

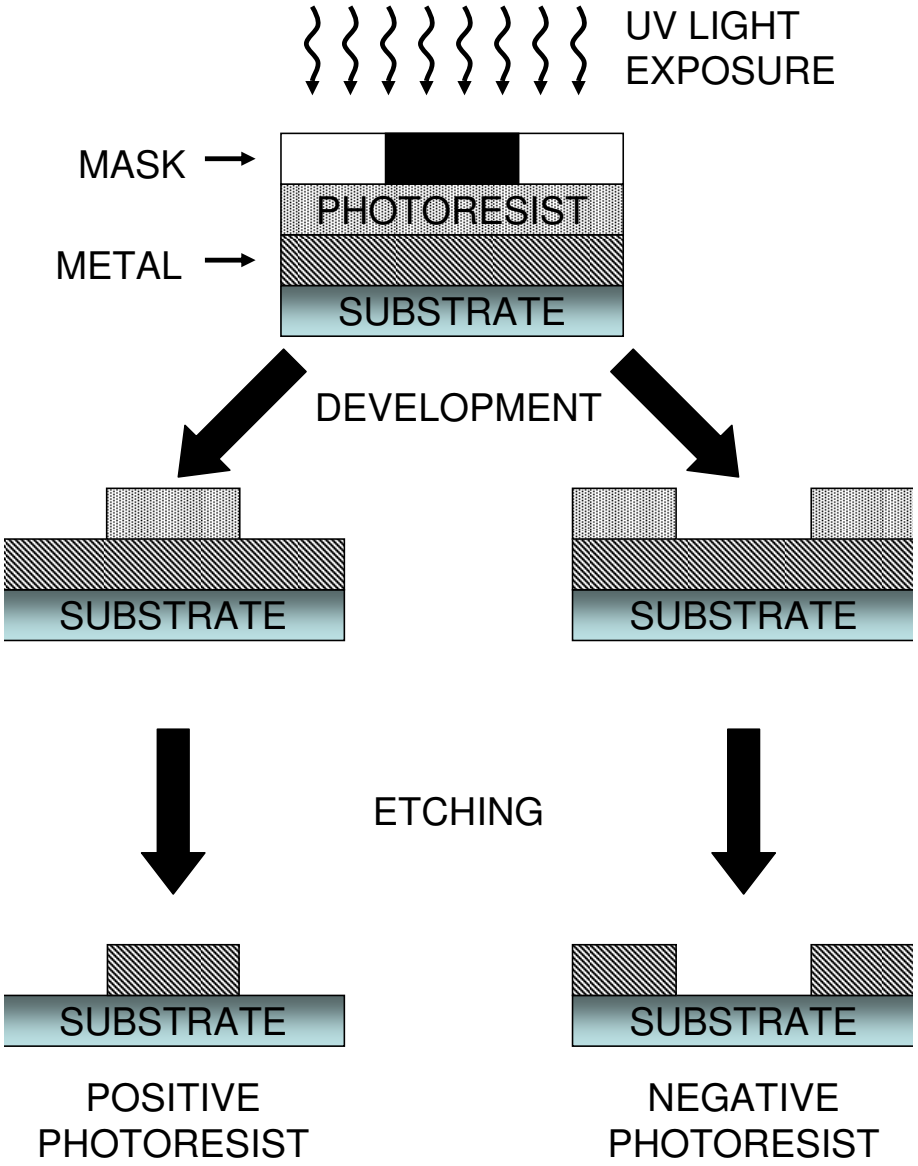


Figure 3.1: Pattern transfer using photolithography and etching with a positive mask (mostly transparent with dark features) and both positive and negative photoresists. The positive photoresist results in the same pattern as the mask being transferred while the negative photoresist inverts the final pattern.

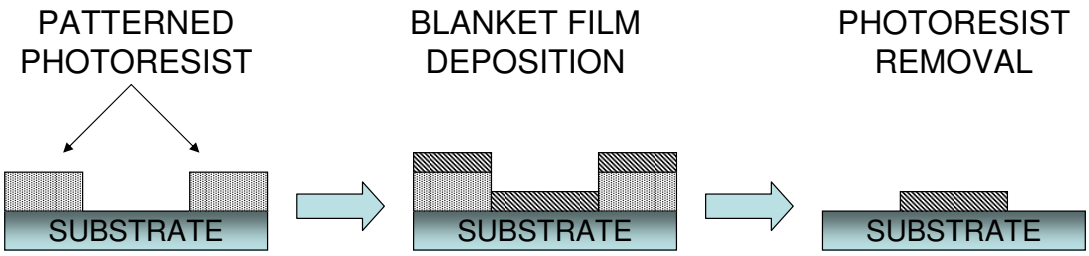


Figure 3.2: Pattern transfer using lift-off. The unwanted material is removed from the substrate along with the patterned photoresist.

3.2 Electrical Characterization

Electrical characterization is used to quantitatively evaluate a device's performance. A brief discussion of the primary electrical parameters used to describe TFTs is provided here, in addition to the methodology employed to extract these parameters from measured data. The parameters include V_T, V_{ON}, the drain current on-to-off ratio, and mobility.

3.2.1 Threshold and Turn-On voltage

The threshold voltage V_T is most the commonly referenced voltage of importance when describing a MOSFET. It is physically attributed to when the inversion layer is initially formed; hence above this threshold conduction in the channel can readily occur. For a MOSFET to be considered on, the gate voltage must be in excess of V_T and the condition for operation in the saturation regime is that $V_{DS} \geq V_{DSAT} = V_{GS}$ - V_T. There are two primary methods for extracting V_T, based on experimental current-voltage relationships. The first is to plot I_D versus V_{GS} on a linear scale with a small V_{DS} to ensure operation in the presaturation regime. The linear portion of this curve is then extrapolated back to the x-intercept, which corresponds to V_T + $\frac{1}{2}V_{DS}$. The second method is to apply a sufficiently large drain voltage to ensure operation in the saturation regime and then to plot $\sqrt{I_D}$ versus V_{GS}, again on a linear scale, and to extrapolate the linear portion of the curve back to the x-intercept, which now directly corresponds to V_T.

While there are many structural and operational similarities between TFTs and MOSFETS, the full relevance of V_T to an accumulation-mode unipolar TFT is ambiguous. Since there is no inversion layer, V_T loses its physical significance and becomes simply a modeling parameter. Having multiple extraction methods for V_T, which could potentially yield different results, and also room for interpretation as to where the "linear portion of the curve" begins in the two extraction methods further dilutes the concept of V_T.

A parameter with more physical significance for a TFT is the turn-on voltage, V_{ON}. This is defined as the onset of conduction or, more simply, where the drain current initially deviates

from its off current level. This is clearly visible when the drain current is plotted versus V_{GS} on a logarithmic-linear scale. V_{ON} also has significance when extracting the average mobility and when modeling the gate voltage dependence of mobility in a TFT, as discussed in Sec. 3.2.3. In this work, V_{ON} is determined with $V_{DS} = 30$ V.

3.2.2 Drain Current On-to-Off Ratio

The drain current on-to-off ratio is of interest for any switching applications and also as a measure of current drive. It is the difference between the off-current level and the maximum on-current level, in this work taken at $V_{GS} = 40$ V and $V_{DS} = 30$ V. For switching applications, an on-to-off ratio of greater than $\sim 10^6$ is typically desired. As a cautionary note, this parameter is highly susceptible to the off-current level. The off-current is a function of the insulator used, any subsequent processing that may damage the insulator, and also the noise floor of the measurement equipment. For completeness when reporting device parameters, the transfer curve should be provided or the off-current should be explicitly stated.

3.2.3 Mobility

Mobility is arguably the most important electrical parameter when describing a transistor's performance. It is a measurement of how quickly a carrier can move in a given material and, thus, has a direct impact on the current drive and potential switching speeds; i.e., the time it takes to turn a device on or off. Three different types of mobility and their extraction from experimental data are briefly discussed here; incremental, average, and saturation. In crystalline silicon technology it is commonly assumed that the mobility is defined exclusively by a material's physical properties and is independent of the bias applied. This leads to mobility being described as a constant, usually in the context of the square-law model. This is not the case for AOS-based TFTs where the mobility is shown to be a function of V_{GS}. A more thorough discussion of mobility extraction for TFTs can be found in Hoffman. [58]

3.2.3.1 Incremental Mobility

Incremental mobility μ_{inc} represents the mobility of carriers as they are incrementally added to the channel via a small increase in the gate voltage. This type of mobility is useful for studying the physical nature of conduction in the channel since trapping mechanisms that affect initially injected carriers at low applied gate voltages do not affect the incrementally added charges at higher biases. This provides insight into the ultimate performance potential of a material. μ_{inc} is

defined as

$$\mu_{inc}(V_{GS}) = \left.\frac{G'_{CH}(V_{GS})}{\frac{W}{L}C_{ins}}\right|_{V_{DS}\to 0} \tag{3.3}$$

where W and L are the transistor width and length, respectively, C_{ins} is the insulator capacitor, and G'_{CH} is the differential channel conductance. The channel conductance G_{CH} is defined as [58]

$$G_{CH}(V_{GS}) \equiv \lim_{V_{DS}\to 0}\left(\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}}\right) \cong \left(\left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}}\right)\Bigg|_{V_{DS}\to 0} \tag{3.4}$$

and the differential channel conductance G'_{CH} is defined as

$$G'_{CH}(V_{GS}) = \frac{dG_{CH}}{dV_{GS}} \cong \frac{\Delta G_{CH}}{\Delta V_{GS}}. \tag{3.5}$$

Note that the approximate forms of Equations 3.4 and 3.5 are discretized to allow for application to measured data.

3.2.3.2 Average Mobility

Average mobility μ_{avg} describes the mean mobility of all of the carriers in the channel at any given gate votlage. This provides a better idea of transistor performance in circuit applications. μ_{avg} is defined as [58]

$$\mu_{avg}(V_{GS}) = \left.\frac{G_{CH}(V_{GS})}{\frac{W}{L}C_{ins}\left[V_{GS} - V_{ON}\right]}\right|_{V_{DS}\to 0}, \tag{3.6}$$

which is almost identical to the expression used to describe μ_{eff} for a MOSFET; the primary differences being the use of V_{ON} in the denominator instead of V_T and the gate voltage dependence of the channel conductance.

3.2.3.3 Saturation Mobility

Saturation mobility is the least used type of mobility in conventional silicon MOSFET technology, but it has the advantage of being less sensitive to series resistance than μ_{inc} and μ_{avg}. μ_{sat} is determined from the square-law model of drain current in saturation and is defined as [59]

$$\mu_{sat} = \frac{2m^2}{\frac{W}{L}C_{ins}} \tag{3.7}$$

where m is the slope of the linear portion of a $\sqrt{I_D}$ versus V_{GS} plot when the transistor is operating in the saturation regime. Saturation mobilities are not reported for TFTs fabricated in this work.

3.2.4 Simulation

Since both μ_{avg} and μ_{inc} are functions of gate voltage, simple Level 1 modeling in SPICE that relies on the square-law model and assumes a constant mobility is likely not adequate for describing the drain currents of TFTs. A closed-form dc model which accounts for this gate voltage dependence has been demonstrated by Hoffman. [60] μ_{avg} is redefined as a function of the effective voltage, $\mu_{avg}(\mathrm{V}_{eff})$, which is equivalent to $\mu_{avg}(\mathrm{V}_{GS})$ shifted by -V_{ON}. An nth-order polynomial is fit to $\mu_{avg}(\mathrm{V}_{eff})$ with the form [60]

$$\mu_{avg}(V_{eff}) = \begin{cases} 0 & \mathrm{V}_{eff} \leq 0 \\ \sum_{i=0}^{n} c_i \left[V_{eff}\right]^i & \mathrm{V}_{eff} > 0 \end{cases}. \tag{3.8}$$

This polynomial is used to model the drain current. As an example, the drain current in the saturation regime is defined as [60]

$$I_D = C_{ins} \frac{W}{L} \sum_{i=0}^{n} \left(\frac{c_i}{i+2} \left(V_{GS} - V_{ON}\right)^{i+2} \right). \tag{3.9}$$

A sixth order polynomial with 8 digits of precision is fit to the mobility and used to model the currents and circuit performance in this work. Figure 3.3 illustrates the application of this model to the I_D-V_{DS} characteristic of an IGO-based TFT; the simulated results are shown to be in good agreement with experimental data for all modes of operation.

In simulating circuits, as opposed to discrete transistors, it has been observed that the sign on the coefficient of the largest power in the polynomial describing the mobility must be positive. Drain current models are only valid within the range of measured voltages for the mobility. Simulations of single transistors can be easily limited to this region by biasing the terminals of the device. However, when multiple transistors are used there are unbiased nodes for which the simulator will attempt to solve. If the coefficient of the largest power is negative, the modeled drain current is eventually pulled down to a negative value for large a bias, as depicted in Fig. 3.4(a). This eliminates the uniqueness of the current-voltage relationship and can result in simulations converging on unrealistic bias points since the simulation is not easily limited to the valid voltage range. If the largest power is positive, the current-voltage characteristics remain diodic and unique, as illustrated in Fig. 3.4(b), allowing circuit simulations to converge to appropriate bias points.

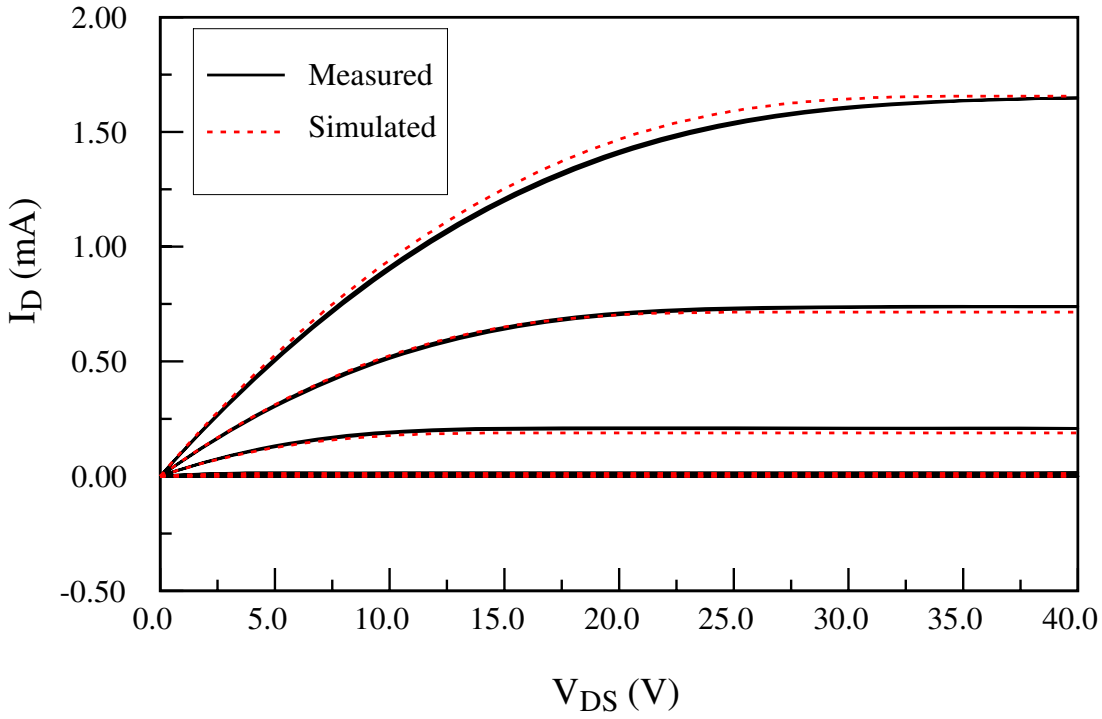
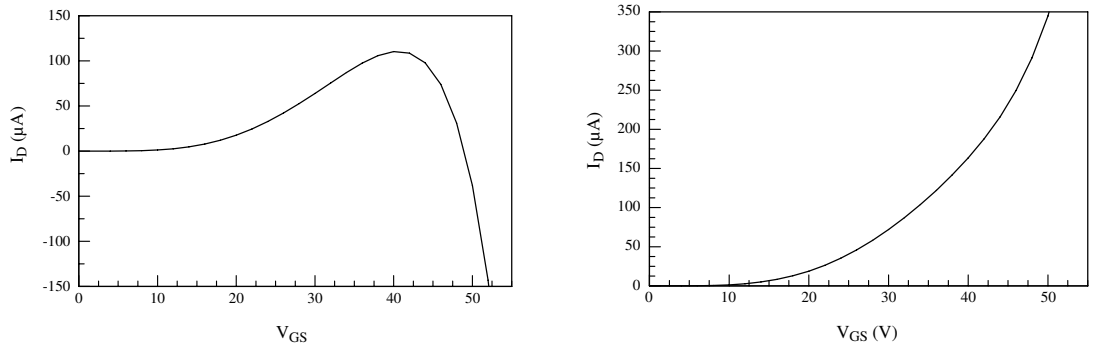


Figure 3.3: Comparison of measured and simulated drain current output curves for an IGO TFT. The drain voltage is swept from 0 V to 40 V while the gate voltage is stepped from -10 V to 40 V in 10 V steps. The modeled current is shown to be in good agreement with experimental data. The drain current model takes into account the gate voltage dependence of the mobility by fitting a sixth order polynomial to measured μ_{avg} data and using the coefficients of the polynomial to model the current using a closed-form model as suggested by Hoffman. [60]



(a) Negative highest-order coefficient

(b) Positive highest-order coefficient

Figure 3.4: When modeling the drain current using a closed-form DC model based on a polynomial fit of the voltage-dependant mobility, it is important to verify that the coefficient of the largest power in the polynomial fit is positive. If the coefficient is negative, as seen in 3.4(a), the modeled drain current will eventually be pulled negative at large biases. This eliminates the uniqueness of the current-voltage relationship and can result in simulations converging on unrealistic bias points. If the coefficient of the largest power is positive, then the current-voltage characteristics remain unique and simulations can converge on appropriate bias points.

3.3 Signal Characterization and Generation

Sine waves are commonly used as the input to rectifiers so the reader needs to be familiar with how they are characterized in order to compare results from different sources. The defining characteristics of a sine wave are its amplitude, frequency, and phase angle. For this work, phase is neglected since the time scale used for measurements can be arbitrarily shifted to ensure that the phase angle is always 0. Figure 3.5 illustrates one period of a sine wave with its characteristics labeled. The angular frequency of a sine wave is described by the standard relationship $\omega=2\pi f$. ω is the angular frequency, measured in radians per second, while f is the frequency measured in Hertz and equal to the inverse of the waveform period T. Hence a period of $T = 1\times10^{-6}$ seconds corresponds to a frequency of f = 1 MHz. The amplitude of a sine wave is characterized by its peak value (assuming the wave is centered around zero). The total amplitude of the sine wave is the peak-to-peak or peak-to-trough value, which is twice the peak value. It is also common to refer to root-mean-square (rms) value which, for sine waves, is equal to the peak value divided by $\sqrt{2}$.

A differential sine wave is used to drive the rectifying circuits reported herein. It is generated by passing a single-ended sinusoidal signal from an HP 3325B synthesizer/function generator through a balancing transformer to create a floating differential drive. Each phase of the differential signal is passed through two identical amplification stages, based on National LM7372MR opamps configured for a gain of ∼4/stage, resulting in an overall gain of ∼16 per phase. The signal

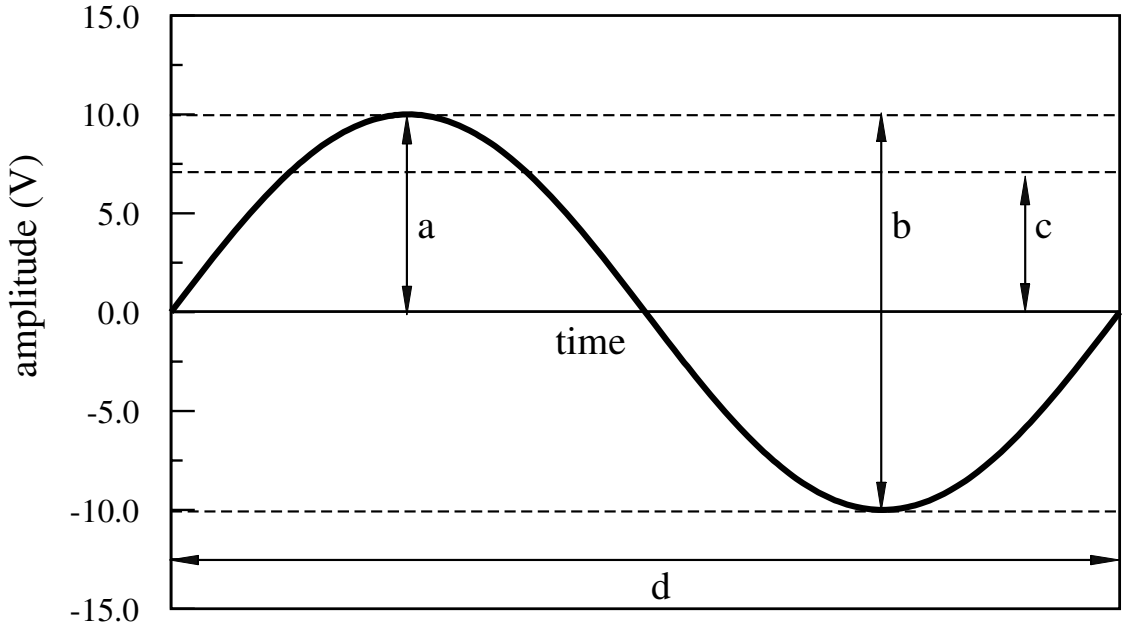


Figure 3.5: The defining characteristics of a sinusoidal voltage wave are: (a) V_{peak}, (b) $V_{peak-to-peak}$, (c) V_{rms}, and (d) the waveform period T.

generator is limited to a maximum sine wave output frequency of 20 MHz. The amplification unit is actively cooled with a heat sink and a fan for operation in this frequency regime.

4. AC/DC RECTIFICATION USING AOS-BASED TFTS

This chapter is devoted to the implementation of AC/DC rectifiers using two different circuit configurations based on AOS TFTs.

4.1 Full-Wave Rectification Circuits

Full-wave rectifiers are commonly used for power or signal conditioning in a variety of circuit applications. One application of particular interest is that of an rf identification (RFID) transponder. Such transponders are typically passive devices embedded in identification cards or product labels that rely on coupling to external rf radiation provided by the RFID reader, typically at 13.56 MHz, to harvest the power necessary for their operation and communication. These frequencies are well in excess of what has previously been reported for AOS-based TFTs. [46, 54]

In silicon technology, a full-wave rectifier would likely be implemented with a full-bridge diode rectifier. However, many properties of amorphous oxide semiconductors make them attractive for this application including their relatively low cost, transparency, and improved flexibility compared to crystalline semiconductors. Diodes are not currently a viable option when using AOSs, thus a solution based on TFTs is required.

Figure 4.1 illustrates two possible configurations of a transistor which allow for rectification. Figure 4.1(a) is a diode-tied connection of the transistor where the gate terminal is tied to the drain, effectively turning the transistor into a two-terminal device with diode-like current-voltage characteristics. This arrangement ensures that when the transistor is conducting, it is operating in the saturation mode. A demerit of this configuration is that in order to turn the device on, a large voltage may be required, depending on the saturation voltage of the transistor. The other configuration, Fig. 4.1(b), is referred to as being switch-tied and requires a differential input source, i.e., one which has positive and negative terminals that are equal in magnitude and opposite in polarity. The benefit of this configuration is that the transistor is allowed to operate in the pre-saturation regime, resulting in less voltage drop across source and drain terminals.

Figure 4.2 illustrates two possible circuit configurations for full-wave rectification. Figure 4.2(a) uses four diode-tied transistors and is an exact analog to a full-bridge rectifier implemented with diodes (not shown). The positive output node is always one V_T lower than the highest potential in the circuit, while the negative output node is always one V_{ON} above the lowest potential, regardless of the phase of the input signal. Figure 4.2(b) uses two diode-tied and two switch-tied circuits to accomplish rectification. The diode-tied transistors between the inputs and the positive output terminal result in a similar one V_T drop from the highest potential in the circuit.

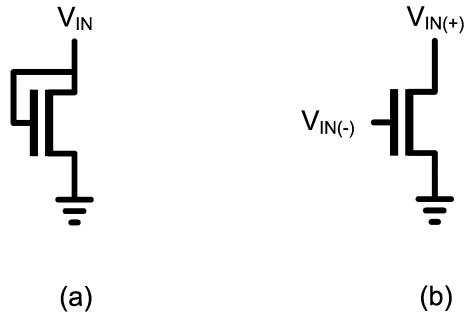


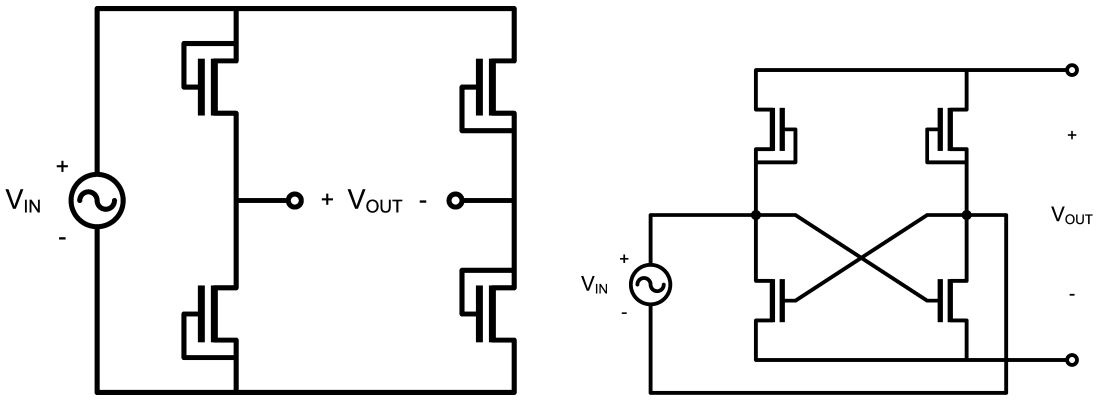
Figure 4.1: Two possible configurations for accomplishing rectification with a transistor. (a) A diode-tied configuration, where the gate is tied to the drain and the transistor becomes a two-terminal device. This configuration always operates in saturation and, because $V_{GS} = V_{DS}$, the voltage drop between the drain and source is always equal to V_T. (b) A switch-tied configuration which requires the use of a differential input source. The benefit of this configuration is that the transistor can operate with a much smaller voltage drop across the drain to source.

The switch-tied transistors between the inputs and the negative output terminal are effectively tying the lowest input potential in the circuit directly to the output through a much smaller voltage drop. The usable output voltage is the difference between the two output terminals. Thus, the switch-tied rectifying circuit is expected to have an improved output voltage; this difference is later illustrated in Fig. 4.4. Both rectifier implementations are present on the same mask set. Thus, they are fabricated simultaneously. The switch-tied circuit in Fig. 4.2(b) is an n-type analog to what was previously accomplished with p-type OTFTs, as discussed in Sec. 2.4.3. [56]

4.2 AC/DC Rectifier Fabrication

Fabrication begins with 25×25×1.1 mm Corning 1737 glass slides coated with ∼200 nm of ITO (purchased from Delta Technologies). Staggered bottom-gate TFTs are used in this application; there are 9 primary steps and 4 masks required to complete the integrated circuit. The masks are made with high-resolution printing (20,000 dots per inch) on mylar, limiting the minimum feature size to 10 μm. The masks are designed in AutoCAD and purchased from CAD/Art Services Inc.. The fabrication process follows:

1. Substrate cleaning: Substrates are first rinsed with 18 MΩ-cm Millipore water and then cleaned in an ultrasonic bath with a solution of Contrad70. Following the ultrasonic treatment, samples are thoroughly rinsed with ultra-pure water and finally cleaned with acetone, isopropyl alcohol (IPA), and Millipore water sequentially and placed in a dehydration oven at ∼125 °C for at least 10 minutes.



(a) Diode-tied Full Bridge Rectifier (b) Switch-tied Full Bridge Rectifier

Figure 4.2: Two full-wave rectifying circuits implemented using n-type TFTs. (a) Four diode-tied transistors, which is equivalent to a bridge rectifier typically implemented with diodes in silicon technology. (b) Two diode-tied and two switch-tied transistors; this configuration increases the output voltage.

2. Mask A: The gate electrode (ITO) is patterned using standard photolithographic techniques and ITO is etched using ∼12 M hydrochloric acid (HCL) for 5 minutes. A digital multimeter is used to verify that the substrate is no longer conductive, indicating that the ITO is completely etched.

3. Insulator deposition: ∼100 nm of silicon dioxide is deposited by PECVD. Both silane-based and TEOS-based chemistries were explored, however based on availability, the results presented here-in are from the silane-based films deposited at Hewlett Packard.

4. Channel deposition: IGO is deposited via rf magnetron sputtering from a circular 2 inch diameter target with a 1:1 molar ratio of In_2O_3:Ga_2O_3 (purchased from Cerac, Inc.) using a power density, argon/oxygen ratio, total flow rate, deposition pressure, and deposition time of 23.8 W/cm^2, 95/5, 42.2 sccm, 5 mTorr, and 10 minutes, respectively. These parameters were determined via a design of experiment approach, implemented using Si/SiO_2 substrates with the channel and source/drain layers patterned with shadow masks, to give a slightly positive and near-zero turn-on voltage. A representative transfer curve for these sputtering conditions is illustrated in Fig. 4.3.

5. Mask B: The channel layer is patterned using standard photolithographic techniques and etched in a ∼2.4 M HCL solution for 80 seconds.

6. Mask C: Contact holes (vias) are opened in the dielectric by etching using a buffered hydrofluoric (HF) acid solution that has an etch rate of ∼100 nm/minute for thermally grown

silicon dioxide. The vias could be patterned and etched prior to the channel deposition. However, the process sequence used is motivated by a desire to maintain a pristine interface between the semiconductor and insulator, free from exposure to the organic polymers in the photoresist.

7. Channel anneal: The substrate stack (gate, insulator, and IGO channel) is annealed in a box furnace. The thermal cycle begins at room temperature (∼22 °C) and increases at a rate of 2 °C/minute until the peak temperature of 400 °C is reached. The substrate is held at the peak temperature for 1 hour and then passively cooled to room temperature at ∼2 °C/minute. This step is performed after the insulator etch to help devolve any hydrogen ions that may have been introduced in the insulator because of the exposure to HF acid.

8. Mask D: Photoresist is deposited and patterned for the lift-off of the source/drain contacts.

9. Source/drain metal deposition: Aluminum is thermally evaporated to a thickness of ∼500 nm. Samples are soaked in acetone for 1 hour followed by a brief (∼15 seconds) sonication in the acetone solution to selectively remove unwanted aluminum via lift-off.

The channel width and length are 150 μm and 15 μm, respectively. The gate/source and gate/drain overlaps are 10 μm, resulting in per-transistor parasitic capacitances (ignoring any contribution from the semiconductor) of ∼1.0 pF. Transistors that are diode-tied have half of this capacitance, since the gate and drain are held at the same potential, thus eliminating the capacitance from this overlap.

If transparency is desired, the aluminum top contact can be replaced by sputtered ITO resulting in an entirely transparent circuit. Lift-off can still be used for patterning, thus the only difference would be the material deposition of step 8. Based on previous work, the entire stack would exhibit an average transmission of ∼75% in the optical portion of the electromagnetic spectrum. [46]

4.3 Electrical Characterization and Discussion

Figure 4.3 illustrates the log(I_D)-V_{GS} transfer curves with V_{DS} = 1 V (triangles) and V_{DS} = 30 V (circles) for a staggered bottom-gate IGO TFT fabricated on a thermally grown silicon dioxide/silicon substrate and patterned using shadow masks. The sputter deposition parameters and post-deposition anneal are identical to those used for the creation of the rectifiers. V_{ON}, V_T, peak μ_{INC}, peak μ_{AVG}, and the drain current on-to-off ratio are determined to be ∼1 V, ∼5.7 V, 14 $cm^2V^{-1}s^{-1}$, 10 $cm^2V^{-1}s^{-1}$, and ∼1×10^7, respectively. V_T is extracted in the saturation

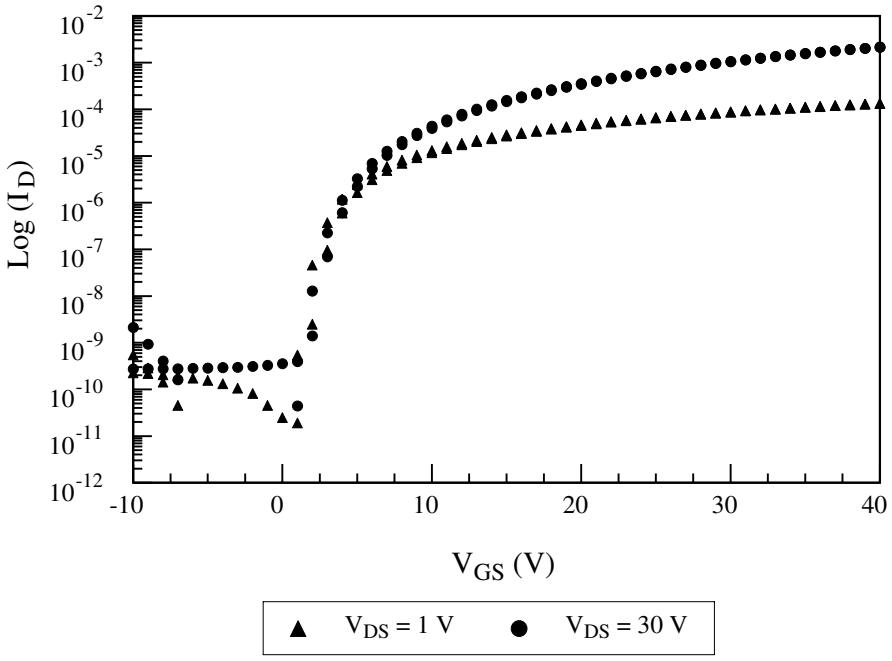


Figure 4.3: Log(I_D)-V_{GS} transfer curves with V_{DS} = 1 V (triangles) and V_{DS} = 30 V (circles) for a staggered bottom-gate IGO TFT fabricated on thermally grown SiO_2. The turn-on voltage is near zero and positive with much less than 1 V of clockwise hysteresis present at small gate biases. V_T, peak μ_{INC}, and peak μ_{AVG} for this device are ∼5.7 V, 14 $cm^2V^{-1}s^{-1}$, and 10 $cm^2V^{-1}s^{-1}$, respectively.

regime by plotting the square root of the drain current versus the gate voltage, as discussed in Sec. 3.2.1. Forward and reverse sweeps are plotted for both drain biases; approximately 1 V of hysteresis is observed. Current-voltage measurements are obtained using an Agilent 4156C Precision Semiconductor Parameter Analyzer with measurements taken in a dark box.

It is expected that the integrated transistors fabricated using PECVD silicon dioxide should exhibit slightly poorer performance. Previous reports show a peak incremental mobility of ∼7 $cm^2V^{-1}s^{-1}$ along with a decreased drain current on-to-off ratio of $\sim 10^4$. These effects are attributed primarily to the use of a different insulator with more surface roughness and also to non-idealities introduced by photolithography and etching. [46]

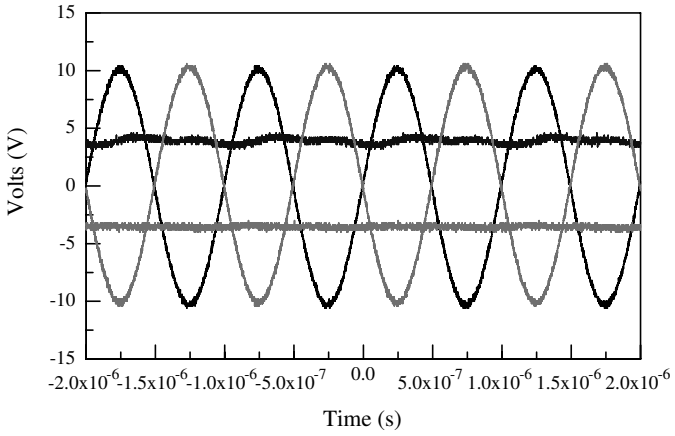
Figure 4.4 illustrates the normal output from the two rectifying circuits. There is no intentional load besides the active measurement probes in Fig. 4.4(a) and Fig. 4.4(b). The circuits are driven using a differential sine wave input of 20 V peak-to-peak at 1 MHz in all three cases. This drive voltage is equivalent to an rms voltage of 7.07 V. The output from both the positive and negative terminals are shown; the actual DC output voltage is the difference between these two terminals. Figure 4.4(a) corresponds to the bridge configuration and appears qualitatively ideal; the output terminals show little ripple and are symmetric, as expected for the bridge configuration.

Figure 4.4(b) corresponds to the cross-tied circuit. The positive output voltage terminal is comparable to that of the bridge configuration while the negative output voltage terminal is pulled down, closer to the lowest input value, thus increasing the DC output voltage level. However, there is substantially more ripple in both the output rails in Fig. 4.4(b). In the positive output rail this might be due to slight variations in transistor performance; if there is any mismatch in the voltage drops across the top two transistors, a perfectly flat steady state can never be reached. Since the negative output terminal in the cross-tied circuit is tied to the lowest input voltage, it is not too surprising that the output signal closely follows that of the input, since the voltage drop across the source-drain terminals is not fixed at V_T like the diode-tied transistors. If either circuit is loaded with a capacitor, the ripple can be reduced, resulting in a smoother DC output voltage. Figure 4.4(c) illustrates the improvement in the cross-tied output; it uses the same circuit and input signal as illustrated in Fig. 4.4(b), the only difference being the addition of a 10 pF capacitor load.

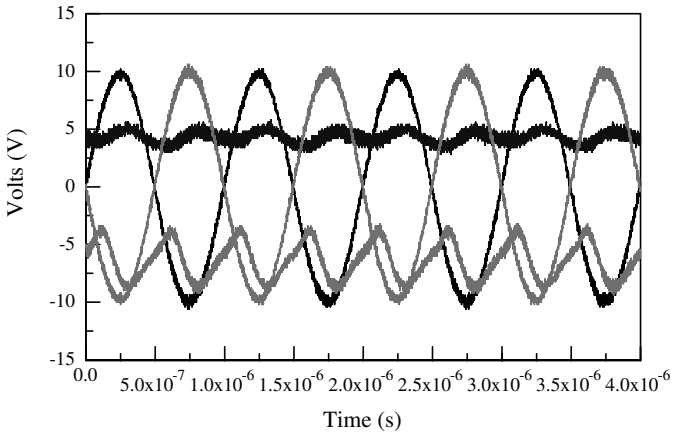
The effect of the load and input signal frequency on the output voltage is illustrated in Fig. 4.5. The input signal is a sine wave maintained at 20 V peak-to-peak (7.07 V_{RMS}) and supplied at several frequencies. The active probes provide a 2 MΩ and 0.05 pF load across the output terminals. In addition to this load, two standard probes are also landed across the output terminals and connected with a resistor. The applied resistance is varied among the following values: 100 kΩ, 300 kΩ, 499 kΩ, 750 kΩ, 1 MΩ, 5.6 MΩ, and 10 MΩ. The effective resistance seen by the circuit is reflected on the x-axis of Fig. 4.5.

Two general trends are evident from Fig. 4.5. First, exploring the effect of resistance on V_{OUT}, it is clear that increasing the load resistance monotonically increases the output voltage. There are several points where this trend is not explicitly followed, most notably at higher loads. This is attributed to noise in the measurement setup; a small amount of jitter is observed during testing with the oscilloscope. This noise is likely introduced by either added inductance from the wires used to apply the load resistance or coupling between the power lines supplying the driver circuit and the active probe leads. Whenever there is a decrease in output voltage with increasing resistance, the two values are within 3% of each other. This observation supports the hypothesis that this deviation from the trend is associated with random noise.

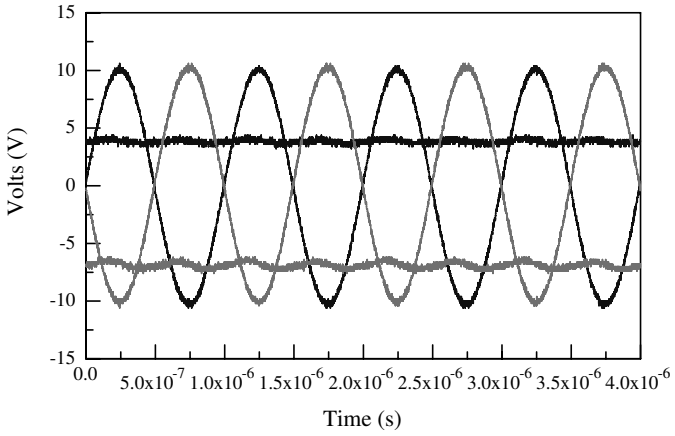
The second trend is a decrease in output voltage with increasing frequency. This frequency dependence of the output voltage is not reflected in simulations which take into account the intrinsic overlap capacitances of the transistors. Hence, there is a deficiency in current device or circuit modeling at these frequencies. As suggested elsewhere in the context of using OTFTs as rectifiers, this is likely due to the transistors operating in the non-quasistatic (NQS) regime. [56]



(a) Diode-tied full bridge rectifier



(b) Cross-tied rectifier



(c) Capacitively loaded switch-tied reftifier

Figure 4.4: Comparison of output versus input siganls for the two rectifying circuits. Black lines correspond to the positive input and output terminals while grey lines represent the negative terminals. The input signal is a differential 20 V peak-to-peak sine wave at a frequency of 1 MHz. The DC output voltage is the difference between the two output terminals. (a) The qualitatively ideal output of an unloaded diode-tied full bridge rectifier; the output signals are flat and of equal magnitudes. (b) The improved output swing created by the switch-tied transistors pulling the output down towards the negative input. However, as a result the negative output terminal slightly follows the sine wave nature of the inputs when unloaded, resulting in a varying DC output. (c) Loading the switch-tied circuit with a capacitor (10 pF in this case) greatly smooths the output.

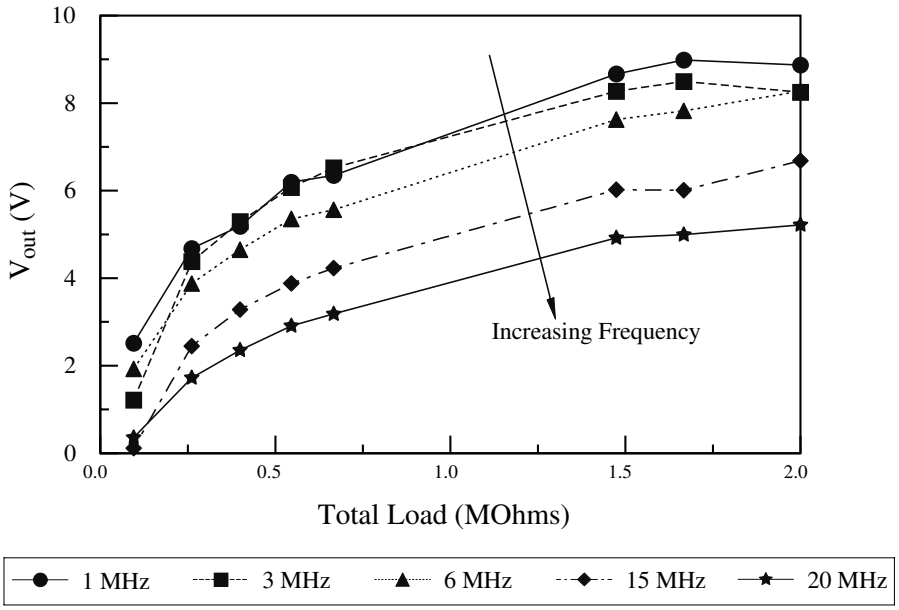


Figure 4.5: Output voltage as a function of load resistance for varying input frequencies. The input is a 20 V peak-to-peak fully differential sine wave. Two trends are apparent. First, output voltage generally increases with increasing load resistance and, second, decreases monotonically with increasing frequency. The few points where V_{OUT} does not increase with increasing load are attributed to noise in the measurement; note that whenever this is the case the two consecutive data points are within 3% of each other. The deceasing output with increasing frequency is likely due to TFT operation in a non-quasi-static regime.

Quasi-static operation assumes that, using varying terminal voltages v_X(t) (where the subscript X denotes the terminal of interest), the charge per unit area at any position in the channel at any time t' is assumed to be identical to that expected if dc voltages were used instead; i.e. $V_X = v_X$(t'). [61] Since charge in the channel is transported at a finite velocity, the net amount of charge in the channel cannot change instantaneously. For the assumption of quasi-static operation to be true, the variation of the terminal voltages must be sufficiently slow.

Defining an exact time or frequency corresponding to a breakdown of the validity of the quasi-static assumption is somewhat difficult. However, the transit time for a given transistor constitutes a good first-order estimator. The transit time is defined as the average time it takes for an electron to travel the length of the channel and can be rigorously defined as [61]

$$\tau = \frac{|Q_I|}{I_D} \tag{4.1}$$

where Q_I represents inversion layer charge in a MOSFET and can likely be replaced by the accumulated channel charge in a unipolar TFT. In terms of device performance and geometry, the transit time can be approximated as [6]

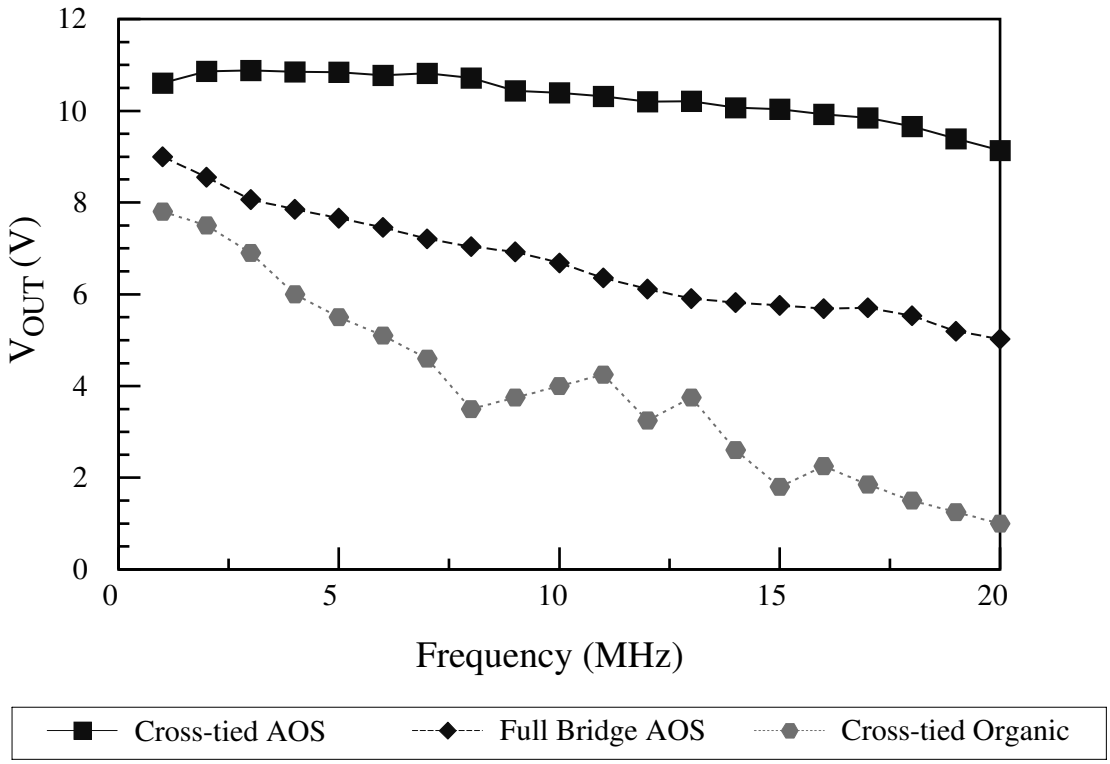


Figure 4.6: V_{OUT} versus frequency for the two configurations implemented using AOS-based TFTs (black symbols and lines) in addition to the previously reported results from a cross-tied circuit implemented with OTFTs (grey lines and symbols). The two AOS-based circuits are driven with a 20 V peak-to-peak (7.07 V_{rms}) differential sine wave with a 2 MΩ load on the output. The data for the organic circuit is reported as being normalized to a 10 V_{rms} (28.2 V peak-to-peak) differential sine wave input with a 10 MΩ output load. [56] Despite the larger input signal and load, the output voltage of the organic circuit is always less than the AOS-based circuits. The degradation of V_{OUT} with respect to frequency is observed for all three cases. However, the AOS-based circuits are less affected than the organic-based circuit.

$$\tau \cong \frac{L^2}{\mu V} \tag{4.2}$$

where L is the channel length, μ is the mobility, and V is the voltage seen by carriers in the channel. This expression is valid to the extent that the mobility is linear with respect to the electric field and also that the electric field is uniform across the channel, i.e., it is equivalent to the drain voltage divided by the channel length. This corresponds to a transistor operating in the linear portion of the pre-saturation current regime. A more thorough analysis which includes an expression for transit time in the saturation regime can be found in Tsividis. [61] Based on this transit time, the unity-gain frequency can be approximated as [6]

$$f_T = \frac{1}{2\pi\tau} \approx \frac{\mu V}{2\pi L^2}\,. \tag{4.3}$$

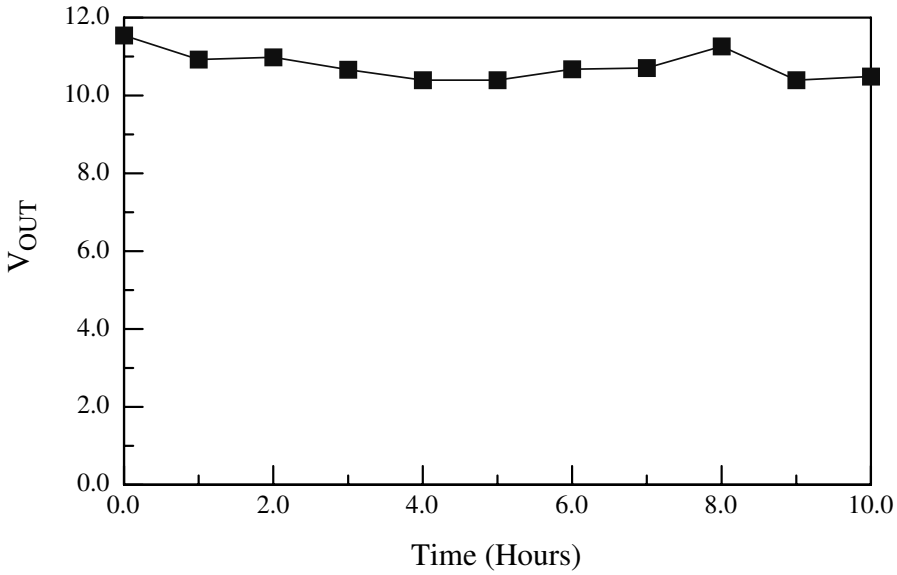


Figure 4.7: V_{OUT} versus time for a cross-tied rectifier with an input of a 20 V peak-to-peak sine wave at 1 MHz. The input signal is applied constantly for the duration of the test and the output is sampled once an hour for 10 consecutive hours. There is no clear trend towards a decrease in the output; all variation in the signal is attributed to random noise in the measurement setup.

Using a mobility of 10 $cm^2V^{-1}s^{-1}$, a voltage of 10 V, and a length of 15 μm corresponds to a unity-gain frequency of $\sim$7 MHz. This frequency estimate constitutes a best-case scenario since it only takes into account the intrinsic part of the transistor; i.e., it ignores extrinsic capacitive or resistive effects from the source and drain. As a point of reference, assume a single-crystal silicon MOSFET with a mobility of 600 $cm^2V^{-1}s^{-1}$, a 1 μm channel length, and an applied drain bias of 5 V. These parameters result in a maximum operation frequency of $\sim$48 GHz. Hence, many other factors in MOSFETs limit the frequency performance and the quasi-static assumption is almost universally appropriate. However, this is likely not the case for TFTs which employ novel channel materials for large area, low cost, or flexible electronic applications. This is especially the case when long channel lengths are involved. Thus, circuit simulation at frequencies on the order of the unity-gain frequency should be examined with suspicion. Note that Eq. 4.3 reveals that the unity gain frequency depends on the inverse of the square of the channel length. Since the AOS TFTs used in this work possess very long channel lengths (15 μm), there is substantial room for improvement with regard to the frequency performance of this technology.

Figure 4.6 further explores this frequency dependence for both circuit configurations by stepping the input frequency from 1 to 20 MHz in 1 MHz increments. The input signal is the same differential sine wave with an amplitude 20 V peak-to-peak used previously and the output of the rectifiers is loaded only with the active probes used for measurement (2 MΩ). For comparison,

the approximate output voltages from the previously published OTFT switch-tied rectifier are also plotted. [56] The OTFT circuit is also driven differentially by a sine wave, with the output voltage reported as being normalized to an input of 10 V_{rms} (which is equivalent to an amplitude of 28 V peak-to-peak) and with a load of 10 MΩ. Despite this larger input signal and load resistance, the organic-based circuit is outperformed by both configurations of the amorphous oxide semiconductor rectifiers in terms of output at a given frequency and also the amount of degradation seen with increasing frequency. The best performance is exhibited by the cross-tied AOS-based rectifier with a dc output voltage of ∼9.5 from an input of ∼7.07 V_{rms} at 20 MHz.

The long-term stability of the cross-tied rectifier under a constant input stress is illustrated in Fig. 4.7. The input is kept constant at 1 MHz with an amplitude of 20 V peak-to-peak and the output is loaded with a 10 pF smoothing capacitor for the entire duration of the experiment. The output voltage is sampled once per hour for 10 consecutive hours; there is no observable decrease in the output signal with time. The slight variation in the data shown in Fig. 4.7 is attributed to the previously mentioned inherent noise in the testing setup.

4.4 Conclusions

Two full-wave rectifying circuits based on amorphous oxide semiconductors are fabricated using standard photolithographic patterning techniques; nine primary steps, four masks, and a peak temperature of 400 °C are required for fabrication. The cross-tied rectifier exhibits an improved output compared to the bridge rectifier. Both circuits are shown to operate successfully up to 20 MHz. This is the highest reported operation frequency for a circuit based on AOS TFTs. The best performance is exhibited by the cross-tied rectifier with a dc output voltage of ∼9.5 V from an input of only ∼7.07 V_{rms} at 20 MHz, while both circuits substantially outperform previously reported OTFT-based cross-tied rectifiers. A 10 hour stability test further suggests that AOS based circuits may be an excellent contender for low megahertz frequency applications.

5. ENHANCEMENT-DEPLETION INVERTER USING AOS-BASED TFTS

This chapter is devoted to the development and implementation of an enhancement-depletion (E-D) inverter using AOS-based TFTs.

5.1 Design and Simulation

As discussed in Sec. 2.4.2, inverters implemented using AOS-based TFTs have, to date, exclusively used enhancement-mode transistors as the load. These inverters have gains of less than 2; this is adequate for oscillation to occur when configured as a ring oscillator, but is not ideal for digital logic applications. If a depletion load can be realized, the gain is expected to improve in addition to allowing the high output signal to reach the applied rail voltage, V_{DD}. Not-AND (NAND) and not-OR (NOR) logic gates can be implemented by adding another control transistor either in series or parallel, respectively, to the E-D inverter. Any other digital logic gate (such as AND, OR, and XOR) can then be created by using different combinations of the inverter, NAND, and NOR logic gates. With this toolbox of digital components, virtually any digital logic system can be realized.

One method for implementing the depletion load TFT is to utilize a different channel material than that of the control transistor. A material that seems well suited for depletion-mode applications is IZO; previously reported V_{ON} and V_T values for this material are predominantly negative. [48, 49, 50] A staggered bottom-gate TFT using IZO as the channel layer is fabricated on an Si/SiO_2 substrate for the purpose of mobility extraction and simulation, as discussed in Sec. 3.2. The channel layer and source/drain contacts are patterned using shadow masks. The device is depletion-mode with V_{ON} = -9 V and exhibits counter-clockwise hysteresis with a turn-on shift of ∼-4 V. For simulation purposes, the turn-on voltage is approximated as -11 V to account for the hysteresis.

Figure 5.1 illustrates the simulation results of an E-D inverter using this IZO depletion-mode TFT model in conjunction with an enhancement-mode TFT model (based on an IGO TFT with V_{ON} = 2 V). The depletion transistor has a width of 37.5 μm and the enhancement transistor has a width of 75 μm; both transistors have a channel length of 15 μm. V_{DD} is set to 15 V while the input voltage is swept from 0 V to 15 V. The high output voltage is equal to V_{DD}, the low output voltage is less than 2 V, and the transition between the two is centered at ∼7.5 V; the shape and location of this switching characteristic is defined by the relative sizing of the load and

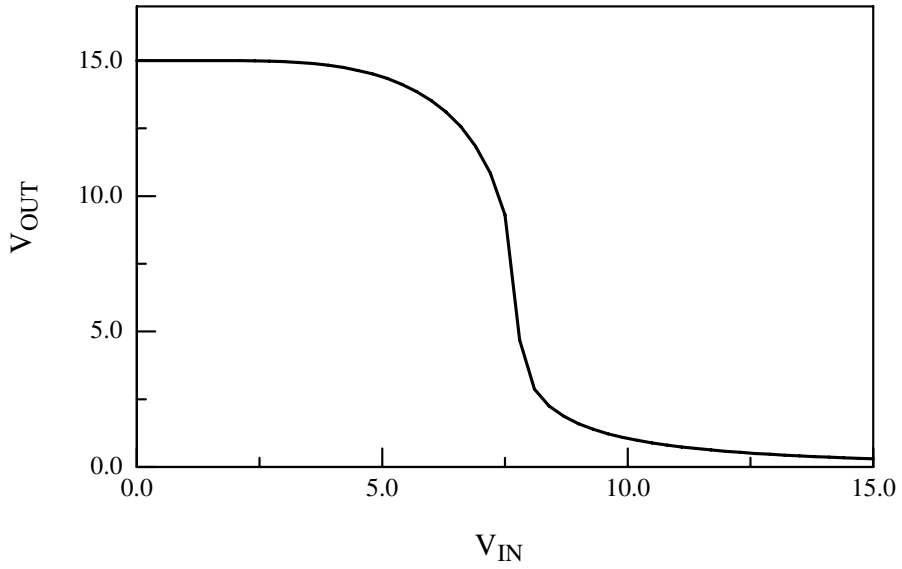


Figure 5.1: Simulated voltage transfer characteristic for an enhancement-depletion inverter, with V_{DD} = 15 V, based on models that accurately reflect the DC performance of an IZO-based depletion-mode TFT and an IGO-based enhancement-mode TFT. The simulated depletion and enhancement transistors have widths of 37.5 μm and 75 μm, respectively, and both have a channel length of 15 μm. The high output level reaches the rail voltage and the gain of this inverter is ∼15.

control transistors. The simulated gain is ∼15, making it a good candidate for use in digital logic applications.

5.2 E-D Inverter Fabrication

Fabrication of the E-D inverter is similar to the AC/DC rectifier outlined in Sec. 4.2 and begins with 25×25×1.1 mm Corning 1737 glass slides coated with ∼200 nm of ITO. Staggered bottom-gate TFTs are used for both the control and the load transistors. The inclusion of a second channel deposition increases the complexity by requiring another masking step and a second, lower temperature anneal. Due to the chemical similarities between the two channel materials, there is no etching procedure that provides a large selectivity between them. Hence, lift-off is used to pattern the channel material which is deposited second. This results in a total of 12 primary steps and 5 masks to fabricate the circuit. The layout is performed in Cadence; the mylar mask set is purchased from CAD/Art Services Inc.. The fabrication process follows:

1. Substrate cleaning: The substrates are first rinsed with 18 MΩ-cm Millipore water and then cleaned in an ultrasonic bath with a solution of Contrad70. Following the ultrasonic treatment, the samples are thoroughly rinsed with DI water and finally cleaned with acetone, isopropyl alcohol (IPA), and Millipore water sequentially and placed in a dehydration oven at ∼125 °C for at least 10 minutes.

2. Mask A: The gate electrode (ITO) is patterned using standard photolithographic techniques. The ITO is etched using ∼12 M hydrochloric acid (HCl) for 5 minutes. A digital multimeter is used to verify that the substrate is no longer conductive, indicating that the ITO is completely etched.

3. Insulator deposition: ∼100 nm of silicon dioxide is deposited using the PECVD reactor at Oregon State University using silane and nitrous oxide precursors. The deposition pressure, silane flow, nitrous flow, temperature, and rf power are ∼250 mTorr, 75 sccm of a 2% silane/98% He gas mixture, 100 sccm of N_2O, 400 °C, and 250 W, respectively.

4. Control TFT channel deposition: IGO is deposited via rf magnetron sputtering from a circular 2 inch diameter target with a 1:1 molar ratio of In_2O_3:Ga_2O_3 (purchased from Cerac, Inc.) using a power density, argon/oxygen ratio, total flow rate, deposition pressure, and deposition time of 23.8 W/cm^2, 94/6, 42.7 sccm, 5 mTorr, and 10 minutes, respectively. Slightly more oxygen is used than during the fabrication of the AC/DC rectifiers in an effort to maintain a positive or near- zero turn-on voltage. The control transistor channel is deposited first in an effort to minimize hysteresis or mobility degradation that may be introduced by exposing the semiconductor/insulator interface to photoresist or other processing steps.

5. Mask B: The control TFT channel layer is patterned using standard photolithographic techniques and etched in a ∼2.4 M HCL solution for 80 seconds.

6. IGO channel anneal: The substrate stack (gate, insulator, and IGO channel) is annealed in a box furnace. The thermal cycle begins at room temperature (∼22 °C) and increases at a rate of 2 °C/minute until the peak temperature of 400 °C is reached. The substrate is held at the peak temperature for 1 hour and then passively cooled to room temperature at ∼2 °C/minute.

7. Mask C: Photoresist is deposited and patterned for lift-off of the depletion-mode channel.

8. Depletion-mode channel deposition: IZO is deposited via rf magnetron sputtering from a circular 2 inch diameter target with a 1:1 molar ratio of In_2O_3:ZnO (purchased from Cerac, Inc.) using a power density, argon/oxygen ratio, total flow rate, deposition pressure, and deposition time of 15.9 W/cm^2, 89/11, 45 sccm, 5 mTorr, and 15 minutes, respectively. The samples are soaked in acetone for 1 hour after the channel deposition, followed by a brief (∼15 second) sonication in the acetone solution to perform the lift-off.

9. Mask D: Vias are opened in the dielectric by etching with a buffered hydrofluoric (HF) acid solution for 45 seconds.

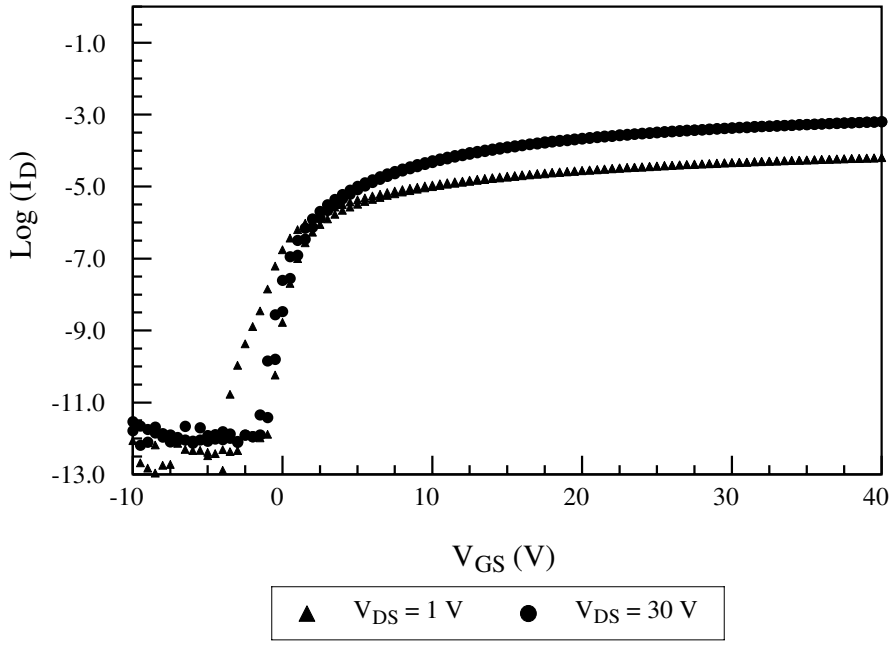


Figure 5.2: Log(I_D)-V_{GS} transfer curves with V_{DS} = 1 V (triangles) and V_{DS} = 30 V (circles) for a staggered bottom-gate IGO TFT fabricated using the full integration process detailed in Sec. 5.2. The turn-on voltage is ∼-1 V, V_T is ∼1.4 V, peak incremental and average mobilities are ∼5 $cm^2V^{-1}s^{-1}$ and ∼4.5 $cm^2V^{-1}s^{-1}$, respectively, and a drain current on-to-off ratio of 1×10^8 is observed. These transfer curves are similar to those previously reported for an IGO TFT fabricated on thermally oxidized silicon using shadow masks to pattern the channel and source/drain layers, as illustrated in Fig. 4.3.

10. IZO channel anneal: The entire TFT stack (gate, insulator, and both channels) is annealed in a box furnace using the same ramp rate and dwell times as step 6 with a lower peak temperature of 200 °C. Since this temperature is substantially less than the first anneal, it is thought to have little effect on the previously annealed materials. This anneal is intentionally performed after the insulator etch to help devolve any hydrogen ions that may have been introduced in the insulator because of the exposure to HF.

11. Mask E: Photoresist is deposited and patterned for the lift-off of the source/drain contacts.

12. Source/drain metal deposition: Aluminum is thermally evaporated to a thickness of ∼500 nm. Samples are soaked in acetone for 1 hour followed by a brief (∼15 seconds) sonication in the acetone solution to selectively remove unwanted aluminum via lift-off.

5.3 Electrical Characterization and Discussion

Figure 5.2 illustrates the log(I_D)-V_{GS} transfer curve with V_{DS} = 1 V (triangles) and V_{DS} = 30 V (circles) for a staggered bottom-gate IGO TFT fabricated using the complete integrated

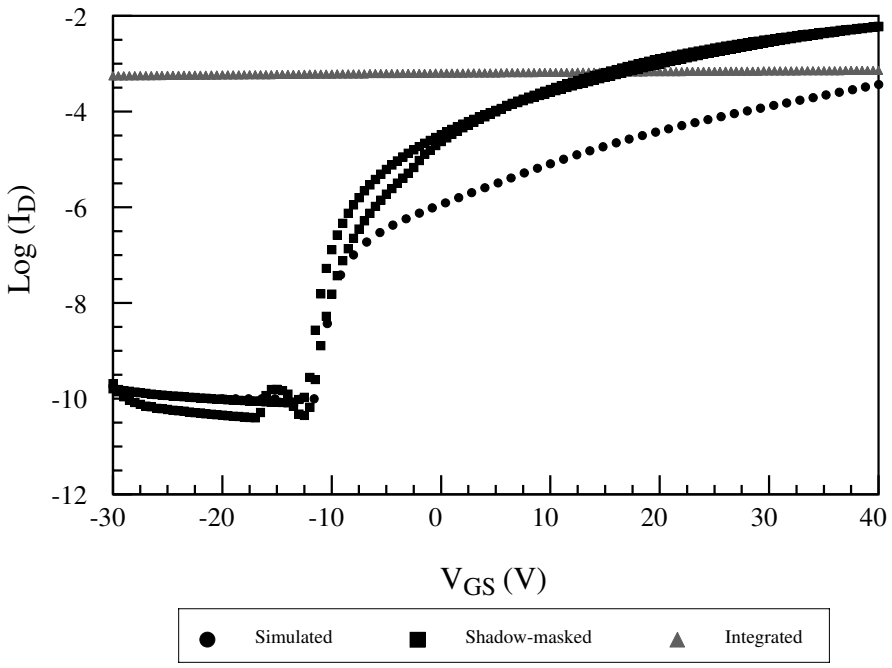


Figure 5.3: Log(I_D)-V_{GS} transfer curves with V_{DS} = 30 V for the simulated IZO-based TFT (black circles) and experimental data from an IZO-based TFT fabricated on a thermally oxidized silicon substrate and patterned using shadow masking (black squares). The two devices have virtually identical turn-on voltages of ∼-12 V, with the fabricated device demonstrating improved current drive. The log(I_D)-V_{GS} transfer curve with V_{DS} = 1 V of an integrated IZO-based TFT, processed using the same deposition and anneal parameters as the shadow-masked device, is also illustrated (grey triangles). This device exhibits no gate modulation and high levels of current; the integrated IZO TFT is effectively a conductor. With V_{DS} = 30 V, the amount of current flow in the integrated device exceeds the set compliance limit of 20 mA.

process flow previously described in Sec. 5.2. This device has a slightly negative V_{ON} of ∼-1 V, a threshold voltage of ∼1.4 V, ∼3 V of clockwise hysteresis with V_{DS} = 1V, a drain current on-to-off ratio of 1×10^8, and peak incremental and average mobilities of ∼5 $cm^2V^{-1}s^{-1}$ and ∼4.5 $cm^2V^{-1}s^{-1}$, respectively. The mobility of the integrated TFT is comparable to what has been previously reported by Presley *et al.* [46], as discussed in Sec. 4.3, while the drain current on-to-off ratio is improved due to a lower off-current. Of particular interest is comparison to the transfer curve previously presented in Fig. 4.3. The two IGO TFTs are sputtered in nearly identical conditions and exhibit similar turn-on voltages, despite differences in patterning techniques and physical dimensions.

Figure 5.3 illustrates three transfer curves corresponding to three different IZO TFTs. Black circles represent the transfer curve of the simulated TFT with V_{DS} = 30 V, black squares correspond to measured data from a shadow-masked device fabricated on thermally grown silicon dioxide using the sputtering parameters described in step 8 of the fabrication process and subjected to a 200 °C post-deposition anneal with V_{DS} = 30 V, and grey squares correspond to IZO

TFTs fabricated with the complete integration process with V_{DS} = 1 V (currents greater than the compliance limit of 20 mA flow when a bias of 30 V is applied). The simulated IZO TFT and shadow-masked device have a nearly identical turn-on voltage of ∼-12 V, resulting in depletion-mode operation as desired. The fully integrated device, however, shows no gate modulation and drain current in the milliampere range; it is effectively a conductor. The effect this has on the inverter VTC is shown in Fig. 5.4. Little voltage is dropped across the load, even for large input values up to 40 V, resulting in an always high output state. The small voltage drop observed at high input voltages is attributed to ohmic losses across the IZO device.

In order to explore this discrepancy between the shadow-masked and fully integrated devices, staggered bottom-gate IZO TFTs are fabricated on 25×25 mm thermally oxidized silicon substrates; the resulting device stack is equivalent to the shadow-masked TFTs. The channel layer is photolithographically patterned using both lift-off and etching (using masks C and B, respectively) while the source-drain contacts are formed by lift-off of thermally evaporated aluminum. In both cases, the resulting IZO devices demonstrate similar behavior to the fully integrated devices; i.e., the IZO always behaves as a conductor. This suggests that the disconnect in performance is arising either from exposure of the channel material to the chemicals and processes necessary to perform the photolithographic patterning and lift-off or because of a difference in the absolute dimensions of the active area. It is unlikely that reducing the device dimensions is responsible for this change in performance. While there are several reports in the literature of discrete IZO TFTs being successfully fabricated using lift-off to pattern the channel [48, 49, 50], this does not rule out the potential for a disconnect in performance between shadow masked and integrated TFTs. Hence, the disconnect is tentatively attributed to an undetermined processing issue.

Several experimental variables are modified in an effort to restore transistor operation to the IZO TFTs. Samples are again fabricated on 25×25 mm thermally oxidized silicon substrates using lift-off to pattern the channel and source/drain contacts, since this process appears correlate to the completely integrated devices. The amount of oxygen present during the channel deposition is increased in an effort to decrease the carrier concentration of the film; the Ar/O_2 ratio is changed from ∼89/11 to ∼85/15 while maintaining a processing pressure of 5 mTorr. The thickness of the IZO film is decreased by shortening the deposition time by ∼33% to reduce the absolute number of carriers in the channel, thus making it easier to deplete the channel and turn the device off. The anneal temperature is also decreased by 25%. All of these changes have been shown to decrease mobility and increase V_{ON} in AOS-based TFTs, as described in Sec. 2.3. These variables are modified independently and also in combination with each other; regardless of the parameters used the resulting IZO-based devices exhibit no field-effect.

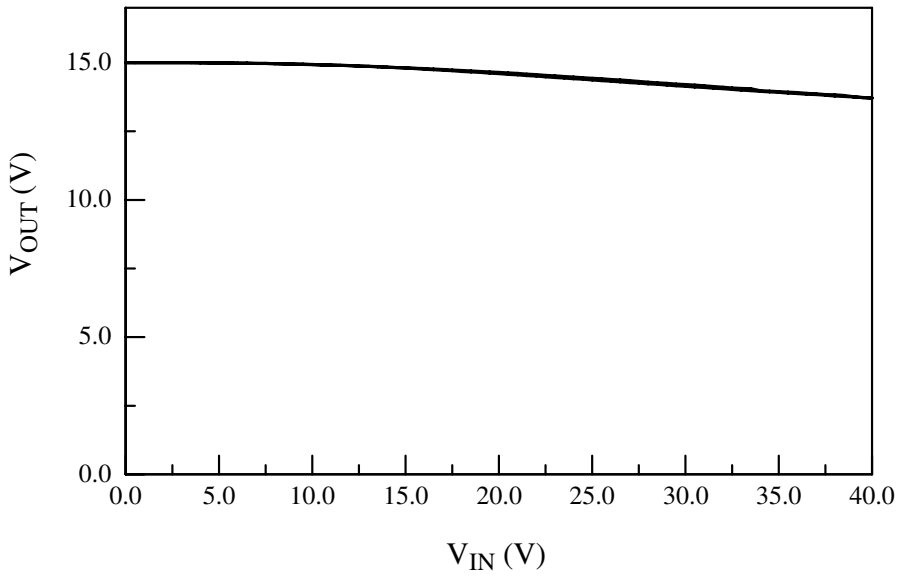


Figure 5.4: Measured voltage transfer characteristic with V_{DD} = 30 V for the fully integrated E-D inverter. Due to the conductive nature of the integrated IZO transistor, negligible voltage is dropped across the load.

Attempts to realize a depletion-mode IGO-based TFT with performance in line with the simulated depletion-mode TFT are also undertaken. The oxygen partial pressure during deposition is decreased, the channel thickness is increased, and two post-deposition anneal temperatures are utilized: 200 °C and 400 °C. The annealing temperature is found to be the dominant variable in controlling V_{ON}; devices annealed at 200 °C exhibit a turn-on voltage that ranges from 4-12V while devices exposed to a 400 °C anneal consistently exhibit a turn-on voltage of ∼-1 V. It is expected that a depletion mode IGO TFT can be realized with higher anneal temperatures, however the thermal ceiling of this process is limited to 400 °C by the anneal of the control transistor.

5.4 Conclusion and Recommendations for Future Work

An E-D inverter is simulated using drain current-voltage models for IZO- and IGO-based TFTs. The resulting gain of ∼15 is an improvement over current reports of AOS-based inverters in the literature, which are limited to gains less than 2. Large gains are preferred for digital logic applications because the noise margins for high and low input signals are increased and smaller changes in the input voltage can be used to change the output state. The deposition parameters for the two channel materials, in addition to the post-deposition anneals, are optimized on thermally oxidized silicon substrates using shadow masks to pattern the channel and source/drain layers; transfer curves that closely match those of the simulated transistors are obtained in both cases. The IGO-based control transistor is successfully integrated, resulting in a V_{ON} of ∼-1 V, a threshold

voltage of ∼1.4 V, and an average mobility of ∼4.5 $cm^2V^{-1}s^{-1}$. An integrated depletion-mode TFT load was unable to be realized in the present work; integrated IZO TFTs are found to be highly conductive between the source and drain terminals with no gate modulation of the current. Due to the conductive nature of the load, little voltage is dropped across the load and the inverter shows no significant output voltage variation. The cause for the discrepancy between the behavior of the shadow-masked and photolithographically patterned IZO TFTs is attributed to an unknown processing issue. There is little change in performance between shadow masked and photolithographically patterned IGO-based TFTs.

The benefits of the E-D inverter warrant further investigation of the integration of a depletion load. It should be possible to successfully fabricate a depletion-mode transistor patterned via lift-off by re-optimize the deposition parameters and annealing conditions for IZO based TFTs using the mask set and a partial integration process on Si/SiO_2 substrates. However, little work has been reported on the stability of IZO-based TFTs and this material may ultimately be a poor choice for integrated circuits.

A second option is to utilize a single channel material (such as IGO, IGZO, or ZTO) with two depositions and anneals. Since the depletion load likely requires a higher anneal temperature, it needs to be deposited and annealed first. This may negatively affect the semiconductor/insulator interface of the control transistor. If localized annealing is possible, a variation on this idea is to perform a single channel material deposition and anneal the control and load transistors to different extents in order to control the turn-on voltage, thus maintaining a pristine interface for both transistors.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

The primary focus of this thesis is investigation and fabrication of amorphous oxide semiconductors in circuit applications. Prior to the work reported herein, the only integrated circuits reported using AOS-based TFTs have been inverters implemented with enhancement-mode TFT loads, ring oscillators, and a simple pixel driving circuit. The maximum operating frequencies for these circuits has yet to exceed a megahertz, leading to questions regarding the applicability of these materials for high-frequency applications.

The fabrication procedure and electrical characterization for two AC/DC rectifiers implemented with amorphous oxide semiconductors are presented herein. Staggered bottom-gate TFTs using indium gallium oxide as the channel layer are successfully integrated using traditional photolithographic and etching techniques. The cross-tied configuration is found to provide an improved output swing compared to the traditional bridge configuration implemented with diode-tied transistors. Both the cross-tied and bridge rectifiers demonstrate an excellent DC output voltage response of ∼10.5 V and 9 V, respectively, at 1 MHz with a 7.07 V_{rms} input. The output voltage decreases with decreasing load impedance, as expected, and also decreases with increasing input frequency. At 20 MHz, the limit of the signal generation capability, both circuits still exhibit very usable output voltages greater than 5 V. These results are superior to what has previously been reported for organic p-type TFTs in an analogous cross-tied configuration. [56]

The simulation, fabrication procedure, and electrical characterization for an E-D inverter based on heterogeneous channel materials is also presented. The simulation is performed using models based on depletion-mode IZO-based and enhancement-mode IGO-based TFTs and demonstrates a gain of ∼15. Previous reports of enhancement-enhancement inverters based on oxide semiconductors have been limited to gains of less than 2. Processing of the channel materials is optimized by fabricating TFTs on thermally oxidized silicon substrates using shadow masking; the resulting IGO-based and IZO-based TFTs both demonstrate comparable performance to the models used for simulation. The inclusion of a second channel layer material increases the complexity of the process by requiring additional deposition, masking, and annealing steps. Integrated IGO TFTs are found to perform similarly to shadow-masked TFTs. Integrated IZO-based TFTs are found to be conductive and to exhibit no gate modulation. Due to the conductive nature of the load, the fabricated E-D inverter shows no significant output voltage variation. This disconnect

in performance between integrated IZO-based TFTs and those patterned via shadow masking is attributed to an undetermined processing issue.

6.2 Recommendations for Future Work

While there have been several reports of amorphous oxide semiconductors in circuit applications, there are still a multitude of unanswered questions. The results of this work suggest two directions for future exploration; high speed characterization and process integration. The frequency dependence of the output voltage from the rectifying circuits observed in this work suggests that the transit time may play an important role in determining the actual performance and limitations on simulating amorphous oxide semiconductors in high-speed applications. While this frequency dependency is attributed to TFT operation in a non-quasistatic mode, this assumption needs to be verified and implications of non-quasistatic operation need to be further investigated.

Secondly, many integration issues need to be addressed in order to expand the potential application space of AOS-based electronics. All of the current reports of successfully integrated oxide-based circuits are implemented using IGO or IGZO as the channel layer. As evidenced here, the integration of other materials may not be as straightforward. More work needs to be done to explore the disconnect in device performance observed herein and also to incorporate a wider variety of materials (including different contacts, insulators, and semiconductors) into AOS-based circuits. One channel material of particular interest that has yet to be integrated into a circuit application is zinc tin oxide. This material has two substantial benefits over the indium- and gallium-based films; the raw material cost is much lower and ZTO can be reactively sputtered from a metal target. However, the robust nature of ZTO requires a reactive ion etch, making it more difficult to work with and integrate.

Once the integration challenges of implementing a depletion-mode TFT are overcome, either through the use of a different material or by changes in the process flow, the E-D inverter, NAND, and NOR logic gates should be revisited. These fundamental building blocks provide a path towards more sophisticated digital circuits and should greatly expand the potential application space for amorphous oxide semiconductors.

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