AN ABSTRACT OF THE THESIS OF

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David J. Allstot

A high-swing, high-linearity Class-AB CMOS operational amplifier suitable for high speed application is presented. It does not exhibit large-signal slewing effects as do others; its output current is limited by MOSFET aspect ratios and the total power supply voltage. A rail-to-rail common-mode input range is achieved by a topology which has two parallel-connected complementary input pairs. The DC bias and AC small-signal currents are summed so that the small-signal gain is constant over the full common-mode voltage range.

A High-Swing
Class-AB CMOS Operational Amplifier

by

Choung Yu

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Professor of Electrical & Computer Engineering
in charge of major

Redacted for privacy

Head of Department of Electrical & Computer Engineering

Redacted for privacy

Dean of Graduate School

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A High-Swing Class-AB CMOS Operational Amplifier

I. INTRODUCTION

In analog CMOS sample/hold applications, fast slewing operational amplifiers are often required for driving large capacitive loads. This is especially true when using correlated double-sampling techniques wherein the amplifier is periodically reset at a high frequency using a unity-gain configuration in order to sample the low-frequency noise and DC offset voltages onto a capacitor whereby the effects of these errors are subsequently removed [1]-[2].

The need for high speed suggests the use of a CMOS class-AB operational amplifier since it does not exhibit large-signal slew-rate limiting in the classical sense [3]-[5]. As a consequence of the continued scaling of CMOS VLSI technologies, the power supply voltage is being reduced from 10 volts to 5 volts and perhaps eventually 3.3 volts [6], which means the analog circuits must now operate over a much higher percentage of the available power supply voltage in order to maintain a given output voltage level.

A circuit topology for high-swing, high-linearity class-AB CMOS operational amplifiers has been developed.

The technique [7] uses complementary parallel-connected input pairs with appropriate DC bias/level shifting circuitry to obtain an input common-mode voltage range that equals or exceeds the output linear range, and is nearly equal to the total power supply voltage.

The circuit configuration is based on three main concepts. The first is a differential class-AB structure which does not exhibit slewing effects, and results in a fast settling time. Second, a parallel-connected topology is used to give high common-mode input range and high linearity. Third, an adaptively-biased output stage is used to guarantee full current driving capability to the load while maintaining the maximum possible output voltage. These features will be discussed in detail in section II. In section III, AC and transient analysis will be given. Some limitations will be discussed in section IV and the circuit realization is given in section V.

II. CIRCUIT DESCRIPTION

A. A Basic class-AB differential amplifier

The term class-AB is taken to mean a circuit which can deliver to and source from a load, a current that is larger than the DC quiescent current.

A simplified differential-input CMOS class-AB operational amplifier circuit is shown in Fig. 1. With both inputs grounded, the quiescent currents in the input transistors are determined by the bias voltages V_1 and V_2. Upon the application of a positive differential input voltage, the gate-to-source voltages of both M1 and M5 increase while those of M2 and M4 decrease from their quiescent values. The small-signal current increases in the M1-M5 branch and decreases in the M2 - M4 branch as in a conventional differential-input amplifier. For a large differential input signal, current in one of the branches will be cut off while current in the other increases monotonically. The amount of current can be much greater than that in the quiescent state, and is limited by MOSFET aspect ratios and the total power supply voltage. Transistors pairs M3 - M7 and M6 - M10 form simple current mirrors that reflect the input currents to the output stage.

Finally, a cascode structure M7 - M10 is used to provide high output resistance and thus offer high voltage gain.

A single-stage configuration is particularly suitable for class-AB operation. Thus, there are no high-frequency second-stage noise components, which would greatly reduce the dynamic range of the sampled-data system due to aliasing effects. Also, there is no need for extra compensation components, since for typical applications, the load capacitance is sufficient to guarantee a stable closed-loop response.

By taking advantage of the large current available in the output, the circuit does not obey the normal relationships between slew rate and input stage transconductance, input-stage bias current, and unity-gain bandwidth as in the cases of the two-stage and folded cascode op-amps. In fact, the circuit does not display slew-rate limiting at all and a fast settling time is therefore expected. For a given speed, a savings in the quiescent power dissipation can usually be achieved.

B. Solution for high dynamic range

1) The limiting factors of dynamic range

A general purpose operational amplifier is typically used in the configuration of either an inverting single-ended gain stage or a non-inverting unity-gain voltage follower. Therefore, in order to provide a high overall dynamic range of operation, the amplifier must exhibit both a large output voltage swing, and a large common-mode input voltage range.

The linear relation $V_o = A (V^+ - V^-)$ between the output and input voltages is valid only for a limited range of V_o. For a CMOS operational amplifier with a cascoded output stage, the output swing is usually to within two saturation voltages (typically 0.5 volts) of either power supply.

For a unity-gain voltage-follower connection (V^- and V_o shorted together and V_{in} connected to V^+), the relation between V_{ic} and V_{in} is given by

$$V_o = V_{in} [A/(1+A)] = V^- \quad (1)$$

$$V+ = Vin \quad (2)$$

$$V_{ic} = \frac{V^+ + V^-}{2} = \frac{V_{in} [1 + A/(1+A)]}{2} \simeq V_{in} \quad (3)$$

; For A >> 1

Since all devices must remain in saturation to achieve high gain over the common-mode input range, the limitation of input voltage range also limits the dynamic range of the circuit.

For the basic CMOS class-AB amplifier shown in Fig. 1, the maximum value of the common mode input allowed to keep all devices in saturation is given by

$$V_{in(max)} + V_1 - V_{GS5} = V_{DD} - V_{SG6} - V_{DSAT5} \quad (4)$$

$$V_{in(max)} = V_{DD} - (V_T + 2|V_{DSAT}|) \quad (\text{for } V_1 = V_{GS5}) \quad (5)$$

and the minimum value is given by

$$V_{in(min)} - V_2 + V_{SG4} = V_{SS} + V_{GS3} + {}^{\circ}V_{DSAT4}{}^{\circ} \quad (6)$$

$$V_{in(min)} = V_{SS} + (V_T + 2|V_{DSAT}|) \quad (\text{for } V_2 = V_{SG4}) \quad (7)$$

Thus, the input common-mode voltage range is to within only one threshold voltage plus two saturation voltages (typically 1.25 volts) of either power supply. Thus, the linear voltage range in a unity-gain configuration is limited by the input common-mode range rather than by the voltage swing of cascode output stage.

2) A circuit topology for high swing

To increase the common-mode range, note from Fig. 2 that by level-shifting the inputs by one threshold voltage plus one saturation voltage (the voltage for all batteries) in the positive direction, the input common-mode range is identically shifted to within one saturation voltage (about 0.25 volts) of the positive power supply but about 2.5 volts above the negative supply. Similarly, by level-shifting the inputs by one threshold voltage plus one saturation voltage in the negative direction as shown in Fig. 3, the input common-mode range is also identically shifted to within one saturation voltage of the negative supply but about 2.5 volts below the positive supply voltage. By parallel-connecting the complementary input stages of Figs. 2 and Fig. 3, and sharing the output stage as shown in Fig. 4(a), the DC bias and AC small-signal currents are summed and the circuit exhibits nearly rail-to-rail input common-mode range (Fig 4(b). The input DC bias and level shift circuitry are shown in Fig. 5.

3) High linearity

In addition to providing wide input common-mode range, the circuit of Fig. 4 also exhibits very high

gain linearity over the entire input common-mode voltage range. This important feature is explained as follows: When both input pairs are active, the transconductance is twice what it is if only a single stage is active because of the parallel connection. However, the DC bias current of the output stage is also controlled by current mirrors associated with the input stages. As shown in Fig. 6, if both input stages are active, approximately twice as much bias current flows through the output stage as when only one stage is active. Therefore, the output conductance is increased by a factor of approximately two when both stages are active. Hence, to a first-order, the small-signal voltage gain, g_m/g_{out}, is nearly constant over the entire common-mode range as shown in Fig. 7.

C. Adaptively-biased output stage

From Fig. 1, note that in order to obtain the maximum small-signal voltage gain of the circuit, it is necessary to insure that M7 - M10 are in saturation. To obtain a large output swing, V_{B1} and V_{B2} must be as small as possible. The minimum possible voltage that guarantees proper operation of the circuit in the quiescent state is one threshold voltage and two saturation voltages from the corresponding power supply,

$$V_{BIAS} = V_{B2} - V_{SS} = V_{GS8} + V_{DSAT7} = V_T + 2V_{DSAT} \quad (8)$$

Consider operation during transient when the peak current may reach an amount K^2 times greater than what it is in the quiescent condition. Thus, a minimum V_{BIAS} under this transient condition is given by

$$V_{BIAS} = V_{GS8} + V_{DSAT7} = V_T + 2KV_{DSAT} \quad (9)$$

where K is a constant. Thus, a fixed-bias cascode current mirror cannot deliver the peak current during the transient while maintaining a large output swing. That brings a need for an adaptively-biased output stage which can always maintain the maximum output swing.

The idea of an adaptively biased output stage is shown in Fig. 8. Input current is sensed by M15 and V_{BIAS} is given by V_{GS43} where M3, M15 and M19, M20 are one-to-one simple current mirrors. The relationship between the input current and V_{GS43} is given by

$$V_{GS43} = V_T + 2\ (\ 2I_B/\beta\ )^{\frac{1}{2}} \quad (10)$$

where β is given by K'_n x (W/L). Thus, V_{BIAS} is just the minimum voltage required for giving high swing in the quiescent state and is varied during the transient to simultaneously obtain optimum swing and full current drive capability by always maintaining M7 - M8 in

saturation. The comparison between the current transfer curves of the adaptive-bias and fixed-bias current mirrors is shown in Fig. 9.

Note further that when compared with another adaptively-biased output stage [4], this circuit can provide more peak current by sensing the input current directly rather than by adding another diode-connected transistor in the input branch to mirror current to the output. In practice, the input current is not only limited by aspect ratio and power supply range, but also by the voltage drop in the sensing branch. From Fig. 10, as the input current increases with a positive applied voltage, the voltages required to keep M6, M5, and M1 in saturation are also increased until they reach the power supply range at which point the devices enter the linear region of operation. It is apparent that the peak current will be further limited by adding a diode-connected transistor between M1 and V_{SS}.

III. CIRCUIT ANALYSIS

A. AC analysis

1) Effective input transconductance

The transconductance of a single device is given by

$$gm = (2\beta I_B)^{\frac{1}{2}} \tag{11}$$

where I_B is the bias current and β is the transistor gain factor given by K' x (W/L).

To derive the effective transconductance of a complementary series-connected pair ($g_{ms(eff)}$), from Fig. 1, one can apply a small-signal voltage (ΔV_{in}) to V_{in}^+ with V_{in}^- grounded and measure the output current in the output terminal. The source voltages of M1 - M5 and M2 - M4 are given by

$$V(8) = \frac{g_{mn}\Delta V_{in}}{g_{mn} + g_{mp}} \tag{12a}$$

$$V(7) = \frac{g_{mp}\Delta V_{in}}{g_{mn} + g_{mp}} \tag{12b}$$

where g_{mn} is the transconductance of the NMOS and g_{mp} is the transconductance of the PMOS given by (11). Thus,

the small-signal currents induced in both branches have opposite directions and identical values of $(g_{mn}g_{mp}\Delta V_{in}/g_{mn}+g_{mp})$. Both of the currents will be mirrored into the output branch by the complementary current mirror pairs. The total output current to the output load will be given by

$$I_{out} = \frac{2g_{mn}g_{mp}}{g_{mn} + g_{mp}}\Delta V_{in} \tag{13}$$

Thus, the effective transconductance of the input stage is given by

$$g_{ms(eff)} = \frac{2g_{mn}g_{mp}}{g_{mn} + g_{mp}} \tag{14}$$

Since the complementary pairs are parallel-connected, the total effective transconductance, gm(eff), of the class-AB input stage is just the sum of the two stages.

$$g_{m(eff)} = 2g_{ms(eff)} = \frac{4g_{mn}g_{mp}}{g_{mn} + g_{mp}} \tag{15a}$$

For $g_{mn} = g_{mp} = g_m$, equation (14) reduces to

$$g_{m(eff)} = 2g_m \tag{15b}$$

2) Small-signal low-frequency open-loop voltage gain

Following the same argument as above, the output voltage introduced by a small-signal input voltage is given by

$$\Delta V_o = I_{out}/g_{out} = \Delta V_{in}(g_{m(eff)}/g_{out}) \qquad (16)$$

Thus, the small-signal low-frequency open-loop voltage gain is the same as that of the basic cascode amplifier,

$$A_0 = \frac{g_{m(eff)}}{g_{ds10}\,(\,g_{ds9}/g_{m9}\,) + g_{ds7}\,(\,g_{ds8}/g_{m8}\,)} \qquad (17)$$

The open-loop frequency response with a load capacitance of 10 pF is shown in Fig. 11.

3) Unity-gain frequency and compensation

The open-loop magnitude response of a general one-stage topology is given by

$$|A(jw)| = \frac{A_0}{[\,1 + (\,w/w_d\,)^2\,]^{\frac{1}{2}}} \qquad (18)$$

where w_d is the dominant pole given by g_{out}/C_{out}. To find the unity-gain frequency, we let $|A(jw)| = 1$ and $w = w_u$. Thus, $A_0 = [\,1 + (\,w_u/w_d\,)^2\,]^{\frac{1}{2}}$

and $w_u = A_0 w_d$; For $(\,w_u/w_d\,) >> 1$

$$= \frac{g_{m(eff)}}{g_{out}} \times \frac{g_{out}}{C_{out}} = \frac{g_{m(eff)}}{C_{out}} \qquad (19)$$

Note that the dominant pole is located at the output node for this one-stage amplifier and the load capacitor acts as a compensation capacitance. For a given phase and gain margin, we can relate w_u and w_2 (the important nondominant pole) and choose $g_{m(eff)}$ and C_{out} to meet the desired specifications. In contrast to the two-stage op-amp, an increase in load capacitance actually improves the phase margin rather than degrading it.

B. Large signal transient analysis

One of the advantages of using a class-AB op-amp is that it does not exhibit a large-signal slewing effect as compared with a typical class-A op-amp. To explain this further, start by observing the large-signal behavior of a folded-cascode op-amp (Fig. 12) in a unity-gain feedback configuration. When a large positive voltage step is applied, M2 conducts more current and M1 cuts off. The total current conducted by M2 is 2I. Since M1 and M2 are connected to the current sources, the currents in M8 and M10, which charge C_{load}, are also 2I. Note that the charging current will remain

constant and is independent of the applied voltage. The output voltage thus has a nearly linear rate of increase limited by I which is called slew rate. Since the charging current is limited by the DC bias current, the total settling time is greatly degraded which is not desirable in high-speed applications.

A class-AB op-amp does not have any fixed current source to limit the transient current. The transfer function is thus just like an ideal one-stage amplifier and is given by

$$\frac{v_o}{v_{in}}(s) = \frac{a_0}{1 + s\tau} \qquad (20)$$

where τ is $(1/w_u)$. The time response is

$$v_o = v_{in} \{ 1 - \exp[- (t/\tau)]\} \qquad (21)$$

Thus, the output voltage will increase as an exponential function of time, and the settling time is greatly reduced. The SPICE transient analyses of a class-AB amplifier and a folded-cascode amplifier are shown in Fig. 13 (with the same amount of DC bias current and identical voltage steps). The input step voltages are 1, 2 and 4 volts, respectively. The time scale is in ns for the class-AB op-amp and in μs for the folded-cascode op-amp. The load capacitance is 10 pF for each amplifier.

IV. DISCUSSION

A. Lambda effect

It can be seen from Fig. 10. that if the common-source voltage moves up and down, the resulting channel-length modulations of M1 and M5 will tend to compensate each other. In fact, the circuit will not exhibit channel-length modulation at all if the transistor gain factors are chosen to satisfy [8]

$$\frac{\beta_n}{\beta_p} = \left(\frac{\lambda_n}{\lambda_p}\right)^2 \qquad (22)$$

However, as can be noted from Fig. 6, the lambda effect is significant only when one stage is active. As shown in Fig. 7, it does not greatly affect the gain linearity.

In addition to increasing the channel lengths of the transistors, a possible improvement to the lambda effect is to add a transistor between M1 and V_{SS} to reduce the voltage drop on M1. Unfortunately, the allowable transient current will be reduced by doing so.

B. Body effect

As can be seen in Fig. 4, the voltage required for the CMOS pair to conduct current is at least one threshold voltage for the NMOS and one threshold voltage for the PMOS. The NMOS threshold voltage is given by

$$V_T = V_{TO} + \gamma [(V_{SB} + 2\phi) ^{\frac{1}{2}} - (2\phi) ^{\frac{1}{2}}] \qquad (23)$$

For a large γ , V_T will increase and decrease the overlapping region of conduction. Under the worst case, if both p-well and substrate are connected to the power supplies, the source-to-bulk voltages are maximum, and the two conducting regions may not overlap, which degrades the voltage gain and the linearity around zero bias. A large γ and V_T also make the requirement of reducing the power supply to $\pm$ 2.5 unrealizable.

C. Noise considerations

Noise represents a fundamental limitation of the performance of MOS op-amps. Rules of thumb for reducing the input referred noise are to make the input devices as large as possible and the input structure as simple as possible.

There are 16 transistors (8 transistors) in the

input stage of a high-swing (conventional) class-AB op-amp. The input structure of a class-AB is also much more complicated than the classical source-coupled pair. However, by a close examination (appendix A), the equivalent input-referred noise for a conventional (one input-stage) is given by

$$V_{eq} = \left[\left(V_{n(ipp)}^2 + V_{n(ipn)}^2\right) + \left(V_{n(csp)}^2 + V_{n(csn)}^2\right) + 2\left(V_{n(opp)}^2 + V_{n(opn)}^2\right)\right]^{\frac{1}{2}} \quad (24a)$$

and for a high-swing (two input-stage) as

$$V_{eq} = \left[\frac{1}{2}\left(V_{n(ipp)}^2 + V_{n(ipn)}^2\right) + \frac{1}{2}\left(V_{n(csp)}^2 + V_{n(csn)}^2\right) + 2\left(V_{n(opp)}^2 + V_{n(opn)}^2\right)\right]^{\frac{1}{2}} \quad (24b)$$

which is comparable with a simple source-coupled pair. The SPICE simulation result is shown in Fig. 14.

V. CIRCUIT REALIZATION

Fig. 15. shows the complete schematic of the amplifier. All V_{DSAT} voltages have been set equal to simplify the design. Bias currents are supplied off-chip into two simple current mirrors. The bias current ratios between the level-shifting transistors, input transistors and transistors in the output stage are 5:20:40 to minimize the total power consumption and to give a desirable unity-gain bandwidth. The n-wells are connected to the respective PMOS sources and the NMOS substrates are connected to V_{SS}. The channel length is 10 μm for all NMOS devices and 6 μm for all PMOS devices to reduce the lambda effect. The SPICE parameters and programs are listed in Appendix B and C, respectively.

This circuit was laid out using 3 μm CMOS technology (Fig. 16) and will be fabricated by MOSIS[1].

1. MOSIS is MOS Implementation Service which is an organization that provides university communities with IC fabrication services.

VI. CONCLUSION

A high performance class-AB CMOS operational amplifier which exhibits significant improvements in linearity and drive capability was achieved. SPICE was used to analyze the DC, AC and transient performances. The amplifier specifications are listed in appendix D. It was designed using a 3 um n-well CMOS technology and operates from a 10-V supply (which can be scaled down to 5-V supply with improved process technology), and is capable of rail-to-rail operation at both the input and output.

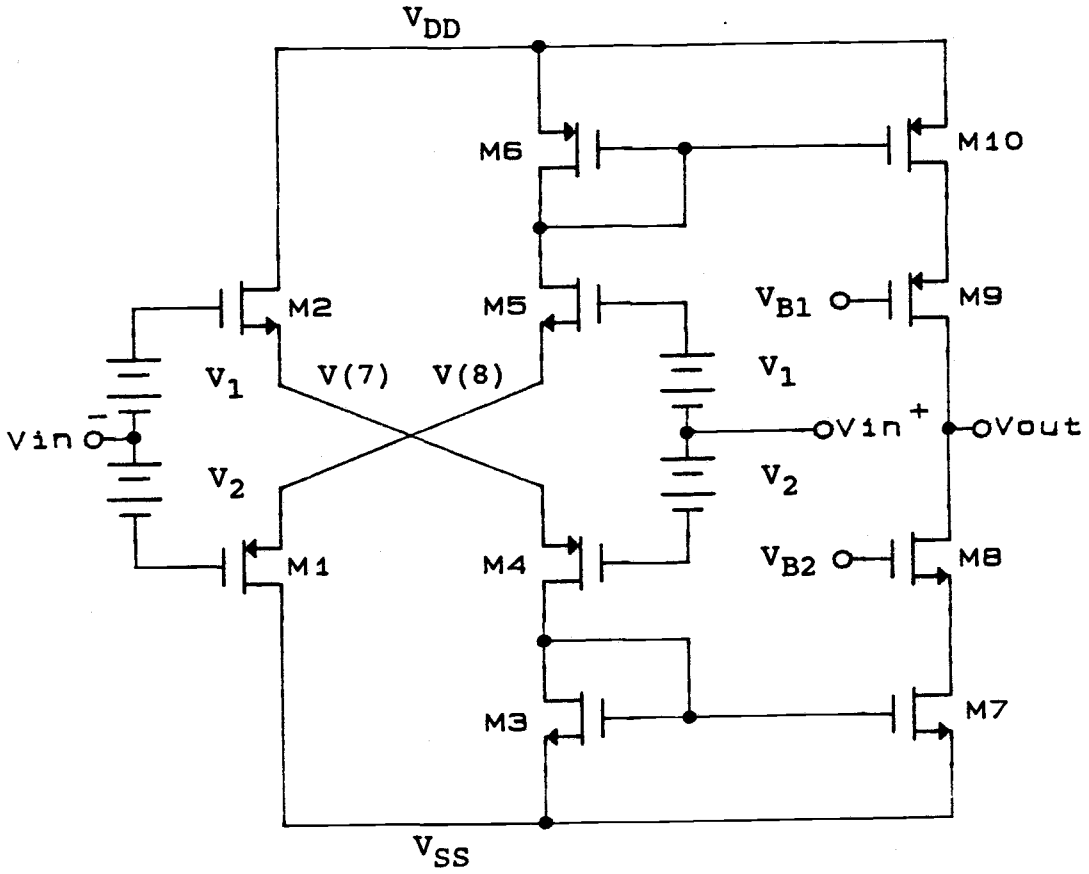


Fig. 1. A simplified differential-input class-AB CMOS operational amplifier.

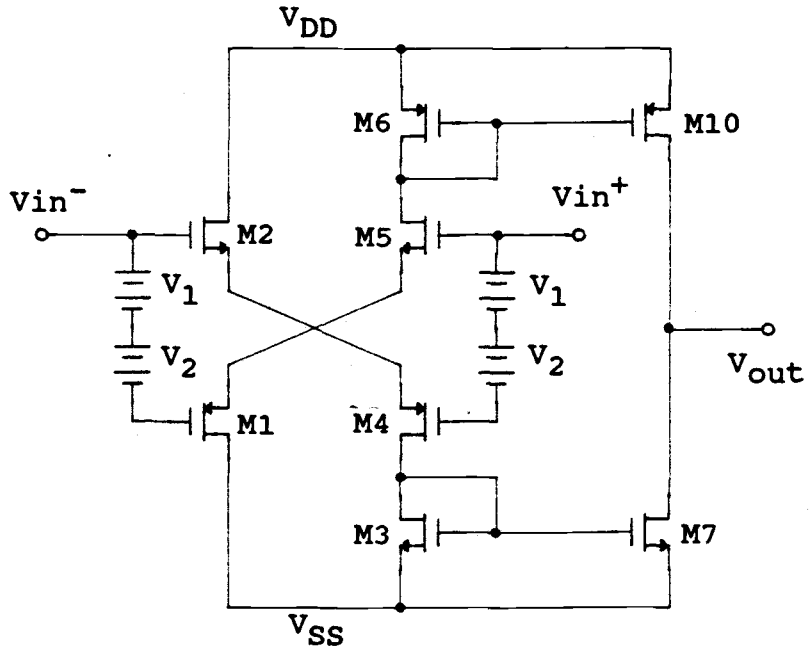


Fig. 2. A class-AB CMOS operational amplifier with positive shift in the input common-mode voltage range.

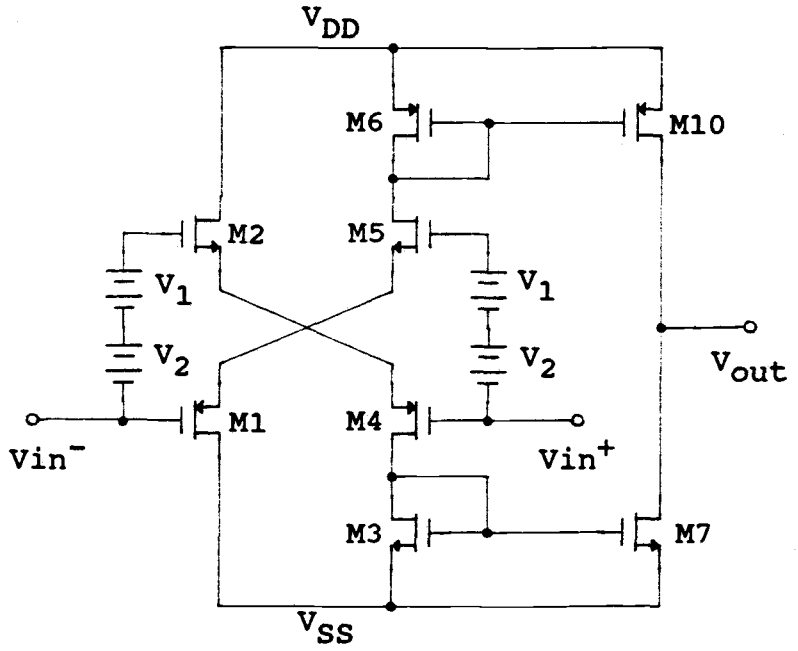
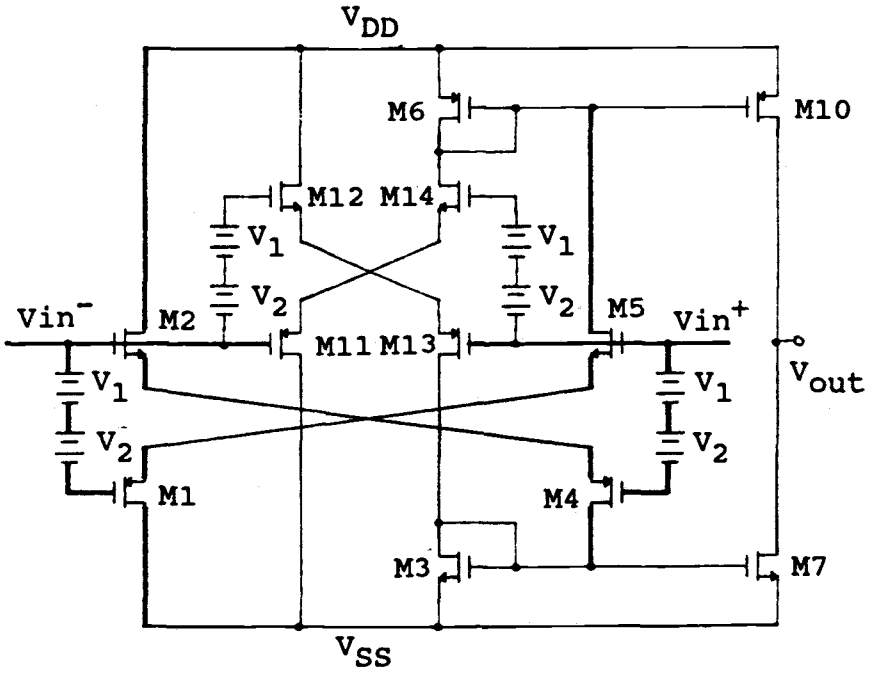
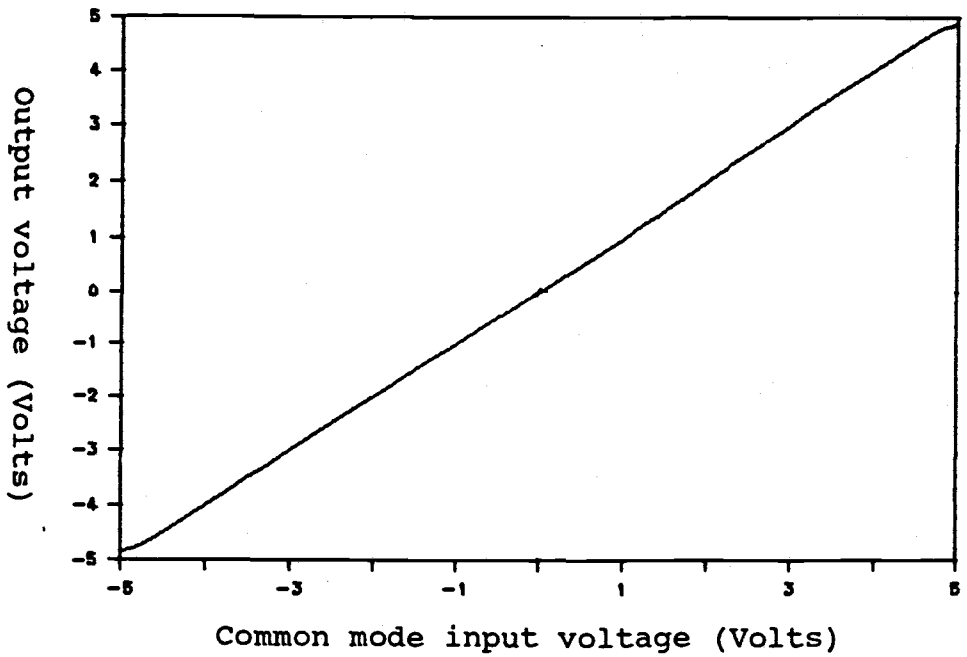


Fig. 3. A class-AB CMOS operational amplifier with negative shift in the input common-mode voltage range.



(a)



(b)

Fig. 4. (a) A simplified schematic of a composite CMOS class- AB operational amplifier. (b) Voltage transfer curve (unity gain).

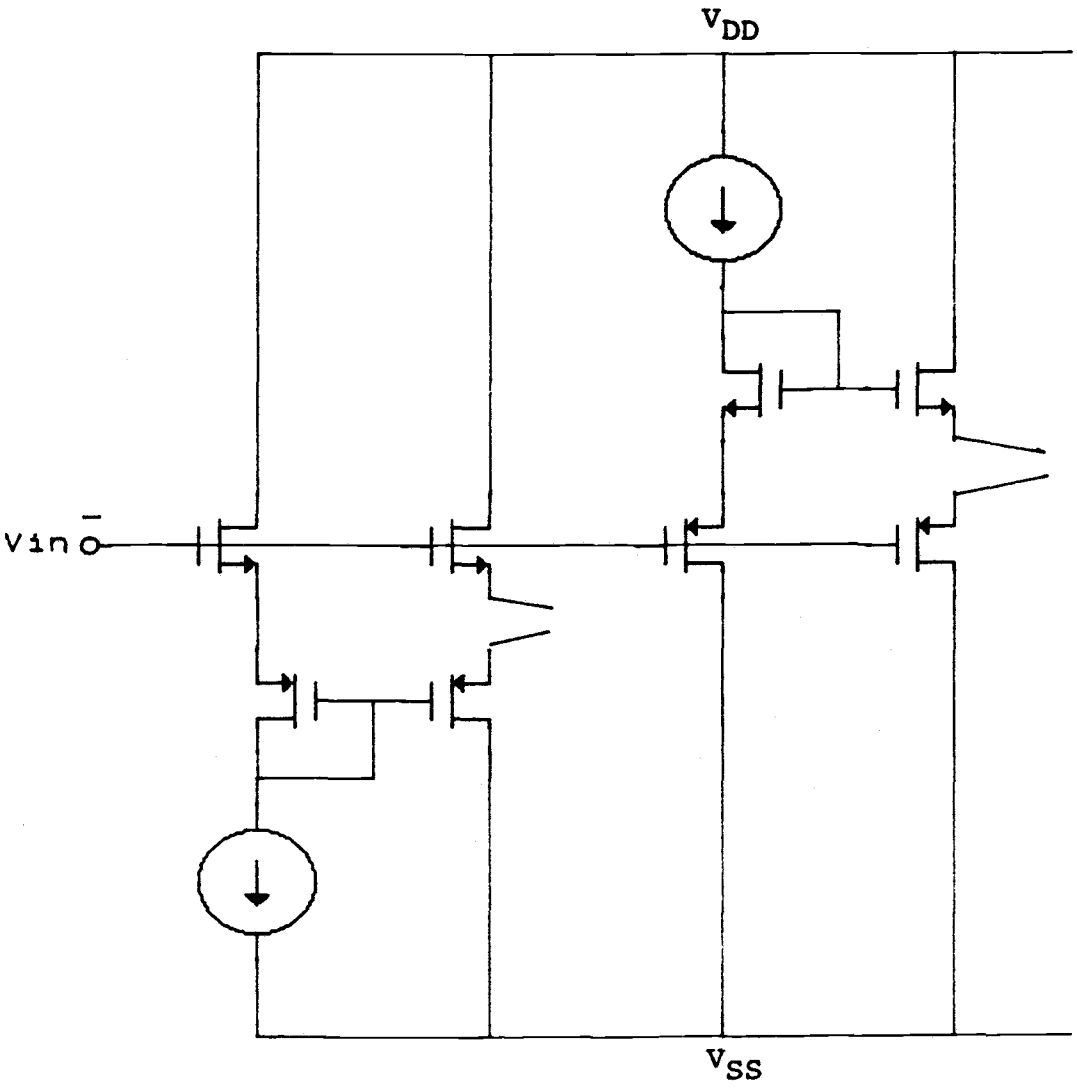


Fig. 5. The input DC bias and level-shift circuitry.

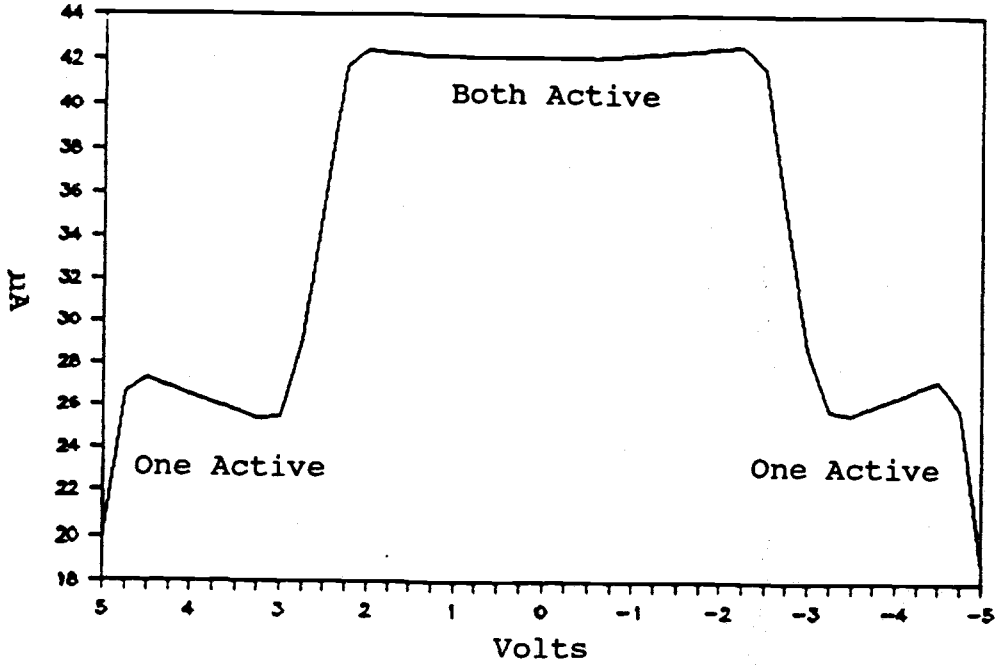


Fig. 6. DC bias current versus input common-mode voltage (unity-gain).

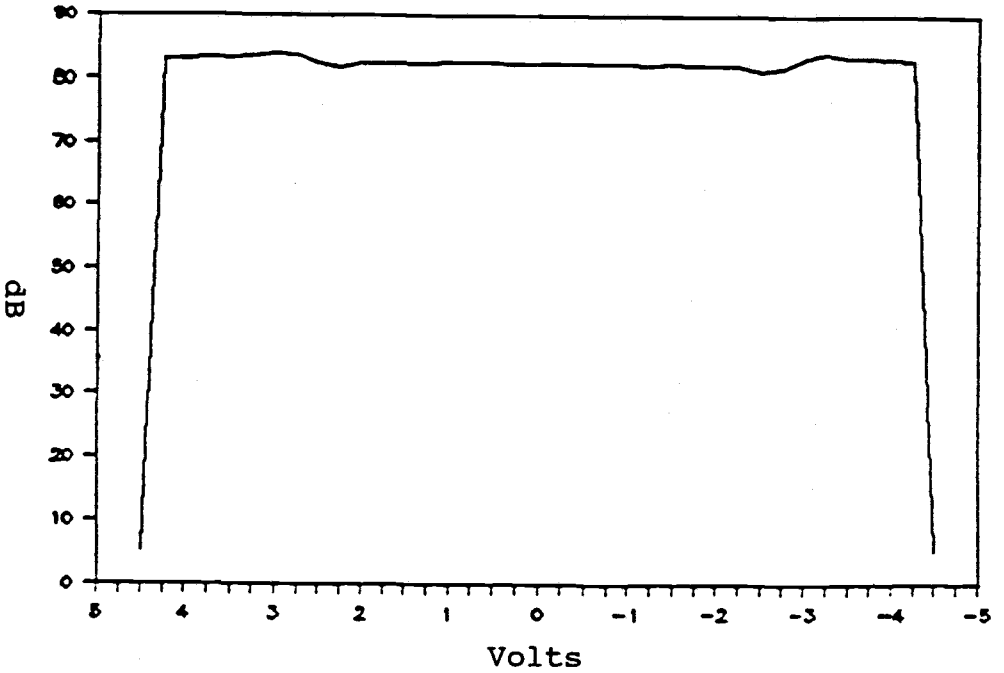


Fig. 7. Small-signal voltage gain versus input common-mode voltage.

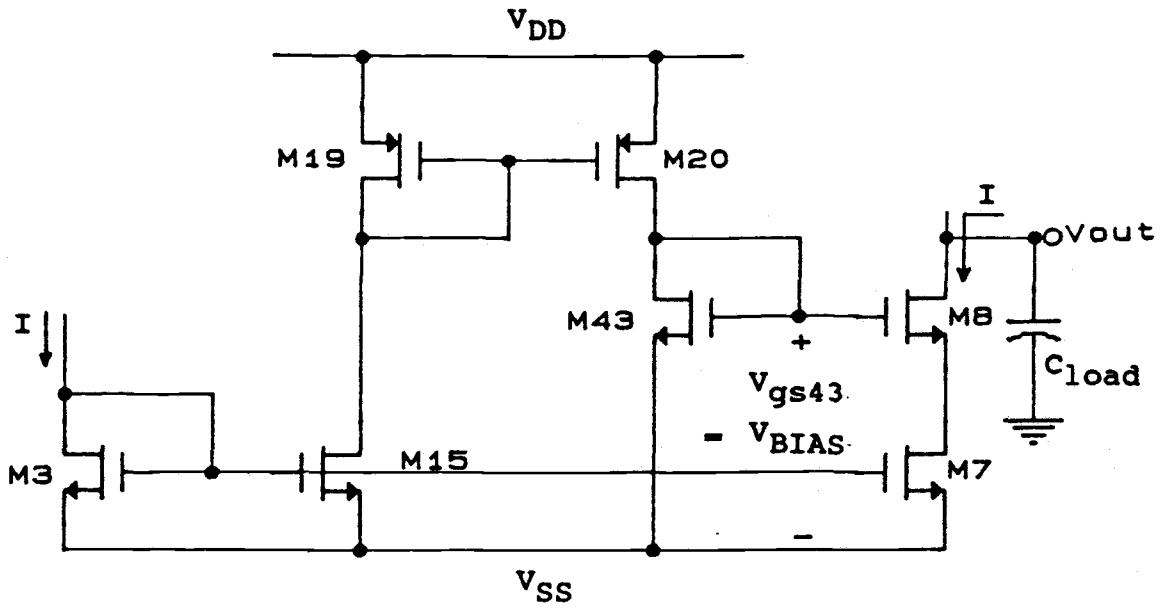
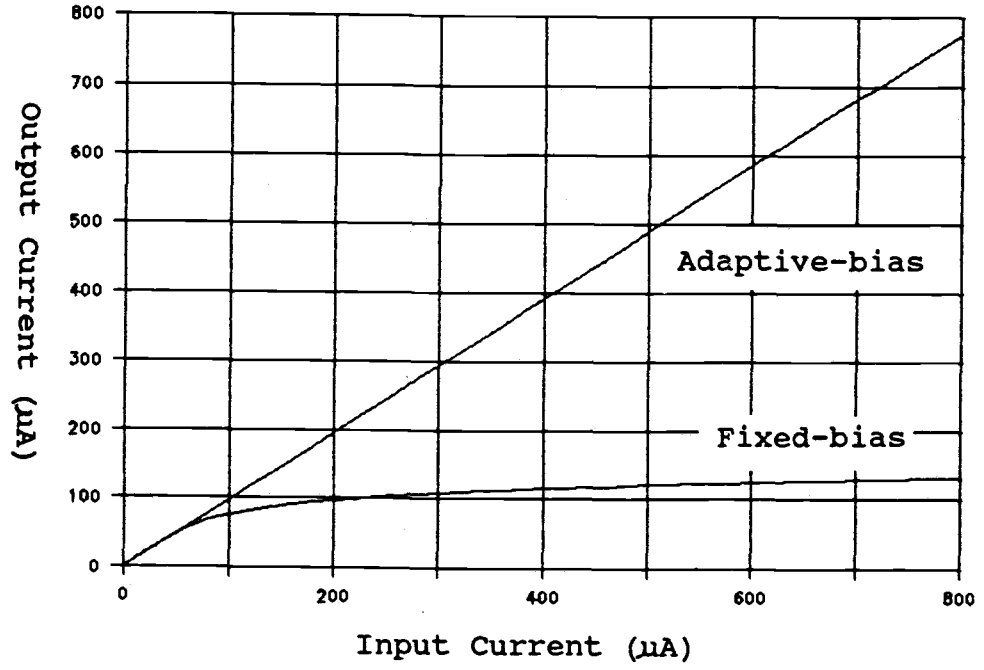
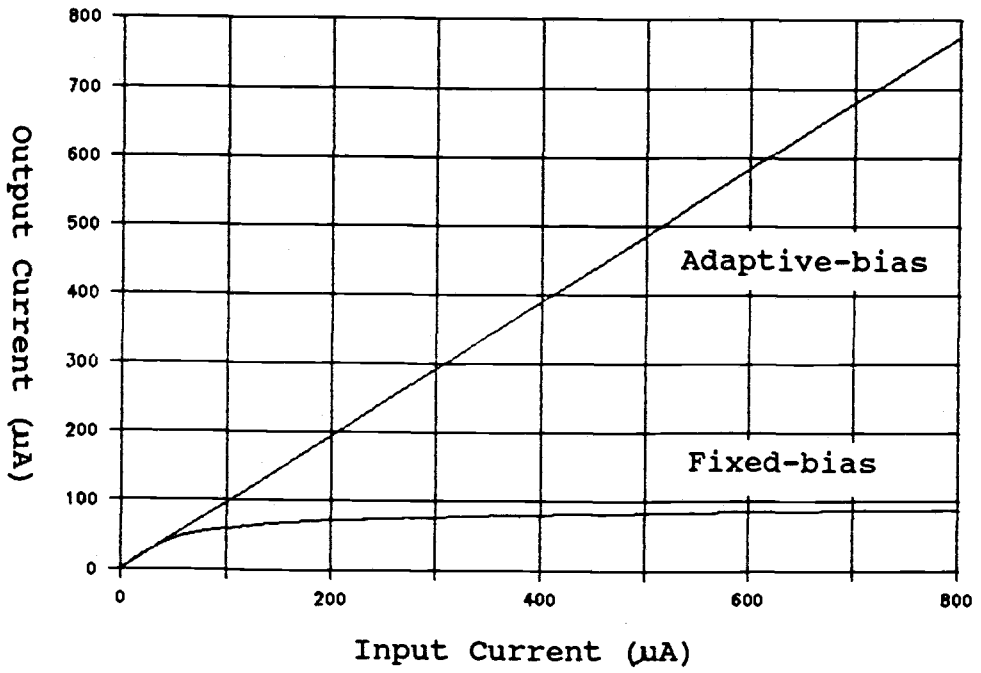


Fig. 8. Adaptively-biased output circuitry.



(a)



(b)

Fig. 9. Transfer curves for the cascode current mirrors. (a) NMOS and (b) PMOS.

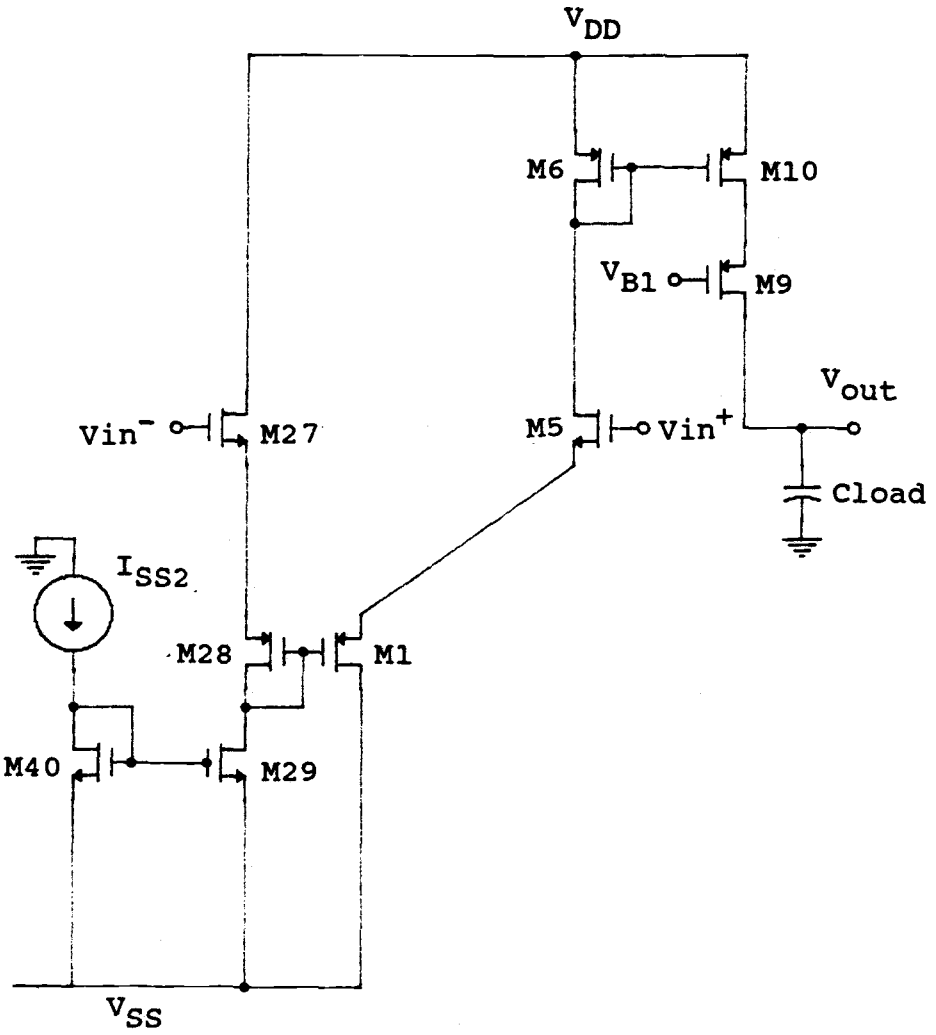
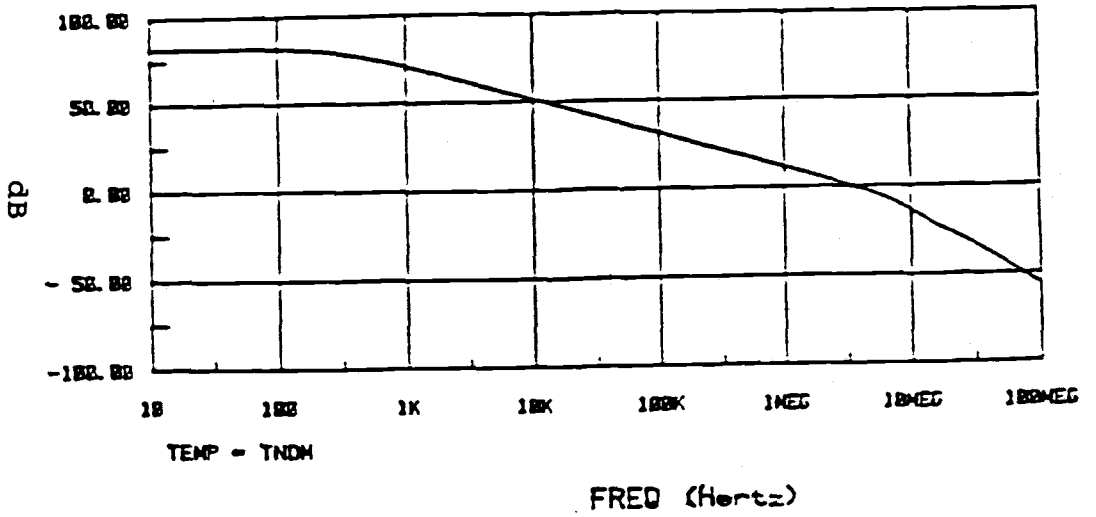
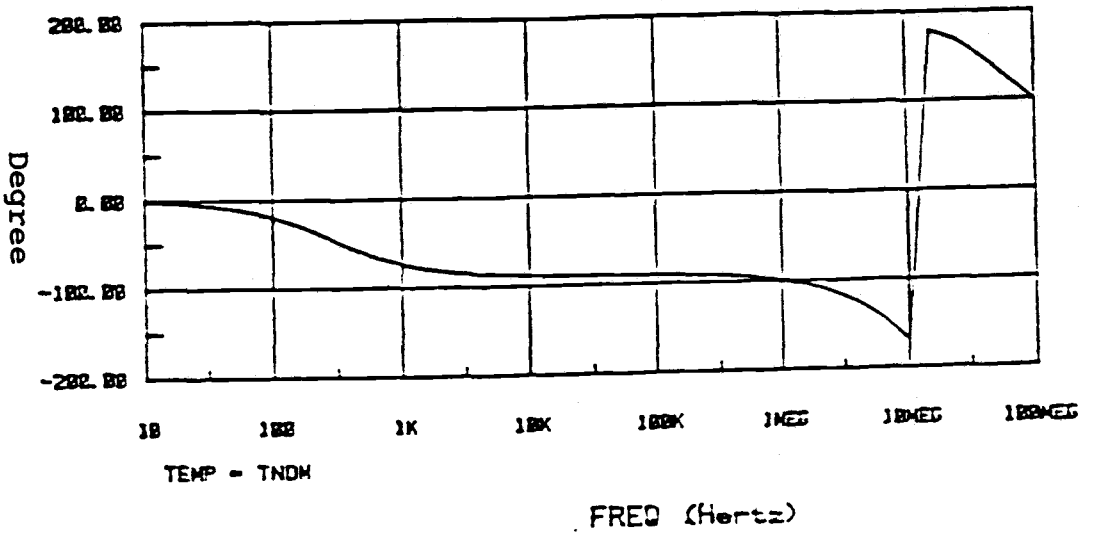


Fig. 10. Active portion of the amplifier for a large positive input signal.



(a)



(b)

Fig. 11. The frequency response of a composite class-AB amplifier. (a) Magnitude and (b) Phase.

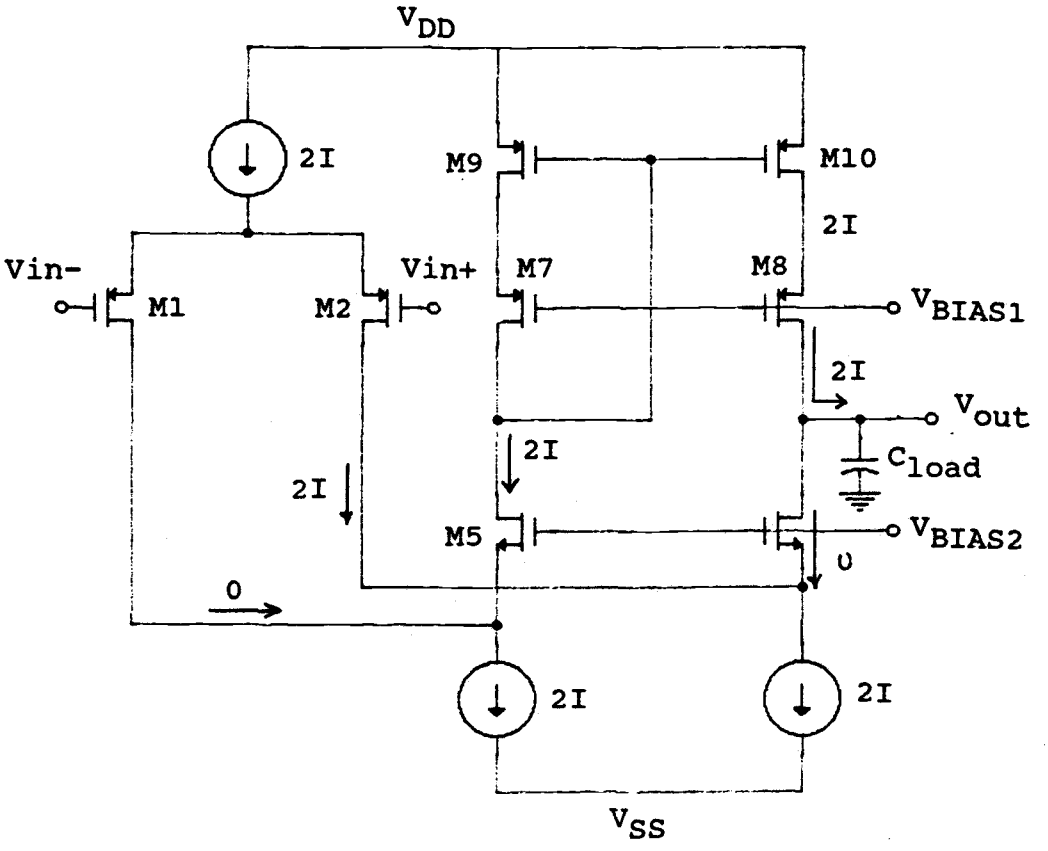
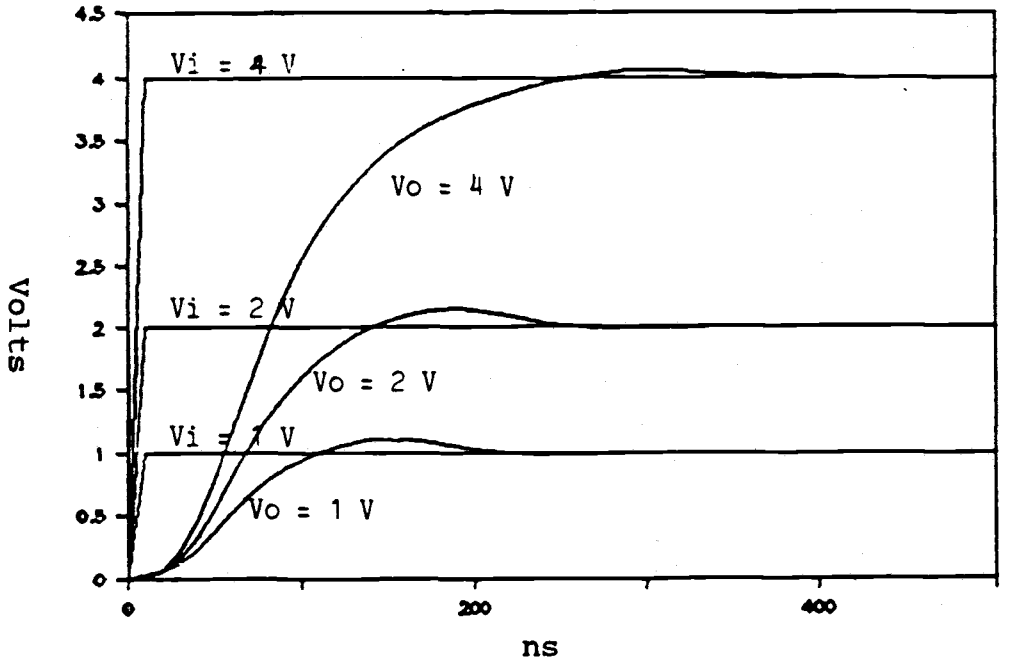
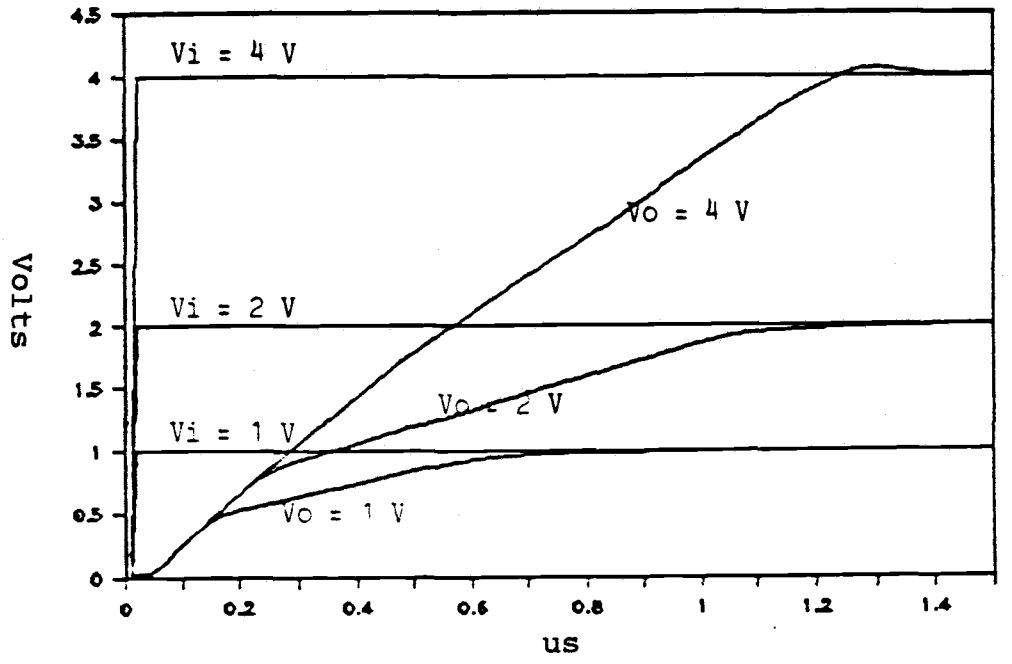


Fig. 12. Schematic of a folded-cascode amplifier.



(a)



(b)

Fig. 13. Transient response of (a) a class-AB amplifier and (b) a folded-cascode amplifier with the same amount of bias currents.

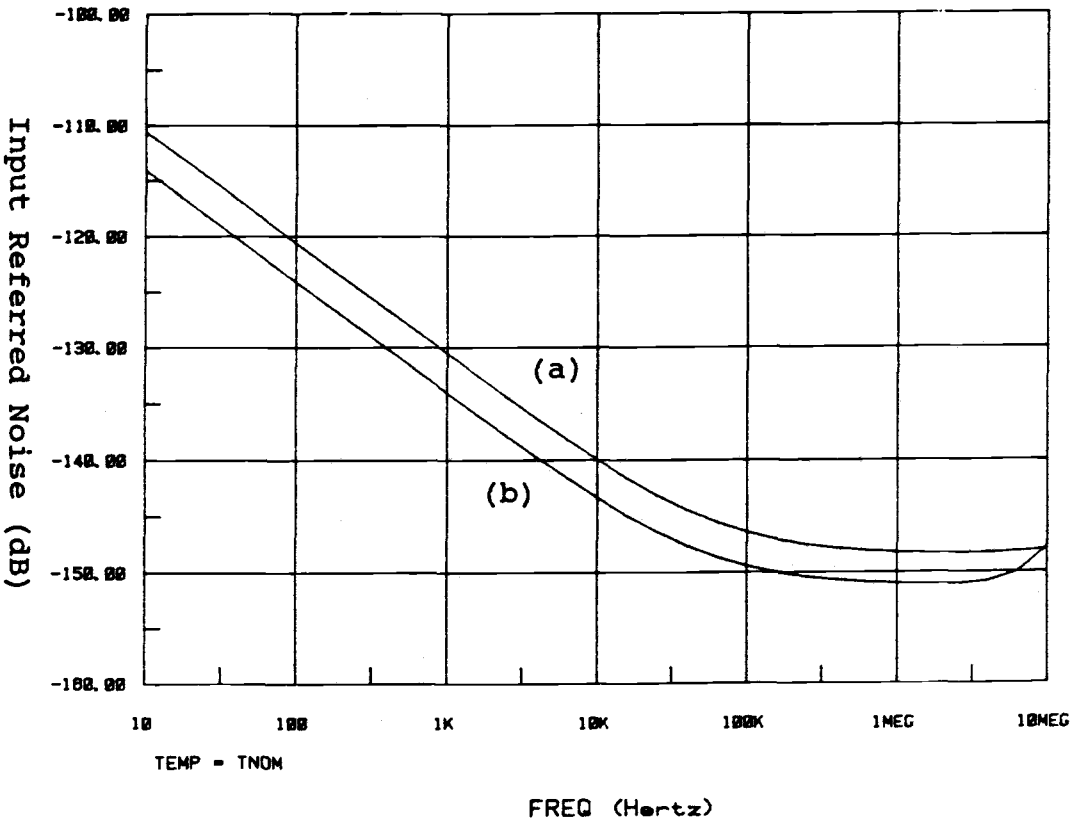


Fig. 14. Input referred noise of (a) a conventional (one input-stage) and (b) a high-swing (two input-stage) class-AB CMOS operational amplifiers.

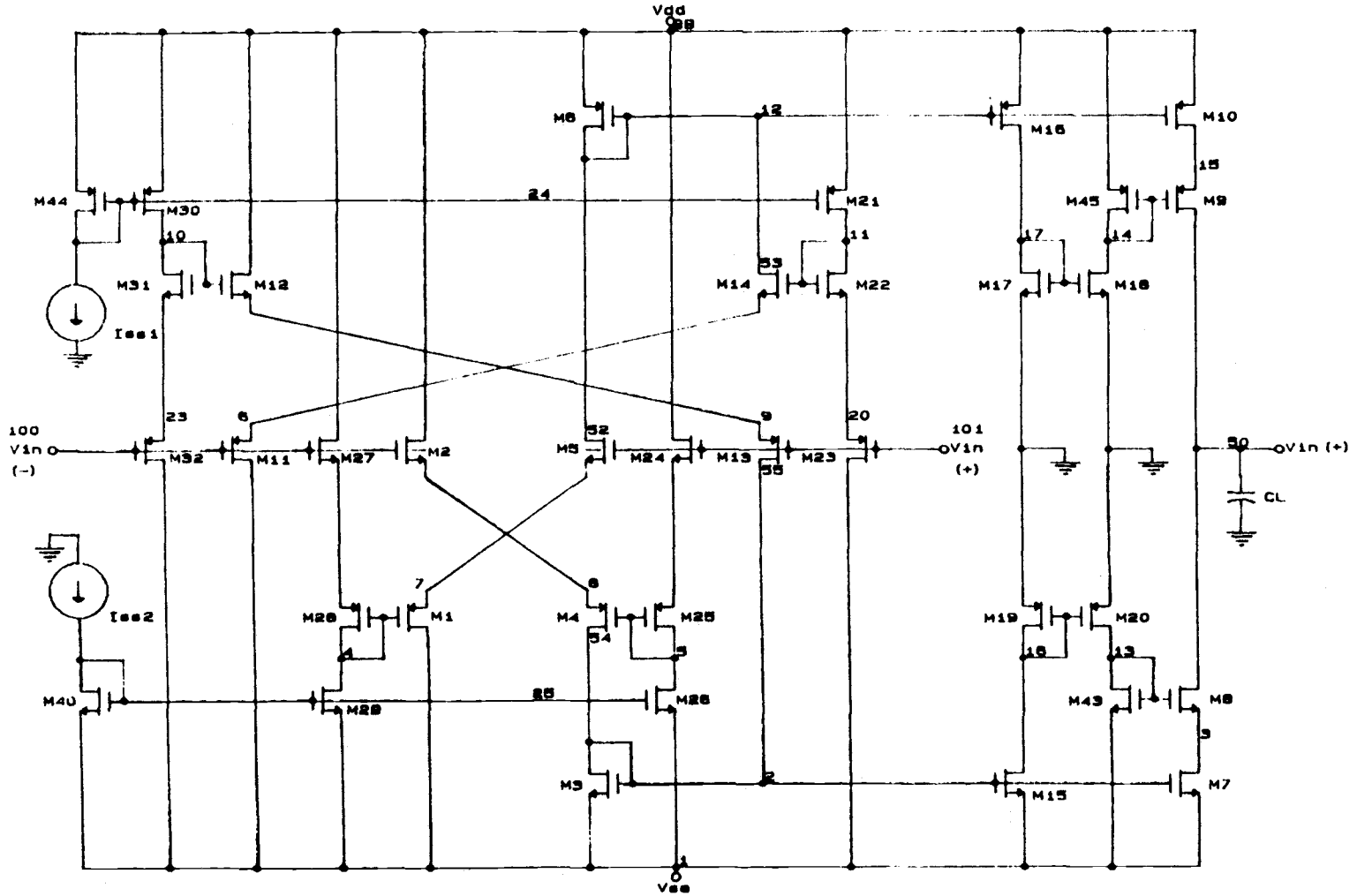


Fig. 15. A complete schematic of the high-swing class-AB CMOS operational amplifier.

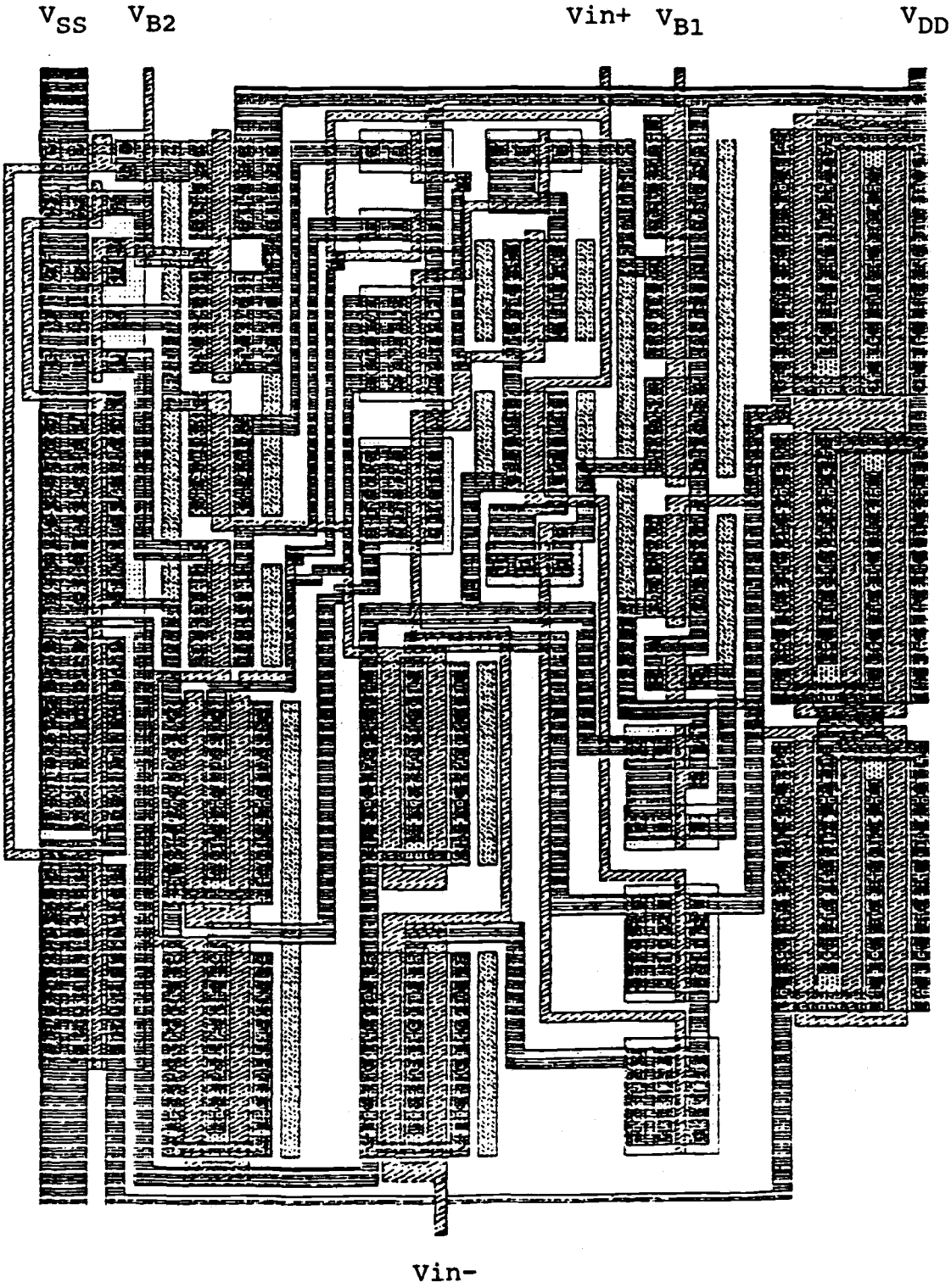


Fig. 16. A layout of the high-swing class-AB CMOS operational amplifier.

VII. REFERENCES

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VIII. APPENDICES

A. Derivation of input-referred noise

For a MOS transistor, the most important noise sources are the thermal noise (at high frequencies) and the flicker noise (at low frequencies). A MOS transistor can be modeled by a noiseless transistor with gate connected to a voltage source V_n, which is given by

$$V_n = (V_{nT}^2 + V_{nf}^2)^{\frac{1}{2}}$$

$$= \left(\frac{8kT\Delta f}{3g_m} + \frac{KFI_B^{AF}\Delta f}{C_{ox}g_m^2L^2f}\right)^{\frac{1}{2}} \qquad (25)$$

where

g_m --- the transconductance;

I_B --- the bias current;

C_{ox} -- the gate oxide capacitance per unit area;

L ---- the channel length;

KF --- the flicker noise coefficient;

AF --- the flicker noise exponent.

Since all the noise source are uncorrelated, the equivalent input-referred noise can be obtained by replacing each transistor with a noiseless transistor and a noise source, adding up all of the individual noise powers, taking the root mean square of the output voltage and dividing it by the small-signal voltage gain of the amplifier resulting in:

$$V_{eq} = \frac{1}{A_0} \left[\sum_i A_{0i}^2 V_{ni}^2 \right]^{\frac{1}{2}} = \left[\sum_i \left(\frac{A_{0i}}{A_0} \right)^2 V_{ni}^2 \right]^{\frac{1}{2}} \qquad (26)$$

For all MOSFETs having the same transconductances ($g_{mn} = g_{mp} = g_m$), the voltage gain (referred to the output) for the input devices (M1, M2, M4, M5, M11, M12, M13, M14, M22, M23, M24, M25, M27, M28, M31 and M32)(See Fig. 15) is given by

$$A_{0ip} = \frac{g_{mn} g_{mp}}{(g_{mn} + g_{mp}) g_{m(op)}} \times \frac{g_{m(op)}}{g_{out}}$$

$$= \frac{1}{2} \times \frac{g_m}{g_{m(op)}} \times \frac{g_{m(op)}}{g_{out}} \qquad (27)$$

where g_{out} is the conductance looking into the output node and $g_{m(op)}$ is the conductance looking into the current mirror. The voltage gain for M21, M26, M29 and M30 (act as the current source for level-shifting circuit) is given by

$$A_{0cs} = \frac{g_m}{g_m/2} \times A_{0ip}$$

$$= \frac{g_m}{g_{m(op)}} \times \frac{g_{m(op)}}{g_{out}} \qquad (28)$$

The voltage gain for the output devices (M3, M6, M7 and M10) is given by

$$A_{0op} = \frac{g_{m(op)}}{g_{out}} \tag{29}$$

while the low-frequency gain of the amplifier is

$$A_0 = \frac{g_{m(eff)}}{g_{out}} \tag{30}$$

For a conventional class-AB op-amp (Fig. 1), $g_{m(op)} = g_{m(eff)} = g_m$ (From (16a). The ratios of the voltage gain are given by

$$\frac{A_{0ip}}{A_0} = \frac{1}{2} \tag{31a}$$

$$\frac{A_{0cs}}{A_0} = 1 \tag{31b}$$

$$\frac{A_{0op}}{A_0} = 1 \tag{31c}$$

For a high-swing class-AB op-amp (Fig. 15), $g_{m(op)} = g_{m(eff)} = 2g_m$ (From (16a). The ratios of the voltage gain are given by

$$\frac{A_{0ip}}{A_0} = \frac{1}{4} \tag{32a}$$

$$\frac{A_{0cs}}{A_0} = \frac{1}{2} \tag{32b}$$

$$\frac{A_{0op}}{A_0} = 1 \qquad (32c)$$

The voltage gain for the other devices is so small that we can neglect their contributions to the overall noise power. Thus, the V_{eq} for a conventional class-AB op-amp (one input-stage) is given by

$$V_{eq} = [\ (\frac{1}{2})^2 \times 4(V_{n(ipp)}^2 + V_{n(ipn)}^2) + (1)^2 \times (V_{n(csp)}^2 + V_{n(csn)}^2) + (1)^2 \times 2(V_{n(opp)}^2 + V_{n(opn)}^2)\ ]^{\frac{1}{2}} \qquad (33a)$$

$$= [\ (V_{n(ipp)}^2 + V_{n(ipn)}^2) + (V_{n(csp)}^2 + V_{n(csn)}^2) + 2(V_{n(opp)}^2 + V_{n(opn)}^2)\ ]^{\frac{1}{2}} \qquad (33b)$$

The V_{eq} for a high-swing class-AB op-amp (two input-stage) is given by

$$V_{eq} = [\ (\frac{1}{4})^2 \times 8(V_{n(ipp)}^2 + V_{n(ipn)}^2) + (\frac{1}{2})^2 \times 2(V_{n(csp)}^2 + V_{n(csn)}^2) + (1)^2 \times 2(V_{n(opp)}^2 + V_{n(opn)}^2)\ ]^{\frac{1}{2}} \qquad (34a)$$

$$= [\ \frac{1}{2} \times (V_{n(ipp)}^2 + V_{n(ipn)}^2) + \frac{1}{2} \times (V_{n(csp)}^2 + V_{n(csn)}^2) + 2 \times (V_{n(opp)}^2 + V_{n(opn)}^2)\ ]^{\frac{1}{2}} \qquad (34b)$$

B. SPICE parameters

	P06	N10
TYPE	PMOS	NMOS
LEVEL	2.000	2.000
VTO	-.750	.750
KP	1.20D-05	4.00D-05
GAMMA	.450	.170
PHI	.620	.520
LAMBDA	3.30D-02	3.30D-02
PB	.870	.820
CGSO	1.73D-10	1.73D-10
CGDO	1.73D-10	1.73D-10
CGBO	1.00D-10	1.00D-10
CJ	1.40D-04	5.50D-05
MJ	.500	.500
CJSW	6.00D-10	3.00D-10
MJSW	.500	.500
JS	1.00D-05	1.00D-05
TOX	6.00D-08	6.00D-08
XJ	5.00D-07	5.00D-07
LD	3.00D-07	3.00D-07
UCRIT	4.00D+04	4.00D+04
UEXP	.200	.100
KF	1.50D-27	1.00D-27
AF	1.250	1.250

C. SPICE program

```
*  3/ 8/88 ******  HPSPICE (2G.5 2201)  ****** 17:22: 6*

 CLASS AB OP-AMP

                              TEMPERATURE =   27.000 DEG C

**********************************************************
CLASS AB OP-AMP
*Vdsat =.35 Volts

***POWER SUPPLY***
VDD 99 0 5
VSS 1  0 -5

***CLASS AB INUPT STAGE***
M1    1   4   7   7 P06 W =160U  L= 6U
+                       AD=1440P AS=1440P PD=178U PS=178U
M2   99 100   8   1 N10 W = 80U  L=10U
+                       AD= 720P AS= 720P PD= 98U PS= 98U
M4    2   5   8   8 P06 W=160U  L= 6U
+                       AD=1440P AS=1440P PD=178U PS=178U
M5   12 101   7   1 N10 W = 80U  L=10U
+                       AD= 720P AS= 720P PD= 98U PS= 98U
M11   1 100   6   6 P06 W =160U  L= 6U
+                       AD=1440P AS=1440P PD=178U PS=178U
M12 99  10   9   1 N10 W = 80U  L=10U
+                       AD= 720P AS= 720P PD= 98U PS= 98U
M13   2 101   9   9 P06 W =160U  L= 6U
+                       AD=1440P AS=1440P PD=178U PS=178U
M14 12  11   6   1 N10 W = 80U  L=10U
+                       AD= 720P AS= 720P PD= 98U PS= 98U

***CASCODE OUTPUT STAGE***
M3    2   2   1   1 N10 W =160U  L=10U
+                       AD=1440P AS=1440P PD=178U PS=178U
M6   12  12  99  99 P06 W =320U  L= 6U
+                       AD=2880P AS=2880P PD=338U PS=338U
M7    3   2   1   1 N10 W =160U  L=10U
+                       AD=1440P AS=1440P PD=178U PS=178U
M8   51  13   3   1 N10 W =160U  L=10U
+                       AD=1440P AS=1440P PD=178U PS=178U
M9   50  14  15  15 P06 W =320U  L= 6U
+                       AD=2880P AS=2880P PD=338U PS=338U
M10 15  12  99  99 P06 W =320U  L= 6U
+                       AD=2880P AS=2880P PD=338U PS=338U
```

```
***LEVEL-SHIFTING CKT***
M21 11  24  99  99 P06 W = 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M22 11  11  20   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M23  1 101  20  20 P06 W= 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M24 99 101  21   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M25  5   5  21  21 P06 W= 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M26  5  25   1   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M27 99 100  22   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M28  4   4  22  22 P06 W= 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M29  4  25   1   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M30 10  24  99  99 P06 W= 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M31 10  10  23   1 N10 W= 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M32  1 100  23  23 P06 W= 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U

***ADAPTIVELY BIASED OUTPUT CKT***
M15 16   2   1   1 N10 W = 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M16 17  12  99  99 P06 W = 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M17 17  17   0   1 N10 W = 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M18 14  17   0   1 N10 W = 20U  L=10U
+                       AD= 180P AS= 180P PD= 38U PS= 38U
M19 16  16   0   0 P06 W = 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M20 13  16   0   0 P06 W = 40U  L= 6U
+                       AD= 360P AS= 360P PD= 58U PS= 58U
M43 13  13   1   1 N10 W =  5U  L=10U
+                       AD=  45P AS=  45P PD= 23U PS= 23U
M45 14  14  99  99 P06 W = 10U  L= 6U
+                       AD=  90P AS=  90P PD= 28U PS= 28U
```

```
***BIAS CKT***
IS1 24   0  5U
IS2  0  25  5U
M44 24  24  99  99 P06 W = 40U  L= 6U
+                      AD= 360P AS= 360P PD= 58U PS= 58U
M40 25  25   1   1 N10 W = 20U  L=10U
+                      AD= 180P AS= 180P PD= 38U PS= 38U

***LOAD CAP***
CL 50 0 10P

***MOSFET MODEL***
.INCLUDE MODEL

***NODE SET***
.NODESET V(100)=0 V(101)=0 V(50)=0
+ V(2) =-4.062    V(12)= 4.09
+ V(6) = 1.000    V(9) = 1.005
+ V(7) =-1.216    V(8) =-1.212
+ V(3) =-4.6320   V(15)= 4.6145
+ V(16)=-4.6561   V(17)= 4.6417
+ V(21)=-1.2079   V(22)=-1.2077
+ V(4) =-2.2288  V(5) =-2.2291
.OPTIONS GMIN=1E-10 NOPAGE  NOMOD  CHGTOL=1E-15
V51  50 51

***AC***
RFB  50 100  10E12
CFB  100  0  1
VIN  101 0 AC 1
.AC  DEC  5  10 1G
.PR  AC  VDB(50) VP(50)
.GR  AC  VDB(50) VP(50)

***DC***
VIN  101  0
RF   100 50 1E12
CF   100  0 1
.DC VIN 5 -5 .25
.PR DC V(51) I(V51)
.GR DC V(51) I(V51)

***TRANSIENT***
VST 50 100
.TRAN .025U .5U
.PR TRAN V(50)
.GR TRAN V(50) V(101)

.END
```

D. Amplifier specifications

Design Parameter	Symbol	SPICE	
Low-frequency open-loop voltage gain	A_0	82.3	dB
Unity-gain frequency	f_u	3.6	MHz
Common mode rejection ratio	CMRR	109.27	dB
Phase margin (Unity-gain)		58.75	^{o}
Settling time (Step Size = 10 ns)	t_s	400	ns
Common mode input range		$\pm$4.25	Volts
Input-referred DC offset voltage	V_{of}	0.6	mV
Input noise density			
f = 1K (Hz)		197.5	$nVf^{-\frac{1}{2}}$
f = 100K (Hz)		50.0	$nVf^{-\frac{1}{2}}$
DC power dissipation	P_D	1.63	mW
Voltage supply		5	Volts
Load capacitance	C_{load}	10	pF