

AN ABSTRACT OF THE THESIS OF

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(Major professor)

The field-effect transistor offers advantages as a chopping device since it does not have an offset voltage and it is not speed limited by its response time.

Offset and drift are caused by leakage current and capacitive coupling between the control gate and the signal path. The capacitive component of this drift is proportional to frequency so in order to increase the chopping frequency and maintain low drift, it is necessary to compensate for the capacitive drifts.

Two techniques of balancing a second capacitor against the detrimental gate-drain capacitance of the chopper are investigated.

First a fixed capacitor is used for balance, and capacitive offset is reduced by about $1/20$.

This balance is then improved by using the capacitance of a second FET for balance. This improves capacitive balance by a factor of two over the fixed capacitor technique and also allows for

cancellation of leakage currents.

An FET chopper when operating at 10KC and balanced with a second FET is observed to have a zero drift of less than 10 uv from 20°C to 100°C.

THE FIELD-EFFECT TRANSISTOR AS A
MEDIUM-SPEED, LOW-LEVEL CHOPPER

by

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THE FIELD-EFFECT TRANSISTOR AS A MEDIUM-SPEED, LOW-LEVEL CHOPPER

INTRODUCTION

Low level d. c. amplification has been a difficult problem since amplifiers were first being constructed. Temperature drifts of circuit parameters have caused difficulty by producing drift of the output while the input remains constant. These drifts can be minimized by prudent selection of the amplifying devices and careful circuit design, but the best performance is attained by use of the chopper amplifier.

The chopper amplifier converts the d. c. signal to an a. c. signal of proportional magnitude and then amplifies the a. c. signal in a capacitively-coupled amplifier. The d. c. signal is then restored at the output. This type of amplification reduces drift to an absolute minimum since bias drift in the a. c. amplifier is not passed to the output.

The success of the chopper amplifier depends on the use of a chopping device which will reliably produce an a. c. output which is proportional to the d. c. input.

The nearly ideal device for this application is the mechanical chopper which is used to periodically short out the input of the amplifier. This produces a square wave of peak-to-peak amplitude equal to the input d. c. signal.

The disadvantages of the mechanical chopper result principally from the fact that it is a mechanical device. This limits its speed of operation and its lifetime.

Since the chopper amplifier bandwidth is directly proportional to the chopping frequency, it is desirable to maximize the chopping rate. However, the mechanical chopper is limited to a few hundred cycles per second chopping rate. This encourages the designer to search for a non-mechanical chopping device.

To this end, much work has been directed toward the development of transistor and photoconductive choppers, but these devices have inherent limitations also.

The transistor is capable of fast operation, but it is plagued with a temperature sensitive offset voltage of several hundred microvolts to several millivolts which produces an a. c. output with zero d. c. input. In order to chop very small signals of microvolt amplitude, it is necessary to match the offsets of two transistors. A good measure of success is attained by this balance technique but offset is still in the tens of microvolts at room temperature.

The photoconductive chopper does not have the offset difficulties of the transistor but it has speed limitations which prevent the use of chopping frequencies above about 1 KC.

The field-effect transistor (FET) seems to be a good quality non-mechanical chopper since it has no offset voltage like the

conventional transistor and its speed of response is not limited like the photoconductive chopper. It also is not without limitation, however, and this brings out the purpose of this thesis.

The objectives of this thesis are to determine the limitations of the FET chopper and to investigate some methods of improving capabilities at higher chopping rates.

CHARACTERISTICS OF THE FIELD-EFFECT TRANSISTOR

Before proceeding any further, it might be well to include a brief description of the FET and its characteristics.

A cross section of a silicon junction FET is shown in Figure 1. It consists of a current conducting slab of P-type silicon which is surrounded by an N-type gate. If the voltage on this gate is such to bias the junction negative, there will be a depletion layer, devoid of current carriers, in the junction region. The magnitude of the reverse bias voltage controls the size of the depletion region which in turn controls the conductance from drain to source. If the voltage is large enough (this value is called the pinch-off voltage, V_p), the depletion region will extend across the P-type region and produce a nearly zero conductance from drain to source.

The transistor characteristic curves resemble those shown in Figure 2 with the region near the origin representing a voltage-controlled resistance. The gate-source voltage controls the drain-source resistance.

The isolation between the gate and the drain-source region is by the reverse-biased diode; so the isolation is limited by the capacitance and leakage of this junction.

It is this imperfect isolation which limits the FET as a chopper.

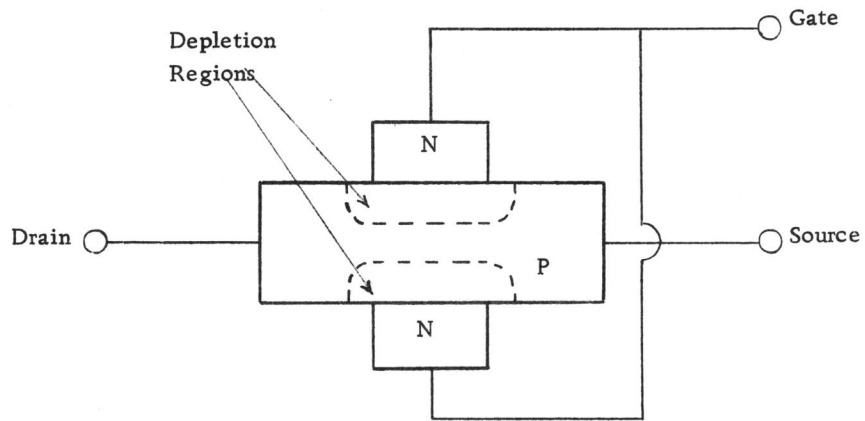


Figure 1. Cross-section of a field-effect transistor.

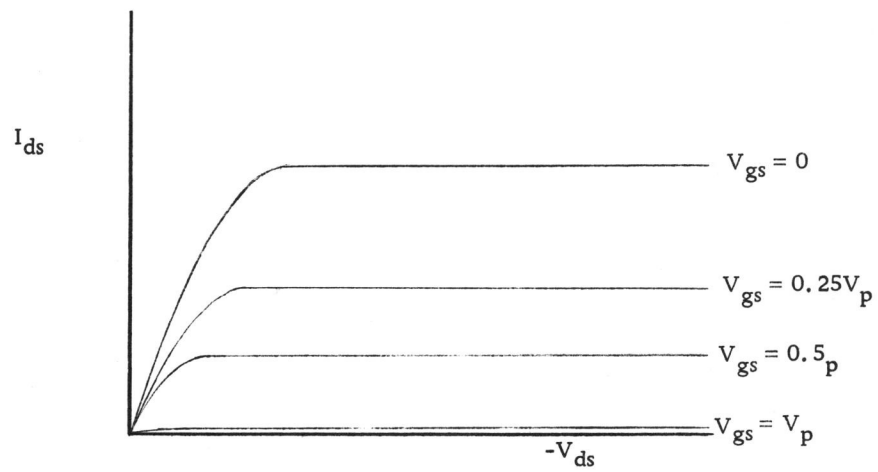


Figure 2. Characteristic curves for a field-effect transistor.

However, it seems worthwhile to pursue its possibilities since it is a device which has no offset voltage and also has potential as a medium-speed chopper (gain-bandwidth is about 20 MC).

BASIC FIELD-EFFECT TRANSISTOR CHOPPER

The basic FET chopper can be constructed in either of two connections, the series or the shunt, as shown in Figure 3.

Both circuits are simple, but the absence of the transformer in the shunt connection makes it the more desirable circuit. Also in favor of the shunt connection is the fact that a d. c. source resistance can easily be compensated for by a proper change in the value of R_d .

An oscillating voltage at V_d produces an oscillating drain-to-source resistance which in turn produces an oscillating signal at e_o , 180° out of phase with V_d .

With an ideal FET, the signal at e_o would have a peak-to-peak amplitude which is proportional to the input d. c. voltage and also depends on the values of R_d and the maximum and minimum of r_{ds} (the drain-to-source resistance).

Practically, there are errors, however, which show up clearly when $e_i = 0$. Then ideally, e_o should also equal zero, but with a non-ideal FET, a portion of the drive voltage V_d is "fed through" into the signal path at e_o .

Two separate mechanisms are responsible for this feed-through voltage reaching the signal path.

The first mechanism is an effective capacitance which exists

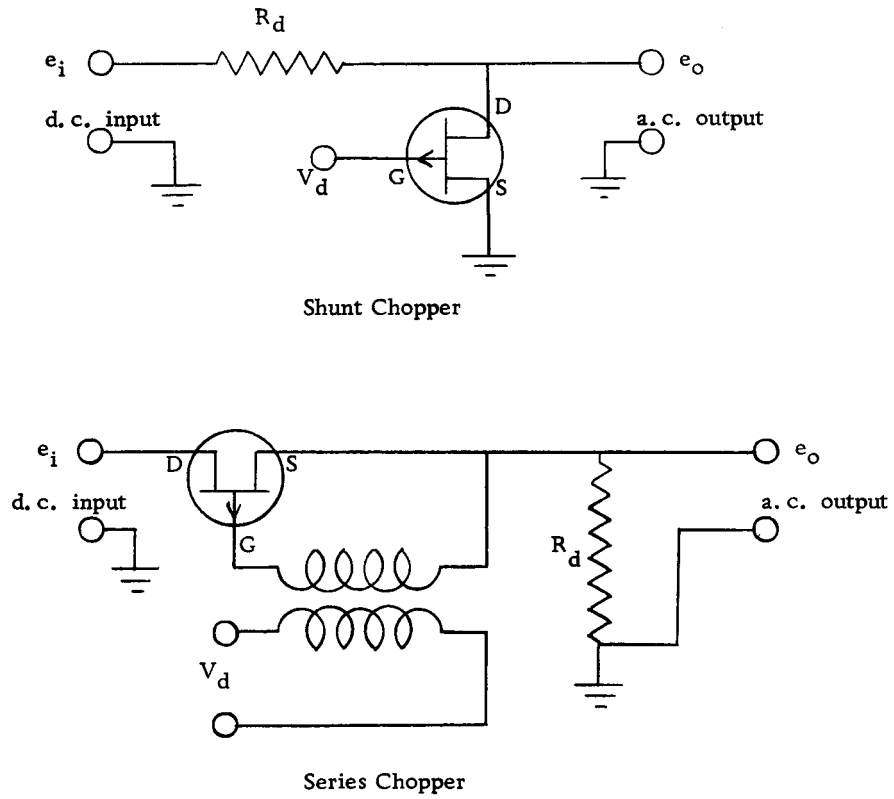


Figure 3. Basic shunt and series choppers.

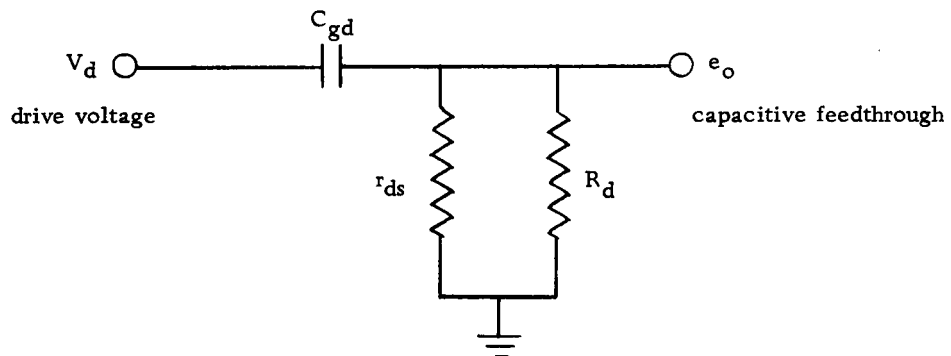


Figure 4. Equivalent circuit for capacitive feedthrough.

between the gate and drain terminals of the FET. This capacitance, C_{gd} , is produced by the fixed capacitance of the transistor housing plus the voltage-variable capacitance of the reverse-biased gate-drain diode.

From the equivalent circuit of Figure 4, with $e_1 = 0$, we see that a differentiated form of V_d will appear at e_o .

$$\text{Capacitive feedthrough} = RC_{gd} \frac{dV_d}{dt} ; R = \frac{(R_d)(r_{ds})}{R_d + r_{ds}}$$

For a square-wave drive, spikes would be observed at e_o and for a sine wave drive, a sine wave would appear at e_o which is distorted by variations in r_{ds} and C_{gd} as V_d varies.

The second mechanism of feedthrough is by reverse leakage current in the gate diode. This leakage, i_L , is small at room temperature, but since it increases by approximately doubling for every 10° of temperature rise, it becomes significant at higher temperatures.

These two feedthrough voltages are detrimental to the chopper operation since with zero input at e_1 , an a. c. output appears at e_o . This produces a zero offset for the amplifier which at constant temperature can easily be compensated, but with any temperature variation, C_{gd} , i_L , and r_{ds} vary, thus producing drift of the d. c. zero point. Therefore, for a well designed chopper it is desired to minimize these feedthrough voltages.

Once a transistor has been chosen, there are only two circuit variables left, one of them being R_d . A reduction in R_d reduces the feedthrough voltages, but it also reduces the chopper gain, i. e. :

$$\frac{e_o \text{ (a. c.)}}{e_1 \text{ (d. c.)}} \quad .$$

Ideally:

$$\frac{\text{peak-peak } e_o}{e_1} = \frac{r_{ds} \text{ (max)}}{r_{ds} \text{ (max)} + R_d} - \frac{r_{ds} \text{ (min)}}{r_{ds} \text{ (min)} + R_d}$$

Reducing R_d causes both feedthrough and gain to decrease, but gain does not decrease quite as fast as the feedthrough voltage, so minimum R_d is desired. However, a chopper gain reduction places stiffer requirements on the amplifier so a tradeoff must be made. Here the choice was $R_d = r_{ds} \text{ (min)}$ which allows a maximum chopper gain of 0.5.

The remaining circuit variable is V_d with the possibility of varying its magnitude and shape. It is desired to minimize the amplitude of V_d since feedthrough is reduced by reducing V_d , but also maximum variation of r_{ds} is desired so as to get maximum chopper gain.

From the approximate relation,

$$r_{ds} = \frac{r_{ds}'}{(1 - V_{gs}/V_p)} ; r_{ds}' = r_{ds} \text{ (with } V_{gs} = 0)$$

it can be seen that if V_d ranges from near zero to V_p , then a maximum variation in r_{ds} would be attained and thus maximum chopper gain would be produced.

With the desirability of minimum V_p , C_{gd} , and i_L in mind, the 2N2841, manufactured by Siliconix, Inc., was chosen as the chopping device. This device has typical characteristics:

$$r_{ds'} = 11K \text{ ohm}$$

$$V_p = 1.2 \text{ volt}$$

$$C_{gd}(V_{gs} = 0) = 2 \text{ pf}$$

$$i_L(V_{gd} = 1V) = 18 \text{ pa}$$

Using a FET with these characteristics and applying the above reasoning, a chopper can be designed as follows:

R_d would be chosen as 11K ohms and V_d would range from 0.1 to 1.3 volts. Chopper gain would then be 0.45 and the leakage component of feedthrough at room temperature would be about 0.2 uv and is in phase with the driving voltage.

The capacitive component of feedthrough is determined by the shape of V_d . If V_d is a 10 KC sine wave, V_f is approximately:

$$V_f(\text{capacitive}) = 2\pi(10KC)(8K\Omega)(1.2V)(2pf) = 1.3 \text{ mv}$$

8K ohm is the average value of R_d in parallel with $r_{ds'}$.

This voltage is very nearly 90° out of phase with the drive voltage.

With a square-wave drive, the height of the switching spikes depends on the rise and fall times of the square wave. If these times were 2 us, the spikes would be about $(11K\Omega)(2pf)(1.2V/2us) = 13 \text{ mv}$.

The sine-wave drive was chosen for two reasons. First, the

frequency response of the amplifier used with a square-wave chopper must be significantly higher than the chopper drive frequency in order to maintain the square nature of the signal. Secondly, the amplifier has a tendency to be overdriven by the 13 mv spikes.

With a sine-wave drive chopper amplifier, as shown in Figure 5, which has a zero-phase-shift a. c. amplifier and the demodulator exactly in phase with the chopper, a large portion of the capacitive feedthrough will be removed at the demodulator. Removal occurs since the demodulator is phase sensitive. Maximum d. c. output results from signals in phase with the demodulator while signals 90° out of phase with the demodulator produce zero d. c. at the output, as shown in Figure 6.

In order for complete removal of the feedthrough voltage, it is necessary that the feedthrough be precisely 90° out of phase with the demodulator if $V_f(\text{cap})$ is a sine wave, and if it is not a sine wave, the average value between 0 and π must equal the average between π and 2π .

However, with 1.3 mv of capacitive feedthrough, 1000 to 1 rejection would be required at the demodulator to prevent masking of microvolt signals. This is difficult to achieve since it requires excellent synchronization of the demodulator and constant phase shift for the amplifier.

At lower frequencies the capacitive feedthrough is less

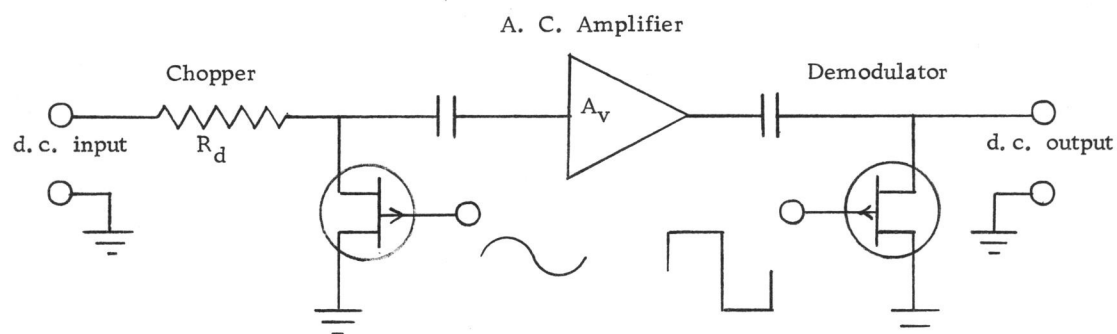


Figure 5. Basic Chopper Amplifier.

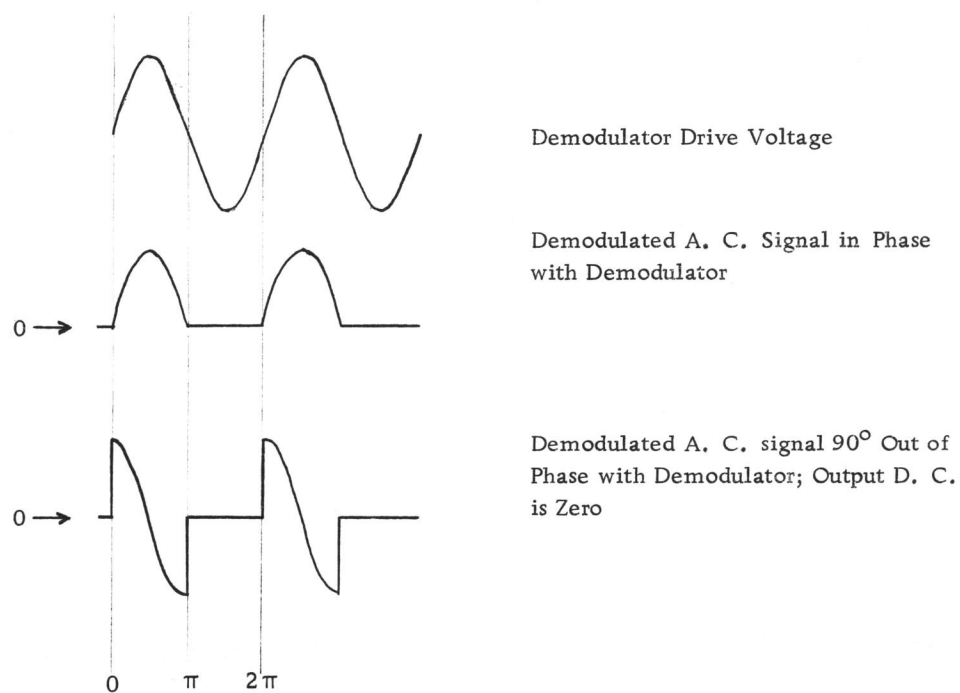


Figure 6. Demodulator Phase Characteristics.

troublesome, but at higher frequencies it, of course, gets worse.

Thus for higher frequency operation, it would be desirable to remove or in some way compensate for the capacitive feedthrough.

FIXED-CAPACITOR COMPENSATION

The simplest technique for removal of the capacitive feedthrough relies on the fact that the feedthrough is nearly sinusoidal in nature. A sine wave which is 180° out of phase with the feedthrough voltage is added to it and as a result, the voltage sum is nearly zero.

The circuit for this technique is illustrated in Figure 7. The amplitude of V_{d2} is adjusted to produce maximum cancellation of the feedthrough voltage. Cancellation depends on balance between the fixed C and C_{gd} so any variation of C_{gd} with gate-to-source voltage or with temperature will produce an unbalance. An estimation of the amount of cancellation can be gained from Figure 8 which illustrates typical variation of C_{gd} with gate to source voltage and temperature.

For example, the average difference between a fixed 1.8 pf capacitor and C_{gd} at room temperature is about 0.1 pf. This has reduced the effective capacitance by a factor of about $1/20$ so we could expect the 1.3 mv feedthrough at 10 KC to be reduced to about 50 uv.

However, a temperature rise to 100°C would raise the average capacitance difference to 0.3 pf and the feedthrough would raise to about 190 uv.

Since this feedthrough voltage is the sum of two voltages 90° out of phase with V_{d1} , the demodulator should still remove a large

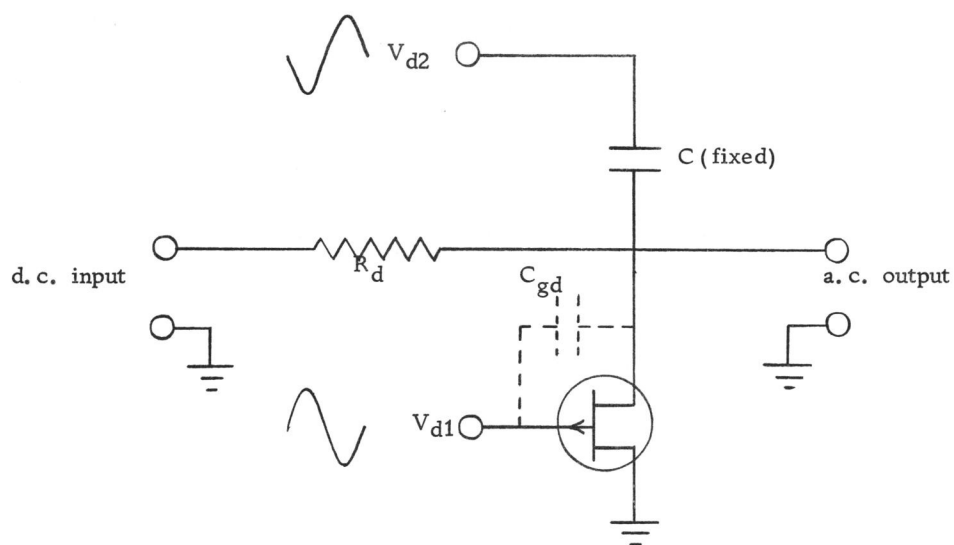


Figure 7. FET chopper with fixed-capacitor compensation.

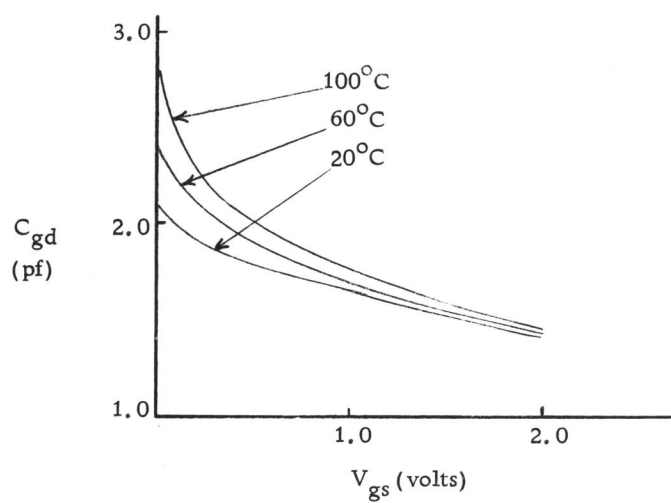


Figure 8. Typical gate-drain capacitance of 2N2841 vs. gate-source voltage and temperature.

portion of this feedthrough. If a 20 to 1 removal of feedthrough over signal at the demodulator were attained, one could expect a zero offset drift due to capacitive feedthrough from 5 uv to 19 uv over the temperature range 20°C to 100°C. This is with a chopping rate of 10 KC and should depend proportionately on the chopping rate. For instance, at 100 KC, drift would be 50 uv to 190 uv.

Added to the capacitive-feedthrough drift would be the drift due to leakage. If at room temperature i_L (max) = 20 pa, then leakage feedthrough = 0.2 uv. This is in phase with the drive voltage and would correspond to a zero offset of 0.4 uv since the chopper gain is 0.5.

At 100°C, i_L (max) has increased to 5 na, so the zero offset would then be 100 uv. This offset is independent of the chopping frequency.

Also affected by temperature is the chopper gain since $r_{ds'}$ varies with temperature. This change can be estimated from the relation $r_{ds'} = 1/g_{fs}$ (g_{fs} is the zero-bias transconductance) and from the estimation that g_{fs} varies -1/2 percent per °C temperature rise. At 100°C, $r_{ds'}$ has risen from 11 K to 19 K producing a chopper gain reduction from 0.46 to 0.35, a drop of 24 percent.

So at 10KC, it should be possible to construct a chopper amplifier with 120 uv zero drift over the temperature range 20°C to 100°C. Gain would be expected to drop about 24 percent.

DIODE-CAPACITOR BALANCE

Further refinements on the fixed-capacitor balance scheme can be realized with the use of a diode capacitor to match the gate-drain capacitance of the FET. Improvement results since both capacitors are voltage variable and also since both change with temperature in the same manner.

The type of capacitor which would best balance the gate-drain capacitance of one FET would be the corresponding capacitance of another FET. A circuit connection which offers a good capacitance balance is shown in Figure 9. With $V_{d2} = -V_{d1}$ and with $C_{gd1} = C_{gd2}$ at all voltages and temperatures, perfect cancellation of capacitive feedthrough would occur.

Cancellation of the leakage feedthrough is also possible with this connection. Thus potentially this connection would offer complete cancellation of both capacitive and leakage feedthroughs.

However, even if two identical FET's were available, differences in the capacitances and the leakages would be expected since the interelectrode voltages on the two transistors are not identical. The gate-drain voltages are identical, but the drain-source voltage of T_1 is nearly zero while the gate-source voltage of T_2 is nearly zero.

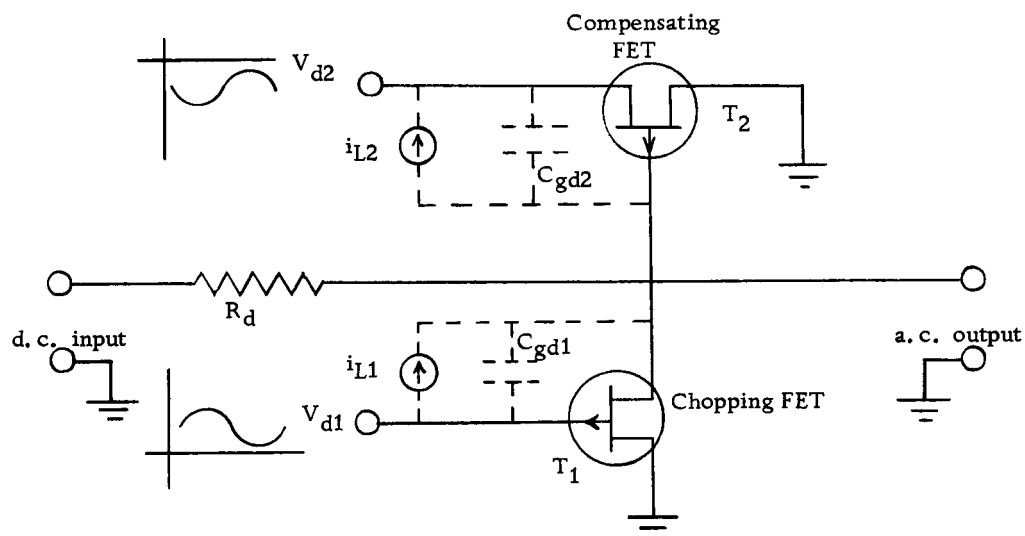


Figure 9. FET chopper with second FET for compensation.

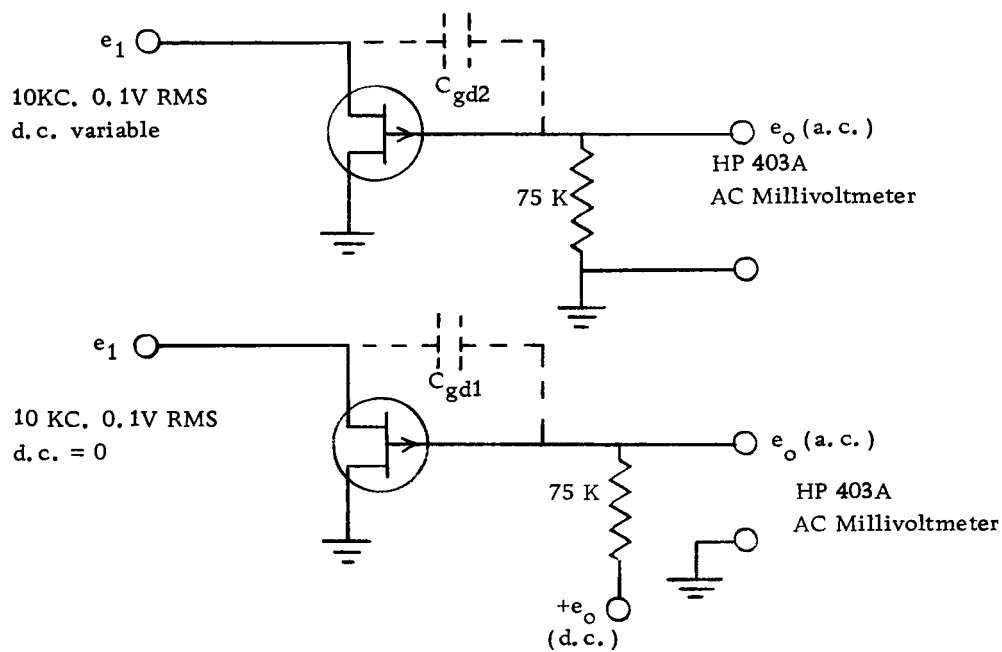


Figure 10. Capacitance Measuring Circuits.

$$C = \frac{e_o(\text{a. c.})}{e_1(\text{a. c.})} \frac{1}{2\pi(10\text{KC})(75\text{K}\Omega)}$$

The capacitances of three transistors were measured under both conditions, using the circuits of Figure 10, and the results indicated that $C_{gd1} = C_{gd2}$ within the accuracy of the measurements (within less than 10 percent).

The leakages under both sets of terminal voltages were also tested, using the circuits of Figure 11. Here also it was found that $i_{L1} = i_{L2}$ to within about 10 percent.

It can therefore be concluded that in order to determine if two transistors will balance, it is necessary to test the transistors under only one of the interelectrode voltage conditions.

If a good match between both capacitance and leakage cannot be found, then an evaluation of the desired application will reveal which is more important to match.

From the analysis of the fixed-capacitor compensated chopper, it was seen that at a 10 KC chopping rate and a 100°C temperature maximum that the expected zero drift would consist of 100 uv by leakage plus about 20 uv by capacitive feedthrough.

Clearly for these conditions of chopping rate and temperature range, the leakage current is most offensive. Therefore, the most noticeable improvements would result from a close match of leakage currents for T_1 and T_2 , this match being most critical at elevated temperatures.

At higher frequencies and less stringent temperature conditions,

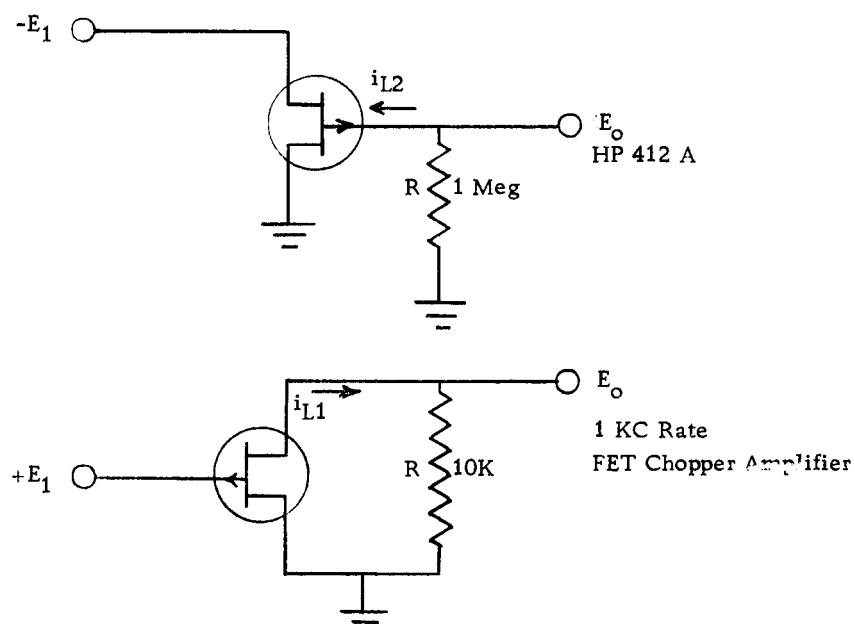


Figure 11. Gate-drain leakage measurement circuits.

$$i_L = \frac{E_o}{R}$$

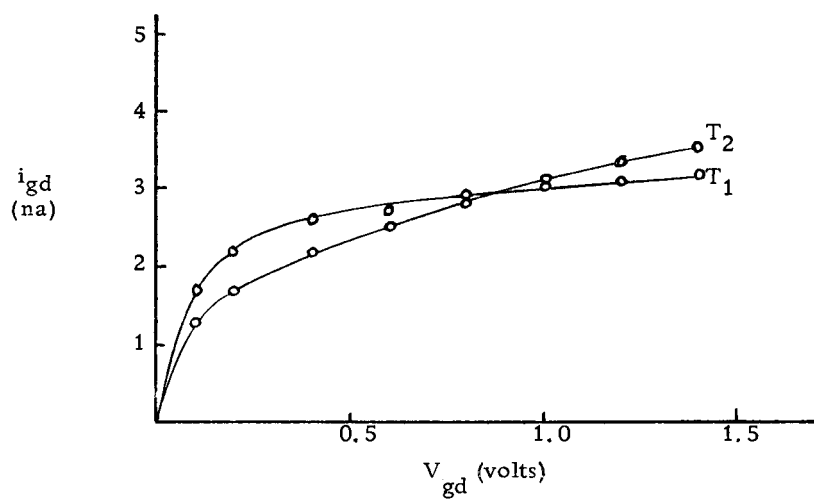


Figure 12. Gate-drain leakage. Currents measured at 100°C .

however, the drift due to capacitive feedthrough would be most important and a good capacitance match would be more important than a good leakage match. However, a capacitance match which is maintained at less than five percent under voltage and temperature variations would be difficult to achieve. Therefore, if the average capacitance difference were at best two percent, the maximum expected reduction of the 1.3 mv of uncompensated capacitive feedthrough at 10 KC would be to 26 uv.

EXPERIMENTAL RESULTS

To verify the above predictions, an uncompensated chopper was constructed with $R_d = 10K$ ohms and with V_d a 10 KC sine wave with a d. c. value of 0.7 volt and a peak-to-peak value of 1.2 volt. The chopping transistor (T_1) had $r_{ds}' = 10K$ ohm and $V_p = 1.1$ volt. Its leakage is shown in Figure 12 and capacitance is shown in Figure 13.

The room temperature feedthrough for this chopper was 900 uv peak-to-peak (Photograph 1). Use of a fixed capacitor for compensation reduced this feedthrough to 50 uv (Photograph 2). The use of a second FET for compensation reduced the feedthrough to about 20 uv (Photograph 3).

The leakage and capacitance of the compensating transistor (T_2) are also shown in Figures 12 and 13. The larger capacitance of T_2 was allowed for by adjusting the amplitude of V_{d2} to produce the best balance.

With the amplitude of V_{d2} set at room temperature, the transistors were placed in a temperature controlled oven. At $100^\circ C$, the feedthrough with fixed-capacitor compensation had increased to 90 uv peak-to-peak (Photograph 4) and the feedthrough for the two-transistor chopper had increased to 40 uv (Photograph 5).

A complete chopper amplifier was constructed as in Figure 14

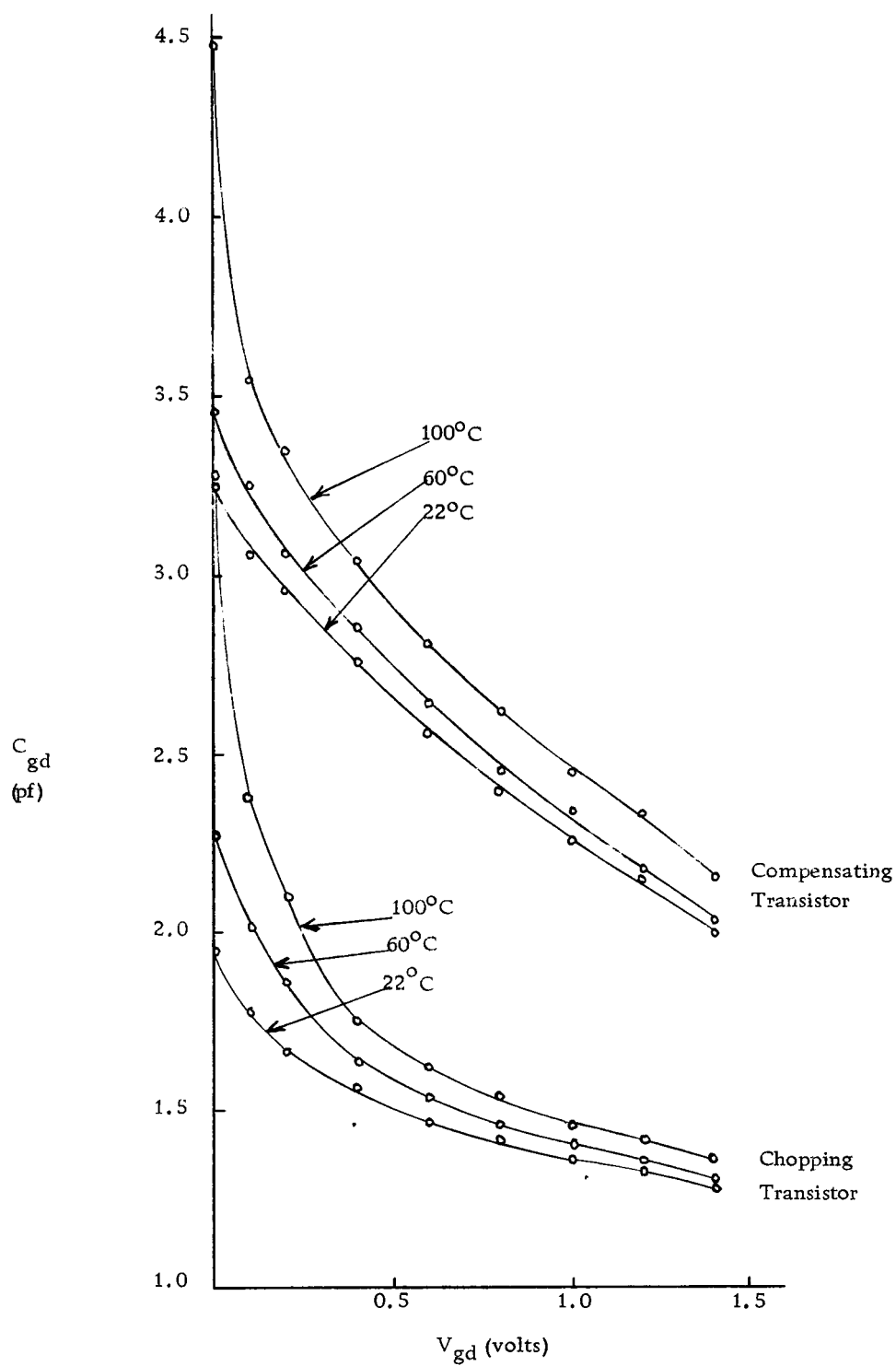
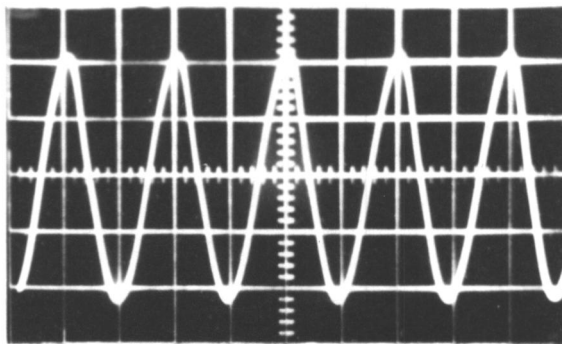
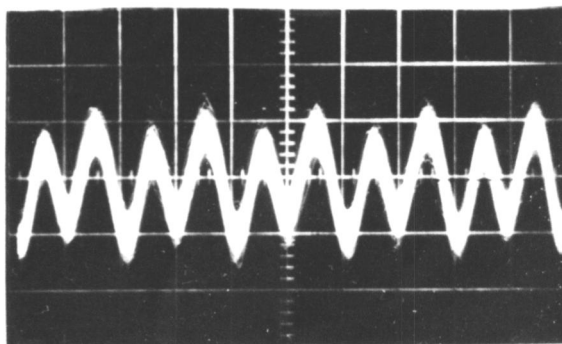


Figure 13. Gate-Drain Capacitance Measurements.



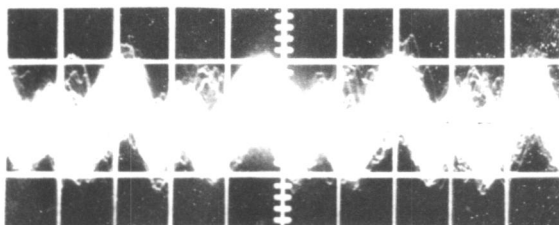
Photograph 1

Uncompensated Capacitive Feedthrough; Room Temperature.
Vertical: 200 uv/div. Horizontal: 50 us/div.



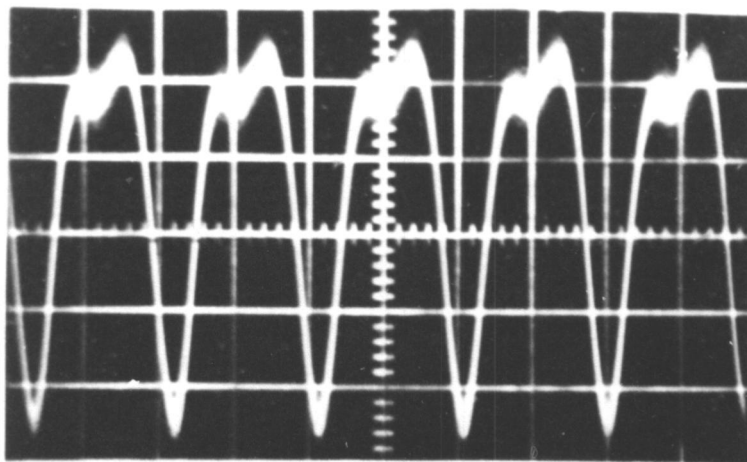
Photograph 2

Feedthrough Balanced with Fixed Capacitor; Room Temperature.
Vertical: 20 uv/div. Horizontal: 50 us/div.

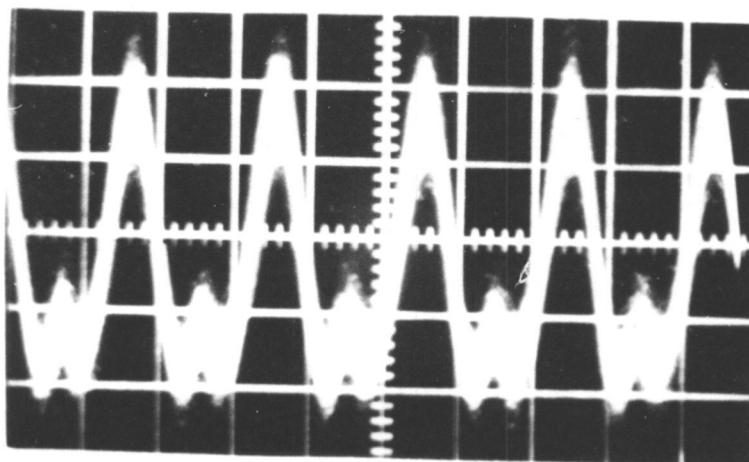


Photograph 3

Feedthrough Balanced with Second FET; Room temperature.
Vertical: 10 uv/div. Horizontal: 50 us/div.



Photograph 4
Fixed-Capacitor Compensation at 100°C.
Vertical: 20 uv/div. Horizontal: 50 us/div.



Photograph 5
Compensation with Second FET at 100°C.
Vertical: 10 uv/div. Horizontal: 50 us/div.

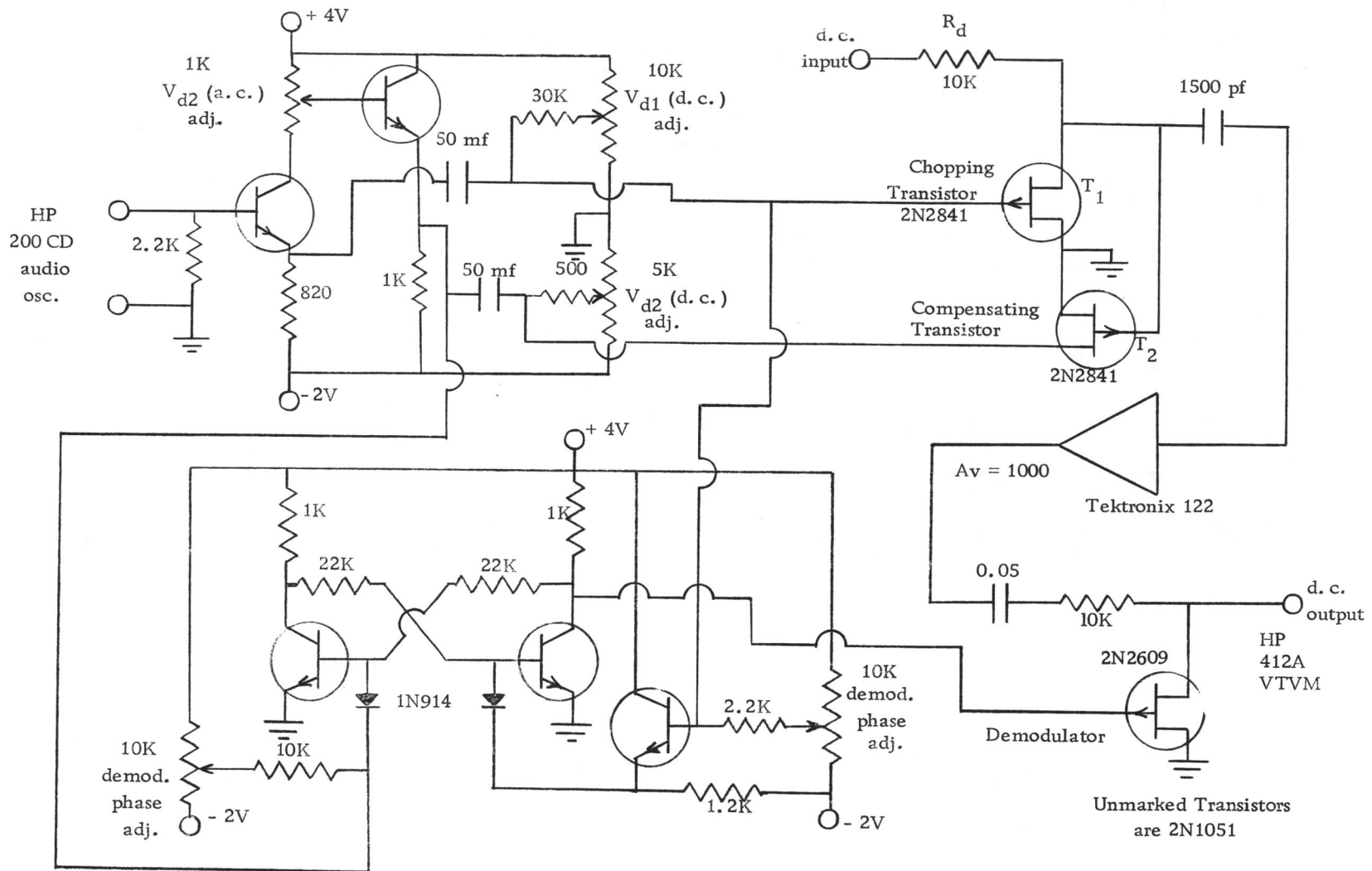


Figure 14. Complete Chopper Amplifier.

with the demodulator timed to compensate for about 15 degrees phase shift in the a. c. amplifier. For fixed-capacitor compensation, T_2 was replaced by a 5 pf fixed capacitor.

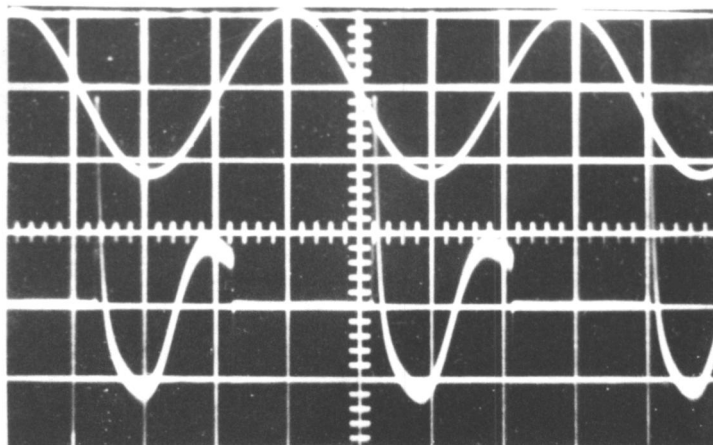
The output of the demodulator at 100° C for the chopper with fixed-capacitor compensation is shown in Photograph 6 and the demodulator output for the two-transistor chopper is shown in Photograph 7. The spikes in these photographs were produced by the demodulator which was driven by a 4 volt square wave. These spikes produced a zero offset at the output but since this offset was constant under the tests made, it had no effect on the drift measurements.

The breadboard and test equipment are shown in Photograph 8.

The d. c. zero drift for the chopper with fixed-capacitor compensation was recorded as 63 uv as referred to the input, while for the two-transistor chopper, zero drift was less than 10 uv.

These drifts can be attributed mainly to leakage effects and the reduction of drift with the two-transistor chopper can be explained by the good match of high temperature leakage currents shown in Figure 12.

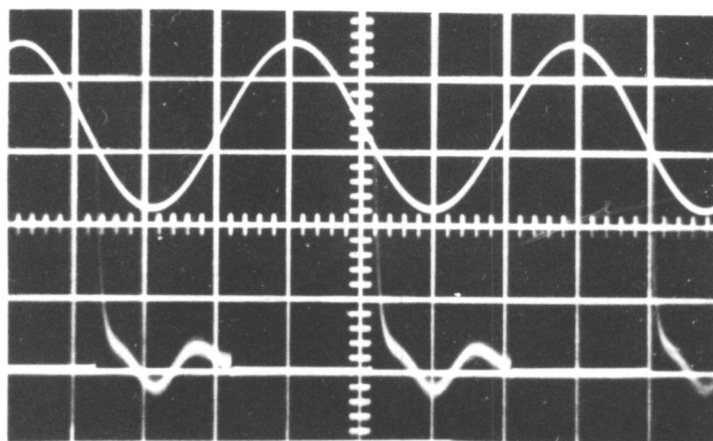
Since the drift is caused mainly by the leakage currents, an increase in the chopping rate would not cause a proportionate increase in zero drift. For example, if the drift at 10 KC were 10 uv, then at 100 KC, a drift of about 40 uv would be expected. However, drift measurements at 100 KC were not possible since a low-noise a. c.



Photograph 6

Demodulator Output at 100°C, Input = 0, Fixed-Capacitor Compensation.
Upper Trace is Drive Voltage.

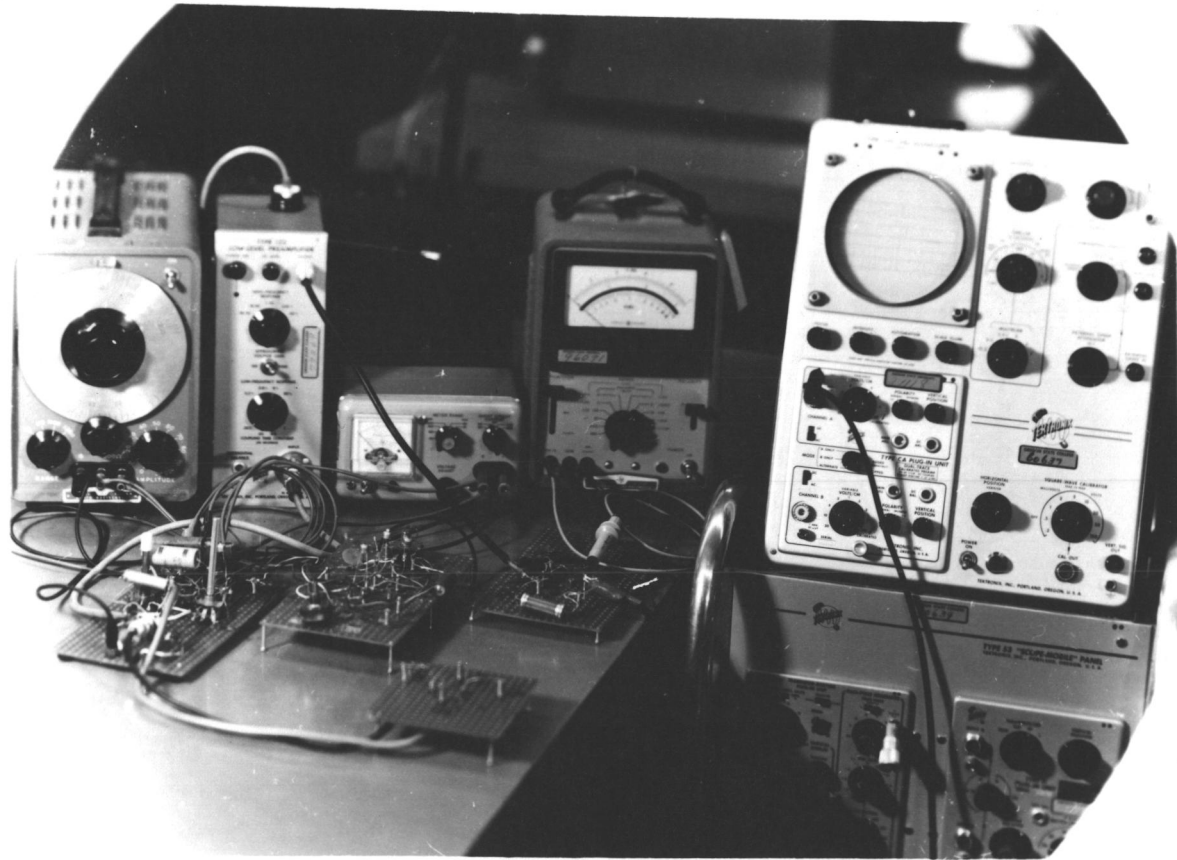
Vertical: 0.5 V/div.
50 mv/div. Horizontal: 25 us/div.



Photograph 7

Demodulator Output at 100°C, Input = 0, Compensation with Second FET.
Upper Trace is Drive Voltage.

Vertical: 0.5 V/div.
50 mv/div. Horizontal: 25 us/div.



Photograph 8
Breadboard and Test Equipment.

amplifier with this bandwidth was not available.

Further observations at 10 KC showed that for both the capacitively compensated amplifier and the two-transistor amplifier, the room temperature gain of 158 dropped to 120 at 100° C. This was the 24 percent gain reduction predicted by the estimation of the increase of the drain-to-source resistance with temperature.

It should be noted that the two-transistor circuit produces drifts under thermal transient conditions which are larger than the 10 uv listed above. Temperature differences between T_1 and T_2 produce capacitance and leakage mismatches which destroy the desired balance and produce drifts. A common heat sink for the two transistors should provide a satisfactory solution to this problem, however.

It should also be noted that the use of an FET as the compensating device is not essential. A standard diode could be used instead if one could be found with capacitances and leakages similar to those of the FET gate diode. Attempts were made to compensate with a 1N914, but large leakage mismatch produced poor results.

SUMMARY AND CONCLUSIONS

A chopper amplifier has been designed and constructed which when operated at a 10 KC chopping rate and over a temperature range 20°C to 100°C has a zero drift of less than 10 uv. However, low drift depends on a critical balance between two components and will suffer under any conditions disturbing this balance.

Providing that a suitable a. c. amplifier were available, the chopping rate could be easily increased to 100 KC with an expected drift increase to about 40 uv, but at this rate and higher frequencies, demodulator synchronization and stability of the drive voltage (V_{d1}) and balancing voltage (V_{d2}) would become more critical.

The FET can be used as a medium-speed chopping device, but the maximum chopping rate is determined by the allowable drift of the zero point.

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