AN ABSTRACT OF THE THESIS OF

Prachee Shree Behera for the degree of Master of Science in Electrical and Computer Engineering presented on September 15, 2005.
Title: A MOSCAP Pipeline Pseudo Passive DAC.

Abstract approved: _____
Gabor C. Temes

The design of a 10-bit pipelined charge redistribution DAC employing MOSCAPs biased in their accumulation mode is presented in this thesis. A switched capacitor filter and output buffer have also been designed for the system. The effect of MOSCAP nonlinearity on the performance of the pipelined charge redistribution DAC has been analyzed. MOS capacitors and their models available for simulation have been discussed. In addition, the effect of more general capacitor nonlinearities on the performance of the DAC has been presented.

A MOSCAP Pipeline Pseudo Passive DAC.

by

Prachee Shree Behera

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented September 15, 2005

Commencement June 2006

Master of Science thesis of Prachee Shree Behera presented on September 15, 2005.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

---

Director of the School of Electrical Engineering and Computer Science

---

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Prachee Shree Behera, Author

ACKNOWLEDGEMENTS

I have a lot of reverence for the institutions of education that form the foundation of my life and career. At my high school St Joseph's Convent, I learnt life's littlest and greatest lessons, that guide me through every day. University College of Engineering introduced me to electronics, provided me with an opportunity to know and interact with a medley of people and developed in me the confidence to deal with any kind challenge in life. At Oregon State University the gates to the magical world of circuits were opened for me. OSU gave me the opportunity to meet people from all over the world and know about their cultures, pitted me against some of the smartest people and taught me that there will always be so much to learn…

I would like to take this opportunity to express my gratitude towards all my well-wishers who have helped me reach this milestone in life.

First and foremost I thank Dr. Gabor C. Temes for entrusting me with this project and for guiding and helping me throughout my Master's program. I have learnt a lot about circuit design from his excellent lectures and courses assignments.

I thank Dr. Un-Ku Moon, Dr. Karti Mayaram and Dr. Huaping Liu for the exciting course lectures and challenging assignments and projects.

Dr. Raghu Settaluri, Prof. Roger Traylor and Dr. Shoichi Kimura agreed to serve on my examining committee at a short notice, my sincerest thanks to them.

Everyone at EECS Office was most helpful when I first came to Corvallis and also there after. I appreciate the staff who make things so smooth and easy for all students, especially Ferne who always goes out of her way to help.

I am also grateful to Dr. Ken Suyama and Dr. Alexander Dec for providing me with the opportunity to work at Epoch microelectronics. In addition to a lot of practical experience, I learned a lot from several useful discussions with them during my short stay at Epoch.

Culture-shock and home sickness weren't problems I faced at Corvallis because of all my friends at OSU, mostly "related to" DB211. I thank them all for their help, encouragement and camaraderie.

Perhaps my life's greatest influence has been and always will be my family. I wouldn't have been molded into what I am today if my parents, grandparents, brother and all my extended family were any different. My thanks, to my parents for their constant belief in me and my choices. My gratitude, towards my grandparents for their love, guidance and blessings. My thanks also, to my uncles and aunts and cousins at Bombay and at Maryland for their love and support during my career.

My sincere gratitude also, to my in-laws in the US and in India for their exuberance during and after my wedding, which took place during the middle of my Masters. My utmost thanks to my parents-in-law for being so warm and understanding at all times.

I don't believe I would be writing this today had it not been for the presence of a never ending source of love, understanding, optimism and encouragement in my life. My truest friend for the last 11 years has helped me make the most of life's ups and pull through its downs. For my husband Manas, an oft thought-of but least spoken word-thanks-for simply, everything.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

A MOSCAP PIPELINE PASSIVE DAC

1. INTRODUCTION

1.1 Motivation

Ever evolving modern communication systems are simultaneously striving for higher performance and smaller circuitry. Data converter designers are constantly challenged to develop circuits for scaling technologies, while still preserving high precision. The chip size, or in other words the area occupied by the circuit elements, is a key determining factor for the cost of the chip. The highest occupants of the chip area in data converter circuits are passive components like capacitors. In order to minimize area, high density capacitors can be realized employing contemporary technologies. However, there is always a trade-off between the density of a realizable on-chip capacitor and its linearity. To meet the demands of linearity structures like metal-insulator-metal (MIM) have been the capacitors of choice.

MOS capacitors (MOSCAPs) have the highest reported capacitor densities, and are readily available in standard digital CMOS fabrication processes. These devices have good control of the absolute value of the capacitance and also

excellent matching between adjacent capacitors. The voltage dependent nonlinearity of MOSCAPs however, deems it unsuitable for circuits where low distortion is important.

In this research the effects of MOSCAP nonlinearity on the performance of a pipeline charge redistribution digital to analog converter (Q-DAC) have been investigated. The Q-DAC was first presented in [1/1] and employs an array of equal valued capacitors at its core. The Q-DAC has previously been designed for high frequency RF applications such as GSM transceivers [1/2] [1/3]. Recent improvements in the design and layout of the DAC results in very high performance (70dB SFDR and 9.7 ENOB), as reported in [1/4].

In previous chip implementations of the Q-DAC, the preferred choice for capacitors has been poly-poly [1/2] or metal-insulator-metal (MIM) capacitors [1/4], as linearity of the system has always been an issue. The area occupied by the array of capacitors at the core of the Q-DAC has been the dominant size determining factor in these chip implementations. The number of capacitors in the Q-DAC and, therefore, the area occupied is directly proportional to its resolution, N (bits). Therefore, high density capacitors need to be used in high resolution Q-DAC implementations to limit area. Another important consideration for high resolution Q-DAC circuits is percentage mismatch between capacitors. Through the use of MOSCAPs, the area reduction can be significant. The percentage mismatch between capacitors can also be reduced, which is desirable for high

resolution converters. However, the drawback of employing MOSCAPs lies in the degradation of the linearity.

In this research the linearity degradation due to nonlinear capacitors used in the Q-DAC is discussed. Simulation results have been presented.

1.2 System specifications

A 10-bit 1MS/s pipelined charge redistribution DAC is designed for audio frequencies in this research. A low pass switched capacitor smoothing filter clocked at 2 MHz is designed as the next stage to the DAC.

1.3 Thesis organization

This thesis has been organized into six chapters. This chapter, Chapter 1, gives a brief introduction of the purpose of the work presented and the motivation behind the research.

In Chapter 2, a description of the working principle of the Q-DAC has been presented. The advantages and limitations have also been discussed.

Capacitors available in CMOS technologies have been discussed in Chapter 3. The working of MOSCAPs and the models available for their simulation

have been analyzed. In addition, the modeling of a more general nonlinear capacitor for simulation has been explained.

Chapter 4 has been dedicated to the detailed discussion of the low-pass filter and the output buffer designed for the DAC. Some relevant theory, the design procedure and the final performance of the designed filter and the output buffer have been provided.

The circuit design details involved in the DAC have been presented in Chapter 5. The design of the operational amplifier (OPAMP) used in the low-pass filter has also been described in this chapter.

The results achieved through simulations and their relevance has been presented in Chapter 6. Chapter 7 is the concluding chapter and provides a summary and suggestions for further research in this project.

2. THEORETICAL BACKGROUND

2.1 Digital-to-analog converters (DACs)

Evolving digital signal processing (DSP) technologies, as well as emerging systems-on-a-chip implementations due to very-large-scale-integration (VLSI) have taken signal processing in digital domain to new heights. The exploding market for digital communications has been one of the outcomes of these advancements.

The same phenomenal changes in the digital domain have also renewed the interest in data converter circuits. Digital-to analog converters (DACs) or more generally data converters are interface circuits in many applications, including digital communications. The performance of the integrated circuits (ICs) designed for communications applications are sometimes decided by the limitations of the implementable DAC architectures. Hence, there is an ever increasing demand for high speed, high performance DAC architectures. Some performance parameters are explained below.

2.1.1 Offset and gain errors

The output of a non-ideal DAC differs from that of an ideal DAC by a finite error term. Figure 2.1 shows the deviation of a non ideal DAC output from that of an ideal DAC. This deviation can be differentiated into gain and offset errors and also differential and integral nonlinearity errors. The *absolute accuracy* of the DAC depends on the sum of the offset, gain and the linearity errors [2/1].

Offset error is the analog non-zero output measured when the digital input to the DAC is all zeros. Offset error usually remains constant for all input codes.

Gain errors appear as a change in the slope of the DAC output. The error is not constant for all input values, but scales with a constant ratio. Neither gain nor offset errors contribute to the nonlinearity of the system and are usually caused by switch charge injection, finite amplifier gain etc.

2.1.2 INL and DNL errors

The nonlinearity errors contribute towards the *relative accuracy* of the DAC and are measured after gain and offset errors are removed from the actual output.

Integral nonlinearity (INL) is a measure of the deviation of the output from a straight line (when input is a ramp). It is caused by the error in the

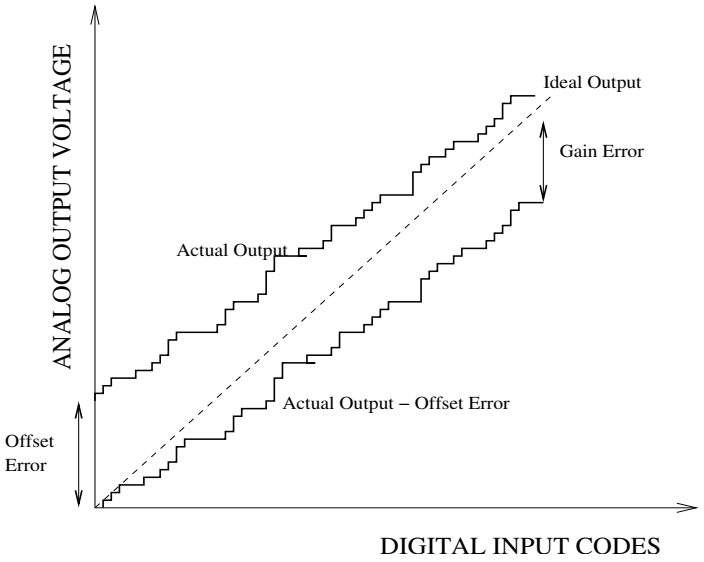


Figure 2.1: Offset and gain errors.

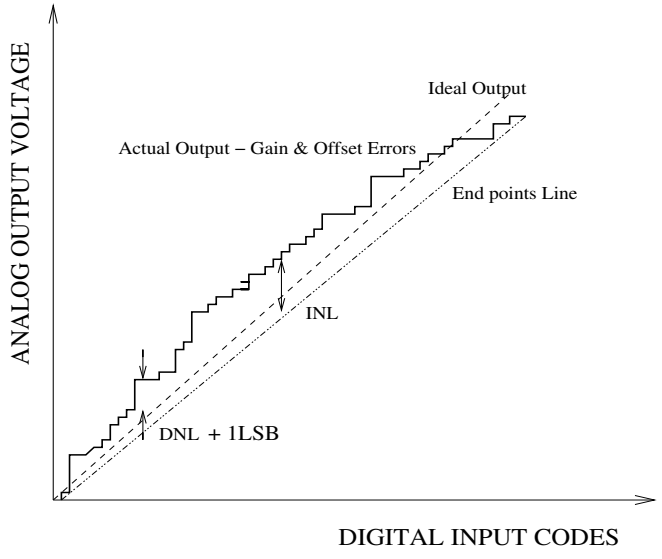


Figure 2.2: INL and DNL errors.

transition points of the codes. To estimate the INL, the absolute difference of the actual output from the expected straight line is expressed as number of LSBs. For an N-bit data converter, 1LSB or least significant bit is defined as$1/2^N$. The ideal straight line for the estimation is the best fit straight line for the output values. Usually the minimum and maximum values of the DAC output are used to define the straight line, in which case the line is said to have been determined by endpoints method. The presence of INL errors can result in adding harmonic distortion to the DAC's output.

Ideally a digital code change from one value to the next consecutive value should result in a change of 1LSB in the DAC's output. In reality there is a variation in the analog step sizes of the output for consecutive codes. This error is expressed as differential nonlinearity (DNL) error. The effect of DNL is to add noise or spurs to an ideal transfer function, thus reducing the accuracy of the converter. Figure 2.2 shows the graphical representation of INL and DNL errors.

2.1.3 Signal-to-noise ratio (SNR) and effective number of bits (ENOB)

It can be shown that for a sinusoidal waveform, there is maximum achievable SNR for a DAC due to the effects of quantization errors. This maximum value, SNRmax is determined by the resolution, N (bits) of the DAC, and the over-sampling ratio (OSR) of the system. The SNRmax in dB can be expressed as,

$$SNR_{max} = 6.02\ N\ (bits) + 1.76 + 10\ \log(\ OSR\ )$$

$$OSR = f_s / 2 f_0$$

The over-sampling ratio, OSR is the ratio of the sampling frequency f_s of the system and the Nyquist rate, which is defined as twice the highest frequency component in the input signal.

The performance of a non-ideal DAC is often expressed as a effective number of bits (ENOB) which is simply back calculated from the SNR formula,

$$ENOB = \frac{[SNR_{achieved} - 1.76 - 10\ \log(\ OSR\ )]}{6.02}$$

Needless to say, ENOB in a real DAC will always be less that the resolution N (bits) of the DAC and its value will be a measure of the accuracy of conversion.

2.2 Charge redistribution DAC (Q-DAC)

Passive charge redistribution DAC was first presented in [2/2]. Similar architectures have been reported in high speed communication applications [2/3] [2/4]. The prime advantages of charge redistribution DAC architecture over its more common current steering counterpart are better linearity and reduced area requirements.

The Q-DAC employs an array of equal valued capacitors at its core. The number of capacitors in the Q-DAC bears a linear relationship with its resolution. This is in contrast with current steering architectures where the number of current sources increases exponentially with resolution [2/3]. When compared with capacitor arrays with binary weighted schemes, the area reduction for higher resolutions can be large.

The Q-DAC architecture, explained in the following section, is such that it does not suffer from harmonic distortion resulting from "glitches" in the output waveform. "Glitches" are sudden changes in the analog output of the DAC, often caused by unequal propagation delays in the switches [2/3]. Most traditional DAC architectures, like binary and thermometer-coded current steering architectures suffer from glitches. These glitches may or may not depend on the DAC input word. When the glitch energy is not dependent on the overall DAC word it contributes to nonlinear distortion in the system. The elimination of this distortion leads to a higher order filter implementation, hence increasing power, cost and area requirements [2/5].

In case of the Q-DAC the digital word is reflected in the charges stored in an array of capacitors. These charges are combined and the final charge stored in the MSB capacitor is taken as the output analog signal. Thus glitch related distortion is eliminated as there is no need for synchronization of clock timings for charge delivery of individual bits.

2.3 Working principle of the charge redistribution DAC

As mentioned previously, the core of the charge redistribution digital-to-analog (Q-DAC) consists of an array of equal valued capacitors and active switches and operates on the theory of successive charge bisection. A three phase non-overlapping clock is required for the timing operation of the DAC. The implementation and design of the three phase clock, logic controls and the switches will be discussed in more detail in Chapter 5.

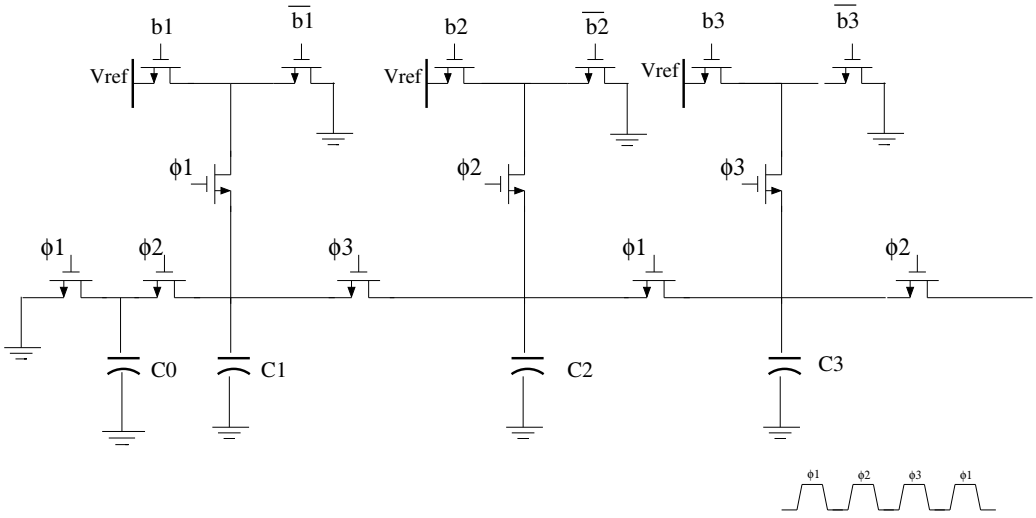


Figure 2.3: Circuit diagram of 3-bit DAC.

2.3.1 3-bit Q-DAC

In order to describe the theory of conversion by bisection a three bit DAC has been considered as shown in Figure 2.3 [2/2]. The three phase clock {Φ1,

Φ_2, $\Phi 3\}$ has been shown as an insert in Figure 2.3. Capacitors Ci, i=0-3 are equal valued, say equal to C.

During phase Φ_1 capacitor C0 is discharged, and capacitor C1 is charged to Vref or zero depending on whether b1 (LSB) is high or low. In the next phase Φ_2 the charges stored in C0 and C1 are re-distributed equally. Therefore at the end of Φ_2 the charge in both C0 and C1 is half of the total charge before redistribution. During phase Φ_2 capacitor C2 is simultaneously charged to Vref $_{or}$ zero depending on b2. The next phase Φ_3, results in the charge sharing between capacitors C1 and C2 and the pre-charging of capacitor C3 in accordance with b3. This sequence of charging and charge bisection continues till the end of Φ_1 of the next cycle. At the end of Φ_1, the charge, Q_3 stored in C3 (MSB capacitor in this case), is the analog equivalent of the digital bit sequence applied to the DAC (b1, b2, b3).

$$Q_3 = (\frac{b1}{2^3} + \frac{b2}{2^2} + \frac{b3}{2})Vref \times C$$

The charges stored in capacitors C0, C1, C2 and C3 at the end of each phase are illustrated in Table 1 for the bit sequences b1=0, b2=0, b3=1 followed by b1=1, b2=1, b3=1 where b3 is the most significant bit (MSB). It can be seen that during Φ_2 of the first cycle the charge stored in C3 is C x Vref/2, which is the analog equivalent of digital code 100. Similarly at the end of Φ_1 of the third cycle, the output will be proportional to 7/8Vref which is the analog equivalent for a 3 bit digital code of 111.

Table 2.1: Charges stored in Q-DAC capacitors during different phases of the clock.

		C0	**C1**	**C2**	**C3**
First Cycle	Φ_1	0	0	-	-
	Φ_2	0	0	0	-
	Φ_3	0	0	0	Vref x C
Second Cycle	Φ_1	0	Vref x C	½ Vref x C	½ Vref x C
	Φ_2	½ Vref x C	½ Vref x C	Vref x C	½ Vref x C
	Φ_3	½ Vref x C	¾ Vref x C	¾ Vref x C	Vref x C
Third Cycle	Φ_1	0	-	⅞ Vref x C	⅞Vref x C
	Φ_2	-	-	-	⅞ Vref x C

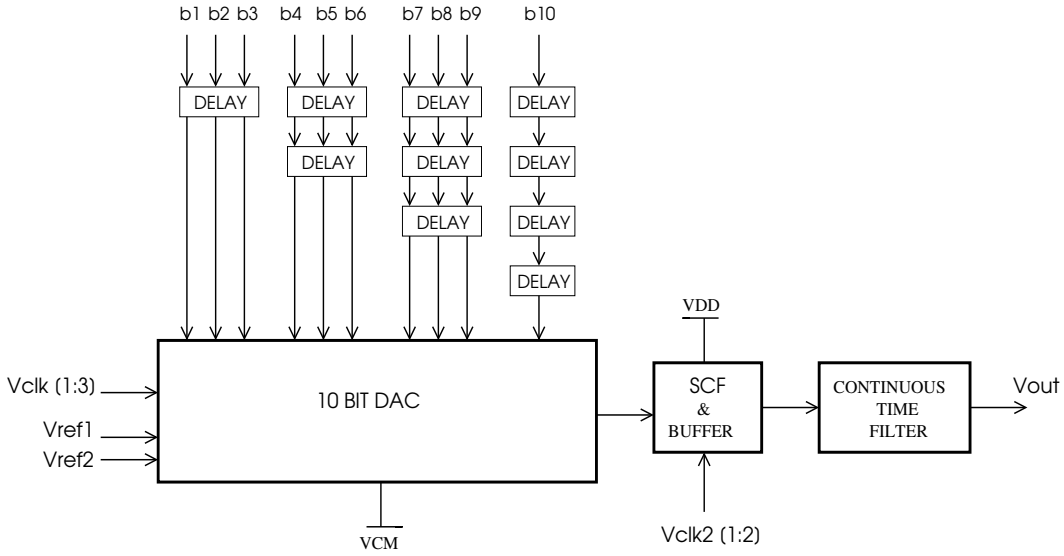


Figure 2.4: System block diagram of pipelined Q-DAC.

2.3.2 Pipelined N-bit Q-DAC

The modular nature of the Q-DAC enables pipelining operation. Any N-bit Q-DAC can thus be composed by cascading 3-bit DAC structures followed by a 1-bit or 2-bit structure if required. Each 3-bit DAC can then be operated by 3-bits of a different digital word and hence the output of the DAC can be updated every clock cycle.

Pipelining requires the use of shift-register arrays for introducing appropriate time delays to the bit sequences. Due to the introduction of these delay elements there is a $(N+2)xT_1$ time delay, (where T_1 is the time duration of each phase of the DAC clock) between the entry of the digital word and the appearance of its analog equivalent at the MSB capacitor. The block diagram of a 10-bit pipelined DAC is shown as a cascade of 3-bit DACs in Figure 2.4.

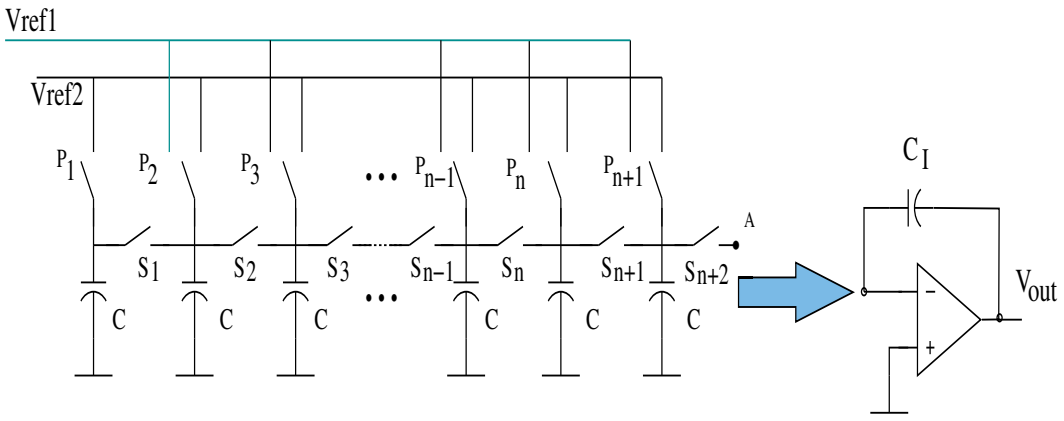


Figure 2.5: General pipelined Q-DAC.

In the more general form of the differential pipelined Q-DAC the two reference voltages can be Vref1 (high) and Vref2 (low) and the common mode of the DAC can be different from zero. A part of the differential N-bit DAC has been shown in Figure 2.5 [2/3]. The other half of the differential structure will be identical and will be operated by bit complements of the digital input word.

The operation is similarly to that of the 3-bit structure described above. The switches, S_1, S_2 etc are "ON" during the phases Φ_1, Φ_2 respectively. The switches P_is are operated by logic combinations of the phases and the bit sequence. For example P_1 is "ON" (connected to Vref1) when both Φ_1 and b1 are high and P_1 is "OFF" (connected to Vref2) when Φ_1 is high but b1 is low.

The output charge, Q^+ at node A after N pre-charge and bisection operations can be expressed as [2/3],

$$Q_A^+ = CV_{ref\ 2} + \frac{C\,(V_{ref\ 2} - V_{ref\ 1})}{2} \sum_i^N b_i \,/\, 2^{N-i}$$

Similarly the output charge for the other portion of the DAC can be shown to be [2/3],

$$Q_A^- = CV_{ref\ 2} + \frac{C\,(V_{ref\ 1} - V_{ref\ 2})}{2} \sum_i^N b_i \,/\, 2^{N-i}$$

$$v_A = (Q_A^+ - Q_A^-) \,/\, C = (V_{ref\ 1} - V_{ref\ 2}) \sum_i^N b_i \,/\, 2^{N-i}$$

If the capacitors C in the DAC are linear, the voltage at node A can simply be given by v_A,

However if the capacitors are nonlinear the above relation is no longer accurate. The analog equivalent of the digital word is only represented by the differential charges in the MSB capacitors. The output charge packets can be converted into a continuous time voltage through an amplifier circuit as represented in Figure 2.5. The accuracy of the conversion depends on linearity of the "ideal" capacitor C_I as shown in the Figure 2.5. The output voltage V_{out}, of the amplifier is then a scaled version of v_A.

2.4 Accuracy considerations in Q-DACs

As discussed previously the circuit non-idealities result in limitations in the DAC performance. Some circuit issues, related to the charge redistribution DAC have been discussed below.

2.4.1 Capacitor non-idealities

Matching of the unit capacitors in the Q-DAC is important in order for accurate charge bisection which in turn affects system performance. In addition associated parasitics as well as voltage and temperature dependence of capacitors play an important role in data converters in general. Capacitor structures will be discussed in detail in Chapter 4.

2.4.2 Switch issues

Switches are the next most important components in the Q-DAC. The non-idealities of switches include channel resistance, charge injection and clock feed-through [2/1]. The switches need to be designed such that there are no settling time problems due to their "ON" resistance. In Chapter 5, the design details of the switches in the system have been presented.

2.4.3 OPAMP considerations

Other limitations in the Q-DAC are due to the non-idealities in the amplifier employed in the filter and buffer (which are intermediate steps before the continuous time analog output is generated). In addition to power consumption due to the amplifier, finite OPAMP bandwidth restricts the conversion speeds. Also finite gain and OPAMP slewing contribute to the overall nonlinearities. Details about the amplifier design are presented in Chapter 5.

3. NONLINEAR CAPACITORS IN CMOS TECHNOLOGY

3.1 Capacitors in CMOS circuits

Capacitors are essential building blocks in integrated circuits. Depending on the application of the circuit, different performance parameters of capacitors come into consideration. In radio frequency (RF) applications capacitors are judged by large quality factors, self-resonance frequencies, large break-down voltages and linearity. For analog or mixed signal applications, such as sample and hold circuits, data converters, switched capacitor filters and continuous time filters, capacitor issues such as linearity, parasitic capacitances, matching, as well as the tolerance on the absolute value of the capacitor are major concerns. In mixed mode circuits the digital portions can always be designed in standard low cost CMOS processes. The analog portion, which usually includes linear capacitors, dictates special fabrication processes for the entire chip. The area consumed by the capacitors is also a large percentage of the chip area. Hence the choice of capacitor structures greatly affects both the performance and the cost of chips.

Many integrated circuits (ICs) involving analog blocks are implemented in double poly silicon (poly) fabrication processes. This facilitates the

realization of efficient poly-poly (or double-poly) capacitor structures [3/1]]. Poly-poly capacitors have the advantage of high linearity and high densities. However, the extra layer of poly silicon increases the cost of fabrication significantly.

In single-poly processes metal-insulator-metal (MIM) or metal-poly structures are used as capacitors. These capacitors demonstrate very good voltage and temperature coefficients and quality factors. However, the thick oxide layer (insulator) in these structures not only results in a low unit capacitance (low density), but also leads to large parasitics [3/2].

Multiple metal layers are now available in many CMOS processes. Using top metal layers can help lower the associated parasitics with metal capacitor structures. Also area reduction can be brought about by special processing steps [3/3]. However, multiple metal layers and special fabrication techniques both translate to high costs for realization of chips. Additionally, the vertical spacing between metal layers does not shrink as fast as the lateral spacing in chips (due to reducing channel lengths). Therefore, these devices do not scale with technology.

CMOS capacitor structures also include the capacitors realized between the poly layer and the n-well or p-substrate layer in CMOS technologies. The voltage dependence of these structures, MOS capacitors (MOSCAPs) limits their use in high precision circuits like data converters. Additionally MOSCAPs have considerable temperature and process dependence, require a dc bias and can handle only limited voltage swings due to their nonlinearity. This makes the MOSCAPs less preferable as compared to the other capacitor structures mentioned above.

Interestingly, MOSCAPs have the highest reported capacitor densities. In TSMC 0.35µm process the unit capacitance per area for a MOSCAP structure is close to 4.5fF/µm^2, which is three times that of the unit capacitance realized through poly-poly structures and more than 100 times that realized using metal-metal layers. Additionally, MOSCAPs are naturally available in all standard CMOS technologies. Therefore, MOSCAPs provide a very low cost alternative, if the effects of nonlinearity associated with them can somehow be mitigated.

3.2 MOS capacitors (MOSCAPs)

The MOS capacitor structure as shown in Figure 3.1 can be simply a layer of silicon dioxide sandwiched between a heavily doped layer of poly-silicon, acting as one plate (gate), and the n-type or p-type substrate acting as the other plate of the capacitor (bulk). The capacitance realized through this structure is a function of the voltage applied to the gate with respect to the bulk, V_{GB}.

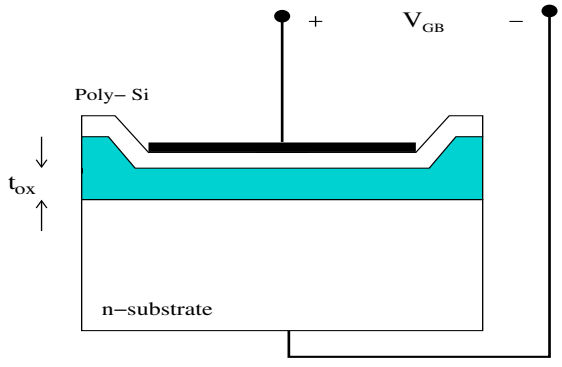


Figure 3.1: Structure of a MOS capacitor.

The operation of the MOS capacitor can be explained through three major physical phenomena, according to which the three regions of operation are accumulation, depletion and inversion. The accumulation region is formed by the accumulation of the majority carriers (of the bulk), at the oxide surface. Thus when a positive voltage is applied to the gate terminal of a MOSCAP with an n-type substrate there is an accumulation of electrons at the oxide surface. The number of electrons accumulated is proportional to the positive potential at the gate terminal. The capacitance per unit area at this region is simply the oxide capacitance C_{ox} and is given by,

$$C_{accumulation} = C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

where, ε_{ox} is the oxide permittivity in Fcm^{-1} and t_{ox} is the oxide thickness in cm, as denoted in Figure 3.1. The oxide capacitance per unit area, C_{ox} is process dependent and can be calculated from the process model parameters.

Depletion region is brought about by the depletion of the majority charge carriers near the oxide layer, leaving behind a space charge region. This space charge region is positively charged, in the case of n-type substrate MOS structure. The depletion charge capacitance also depends on the gate-bulk voltage, V_{GB} and is given by,

$$C_D(V_{GB}) = \frac{\varepsilon_{Si}}{x_d(V_{GB})}$$

where, ε_{Si} is the permittivity in Fcm^{-1} of silicon and x_d is the thickness in cm of the depleted silicon layer. The depletion charge capacitance per unit area, C_D behaves like a capacitor in series with the oxide capacitance per unit area C_{OX}, to form the total capacitance per unit area in the depletion mode, $C_{depletion}$. The depleted silicon layer thickness is directly proportional to V_{GB} and thus capacitance C_D and $C_{depletion}$ are inversely proportional to the gate-bulk voltage V_{GB}.

$$C_{depletion} = \frac{C_{OX} C_D}{C_{OX} + C_D}$$

The inversion region is created if the gate-bulk potential $V_{GB,}$ crosses the threshold voltage (V_{th}) of the semiconductor, for the n-type substrate if V_{GB} decreases below V_{th}. This change in potential results in the minority carriers of the bulk accumulating at the oxide surface. The minority carriers are generated in the depleted silicon layer. In the case of n-type substrate holes are formed in the depleted layer.

At the onset of inversion these holes, minority carriers in this case, rise to the oxide, thus inverting the conductivity type. Holes can also migrate from any p-doped regions close by. The inversion layer capacitance at low frequencies is given by

$$C_{inversion} = C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

In the case of high frequencies, the generation of minority carriers in the depletion region is not fast enough to form an inversion layer. Hence, after the depletion layer thickness reaches its maximum value, any change in the gate voltage V_{GB} does not result in a change of capacitance.

The nonlinear voltage dependence of MOS capacitors can be demonstrated by the C-V characteristics [Figure 3.2] of a unit nMOS structure similar to the one shown in Figure 3.1. In this case, as V_{GB} decreases, the capacitance goes from a maximum value of C_{OX} in the accumulation region, to C_{OX} in series with the depletion capacitance C_D in the depletion region, and then again to C_{OX} in the inversion region.

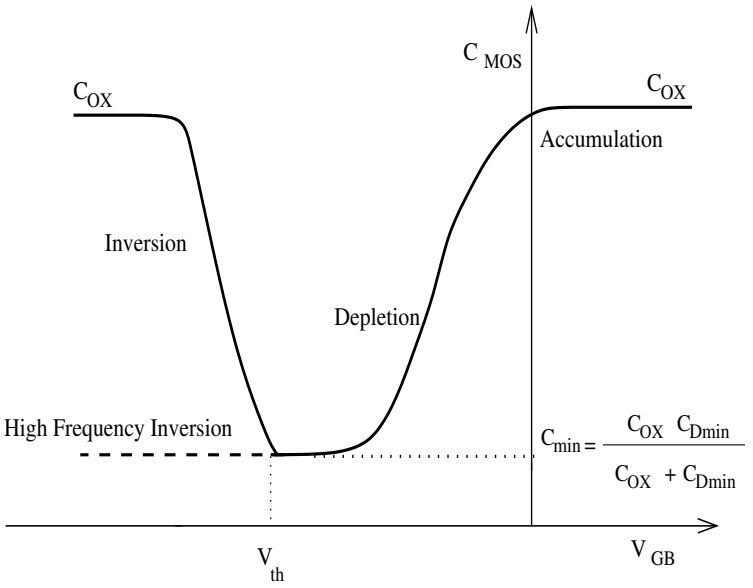
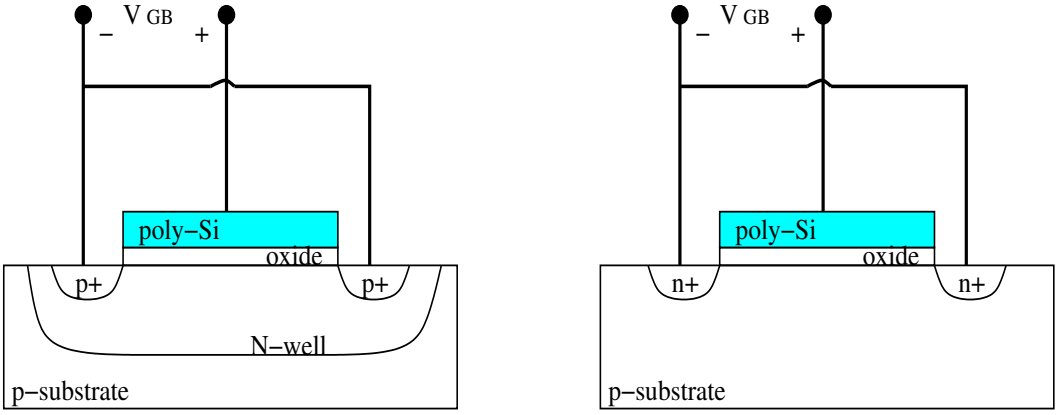
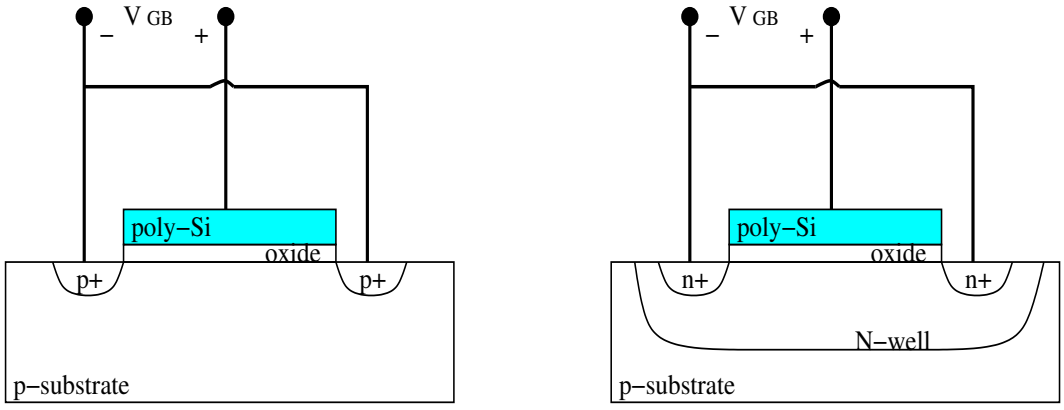


Figure 3.2: C-V characteristics of a MOS capacitor with n-type substrate.



(a) (b)

Figure 3.3: Structures of inversion mode MOSCAPs in CMOS processes.



(a) (b)

Figure 3.4: Structures of accumulation mode MOSCAPs in CMOS processes.

3.2.1 Inversion mode MOSCAPs

Two MOSCAP structures available for inversion mode operation in CMOS technologies are shown in Figures 3.3 (a) and (b) [3/4]. The heavily doped p+ regions in (a) provide the holes, during inversion, when V_{GB} drops below the threshold voltage on the n-well. For positive V_{GB}, the structure in (b) can be used, in which inversion occurs when V_{GB} exceeds the threshold voltage.

In inversion mode capacitors, the bulk of the device is biased such that the p-n junctions are always reverse-biased. Thus, accumulation of majority carriers at the oxide surface is prevented.

3.2.2 Accumulation mode MOSCAPs

MOSCAP structures available for accumulation mode operation in CMOS technologies are shown in Figures 3.4 (a) and (b) [3/4]. The doping profile of these structures prevents the MOSCAP from entering the undesired inversion mode. The structure shown in Figure 3.4 (b) is appropriate if only positive values of V_{GB} are dictated by the circuit requirements.

It has been shown that accumulation mode capacitors results in less distortion than inversion mode capacitors. Also the properties of accumulation mode MOSCAPs are comparatively consistent across different technologies and

hence more universal [3/4]. Therefore, operating in accumulation mode is preferable to that in inversion mode.

3.3 Modeling of MOSCAPs

The MOSCAPs described in the previous section have, unfortunately, no accurate model for simulation in Spectre. However the MOS transistor model, similar to the one depicted in Figure 3.2, can be operated as a capacitor, with the gate and bulk as the two plates of the MOSCAP and the source-drain sections tied. Appropriate biasing and voltage swings applied across the gate and the bulk terminals are of course mandatory. An investigation of the characteristics of the MOS capacitor model as incorporated into the transistor is discussed below [3/5].

3.3.1 BSIM3 model for gate capacitance in MOS transistors

The capacitor modeling in the MOSFET for BSIM version3 model used for simulations in Spectre has been analyzed here for both the nMOS and pMOS cases. The circuit employed for these simulations is similar to the one shown in Figure 3.5. The capacitance is the total capacitance as seen from the gate terminal. The dimension for the nMOS and pMOS devices used for these

simulations are 1µm/1µm. The gate terminal has been assumed to be connected to the circuit and the source and drain terminals are shorted.

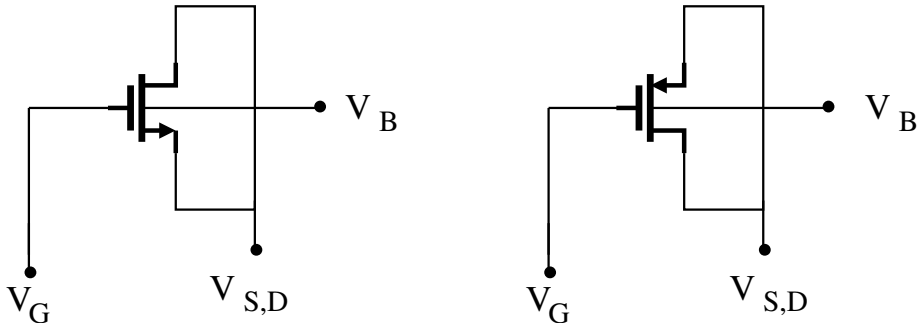


Figure 3.5: Circuit used for generation of C-V characteristics.

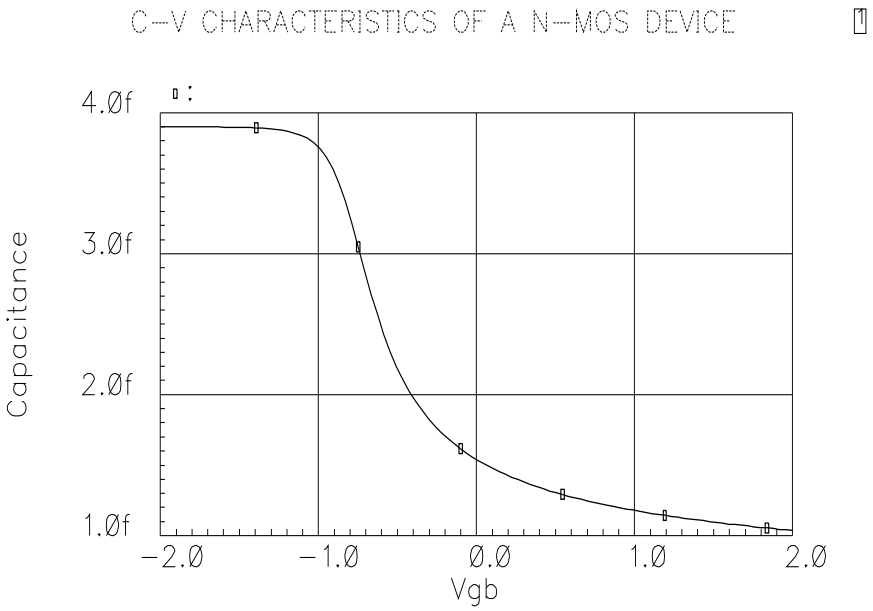


Figure 3.6: C-V characteristics of n-MOS device in accumulation mode.

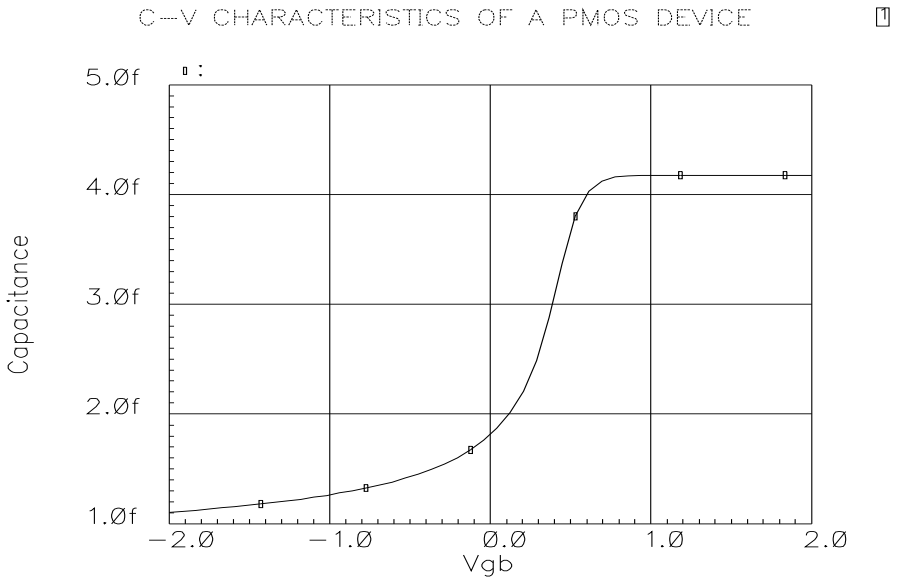


Figure 3.7: C-V characteristic of p-MOS device in accumulation mode.

In the first case the drain-source terminals are connected to the appropriate bias such that the p-n junctions are always reverse biased and thus the transistor never turns "ON". The bulk terminal has been used as the control terminal, for establishing the capacitance of the device. The bulk voltage has been swept such that the gate-bulk voltage V_{GB} for the devices varies from -2 V to +2 V. The C-V curve for the nMOS devices is presented in Figure 3.6 and that for the pMOS device in Figure 3.7. The C-V curves depict the transition from the accumulation mode to the depletion mode.

In the second case, the drain-source terminals have been swept from -2 to +2, while the bulk is connected such that the gate-bulk junctions are always

reverse biased. Figure 3.8 and Figure 3.9 shows the C-V curves for the n-MOS and p-MOS capacitors respectively. Varying the drain-source voltage with respect to the gate is equivalent to sweeping the V_{GS} of the MOSFET. As the V_{GS} crosses the threshold voltage V_{th}, the device goes from depletion to inversion mode. This results in the sharp change of capacitance as seen in Figures 3.8 and 3.9 below.

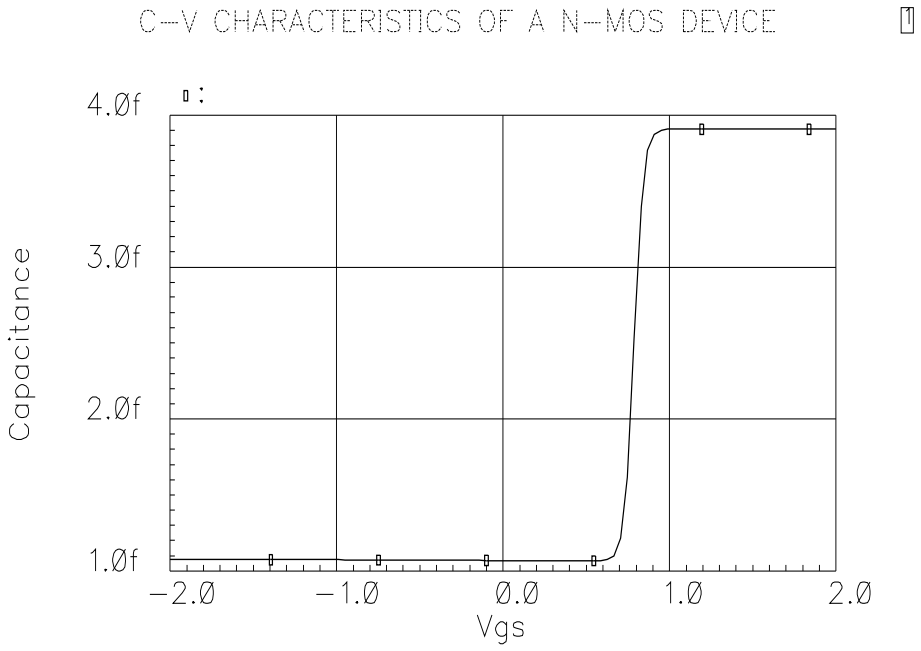


Figure 3.8: C-V characteristics of n-MOS device in inversion mode.

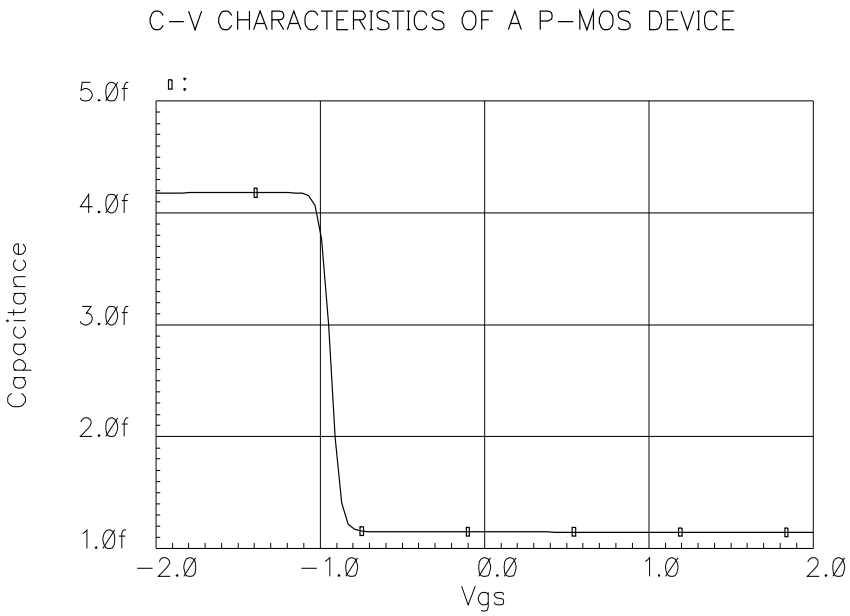


Figure 3.9: C-V characteristics of p-MOS device in inversion mode.

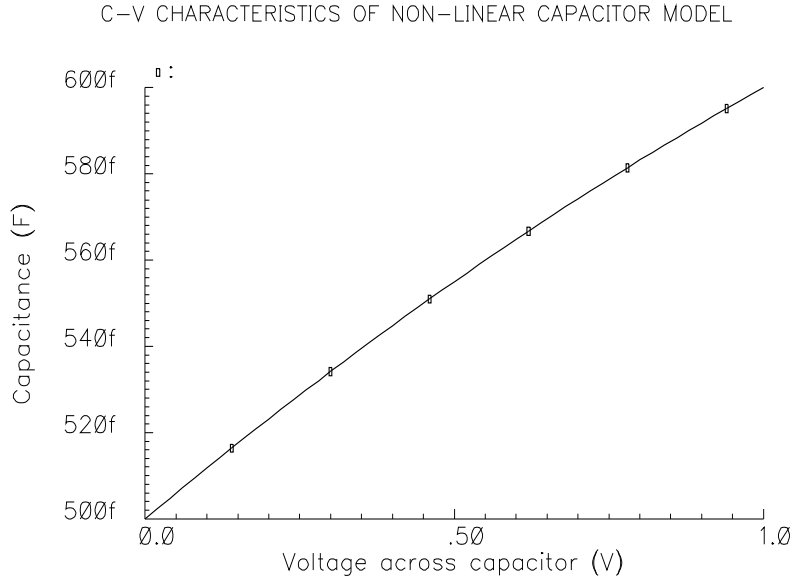


Figure 3.10: C-V characteristics of nonlinear capacitor modeled in Verilog-A.

3.3.2 Verilog-A model

A more general model of a nonlinear capacitor has been coded using Verilog-A. Verilog-A is a hardware description language (HDL) that allows behavioral modeling of nonlinear components and is compatible with Spectre simulations.

The modeled nonlinear capacitor is derived from basic principles and is an accurate and charge conserving model [3/4]. The nonlinear capacitor is required to be in the form of:

$$C(v) = C_0 + C_1 v + C_2 v^2 + \ldots$$

where v is the voltage across the capacitor. The charge q is then the integral of the capacitance C with respect to the voltage v.

$$q(v) = \int_0^v C(v)dv$$

$$q(v) = C_0 \times v + C_1 \times \frac{v^2}{2} + C_2 \times \frac{v^3}{3} + \ldots$$

The current through the capacitor is then,

$$i(t) = \frac{dq(v(t))}{dt}$$

The nominal value of the capacitor used is 0.5 pF. The nonlinear capacitors are modeled such that the maximum capacitance is 0.6 pF (i.e. the maximum nonlinearity is 20 % of the original).

3.4 Series compensation with nonlinear capacitors

Series compensation technique involves replacing a single nonlinear capacitor of size C pF with a series of two nonlinear capacitors of size 2C F each, connected back to back. The equivalent capacitance of the series of capacitors is therefore C F, and the kT/C noise in the circuit remains the same [3/2]. The midpoint of the capacitors can be biased in order to obtain the nominal value of capacitance as shown in Figure 3.11. In MOSCAPs the midpoint needs to be biased to maintain the capacitors in accumulation region.

Series compensation of MOSFET gate capacitors has been effectively implemented in switched capacitor networks, such as modulators and amplifiers resulting in linearity improvements [3/2] [3/7].

This technique results in reducing the swing across each of the capacitors in series. Hence, if node D in Figure 3.11 experiences a 1Vp-p swing,

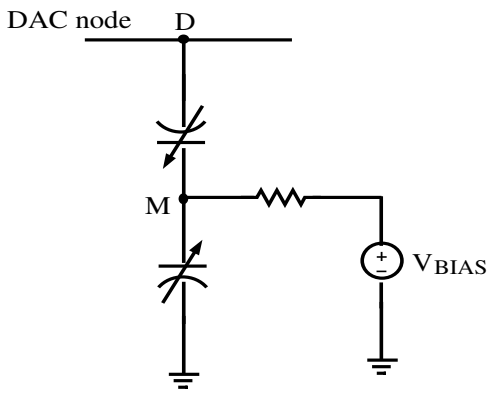


Figure 3.11: Series compensation at a DAC node.

the node M experiences a swing of 0.5Vp-p. The voltage swing across the capacitors is thus halved, as compared to the case when a single capacitor is connected at the DAC node. The series compensation technique can be applied to the array of capacitors employed in the Q-DAC to reduce the effects of MOSCAP nonlinearity in the Q-DAC.

4. SWITCHED CAPACITOR LOW-PASS FILTER

4.1 Introduction

Switched capacitor filters (SCF) are discrete time filters operating on sampled data. They are different from digital filters in which both signal and time are discrete. Unlike continuous time filters, SCF are built with switches, capacitors and OPAMPs. The increased accuracy and matching of capacitors combined with that of MOSFET switches as compared to resistors results in improved accuracy of SCFs. Switched capacitor filters with high dynamic range and accurate amplitude and phase response have been designed for various applications.

Increasing integration over the years has escalated the popularity of switched capacitor filters (SCFs) over discrete element filters. SCFs are now part of many modern systems, especially communication applications. In most cases they replace costly and large passive filters. In some they simply relax the requirements of continuous-time filters, which in turn leads to cost and size benefits.

4.2 Filter requirements

A digital to analog conversion system has been designed in this research for audio frequencies. The conversion rate had been fixed at a frequency of 1MS/s. The audio DAC should feature a flat gain for signals within the audible frequency range (20 Hz – 20 kHz) and should preferably have a linear phase response.

The output of the pipelined Q-DAC [Figure 1.4] is in the form of charge packets and the Q-DAC by itself does not have any driving capability. The output charge, if converted into voltage will have a staircase-like appearance because of the many circuit non-idealities like charge injection etc. The pipelined Q-DAC is, in itself a switched capacitor network and there will be mirror images around the DAC clock frequency (1MHz) and its multiples. Hence, there is a need for a smoothing filter at the output.

A low pass SCF that can be integrated on-chip, clocked at twice (2MHz) the frequency of the Q-DAC will greatly reduce the requirements of any off chip smoothing filter. This low-pass filter, should offer minimum attenuation for frequencies of interest (20 Hz – 20 kHz) and reject components at higher frequencies. The signal-to-noise ratio (SNR) and the total harmonic distortion (THD) of the SCF filter are important because it would limit the performance of the entire system.

4.2.1 Group delay

Group delay is used as a criterion to measure phase nonlinearity in filters. A constant group delay or a linear phase filter is considered ideal for audio applications. In such a filter all the frequencies in the pass band are delayed by the same amount, thus preserving the wave-shape. A mathematically description of the concept of linear phase delay filters follows.

In analog filter domain, let the transfer function at a real frequency s = jω, be H(s).

$$H(s) = H(j\omega) = \left|H(j\omega)\right|.e^{j\theta(\omega)}$$

| H (jω)| is the magnitude component and θ (ω) is the phase component [3/2].

The phase delay T_{ph} (ω) of the filter can be defined as the phase shift experienced by each frequency component of the input signal. Phase delay expresses the phase response of the filter as a time delay in seconds.

Mathematically,

$$T_{ph}(\omega) = -\frac{\theta(\omega)}{\omega}$$

The group delay can be defined as the derivative of the phase with respect to frequency, or the slope of the phase response.

Mathematically,

$$T_g(\omega) = -\frac{\partial\theta(\omega)}{\partial\omega}$$

The group delay signifies the time delay experienced by a narrow band of frequencies. For example in an amplitude modulated system, the group delay can

be interpreted as the propagation time delay of the envelope of the amplitude modulated signal.

In a linear phase filter, the phase is a linear function of frequency for the pass-band frequency range. Therefore, the phase delay and the group delay over the pass-band are identical and equal to a constant (α).

. $$\theta(\omega) = \alpha \times \omega \Rightarrow T_{ph} = T_g = \alpha$$

Linear phase implies that there is no phase distortion in the frequency range of interest, as the signal propagates through the filter; thereby, maximally preserving the shape of the waveform. Nonlinear phase response on the other hand results in unequal delay characterized by undesired components in the transient response.

4.2.2 Comparison of filter types

A Bessel filter has been chosen to be designed for the system, as its linear phase response is considered desirable for audio applications. The Bessel filter provides a nearly constant propagation delay for all frequencies in the pass-band. Therefore, applying a square wave (consisting of a fundamental and many harmonics) to the input of a Bessel filter results in an output square wave with no overshoot (the frequencies are delayed by the same amount).

Chebyshev and elliptic filters feature very steep transition-band slopes, but also have ripple in the pass-band and a very nonlinear phase response.

For audio applications, this nonlinear phase response is undesirable as phase and frequency, as well as amplitude, provides critical information. Butterworth filters have advantages of flat pass-band response, adequate roll-off and relative insensitivity to component tolerance making them a good choice for audio applications. The Butterworth design, however, exhibits large group delays near the cutoff frequency. Constant group delay characteristic can however be added on to these filter designs by cascading all-pass filters with delay equalizing properties [4/1].

The comparative plots for amplitude and phase response and group delay have been provided in Figures 4.1 through 4.3. Four types of filters – Bessel, Butterworth, Chebyshev and Elliptic have been compared.

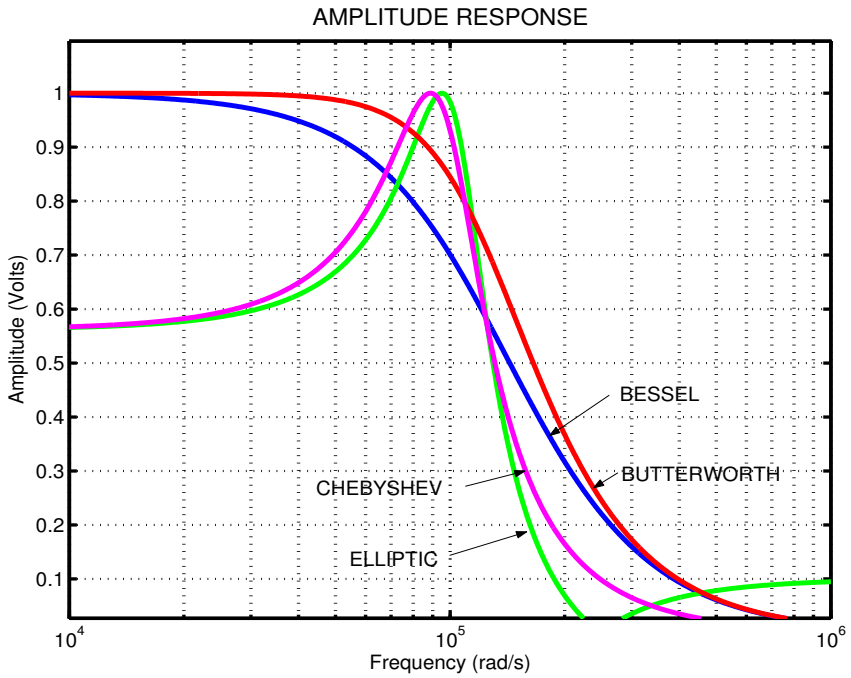


Figure 4.1: Comparison of amplitude response for different filter types.

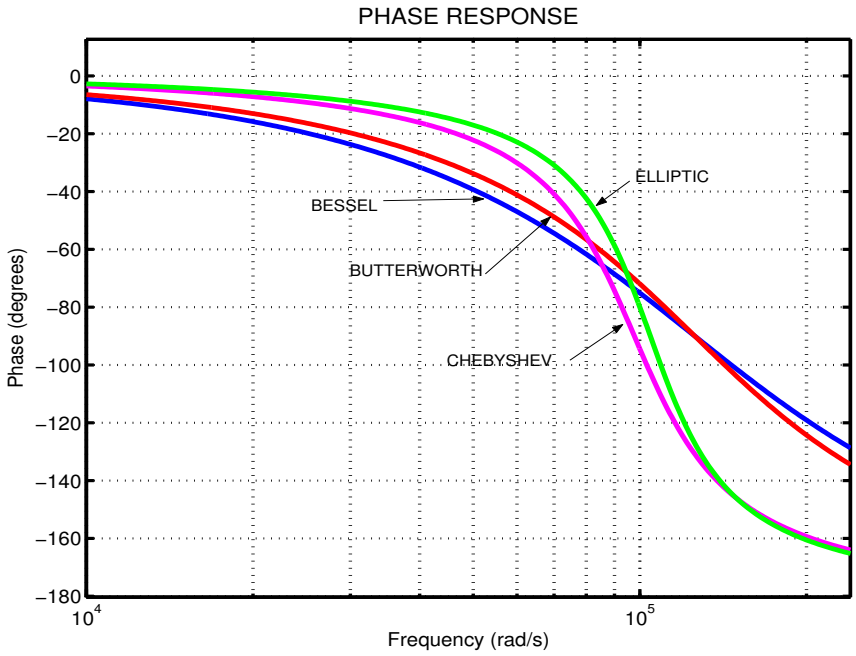


Figure 4.2: Comparison of phase response for different filter types.

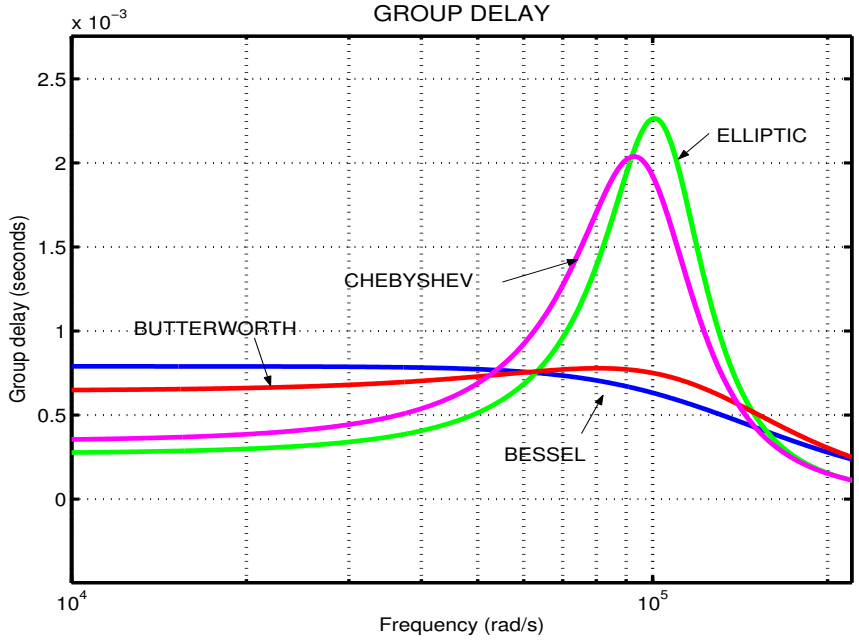


Figure 4.3: Comparison of group delay for different filter types.

4.3 Bessel filter design

A Bessel filter was chosen to be designed for the system. The filter design involves a number of steps and several software tools like MATLAB, Switcap2 and SpectreRF have been employed during the design process. This section provides the theory, calculations and the simulations involved in the filter design.

4.3.1 Filter approximation

A continuous time approximation of the required filter was first computed. Then a discrete time equivalent was obtained using MATLAB, from which the values of the components were computed. The continuous time transfer function of a general Bessel-Thompson filter can be expressed as a normalized transfer function H(s), in which the pass-band edge is equal to 1 Krad/sec and the DC gain has been chosen to be zero.

$$H(s) = \frac{a_0^n}{E^n(s)}$$

where,
$$E_s^n = \sum_{i=0}^{n} a_i s^i = a_n s^n + a_{n-1} s^{n-1} + \ldots + a_0$$

The coefficients a_i can be determined by employing the Bessel-Thompson's approximation for a maximally flat group delay filter, for any order n

[4/2]. The order of the filter required can be estimated from the expressions of loss and group delay obtained during the approximation, provided there is an estimation of the loss of the flat group delay filter at the pass-band, the pass-band edge frequency and the DC delay [4/1]. The loss of the filter α (ω) is approximately:

$$\alpha(\omega) \approx \frac{10\log_e}{2n-1}\left(\omega T_g^{DC}\right)^2$$

The group delay at a frequency ω can be expressed as:

$$T_g(\omega) = T_g^{DC}\ [1 - ((a_0^n)^2 (\omega T_g^{DC})^{2n} e^{-(\omega T_g^{DC})^2/2n-1})]$$

A second order filter was determined to be sufficient for the DAC and the coefficients a_i of the transfer function were calculated as follows:

$$a_i^n = \frac{(2n-i)!}{2^{n-i} i!(n-i)!}$$

The coefficients can also be determined from the tables for maximally flat delay polynomials. The normalized continuous time transfer function as determined from the Bessel-Thomson coefficient a_i is given below.

$$H(s) = \frac{a_0}{a_2 s^2 + a_1 s + a_0}$$

$$= \frac{3}{1s^2 + 3s + 3}$$

The pole locations for the normalized transfer function were determined to be:

$$p_{1,2} = -1.5 \pm j0.86603$$

The de-normalized transfer function and the poles were determined by frequency scaling for the pass-band edge frequency of 30 kHz. The de-normalized transfer function and the pole locations are:

$$H(s) = \frac{1.065917 * 10^{11}}{1s^2 + 5.65487 * 10^5 s + 1.065917 * 10^{11}}$$

$$p_{1,2} = -2.827433 * 10^5 \pm j1.632419 * 10^5$$

Figure 4.4 shows the ac response for the continuous time Bessel filter for a pass-band edge of 30 kHz and its pole zero locations are shown in Figure 4.5(a). Figure 4.5 (b) shows the group delay to be approximately 3.3μsec over the frequency range of interest.

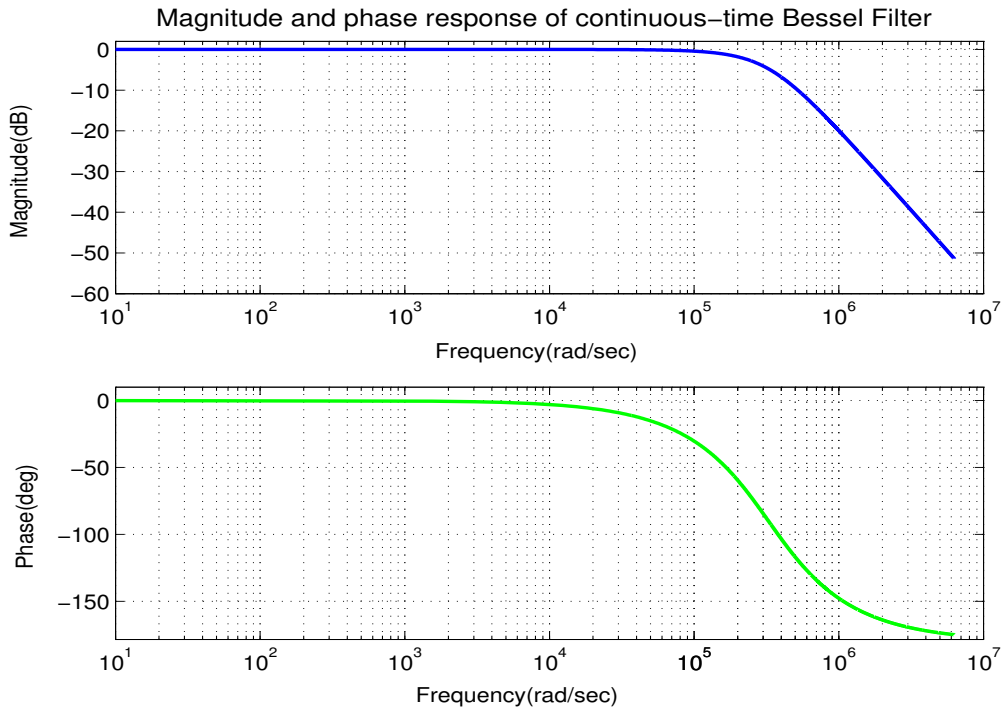
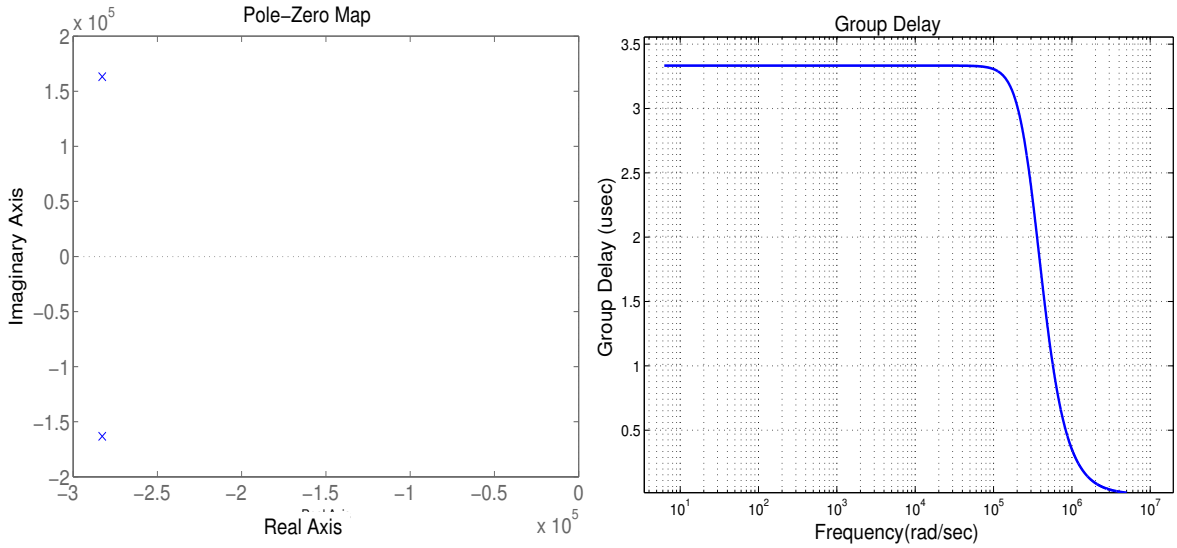


Figure 4.4: Frequency response of 2nd order continuous time Bessel filter.



(a) (b)

Figure 4.5: Pole-zero locations and group delay for continuous time Bessel filter.

4.3.2 Bilinear transformation

The discrete time equivalent of the Bessel filter for a sampling frequency of 2MHz was determined using bilinear transformation. Bilinear transformation is used to map the analog frequency response into sampled data response without aliasing. In this method the entire left half of the s-plane is mapped onto the inside of the unit circle in the z-plane, where the circumference of the unit circle is representative of the imaginary axis of the s-plane. This results in warping of the frequency scale and pre-warping is employed to ensure that the frequency response in the z-domain is accurate. Pre-warping simply involves replacing the s-domain frequency ω, by the normalized frequency Ω, such that:

$$\Omega = \frac{2}{T}\tan\left(\frac{\omega}{2}\right)$$

The pre-warped transfer function in s-domain is then transformed onto the z-domain by replacing s by $\frac{2}{T}\frac{z-1}{z+1}$. Bilinear transformation is thus a nonlinear operation. Flat gain and ripple in the s-domain are preserved in the z-domain but phase linearity is lost. Matched s → z transformation is an alternative method of obtaining the z-domain transfer function in which both gain and phase are preserved for frequencies much smaller than the stop-band frequency, but are aliased for all other frequencies [4/1]. Bilinear transformation was chosen over matched s → z transformation in order to avoid the effects of aliasing. Furthermore

for small frequencies (as compared to the sampling frequency), including 0, bilinear transformation is almost linear in phase.

The z-domain transfer function of the filter was determined to be:

$$H(z) = \frac{5.81097 * 10^{-3} + 1.16219 * 10^{-2} z^{-1} + 5.81097 * 10^{-3} z^{-2}}{1 - 1.73031 z^{-1} + 7.53557 * 10^{-1} z^{-2}}$$

The magnitude and the phase response in the z-domain are shown in Figure 4.6 and the poles and zeros in Figure 4.7.

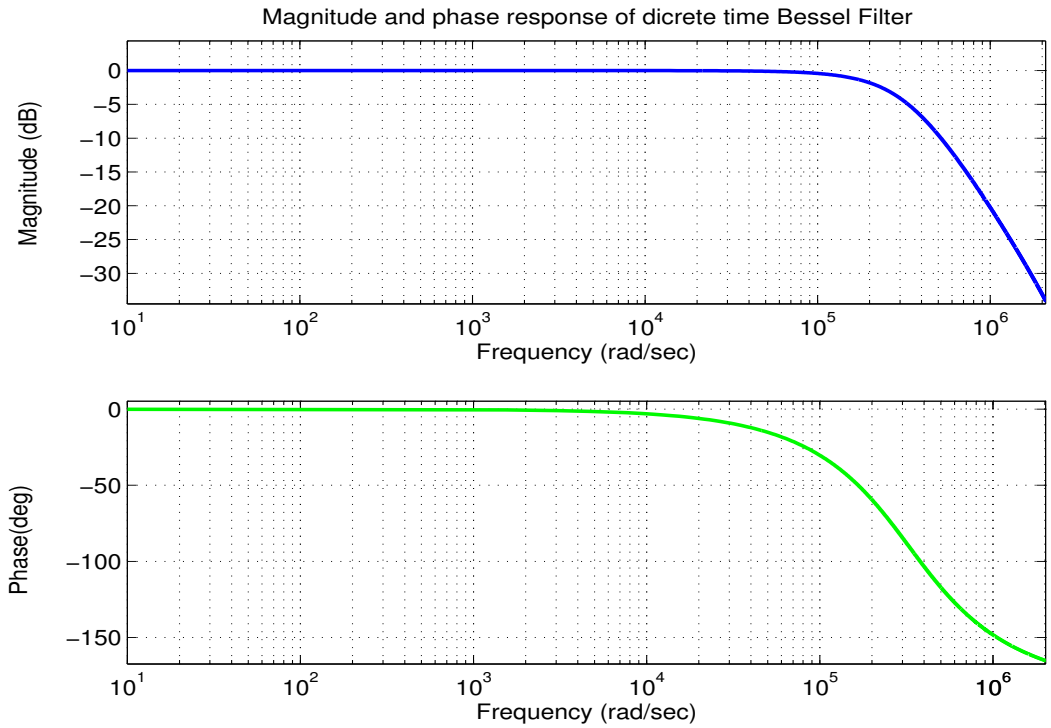


Figure 4.6: Frequency response of discrete time Bessel filter.

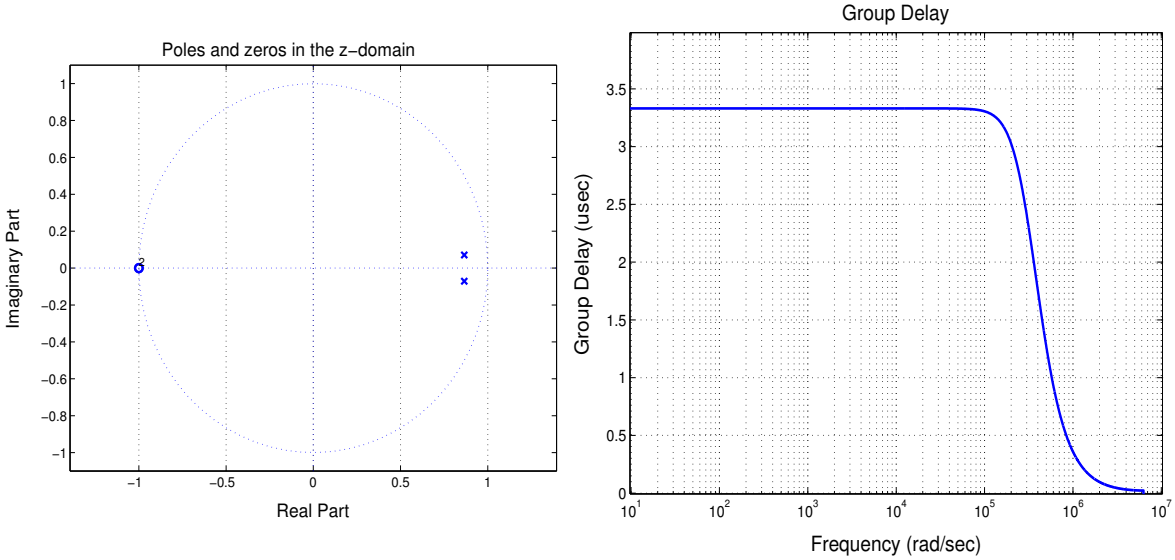


Figure 4.7: Pole-zero locations and group delay for the discrete time Bessel filter.

The poles and zeroes in the z-domain as obtained from MATLAB are:

$$z_{1,2} = -0.999 \pm j2.763753 \quad *10^{-7}$$

$$p_{1,2} = -8.65157 \quad *10^{-1} \pm j7.11419 \quad *10^{-2}$$

The two zeroes of H (z) are actually at -1 ± j0, the values of $z_{1,2}$ contain small discrepancies due to numerical computational errors. Figure 4.7 shows that group delay is nearly constant for the frequency range of interest. Loss is less than 1 dB and group delay deviation is less than 0.3μsec at the pass-band edge of 30 kHz. Figure 4.8 shows that the transformation introduces two zeros at z = -1. It was found that replacing the two zeros at z = -1 by a single zero at z = 0 results in a better capacitance spread and a smaller total capacitance after the scaling

operations described below. The transfer function still meets the specifications and the constant group delay characteristic was not lost by this transformation. The corresponding frequency response, shown in Figure 4.8 is very similar to the previous response. Figure 4.9 (a) shows the zero shifts while Figure 4.9 (b) confirms that flat group delay characteristic of the system is maintained.

$$H(z) = \frac{4 * 5.81097 \ * 10^{-3}}{1 - 1.73031 \ z^{-1} + 7.53557 \ * 10^{-1} z^{-2}}$$

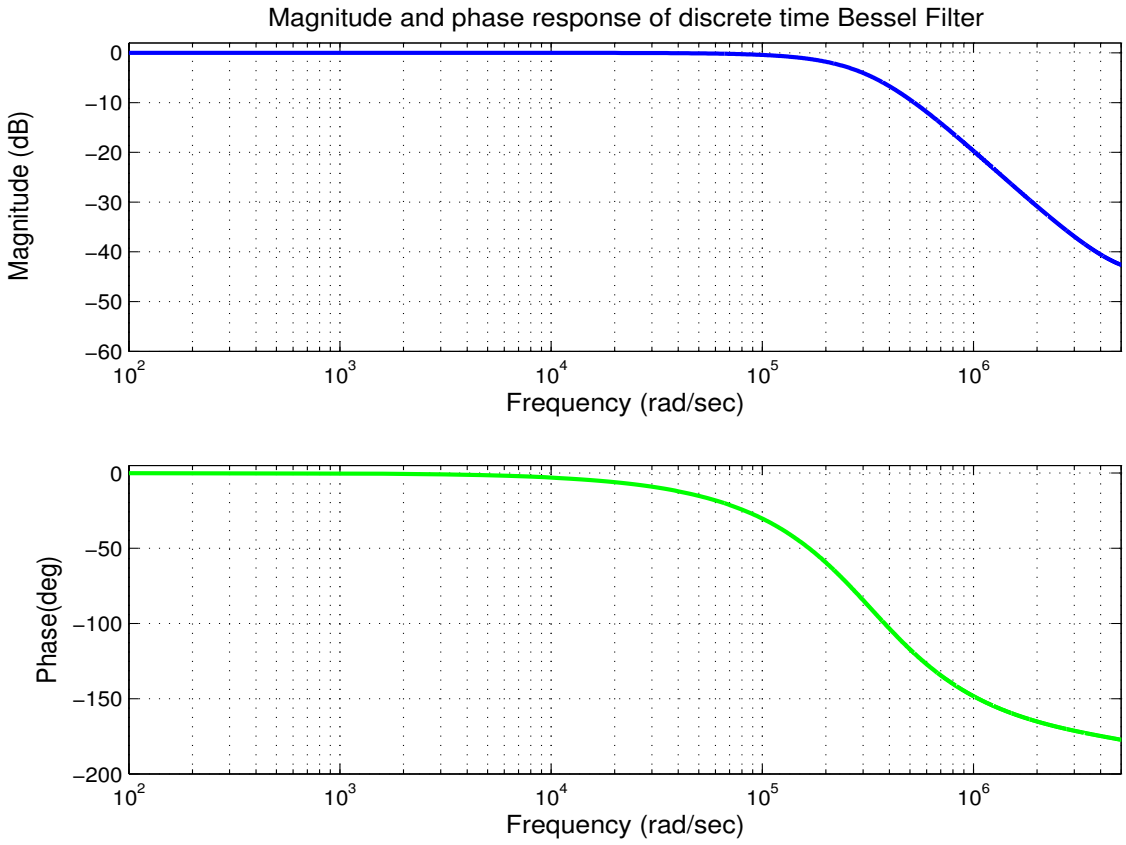


Figure 4.8: Frequency response of the discrete time Bessel filter after zero shifting.

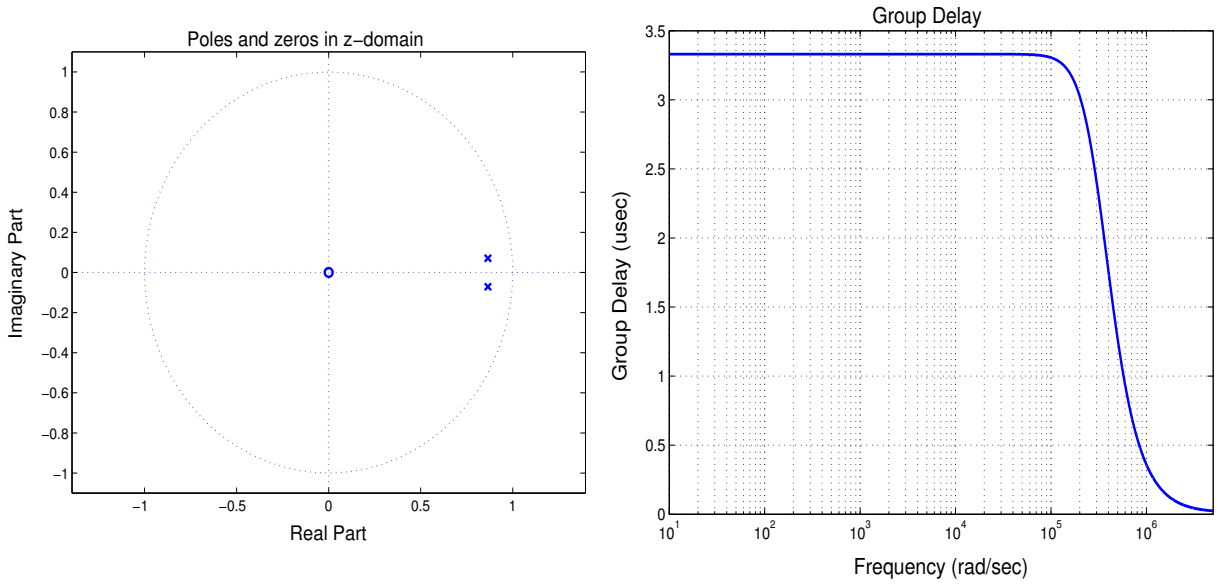


Figure 4.9: Pole-zero locations after zero shifting and the corresponding group delay response of the discrete time Bessel filter.

4.3.3 Switched capacitor filter

A low-Q biquad model based on an active RC filter has been chosen for the implementation of the second order filter [4/4]. The switched capacitor filter based on this model has been shown in Figure 4.10. The switches operate on a two phase 2MHz clock clk2 (Φ_{11},Φ_{12}) as shown in the Figure 4.10. The phases Φ_{11},Φ_{12} are non-overlapping as shown in the inset in Figure 4.10. The circuit has been shown without switch sharing for clarity. The signal flow representation of the discrete time filter has been shown in Figure 4.11 [4/4]. For low pass operation the input through K_1C_1 is the major signal path [4/5].

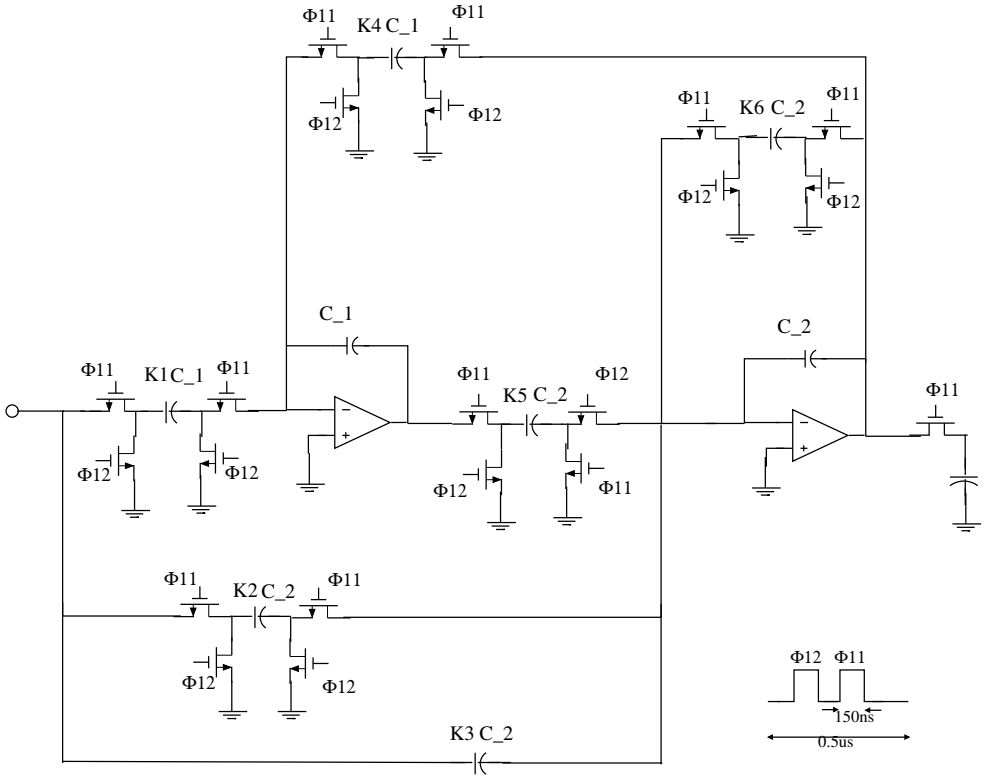


Figure 4.10: Switched capacitor low Q biquad circuit.

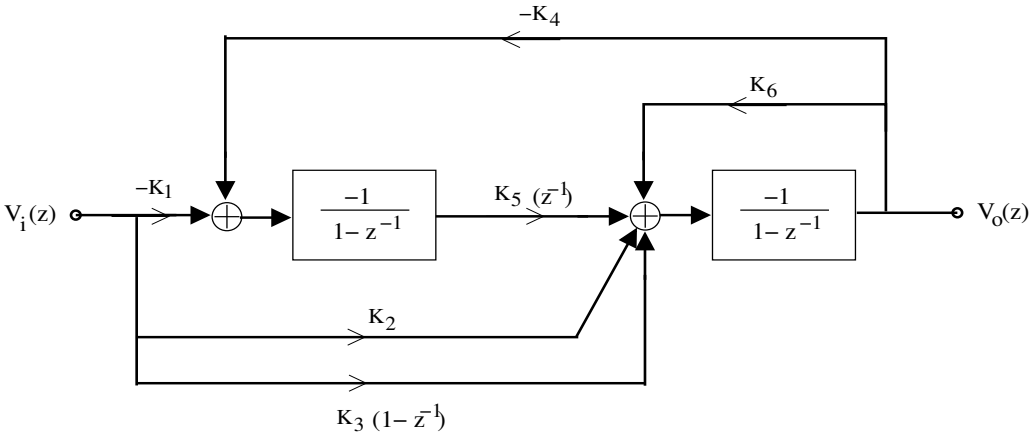


Figure 4.11: Signal flow graph for the switched capacitor biquad.

The switched capacitor biquad shown in Figure 4.10 can be represented by the transfer function given below.

$$H(z) = -\frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1}$$

The values of the capacitors K_i (i = 1-6) have been calculated by equating like terms of the transfer function above and the transfer function of the designed low-pass Bessel filter, given in Section 4.3.2. The capacitors C_1 and C_2 have been assumed to be 1pF each, which results in the calculated kT/C noise power due to the smallest capacitor to be less than -150dB. The values of the capacitors have been tabulated in Table 4.1, presented later in this chapter. The capacitor K_3 was found to be zero and the value of capacitor K_2 was negligibly small, and has been neglected in the switched capacitor implementation. Hence, for this low pass implementation of the biquad capacitor K_1 C_1 is the only forward path.

The input capacitor of the SCF should accept the output of the Q-DAC, which is in the form of charge stored in the MSB capacitor. The output charge needs to be delivered into a "virtual ground" node [4/6]. The input capacitor in the biquad circuit in Figure 4.10 is designed to sample the output voltage rather than charge. Therefore the structure of the switched capacitor K_1 was altered such that during the input phase Φ_{12}, the charges in the MSB capacitor and capacitor K1 are shared. The charge sharing occurs in the ratio of the capacitor K_1 and the unit

capacitor of the DAC. It was verified that this change in the circuit results in a negligible change in the pass band frequency response. The altered circuit has been illustrated in Figure 4.12 below. The signal paths due to K_2 and K_3 have also been removed in this circuit. Switch sharing has been implemented in the filter circuit but has not been shown in Figure 4.12 for clarity.

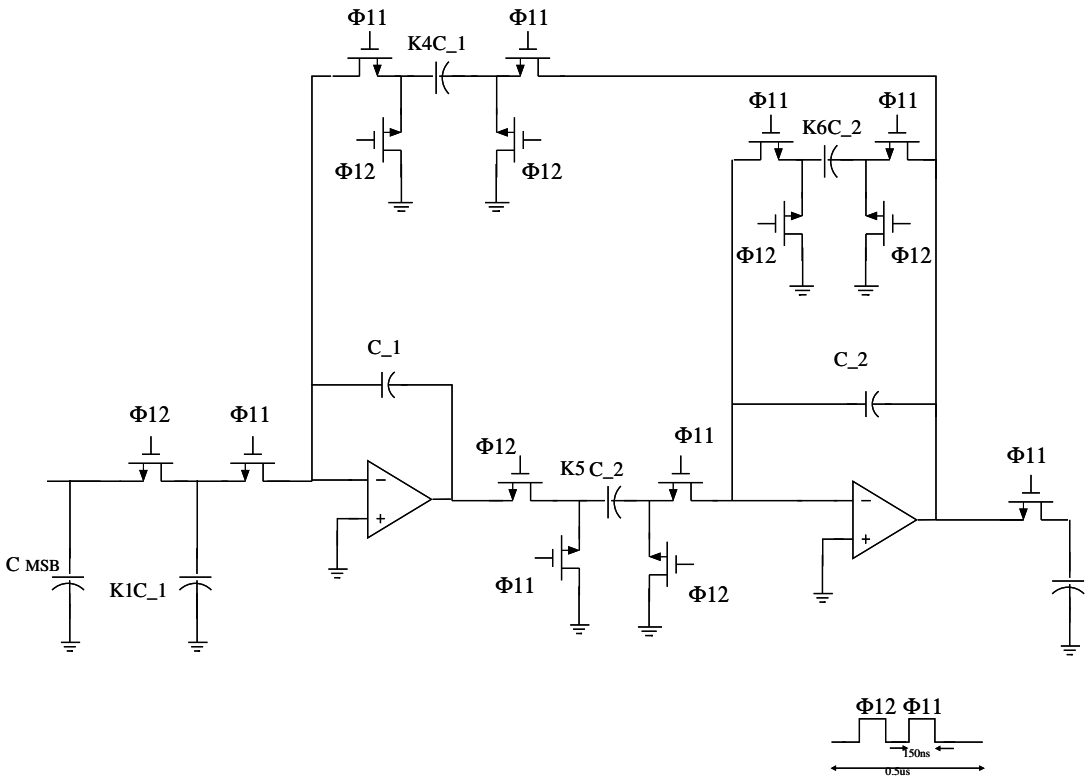
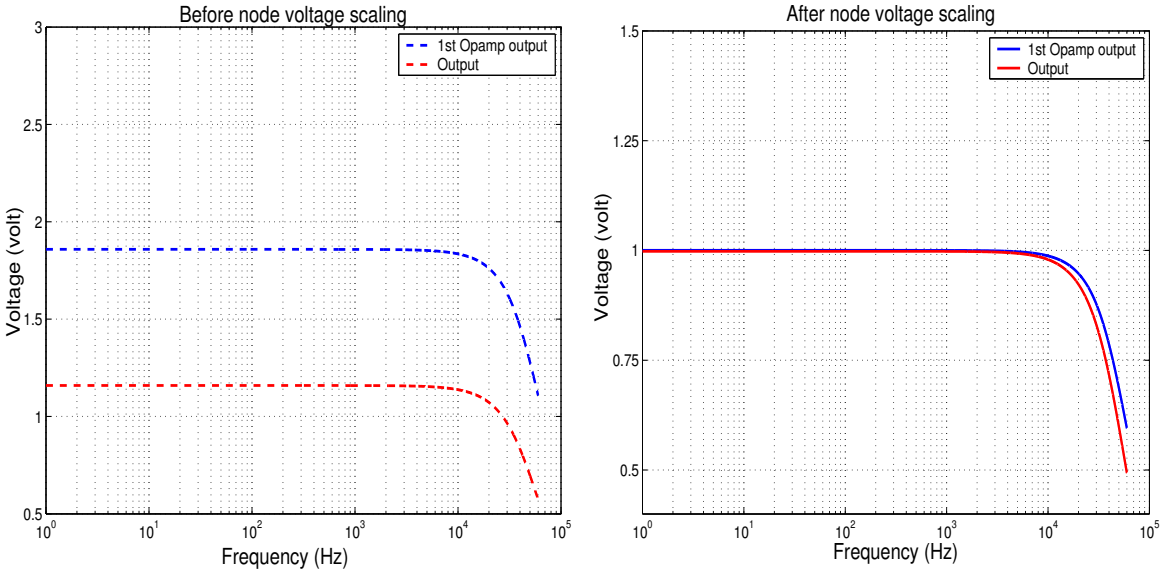


Figure 4.12: Switched capacitor biquad employed in the system shown without switch sharing.

4.3.4 Dynamic range scaling

The filter response depends on the capacitor ratios and not the absolute values. Thus the actual performance of the SCF can be improved and the area occupied by the filter can be optimized by performing scaling operations on the capacitors [4/3].



(a) (b)

Figure 4.13: Magnitude response of biquad output node (a) before and (b) after scaling for maximum dynamic range.

For maximum dynamic range, all OPAMP output node voltages should be scaled such that each saturates for the same input voltage level. Since the DC gain of the filter is required to be 1 or 0 dB, dynamic range scaling simply involves

scaling the capacitors such that output of both OPAMPS never exceeds 0 dB. The scaling factor for each stage *i* is simply $k_i = V_{pi}/V_{p,out}$, where V_{pi} is the peak output voltage of OPAMP *i* and $V_{p,out}$ is the peak pass-band value of V(out), which is 0 dB in this case. It can be shown that multiplying each capacitor connected or switched to the output terminal of OPAMP *i* by the factor k_i, scales the output of that OPAMP to $V_{p,out}$ [4/3]. This operation repeated for each OPAMP in the filter not only results in maximum dynamic range but also reduces the output noise level. Figure 4.13 shows the results of dynamic range scaling on the OPAMP outputs. Table 4.1 also shows the capacitor values after dynamic range scaling.

4.3.5 Minimum capacitance scaling

The scaling for dynamic range was performed before that for minimum capacitance, as the latter does not contribute to any change in the output of the OPAMPs. It can be shown that scaling all the capacitor in the input branches of an OPAMP by any factor results in no change in the output voltage of that OPAMP [4/3].

For minimum capacitance scaling all capacitors in the filter were divided into non-overlapping sets such that set *i* contains capacitors in the input branches of OPAMP *i*. Each input branch capacitor C_i of set *i* was then multiplied by C_{min} / $C_{i,min}$, where C_{min} is the smallest capacitor to be employed in the SCF and $C_{i,min}$ is the smallest capacitor in the set. This scaling operation results in the smallest

capacitor being set equal to C_{min} and reduces the total capacitance and the capacitance spread. All scaling operations were performed with the help of Switcap2 for an ideal OPAMP with open loop gain of 70 dB and ideal switches and capacitors. A minimum capacitance of 0.5 pF has been chosen for the filter. A minimum capacitance of 0.5 pF size leads to accurate matching of the capacitors in the SCF as well as sufficiently low thermal noise power due to the capacitors in the filter. Table 4.1 below shows the capacitance values before and after the scaling operations.

Table 4.1: Capacitor values before and after the scaling operations.

Capacitors	**Before scaling (pF)**	**After node voltage scaling (pF)**	**After scaling for minimum capacitance (pF)**
C_1	1	1.862	5.3
C_2	1	1.1635	0.178
K1 C_1	0.176	0.176	0.5
K2 C_2	0	0	0
K3 C_2	0	0	0
K4 C_1	0.176	0.2043	0.582
K5 C_2	0.176	0.327	0.5
K6 C_2	0.327	0.381	0.582

4.4 Simulation results

MATLAB and Switcap2 have been used for the filter simulations with ideal switches and ideal OPAMPs. MATLAB facilitates the analysis of the continuous time and discrete time filter transfer functions. The frequency response, group delay and pole zero locations of the filter, as specified by the transfer function polynomials have been plotted using MATLAB. The discrete time simulator Switcap2 allows the circuit simulations for the filter with ideal switches and OPAMPs. Scaling operations were performed with Switcap2 as a first cut design approach.

Final circuit simulation for the system has been done in SpectreRF. SpectreRF can be used to perform time and frequency domain analysis of switched capacitor networks or any time-varying network in general. Unlike other circuit simulators like SPICE, SpectreRF is capable of performing small signal analyses like ac about a periodic operating point [4/7]. Hence, SpectreRF can be employed for transistor level simulations to predict the frequency response of the discrete time filter designed, with an active clock signal, clk2 (Φ_{11}, Φ_{12}). SpectreRF's periodic steady state (pss) and periodic small signal (pac) analyses have been performed for simulating the filter frequency response [4/8]. These analyses facilitate the simulation of the ac response of the filter over a periodic operating point as defined by the clock clk2, with the non-overlapping phases, Φ_{11} and Φ_{12} as shown in Figure 4.14.

The SCF employs only n-MOS switches and an operational amplifier (OPAMP) with a open loop gain and unity gain bandwidth of 70 dB and 80 MHz respectively. The design of the switches and the OPAMP will be discussed in detail in Chapter 5.

The frequency response of the final filter circuit with real OPAMPs and switches has been provided in Figures 4.14 and 4.15. Figure 4.15 (b) shows the linear phase response of the filter in the audio frequency range.

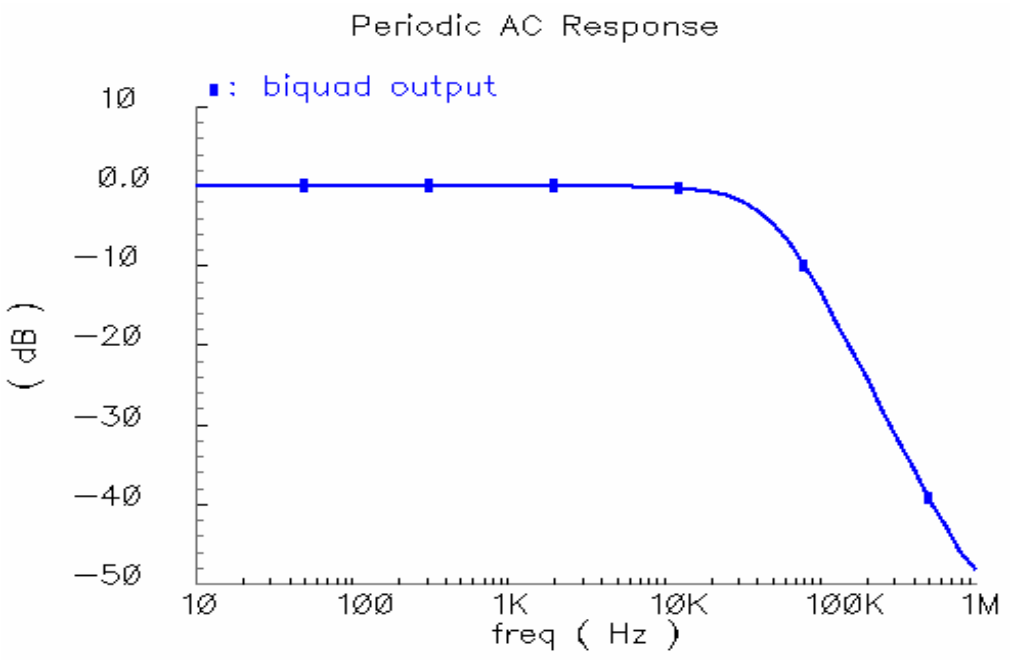
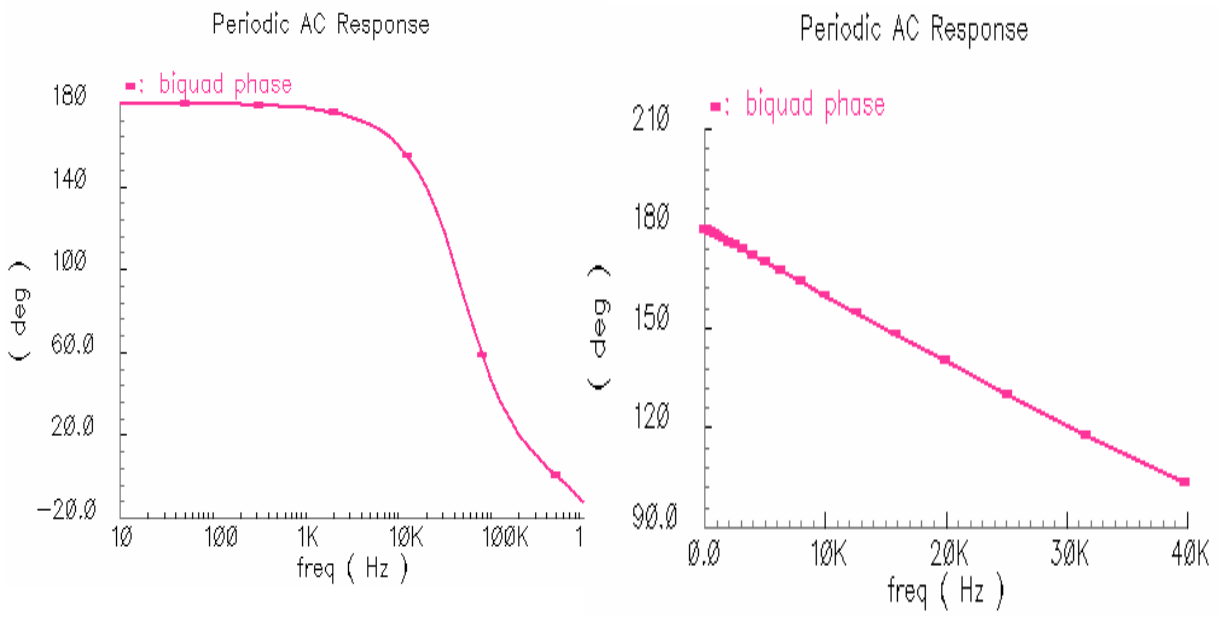
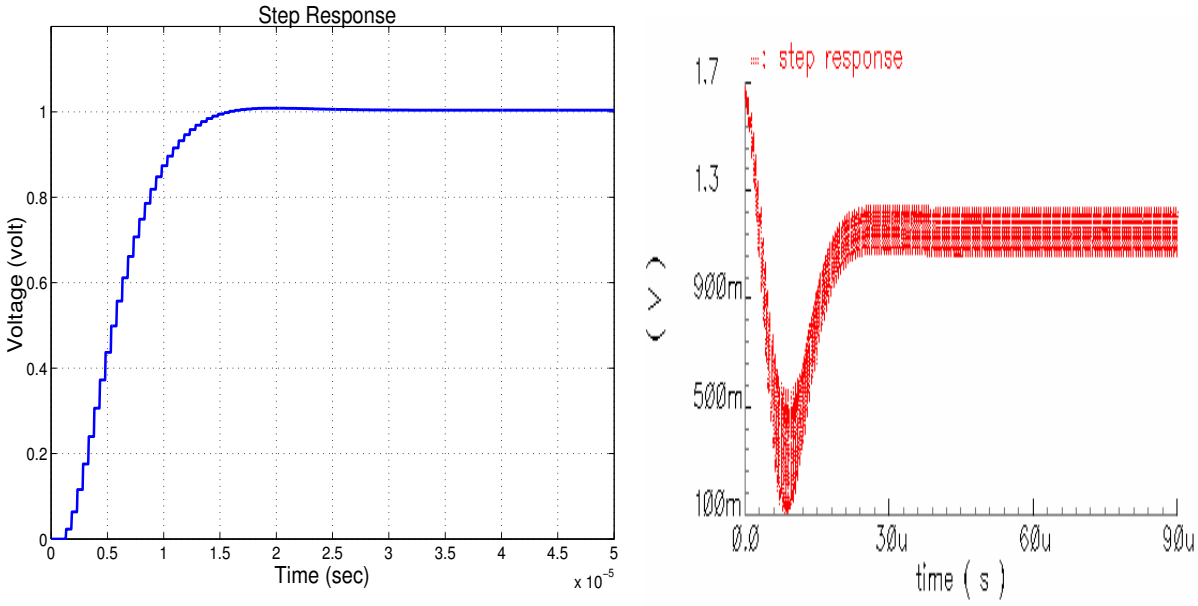


Figure 4.14: Amplitude response of the switched capacitor filter as simulated using real circuit components in SpectreRF.



(a) (b)

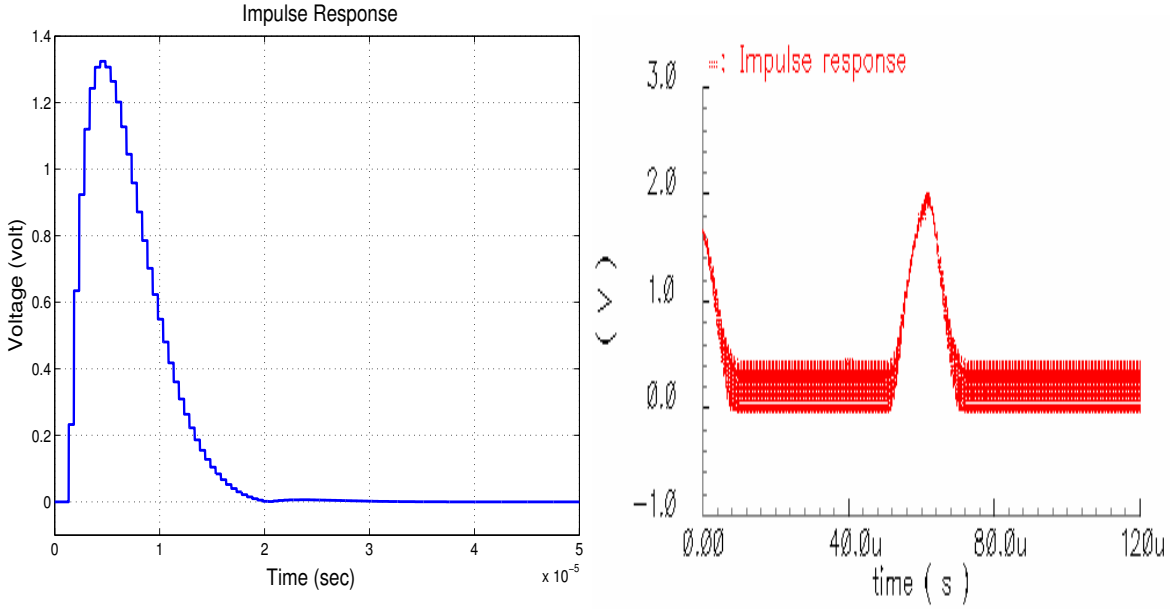
Figure 4.15: (a) Phase response (b) magnified version of phase response over pass-band of the SCF as simulated using real circuit components in SpectreRF.



(a) (b)

Figure 4.16: Step response of the SCF as simulated in (a) Switcap2 and (b) SpectreRF.

A linear phase response filter is characterized by no ringing in the step and impulse responses. Figures 4.16a) and (b) show the step response as simulated in Switcap2 and SpectreRF respectively. Figures 4.17(a) and (b) show the impulse response of the filter as simulated in Switcap2 and SpectreRF respectively. The Switcap simulations involve ideal circuit elements whereas the simulations in SpectreRF employ nMOS switches and a real OPAMP. The output of the real OPAMP has been dc biased to sit at a voltage of about 1.65V. Figures 4.16(b) and 4.17(b) show the initial output voltage to be at 1.65V and the short time required for the output node to respond to the input.



(a) (b)

Figure 4.17: Impulse response of the SCF as simulated in (a) Switcap2 and (b) SpectreRF.

The filter output settles within a period of 30μs, as seen in Figures 4.16 and 4.17 above. The settling time for a single pole response at 20 kHz, will lead to settling time of 50 μs. Therefore, the filter settling time response is as expected.

5. CIRCUIT DESIGN

5.1 Introduction

The working principles of the pipelined Q-DAC and the switched capacitor filter have been described in the previous chapters. This chapter provides a discussion of the considerations that went into the choice of capacitor and switch sizes for the Q-DAC and SCF. The OPAMP employed in the SCF has also been discussed. An explanation of modeled components used in order to aid in simulation has also been provided.

The circuit has been designed for a 3.3V 0.35µm TSMC process. The minimum channel length recommended for use is 0.4µm. The nominal threshold values of gate-source voltage, V_{th0} for n-MOS and p-MOS transistors are 0.56 V and -0.76V, respectively. The capacitance per unit area for the oxide layer Cox for this process is approximately 4.4fF/μm^2.

5.2 Pipelined Q-DAC

As discussed previously the N-bit pipelined DAC is composed of (4N+2) switches and (N+1) equal valued capacitors [Figure 2.3]. The operation of

the DAC is ideally independent of the size of the capacitors. The capacitor size is influenced by two factors, namely, the die area occupied and the sampled noise consideration. A capacitor size of 0.5 pF has been selected for the DAC capacitors. This result in a total capacitance of 5.5 pF required for the Q-DAC and the total calculated noise power due to the switched capacitor is approximately -162 dB, both of which are acceptable numbers. When series compensation is employed, two capacitors of 1pF each are connected in series in order to keep the noise level comparable. The minimum capacitor size employed in the SCF is also 0.5 pF.

The pipelined operation requires the use of delay elements and some logic gates. Both of these elements have been modeled in Verilog-A codes for simulation purposes.

5.3 Switch design

The function of the switches as discussed in the working of the DAC is to charge and discharge the capacitors to the high/low logic voltages and to redistribute the charges between consecutive capacitors [Figure 2.3]. The charging and discharging functions are controlled by both the bits and the phases of the clocks.

A decision to use all nMOS switches for the pipelined DAC and the following filter and buffer stages was made at the outset. The parasitic capacitances associated with the top plate of the DAC capacitors, along with the total voltage

dependent junctions capacitances of the switches connected to the top plate of these capacitors are the main contributors to the nonlinearity of the DAC [5/1][5/2]. The accuracy of the charge bisection of the Q-DAC depends on the matching of these parasitics [5/3]. Analysis shows that the use of nMOS switches as compared to p-MOS help minimize this parasitic capacitance by allowing the setting the Q-DAC common mode close to ground [5/4].

This system has been designed for a supply voltage of 3.3V. Hence clock "ON" / "OFF" voltages are 3.3V and 0V respectively. Although the nominal value of the threshold voltage for nMOS devices is 0.56V, it can be as high as 0.9V due to the bulk-source voltage (body effect) variations during the DAC operation. While the nMOS switches work effectively for the choice of Vref2 and Vref1 (1V and 0V respectively) in this system, the headroom is still too low for ensuring that the transistor remains in triode region. Using a bootstrapping method to generate a higher swing of voltages for the switch operation is a better choice [5/5].

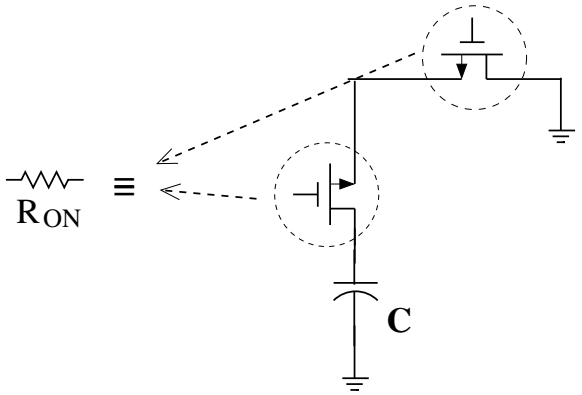


Figure 5.1: Time constant of a node due to switch's "ON" resistance.

The "ON" resistance associated with the switches for a switched capacitor network determines the settling behavior for a particular node voltage. The switch sizes should be chosen such that the node voltage settles within the clock (or clock phase) period. The time constant τ, associated with a switched capacitor node as shown in Figure 5.1 can be estimated from $2R_{ON}C$. The "ON" resistance of a MOS transistor operating in the triode region as denoted in Figure5.1 can be given by [5/6]:

$$R_{ON} = 1/[\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})]$$

For 0.1 percent settling within $3/8^{th}$ of one clock phase period, the time constant, τ associated with a node should satisfy the following relation [5/7].

$$7\tau \leq \frac{3T_{ph}}{8}$$

$$\Rightarrow \quad R_{ON} \leq \frac{3T_{ph}}{56 * C_{max}}$$

The nMOS switches are designed such that the time constant τ at each node is sufficiently small so as to allow the settling of the node voltage in a small fraction of the phase duration.

The capacitors employed in the DAC are 0.5 pF each and the Q-DAC switches operate on the phases of clk1, Φ_1, Φ_2 and Φ_3, the time periods of which are 200nsec each. The minimum capacitance used for the following switched capacitor filter is 0.5 pF and the time periods of the phases of clk2, Φ_{11} and Φ_{12} are

150nsec each. The maximum R_{ON} for the Q-DAC switches is therefore 10 kΩ and that for the SCF is 8 kΩ. The switches employed for both the DAC and the filter are n-MOS transistors of size 1µm / 0.4µm. Calculations show that R_{ON} for the V_{GS} - *Vth* voltages used in the system is only a few kilo-ohms. Simulations confirm that the node voltages settle early during the phase periods.

5.4 Clock implementation

The Q-DAC requires a three phase clock operating at 1MHz (clk1) and the SCF requires a two phase clock (clk2) operating at twice the frequency, i.e. 2MHz. The clock phases have been generated using ideal periodic pulses for simulation purposes. Non-overlapping phases are required, so that there is no loss of charge during charge transfers [5/6]. The time periods of the phases for clk1 and clk2 and their synchronization has been shown in Figure5.2.

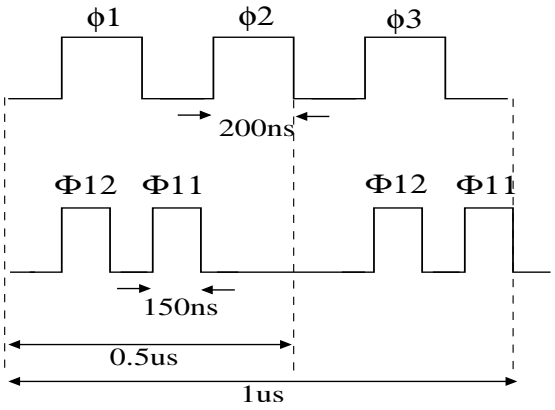


Figure 5.2: Time periods of clock phases used in the DAC and SCF.

5.5 Filter and output buffer

The filter design has been discussed in detail in Chapter 4. The filter response with n-MOS switches and real OPAMP, as simulated in SpectreRF, has been provided in Figures 4.14 through 4.16. The output of the SCF is also delivered in the form of charge packets. An output buffer converts this charge into a continuous time voltage. This section provides a description of the output buffer and also discusses the design details of the OPAMP employed in the SCF and buffer.

5.5.3 Output buffer

The analog output of the Q-DAC is taken in the form of charge stored in the MSB capacitor. As discussed in Section 2.3.2., the voltage across the MSB capacitor is the analog equivalent of the digital input bits only in the case of linear capacitors in the Q-DAC. In the case of nonlinear capacitors, this voltage is highly nonlinear. However the charge stored in the MSB capacitors is still an accurate representative of the digital input. This is because accurate charge bisection occurs as long as there is close matching between the capacitors in the DAC and the parasitics associated with each capacitor. Another charge-bisection occurs between the MSB capacitor and the input capacitor K1C_1 of the SCF at every DAC clock phase Φ_3. Hence, as long as the output of the SCF is delivered in

the form of charge packets, the signal integrity is preserved. However it is required to convert the information in the form of charges into an equivalent voltage.

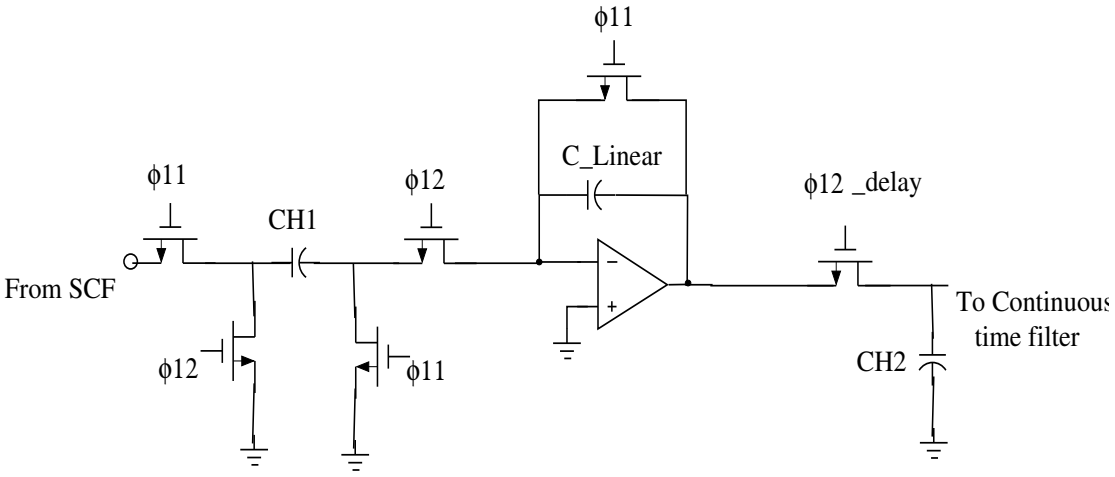


Figure 5.3: Circuit of the output buffer.

The charge to voltage conversion has been achieved using the output buffer circuit shown in Figure 5.3. A linear feedback capacitor is required for the conversion of the charge into proportional output voltage. The buffer circuit also operates on the phases of the 2 MHz SCF clock. The SCF output charge is stored in capacitor CH1 during phase Φ_{11} and the output of the buffer is reset during Φ_{11}.

5.5.2 Finite OPAMP gain and bandwidth

The performance of the SCF filter is considerably affected by the amplifier dynamics. Finite OPAMP gain and bandwidth result in deviation of the filter's magnitude and phase response. Hence the group delay of the filter is also

affected by the OPAMP characteristics. If the clocking frequency *fc*, is at most one-fifth of the OPAMP bandwidth, the deviations caused due to finite bandwidth will be negligible [5/8]. Thus a minimum bandwidth of 10MHz is required for the OPAMP, as the SCF needs to be clocked at a frequency of 2MHz. The error in the magnitude response of the filter due to finite OPAMP gain A_0 has been estimated to be equal to m(ω) [5/8],

$$m(\omega) = -\frac{1}{A_0}(1+\frac{C_1}{C_2})$$

where capacitor C1 is the input switched-capacitor of the integrator and C2 is the integrating capacitor.

From the capacitor values obtained for the SCF biquad, the OPAMP gain required was calculated to be greater than 25dB. Simulations show that the filter gain and phase responses are not affected for an OPAMP gain of at least 60dB and a bandwidth of at least 12MHz.

5.5.3 Single-ended OPAMP design

The OPAMP required for the switched capacitor filter and the following output filter needs to be designed for a minimum gain of 60dB and a minimum bandwidth of more than 12MHz. In addition to that, the OPAMP is required to be able to operate for different capacitive loads and feedback

capacitances. It also needs to be stable for unity gain configuration required for the reset phase of the output buffer.

A two-stage single-ended, folded-cascode OPAMP has been designed for the system. Though it was possible to achieve the desired gain from a single stage, a 2nd stage was added to keep the OPAMP slew rate independent from the load capacitors at the output [5/9].

The schematic of the OPAMP with the transistor sizes and dc currents in each branch has been shown in Figure 5.4. The detailed schematic of the bias circuit has also been shown in Figure 5.5.

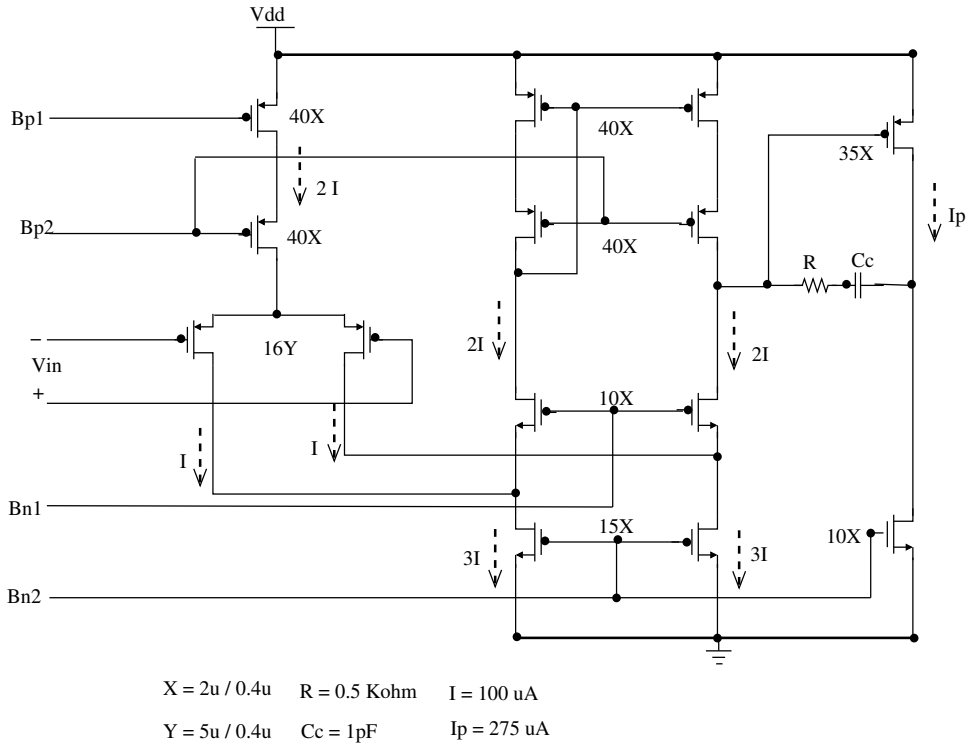


Figure 5.4: Schematic of the OPAMP.

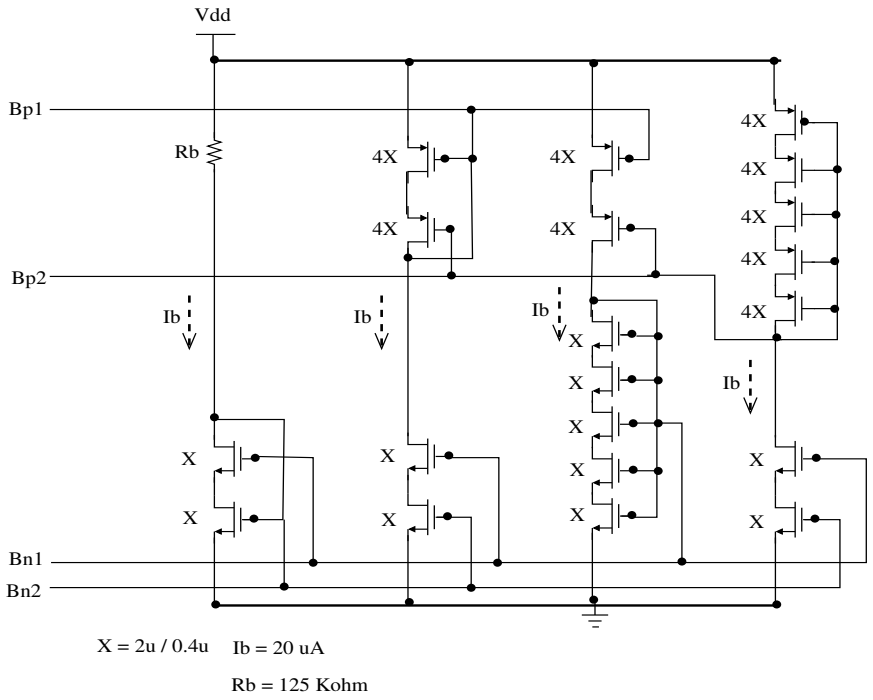


Figure 5.5: Schematic of the bias circuit.

The OPAMP simulations were performed in SpectreRF. The OPAMP has a simulated open-loop dc gain of 70dB and a unity gain bandwidth of 80MHz for a load capacitance of 2pF [Figure 5.6]. The worst case loop phase margin is more than 63˚ [Figure 5.7]. The single-ended output swing of the OPAMP is more than 2.4 Vp-p, as shown in Figure 5.8. Figure 5.9 shows the settling time response of the OPAMP. For a voltage step of 1V, the OPAMP output settles to 0.1% of the final value, within 25nsec. The total power consumption of the OPAMP and the biasing circuitry is about 3mW from a supply voltage of 3.3V.

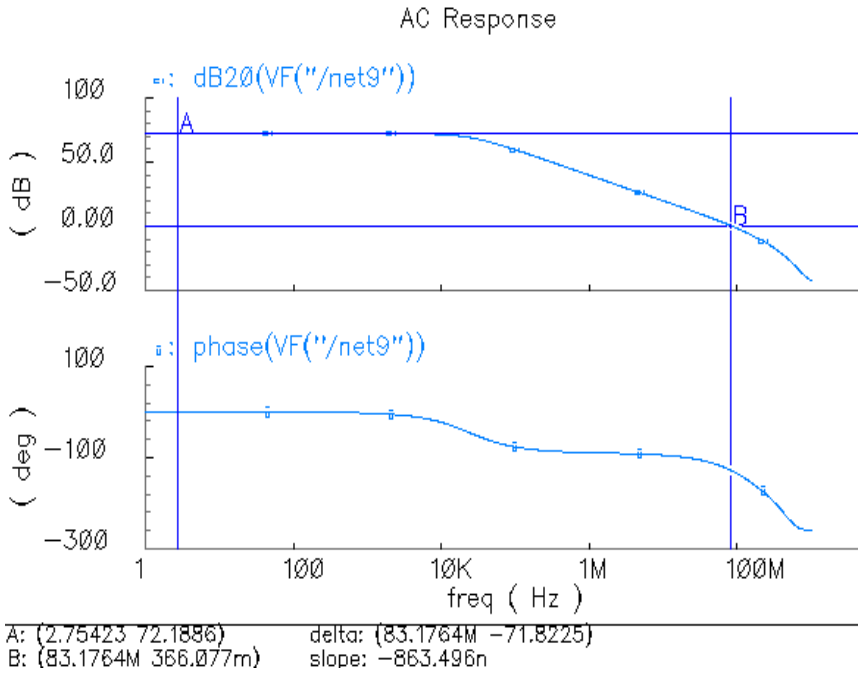


Figure 5.6: DC gain and unity gain bandwidth of the OPAMP.

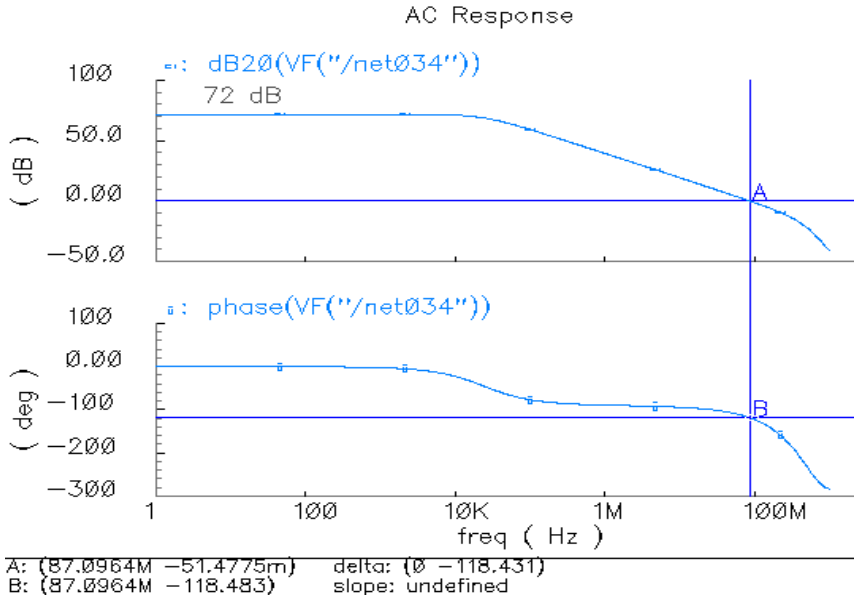


Figure 5.7: Worst case phase margin of the OPAMP.

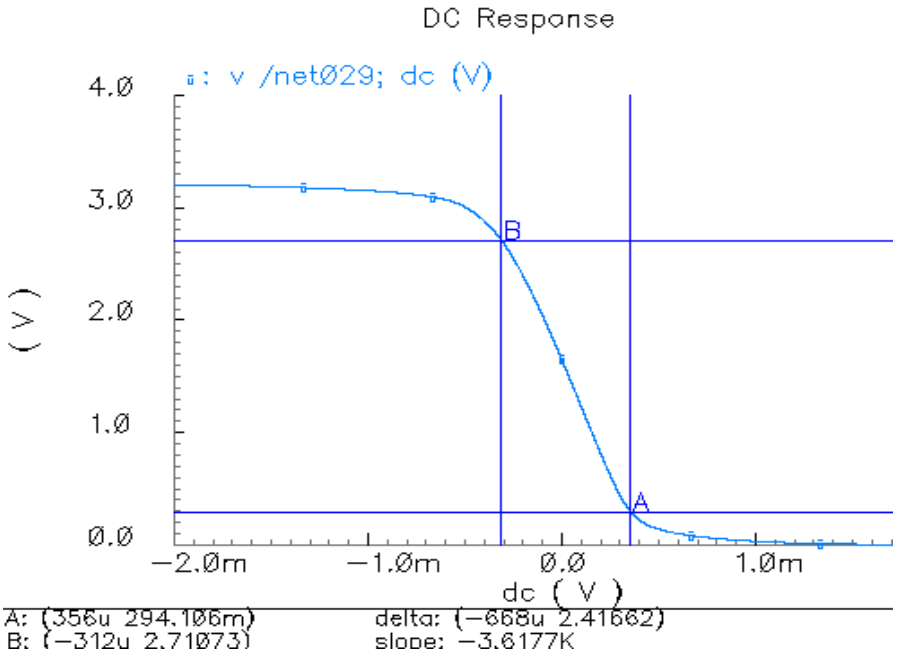


Figure 5.8: Output swing of the OPAMP.

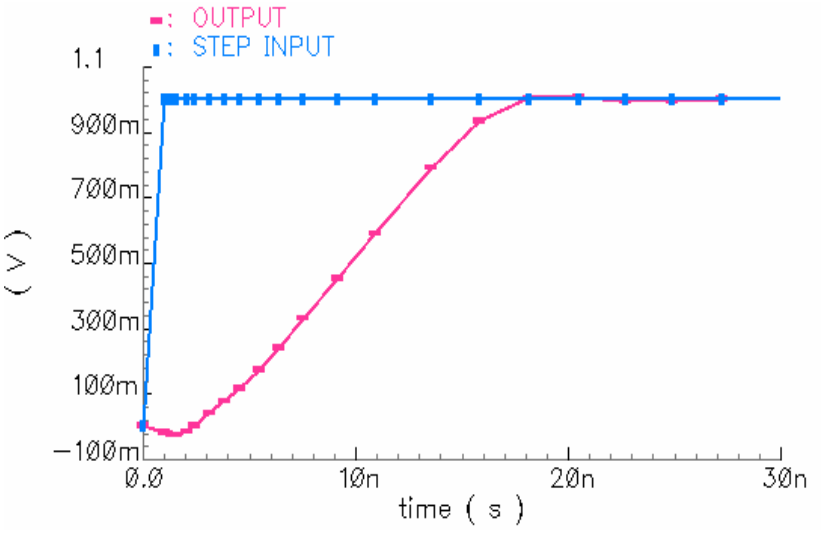


Figure 5.9: Settling time response of the OPAMP.

5.5.3 Fully differential OPAMP design

A fully differential OPAMP was required for the fully differential system. The single-ended OPAMP in the previous section was made fully differential by the addition of a common mode feedback (CMFB) circuit. The schematic of the common mode circuit and the fully differential OPAMP are shown in Figures 5.10 and 5.11 respectively. The biasing circuit shown in Figure 5.5 has also been used to bias the CMFB current source. As shown in Figure 5.11, the common mode feedback has been applied to a split portion of the p-MOS cascode pair in the first stage. The other portion has been biased appropriately. This results in lower power consumption in the CMFB circuit. The total power consumed in the fully differential OPAMP including the CMFB and biasing circuits is approximately 4.3 mW from a supply of 3.3 V .

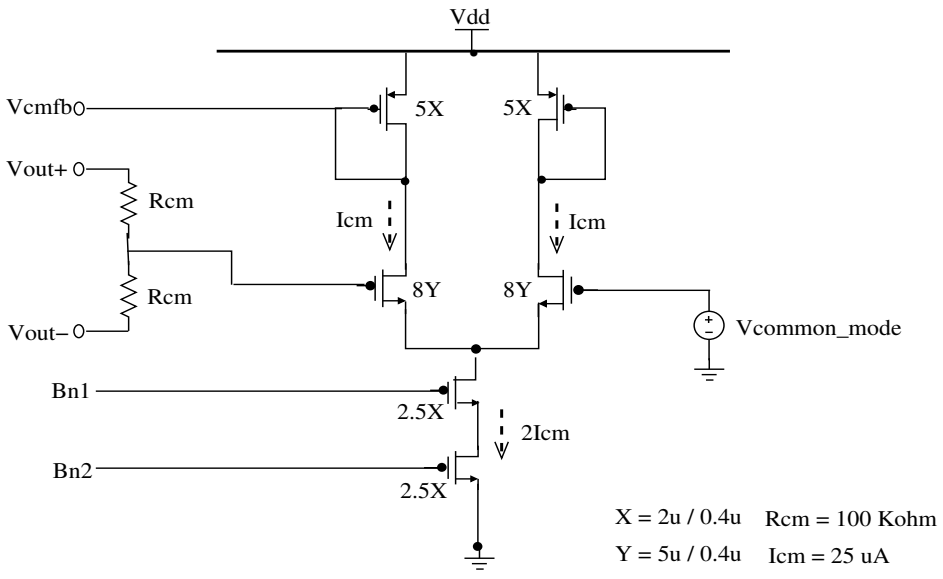


Figure 5.10: Schematic of the common mode feedback circuit for the OPAMP.

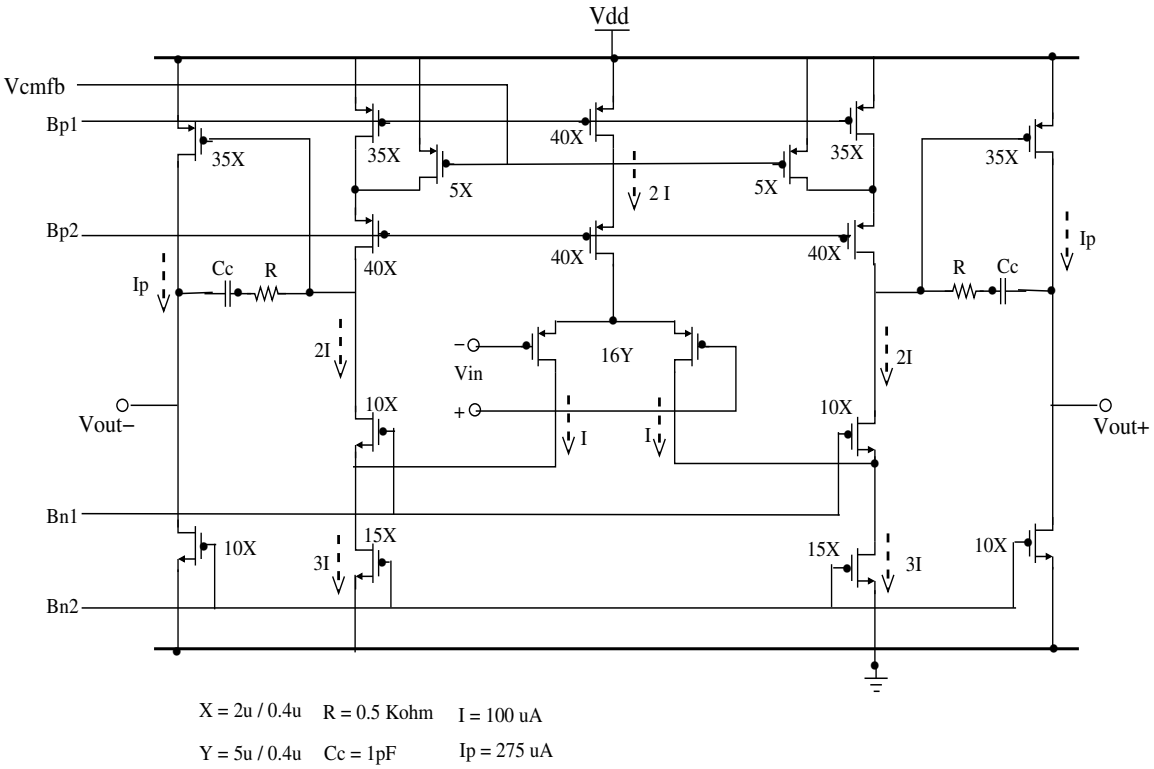
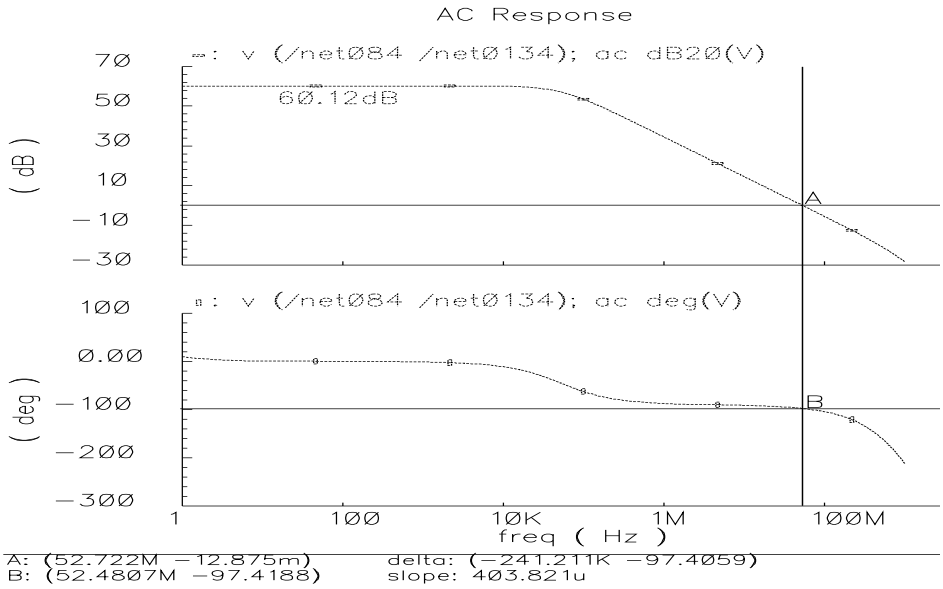
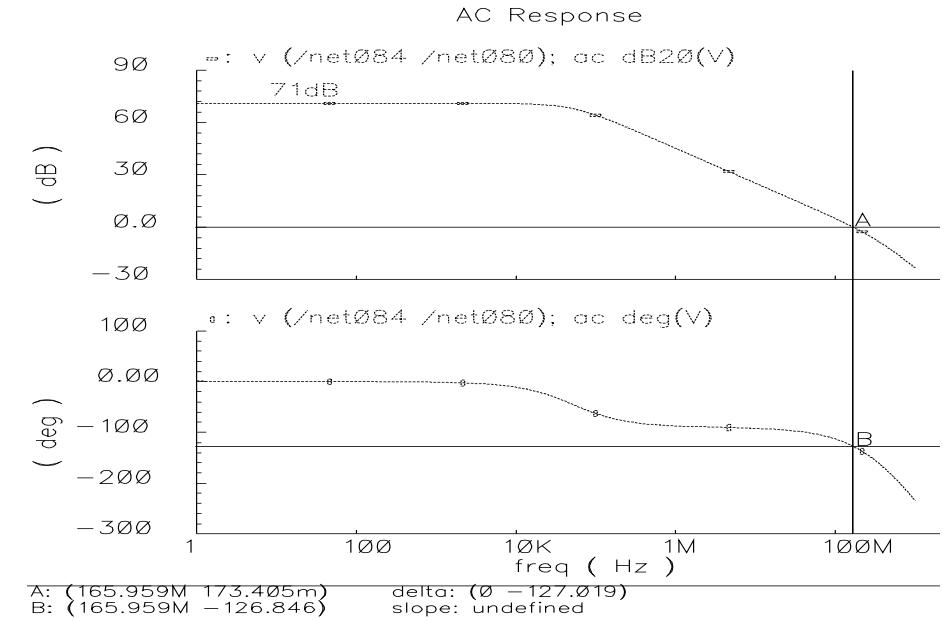


Figure 5.11: Schematic of the fully differential folded cascode OPAMP.

The OPAMP has been used in the fully differential switched capacitor biquad as well as the output buffer, the single-ended versions of which have been shown in Figure 4.12 and Figure 5.3 previously. It is required to operate for different values of input, feedback and load capacitors due to the different circuit conditions during the clock phases. The loop characteristics were simulated for each of these conditions in order to ensure that the OPAMP performs satisfactorily. The worst case loop unity gain bandwidth is 52 MHz for an input



(a) Worst case bandwidth.



(b) Worst case phase margin.

Figure 5.12: Loop ac response of the fully differential OPAMP.

capacitor of 0.5 pF and a feedback capacitor of 0.25 pF. Figure 5.12 (a) shows the loop ac response for the above conditions. The worst case phase margin of 53˚ was obtained for the case of 5.3 pF feedback and 0.5 pF load capacitors. The loop response for this case has been shown in Figure 5.12 (b). Simulated loop gain of the OPAMP is greater than 60 dB for all circuit configurations employed in this system.

The common mode feedback loop response should also be stable. The CMFB loop should have sufficiently large gain and bandwidth, such that it does not limit the overall performance of the OPAMP. The ac response of the CMFB loop has been shown in Figure 5.13. The dc gain across the CMFB loop is 55 dB, its unity gain bandwidth is 24 MHz and the phase margin is 64 ˚.

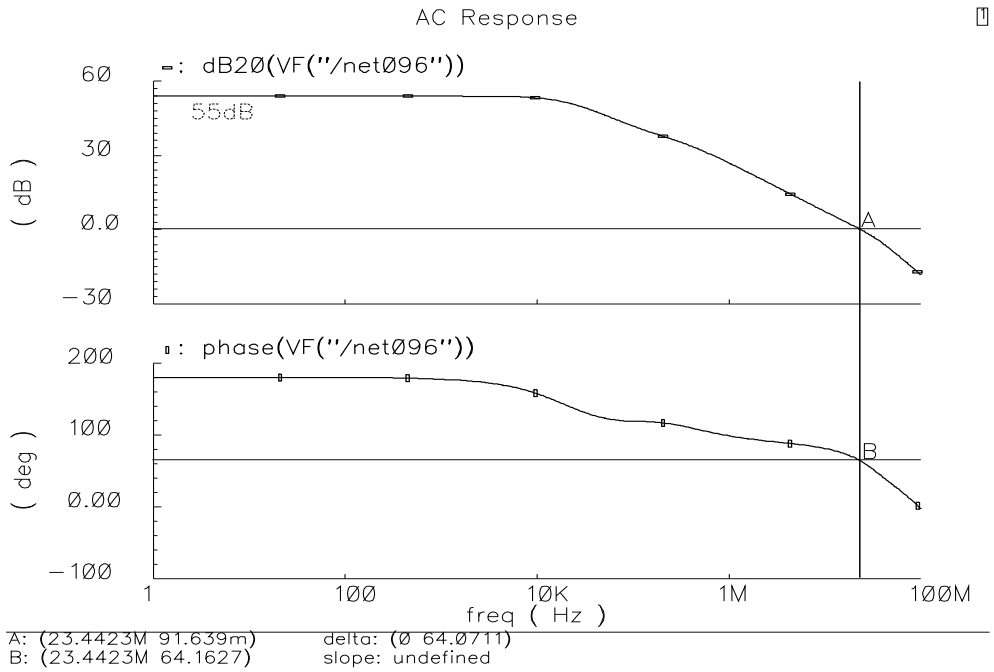


Figure 5.13: AC response for the common mode feedback loop.

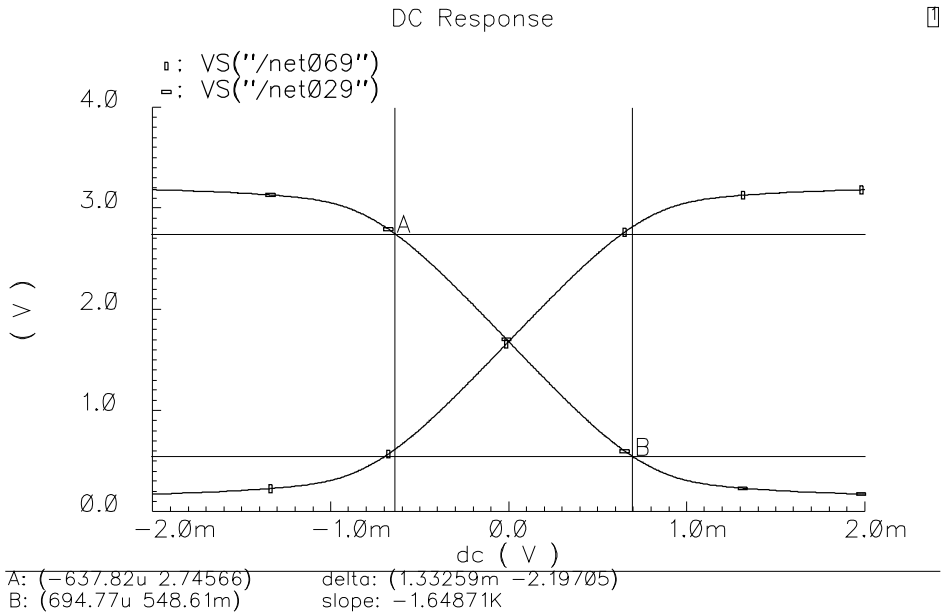


Figure 5.14: Output swing of the fully differential OPAMP.

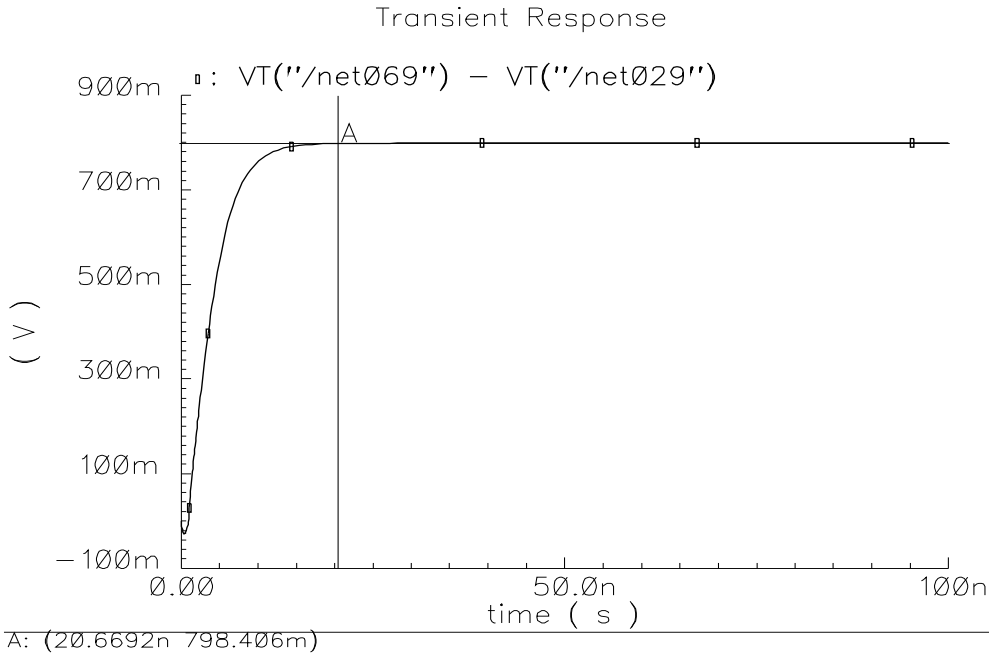


Figure 5.15: Settling time response of the fully differential OPAMP.

The output swing of the fully differential OPAMP is shown in Figure 5.14. The differential swing is approximately 4.2 V. The output of the OPAMP settles to 0.1% of its final value within 22ns. Figure 5.15 illustrates the settling response of the OPAMP for an input capacitor of 0.5 pF and a feedback capacitor of 0.25 pF.

6. RESULTS

6.1 System overview

This research presents the analysis of nonlinear capacitors employed in a 10-bit pipelined, charge redistribution digital-to-analog converter (Q-DAC) designed for audio frequencies. The block diagram of the system has been provided in Figure 6.1. For the purposes of this research the 10-bit Q-DAC and the following switched capacitor filter and an output buffer has been designed. Although a continuous time filter as shown in Figure 6.1 should follow the SCF, it has not been designed for this project.

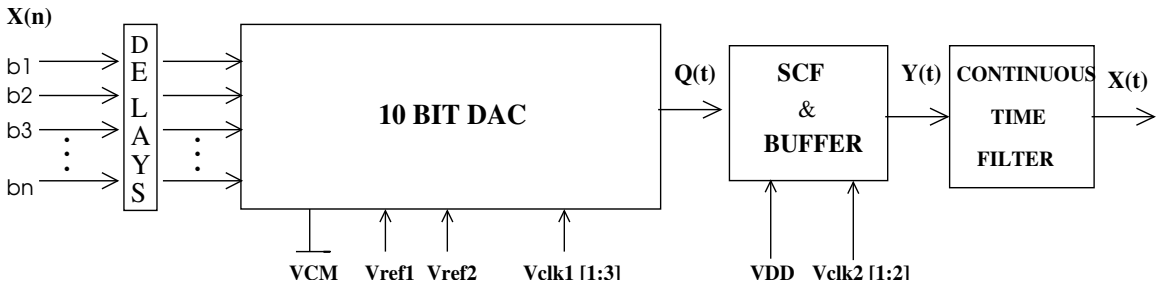


Figure 6.1: Block diagram of the system.

The input to the DAC is a parallel stream of input bits (b1… b_N), the analog equivalent of which represents an audio signal (20Hz-20kHz). The

signal flow graph depicting the propagation of the signal from the digital input bits to the continuous time output is shown in Figure 6.1. The signals have been further illustrated by their time and frequency domain representations in Figure 6.2 below.

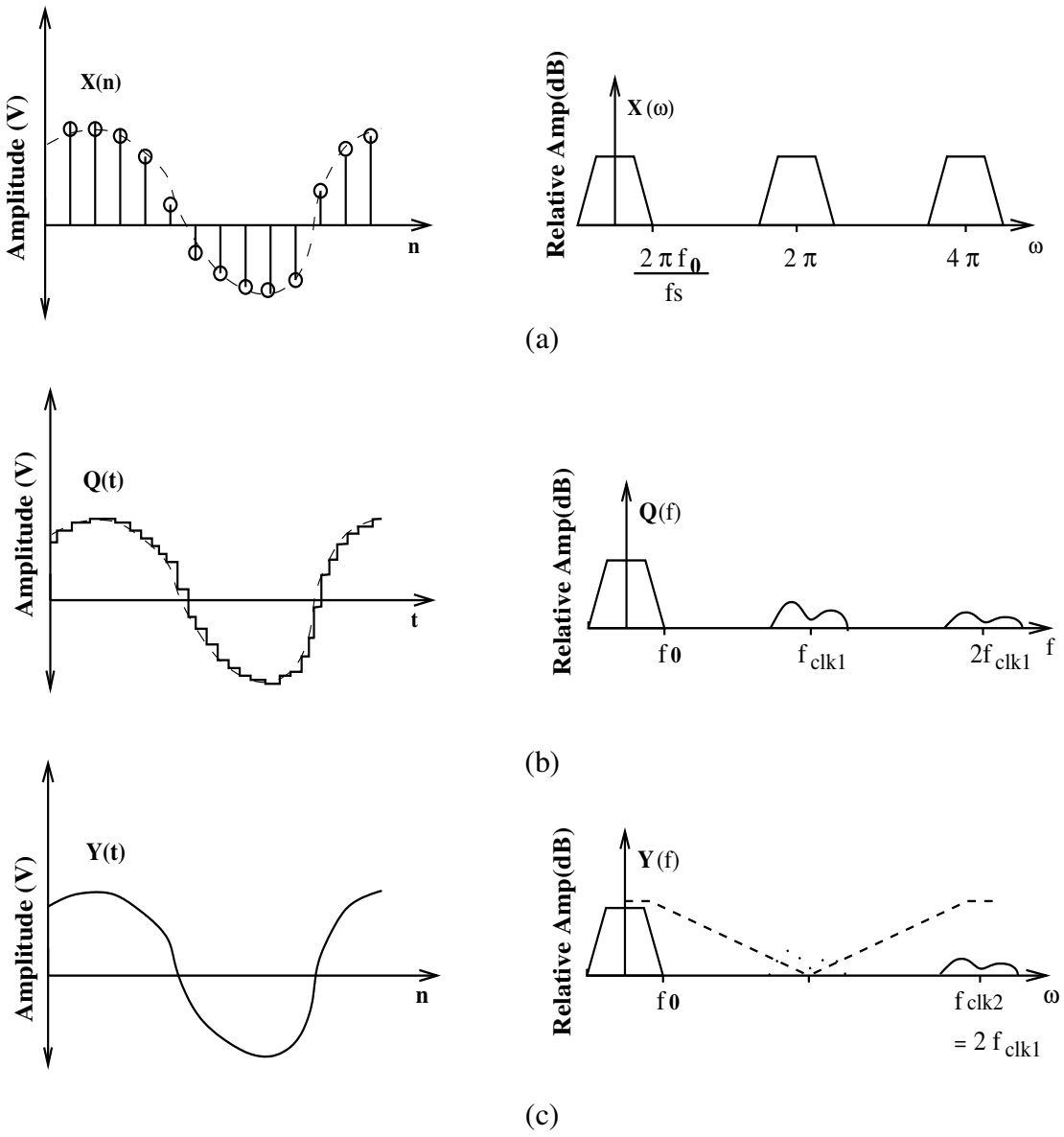


Figure 6.2: Time domain representations and frequency spectrums of (a) input bit stream, X, (b) output of the Q-DAC, Q and (c) output of the SCF and buffer, Y.

A possible time domain representation of the digital signal X (n) is shown in Figure 6.2 (a).The analog equivalent signal, of X is shown as a dotted envelope. The spectrum of the analog equivalent is band limited to a frequency, f_0, which is 20 kHz for an audio signal. The frequency spectrum X (ω) for the digital sequence X (n) sampled at frequency, fs is also shown in Figure 6.2 (a). The frequency fs, for this system is 1MHz.

The time domain representation of the output of the DAC, Q (t) and its frequency spectrum Q (f) are illustrated in Figure 6.2(b). The time domain representation shows the staircase-like appearance of the Q-DAC output. The spectrum shows the images around the Q-DAC's clock frequency, clk1 (1 MHz in this case) and its multiples. The spectrum of the output will also contain several harmonic terms and intermodulation products in addition to the noise floor, which have not been shown in this illustration.

Finally the output of the SCF and buffer block (Figure 6.1) has been shown in Figure 6.2 (c). The time domain representation Y(t) is smoother than Q(t), which signifies that high frequency components have been filtered by the SCF. The Y (f) spectrum illustrates the cancellation of the image around fclk1 due to the attenuation caused by the filter at those frequencies. The frequency response and the cancelled image have also been shown for reference, in dotted lines in Figure 6.2 (c).

The theory and the working principle behind the pipelined charge redistribution DAC has been presented in Chapter 2. A switched capacitor 2^{nd} order

Bessel filter has been chosen to be designed as the smoothing filter. The output buffer acts as an interface to the continuous time filter; it converts the sampled data signal into a continuous time voltage. The design of the filter and buffer has been discussed in detail in Chapter 4. Also, the design details of amplifiers and switches employed in the Q- DAC, SCF and buffer have been discussed in Chapter 5.

6.2 Simulation set-up

TSMC 0.35µm process's model parameters have been used for all simulations. The process is for a supply voltage of 3.3 V. The values of important process parameters have been presented in Section 5.1. All circuit simulations presented here have been performed in SpectreRF. Verilog-A has been employed for behavioral modeling of all ideal elements included in the circuit.

The input to the Q-DAC is a 10-bit parallel stream of digital bits. While a single digital bit stream maybe generated using ideal pulses and can be controlled to provide a desired signal, it is difficult to do so for 10 bits. Hence, an ideal 10-bit analog-to-digital converter (ADC) block was implemented by Verilog-A coding. The ADC generates a parallel stream of 10-bits sampled at a frequency of 1MHz. Figure 6.3 illustrates the bits generated for an analog ramp waveform. Furthermore, the bit complements are generated through ideal NOT gates coded in Verilog-A. Delay blocks required before the digital stream is applied to the Q-DAC have also been implemented with Verilog-A coding [Figure 6.1, Figure 2.4].

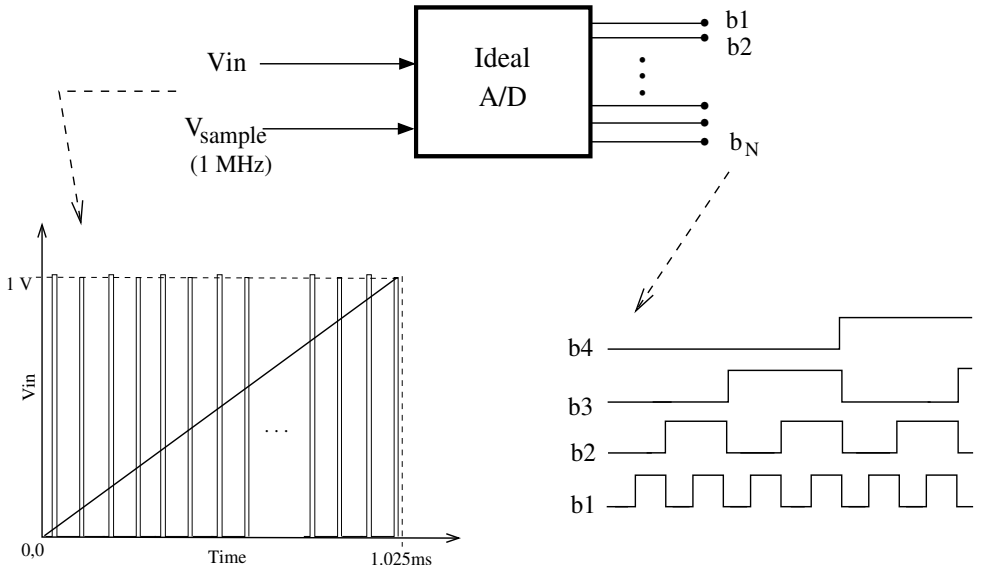


Figure 6.3: Generation of 10-bit parallel input stream.

Ideal voltage sources provide the supply voltages to the OPAMP in the filter and buffer and the reference voltages for the DAC. The non-overlapping phases of the 1 MHz clock required by the Q-DAC switches and the 2 MHz clock required in the filter and buffer switches are provided by appropriately delayed pulse waveforms [Figure 5.2].

6.2.1 Spectrum analysis using dft in SpectreRF

A transient analysis of the system was performed in SpectreRF in order to obtain the output waveform of the system. The precision of the transient simulation and hence the spectrum analysis depends on the magnitude of the time steps used for simulation. It was ensured that the time steps are sufficiently small in

order to correctly simulate the 1MHz and 2MHz clock phases of the DAC and the SCF filter.

SpectreRF's *dft* function, in the waveform calculator was employed for spectrum generation. The *dft* function in SpectreRF computes the discrete Fourier transform of the waveform by FFT (fast Fourier transform) method, implemented using the radix-2 Cooley-Tukey algorithm [6/2], which requires the number of samples to be a power of 2. Additionally, the number of samples should be large enough to accurately represent the output waveform. The selection of the sampling frequency is based on the Nyquist criteria, and should be at least twice the maximum frequency component in the signal. For discrete time applications, the number of samples should be such that the waveform is sampled at a rate much higher that the clock rates in the system. This ensures that the continuous time output waveform is adequately represented.

A 2^{20}-point discrete Fourier transform (DFT) was computed on 11 consecutive cycles of the output to observe its spectrum. The first cycle was neglected to exclude the output prior to the settling [Figure 6.4]. Rectangular (none) windowing was used, which requires that the DFT is performed on an integer number of time periods of the input signal.

6.2.2 Analysis of nonlinearity errors in MATLAB

The nonlinearity errors in the output waveform were computed for an input ramp, similar to the one shown in Figure 6.3. The output of the system, as simulated in SpectreRF was stored and analyzed using MATLAB. The ideal ramp input was employed as a reference to extract the offset and gain errors. The nonlinearity errors were computed from the output, after compensating for the gain and offset errors. A straight line was estimated by endpoints method, for computing the INL errors of the output.

Figures 6.6, 6.10, 6.13, 6.19 and 6.22 in Sections 6.3 and 6.4 show the computed nonlinearity errors for different capacitors employed in the system.

6.3 Performance of the single-ended system

The performance of the single-ended system has been analyzed with transistor level circuits of the Q-DAC, SCF and the output buffer. The input for these transient simulations is the digital equivalent of a 0.8 Vp-p 10 kHz sinusoid. Since the reference voltage (Vref) of the DAC is 1 V, this input corresponds to approximately -2 dBr, (dBr is defined as the ratio of the input signal to the reference voltage of the DAC, and 0 dBr corresponds to an input signal of 1 Vp-p).

6.3.1 Single-ended system with ideal capacitors

For this case, ideal capacitors from analogLib were assumed at the core of the Q-DAC. Figure 6.4 shows the transient output of the sample and held signal at the output of the buffer. The spectrum of this waveform is shown in Figure 6.5. The spurious free dynamic range (SFDR) of the system is approximately 87.6 dB.

The INL and DNL errors were generated from MATLAB for the output when a ramp input was provided to the system. The nonlinearity errors have been shown in Figure 6.6 for the 2^{10} digital codes. The INL and DNL have been represented in terms of LSB, where 1LSB = $1/2^{10}$V.

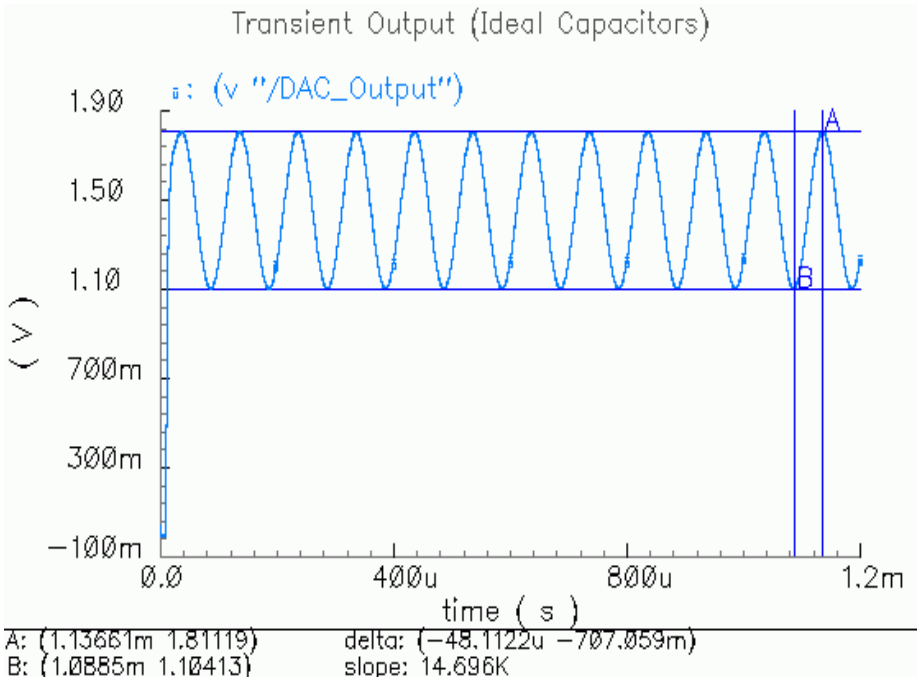


Figure 6.4: Transient output of the single-ended system employing ideal capacitors.

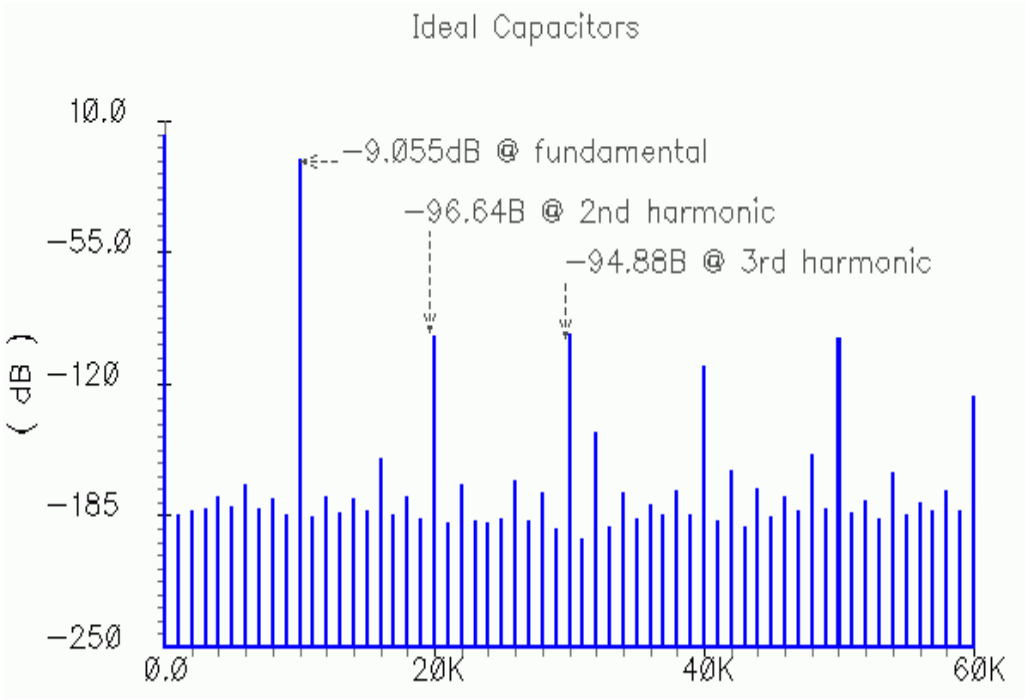


Figure 6.5: Spectrum of the output waveform for ideal capacitors in the single-ended system.

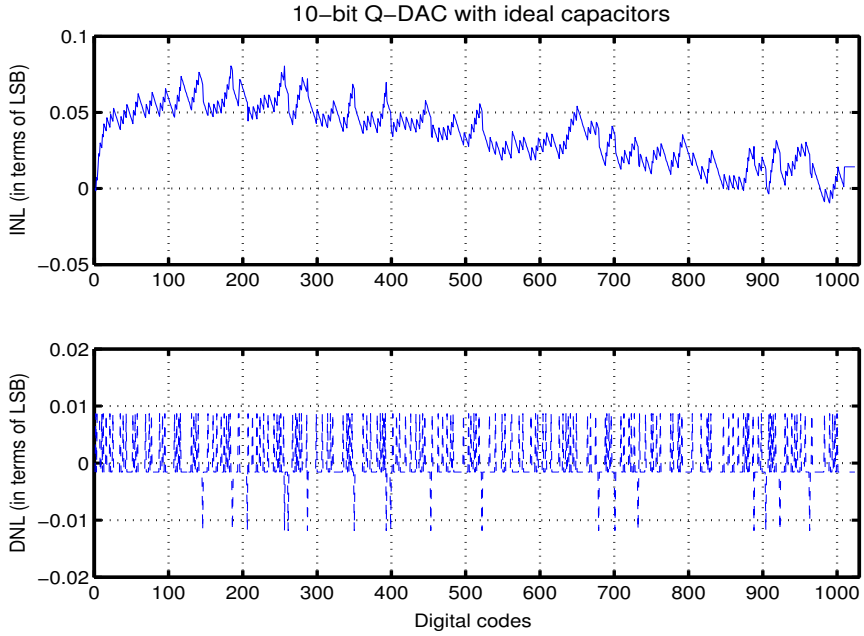


Figure 6.6: INL and DNL errors in case of ideal capacitors in the single-ended system.

6.3.2 Single-ended system with MOS capacitors

The performance of the system was then analyzed with MOSFET gate capacitance employed in the array of capacitors in the Q-DAC. The MOSFET gate capacitance modeled in the BSIM3v3 version of the TSMC 0.35µm process has been employed for the system analysis in this section [Figure 3.1]. A p-MOS transistor, with its drain-source nodes shorted, has been connected between each DAC node and ground, such that the DAC node sees the gate-bulk capacitance. The connection at a single DAC node has been shown in Figure 6.7 for visualization.

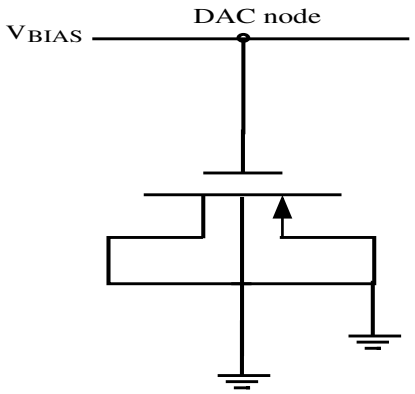


Figure 6.7: Single MOSCAP connected at a Q-DAC node.

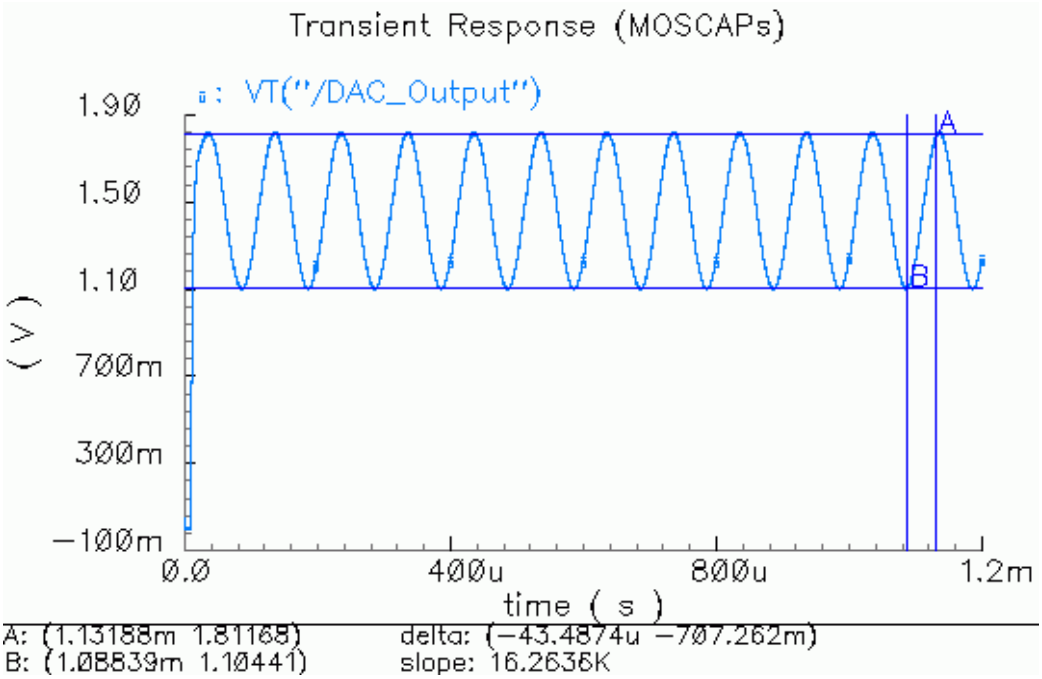


Figure 6.8: Transient output of the single-ended system employing MOS capacitors.

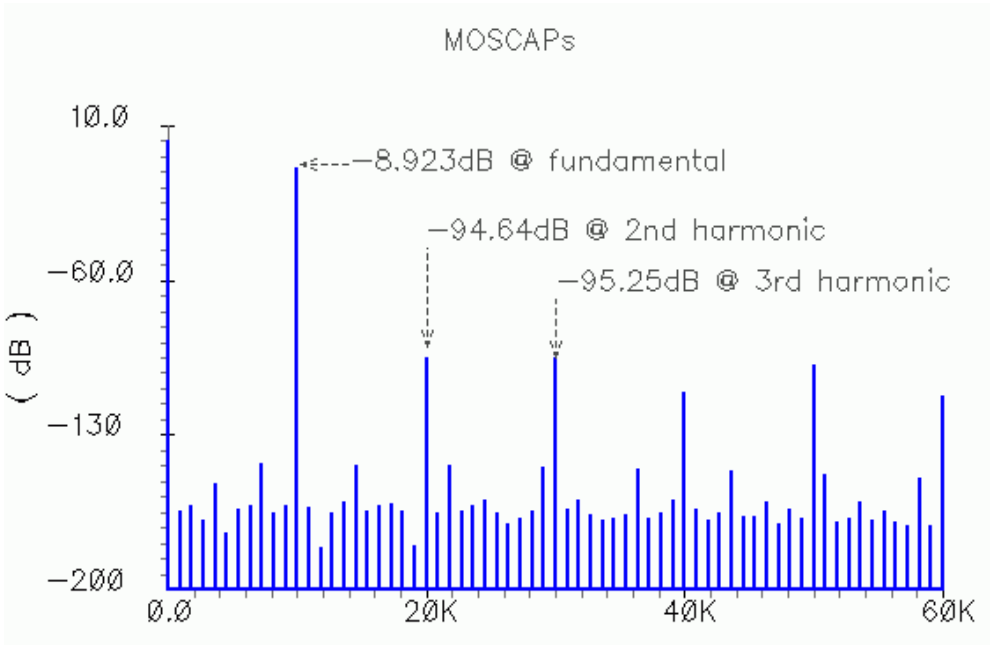


Figure 6.9: Spectrum of the output waveform for MOSCAPs in the single-ended system.

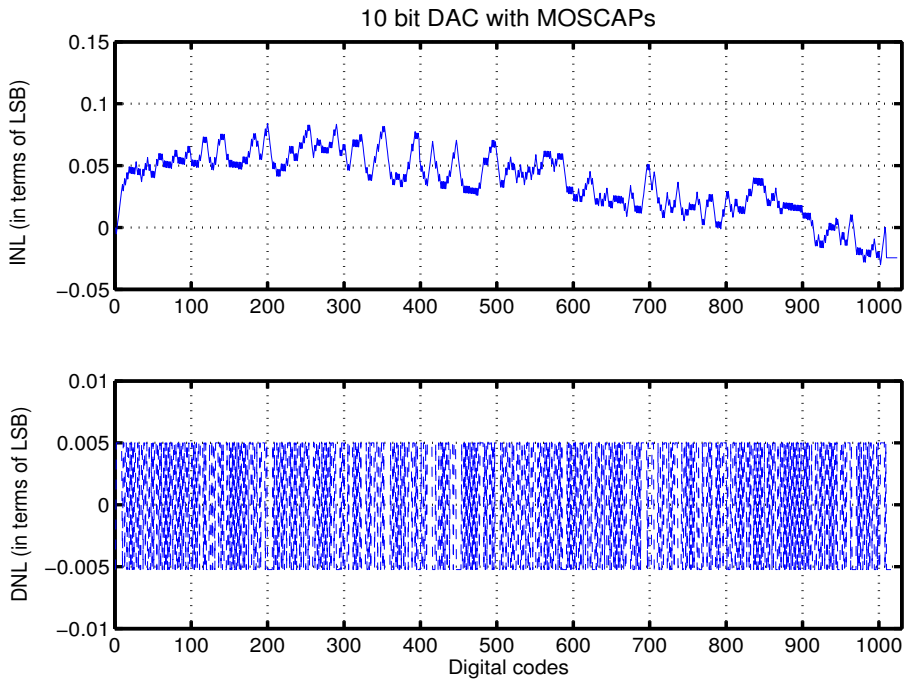


Figure 6.10: INL and DNL errors in case of MOSCAPs in the single-ended system.

The sizes of the p-MOS transistors employed as capacitors in this case are 11.5µm/ 10µm each, which results in a total gate capacitance of approximately 0.5pF when V_{GB} is 1V. The output waveform and its spectrum for this case have been shown in Figures 6.8 and 6.9 respectively. The SFDR achieved is 85.7dB. The nonlinearity errors for this case have been presented in Figure 6.10.

6.3.3 Single-ended system with nonlinear capacitors

Ideally, the biasing point of MOSCAPs should be such that they mostly operate in deep accumulation, where the voltage nonlinearity is small. However, the MOSFET gate capacitance model available does not accurately

reflect this nonlinearity in the deep accumulation region, as observed from the C-V curves [Figure 3.6] [Figure 3.7]. For this reason and also to provide a general estimate of the effects of nonlinear capacitors in this particular application, a more general model has been developed in Verilog-A. The nonlinear capacitor model is ensured to be a charge conserving model [6/1]. The modeling has been discussed in detail in Section 3.3.2.

The nominal value of the capacitor modeled is 0.5pF each. The total nonlinearity is 20% of the nominal value and both 1st and 2nd order nonlinearity have been included.

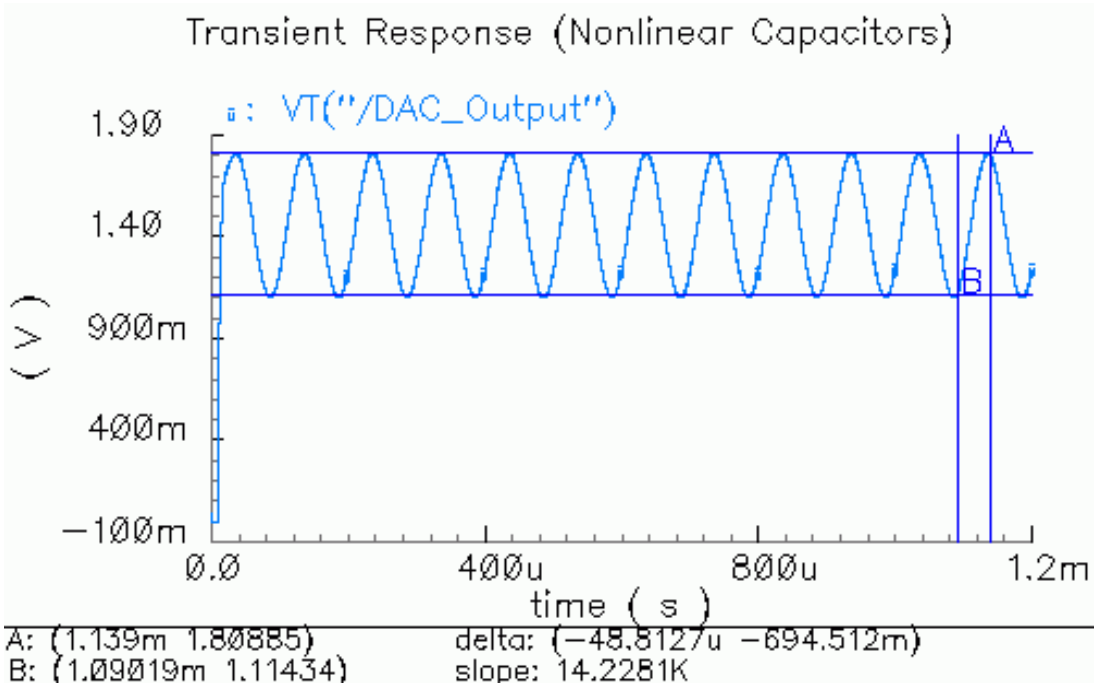


Figure 6.11: Transient output of the single-ended system employing nonlinear capacitors.

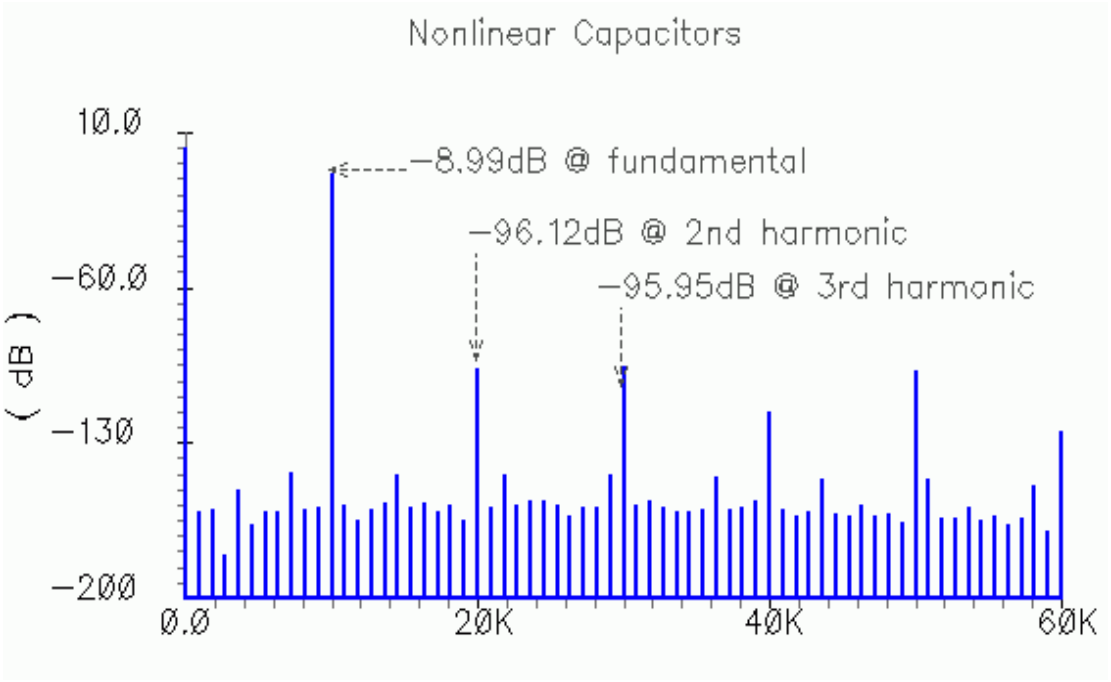


Figure 6.12: Output spectrum for nonlinear capacitors in the single-ended system.

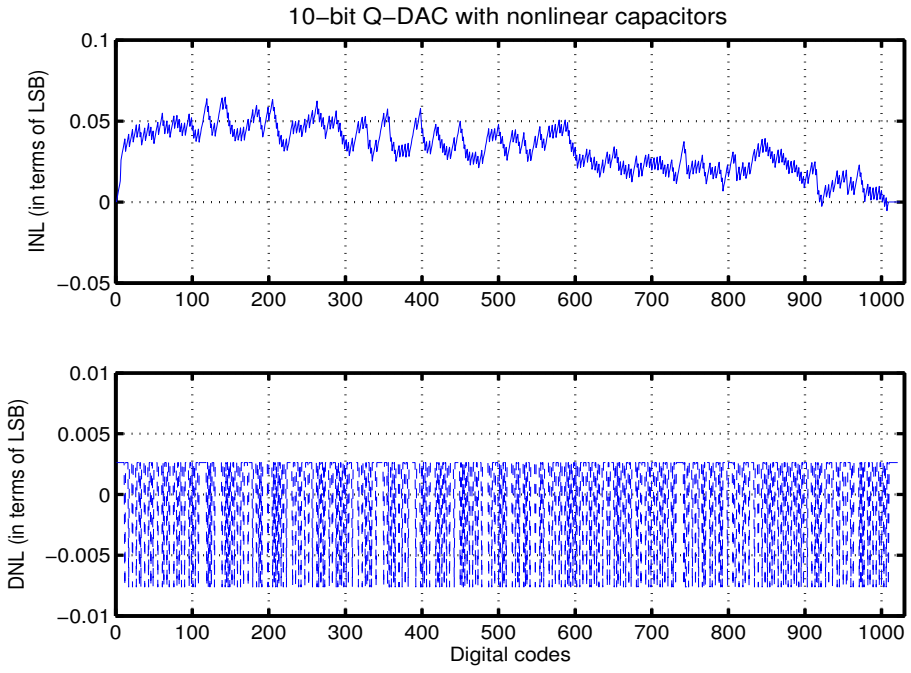


Figure 6.13: INL and DNL errors for nonlinear capacitors in the single-ended system.

Figure 6.11 shows the sampled and held output of the system with the Q-DAC employing nonlinear capacitors. Its spectrum is shown in Figure 6.12 and the SFDR is 87.1 dB. The nonlinearity errors computed are shown in Figure 6.13.

6.4 Performance of the fully differential system

In the fully differential version of the system two Q-DAC structures are required. The second Q-DAC is a replica of the first, except for the fact that it operates on bit complements [6/3]. Fully differential versions of the switched capacitor filter and the output buffer follow the Q-DAC structures, the single-ended versions of which are provided in Figure 4.12 and Figure 5.3, respectively. Two linear capacitors are now employed as feedback capacitors in the output buffer. The fully differential OPAMP described in Section 5.5.3 is employed in the SCF and buffer circuit realizations.

The area required for the differential version as compared to the single-ended version will be approximately doubled, due to twice as many capacitors being required and also the addition of the CMFB circuit in the fully differential OPAMP.

6.4.1 Fully differential system with ideal capacitors

An similar analysis to that in the case of single-ended system results in the waveforms shown in Figure 6.14 of the two output nodes of the differential system. The spectrum of the differential output is shown in Figure 6.15. The SFDR achieved is approximately 87.2 dB, dominated by the third harmonic. The nonlinearity errors of the differential output in the case of a ramp input have been shown in Figure 6.16.

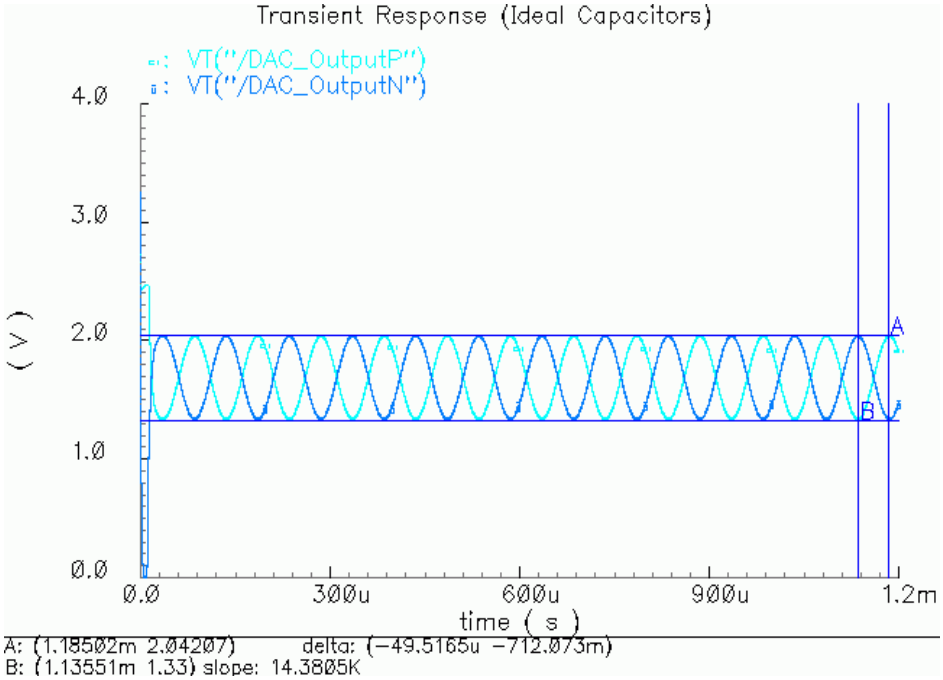


Figure 6.14: Transient waveforms of the positive and negative output nodes of the differential system employing ideal capacitors.

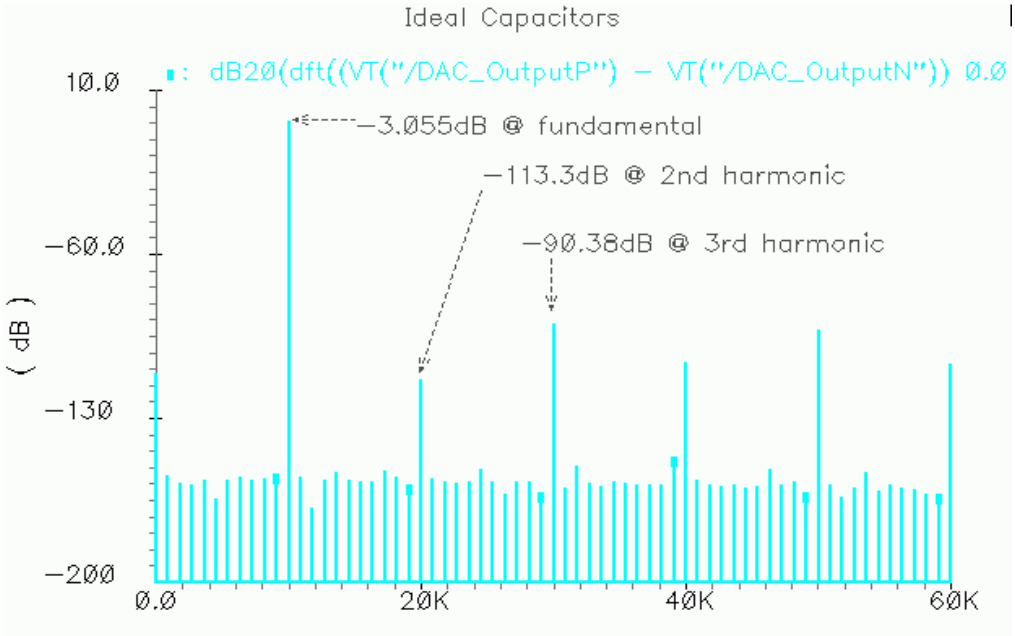


Figure 6.15: Spectrum of the output waveform for ideal capacitors in the differential system.

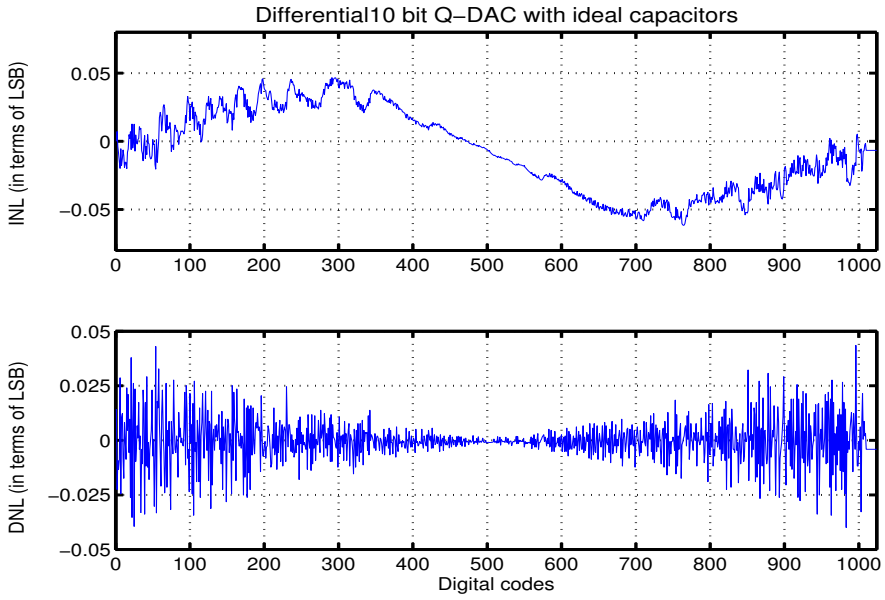


Figure 6.16: INL and DNL errors in case of ideal capacitors in the differential system.

6.4.2 Fully differential system with MOS capacitors

The output waveforms for the case when the ideal capacitors in the Q-DAC are replaced by MOSFET gates capacitors are been presented in Figure 6.17. The MOSCAPs employed are connected as shown in Figure 6.7, for each DAC node in both the Q-DAC structures in the differential system. The sizes of the MOS transistors are 11.5µm/ 10µm each. The spectrum of the differential output is provided in Figure 6.18. The SFDR achieved in the case of MOSCAPs used in the differential system is approximately 86.3 dB. The INL and DNL errors of the differential output as computed in MATLAB are presented in Figure 6.19.

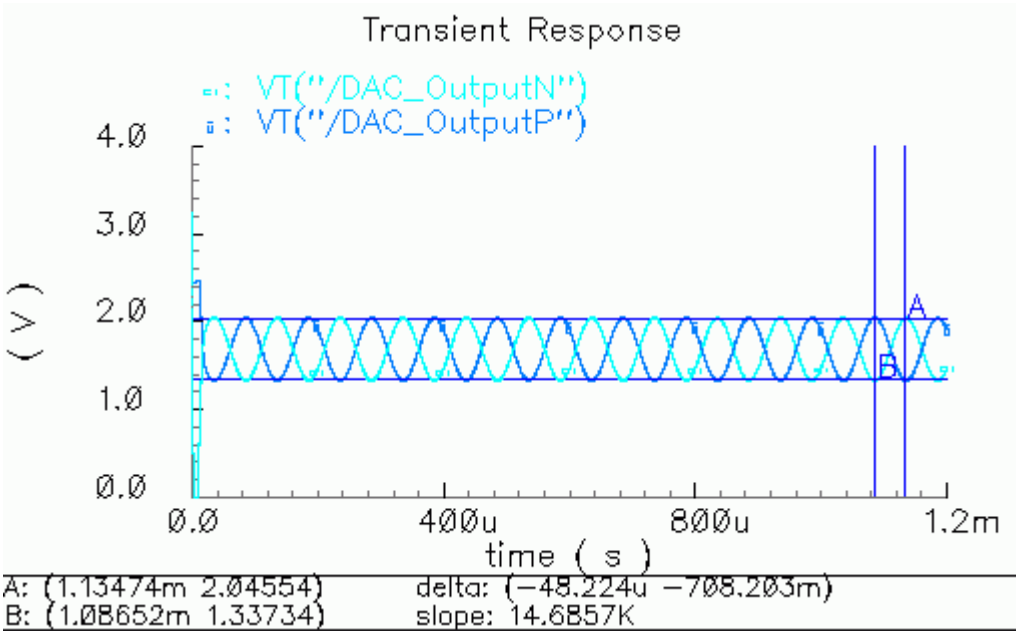


Figure 6.17: Transient waveforms of the positive and negative output nodes of the differential system employing MOS capacitors.

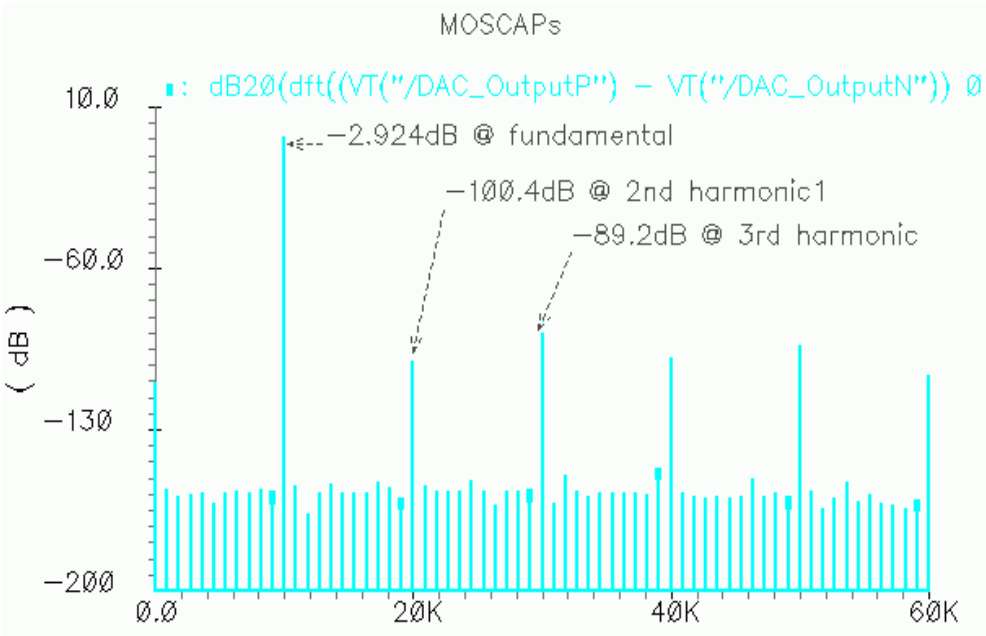


Figure 6.18: Spectrum of the output waveform for MOS capacitors in the differential system.

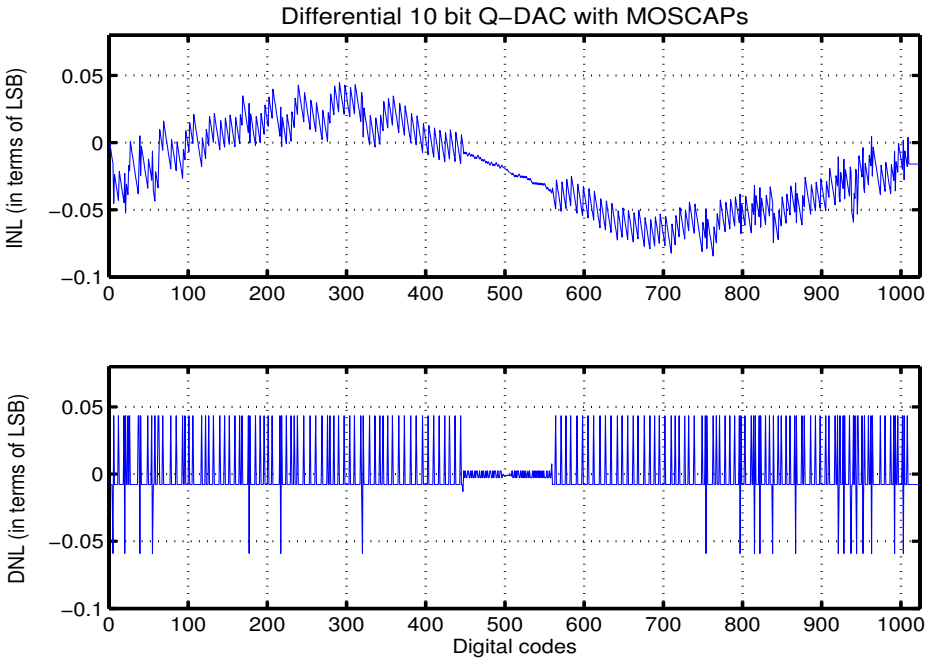


Figure 6.19: INL and DNL errors in case of MOS capacitors in the differential system.

6.4.3 Fully differential system with nonlinear capacitors

The performance of the differential system in the presence of a more general model of a nonlinear capacitor has been provided in this section. The nonlinearity of the capacitor model is 20% of the nominal value of 0.5 pF. Figure 6.20 below shows the output waveforms when ideal capacitors in the system are replaced by nonlinear capacitors. The spectrum of the differential output is presented in Figure 6.21, and shows the SFDR in this case to be 87.9 dB approximately. The nonlinearity errors computed for 2^{20} digital codes are presented in Figure 6.22.

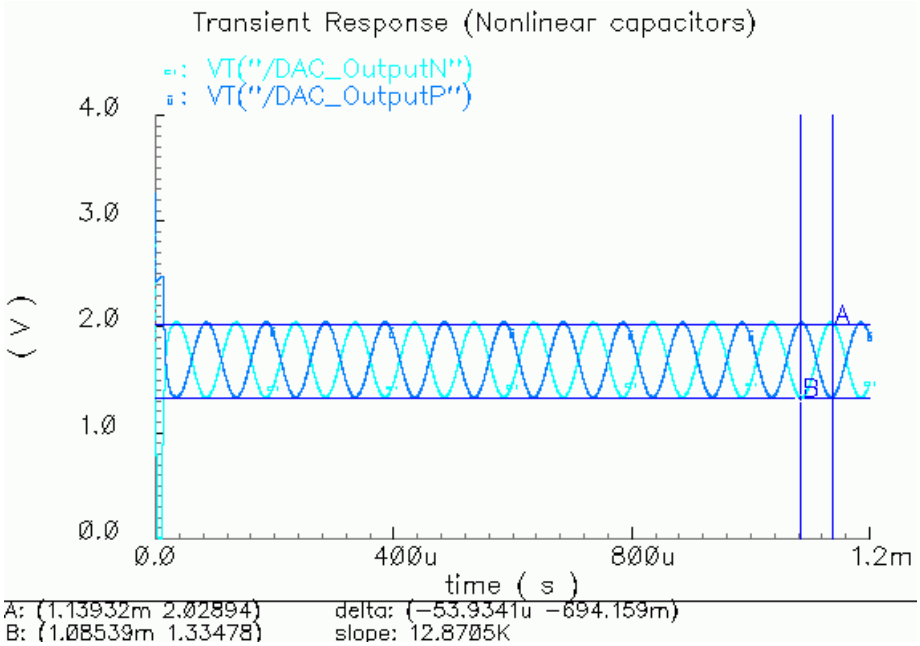


Figure 6.20: Transient waveforms of the positive and negative output nodes of the differential system employing nonlinear capacitors.

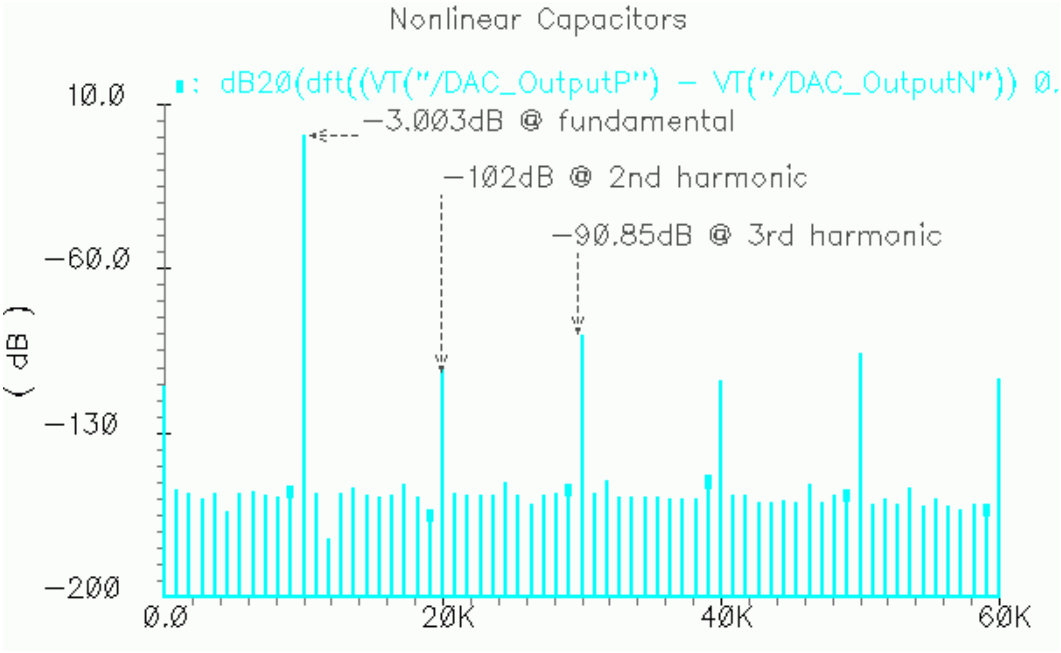


Figure 6.21: Spectrum of the output waveform for nonlinear capacitors in the differential system.

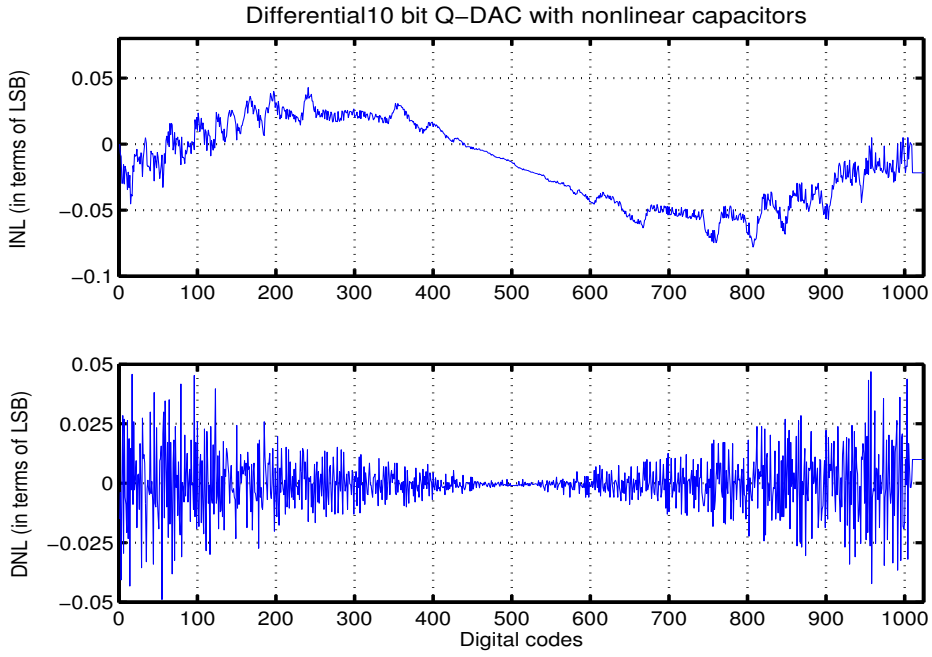


Figure 6.22: INL and DNL errors in case of MOS capacitors in the differential system.

6.5 Summary

The results presented in Sections 6.3 and 6.4 above have been summarized in Tables 6.1 and 6.2 respectively. Table 6.1 provides the simulation results achieved in the simulation of the single-ended system. Single-ended system was analyzed to see the effects of nonlinear capacitors on the 2nd harmonic in the output spectrum. The results show that both, the even and odd harmonics in the spectrum of the system are not increased if linear capacitors in the Q-DAC are replaced by MOSCAPs or any general nonlinear capacitor.

Table 6.1: Summary of the performance of the single-ended system.

Single-ended system			
Performance parameters	Ideal Capacitors	MOSCAPs	Nonlinear Capacitors
Fundamental	-9.055 dB	-8.923 dB	-8.99 dB
2nd harmonic	-96.64 dB	-94.64 dB	-96.12 dB
3rd harmonic	-94.88 dB	-95.25 dB	-95.95 dB
SFDR	85.83 dB	85.72 dB	86.96 dB
Max INL	0.0806 LSB	0.0849 LSB	0.0659 LSB
Max DNL	0.0118 LSB	0.0053 LSB	0.0076 LSB

Table 6.2: Summary of the performance of the differential system.

Fully differential system			
Performance parameters	Ideal Capacitors	MOSCAPs	Nonlinear Capacitors
Fundamental	-3.06 dB	-2.93 dB	-3.00 dB
2^{nd} harmonic	-113.3 dB	-100.4 dB	-102.00 dB
3^{rd} harmonic	-90.38 dB	-89.2 dB	-90.85 dB
SFDR	87.33 dB	86.28 dB	87.86 dB
Max INL	0.0616 LSB	0.0844 LSB	0.0779 LSB
Max DNL	0.0435 LSB	0.0590 LSB	0.0489 LSB

The simulation results of the fully differential system are provided in Table 6.2. In reality a differential structure should only be used for this (or any) DAC, in order to make the output immune to common mode noise or interference signals. The second harmonic in the differential system is greatly reduced, which is as expected, as even harmonics are cancelled in a differential structure. The fundamental in the spectrum of the differential system is 6 dB higher than that in the single-ended system. This is because the differential output voltage has twice the magnitude than that of the positive or negative output node voltages. However SFDR remains the same as distortion is also doubled. The magnitude of the nonlinearity errors for the differential system is almost equal to that in the single-

ended system, as the distortion in the Q-DAC system is dominated by the third harmonic.

Simulations support the theoretical deduction that the charge redistribution DAC is not affected by the nonlinearities of the capacitors employed at its core. Thus, high density capacitors such as MOSCAPs can be employed in this application despite their voltage dependent characteristics.

7. CONCLUSIONS

7.1 Summary

A charge redistribution digital-to-analog converter (Q-DAC) has been designed for this research. The following smoothing filter and a required output buffer circuit have also been designed for the system. The performance of the system for different voltage-dependent nonlinear capacitors has been analyzed. Simulation results verify that the structure of the Q-DAC makes it immune to capacitor nonlinearities. Thus a Q-DAC system employing nonlinear MOSFET gate capacitors will results in a similar performance as compared to that designed using other more linear capacitor structures, such as poly-poly.

Since capacitor nonlinearity does not result in a performance degradation series compensation of capacitors is not required. However, series compensation can be utilized in the input-output branches of the switched capacitor smoothing filter, which can also be designed using MOSCAPs with proper biasing [7/1]. The SCF in the simulation results presented here employs linear capacitors.

The output buffer circuit requires two linear capacitors to convert the charge into an equivalent output voltage. These capacitors can be metal-

insulator-metal (MIM) realizations, available in standard digital processes. MIM capacitors exhibit low densities but are linear in nature.

7.2 Future Work

The results presented in this Thesis suggest that a system involving Q-DAC could be implemented in any digital process by using high density MOS capacitors. Time limitations prevented further analyses of the system including noise simulations and the effect of mismatches in MOSCAPs. Further research should aim at actual chip implementation of the system to obtain the measurement data.

BIBLIOGRAPHY

Chapter 1

[1/1] F.-J. Wang, G.C. Temes, "A Quasi-Passive CMOS Pipeline D/A Converter", IEEE J. Solid State Circuits, Vol. 24, No. 6, June 1989.

[1/2] P. F. Ferguson, Jr., X. Haurie, G. C. Temes, "A Highly Linear Low-Power 10 bit DAC for GSM", Proc. of the IEEE CICC, May, 2000.

[1/3] K. Khanoyan, F. Behbahani, A.A. Abidi, "A 10 b, 400 MS/s glitch-free CMOS D/A converter", Symposium on VLSI Circuits Digest of Technical Papers, June 1999 Page(s):73 – 76.

[1/4] G. Manganaro, Sung-Ung Kwak, A.R. Bugeja, "A Dual 10-b 200-MSPS Pipelined D/A Converter with DLL-Based Clock Synthesizer," IEEE J. Solid State Circuits, Vol. 39, No. 11, Nov 2004.

Chapter 2

[2/1] D. A. John and K. Martin, *Analog Integrated Circuit Design*, Wiley 1997.

[2/2] F. - J. Wang, G. C. Temes, "A Quasi-Passive CMOS Pipeline D/A Converter", IEEE J. Solid State Circuits, Vol. 24, No. 6, June 1989.

[2/3] G. Manganaro, Sung-Ung Kwak, A.R. Bugeja, "A Dual 10-b 200-MSPS Pipelined D/A Converter with DLL-Based Clock Synthesizer," IEEE J. Solid State Circuits, Vol. 39, No. 11, Nov 2004.

[2/4] P. F. Ferguson, Jr., X. Haurie, G. C. Temes, "A Highly Linear Low-Power 10 bit DAC for GSM, " Proc. of the IEEE CICC, May 2000.

[2/5] Fong-Jim Wang, "Architecture and Circuit Design for a Pipeline Data Converter," PhD Thesis, University of California, L. A., 1991.

Chapter 3

[3/1] P. J. Hurst, P. R. Gray, R. G. Meyer, S. H. Lewis, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons Inc, 2001.

[3/2] Hirokazu Yoshizawa, Yunteng Huang, Paul F. Ferguson, Jr., and Gabor C. Temes, "MOSFET-Only Switched-Capacitor Circuits in Digital CMOS Technology," IEEE J. Solid State Circuits, Vol. 34, No. 6, June 1999.

[3/3] M.E. Elta, A. Chu, L.J. Mahoney, R.T. Cerretani, and W.E. Courtney, "Tantalum oxide capacitors for GaAs monolithic integrated circuits," IEEE Electron Device Lett., vol. EDL-3, May 1982.

[3/4] S. Pavan Y., "High Frequency Continuous Time Filters in Digital CMOS Processes", Eng.Sc.D. Thesis Columbia University, 1999.

[3/5] N. Seshan, "Design of low power 2.4GHz CMOS LC balanced oscillators with low phase noise and large tuning range", M.S. Thesis, Oregon State University, 2002.

[3/6] Ken Kundert, "Modeling Varactors," The Designer's Guide Community, Version 4, 19th June 2002.

[3/7] Y. Huang, G.C Temes, H. Yoshizawa., " A High-Linearity Low-Voltage All-MOSFET Delta-Sigma Modulator," IEEE Custom Integrated Circuits Conference, pp. 293-296, May 1997.

Chapter 4

[4/1] G. C. Temes, J.W. La Patra, "Introduction to circuit synthesis and design", McGraw-Hill New York, 1977.

[4/2] P. K. Hanumolu, "Flat Group Delay Analog Low Pass Filter Design", Project Report, OSU, December 2001.

[4/3] R Gregorian, G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. Wiley Series on Filters, Design, Manufacturing, and applications, A Wiley-Interscience publication, New York,1986.

[4/4] K. Martin,"Improved Circuits for the Realization of Switched capacitor Filters," IEEE Trans. Circuits and Systems, April 1980.

[4/5] D.A John and K. Martin, *Analog Integrated Circuit Design*. Wiley 1997.

[4/6] P.F.Ferguson, Jr., X. Haurie, G.C. Temes, "A Highly Linear Low-Power 10 bit DAC for GSM", Proc. of the IEEE CICC, May, 2000.

[4/7] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," In http://www.designers-guide.com/Analysis/sc-filters.pdf

[4/8] David Stoops, "Simulating Switched Capacitor Circuits with SpectreRF," M.S. Project, Oregon State University, 2003.

Chapter 5

[5/1] R Gregorian, G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. Wiley Series on Filters, Design, Manufacturing, and applications, A Wiley-Interscience publication, New York,1986.

[5/2] D.A John and K. Martin, *Analog Integrated Circuit Design*. Wiley 1997.

[5/3] A. Rofougaran, G. Chang, J.J. Rael, J.Y.-C. Chang, M. Rofougaran, P.J. Chang, M. Djafari, M.-K. Ku, E. W. Roth, A.A. Abidi, H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS. I. Architecture and transmitter design", IEEE J. Solid State Circuits, Volume 33, Issue 4, April 1998.

[5/4] G. Manganaro, Sung-Ung Kwak, A.R. Bugeja, "A Dual 10-b 200-MSPS Pipelined D/A Converter with DLL-Based Clock Synthesizer," IEEE J. Solid State Circuits, Vol. 39, No. 11, Nov 2004.

[5/5] Y. Huang, G.C Temes, H. Yoshizawa., " A High-Linearity Low-Voltage All-MOSFET Delta-Sigma Modulator," IEEE Custom Integrated Circuits Conference, pp. 293-296, May 1997.

[5/6] B. Razavi, *Design of Analog CMOS Integrated Circuits.* McGraw-Hill, New York, 2001

[5/7] P. K. Hanumolu, "Design of a Switched Capacitor Filter", Project Report, OSU, March 2002.

[5/8] Ken Martin, Adel S. Sedra, "Effects of the OP Amp Finite Gain and Bandwidth on the Performance of the Switched-Capacitor Filters," IEEE Transactions on Circuit and Systems, August 1981.

[5/9] Un-Ku Moon, "CMOS High-Frequency Switched-Capacitor Filters for Telecommunication Applications," IEEE J. Solid State Circuits, Vol. 35, Issue 2, Feb 2002.

Chapter 6

[6/1] Ken Kundert, "Modeling Varactors," The Designer's Guide Community, Version 4, 19th June 2002.

[6/2] Waveform Calculator User Guide, Product version5, Product documentation, Cadence.

[6/3] G. Manganaro, Sung-Ung Kwak, A.R. Bugeja, "A Dual 10-b 200-MSPS Pipelined D/A Converter with DLL-Based Clock Synthesizer," IEEE J. Solid State Circuits, Vol. 39, No. 11, Nov 2004.

Chapter 7

[7/1] Hirokazu Yoshizawa, Yunteng Huang, Paul F. Ferguson, Jr., and Gabor C. Temes, "MOSFET-Only Switched-Capacitor Circuits in Digital CMOS Technology," IEEE J. Solid State Circuits, Vol. 34, No. 6, June 1999.