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Mobility Assessment of Depletion-Mode Oxide Thin-Film Transistors Using the Comprehensive Depletion-Mode Model

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In an enhancement-mode, n-channel (p-channel) oxide thin-film transistor (TFT), current arises as a consequence of electron (hole) transport within a narrow accumulation layer. The square-law model accurately describes enhancement-mode TFT behavior and establishes the equations appropriate for carrier mobility extraction. In contrast, in a depletion-mode oxide TFT, carrier transport can occur within an accumulation layer and/or within the 'bulk' portion of the channel. The comprehensive depletion-mode model accurately describes depletion-mode TFT behavior and establishes a set of equations, different from those obtained from square-law theory, which can be used for carrier mobility extraction. Simulation reveals that when square-law theory mobility extraction equations are used to assess depletion-mode TFTs, the estimated interface mobility is often overestimated.

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We recently proposed a general procedure for the electrical characterization of oxide thin-film transistors (TFTs). This procedure was advanced so that future researchers are able to avoid common measurement artifacts which would render their oxide TFT electrical assessment unreliable. The intent of the present contribution is to warn of another measurement artifact – mobility overestimation when evaluating a depletion-mode TFT – and to elucidate the subtle nature of this effect via simulation.

As typically defined, the gate turn-on (V_{ON}) and threshold voltage (V_T) of a depletion-mode TFT are negative (positive) for an n-channel (p-channel) TFT. This means that mobile carriers (electrons or holes) are present in the channel even when no gate voltage is applied. Depending on the polarity, an applied voltage can either enhance or deplete the concentration of carriers in the channel of a depletionmode TFT. When the carrier concentration is enhanced by the applied gate voltage, these additional carriers are induced into an accumulation layer existing in close physical proximity to the gate insulator. Thus, two kinds of carriers - interface and 'bulk' - contribute to current in a depletion-mode TFT. The mobility of an interface carrier is expected to be less than the mobility of a 'bulk' carrier due to interface roughness and other types of interface scattering. These considerations, it turns out, often lead to depletion-mode TFT mobility overestimation artifacts since carriers being transported in the 'bulk' (with higher mobility) are inadvertency included in the estimation of gate voltage-induced interface transport.

Elucidation of depletion-mode TFT mobility overestimation artifacts is accomplished by simulation of TFT current – voltage (I-V) characteristics using the comprehensive depletion-mode model.² This model was originally developed for n-channel TFTs. However, we extend and refine this model to p-channel TFT behavior and employ it for the assessment of p-channel oxide TFTs since this topic has elicited a significant amount of recent interest.³⁻²¹

TFT Modeling

Transfer curves and corresponding energy band diagrams distinguishing between enhancement- and depletion-mode TFT behavior are illustrated in Fig. 1. The enhancement-mode case (Fig. 1a and 1c) is the familiar one, in which V_{ON} corresponds to the onset of current as measured on a log (I_D) - V_G transfer curve while the threshold voltage (V_T) is indicative of the flow of appreciable TFT current as measured in the context of an I_D-V_D output curve or an I_D-V_G (linear scale) transfer curve. As noted in Fig. 1c, V_{ON} is the applied

gate voltage corresponding to flatband in the channel layer. Additionally, in an enhancement-mode TFT, subthreshold current flow occurs when the channel is weakly accumulated and interface trapping of carriers is at its maximum effectiveness. Finally, enhancement-mode TFT operation is usually well described using the square-law model.

Although it does not appear to be very well appreciated, depletion-mode TFT operation is distinctly different than that of enhancement-mode TFT operation. For example, Fig. 1d reveals that the log (I_D) - V_G onset voltage corresponds to full depletion of the channel, rather than flatband (Fig. 1c) as is the case for enhancement-mode operation. Thus, we propose to denote this depletion-mode TFT log (I_D) - V_G onset voltage as a turn-off voltage (V_{OFF}) in order to distinguish it from V_{ON} . Additionally, the onset of current flow in an I_D – V_D output curve is most accurately described as a pinch-off voltage (V_{PO}) for a depletion-mode TFT. Drain current flowing between an applied gate voltage of V_{OFF} and V_{PO} corresponds to subpinchoff associated with a situation in which the channel is weakly depleted. Finally, depletion-mode TFT operation is accurately described by the comprehensive depletion-mode model, but not by the square-law model.

A summary of TFT drain current and voltage constraint equations for the square-law model and for the comprehensive

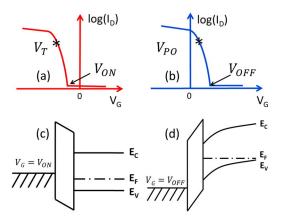


Figure 1. Transfer characteristics for a p-channel (a) enhancement-mode, and (b) depletion-mode TFT, and corresponding energy band diagrams illustrating that (c) V_{ON} corresponds to the flatband voltage for an enhancement-mode TFT, while (d) V_{OFF} corresponds to the applied gate voltage required to fully deplete the channel of a depletion-mode TFT.

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Table I. A summary of p-channel TFT drain current equations and voltage constraint equations for the square-law model and for the comprehensive depletion-mode TFT model.

Model	Drain Current Equation	Voltage Constraint Equation
Square-law model	$I_{D,PRESAT} = -\frac{W}{L} \mu C_G \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]$	$V_G \geq V_T \ V_D < V_{DSAT}$
	$I_{D,SAT} = -\frac{W}{2L} \mu C_G (V_G - V_T)^2$	$V_G \geq V_T V_D \geq V_{DSAT}$
Compre-hensive depletion-mode model	$I_{D,PRESAT}^{DEP} = \frac{W}{L} \sigma h \left\{ \left(1 + \frac{C_S}{C_G} \right) V_D - \frac{2}{3} V_P \left[\left(\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P} \right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P} \right)^{\frac{3}{2}} \right] \right\}$	$0 < V_G \le V_{PO} V_D < V_{DSAT}$
	$I_{D,SAT}^{DEP} = \frac{W}{L} \sigma h \left\{ \left(1 + \frac{C_S}{C_G} \right) V_{DSAT} - \frac{2}{3} V_P \left[\left(\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P} \right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{PO}}{V_P} \right)^{\frac{3}{2}} \right] \right\}$	$0 < V_G \le V_{PO} V_D \ge V_{DSAT}$
	$I_{D,PRESAT}^{ACC} = \frac{W}{L} \left[-\mu_{interface} C_G (V_G V_D - \frac{V_D^2}{2}) + \sigma h V_D \right]$	$V_G \le 0 V_D < V_G < V_{DSAT}$
	$I_{D,PRESAT}^{ACC-DEP} = -\frac{W}{2L} \mu_{\text{interface}} C_G V_G^2 - \frac{W}{L} \sigma h V_G - \frac{W}{L} \sigma h \left\{ \left(1 + \frac{C_S}{C_G} \right) \right\}$	$V_G \le 0 V_G \le V_D < V_{DSAT}$
	$(V_D - V_G) - \frac{2}{3}V_P \left[\left(\frac{C_S^3}{C_G^3} - \left(\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P} \right)^{\frac{3}{2}} \right] \right]$	
	$I_{D,SAT}^{ACC} = -\frac{W}{2L} \mu_{\text{interface}} C_G V_G^2 - \frac{W}{L} \sigma h V_G - \frac{W}{L} \sigma h \left\{ \left(1 + \frac{C_S}{C_G} \right) (-V_{PO}) \right\}$	$V_G \le 0 V_D \ge V_{DSAT}$
	$-\frac{2}{3}V_{P}\bigg[\bigg(\frac{C_{S}^{3}}{C_{G}^{3}}-\bigg(\frac{C_{S}^{2}}{C_{G}^{2}}+\frac{V_{PO}}{V_{P}}\bigg)^{\frac{3}{2}}\bigg]\bigg\}$	
	Model parameters	Equation
	Channel conductance	$\sigma = \mu_{ m bulk} q p_{vo}$
	Threshold voltage	$V_T = -\frac{qp_{to}h}{2C_S} - \frac{qp_{to}h}{C_G}$
	Pinch-off voltage	$V_{PO} = \frac{qp_{vo}h}{2C_S} + \frac{qp_{vo}h}{C_G} \left(V_P = \frac{qp_{vo}h}{2C_S} \right)$
	Saturation voltage	$V_{DSAT} = V_G - V_{PO} \text{ or } V_{DSAT} = V_G - V_T$
	Geometrical-based	$W(width),L(length),h(channelthickness),C_G(gate$
	Channel-based	insulator capacitance density) $p_{vo}(\text{hole concentration in the valence band at zero bias}),$ $p_{to}(\text{empty trap density at zero bias})$ $\mu_{\text{interface (interface mobility)}, \mu_{\text{bulk}}(\text{bulk mobility}),$

depletion-mode model is given in Table I. First consider the square-law model. Ignoring subthreshold, Table I provides analytic drain current relations for a TFT operating in pre-saturation ($I_{D,PRESAT}$) and in saturation ($I_{D,SAT}$). Two common approaches for assessing mobility^{22–24} involve linearizing $I_{D,PRESAT}$ by ignoring the $V_D^2/2$ term in the $I_{D,PRESAT}$ equation given in Table I. Then defining the channel conductance as $G_D = I_D/V_D$, the average mobility, μ_{AVG} , is evaluated using G_D , and the incremental mobility, μ_{INC} , is assessed in terms of the derivative of G_D with respect to V_D , as indicated in Table II. The essential thing to note here is that these mobility assessment procedures depend critically on the viability of the square-law model for describing TFT I-V characteristics. Fortunately, the square-law model works quite well for describing enhancement-mode TFT behavior.

However, the square-law model is not appropriate for depletionmode TFT assessment. Rather, the comprehensive depletion-mode model is a more appropriate model for describing depletion-mode TFT I-V characteristics. Returning to Table I, according to the comprehensive depletion-mode model, the appropriate analytical expression for describing pre-saturation depends on whether the depletion-mode TFT channel is in depletion ($I_{D,PRESAT}^{DEP}$), accumulation ($I_{D,PRESAT}^{ACC}$), or a combination of accumulation and depletion ($I_{D,PRESAT}^{ACC-DEP}$). This means that when the previous procedure for evaluating μ_{AVG} and μ_{INC} is employed, much different mobility expressions are obtained (see Table II) since the comprehensive depletion-mode model pre-saturation drain current analytical equations (i.e., $I_{D,PRESAT}^{DEP}$, $I_{D,PRESAT}^{ACC-DEP}$) differ so dramatically from that of the analytical equation used for square-law modeling of pre-saturation (i.e., $I_{D,PRESAT}$). Notably, in formulating the comprehensive depletion-mode model, two different mobilities - $\mu_{interface}$ and μ_{bulk} - must be introduced to account for differences in carrier mobility at the interface and in the 'bulk'. In general, μ_{bulk} > $\mu_{interface}$ due to enhanced scattering when a carrier is in close physical proximity to an interface.

C_S(channel layer capacitance density)

Table II. Average and incremental mobility equations according to the square-law model and the comprehensive depletion-mode model.

Consequently, mobility overestimation artifacts arise in the assessment of depletion-mode TFTs since (i) the square-law model (upon which mobility assessment is premised) is invalid and (ii) bulk mobility contributions inflate estimates of what is implicitly assumed to be the interface mobility. Simulations based on the comprehensive depletion-mode model are now examined in order to elucidate depletion-mode TFT overestimation artifacts. All simulations are accomplished using MATLAB. The full derivation of the comprehensive depletion-mode model is presented in Ref 2. The general procedure for fitting and parameters extraction begins with V_{PO} extraction from the output curve. Given device dimensions and other known material parameters, an estimation of p_{vo} (hole concentration in the valence band at zero bias) can be determined from the mathematical definition of $V_{PO}.$ Finally, optimization of $\mu_{interface},$ and μ_{bulk} parameters allows for fitting of experimental output and transfer curves. As a final note, although we cannot claim to have accurately and uniquely determine p_{vo} , $\mu_{interface}$, and μ_{bulk} , we have very little leeway in modifying these simulation parameters if we wish to obtain an accurate fit to measured transfer and output curves within the framework of the comprehensive depletion-mode model.

Simulation Results

Consider a p-channel TFT with two different hole concentrations $p_{vo}=10^{15}$ and $10^{18}~cm^{-3}$. The comprehensive depletion-mode model (Table I) is used to simulate the I-V characteristics shown in Figs. 2 and 3 for these two hole concentrations, assuming that $\mu_{interface}=1~cm^2~V^{-1}~s^{-1}$ and $\mu_{bulk}=10~cm^2~V^{-1}~s^{-1}$. Other model parameters employed in these simulations are listed in the captions of Figs. 2 and 3

The drain current-gate voltage ($log(I_D)$ - V_G) transfer curves included in Fig. 2 reveal a turn-on voltage, V_{ON} , of 0 and turn-off voltage, V_{OFF} of 25.5 V for $p_{vo}=10^{15}$ and 10^{18} cm⁻³, respectively. Thus, a low (high) hole concentration leads to enhancement-mode (depletion-mode) TFT behavior.²⁵ In fact, in the limit of low doping as p_{vo} approaches 0, the comprehensive depletion-mode model reverts to the square-law model since $\sigma{\to}0$ and $V_P{\to}0$. The $log(I_D)$ - V_G transfer curves given in Fig. 2 also show that at any given V_G , I_D will be larger for the depletion-mode TFT since more holes are available to conduct current and 'bulk' holes have a higher mobility than gate voltage-induced holes in the accumulation layer. The I_D - V_D output curve shown in the insert of Fig. 2 is simulated for the $p_{vo}=10^{18}$ cm⁻³ case. The corresponding I_D - V_D output curve for $p_{vo}=10^{15}$ cm⁻³ (not shown) display significantly reduced drain current.

Figure 3 shows two simulated $(I_{D,SAT} - V_G)^{1/2}$ transfer curves plotted for $p_{vo} = 10^{15}$ and 10^{18} cm⁻³. The saturation mobility, μ_{SAT} , is estimated as

$$\mu_{SAT} = \frac{m^2}{\frac{W}{2L}C_G},\tag{1}$$

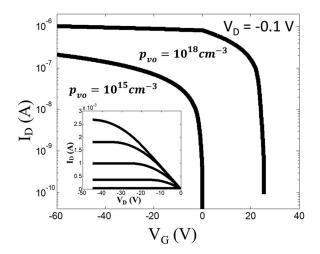


Figure 2. Simulated drain current-gate voltage (log (I_D) - V_G) TFT transfer curves for $p_{vo}=1\times10^{15}$ (left) and 1×10^{18} cm⁻³(right) at $V_D=-0.1$ V. The inset figure shows simulated drain current - drain voltage (I_D - V_D) output curves, in which V_G is increased from -30 V (top curve, showing maximum current) to 20 V in 10 V steps for $p_{vo}=1\times10^{18}$ cm⁻³. Other model parameters used in this simulation are: $\mu_{interface}=1$ cm² V⁻¹ s⁻¹, $\mu_{bulk}=10$ cm² V⁻¹ s⁻¹, W/L=10, h=50 nm, $\epsilon_s=10$, $C_G=3.45\times10^{-8}$ Fcm⁻².

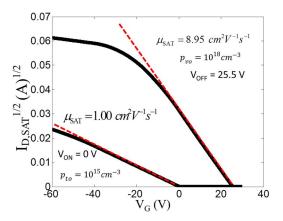
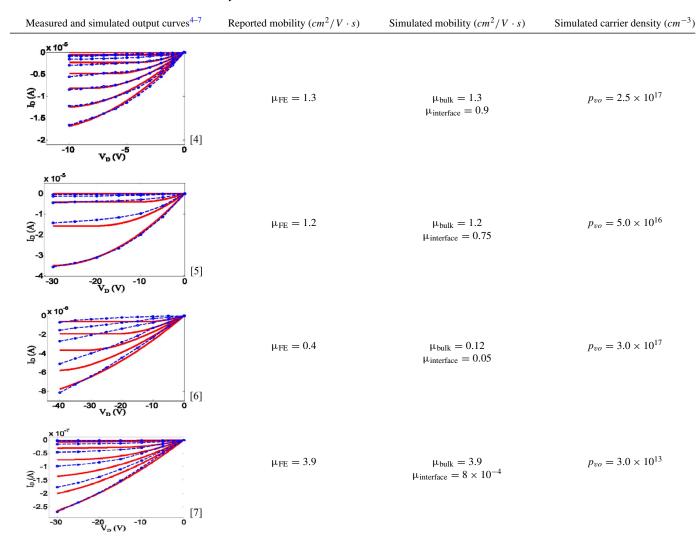


Figure 3. Simulated $(I_D)^{1/2}$ - V_G TFT transfer curves for $p_{vo}=1\times 10^{15}$ (left) and 1×10^{18} cm $^{-3}$ (right) at $V_D=-40$ V. Model parameters used in this simulation are: $\mu_{interface}=1$ cm 2 V $^{-1}$ s $^{-1}$, $\mu_{bulk}=10$ cm 2 V $^{-1}$ s $^{-1}$, W/L = 10, h = 50 nm, $\epsilon_s=10$, and $C_G=3.45\times 10^{-8}$ Fcm $^{-2}$. The dashed line is used to extract the slope of the $(I_D)^{1/2}$ - V_G curve.

Table III. Measured (Blue) and simulated (Red) output curves and mobility estimates for p-channel, depletion-mode TFTs, reported in the literature with $SnO^{4,5}$ and $CuO^{6,7}$ channel layers.



where m is the slope of a regression fit to the straight line portion of the $(I_{D,SAT}$ - $V_G)^{1/2}$ transfer curve. The saturation mobility extraction procedure works well for $p_{\nu o}=10^{15}~cm^{-3},$ yielding a saturation mobility identical to the value of the interface mobility assumed as a simulation parameter. However, this saturation mobility extraction procedure fails miserably for $p_{\nu o}=10^{18}~cm^{-3},$ provided an estimate of the saturation mobility that is much closer to the value of the bulk mobility assumed as a simulation parameter.

Table III shows a comparison between the measured output curves of four p-channel, depletion-mode TFTs reported in the literature and corresponding output curves simulated using the comprehensive depletion-mode model. Reported and simulated mobility estimates are also compared in Table III. Simulations of output curves obtained for SnO channel layers from reference 4 and 5 provide relatively accurately fits to the measured data, indicating that reported mobilities correspond to the 'bulk' mobilities while estimated interface mobilities are $\sim 60\% - 70\%$ of their bulk values. The quality of the simulation fits is less satisfying for the output curves obtained for CuO channel layers from reference 6 and 7, suggesting that these devices may possess some additional non-idealities not accounted for in the simulation. In both of these CuO channel layer cases, simulation suggests that the reported mobilities are significantly overestimated compared to simulated interface mobility estimates.

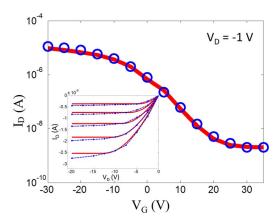


Figure 4 Simulated (red solid line) and measured (blue circle) drain current gate voltage (log (I_D) - V_G) transfer curves for a depletion-mode SnO TFT²¹, using the comprehensive depletion-mode model, including subpinchoff current, off-current, and other components. Model parameters used in this simulation are: $p_{vo} = 1 \times 10^{18} \ cm^{-3}$, $\mu_{interface} = 4.8 \ cm^2 \ V^{-1} \ s^{-1}$, $\mu_{bulk} = 6.75 \ cm^2 \ V^{-1} \ s^{-1}$, W/L = 1, $h = 15 \ nm$, $\epsilon_s = 10$, $C_G = 5.6 \times 10^{-8} \ Fcm^{-2}$, $C_{DOS} = 6.8 \times 10^{-6} \ Fcm^{-2}$ (S = \sim 7.2 V/decade), $R_{surface} = 2 \times 10^9 \ \Omega$, and $V_D = -1 \ V$. The inset figure is a set of simulated (red solid line) and measured (blue circle) drain current - drain voltage ($I_D - V_D$) output curves in which $V_D = -8$, -6, -4, -2, and 0 V from bottom to top.

Table IV. A summary of drain current and voltage constraint equations used to incorporate the subpinchoff current into the simulation of a p-channel, depletion-mode TFT transfer curve. Identical equations are applicable for square-law modeling of p-channel, enhancement-mode TFT except that V_{OFF} is replaced by V_{ON} and C_{DOS} is replaced by C_{IT} , the interface trap capacitance.²⁶

Voltage Constraint Equation

$$I_{OFF} = V_D \left(\frac{1}{R_{\text{surface}}} + \frac{1}{R_{bulk}} \right) + I_G$$

$$V_G \ge V_{OFF}$$

$$I_{D,SUB} = \frac{W}{L} \mu C_G \left(\frac{k_B T}{q} \right)^2 \exp \left[\frac{q \left(V_G - V_{OFF} \right)}{\left(1 + \frac{C_{DOS}}{C_G} \right) k_B T} \right] \left(1 - e^{\frac{-q V_D}{k_B T}} \right)$$

$$\frac{1}{I_D} = \frac{1}{I_{D,PRESAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$$

$$V_G \le V_{OFF} V_D > V_{DSAT}$$

$$\frac{1}{I_D} = \frac{1}{I_{D,SAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$$

$$V_G \le V_{OFF} V_D \le V_{DSAT}$$

 R_{surface} (surface resistance), R_{bulk} (bulk resistance),

 I_G (gate leakage current),

 C_{DOS} (channel layer density of states capacitance density)

Figure 4 shows measured and simulated I_D -V_D output curves and log (I_D) - V_G transfer curves for a SnO depletion-mode TFT. Simulations are accomplished using the comprehensive depletion-mode model in conjunction with subpinchoff and off current contributions, using the procedure summarized in Table IV. The simulation fit is quite good. Simulated interface and bulk mobilities are 4.8 and 6.75 cm 2 V $^{-1}$ s $^{-1}$, respectively, suggesting that the reported channel mobility of 6.75 cm 2 V $^{-1}$ s $^{-1}$ is a bit overestimated. A notable and undesirable aspect of the transfer curve shown in Fig. 4 (and of all p-channel oxide TFTs reported to date) is the very large off current (i.e., $I_{OFF} = 2$ nA), leading to very small drain current on-to-off ratios ($I_D^{ON-OFF} = 5 \times 10^3$ for the transfer curve shown in Fig. 4). I_{OFF} is simulated (see Table IV) by specifying that $R_{surface} = 2 \times 10^9~\Omega$ since the reported gate current is negligible ($\sim 10^{-12}~A$) and $R_{bulk} \approx$ $10^{11}~\Omega$ (assuming a bulk mobility of 6.75 cm² V⁻¹ s⁻¹ and a carrier concentration equal to the intrinsic carrier concentration of a ~ 0.7 eV bandgap semiconductor, 4 i.e., $n_i(SnO) = \sim 7 \times 10^{12} \text{ cm}^{-3}$). This relatively low value of the simulation parameter R_{SURFACE} is likely a consequence of enhanced leakage associated with grain boundaries in the polycrystalline layer since enhanced leakage is known to occur in polycrystalline silicon TFTs.2

Conclusions

Mobility artifacts for p-channel, depletion-mode TFTs are elucidated using the comprehensive depletion-mode model. Mobility in depletion-mode TFT is often overestimated due to 'bulk' mobility contributiones to carrier transport.

Acknowledgments

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References

- 1. J. F. Wager, Journal of the SID. 18/10, 749 (2010).
- 2. D. Hong, G. Yerubandi, H. Q. Chiang, M. C. Spiegelberg, and J. F. Wager, Crit. Rev. Solid State Mater. Sci. 33, 101 (2008).

- 3. K. Matsuzaki, K. Nomuran, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. Lett. 93, 202107-1 (2008).
- 4. Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. lett. 93, 032113-1 (2008).
- 5. E. Fortunato, R. Barros, P. Barquinha, V. Figueiredo, S. K. Park, C. Hwang, and R. Martins, Appl. Phys. lett. 97, 052105-1 (2010).
- 6. S. Sung, S. Kim, K. Jo, J. Lee, J. Kim, S. Kim, K. Chai, S. J. Pearton, D. P. Norton, and Y. Heo, Appl. Phys. Lett. 97, 222109-1 (2010).
- 7. E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Goncalves, S. K. Park, C. Hwang, and R. Martins, Appl. Phys. Lett. 96, 192102-1 (2010).
- X. Zou, G. Fang, L. Yuan, M. Li, W. Guan, and X. Zhao, IEEE Electron Dev. Lett. 31, 827 (2010).
- 9. H. Lee, H. Kim, and C. Kim, Jpn. J. Appl. Phys. 49, 020202-1 (2010).
- 10. H. Yabuta, N. Kaju, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, Appl. Phys. lett. 97, 072111-1 (2010).
- 11. L. Y. Liang, Z. M. Liu, H. T. Cao, Z. Yu, Y. Y. Shi, A. H. Chen, H. Z. Zhang, Y. Q. Fang, and X. L. Sun, J. Electrochemical Society, 157, H598 (2010).
- 12. C. Ou, Dhananjay, Z. Y. Ho, Y. Chuang, S. Cheng, M. Wu, K. Ho, and C. Chu, Appl. Phys. lett. 92, 122113-1 (2008).
- 13. E. Fortunato and R. Martins, Phys. Status Solidi RRL. 9, 336 (2011).
- 14. X. Zou, G. Fang, J. Wan, X. He, H. Wang, N. Liu, H. Long, and X. Zhao, IEEE trans. Electron Dev. 58, 2003 (2011).
- 15. K. Nomura, T. Kamiya, and H. Hosono, Adv. Mater. 23, 3431 (2011).
- 16. Z. Q. Yao, S. L. Liu, L. Zhang, B. He, A. Kumar, X. Jiang, W. J. Zhang, and G. Shao, Appl. Phys. lett. 101, 042114-1 (2012).
- 17. D. Nam, I. Cho, J. Lee, E. Cho, J. Sohn, S. Song, and H. Kwon, J. Vac. Sci. Technol. **B** 30, 060605-1 (2012).
- 18. R. Martins, V. Figueiredo, R. Barros, P. Barquinha, G. Goncalves, L. Pereira,
- I. Ferreira, and E. Fortunato, *Proc. of SPIE*, **8263**, 826315-1 (2012).

 19. L. Y. Liang, Z. M. Liu, H. T. Cao, W. Y. Xu, X. L. Sun, H. Luo, and K. Cang, *J. Phys.* D: Appl. Phys. 45, 085101 (2012).
- 20. S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, and H. K. Cho,
- ACS Appl. Mater. Interfaces 5, 2417 (2013). 21. J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato,
- U. Schwingenschlogl, and H. N. Alshareef, ACS Nano, 7, 5160 (2013).
- 22. S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd edition, p.308, John Wiley & Sons, New York (2007).
- 23. R. L. Hoffman, J. Appl. Phys. 95, 5813 (2004).
- 24. R. L. Hoffman, Solid-State Electronics 49, 648 (2005).
- 25. L. Liu, J. Chen, J. Jeng, and W. Chen, Electrochem. Solid State Science and Technology 2, 59 (2013).
- 26. J. F. Wager and B. Yeh, Oxide thin-film transistors: device physics, Semiconductors and Semimetals, 88, 283 (2013).
- 27. B. Inigues, T. Ytterdal, T. A. Fjeldly, M. S. Shur, and Y. Kuo, Thin film transistors materials and processes, volume 2, polycrystalline silicon thin film transistors, p.95, Kluwer Academic Publishers, Massachusetts (2004).