AN ABSTRACT OF THE DISSERTATION OF

Jiaming Lin for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on July 8, 2013.

Title: Design Techniques for Low Power High Speed Successive Approximation Analog-to-Digital Converters.

Abstract approved:

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Gabor C. Temes

This dissertation presents two high-speed pipeline successive approximation analog-to-digital converters (SAR ADCs). Capacitive DACs and resistive DACs are utilized in these two pipeline SAR ADCs, respectively.

The pipeline SAR ADC with capacitive DACs can save 50% switching power compared with other time-interleaved SAR ADCs since the total capacitance of the DACs in this ADC is more than 50% less than the conventional time-interleave ones. Several switching techniques are implemented to alleviate the impact from the parasitic capacitance and improve the performance.

The pipeline SAR ADC with resistive DACs overcomes the influence from the parasitic capacitance with negligible static power consumption on the resistive DACs. Also, the complicated switching techniques can be avoided to simplify the timing logic.

To verify the above two architectures, two chips were designed and fabricated in 40nm CMOS process.

Finally, a new architecture of multi-step capacitive-splitting SAR ADC is proposed for low power applications. By using two identical capacitor-splitting capacitor arrays, the switching power and capacitor area can be reduced significantly.

Design Techniques for Low Power High Speed Successive Approximation Analog-to-Digital Converters

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APPROVED:

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Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Jiaming Lin, Author

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TABLE OF CONTENTS

Page

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

Design Techniques for Low Power High Speed Successive Approximation Analog-to-Digital Converters

1 Introduction

1.1 Motivation

As the interface between nature world (analog signal) and the digital world (digital signal), the analog-to-digital converter (ADC) is one of the most important blocks in the circuit. The ADC is used to quantize the continuous analog signal into the numerical digital words. According to the sampling theorem, in order to reconstruct the input signal from the sampled one, the sampling frequency needs to be at least twice the signal bandwidth, i.e., $f_s > 2f_B$.

With broad-market demand, especially in digital high-speed links, the high-speed, yet energy-efficient ADCs at minimum area are justified.

Currently, portable devices are become more and more popular. Low power dissipation is also a stringent requirement for these portable devices, since battery life is one of the most critical specifications. Also, because of the integration of massive amounts of analog blocks as well as digital blocks, it is one of the most important cost issues to remove heat produced on chip.

1.2 ADC Architecture

As shown in Fig. 1-1, there are several types of ADCs [1-1]. Incremental, dual-slope and delta-sigma ADCs are very suitable for high-resolution but low-speed application due to the oversampling. If the signal bandwidth is several hundred megahertz, since the oversampling ratio is usually larger than 8, the sampling clock frequency should be larger than several tens gigahertz so that the ADC will be very power-hungry. Therefore, for high-speed application, flash and pipeline ADCs are very popular. However, the number of comparators is proportional to 2^N, where N is the resolution of the ADC, which means the power consumption of the comparator is huge even for medium-resolution application. Since there are many active blocks, such as opamps, in the pipeline ADC, it is not a good candidate for low-power applications.

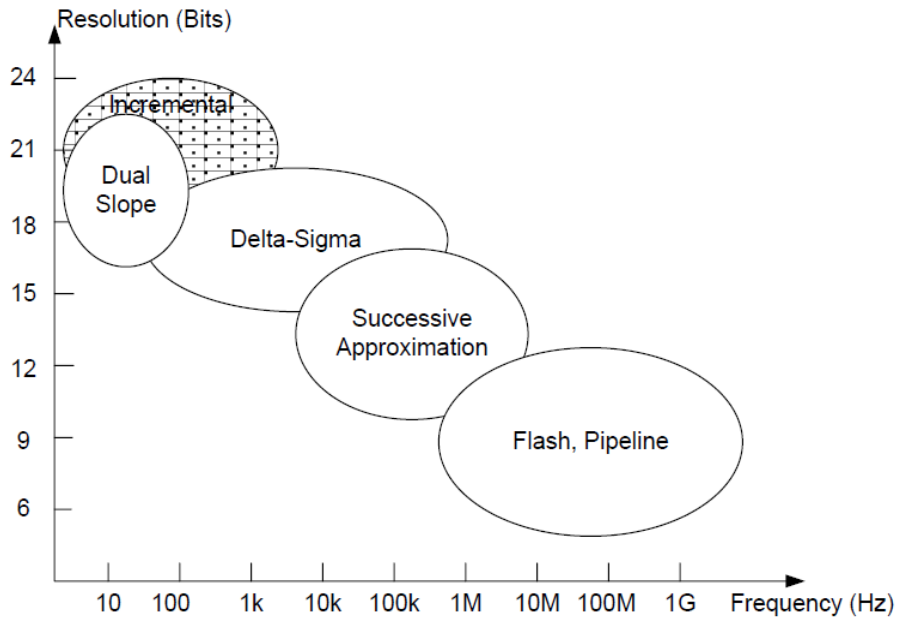


Fig. 1-1. The existing ADC architecture.

For low power application, successive approximation ADC (SAR ADC) is a very good choice. Since there are only capacitors and one comparator in the architecture, the power dissipation is very small. However, due to the conventional SAR algorithm, it takes N+1 clock cycles to resolve one input word. The conversion speed is slow. Therefore, time-interleaved architecture is used to increase the speed of SAR ADC.

The diagram of time-interleaved architecture is illustrated in Fig. 1-2. The time-interleaved architecture increases the speed of the ADC by using a number of identical ADCs working in parallel. A suitable combination of the results makes the operation of the ADCs as a whole equivalent to an ADC whose speed has been increased by a factor equal to the number of parallel ADCs.

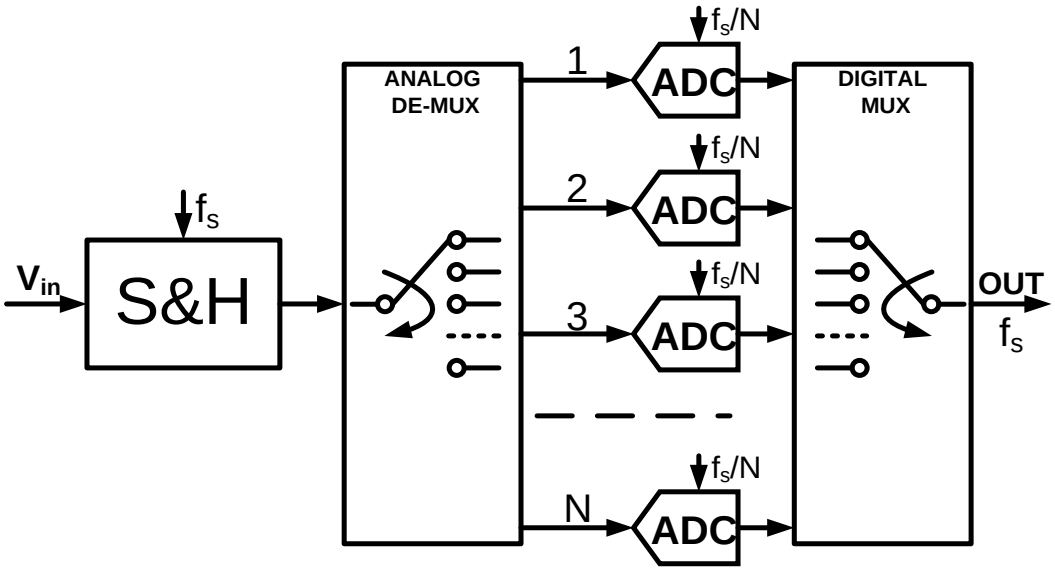


Fig. 1-2. Time-interleaved ADC.

The architecture uses a sample-and-hold circuit to sample the input signal V_{in} at full

speed f_s. Then, an analog demultiplexer (demux) delivers the input signal to the N parallel ADCs whose conversion speed is f_s/N. Finally, a digital multiplexer (mux) sequentially collects the output digital codes from the ADCs one by one to obtain the full speed ADC output codes.

1.3 Current-State-of-the-Art Gigahertz ADCs

To illustrate the performance improvement, a total of 32 papers are surveyed from [1-2]. The survey window is defined as ADCs which have >1GSPS sampling-rate and fabricated in CMOS process.

The comparison is based on the Walden Figure of Merit (FoM) of the ADCs. FoM represents the energy used per conversion step and defined as followed,

$$FoM = \frac{P}{2^{ENOB} \cdot f_S} \tag{1}$$

where P denotes the power consumption, fs is the sampling-rate and ENOB is the effective number of bits which equals to

$$ENOB = (SNDR - 1.76)/6.02 \tag{2}$$

in which SNDR is the signal-to-noise and distortion ratio.

Two-step-subranging, folding and interpolating ADCs are included in the category of flash ADCs. These three architectures are treated as modifications for the flash ADCs to improve its performance. Fig. 1-3 demonstrates the FoM trend in the past ten years, while Fig 1-4 illustrates the FoM versus the sampling frequency. Decrease o fFoM is due to the scaling-down sub-micro technology. For example, the lowest FoM

presented by the 8-bit 1.2GSample/s time-interleaved SAR [1-3] shows the benefit from 32nm CMOS process. Flash and pipeline are still the dominant architectures to achieve gigahertz sampling-rate with good FoM. With the help of time-interleaving technology, SAR ADCs become an important candidate for gigahertz-sampling-rate applications. The fastest ADC is a 40GHz 6bit time-interleaved SAR published on ISSCC 2010 [1-4]. All these time-interleaved SAR ADCs emerged in the past five years. Moreover, the power consumption of the time-interleaved SAR ADC becomes smaller and smaller.

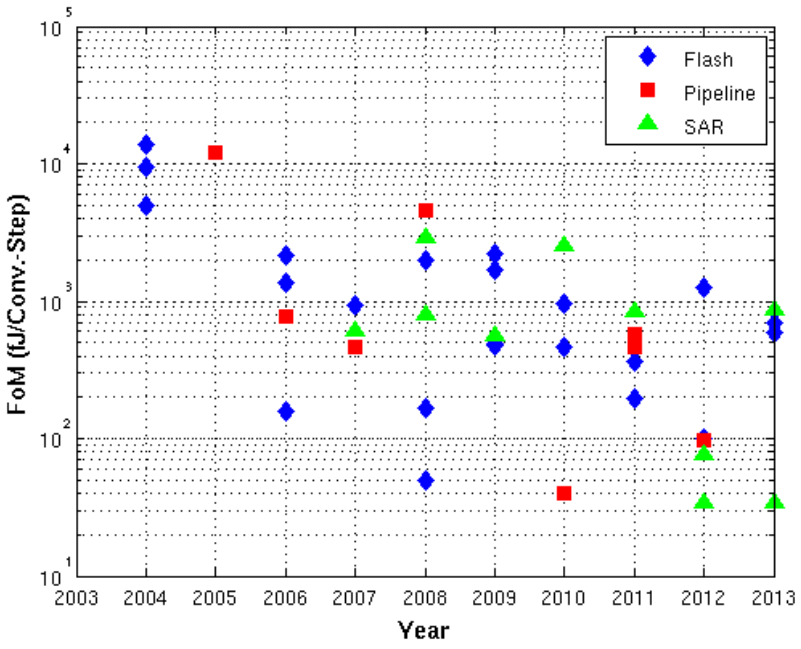


Fig. 1-3. FoM trend of Nyquist ADCs during past 10 years.

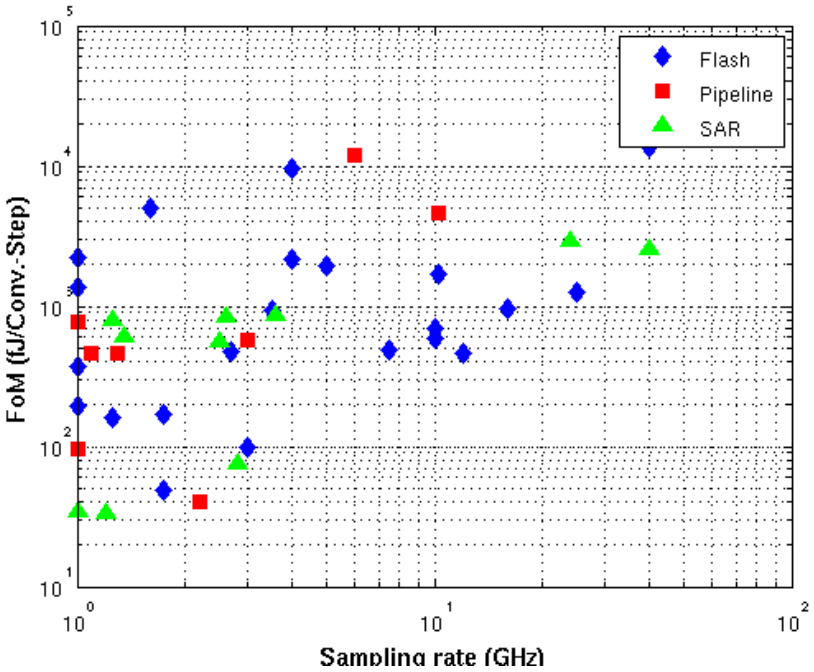


Fig. 1-4 . FoM versus sampling rate.

1.4 Design Techniques of High-Speed Low-Power SAR ADCs

A SAR ADC only requires one single comparator and DAC. Also, since SAR resolves one bit, instead of one level per comparison, it is possible for the SAR to be implemented in a small area at low power. This characteristic also renders the architecture highly scalable and easier to calibrate.

1.4.1 Synchronous and Asynchronous Clocking

A synchronous approach relies on a clock to divide the conversion phase into equally timed slots as the conversion proceeds from MSB to LSB. However, the time for bit determination of the comparator is signal dependent. The design of the comparator is chosen to accommodate the worst case, in which the comparator resolve

time for a small residue voltage. For SAR algorithm, there are only two steps when the input signal is within 1LSB difference from the reference voltage. Therefore, for most steps, the comparator is over-designed. In order to lower the power dissipation of the comparator in synchronous SAR ADC, dynamic biasing of the comparator is used to lower the power consumed by the comparator. When the voltage difference of the inputs is large, low bias current is sufficient. In [1-5], dynamic biasing is achieved by sensing the common node of the differential input pair of the comparator and lowers the bias current by increasing the V_T of M_{bias}, as illustrated in Fig. 1-5.

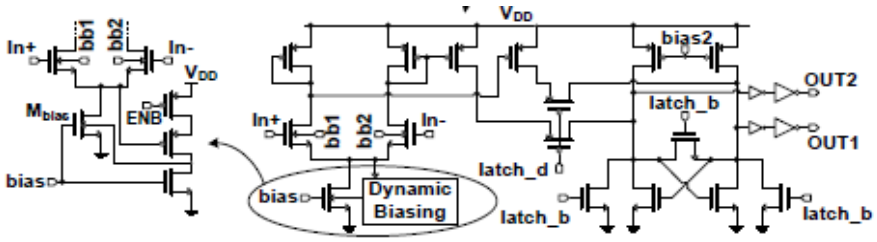


Fig. 1-5. Schematic of the comparator dynamic biasing circuit.

The semi-synchronous technique is also a good choice [1-6]. In SAR algorithm, there are hard decision and easy decision. Hard decision occurs when the sampled input signal is very closed to the reference voltage. In hard decision, the settling time allocated to the DAC should be long enough to meet the required accuracy. Also, the comparator needs long time to resolve the bit. However, in easy decision, the settling time can be short because the settling accuracy is not so important due to the sampled input voltage is far away from the reference voltage. The output bit can also be determined very fast by the comparator. The semi-synchronous technique is based on

the observation that a hard decision is followed by a number of easy decisions and an easy decision may be followed by a hard decision. Therefore, the semi-synchronous technique uses a ready signal and a DAC settling clock to dynamic allocate the time for comparator resolution and DAC settling.

Another way to take advantages of different conversion time for different input signal is the asynchronous technique, which generates the timing in a dynamic way. The SAR asynchronous conversion efficiently utilizes the faster comparison cycle for large comparator inputs [1-7]-[1-9]. A ready signal will be generated to trigger next bit conversion as soon as the comparator finishes resolving the current bit.

Metastability of the comparator, which makes the comparator spend an unbounded time on resolving an arbitrarily small input, is one of the most important limits for asynchronous architecture. In order to avoid metastability, the regeneration speed and resolution of the comparator should be increased, which costs a significant large power burned on the comparator. Since only one of the residual voltages will fall within ½ V_{LSB}, an off-line digital calibration algorithm is proposed in [1-7] to fill in the missing end bits after the last output bit when metastability happened.

The delay from the comparator to the output of the SAR logic is critical. The circuit in [1-3] utilizes an alternate comparator to eliminate the comparator reset time from the critical path. The scheme in [1-9] uses six comparators instead of one to directly feed the output bit to the CDAC input to eliminate the logic delay.

1.4.2 C-2C Capacitor Ladder

In [1-5], [1-7], C-2C capacitor ladder network is used as the capacitor array in the SAR ADCs. Capacitive ladder has effectively low input capacitance which enables the high input bandwidth applications. For NBIT-bit C-2C SAR, the total input capacitance is three times the unit capacitance (Cu), independent of the resolution compared to 2^{NBIT}*Cu in the traditional SAR.

In a C-2C capacitor ladder, the actual ratio of the capacitor network is highly sensitive to the capacitance ratios and the parasitic capacitors associated with the interconnect circuitry, thus it requires extra effort on the layout and calibration [1-5], [1-7]-[1-8]. In [1-7] and [1-8], redundancy-bit is used to alleviate the impact from the parasitic capacitors at the floating node in the capacitor ladder. In [1-5], an adjustable capacitive array, which is called C-bank, is used to trim the capacitance ratios.

1.4.3 Time-Interleaved Techniques

Time-interleaved technology is an efficient way to realize high speed ADC while maintaining relatively low speed operation frequency in the sub-ADCs, which reduces the power dissipation. However, in time-interleaved architecture, it is imperative to minimize the timing skew resulting from the mismatches among sampling intervals, which is mainly due to the mismatch among clock drivers and clock routes.

In [1-10], a front-end sampling switch, which is closed only half of the period of the master clock, is employed, a disadvantage of which is the decrease in bandwidth.

In [1-11], a master clock is used to synchronize the different sampling instants and matched lines to distribute clock and input signals to the channel.

Digital calibration for eliminating timing skew can also be employed. In [1-12], an on-chip timing-skew calibration processor (TSCP) is used to count the zero-crossing occurrences in every sampling interval when a testing signal is applied, to detect the timing skews, and then automatically adjusts the delays of the clock drivers to ensure uniform sampling intervals.

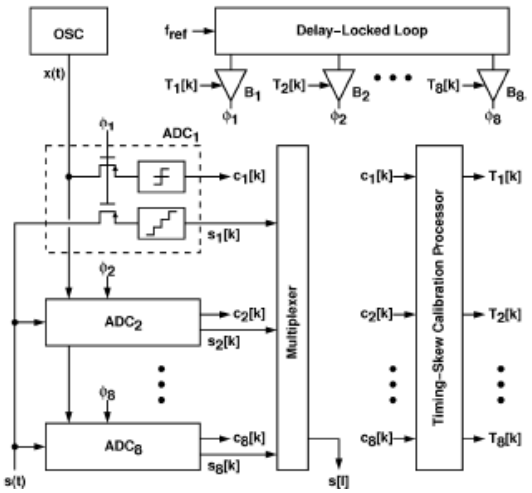


Fig. 1-6. ADC block diagram using TSCP to eliminate timing skew.

In [1-13], a correlation-based algorithm is used to minimize the timing skew by adding an auxiliary comparator with a clock whose edges periodically coincide with the ideal sampling instances for the sub-ADC clocks. Digitally adjustable delay cells are iteratively tuned until the correlation of the auxiliary comparator output with each channel is maximized, forcing the sampling instances to approach their ideal locations.

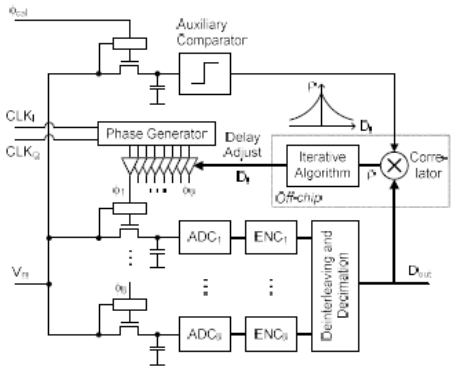


Fig. 1-7. ADC architecture using correlation-based algorithm to minimize the timing skew.

1.5 Structure of the Dissertation

Chapter 2 will propose a 1GSample/s 6-bit pipeline SAR ADC with capacitive DACs. The details of the circuit implementation will also be presented. Measurement results and the analysis of the measurement results will be given.

Chapter 3 will propose another 1GSample/s 6-bit pipeline SAR ADC with resistive DACs, which is a modification of the previous one with capacitive DACs. The details of the circuit implementation and the simulation results will be presented.

Chapter 4 will propose a low power multi-step capacitive-splitting SAR ADC and Chapter 5 will summarizes the whole dissertation.

2 The Design of a Pipeline SAR ADC with Capacitive DACs

2.1 Architecture

The architecture of a pipeline SAR ADC was first proposed in 1985[2-1]. The diagram of the architecture is shown in Fig. 2-1.

The circuit works as follows. In the first phase of first clock cycle Φ_1, the sampling capacitor C_1 samples the input signal V_{in1} and then holds it for the next n-bit clock cycles for the n-bit conversion. In the second phase of Φ_1, C_1 delivers the sampled signal V_{in1} to the first comparator (the leftmost one) and generates the MSB b_1. According to the SAR algorithm, V_1 will always be at the middle of V_{refp}-V_{refn}. In the next clock cycle Φ_2, C_1 deliver V_{in1} to the second comparator and generate the next bit b_2 by comparing it with the reference voltage V_2. The voltage V_2 depends on the MSB b_1. If b_1 is 1, then V_2 will be ¾(V_{refp}-V_{refn}). If b_1 is 0, V_2 will be ¼(V_{refp}-V_{refn}). Meanwhile, C_2 starts to sample the input signal. The sampled signal V_{in2}, which will be held on C_2 for the next n clock cycle, is delivered to the first comparator and generates its own MSB, b_1. In the third clock cycle Φ_3, V_{in1} is passed to the third comparator and get the third bit of V_{in1}, which is b_3; V_{in2} is delivered to the second comparator and generate the second bit of V_{in2}, which is b_2. In Φ_3, C_3 sample the input signal and get V_{in3} on it for the next n clock cycle and also pass the V_{in3} to the first comparator to get MSB b_1. The process continues until all bits are generated in the pipeline fashion.

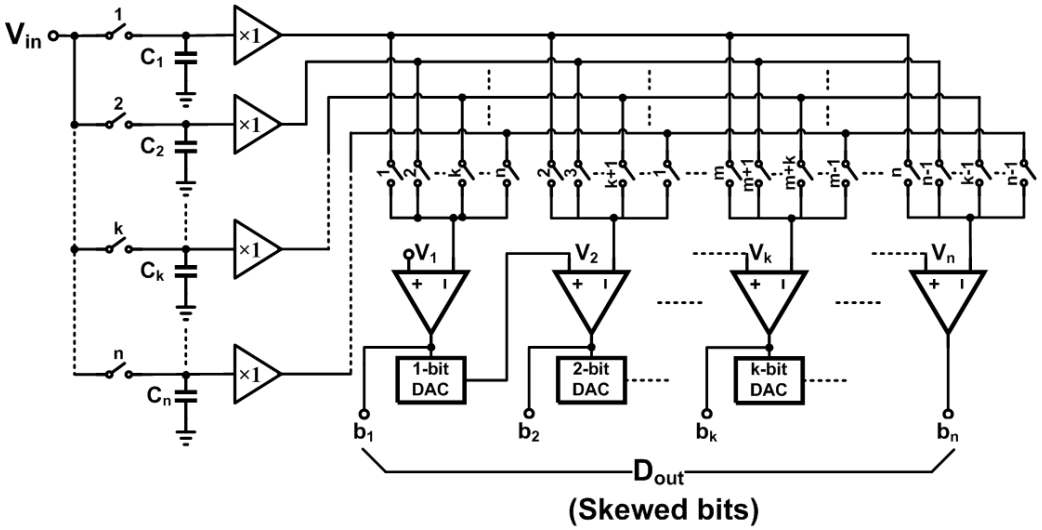


Fig. 2-1. The original pipelined SAR.

The advantages of this architecture are as followed:

High speed: Since this SAR ADC is working in pipeline fashion, the throughput is 1/N after first N clock cycle latency. Thus SAR ADC is N times faster than the single-channel SAR ADC. Moreover, since the output of bit of each stage directly feeds to the next stage, the SAR logic delay is eliminated and the circuit can run at higher speed.

Small area: Compared with the conventional time-interleaved SAR ADC, the area of the capacitive DAC is smaller in the pipeline SAR ADC. The N capacitive DACs that are used to generate the reference voltage are not same. The DAC used to generate the reference voltage for b_2 determination is 1-bit DAC, which means only two C and one 2C are needed, where C is the unit capacitance. The DAC for b_3 determination is 2-bit DAC. Hence it has two C, one 2C and one 4C. The DACs

become bigger and bigger from MSBs determination to the LSBs determination. The DAC for the LSB determination is the biggest one and its total capacitance is $2^N \times C$, where N is the resolution of the pipeline SAR ADC. Therefore, the total capacitance of the capacitive DAC in pipeline SAR ADC is $2\times (2^N-2)\times C$, rather than $N\times 2^N \times C$ for N-channel N-bit conventional time-interleaved SAR ADC.

Low power: Fig. 2-2 shows the switching power of the capacitive array in the pipeline SAR ADC. Compared with the conventional time-interleaved SAR ADC, the switching power on the DACs in pipeline SAR ADC is 50% less. Moreover, since the power consumed by the clock buffers for the switches in the DACs is huge, the pipeline SAR ADC can save this portion of the power too because the total capacitance of the DACs is much smaller and the total size of the switches is proportional to the total capacitance.

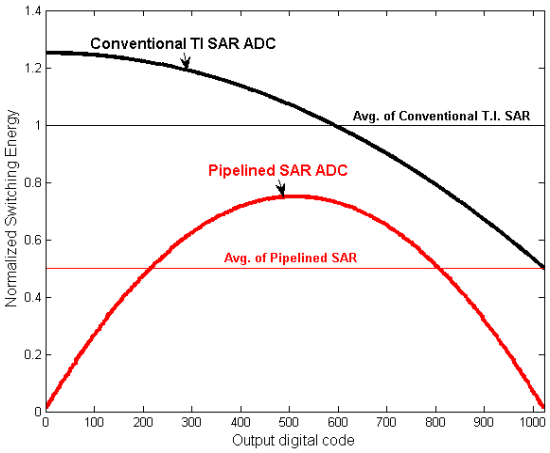


Fig. 2-2. Normalized energy versus output code required for the switching of the capacitor array.

For high-speed applications, the unit-gain buffer will be very power hungry. In order to save power further, the unit-gain buffers are eliminated. However, since now

there is no isolation between the sampling capacitors and the comparators, the parasitic capacitors at the input node of the comparators will have great impact on the performance of the ADC by sharing the charge on the sampling capacitors.

If the voltage on the sampling capacitor is V_{in}, then the actual voltage V_{in}' seen by the comparator is not V_{in}, but

$$V_{in}^{'} = \frac{C_s}{C_s + C_p} V_{in} \tag{2-1}$$

where C_s is the sampling capacitance and C_p is the parasitic capacitance at the input of the comparator.

Moreover, the actual reference voltage V_{ref}' used by the comparator is not the theoretical value V_{ref}, but

$$V_{ref}^{'} = \frac{2^N \cdot C_u}{2^N \cdot C_u + C_p} V_{ref} \tag{2-2}$$

where N is the resolution of the DAC and C_u is the unit capacitance of the DAC.

Since the sampling capacitor will pass its voltage to all comparators, the sampled voltage will attenuated by the parasitic capacitance in an accumulated methods, which means at the k^{th} comparison, the actual sampled voltage $V_{in,k}$' seen by the k^{th} comparator is

$$V_{in,k}^{'} = \left(\frac{C_s}{C_s + C_p} \right)^k V_{in} \tag{2-3}$$

However, the actual reference voltage $V_{ref,k}$' is still the value shown in equation (2-

2).

This accumulated attenuation will cause two side effects. The first one is that the sampled input voltage becomes very small, which requires the last comparator to be very accurate. The second effect is that the sampled input voltage and the reference voltage have different attenuation ratio, which will cause nonlinearity. Fig. 2-3 shows the 8192-length FFT spectrum of a 6-bit pipeline SAR ADC in which the sampling capacitance is 20 fF and the parasitic capacitance at the input of the comparator is 2 fF. Other parts in the circuit are ideal.

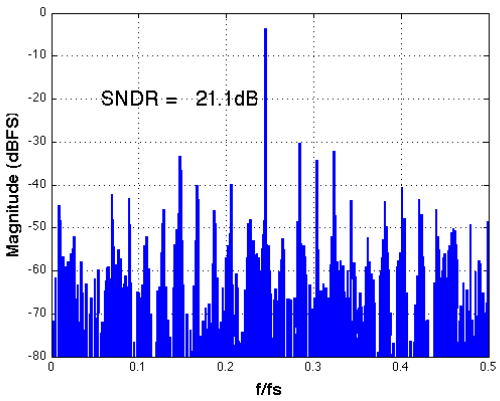


Fig. 2-3. The 8192-length FFT of a 6-bit pipeline SAR ADC with 20 fF sampling capacitor and 2 fF parasitic capacitance at the input of a comparator.

In order to reduce the influence from the parasitic capacitors, increasing the capacitance will be helpful since the attenuation from the parasitic capacitors will be negligible. Fig. 2-4 shows the FFT spectrum of a 6-bit pipeline SAR ADC with 200 fF sampling capacitor and the parasitic capacitance at the input of the comparator is still 2 fF.

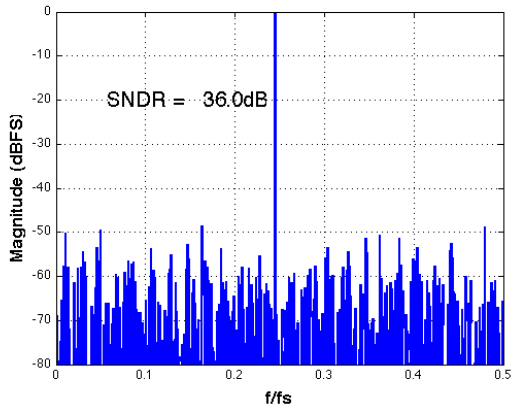


Fig. 2-4. The 8192-length FFT of a 6-bit pipeline SAR ADC with 200 fF sampling capacitor and 2 fF parasitic capacitance at the input of a comparator.

In order to reduce the total sampling capacitance in the pipeline SAR ADC to reduce the area, we can split one sampling cap into several smaller ones. Fig. 5 shows the 8192-length FFT of a 6-bit pipeline SAR ADC with one 100fF sampling capacitor and one 40fF sampling capacitor for one sampling branch. The 100fF sampling capacitor is used for first four MSBs determination and the 40fF sampling capacitor is used for last two LSBs determination.

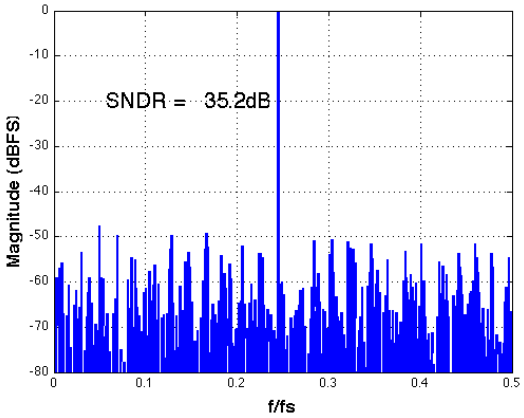


Fig. 2-5. The 8192-length FFT of a 6-bit pipeline SAR ADC with one 100 fF sampling capacitor and one 40 fF sampling capacitor. The parasitic capacitance at the input of a comparator is 2 fF.

Since the MSB is important since any mismatch of the gain ratio between the sampled input signal and the reference voltage will degrade the performance a lot, the architecture whose simulation result is shown in Fig. 2-5 still needs 100 fF sampling capacitor for MSB stages.

However, from this scheme, we can conclude that splitting the sampling capacitor can help reduce the nonlinearity and also reduce the total area occupied by the sampling capacitors. By splitting the sampling capacitor into more groups of capacitors, the performance of the circuit can be better since the accumulated effect between the stages will be smaller. Moreover, the sampling capacitance can be reduced further. Fig. 2-6 shows the 8192-length FFT spectrum of a 6-bit pipeline SAR ADC with six identical 20 fF sampling capacitors in one channel while the input parasitic capacitance of the comparator is 2 fF.

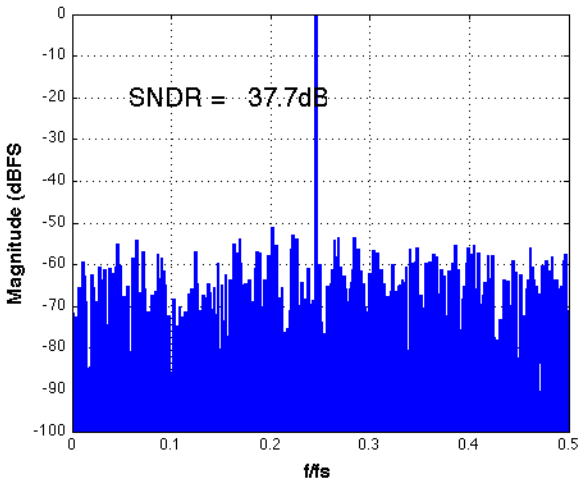


Fig. 2-6. The 8192-length FFT of a 6-bit pipeline SAR ADC with six identical 20 fF sampling capacitor and the parasitic capacitance at the input of a comparator is 2 fF.

The sampling capacitors are now split into 6 smaller equal-value capacitors. Although the number of the sampling cap increased from 6 to 36, the total capacitance of the sampling capacitor array can be significantly decreased to achieve good performance because the influence of the parasitic of the input of the comparator is negligible. The parasitic capacitors will only introduce a gain error, which has no influence on the linearity. The new diagram and timing of the circuit are illustrated in Fig. 2-7.

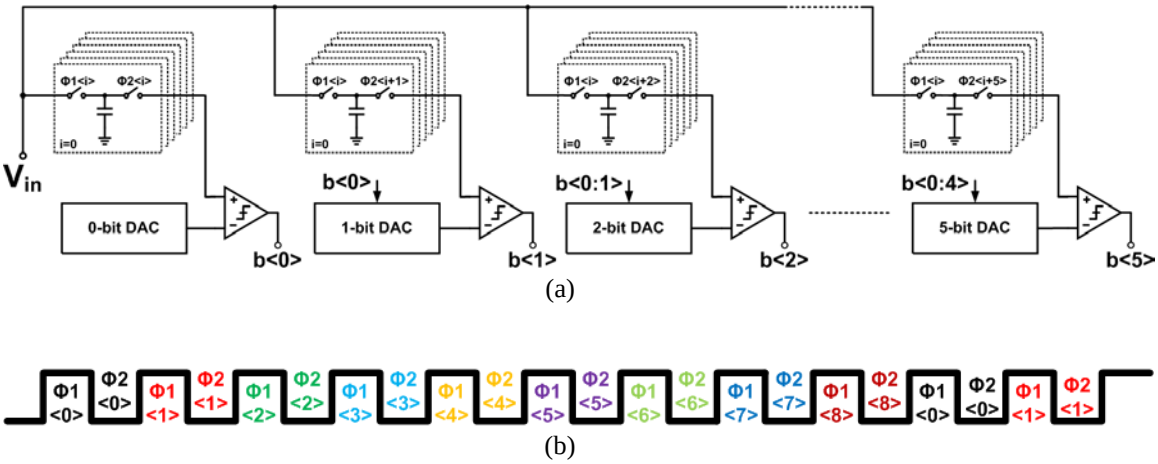
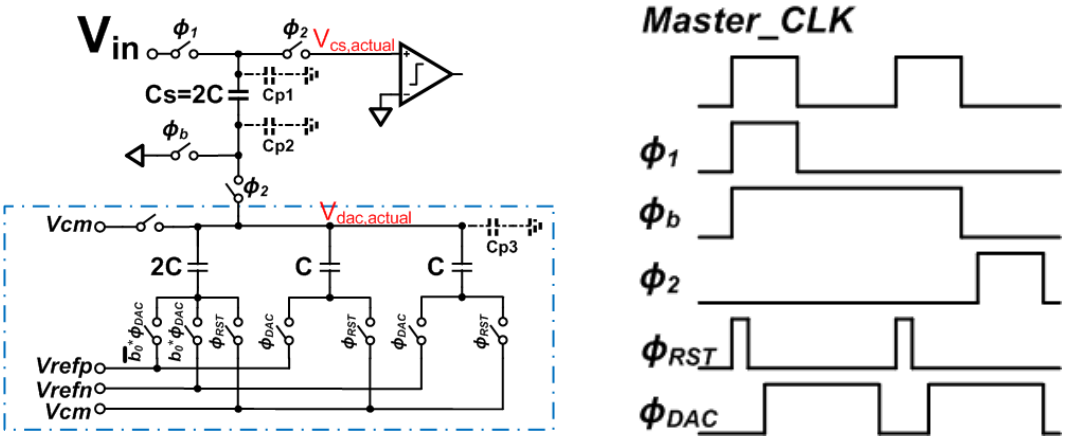


Fig. 2-7. (a) The new diagram of the pipelined SAR ADC; (b) The timing diagram of the circuit.

In addition to the accumulated attenuation from the parasitic capacitors at the input of the comparators, the different attenuation ratio between the sampled signal and the reference signal generated by the DAC is another critical problem. In order to solve this problem, the DAC can be stacked with the sampling capacitor array, as shown in Fig. 2-8.



(a) (b)

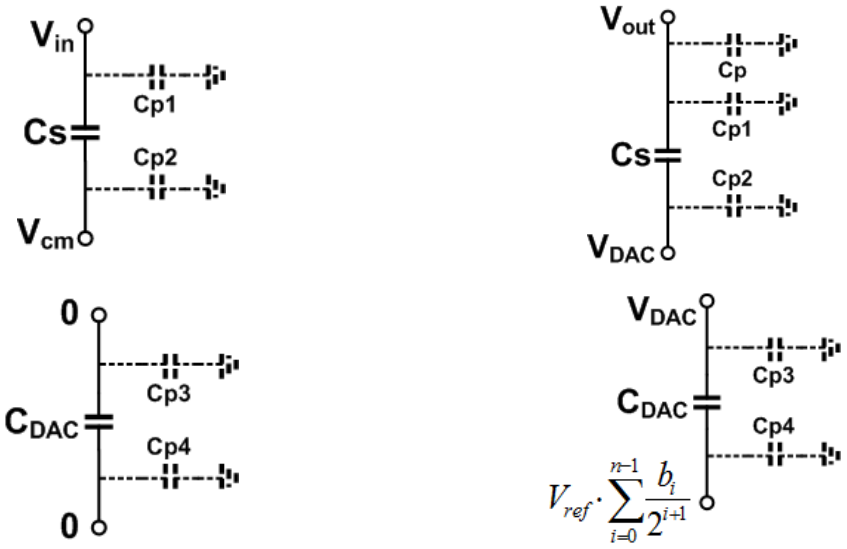
Fig. 2-8. (a) The sampling part is stacked with the DAC; (b) The timing diagram of the controlling signal for the switches in the sampling part

The additional benefit of stacking these two parts is that the DACs do not need to reset to the common-mode voltage anymore. They can be reset to the ground so that the V_{gs} for the reset switches can be increased whose sizes can be reduced dramatically, which results in lower power consumption of the clock buffers for these reset switches.

In the architecture, the output voltage of the sampling capacitor array is $V_{in}+V_{DAC}-V_{cm}$, where V_{in} is the sampled input signal, V_{DAC} is the reference voltage generated on the capacitive DAC and the V_{cm} is the input common-mode voltage. The influence of the attenuation fact due to the input parasitic capacitors is shown next. Theoretically, without considering the parasitic capacitors at the node between the sampling capacitor and the capacitive DAC array, the voltage seen by the comparator is

$$V_{out} = \left(V_{in} + V_{DAC} - V_{cm}\right) \cdot \frac{C_s}{C_s + C_p} \tag{2-4}$$

From equation (2-4), we can see that the sampled input voltage and the reference voltage generated by the DAC time have the same attenuation.



(a) (b)

Fig. 2-9. The voltage states at (a) Φ_1 and (b) Φ_2.

However, as demonstrated in Fig 2-9, if we consider the parasitic capacitors at all nodes, the output voltage seen by the comparator is as follows. Due to the charge conservation,

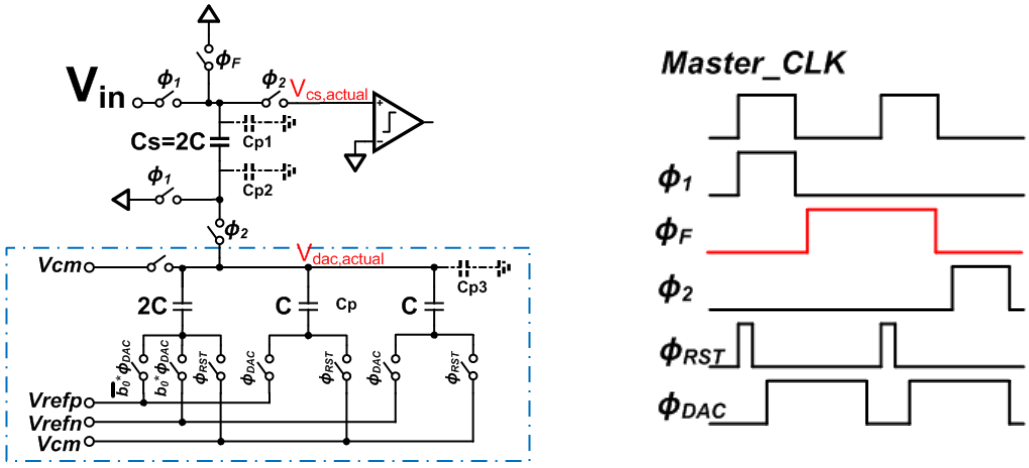
$$\left(V_{in}-V_{cm}\right)\cdot C_S+V_{in}\cdot C_{p1}=\left(V_{out}-V_{DAC}\right)\cdot C_S+V_{out}\cdot C_{p1}+V_{out}\cdot C_p \tag{2-5}$$

$$0=\left(V_{DAC}-V_{ref}\cdot\sum_{i=0}^{n-1}\frac{b_i}{2^{i+1}}\right)\cdot C_{DAC}+V_{DAC}\cdot C_{p3} \tag{2-6}$$

Therefore,

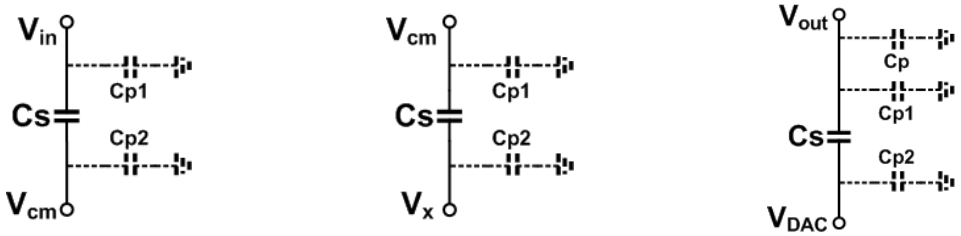
$$V_{out}=V_{in}\cdot\frac{C_S+C_{p1}}{C_S+C_{p1}+C_p}+\left(V_{ref}\cdot\sum_{i=0}^{n-1}\frac{b_i}{2^{i+1}}\right)\cdot\frac{C_{DAC}}{C_{DAC}+C_{p3}}\cdot\frac{C_S}{C_S+C_{p1}+C_p}-V_{cm}\cdot\frac{C_S}{C_S+C_{p1}+C_p} \tag{2-7}$$

From equation (2-7), we can see that V_{in} and V_{ref} have different attenuations, which will introduce nonlinearity in the circuit. In order to solve this problem, we can add an additional switch at the top of the sampling capacitor, as shown in Fig 2-10.



(a) (b)

Fig. 2-10. (a) The sampling part with an additional switch controlled by Φ_F; (b) The timing diagram of the controlling signal for the switches in the sampling part.



(a) (b) (c)

Fig.2-11. The connection status of the sampling capacitor at (a) Φ_1; (b) Φ_F; (c) Φ_2.

(a) (b)

Fig. 2-12. The voltage connection status of the DAC array at (a) Φ_1; (b) Φ_2.

With the additional switch, the sampling capacitor will flip once so that the sampling signal will experience the attenuation ratio twice, which is similar to the reference voltage, which is demonstrated by the following equations.

Based on the rule of charge conservation, the following equations can be derived from Fig. 2-11 and Fig. 2-12.

From Fig 2-11(a) to Fig 2-11(b),

$$V_x = V_{cm} + \frac{C_S}{C_S + C_{p2}}\left(V_{cm} - V_{in}\right) \tag{2-8}$$

From Fig 2-11(b) to Fig 2-11(c),

$$V_{out} = V_{cm} + \left(V_{DAC} - V_x\right) \cdot \frac{C_S}{C_S + C_p + C_{p1}} \tag{2-9}$$

From Fig 2-12(a) to Fig 2-12(b),

$$V_{DAC} = \frac{C_{DAC}}{C_{DAC} + C_{p3}} V_{ref} \sum_{i=0}^{n-1} \frac{b_i}{2^{i+1}} \tag{2-10}$$

By combining equations (2-8) to (2-10), we get

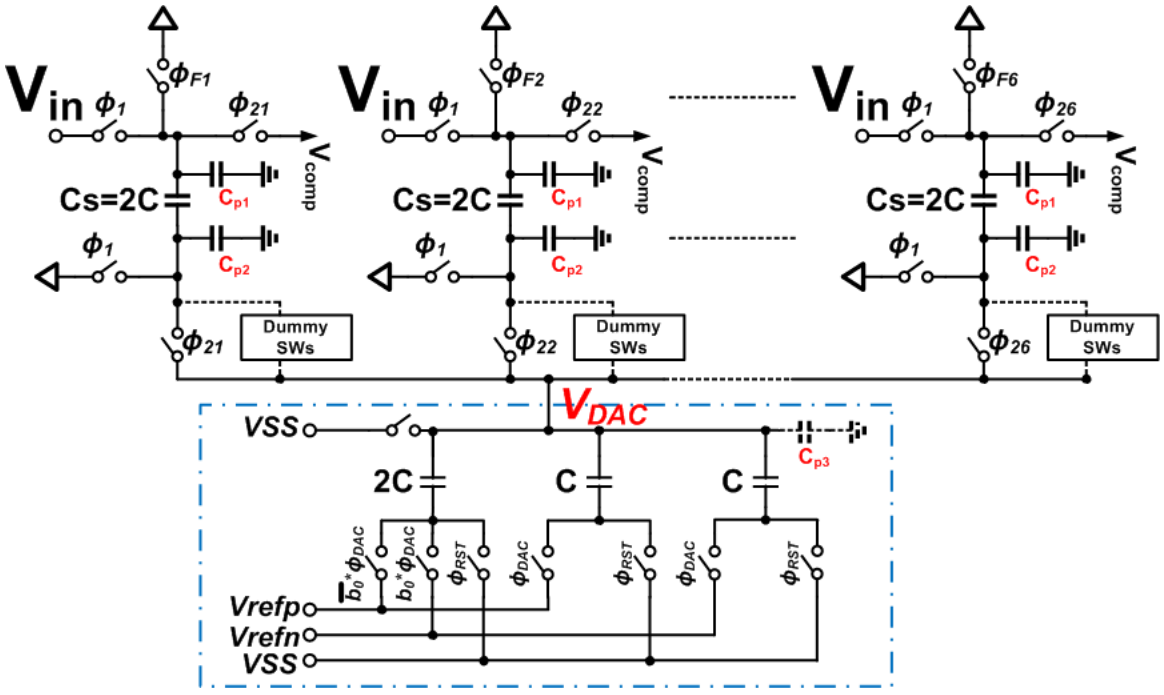
$$V_{out} = V_{cm} \frac{\left(C_p + C_{p1}\right)\left(C_S + C_{p2}\right) - C_S^2}{\left(C_S + C_{p2}\right)\left(C_S + C_p + C_{p1}\right)} + \left(\frac{C_{DAC}}{C_{DAC} + C_{p3}} V_{ref} \sum_{i=0}^{n-1} \frac{b_i}{2^{i+1}} + \frac{C_S}{C_S + C_{p2}} V_{in} \right) \frac{C_S}{C_S + C_p + C_{p1}} \tag{2-11}$$

If

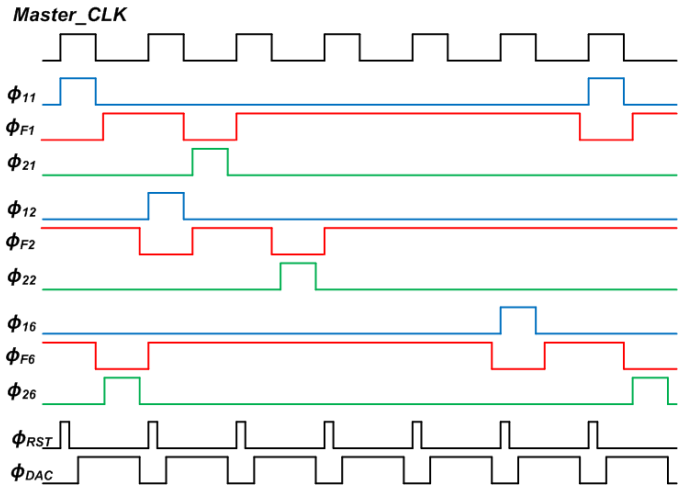
$$\frac{C_{DAC}}{C_{DAC} + C_{p3}} = \frac{C_S}{C_S + C_{p2}} \tag{2-12}$$

then the parasitic capacitors at all node only introduce an gain error, which will not affect the linearity of the whole ADC.

In order to make the attenuation from C_{p3} and C_{p2} be same, some dummy switches are added at the internal node between the capacitive DAC and the sampling capacitors, as shown in Fig 13.



(a)



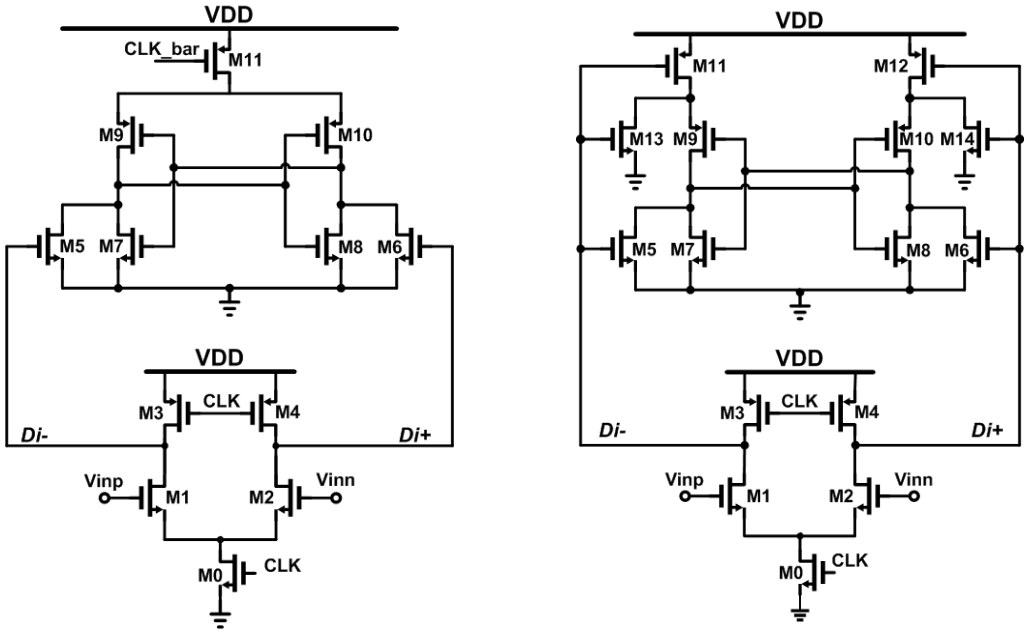
(b)

Fig. 2-13. (a) The diagram of adding dummy switches between the sampling capacitors and the capacitive DAC; (b) the timing for the control signal of all the switches.

2.2 Comparator

Since the pipeline SAR ADC is working at the speed of 1GSample/s, dynamic latched comparator is chosen. There are a few dynamic latched comparators published in the literature [2-2],[2-3],[2-4],[2-5]. As shown in Fig 2-14(a), the dynamic latched comparator with separated input- and output-stage was first introduced by D. Schinkel in [2-2]. For its operation, when CLK is low, the internal nodes between first stage and second stage, Di+ and Di-, are reset to be VDD and the output nodes are reset to be ground. When CLK is high, the parasitic capacitors at internal nodes Di+ and Di- are discharged to the ground. Since Vinp and Vinn are different, the discharge ratios are different due to different discharge current so that the voltage of Di+ and Di- will be different during the discharging. When the difference of the voltage of Di+ and Di- is large enough for the regenerative latch at the second stage, the two outputs will

become one and zero respectively due to the positive feedback.



(a) (b)

Fig. 2-14. (a) Double-tail dynamic latched comparator; (b) modified version.

Since there are separated input- and output-stages, the comparator can have both high speed and low offset. By choosing smaller size of transistor M0 for differential input pair, a long integration time and a better $gm/I_{D1,2}$ ratio can be obtained to have a larger gain and smaller offset. The larger the size of transistor M11 is, the smaller the latch regeneration time is, which results in faster decision of the comparator. Therefore, this dynamic latched comparator can get fast speed and low input-referred offset voltage less dependent on input common-mode voltage.

However, in this architecture, two non-overlapping clock phase CLK and CLK_bar are needed which makes the clock generator complex. Hence, M. Miyahara [2-3] and B. Verbruggen [2-4] introduced a modified dynamic latched comparator, as shown in

Fig 2-14(b). The beauty of this scheme is that since the tail current transistor in second stage is driven by Di+ and Di- nodes instead of CLK_bar, only one clock phase is needed and clock loading is reduced. Moreover, the input-referred offset will be further reduced since the mismatch at the second stage will be divided by a gain not only from input transistors M5/M6, but from M11/M12 as well at the second stage.

However, the reduced offset voltage is traded off with the increased delay since the gate voltages, Di+ and Di-, of M11 and M12 becomes smaller and smaller during the regeneration phase and the tail current of the second stage becomes smaller and smaller.

The dynamic latched comparator used in this pipeline SAR ADC is shown in Fig. 2-15 [2-5].

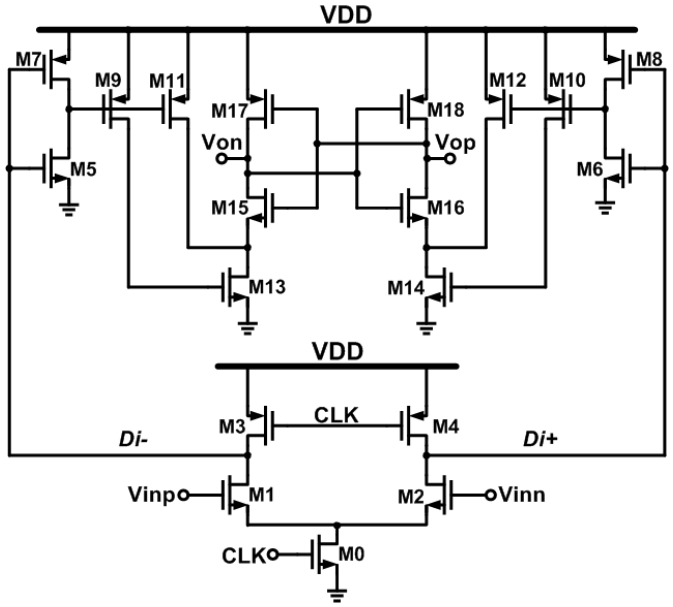


Fig. 2-15. The dynamic latched comparator used in the pipeline SAR ADC.

The basic architecture is from the ones in Fig. 2-14 so that it keeps the beauty of

these two architectures, which are low input-referred offset and high regenerative speed in addition to the advantages of less kickback noise, reduced clock loading, simple clock phase needed over a wide common-mode and supply voltage range.

2.3 Layout

The layout of the sampling parts is critical to the performance of the whole circuit. The diagram of the sampling part is shown in Fig 2-16.

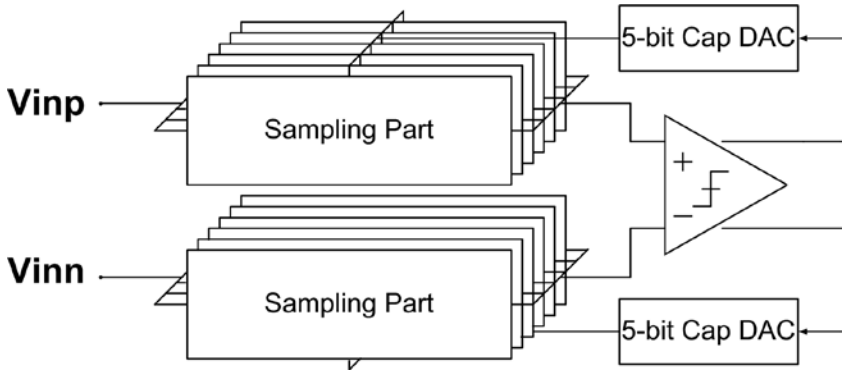
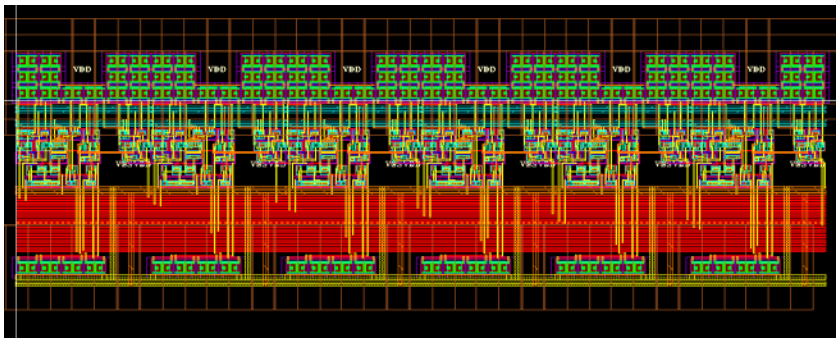
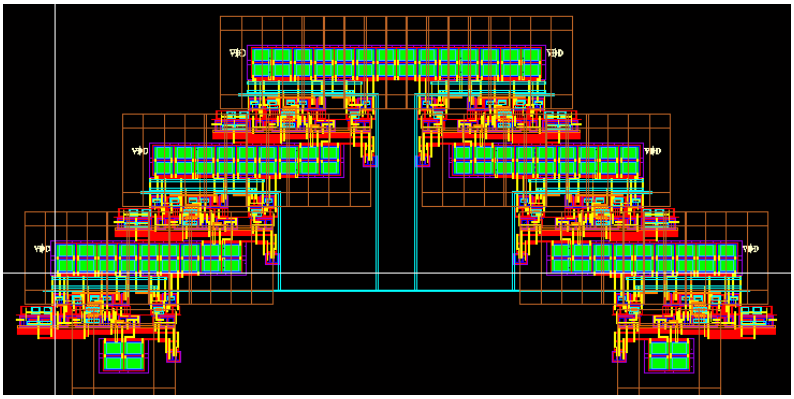


Fig. 2-16. The diagram of the fifth channel.

The sampling part is composed with six identical unit parts. The layout of the sampling part is shown in Fig 2-17.



(a)



(b)

Fig. 2-17. Two layout styles of the sampling part. (a) Serial alignment; (b) folded-stair pattern.

In Fig. 2-17(a), the six identical sampling parts are aligned in serial, which is very compact. However, since the output of the whole sampling part is at the most right end, the distances between the output of the most-left sampling part and the most-right one are significantly different, which introduces different parasitic capacitors resulting in different gain errors due to the charge sharing between the sampling capacitor and the parasitic capacitor in different channels. Like in conventional time-interleaved architecture, the gain mismatch in channels will degrade the performance of the circuit.

In order to improve the performance, the layout of the sampling part is modified as shown in Fig. 2-17(b). The output of the whole sampling part is now in the middle so that the distances from the output of a single sampling unit to the outputs of the whole sampling parts are almost same, which will reduce the gain mismatch from the parasitic capacitors and improve the SNDR dramatically. The comparison between these two layout patterns is shown in Fig. 2-18. The drawback of the folded-stair layout pattern is that the area of the sampling part will increase by 50%.

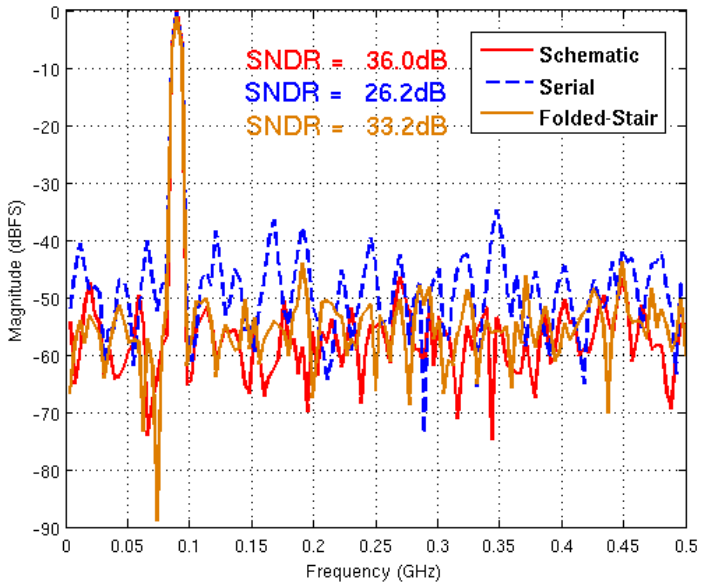


Fig. 2-18. Post-layout simulation results for the serial and folded-stair pattern of the sampling part.

Therefore, the sampling part is drawn in folded-stair pattern. The layout of one channel is shown in Fig. 2-19.

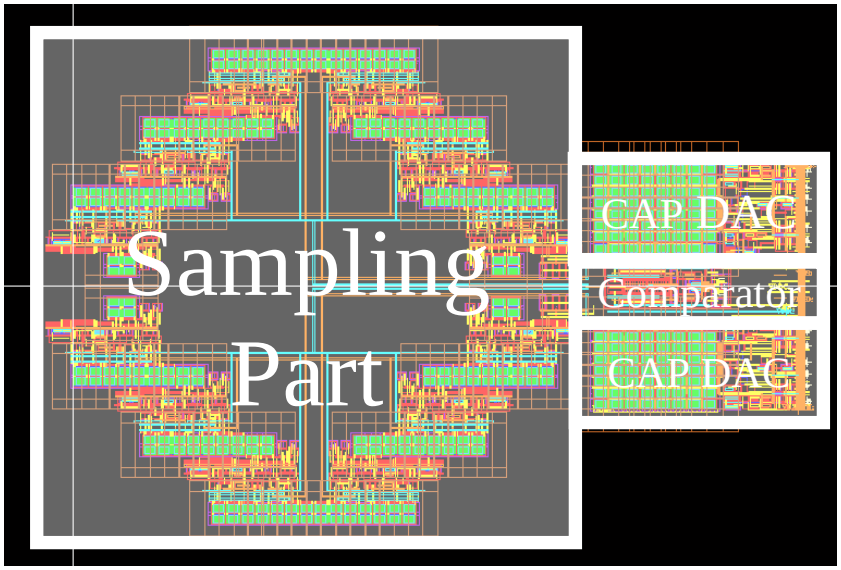


Fig. 2-19. The layout of one channel.

The layout of the whole chip is shown in Fig. 2-20.

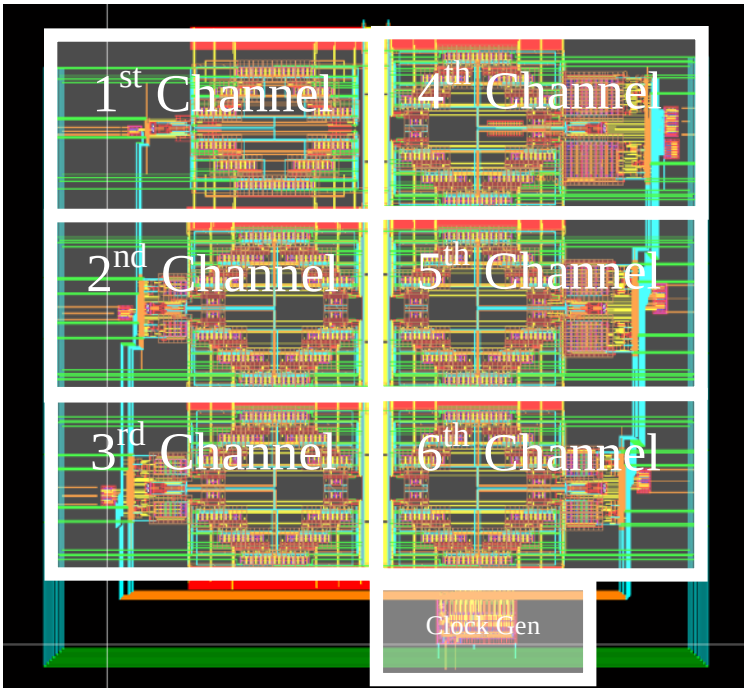


Fig. 2-20. The layout of the whole chip.

2.4 Test Results

The chip is fabricated in Global Foundry 40nm process. The area of the core circuit, which is shown in Fig 2-21, is 400um*400um. The die is carried in QFN-16 package. The test board is shown in Fig. 2-22.

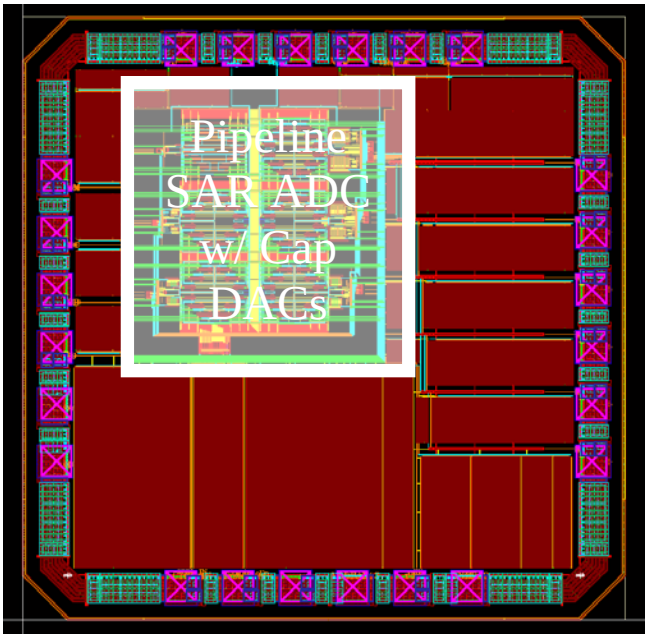


Fig. 2-21. Die photo of the pipeline SAR ADC with capacitive DACs

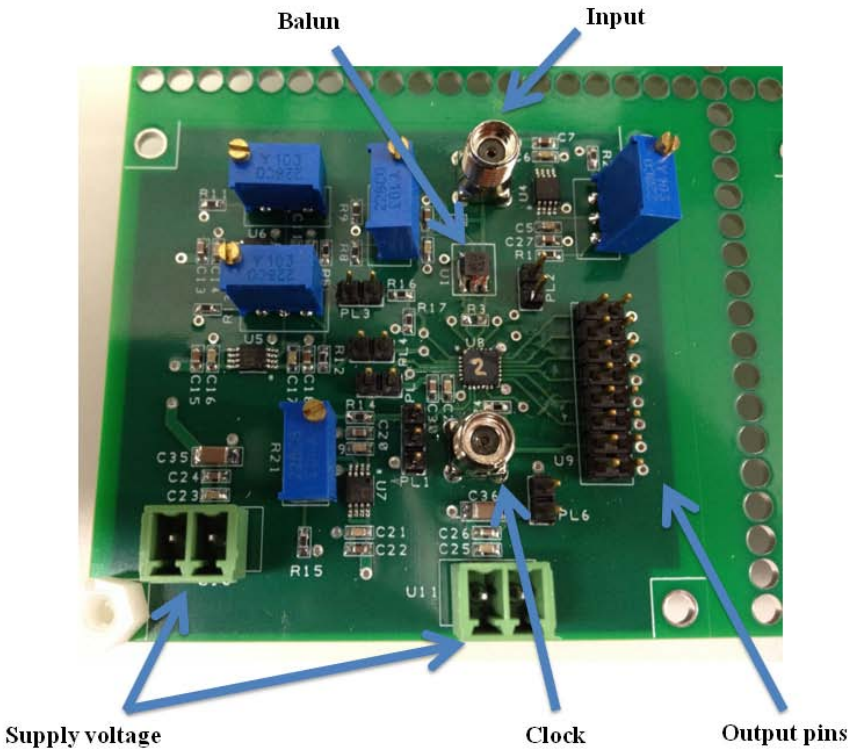
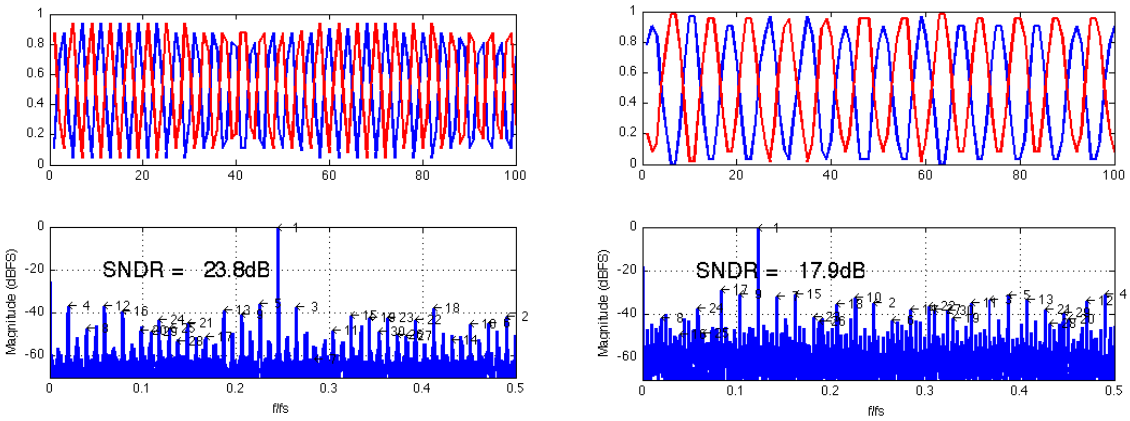


Fig. 2-22. The test board of the pipeline SAR ADC with capacitive DACs.

When the sampling clock for my chip in the testing is set to be 200MHz and 400MHz, the results are shown in Fig 2-23. In the upper part, the two curves are the transient waveform of the positive and negative output codes with binary weights. In the 8192-length-FFT plots, the small numbers with arrows are shown the order and location of the harmonic bins.



(a) (b)

Fig. 2-23. Output spectrum when clock is (a) 200MHz and (b) 400MHz in test.

2.5 Analysis

In the FFT plot, we can see that 1) lots of harmonics have shown up; 2) The dc bin is high, more than -30dB; 3) The SNDR decreases a lot when the clock frequency is doubled.

Some simulations in MATLAB are done to duplicate some non-ideal effects in the pipeline SAR ADC. The results are nearly coincident with the testing results, which are shown below in Fig 2-24.

In MATLAB,

1) The peak-to-peak clock jitter is set to be 10ps and generate uniform distributed jitter on the control signals.

2) Since in the layout the sampling capacitors in the positive side and negative side are separated far away, mismatch is added to all sampling capacitors. The sampling

capacitance is normal distributed. 1-sigma is 10% of the nominal value.

3) The capacitors in the cap DAC are close to each other and laid out in common-centroid pattern, the normal distributed mismatch is added to these caps whose 1-sigma is 5% around the nominal value.

4) The input transistors of my comparators are huge in order to make the input referred offset of the comparator is small. I found that the extracted input capacitance is 15fF, nearly same as my sampling capacitance which is 20fF. I set a normal distributed offset with σ=10mV and a normal distributed varied input parasitic caps with σ=10%.

The MATLAB simulation result is shown in Fig 2-24. The sampling clock is 200MHz. The FFT is very much like the corresponding test result.

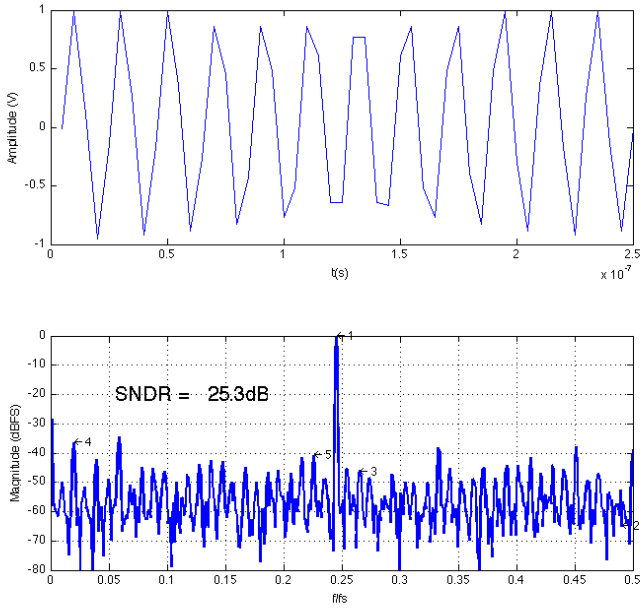


Fig. 2-24. The imitated simulation result in MATLAB.

Monte Carlo simulation is also done when input parasitic capacitance is 20fF and 5fF and keep the σ value same as 10%. The smaller the parasitic capacitance is, the better the performance is, which make sense since if the parasitic capacitance is small enough compared to the sampling capacitance, the non-ideality of the parasitic capacitor is negligible.

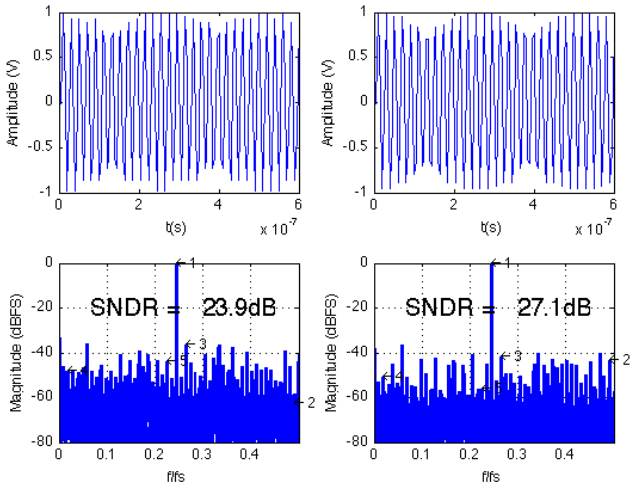
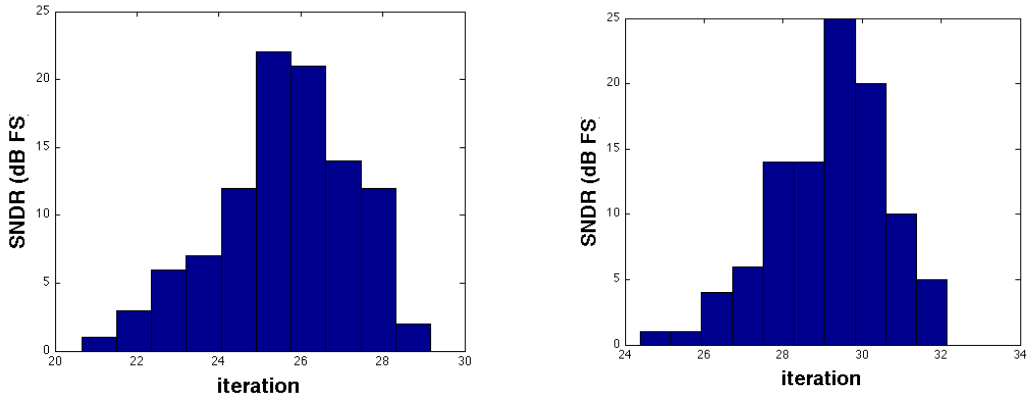


Fig. 2-25. Single run as input parasitic capacitance is 20fF (left) and 5fF (right).



(a) (b)

Fig. 2-26. Imitated monte Carlo simulation results at 200MHz clock when (a) parasitic capacitance is 20fF and (b) parasitic capacitance is 5fF.

From the MATLAB simulation, it is concluded that one cause of the huge dc tone and the rise of noise floor is the variation of the input parasitic capacitance of the comparator because they introduce huge imbalance between the positive and negative sides. The reason why so large input transistors is used in the comparator is to reduce the input referred offset. However, if the size of the input transistor is huge, then the parasitic capacitance at the input node will be huge. The large input parasitic capacitance will reduce the input range of the comparator, which inevitably increases the offset requirement of the comparator for the same error tolerance.

2.6 Conclusions

The chart of power breakdown of the pipeline SAR ADC with capacitive DACs is illustrated in Fig 2-27. The avdd power includes the power dissipated by the comparators and the sampling part switches. The dvdd power includes the power consumed by the clock generator, the local clock buffers. The CDAC power is the switching power of the capacitive DACs. The summary of performance of the chip is shown in Table I. Since this architecture is too sensitive to the parasitic capacitors in the critical path, a new version of the pipeline SAR ADC is developed and will be discussed in the chapter three.

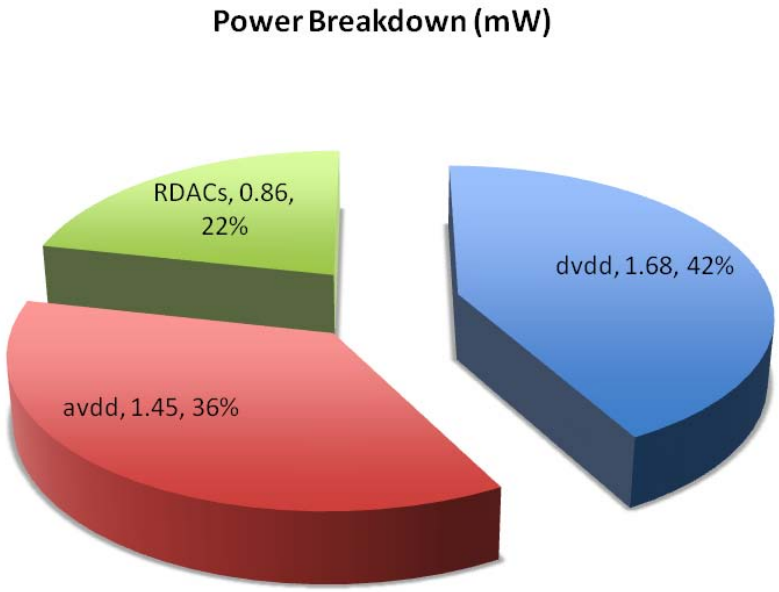


Fig. 2-27. The chart of the power breakdown of the pipeline SAR ADC with capacitive DACs. Total power is 4.17mW

Table 2-1. The summary of the performance of the 6-bit 1GSample/s pipeline SAR ADC with capacitive DACs

	Schematic	Test 1	Test 2
Technology	40nm CMOS process		
Resolution	6-bit		
Supply Voltage	1.1 V		
Input Range	2.2 Vppd		
Clock Frequency	1GHz	200MHz	400MHz
SNDR	35.9 dB	23.8 dB	17.9 dB
Power consumption	4.15m W	-	-
FOM	95 fJ/conv-step	-	-

3 The Design of a Pipeline SAR ADC with Resistive DACs

3.1 Architecture

Since the pipeline SAR ADC is very sensitive to the parasitic capacitors due to the gain error between the input signal and the reference voltage, the resistive DAC is taken into consideration.

Although the resistive ladder will consume some static power while the capacitive DAC just consumes dynamic power, the static power is relatively smaller, due to much of the power consumption of a high speed ADC consumed by the clock buffers and clock generators are seen Fig 2-27 in chapter two. Moreover, thanks to the shrinking of the CMOS technology, the area occupied by the resistive array is significantly reduced. Also, the parasitic capacitances are diminished, so larger resistance can be used and therefore lower static power dissipation since for a given settling time and settling error, the smaller the parasitic capacitance is, the larger the resistance can be (explanation can be found later in this chapter). Recently, some paper [3-1] also shows very promising FOM using resistive DAC to generate reference voltage for SAR ADC. Therefore, resistive DAC can be a good solution for high-speed circuit design.

There are four kinds of resistive DACs taken into consideration. The first one is the resistive string, which is widely used in flash ADCs as the reference voltage generator. However, the number of the resistors increased proportional to 2N, where N is the

number of the bits of the DAC.

The second choice is the R-2R ladder. The scheme is shown in Fig 3-1. The R-2R ladder reduces the number of the resistors and the area occupied by the resistors. However, the power consumption is linearly proportional to the number of bits of the DAC.

The leftmost resistor is the MSB resistor and the rightmost resistor is the LSB resistor. One dummy resistor, whose resistance is also 2R, is needed for the binary search algorithm. During the conversion phase, the MSB resistor is switched to V_{ref}. V_{out} now goes to $V_{ref}/2$. If V_{out} is smaller than V_{in}, the MSB resistor is left connected to V_{ref}. Otherwise, the MSB resistor is reconnected to ground. This process is repeated N times, with a smaller resistor being switched each time, until the conversion is finished.

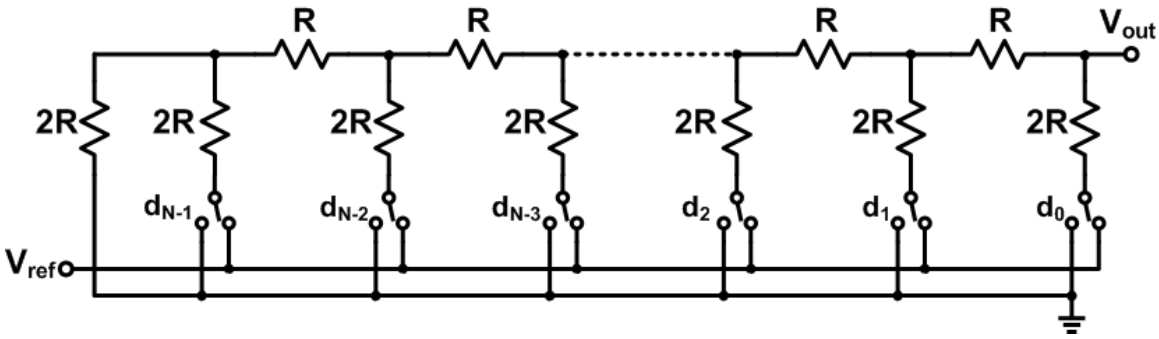


Fig. 3-1. The diagram of the R-2R ladder.

The third choice is binary weighted resistive array, which is shown in Fig 3-2. The smallest resistor, R, is the MSB resistor and the biggest resistor, $2^{N-1}R$, is the LSB resistor. One dummy resistor, whose resistance is also $2^{N-1}R$, is also needed for binary

search algorithm. The switching algorithm of the bottom switches is same as the one of the R-2R ladder.

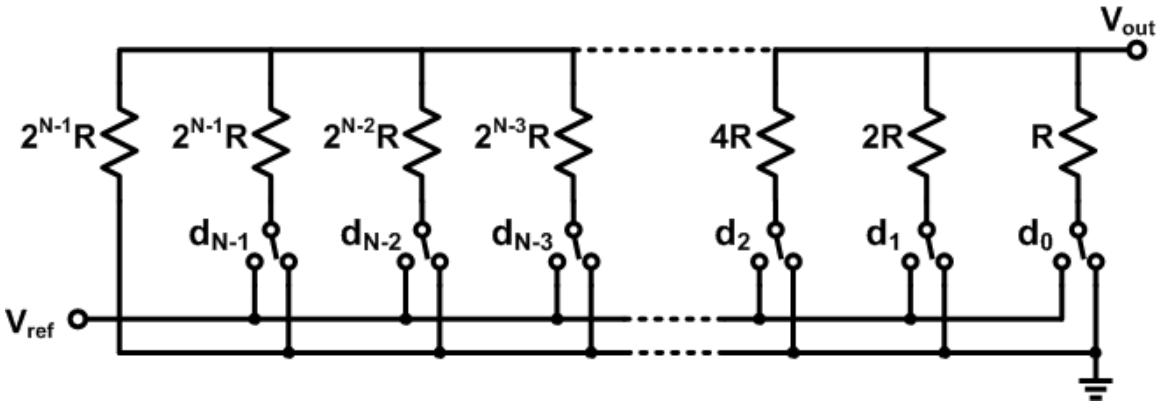


Fig. 3-2. The scheme of the binary-weighted resistive array.

The output voltage of this resistive array is defined as:

$$V_{out} = V_{ref} \cdot \frac{R}{2} \cdot \sum_{k=0}^{N-1} d_k \frac{1}{2^k \cdot R} \tag{3-1}$$

In order to reduce the total resistance of the resistive array, the binary-weighted array with bridge resistor is used, as shown in Fig. 3-3. The binary search algorithm is same as previous two resistive arrays.

By using Thevenin's theorem, the output voltage Vout can be calculated:

$$V_{out} = \frac{R}{2^{m+1}} V_{ref} \cdot \sum_{k=m}^{N-1} d_k \frac{1}{2^{k-m} \cdot R} + \frac{R}{2} V_{ref} \cdot \sum_{k=0}^{m-1} d_k \frac{1}{2^k \cdot R} \tag{3-2}$$

$$V_{out} = \frac{R}{2} V_{ref} \cdot \sum_{k=0}^{N-1} d_k \frac{1}{2^k \cdot R} \tag{3-3}$$

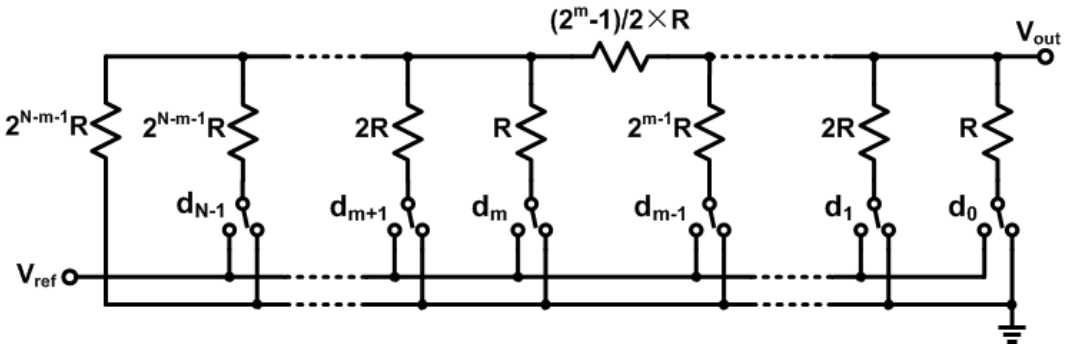


Fig. 3-3. The scheme of the binary-weighted resistive array with a bridge resistor.

We can simplify the circuit scheme to investigate the settling behavior of using resistive array to charge the sampling capacitor. The diagram is shown in Fig. 3-4. In Fig 3-4, V_{ref} is the reference voltage generated by the resistive DAC. R is the Thevenin's equivalent output resistance of the resistive DAC, C is the sampling capacitance and C_p is the parasitic capacitance at the output of the circuit.

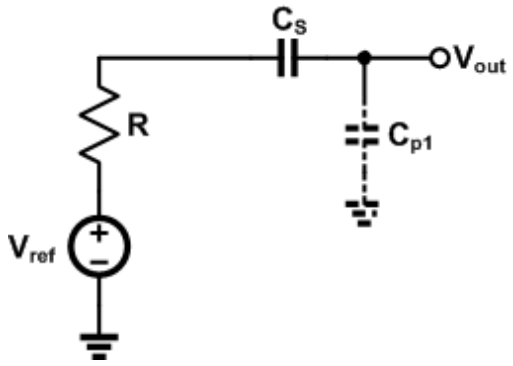


Fig. 3-4. The diagram of the simplified circuit.

After some calculation, we get

$$V_{out} = \frac{V_{ref}}{1+\frac{C_{p1}}{C_S}} u(t) \cdot \left(1 - e^{-\frac{1+\frac{C_{p1}}{C_S}}{RC_{p1}} t}\right) \tag{3-4}$$

If $C_S >> C_p$, then equation (3-4) will give approximately

$$V_{out} = V_{ref} u(t) \cdot \left(1 - e^{-\frac{1}{RC_{p1}} t}\right) \tag{3-5}$$

From equation (3-5), we can see that the time constant is RC_{p1}, which means only the parasitic capacitance will influence the settling behavior. Since the parasitic capacitance is very small, the total resistance of the DAC can be chosen to be very large, resulting in small static power consumed by the resistive DAC.

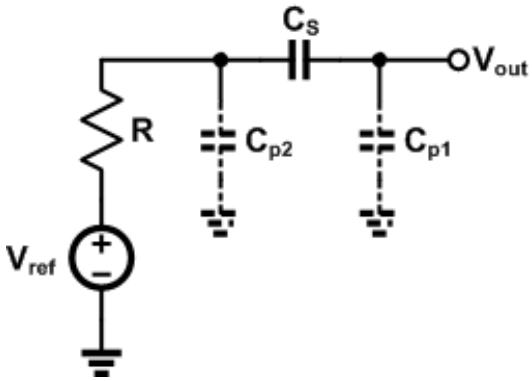


Fig. 3-5. The diagram of the simplified circuit with parasitic capacitors C_{p1} and C_{p2}.

If we consider the parasitic capacitor between the resistive array and the sampling capacitor, C_{p2}, as shown in Fig 3-5, equations (3-4) and (3-5) need to be rewritten as

$$V_{out} = \frac{V_{ref}}{1+\frac{C_{p1}}{C_S}} u(t) \cdot \left(1 - e^{-\frac{C_S + C_{p1}}{R\left(C_S C_{p1} + C_S C_{p2} + C_{p1} C_{p2}\right)} t} \right) \tag{3-6}$$

If C_{p1} and C_{p2} are much smaller than C_S, equation (3-6) will give approximately

$$V_{out} = \frac{V_{ref}}{1+\frac{C_{p1}}{C_S}} u(t) \cdot \left(1 - e^{-\frac{1+\frac{C_{p1}}{C_S}}{R\left(C_{p1} + C_{p2}\right)} t} \right) \approx V_{ref} u(t) \cdot \left(1 - e^{-\frac{1}{R\left(C_{p1} + C_{p2}\right)} t} \right) \tag{3-7}$$

From equation (3-6) and (3-7), the settling is still mainly determined by the equivalent output resistance of the resistive DAC and the total parasitic capacitors at the path from the output of the DAC to the input of the comparator.

The approach to calculate the static power of the resistive DAC is given next. The R-2R DAC is chosen for an example.

$$I_1 = \frac{d_1 V_r - V_{out}}{2R} \tag{3-8}$$

$$I_i = \frac{d_i V_r - \left[V_{out} - R \sum_{k=1}^{i-1} (i-k) I_k \right]}{2R}, \text{ (i=2,3,…,n)} \tag{3-9}$$

$$I_{n+1} = \frac{R \sum_{k=1}^{n-1} (i-k) I_k - V_{out}}{2R} \tag{3-10}$$

Therefore, the total static power consumed by the DAC is

$$P = \sum_{i=1}^{n} d_i I_i V_r \tag{3-11}$$

where V_r is the reference voltage. I_i is the current flowing through each leg. I_1 is the current flowing through the MSB leg and I_{n+1} is the current flowing through the dummy one.

For fair comparison of the static power consumption of these four resistor DACs, we assume that the output resistances of these four DACs are same. Also, we assume that the total parasitic capacitances on the path from the output of the resistive block to the input of the comparator are the same for all cases. Therefore, we only need to guarantee that the output resistances of four resistive blocks are the same in order to get same settling time of the voltage at the inputs of the comparators.

The unit resistance is determined by the settling time. For a 1GSample/s, 6-bit architecture, the voltage at the input of the comparator should settle within 6-bit accuracy in 0.5ns. From previous design, C_p is estimated to be 20 fF. Therefore,

$$-RC_p \ln\left(\frac{1}{2^N}\right) \le \frac{T_s}{2} \tag{3-12}$$

$$-RC_p \ln\left(\frac{1}{2^6}\right) \le 0.5n \tag{3-13}$$

$$R \le 6k\Omega \tag{3-14}$$

The largest output resistance of the resistive string occurs when the reference voltage is in the middle of the string and its value is $2^{N/4}*R_{u1}$, where R_{u1} is the resistance of one unit resistor. For the R-2R ladder, the binary-weighted resistive DAC and the binary-weighted resistive DAC with bridge resistor, the output resistance is

always R_{u2}, where R_{u2} is the resistance of the unit resistor. Hence,

$$R_{u2} = \frac{2^N}{4} \cdot R_{u1} = 6k\Omega \tag{3-15}$$

The comparison of the static power consumed by these four resistive DAC when they are used in the pipeline SAR ADC architecture is illustrated in Fig 3-6. The x-axis is the number of the bits of the DAC while the y-axis is the average static power dissipation. It is demonstrated that the resistive string consumes the least power and the R-2R resistive ladder consumes the most power. Therefore, in terms of the average static power dissipation, the resistive string is the best choice for the architecture.

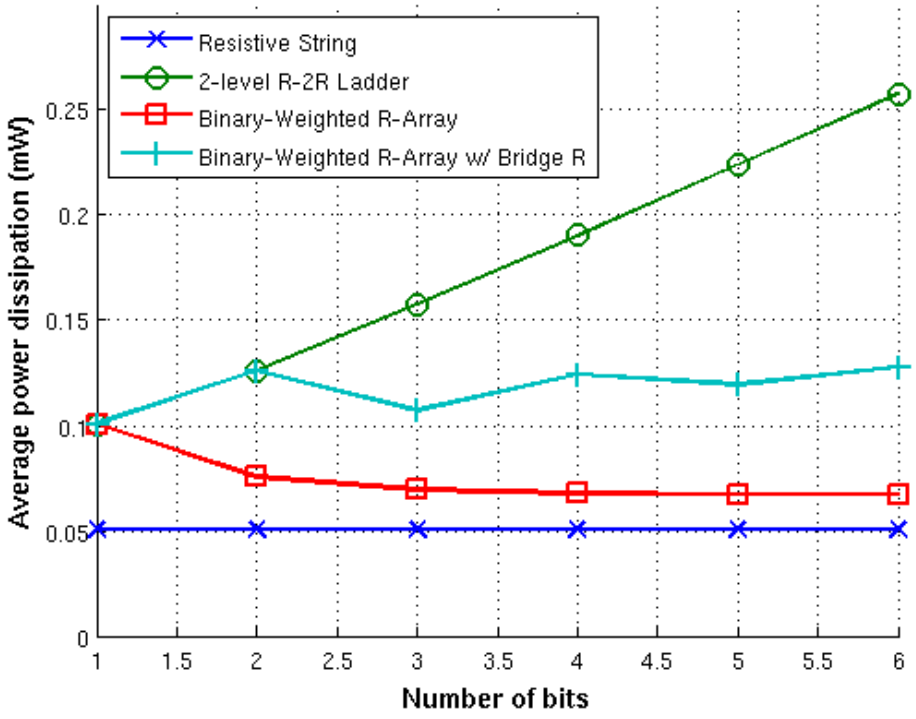


Fig. 3-6. The average static power dissipation by four kinds of resistive DACs of different resolution.

3.2 Logic delay of the circuit

Since the DAC is implemented in the architecture working at 1GHz, the logic delay should be minimized. If the resistive ladder is used for all stages, then the control logic for the switches in each stage is shown in Fig 3-7.

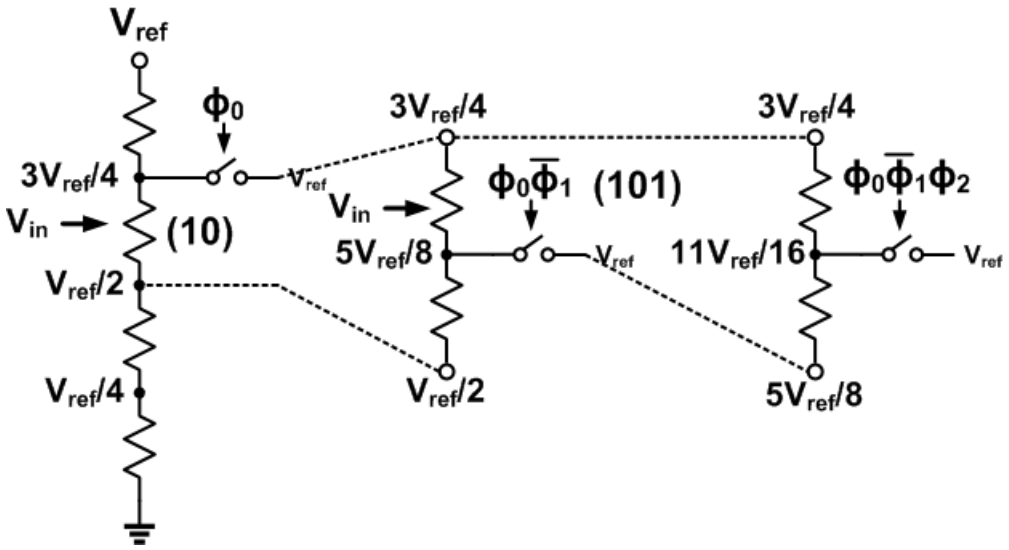


Fig. 3-7. An example of a 4-bit binary-search algorithm on a resistive string.

Fig 3-7 demonstrates an example of a 4-bit binary-search algorithm on a resistive string. The MSB bit is determined by just comparing V_{inp} and V_{inn} without any reference voltage. For LSB determination, the controlling signal of the switch connecting the reference voltage is an AND logic of three previous bits, which needs two 2-input AND gates. The higher the resolution of the DAC is, the more AND gates are needed for generating the controlling signal of the LSB reference voltage switches, which will need more gate delay.

In order reduce the gate delay, the binary-weighted resistive DAC with a bridge

resistor is taken into consideration. Since the previous bits directly control the corresponding bottom switches in the DAC, no logic gates are needed except for some inverters as the local buffers for the signal. Therefore, this kind of DAC is used in the last three LSB stages as reference DACs in the architecture. Moreover, since the number of switches used for the resistive string is exponentially increased with number of bits, while the number of the switches in the binary-weighted resistive DAC is linearly increased, only a 1-bit and a 2-bit resistive strings are used in this architecture. This can significantly limit the silicon area required for the switches and the digital control.

In conclusion, in terms of the static power dissipation, the resistive string consumes the least power. However, control signals for the switches in this DAC need to pass through the logic gates, particularly for the LSB switches, if the DAC is used as SAR DAC, which introduces large logic gate delay. In [3-1], new AND gates are used to minimize the logic delay in high-speed application. The binary-weighted resistive DAC with bridge resistor is a good choice when the resolution of the DAC is high. Since all stages in this pipeline SAR ADC only resolve one bit for one input signal and the output refreshes in every clock cycle, the new AND gates in [3-1] cannot be used. Therefore, two kinds of DACs are used in this pipeline SAR ADC. The resistive strings are used in the second and the third MSB stages, while the binary-weighted resistive DACs with bridge resistor are used in the last three LSB stages. The architecture is shown in Fig 3-8. The second and sixth stages are shown in Fig 3-9 and

Fig 3-10. The other stages are similar to these two stages.

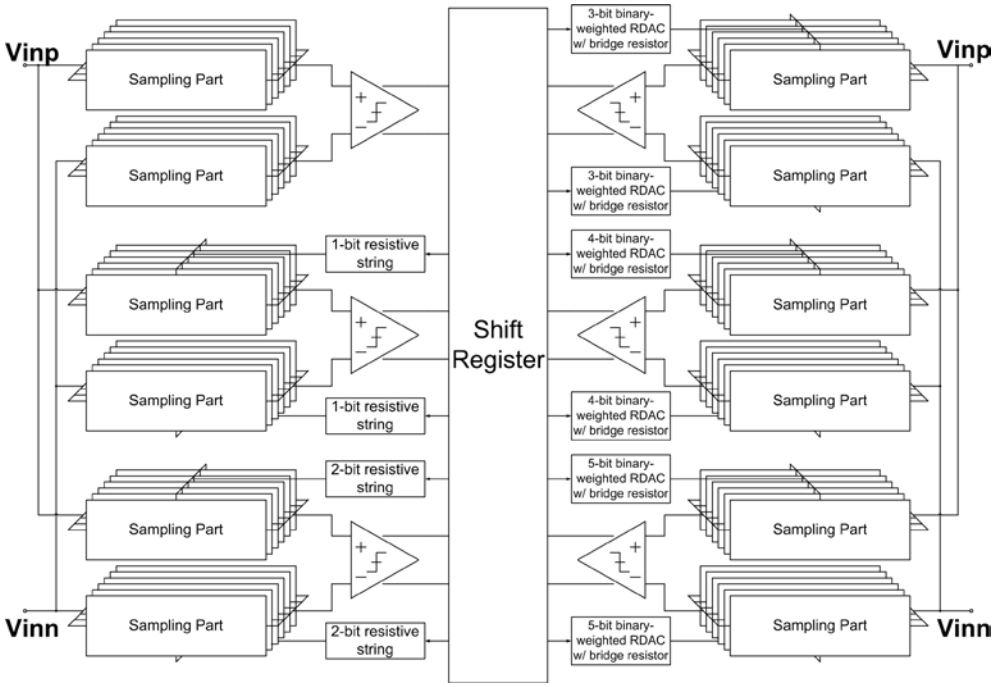


Fig. 3-8. The architecture of the pipeline SAR ADC with resistive DACs.

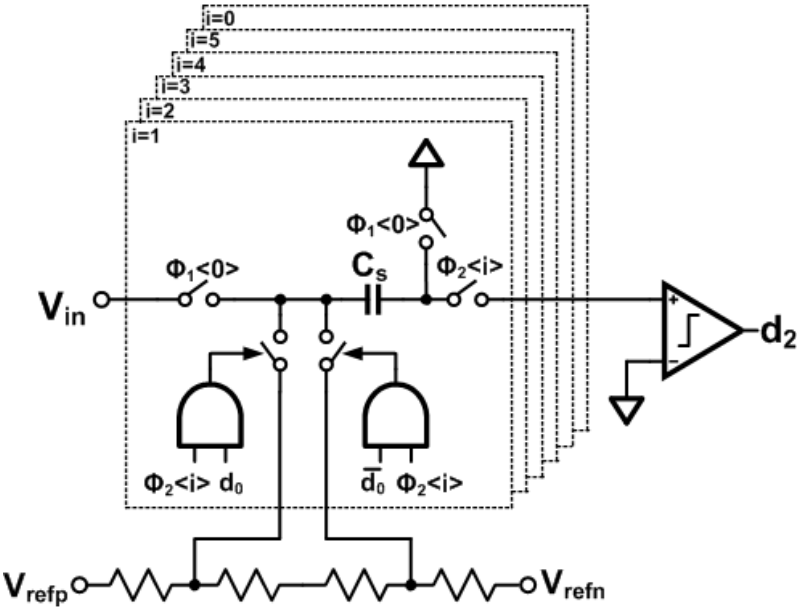


Fig. 3-9. The diagram of the second stage with resistive string as the DAC.

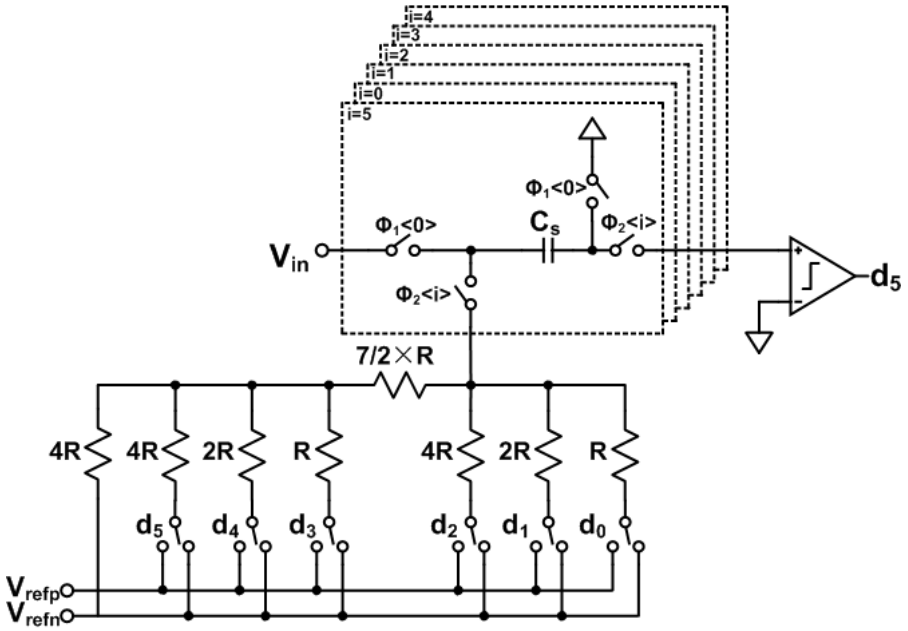


Fig. 3-10. The diagram of the sixth stage with binary-weighted resistive DAC with a bridge resistor as the DAC.

3.3 Layout

Since the parasitic capacitors except the one at the input of the comparator will not introduce any voltage attenuation on the input signal, the folded-stair layout pattern is no longer needed. The layout can be more compact, as shown in Fig 3-11. The input is at the bottom and the output is at the top. The area is 39μm×56μm while the area of the folded-stair layout pattern used in previous version is 50μm×100μm, which means the new sampling part is more than twice smaller.

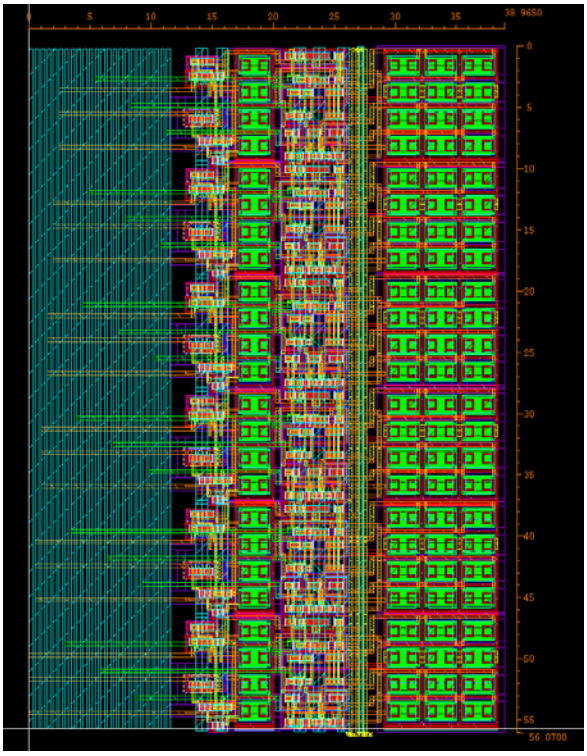
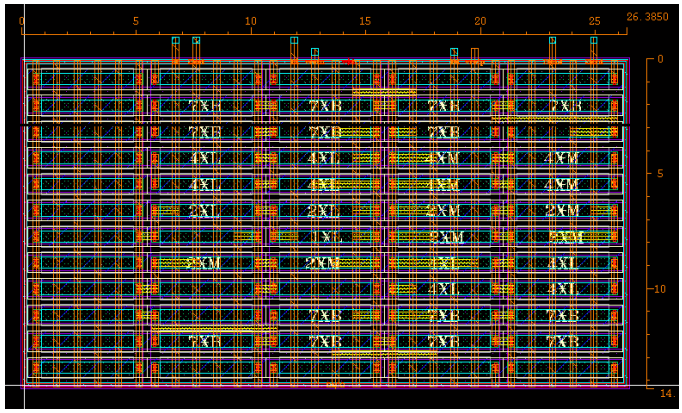
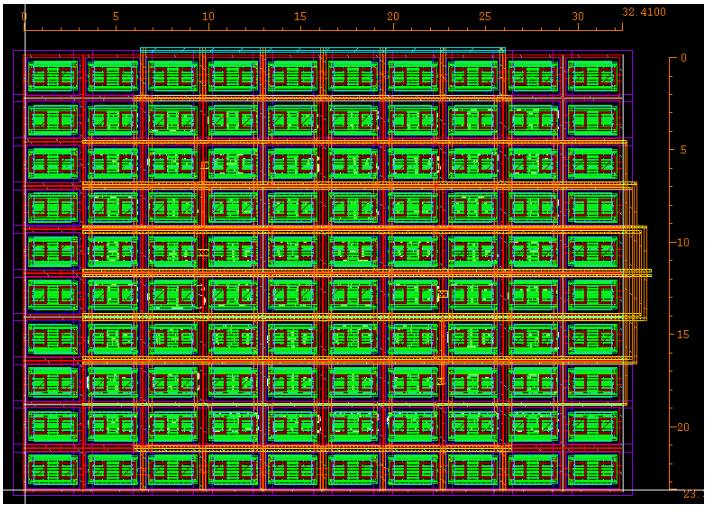


Fig. 3-11. The layout of the sampling part of the pipeline SAR ADC with the resistive DACs.

The layout the 5-bit resistive DAC used in the LSB stage is illustrated in Fig 3-12(a) and its counterpart, the 5-bit capacitive DAC needed in the LSB stage in the pipeline SAR ADC with capacitive DAC is shown in Fig. 3-12(b). The area occupied by this resistive DAC is about 30μm×15μm, while the area of the capacitive DAC is 32μm×24um. The resistive DAC is 40% smaller than the corresponding capacitive DAC.



(a)



(b)

Fig. 3-12. (a) The 5-bit resistive DAC in the LSB stage and (b) the 5-bit capacitive DAC in the LSB stage of the two kinds of pipeline SAR ADCs.

The layout of the third channel with resistive string is shown in Fig 3-13 and the layout of the sixth channel with binary-weighted resistive DAC with a bridge resistor is shown in Fig 3-14.

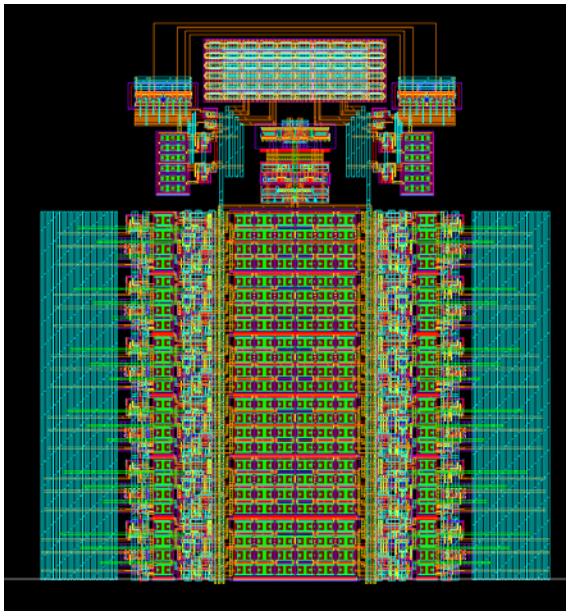


Fig. 3-13. The layout of the third channel with a 3-bit resistive string.

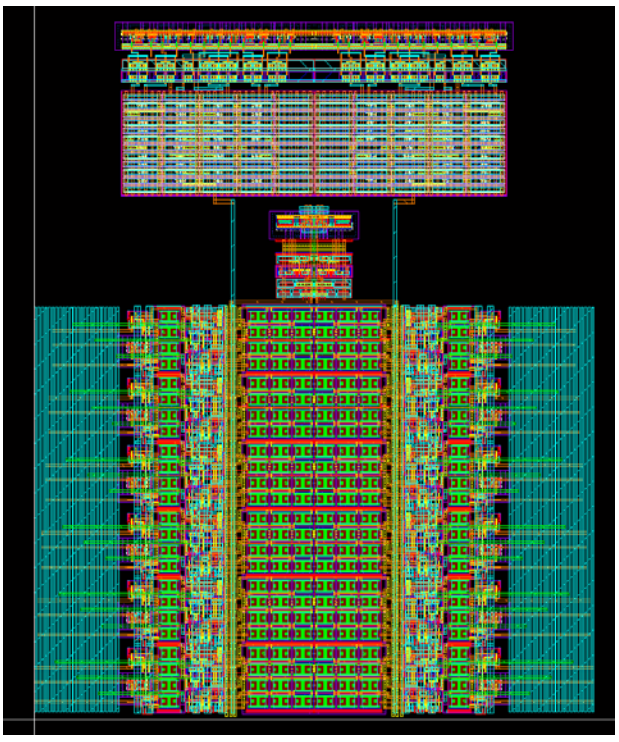


Fig. 3-14. The layout of the sixth channel with a 5-bit binary-weighted resistive DAC with a bridge resistor.

3.4 Summary

The output spectrum of this architecture is shown in Fig 3-15. It is a 256-length FFT. The SNDR can achieve 37dB.

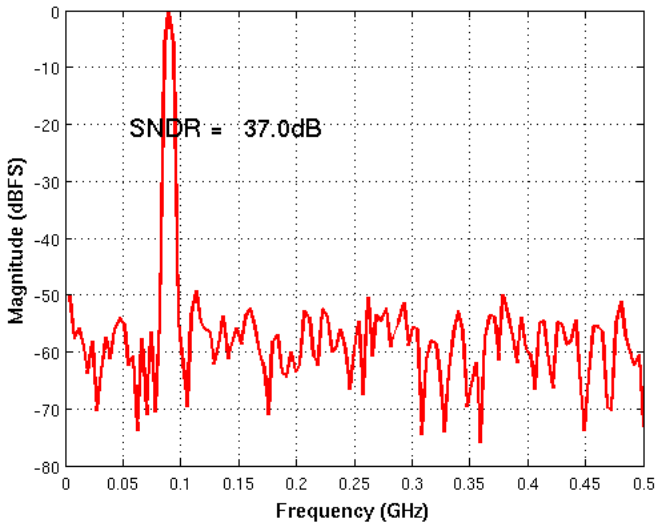


Fig. 3-15. The 256-length FFT of the 1GSample/s 6-bit pipeline SAR ADC with resistive DACs.

The performance of the circuit is listed in Table II. The chart in Fig 3-16 demonstrated the power breakdown of the pipeline SAR ADC with the resistive DACs. The power dissipated by the resistive DAC is only 22% of the total power. The power burned from avdd including the power consumed by the sampling switches and the comparators. The power dissipated from dvdd including the power consumed by the clock generator, local clock buffers, logic gates in the resistive DACs and the output latches of the comparators.

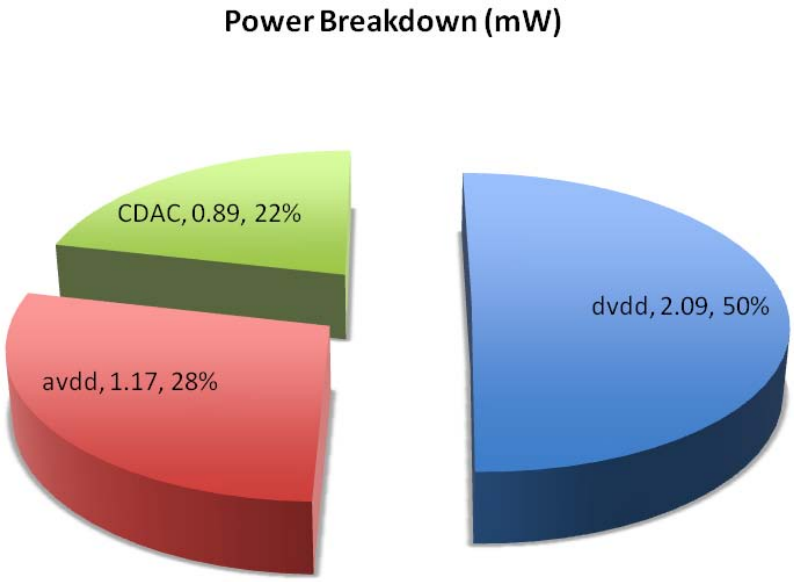


Fig. 3-16. The chart of power breakdown. Total power is 3.99mW.

Table 3-1. The performance of the 6-bit 1GSample/s pipeline SAR ADC with resistive DACs

Technology	40nm CMOS Technology
Resolution	6-bit
Supply Voltage	1.1V
Input Range	2.2 V_{ppd}
Clock Frequency	1GHz
SNDR	37dB
Power consumption	3.99mW
FOM	80fJ/Conv.-Step

4 The Low Power Multi-Step Capacitor-Splitting SAR ADC

4.1 Design Techniques for Low-Power Capacitive DAC

Successive-approximation-register analog-to-digital converters (SAR ADCs) are useful for low-power, medium-resolution applications. Fig 4-1 shows the conventional capacitive DAC for SAR ADC [4-1].

The algorithm is as followed. The largest capacitor, i.e. the 16C in Fig 4-1 is switched to V_{ref} first while other capacitors are connected to ground so that V_{out} is $V_{ref}/2$. If V_{out} is larger than the input voltage V_{in}, 16C is left connected to V_{ref} and b1 is considered to be a 1. Otherwise, 16C goes back to ground and b1 is taken to be 0. This process is repeated until all bits are determined.

The conventional SAR architecture needs a capacitor array with 2^N unit capacitors, where N is the resolution in bits. For typical resolutions (N = 10~12) the array occupies a large chip area. It also consumes considerable switching power during conversion. In the “down” transition, i.e. the comparator decision is zero and current bottom plate switch needs to switch from V_{ref} back to ground, the energy is wasted because the capacitive array needs to be discharged first and recharged to a new voltage. It requires five times more energy to lower Vout than to raise it by the same amount [4-2].

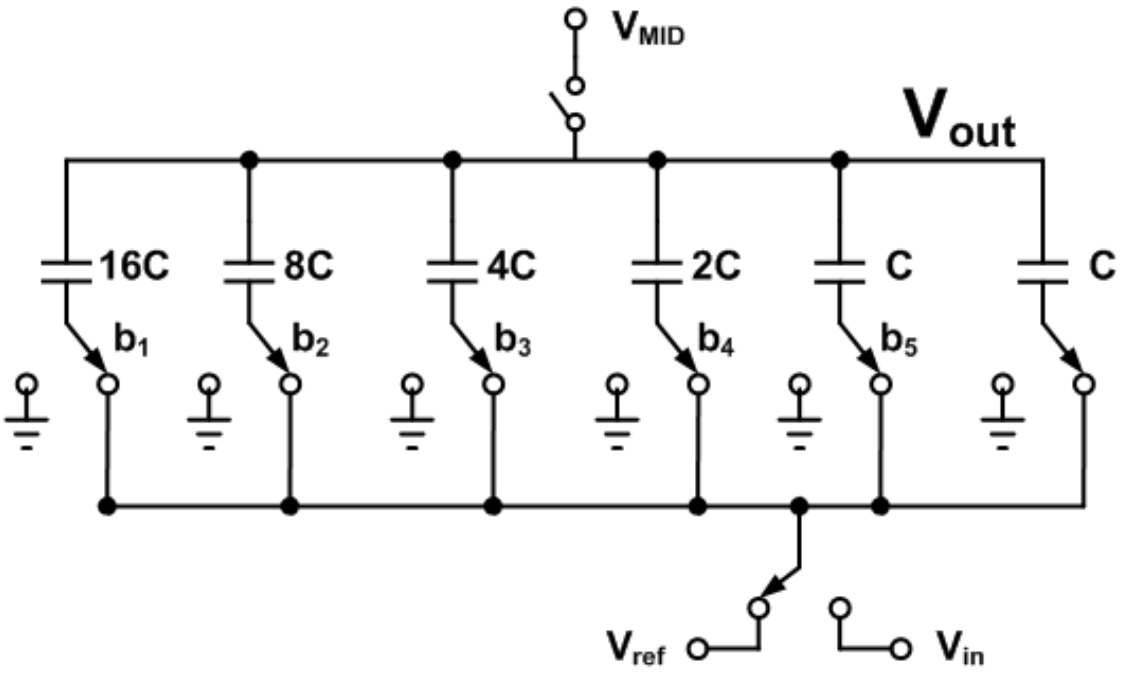


Fig. 4-1. The 5-bit conventional capacitive DAC for a SAR ADC.

Several recent papers proposed improved schemes to reduce the chip area and/or the power dissipation. Ref. [4-2] describes a capacitor-splitting SAR array that reduces the switching power by 37% for 10-bit resolution, but still needs 2^N unit capacitance. Compared with the conventional SAR DAC, the MSB capacitor is split into a copy of the rest of the capacitor array, as shown in Fig 4-2.

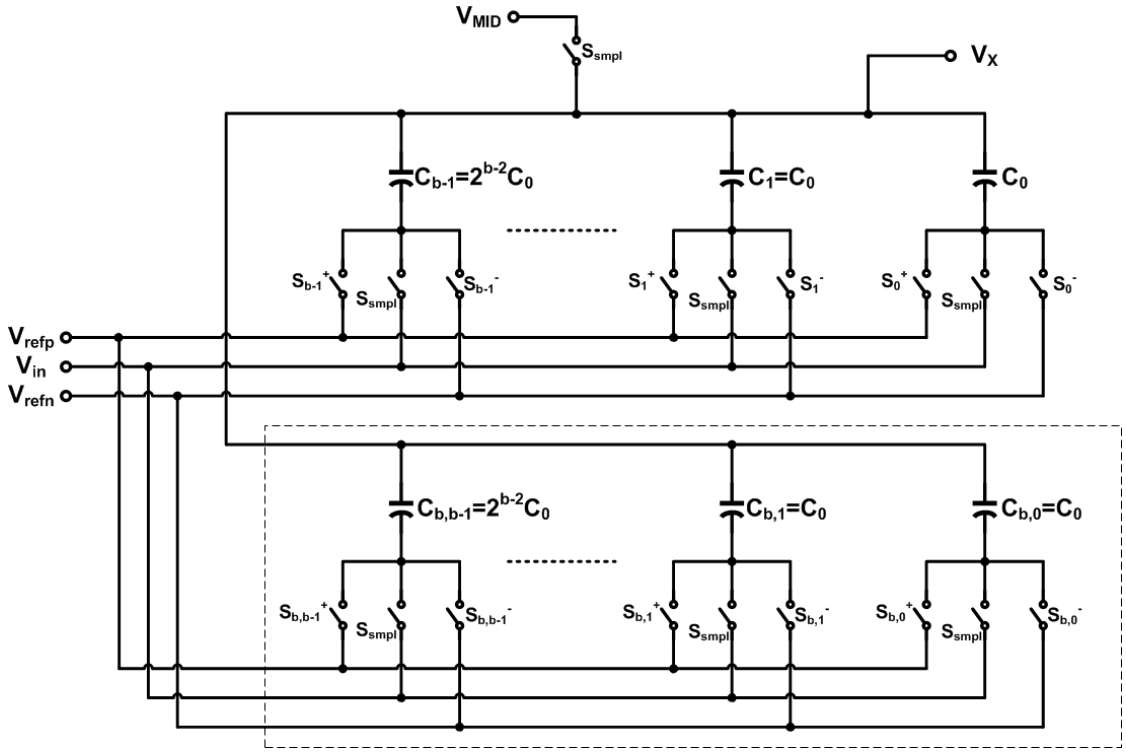


Fig. 4-2. b-bit capacitor-splitting array. The largest capacitor (enclosured in a dotted box) is split into the copy of the rest capacitors.

The algorithm of the capacitor-splitting array is only different compared with the conventional one when the “down” transition happens, i.e., the sub-capacitor $C_{b,i}$ is connected to ground rather that C_i switches back to ground. Therefore, the “down” transition dissipates the same power as the “up” transition.

The junction-splitting SAR ADC [4-3], as shown in Fig 4-3, saves 75% of the switching power for 10-bit resolution by eliminating the “down” transition. For MSB conversion, the two smallest capacitors are used to generate the $V_{ref}/2$. If Vin is larger than $V_{ref}/2$ and b_0 is 1, S_p^1 and S_0^1 are closed and 2C is connected with V_{ref} and C/C block. Otherwise, S_p^1 and S_0^0 are closed and 2C is connected with ground and C/C

block. During each conversion cycle, one sub-capacitor section is appended to the previous capacitor array and the bottom-plate switch connects to Vref or ground based on the decision just made. The process continues until all bits are determined.

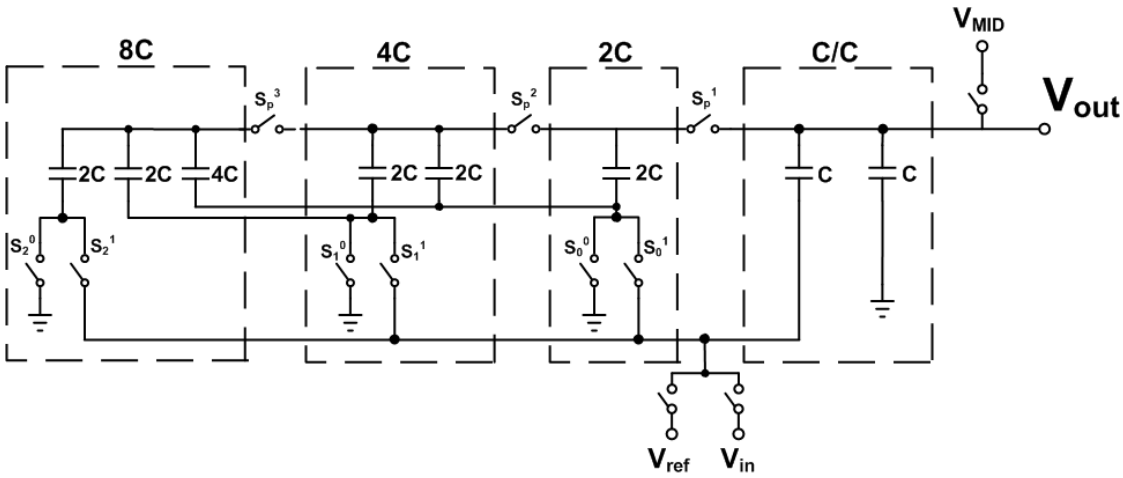


Fig. 4-3. A 3-bit junction-splitting SAR DAC.

However, the junction-splitting SAR DAC still requires 2^N unit capacitance and also is more sensitive to the mismatch of the capacitors, because the MSBs are determined by the smallest capacitors.

Both the capacitor-splitting DAC and the junction-splitting DAC focus on the modification of switching algorithm while keep the total capacitance be 2^N unit capacitance. At each step, the reference voltage generated by the capacitive DAC is

$$V_{out} = V_{MID} - V_{in} + \frac{C_{ref}}{C_{ref} + C_{gnd}} V_{ref} \tag{4-1}$$

Where C_{ref} is the total capacitance connected to V_{ref} and C_{gnd} is the total capacitance connected to ground. The sum of the C_{ref} and C_{gnd} is the total capacitance of the capacitive DAC, C_{tot}. Therefore, we can simplify the SAR algorithm as shown in Fig

4-4. In order to make the analysis simpler, V_{MID} and V_{in} are supposed to be 0. Therefore, the switching energy consumption can be calculated as followed.

$$E = V_{ref} \cdot x \cdot C_{tot} \cdot \left(V_{ref} - x \cdot V_{ref}\right) = x\left(1-x\right)C_{tot}V_{ref}^2 \tag{4-2}$$

If we plot E versus V_{out}, we can get the diagram illustrated in Fig 4-5.

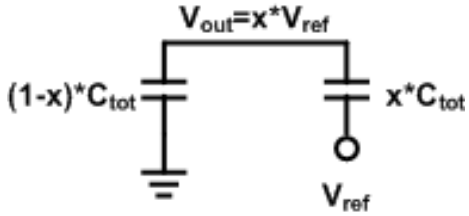


Fig. 4-4. Simplified charge redistribution between capacitors connected with V_{ref} and ground.

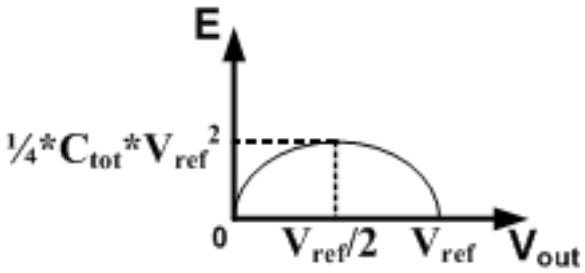


Fig. 4-5. The curve of equation 4-2.

For charge distribution, the energy is only “wasted” in the “down” transition for SAR algorithm. The energy consumptions are same when the voltage boosts from V_1 to V_2 in one step or in two or more steps since the power dissipation is only determined by the final state. Therefore, equation (4-2) and Fig 4-5 demonstrate the fundamental lowest switching energy consumption of capacitive DAC. In conclusion, the junction-splitting algorithm has achieved the lowest switching energy consumption for the capacitive DAC whose total capacitance is 2^N unit capacitance.

In order to further lower the switching energy, one possible method is to reduce the total capacitance and use a charge-sharing approach.

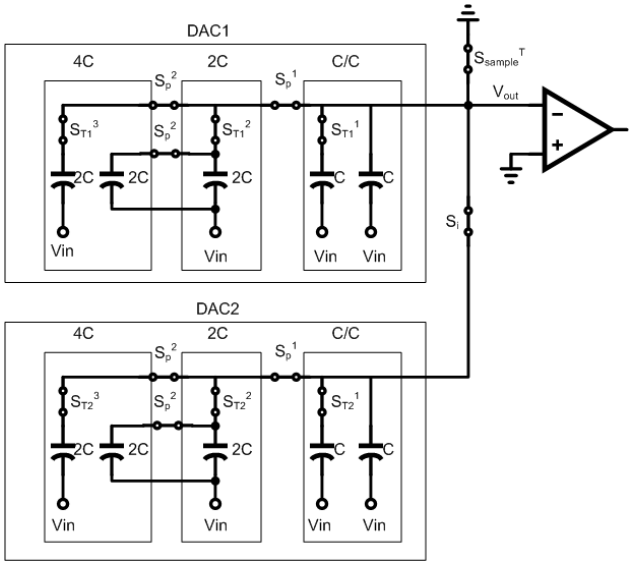


Fig. 4-6. Sampling phase of the two-step junction-splitting SAR ADC.

A two-step junction-splitting SAR ADC was proposed in [4-4]. The circuit is shown in Fig 4-6. The total capacitance is reduced to $2^{N/2}+1$ unit capacitance, and the total switching power is reduced by 92 % for a 10-bit resolution. The N-bit two-step junction-splitting SAR uses two N/2-bit junction-splitting capacitive array to determine the first N/2 bits following the junction-splitting algorithm. Then it uses one more phase to generate the upper and lower bound voltages for the next fine conversion by connecting two junction-splitting capacitive array together. In fine conversion, it uses charge-sharing method to generate reference voltage and determine the remaining N/2 LSBs. However, since the two-step junction-splitting SAR uses the junction-splitting algorithm, the conversion remains sensitive to the mismatch of the

array capacitors.

4.2 Multi-Step Capacitor-Splitting SAR ADC

The multi-step capacitor-splitting SAR ADC combines the mismatch insensitivity of the conventional SAR ADCs with the reduced power and capacitor area of the structure in [4-5]. The capacitive array is shown in Fig 4-7. For simplicity, the proposed structure illustrated in Fig 4-8 is an 8-bit (N = 8) ADC. It contains two 4-bit split-capacitor arrays (SCAs) and a comparator. Initially, the input signal is sampled on both SCAs, as shown in Fig 4-8. Next, coarse quantization is performed to generate the first N/2 = 4 MSBs, using both two SCAs in parallel. Switch S is closed during these operations. In the first step of the coarse quantization, the bottom plates of all capacitors in the two 8C sections are connected to V_{ref}, which generates the test voltage $V_{ref}/2$ for determining the MSB, as shown in Fig 4-9. The next three changes in the bottom-plate voltages of the capacitors follow the capacitor-splitting algorithm of ref. [4-2]. Fig. 4-10 shows the circuit state when the 4th bit is being generated.

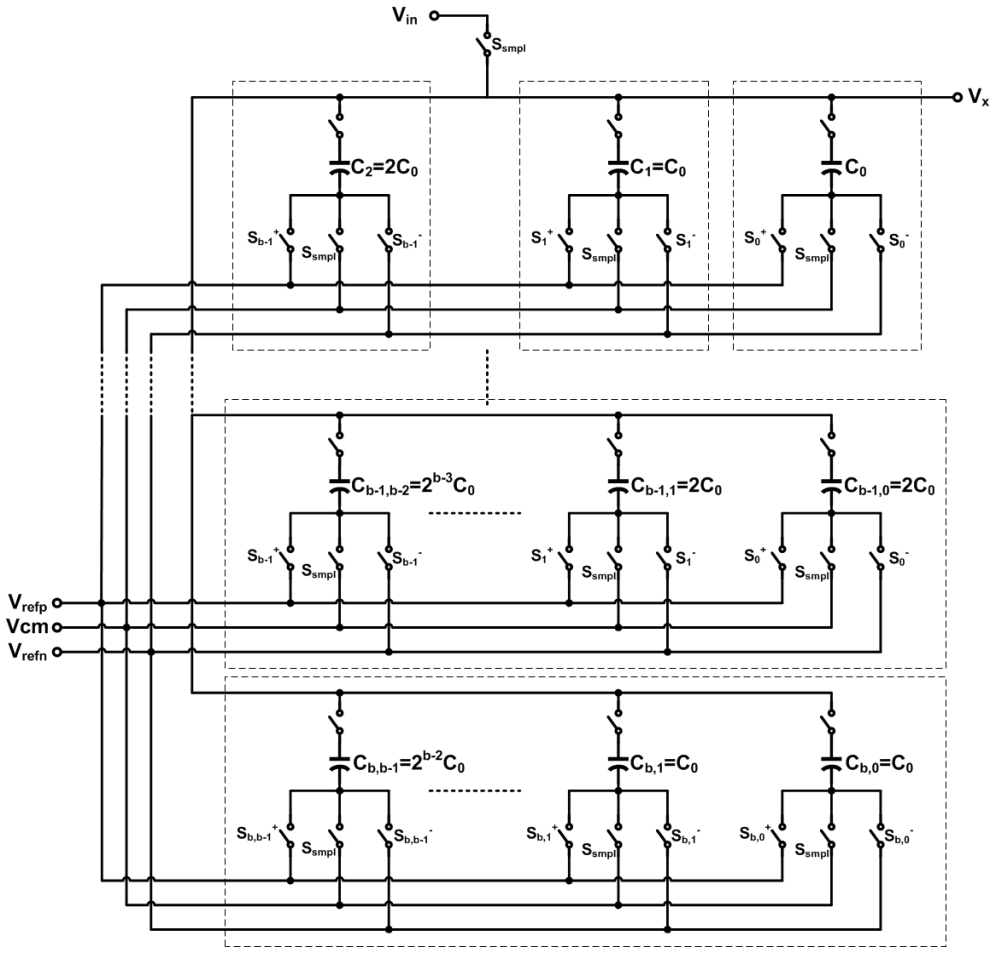


Fig. 4-7. b-bit multi-step capacitor-splitting SAR DAC.

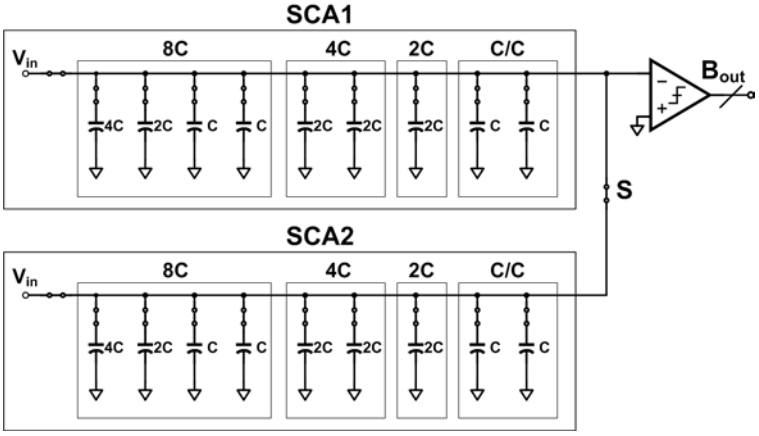


Fig.4-8 The input sampling phase for a 8-bit SAR ADC.

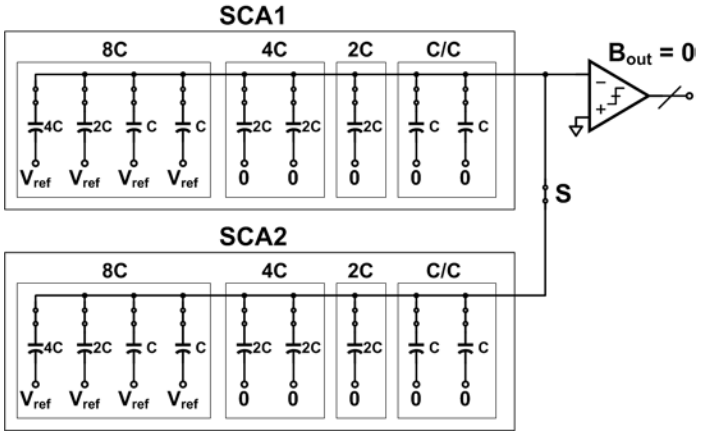


Fig. 4-9. First step in the coarse quantization phase.

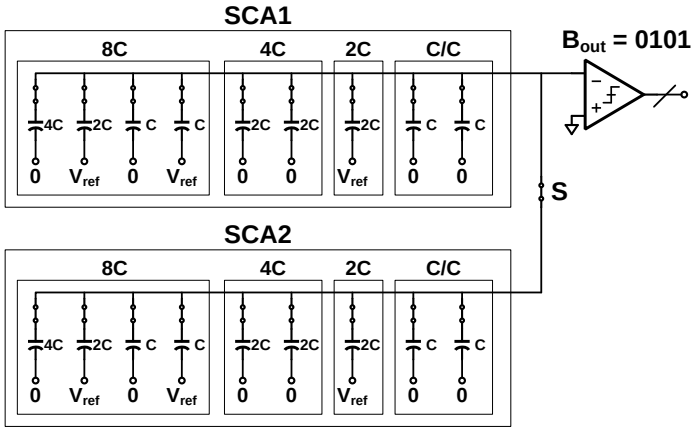


Fig.4-10. Circuit states for determining the 4th bit in the coarse quantization phase.

After the 4th comparison is complete, switch S is turned off. At this point, the states of SCA1 and SCA2 are identical. They both hold the same voltage, which can be used either as a lower bound (LB) or as an upper bound (UB) of the input voltage during the fine quantization, depending on the last bit obtained in the coarse quantization phase. By changing the bottom-plate voltage of the rightmost capacitor of SCA2, a new UB can be obtained. Alternatively, by changing the bottom-plate voltage

of the right-most capacitor of the 8C block in SCA2, a new LB results. In our example, since the last bit in coarse quantization phase is a “1”, the LB already exists across both arrays, and the UB has to be generated across SCA2. This is done by changing the bottom-plate voltage of the rightmost capacitor of SCA2 to V_{ref}, while the bottom-plate voltages of all other capacitors in both SCAs are kept unchanged (Fig. 4-11). Afterwards, all switches connected to the top plates of all capacitors in both SCAs will be turned off.

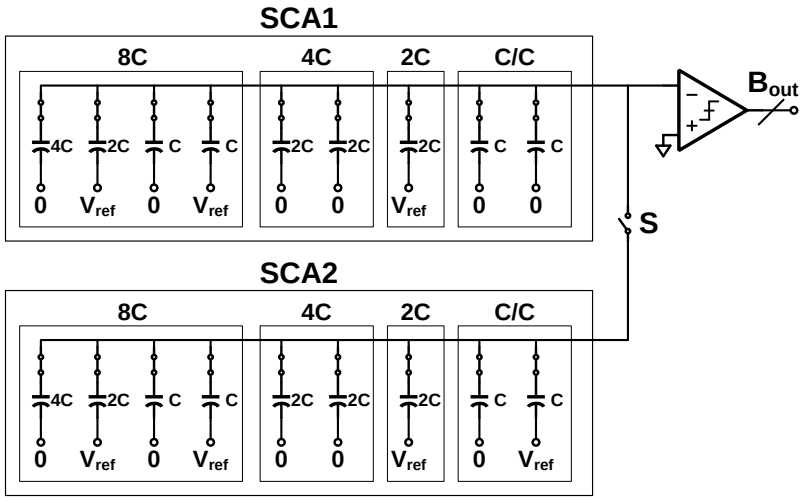


Fig. 4-11. Bound setting for the fine quantization phase.

In the following fine quantization, the capacitors in the SCAs are connected in parallel, section by section, to generate all comparison voltages as in the SAR ADC of ref. [4-4]. During the fine quantization phase, the bottom-plate voltages of all capacitors are left unchanged. Fig 4-12 to Fig 4-15 shows the final circuit state after the LSB has been determined.

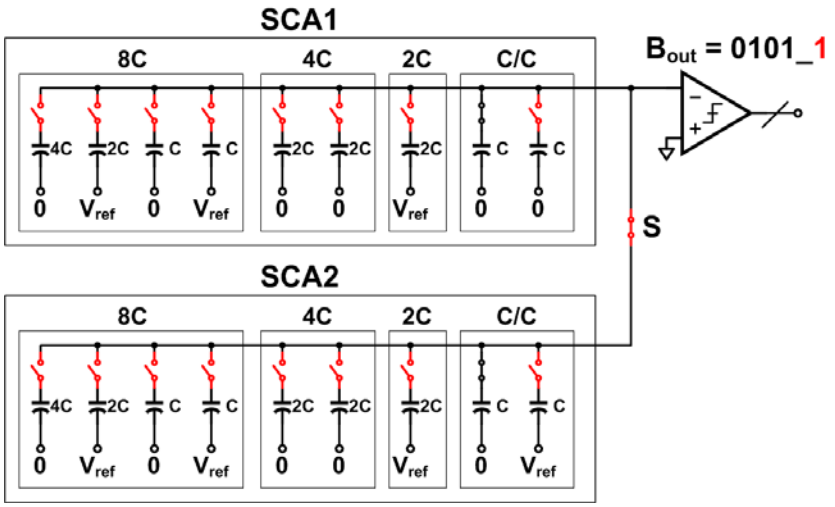


Fig.4-12. Circuit state for determining the 5th bit in the fine quantization phase.

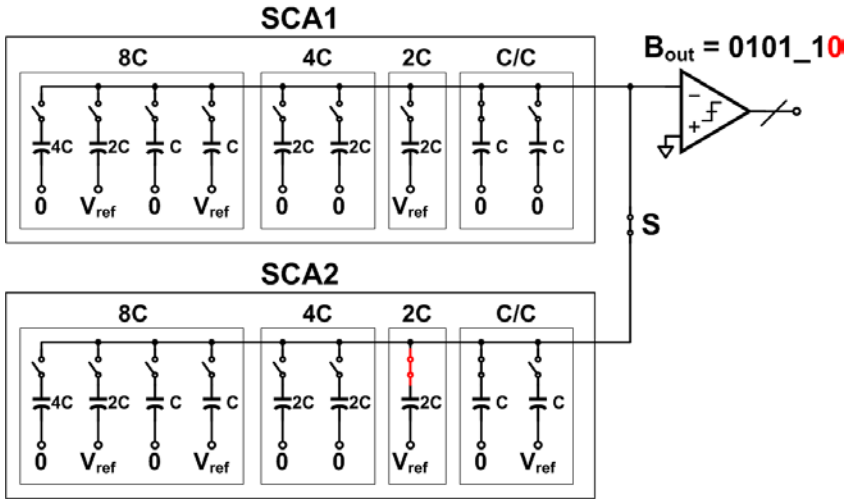


Fig.4-13. Circuit state for determining the 6th bit in the fine quantization phase.

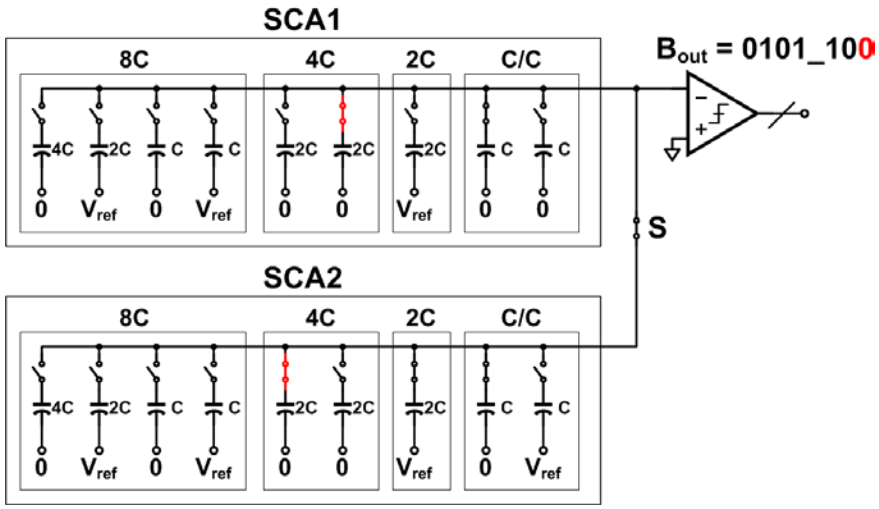


Fig.4-14. Circuit state for determining the 7th bit in the fine quantization phase.

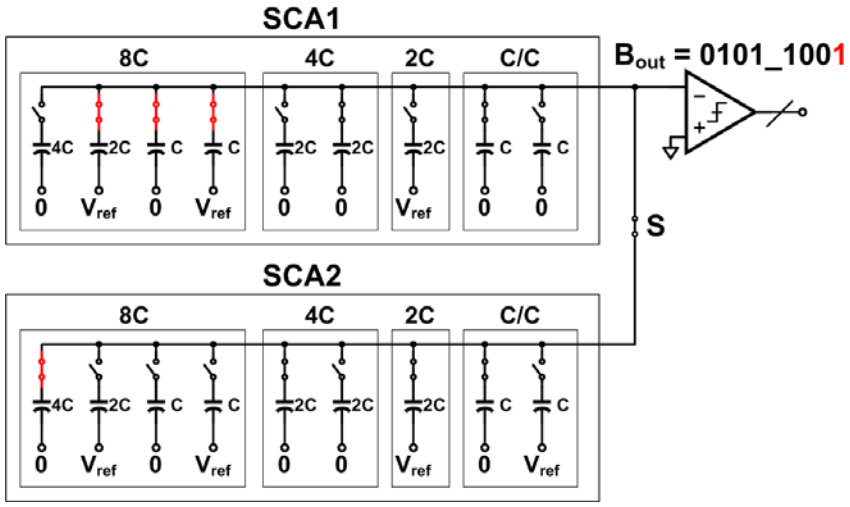


Fig.4-15. Circuit state for determining the LSB in the fine quantization phase.

As in the two-step junction-splitting SAR ADC [4-4], the conversion requires N+1, rather than N, clock periods. However, the proposed architecture saves most of the power and capacitor area by reducing the total number of unit capacitors needed. For example, in an 8-bit SAR ADC, in the earlier schemes of [4-1] – [4-3] 256 unit capacitors are needed, while in the proposed structure only 32 units (16 for each SCA)

are used. Since the power consumption is proportional to the total capacitance, a 96% saving in switching power consumption can be achieved for a 10-bit resolution compared to conventional SAR ADCs. The saving is even larger for higher-resolution ADCs.

4.3 Conclusions

Fig. 4-16 illustrates the switching power consumption of the proposed architecture and of the earlier SAR schemes for a 10-bit-resolution structure, as a function of the output code. Although our earlier scheme [4-4] requires slightly less switching power, the new architecture is much less sensitive to the mismatch of the capacitors, since it uses the largest capacitors to determine the MSBs, rather than the smallest ones. Moreover, the accuracy of the process of deriving the N/2 MSBs is also increased, since the two SCA DACs are connected in parallel during the coarse quantization phase. Table 4-1 illustrates a summary of the discussed five SAR capacitive arrays.

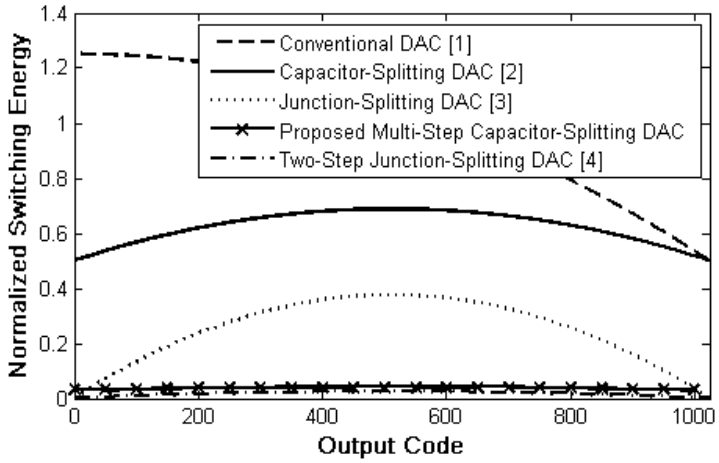


Fig. 4-16 The switching energy per cycle versus output code required for the capacitor arrays in 10-bit SAR ADCs.

Table 4-1. Switching methodology comparison

Capacitive Array	Total Capacitance (C is the Unit Capacitance)	Normalized Avg. Switching Energy for 10-bit Uniform Input
Conventional Cap. Array	$2^N \times C$	1
Conventional Capacitor-Splitting Cap. Array	$2^N \times C$	0.62
Conventional Junction-Splitting Cap. Array	$2^N \times C$	0.25
Two-Step Junction-Splitting Cap. Array	$(2^{N/2+1}) \times C$, N is even	0.02
	$(2(^{N+1)/2+1}) \times C$, N is odd	
Multi-Step Capacitor-Splitting Cap. Array	$(2^{N/2+1}) \times C$, N is even	0.04
	$(2(^{N+1)/2+1}) \times C$, N is odd	

5 Conclusion

A 6-bit 1GSample/s pipeline SAR ADC with capacitive DACs was implemented in 40nm CMOS process. Several schemes were used to overcome the influences from the parasitic capacitors. By splitting one sample capacitor into six identical ones in each stage, it greatly reduced the accumulated effect of charge sharing between the sampling capacitor and the parasitic capacitor at the input node of the comparator from the first to the last stages. By flipping the sampling capacitor once before stacking it with the capacitive array, the circuit not only diminishes the issue of different attenuation ratios on the sampled input signal and the reference voltage, but also lowers the switching energy in the capacitive DACs. Moreover, the dummy switches added to trim the parasitic capacitors at the connection node between the sampling capacitors and DACs can further match the attenuation ratio.

In order to overcome the influence from the parasitic capacitors more effectively, a 6-bit 1GSample/s pipeline SAR ADC with resistive DACs was designed in 40nm CMOS process. The parasitic capacitors will not introduce different attenuation ratios on the sampled input signal and the reference voltage. The parasitic capacitors only affect the settling time. Thanks to the advanced CMOS technology, the parasitic capacitance is very small, which allows the resistors in the DAC to be large enough to make the static power negligible, while the occupied area is even smaller than the capacitive DAC with same resolution.

A multi-step capacitor-splitting SAR ADC was proposed based on the capacitor-splitting SAR ADC and the two-step junction-splitting SAR ADC. The multi-step

capacitor-splitting SAR ADC is less sensitive to the mismatch of the capacitors than the two-step junction-splitting one, and saves more switching energy and area than the conventional capacitor-splitting one.

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