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This thesis will examine the model and design technique of a self-contained analog CMOS Phase-Locked Loop. This system has an adaptable filter and demodulator for an oscillating frequency of up to 1000 KHz and it is programmable by means of an external resistor and capacitor. The first topic to be presented will be the nonlinear feedback system concept and terminology, then the mathematical analysis for the phase comparator, low-pass filter, voltage-controlled oscillator and capture and lock range is developed. Finally, the circuit parameters, description, simulation and layout will be presented.

MODEL AND DESIGN OF CMOS PHASE-LOCKED LOOP

by

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MODEL AND DESIGN OF CMOS PHASE-LOCKED LOOP

CHAPTER 1

INTRODUCTION

Since the concept was first proposed in the early 1920's [1], the development of Phase-Locked Loop (PLL) systems has encouraged its widespread use in a variety of applications such as space telemetry, instrumentation, satellite communications, amplitude and frequency modulations, motor speed control, frequency shift key decoders and frequency synthesizers. The continued improvement of the concept of this system was significantly enhanced in the early 1970's when PLLs began to be built using bipolar junction transistor technology. This method substantially lowered the cost of implementation and in turn encouraged greater utilization of the PLL system. With the continuing advancement of various technologies and the PLL concept itself, these systems have an ever widening acceptance in a greater diversity of applications.

The majority of the integrated PLL systems are designed and fabricated in the more traditional bipolar technology in spite of the advancement of the Complementary Metal-Oxide-Semiconductor (CMOS) process in recent years. The objectives of this thesis are to design, simulate and layout a monolithic analog PLL circuit using a 2-um p-well CMOS process that can be fabricated by the Metal-Oxide-Semiconductor Integrated service (MOSIS).

The remaining topics of this thesis will be presented in the following format. Chapter 2 provides an overview of the Phase-Locked Loop concept. Chapter 3 describes the system blocks, modeling method and mathematical analysis. Chapter 4 contains the circuit parameters and design technique. Chapter 5 gives the SPICE simulation results and the equivalent circuit layout description. And lastly, the conclusions are presented in Chapter 6..

CHAPTER 2

AN OVERVIEW OF THE PHASE-LOCKED LOOP CONCEPT

The Phase-Locked Loop is basically an electronic feedback loop system consisting of a phase comparator, a low-pass filter, an amplifier in the forward path and a voltage-controlled oscillator in the feedback path of the loop [2]. A block diagram representation of the system is illustrated in Figure 2.1.

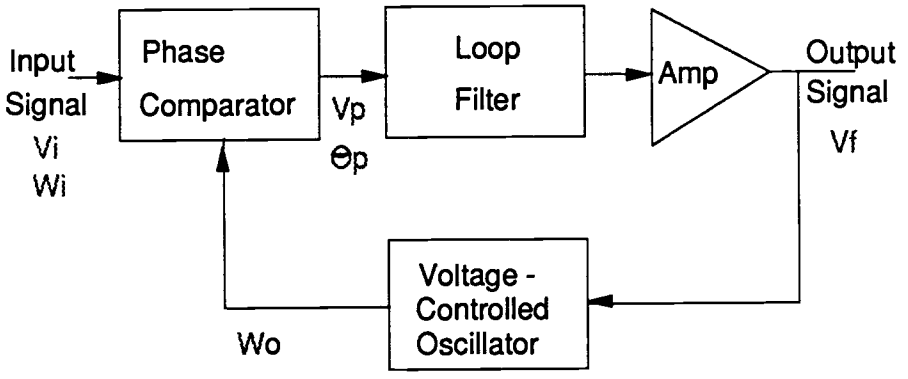

Figure 2.1 Phase-Locked Loop feedback system

Phase-Locked Loop (PLL) systems operate by adaptively producing an oscillating frequency to match the frequency of an incoming signal resulting in a "lock" condition when the two frequencies match each other. The frequency range over which the PLL can acquire lock is known as the "capture range". The capture process begins when a difference in frequency and phase between the incoming signal and the VCOs free running oscillating frequency is detected by the phase comparator. It subsequently produces an error output voltage that contains the sum and difference components of the two frequencies. If these AC components fall outside the low-pass filter band edge, no information can be passed

around the loop and the VCO output remains at the initial free running frequency. As the input signal approaches free running oscillation, the output waveform is again loop filtered and amplified such that only the low frequecy component can pass through.

This low frequency signal is then fed into the input of the voltage-controlled oscillator to force the oscillation frequency to move closer to the input frequency. This continuous positive feedback process eventually forces the PLL to lock in with the input signal. Once locked condition has been acquired and if input frequency changes slightly, the change would appear as a phase difference between the input and VCO signals. This phase difference results in a DC and a sum frequency component which is being filtered out by the low-pass filter.

The DC voltage is then fed back into the VCO to force the synchronization of the two frequencies. This self-correcting mechanism allows the PLL to track the frequency changes of the input signal once it is locked. The frequency range over which the PLL can remain locked once capture has occurred is known as the "lock range".

The above described ability of the loop VCO frequency to remain synchronized and maintain locked with the changing input signal makes PLLs particularly useful in the application of communication systems. Some of the most practical applications of PLL systems are in the area of phase, AM and FM modulation and demodulation.

CHAPTER 3

DESCRIPTION OF THE PHASE-LOCKED LOOP OPERATION

The basic principle of PLLs can be modeled by the conventional feedback system with the voltage-controlled oscillator in the feedback path and the phase comparator, loop filter and amplifier in the forward signal path of the system as shown in Figure 3.1 [3].

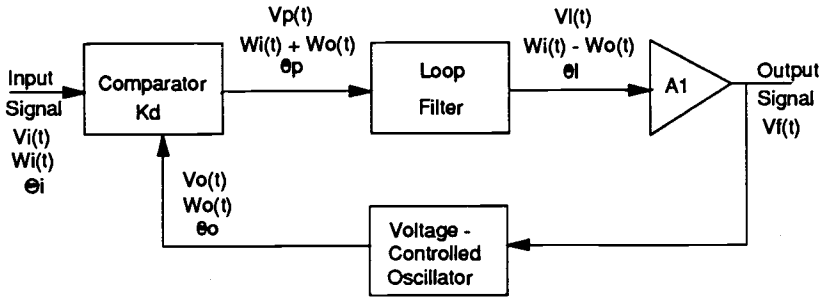

Figure 3.1 PLL model as a feedback system

The initial condition of the PLL is that there is no input signal and the VCO operates at the free running frequency ω_o because there is zero control voltage V_f. The associated VCO output voltage can be described by

$$V_o(t) = V_o \sin(\omega_o t + \theta_o) \qquad (3.1)$$

The input signal eventually appears at the phase comparator input and the signal voltage is represented as

$$V_i(t) = V_i \sin(\omega_i t + \theta_i) \qquad (3.2)$$

The phase comparator is basically an analog multiplier type that outputs the product of the two input signals (one input being the external input signal and the other is the input signal from the voltage-controlled oscillator or VCO) represented by

$$V_p(t) = V_i(t)\, V_o(t) \qquad (3.3)$$

which can also be written as

$$V_p(t) = C_0\, V_i\, V_o\, [(\sin \omega_i t + \theta_i)]\, [\sin (\omega_o t + \theta_o)] \qquad (3.4)$$

where C_0 is a constant and V_p is the phase comparator output voltage.

3.1 PHASE-LOCKED LOOP IN THE UNLOCKED STATE

When the input signal first appears at the PLL, its frequency is usually different from the free running VCO oscillation frequency and the loop is therefore said to be in the "unlocked state". The phase difference between the two inputs to the phase comparator is usually small compared to the frequency difference and is meaningless in mathematical analysis. Equation 3.4 can therefore be rewritten as

$$V_p(t) = \frac{C_o}{2}\, V_i\, V_o\, [\cos(\omega_i - \omega_o)t - \cos(\omega_i + \omega_o)t] \qquad (3.5)$$

The loop filter band edge eliminates the high frequency component and the output voltage can thus be expressed as

$$V_l(t) = C_1\, V_i\, V_o\, [\cos(\omega_i - \omega_o)t] \qquad (3.6)$$

This signal is further amplified by a constant gain factor of A_1 to become

$$V_f(t) = A_1\, C_1\, V_i\, V_o\, [\cos(\omega_i - \omega_o)t] \qquad (3.7)$$

A constantly changing VCO controlled voltage is indicated by the above equation. V_f is a function of the difference of the two input frequencies and a $\Delta\omega$ is the result of this

changing VCO frequency. The delta frequency eventually forces the new VCO frequency to equal the input signal frequency as indicated by the equation

$$\omega_o'(t) = \omega_i(t) = \omega_o(t) + \Delta\omega \qquad (3.8)$$

where ωo' is the free running frequency. This feedback process is regenerative as long as the PLL remains unlocked. The process of changing the oscillation frequency from ω_o' to match with the input frequency ω_i is usually known as the "capture transient" or the "pull-in process" and it is illustrated in Figure 3.2 [4]. Once the pull-in process completes, the PLL is said to then be in the "locked condition".

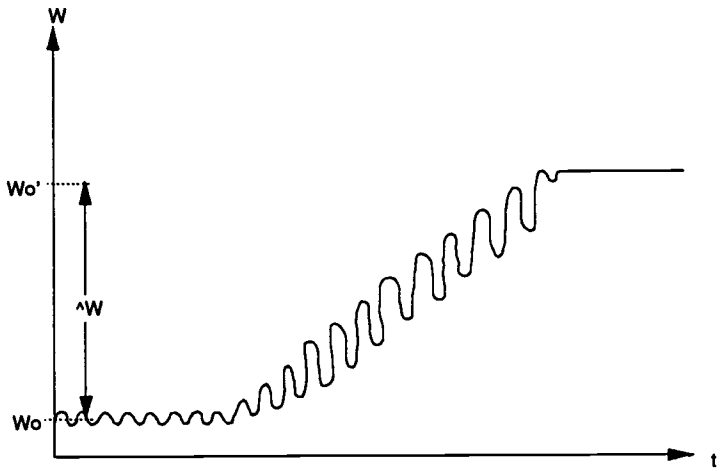

Figure 3.2 Pull-in process or Capture transient

3.2 MODELING A PHASE-LOCKED LOOP IN THE LOCKED CONDITION

After the PLL achieves the locked condition with the input signal, the loop can be modeled and analyzed as a linear feedback system. The block diagram representing the PLL in locked condition is shown in Figure 3.3. The phase error θ_e is the difference

resulting from the subtraction of the phase of the input signal θ_i and the phase of the VCO output θo.

$$\theta_e = \theta_i - \theta_o \qquad (3.9)$$

As can be seen in Figure 3.3, the phase comparator gain is denoted as K_d V/rad, the loop-filter transfer function is F(s), the amplifier gain is A_1, and K_o rad per sec per V and ωo rad is the gain and frequency of the VCO respectively.

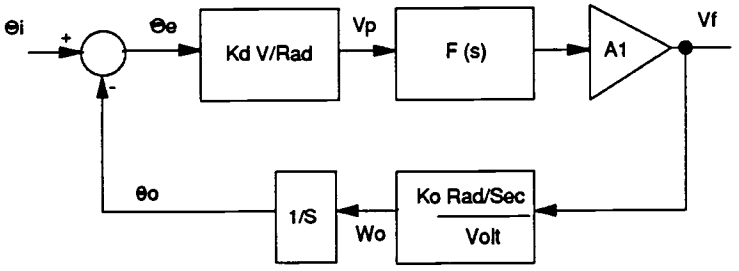

Figure 3.3 System block diagram for PLL in locked condition

The linear relationship between V_p and θ_e is plotted in Figure 3.4, where the phase comparator output signal V_p is the product of K_d and θ_e. This relationship is expressed as

$$V_p = K_d \theta_e \qquad (3.10)$$

where V_p actually contains a DC and a superimposed AC component when the input and VCO's frequencies are matched but with the phase difference. (The transfer function of the VCOs is diagrammed in Figure 3.5.)

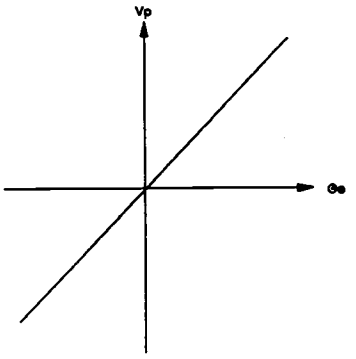

Figure 3.4 The relationship between phase gain and error

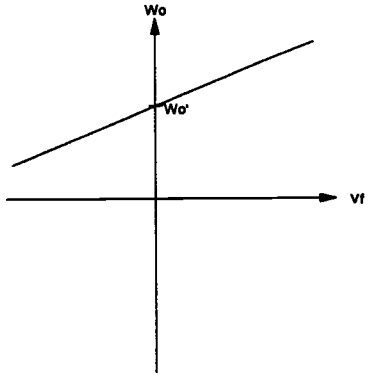

Figure 3.5 VCO oscillation as a function of Vf

The relationship between the oscillation frequency and the control voltage V_f is such that

$$\omega_o = \omega_o' + K_o V_f \qquad (3.11)$$

where ω_o' is the free running frequency with zero control voltage V_f. Futhermore, the closed-loop transfer function can be expressed in Laplace Transform as

$$\frac{V_f}{\theta_i} = K_d F(s) A = \frac{s K_d F(s) A}{s + K_d K_o F(s) A} \qquad (3.12)$$

Since the relationship between frequency and phase is usually expressed as

$$\omega(s) = s\,\theta(s) \qquad (3.13)$$

the transfer loop function can be rewritten in terms of input frequency ω_i as illustrated below

$$\frac{V_f}{\omega_i}(s) = \frac{1}{s}\,\frac{V_f}{\theta_i} = \frac{K_d F(s) A}{s + K_d K_o F(s) A} \qquad (3.14)$$

If the loop filter is removed for analysis purposes, the result is a first-order low pass transfer function which can be written as

$$\frac{V_f}{\omega_i}(s) = \frac{1}{K_o}\,\frac{K_v}{s + K_v} \qquad (3.15)$$

where Kv represents the first-order loop bandwidth and can be expressed as

$$K_v = K_d\, K_o\, A \qquad (3.16)$$

The bode plot and transfer characteristics of this closed- loop locked condition is shown in Figure 3.6 where $1/K_o$ is the low frequency gain. Through further evaluation, it was determined that a loop filter was necessary for the PLL system to allow only the DC and the low frequency component to be fed back to the VCO.

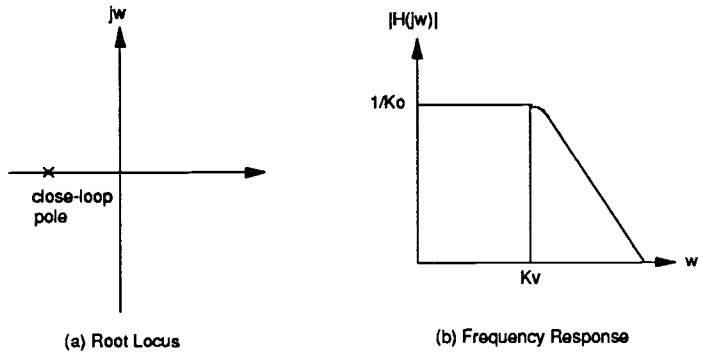

Figure 3.6 Bode plot & frequency response of closed-loop PLL

3.3 LOOP FILTER EFFECT ON PHASE-LOCKED LOOP

The PLL normally contains a first order single-pole low-pass filter or a single-pole low-pass filter with zero added to improve system stability [5]. Occasionally, second or higher order filters are needed and incorporated within the PLL to achieve steeper frequency roll off than the first-order low-pass filter.

3.3.1 FIRST-ORDER LOW-PASS FILTER

The simplest filter is a first-order single-pole low-pass filter with a single resistor and capacitor. The transfer function F(s) is of the form

$$F(s) = \frac{1}{1 + (s / \omega_1)} \qquad (3.17)$$

where ω_1 is the low pass cutoff frequency that can be written as

$$\omega_1 = 1 / (R_1 C_1) \qquad (3.18)$$

. By substituting F(s) in equation 3.17 back to the transfer loop function equation 3.14, the loop becomes a second-order loop system with a transfer characteristic of

$$\frac{V_o}{\omega_i}(s) = \frac{1}{K_o} \frac{K_v \omega_1}{s^2 + s \omega_1 + K_v \omega_1} \qquad (3.19)$$

With a second-order equation in terms of the damping factor ζ and natural frequency ω_n, the denominator of equation 3.19 can be written as

$$D(s) = S^2 + S \omega_1 + K_v \omega_1 = S^2 + 2 \zeta \omega_n S + \omega_n 2 \qquad (3.20)$$

$$\zeta = \frac{1}{2} ((\omega_1 / K_v)^{1/2}) \qquad (3.21)$$

$$\omega_n = (K_v \omega_1)^{1/2} \qquad (3.22)$$

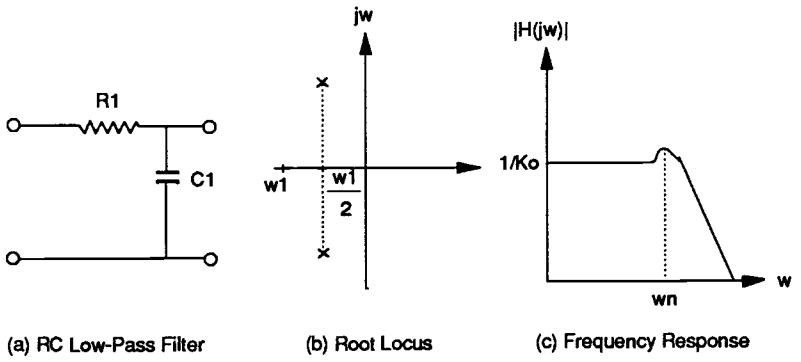

Figure 3.7 Bode plot & freq. response of single-pole filter

The root locus and frequency response plot of the PLL with single-pole filter is shown in Figure 3.7. This second-order frequency response shows a peaking at frequency ω_n which can cause distortion when the PLL is being used in frequency demodulation. A maximally flat response is desired and the damping factor ζ is chosen such that it is equal to the square root of 1/2. By substituting this value into equation 3.22, the cutoff frequency ω_1 can be expressed as

$$\omega_1 = 2\ K_v \qquad (3.23)$$

Subsequently, the -3_{db} cutoff frequency becomes

$$\omega_{-3db} = \omega n = (\frac{1}{2})^{1/2} K_v \qquad (3.24)$$

The above equation indicates that the -3_{db} bandwidth is limited by the PLL's loop gain K_v. Consequently, a system with low loop gain has narrow loop bandwidth and cannot have a wide lock range. Also indicated in equation 3.22 and 3.24 is that a narrow loop bandwidth requires a small ω_1 which would produce an unstable system. This is because the phase shift is 180 degrees at the closed-loop unity gain frequency, as shown in Figure 3.8.

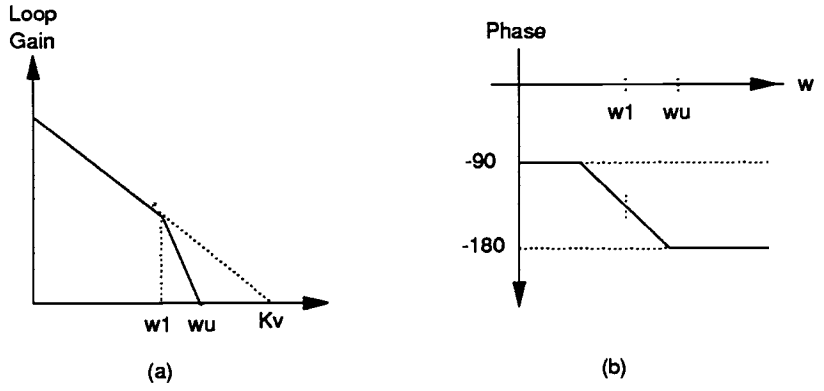

Figure 3.8 Closed-loop system with single pole reponse

The problem of stability can be solved by adding a zero to the single pole filter to improve the loop phase margin, sometimes known as lag lead filter. The root locus and frequency response transfer function for the filter becomes

$$F(s) = \frac{1 + S/\omega_2}{1 + S/\omega_1} \qquad (3.25)$$

$$\omega_1 = \frac{1}{(R_1 + R_2)\,C} \qquad (3.26)$$

$$\omega_2 = 1 / (R_2\,C) \qquad (3.27)$$

The overall loop response for the PLL system can then be expressed as

$$\frac{V_o}{\omega i}(s) = \frac{K_d\,A\,\omega_1\,(1 + S/\omega_2)}{S^2 + S(1 + K_d\,K_o\,A/\omega_2 + K_d\,K_o\,A\,\omega_1)} \qquad (3.28)$$

The frequency and phase response of the lag-lead filter is shown in Figure 3.9 where the phase margin is being moved back up to 90 degrees at the unity gain frequency ω_u. This

improves the phase margin and decreases the sharp peak which occurs at the unity gain frequency, thus increasing the stabilty of the closed-loop system.

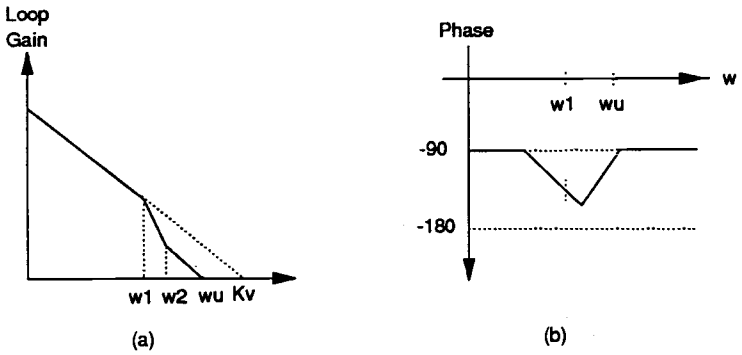

Figure 3.9 Closed-loop system with lag-lead filter response

3.4 LOCK AND CAPTURE RANGE

The capture range (ω_c) is the frequency range over which the PLL can acquire lock with the input signal when initially both signals are oscillating at a different frequency. The lock range (ω_l) is the frequency range over which the PLL can track and remain locked with the input signal once locked condition has been achieved. The frequency of the PLL output voltage V_f transfer characteristics is shown in Figure 3.10.

Initially, the input signal and VCO's free running frequency are different and the loop is not in locked condition. The phase comparator circuit produces the sum and difference components of the two frequencies and the sum frequency component is normally filtered out by the low-pass filter. If the difference component falls outside the loop filter edge area, the loop usually cannot acquire lock because there is zero VCO control voltage present to change the free running frequency. But once the difference between the input signal and

the free running frequency decreases and this component is able to pass through the filter band edge, an output voltage V_f is fedback into the VCO and drives its oscillating frequency toward the input frequency. Subsequently, more of the difference component passes through the loop filter and forces the free running frequency to lock in with the input signal.

This process is nonlinear and the analysis is complicated, but usually this capture range is approximated as

$$\omega_c = K_o K_d A \mid F(j\omega_c)\mid = K_v \mid F(j\omega_c)\mid \qquad (3.29)$$

where $F(j\omega c)$ is the magnitude of the loop filter at frequency ω_c and for the first-order loop filter discussed in the previous section. The magnitude function can be simplified as

$$|F(j\omega_c)| = 1 / \omega\tau \qquad (3.30)$$

and substituting this into equation 3.29, we get

$$\omega_c = (K_v / \tau)^{1/2} \qquad (3.31)$$

For the first-order low-passed filter that has natural frequency as indicated in equation 3.22, the capture range can further be rewritten as

$$\omega_c = \omega_n \qquad (3.32)$$

This equation indicates that the capture range is as large as the natural frequency ω_n and the natural frequency can be chosen according to the low-passed filter RC values.

Once the PLL is locked with the input signal, the different frequency between the two input components to the phase comparator is zero and only a DC voltage appears at the output of the phase comparator. The magnitude of this DC component is proportional to the phase difference of the two input frequencies. The maximum phase comparator output voltage can be written as

$$V_{p\,max} = - K_d (\pi / 2) \qquad (3.33)$$

This voltage is being amplified and fed into the VCO input to produce a delta free running frequency $\Delta\omega_o$ written as

$$\Delta\omega_o = K_d K_o A (\pi / 2) = K_v (\pi / 2) \qquad (3.34)$$

This is the maximum frequency that can be produced by the maximum phase error. The frequency range over which the loop can remain locked with the input signal is known as the "lock range" and is equal to this change in frequency. The lock range can be written as

$$\omega_l = K_v (\pi / 2) \qquad (3.35)$$

The lock range is the result of the DC component and that this is always larger than the capture range, as shown in Figure 3.10.

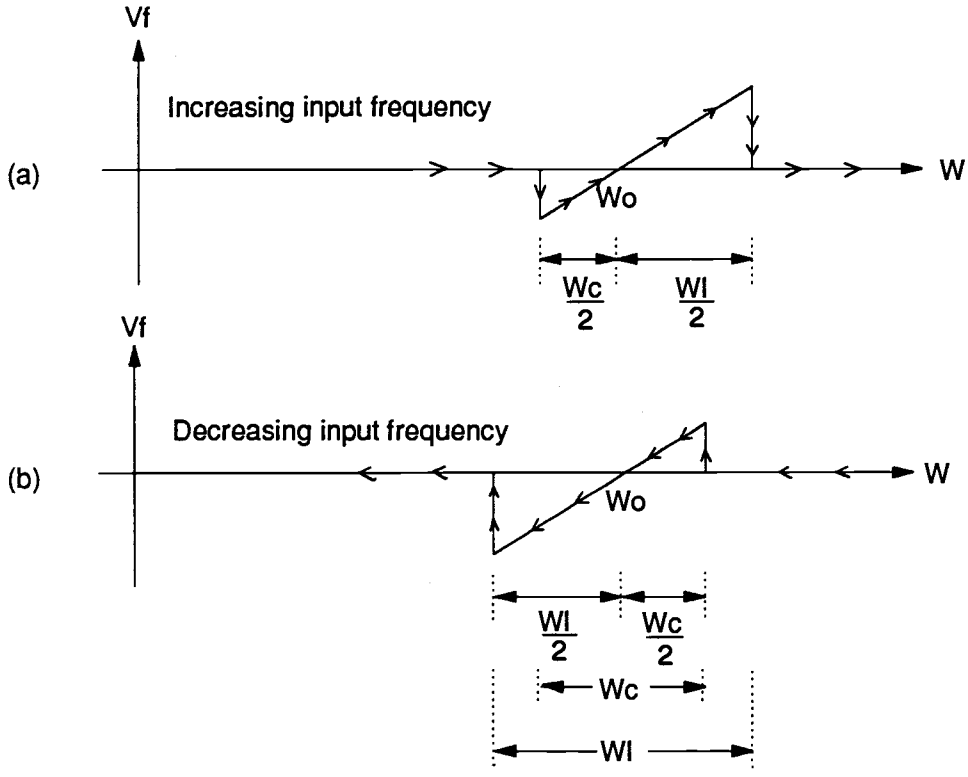

Figure 3.10 Capture and Lock range vs Vf characteristic

CHAPTER 4

CIRCUIT DESCRIPTION AND DESIGN PARAMETERS

The CMOS Phase-Locked Loop (PLL) designed in this project is a self- contained device with an adaptable filter and frequency range of up to 1000KHz. It combines an internal resistor with an external capacitor to generate a first-order low-pass filter. The PLL also uses an external resistor and capacitor to program the free-running center frequency for the VCO.

The PLL system is comprised of a phase comparator, an amplifier, a loop filter, a voltage-controlled oscillator and a bias voltage generator as shown in Figure 4.1. The phase comparator is an analog multiplier circuit type and the loop filter used is a first-order single-pole low-pass filter. The VCO is a combination of a current source and of a Schmitt Trigger. The amplifier converts the differential output voltage from the phase comparator

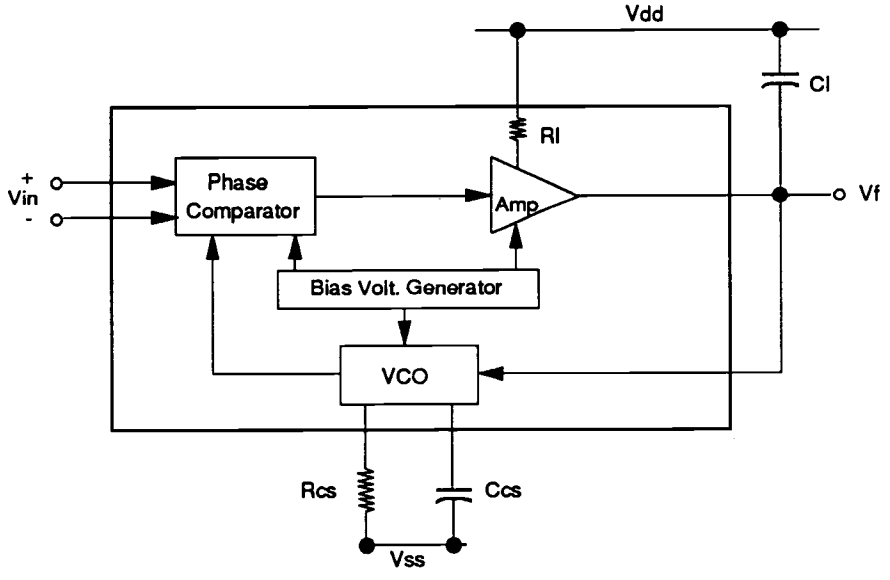

Figure 4.1 CMOS PLL block diagram

to a single ended output and the bias voltage generator provides all the DC bias voltages and bias currents for all the blocks.

The basic functionality of this PLL device begins with the free running center frequency of the system. By changing the value of the externally connected resistor R_{cs} and capacitor C_{cs} (in essence choosing the RC value), the center frequency of the VCO can vary from the hundreds to thousands of Hz range.

The phase comparator accepts a 4 V_{p-p} input signal and mixes it with the VCO's square output signal and the output is then amplified by an internal amplifier. A built-in resistor R_l in the internal amplifier circuit is used in conjunction with the external RC or active filter network as the PLL's loop filter. A single pole loop filter is shown in Figure 4.1 where the capacitor C_l is connected in parallel to R_l. Proper selection of the loop filter value determines the filter bandwidth and capture range for the PLL system.

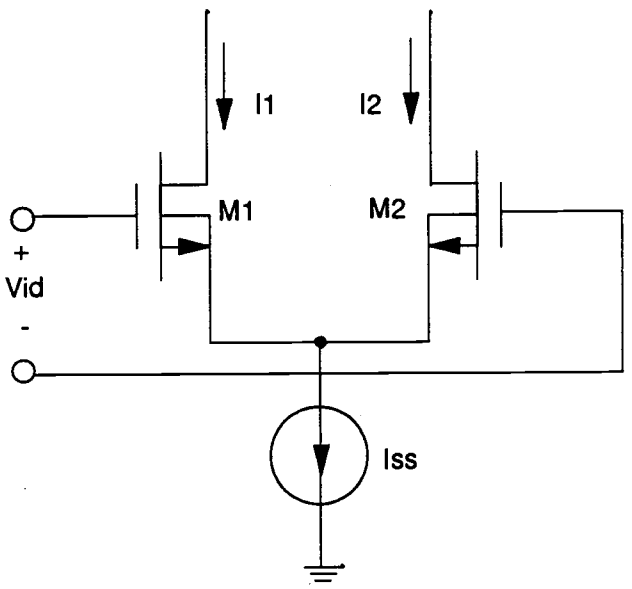

Figure 4.2 Emitter-Coupler pair

The demodulated output voltage V_f will then be fed into the voltage-controlled oscillator as the VCO's control voltage. Along with the resistor R_{cs}, this control voltage generates a bias current that charges and discharges the capacitor C_{cs} to generate the oscillating center frequency for the PLL.

4.1 PHASE COMPARATOR

The phase comparator is often called either the phase detector, mixer, or the balanced multiplier. This signal processing circuit is basically a four-quadrant analog multiplier that produces an output proportional to two analog inputs when these input signals are relatively small. But in communication systems, the phase comparator is modified to accomplish the multiplication of a continuously varying signal by a square wave. The large amplitude of the square wave input causes the devices in the multiplier circuit to be fully on or fully off. It also causes the output voltage of the circuit produced by the small, continuously varying signal to be alternately multiplied by +1 and -1 and therefore the circuit is appropriately called the "balanced multipler".

4.1.1 Gilbert Multipling Cell

The simple multipling circuit is made up of an emitter-coupler pair as shown in Figure 4.2 [6]. The NMOS transistors M_1 and M_2 are biased in the saturation region where the drain to source current I_{ds} can be modeled as

$$I_{ds} = K (V_{gs} - V_t)^2 \qquad (4.1)$$

where V_{gs} is the gate source voltage, V_t is the transistor threshold voltage and K is the expression for the transconductance K'. Therefore, the width and length of the MOS transistor is expressed as

$$K = \frac{K'}{2}\frac{W}{L} \qquad (4.2)$$

The relationship between the output currents and the differential input voltage is expressed as

$$V_{id} = \left(\frac{I_1}{K}\right)^{1/2} - \left(\frac{I_2}{K}\right)^{1/2} \qquad (4.3)$$

Therefore, the corresponding output currents are written in terms of the differential input voltage and parameter K such that

$$I_1 = I_2 + 2\left(K I_2\right)^{1/2} + K V_{id}\,2 \qquad (4.4)$$

$$I_2 = I_1 - 2\left(K I_1\right)^{1/2} + K V_{id}^{\,2} \qquad (4.5)$$

Furthermore, the tail current Iss is the summation of the output current and can be rewritten in terms of the differential input voltage and the tail current.

$$I_1 = \frac{I_{ss}}{2} + \frac{K V_{id}}{2}\left(\frac{2 I_{ss}}{K} - V_{id}^{\,2}\right)^{1/2} \qquad (4.6)$$

$$I_2 = \frac{I_{ss}}{2} - \frac{K V_{id}}{2}\left(\frac{2 I_{ss}}{K} - V_{id}^{\,2}\right)^{1/2} \qquad (4.7)$$

Consequently, the differential output current ΔI can be expressed as

$$\Delta I = I_1 - I_2 = K V_{id}\left(\frac{2 I_{ss}}{K} - V_{id}^{\,2}\right)^{1/2} \qquad (4.8)$$

This equation indicates that the MOS emitter-coupler pair exhibits limited characteristics of an analog multiplier when the differential input voltage is less than the absolute

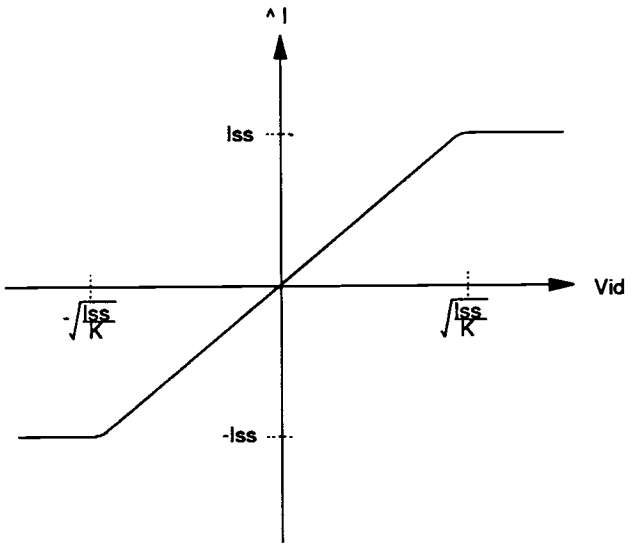

Figure 4.3 The limited multiplication characteristic

value of the tail current over K. This relationship is shown in Figure 4.3 and the equation can be expressed as

$$Vid \leq \left| \left(\frac{I_{ss}}{K} \right)^{1/2} \right| \qquad (4.9)$$

Therefore, when the differential voltage V_{id} meets the absolute value of tail current over K condition, the differential output current can then be approximated as

$$\Delta I = K\, Vid \left(\frac{2\, I_{ss}}{K} \right)^{1/2} \qquad (4.10)$$

The emitter-coupler pair circuit is only considered as a two quadrant multiplier and therefore a different circuit configuration known as the Gilbert Multiplier Cell is used to provide four quadrant multiplication. The Gilbert Cell is shown in Figure 4.4 where I_7 and I_8 are the output currents, I_1 - I_6 are the corresponding current for the MOS transistors M_1

- M_6 and V_x and V_y are the two input voltages. The differential output current ΔI_o for this MOS Gilbert Cell is

$$\Delta I_o = I_7 - I_8 = (I_3 - I_4) - (I_6 - I_5) \tag{4.11}$$

The difference between current I_3 and I_4, I_5 and I_6 can be further expressed as the emitter-coupler pair current I_1 and I_2 which is the function of input voltage V_x and V_y such that

$$I_3 - I_4 = K V_x \left(\frac{2 I_1}{K} - V_{x2} \right)^{1/2} \tag{4.12}$$

$$I_6 - I_5 = K V_x \left(\frac{2 I_2}{K} - V_{x2} \right)^{1/2} \tag{4.13}$$

$$I_1 = \frac{I_{ss}}{2} + \frac{K V_y}{2} \left(\frac{2 I_{ss}}{K} - V_{y2} \right)^{1/2} \tag{4.14}$$

$$I_2 = \frac{I_{ss}}{2} - \frac{K V_y}{2} \left(\frac{2 I_{ss}}{K} - V_{y2} \right)^{1/2} \tag{4.15}$$

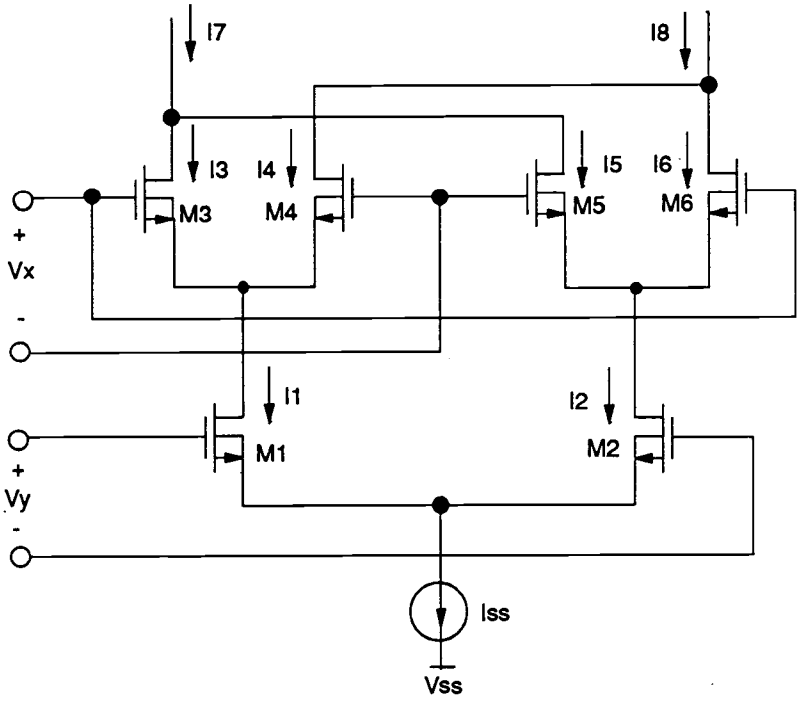

Figure 4.4 CMOS Gilbert multiplier cell

When all these equations are substituted back into equation 4.11, the result becomes

$$\Delta I_o = K V_x\{ [((\frac{I_{ss}}{K} - \frac{V_{y2}}{2})^{1/2} + \frac{V_y}{2^{1/2}})^2 - V_{x2}]^{1/2} - [((\frac{I_{ss}}{K} - \frac{V_{y2}}{2})^{1/2} - \frac{V_y}{2^{1/2}})^2 - V_x^2]^{1/2}\} \quad (4.16)$$

The differential output current seems nonlinear at first glance, but if the input voltages V_x and V_y are considered to be small, Equation 4.16 can be approximated to

$$\Delta I_o = (2)^{1/2} \quad K V_x V_y \quad (4.17)$$

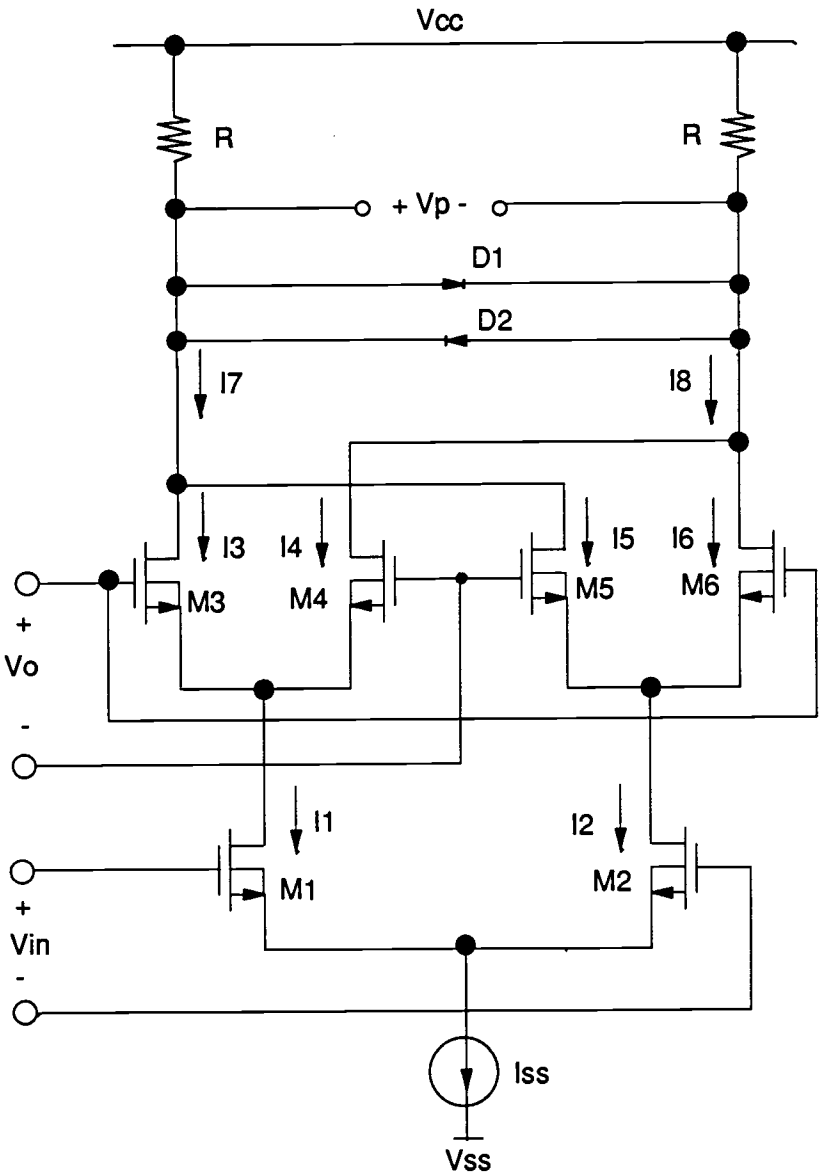

Figure 4.5 CMOS phase comparator circuit

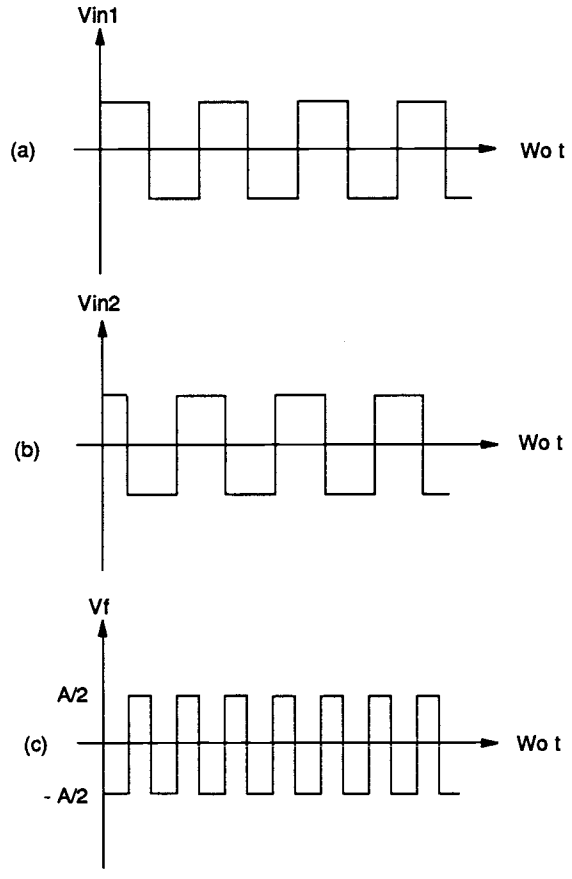

Figure 4.6 Phase comparator input and output waveform

In general, the approximate input range of V_x is assumed to be less than the absolute value of 300mV and V_y is the absolute value of 1.0 V for equation 4.17 to hold true. The Gilbert Cell is usually modified to allow large input voltage multiplication in many applications. But in most communication systems where a large square wave input multiplication is required, the Gilbert Cell is sufficient to be used as a phase comparator.

4.1.2 Phase Comparator Circuit

A CMOS phase comparator circuit is shown in Figure 4.5 where the Gilbert Multipler Cell consists of transistors M_1 - M_6. The diodes D_1 and D_2 are used to limit the differential output amplitude to a two diode voltage drop of approximately 1.5V. With the

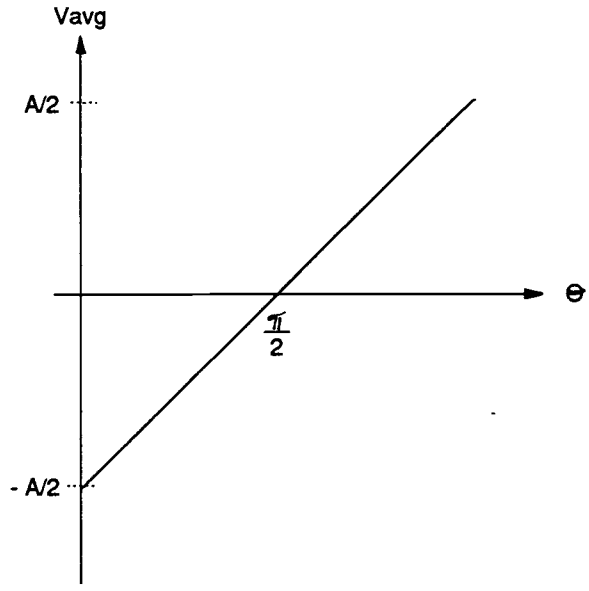

Figure 4.7 Average DC voltage vs phase difference

presence of these diodes, a smaller input signal amplitude is required to cause the output waveform to swing from high to low and visa versa.

The input waveforms are shown in Figures 4.6a and b. Note that they are equal in frequency but differ in phase. This is similar to the condition when the input frequency is drifting away from the VCO signal after the PLL has acquired locked condition. The slight change in frequency is shown as a phase difference between the two signals. The VCO signal is represented by the waveform V_{in1}, the input signal is shown as V_{in2} and therefore the large signal pulse turns two of the four transistors on and off (in the cross-coupled pair) in an alternating fashion. The resulting differential output waveform shown in Figure 4.6c consists of a component that is twice the input frequency and a DC voltage. The high frequency component is usually filtered by the loop filter and only the DC component is passed through to the VCO as the controlled voltage. This average DC voltage output can be represented analytically as

$$V_{avg} = \frac{1}{2}\int_{0}^{2\pi} V_o(t)\, d(\omega_o \tau) = \frac{A}{2}\left(\frac{2\theta}{\pi} - 1\right) \qquad (4.18)$$

In the phase comparator circuit where the diode connecting transistors limits the different output swing, amplitude A is the voltage of a two diode drop and is approximately equal to 1.5V. Equation 4.18 can therefore be rewritten as

$$Vavg = \frac{1.5}{\pi}\left(\theta - \frac{\pi}{2}\right) = Kd\left(\theta - \frac{\pi}{2}\right) \qquad (4.19)$$

and the phase comparator conversion gain factor Kd for this circuit has the value of

$$Kd = \frac{1.5}{\pi}\left(\frac{V}{rad}\right) \qquad (4.20)$$

The average DC voltage as a function of the phase difference between the two input signals is plotted in Figure 4.7, and is zero when the phases of the two input signals are 90 degrees apart.

4.2 AMPLIFIER AND LOOP FILTER

A differential amplifier and an internal resistor combined with an external capacitor as shown in Figure 4.8, provides the loop filtering and amplification necessary for the CMOS PLL system. The differential amplifier which provides the amplification for this system, consists of several components described as follows. Four transistors, identified in Figure 4.8 as M_{13} - M_{16}, provide a large signal gain from the output of phase comparator. These transistors can be further divided into the differential input pair, M_{13} and M_{14}, and the set of transistors which provide the first stage gain, M15 and M16. Providing a constant current souce for the above described amplifier, the bias currents, $Ibias_1$-$Ibias_3$, are generated from the bias voltage for the CMOS PLL. Therefore, the overall large signal gain A_1 is approximately equal to two for this amplifier which gives a $3V_{p-p}$ output signal waveform when the input signal is supplied by the phase comparator output.

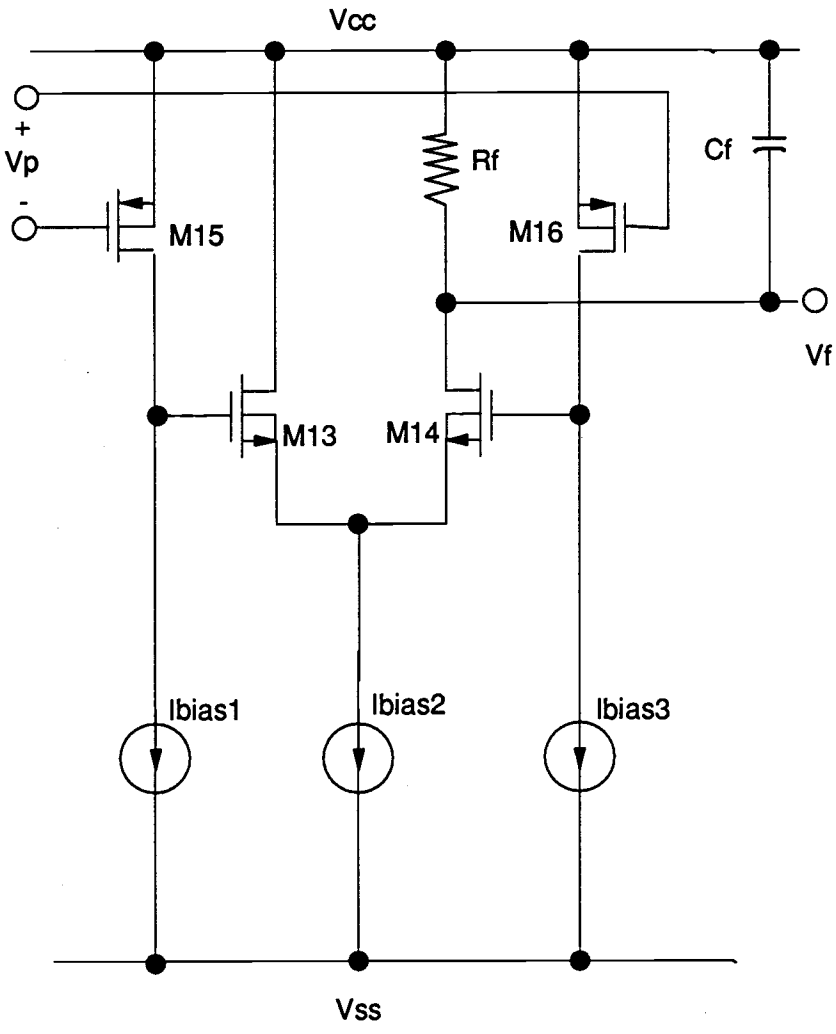

Figure 4.8 CMOS amplifier and loop filter

The loop filter, as mentioned above, consists of an internal 4K ohm resistor R_f and an external capacitor C_f. Thes two devices combine to form a first-order low-pass loop filter for the CMOS PLL system. Note that with the capacitor C_f placed externally, it can be choosen to provide the desired cutoff frequency for the close-loop system.

4.3 VOLTAGE - CONTROLLED OSCILLATION

The CMOS voltage-controlled oscillator shown in Figure 4.9 make use of a Schmitt Trigger and a current source circuit to provide oscillation. The control voltage from the output of the amplifier as described in Section 4.2, along with an external resistor R_{cs}, varies the amount of current which can flow through the current source to charge and discharge an external capacitor C_{cs}. This charging and discharging turns the Schmitt Trigger on and off, respectively.

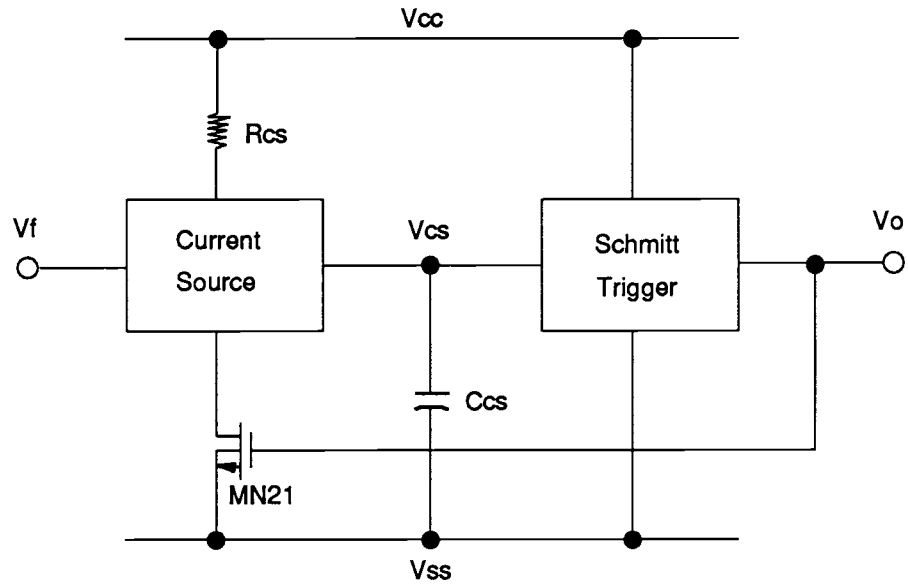

Figure 4.9 VCO block diagram

Initially, the output of the Schmitt Trigger is low, transistor MC_{21} is shut off and the current source charges up capacitor C_{cs}. The corresponding rise in the capacitor voltage turns the Schmitt Trigger off hard and therefore the output voltage goes high. This voltage is then fed back and causes the transistor MC_{21} to turn on. This allows capacitor C_{cs} to discharge voltage which subsequently turns the Schmitt Trigger back on strongly, which in

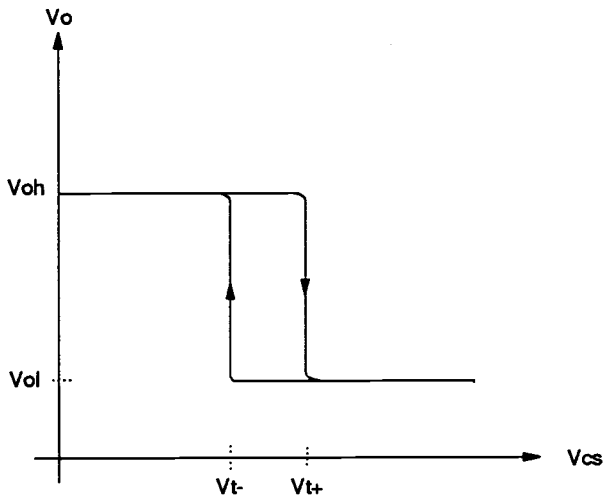

Figure 4.10 Schmitt Trigger transfer function

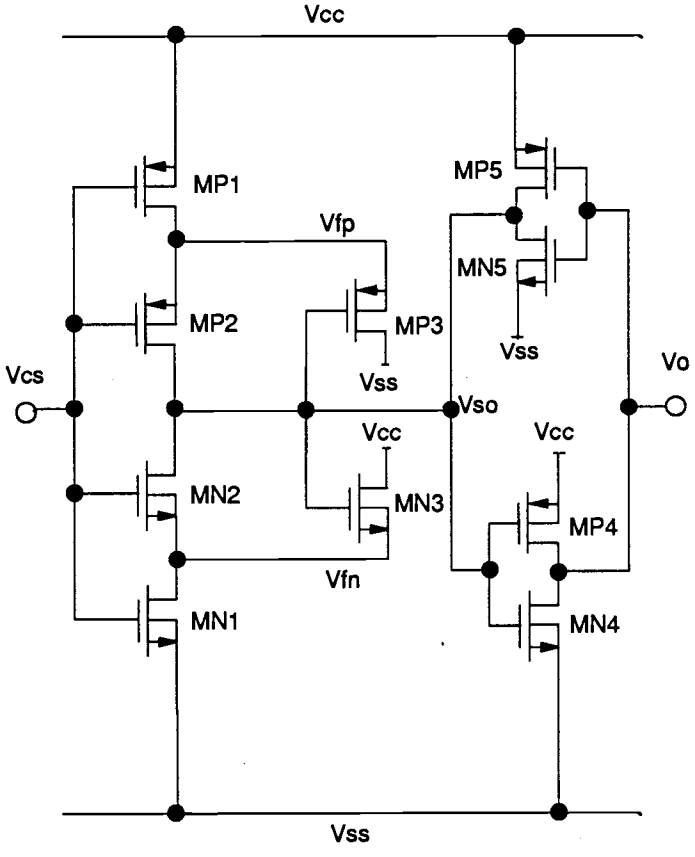

Figure 4.11 CMOS Schmitt Trigger circuit

turn, again shuts off MC_{21}. This cycle of turning the Schmitt Trigger on and off results in a square-wave output V_o which becomes the VCO's oscillating frequency.

4.3.1 Schmitt Trigger

The CMOS Schmitt Trigger has an input and output characteristic which exhibits hysteresis, as seen in the plotted diagram labelled Figure 4.10 [7,8]. In this diagram, the positive and negative trip points are denoted as V_{t+} and V_{t-} respectively. The value of the positive trip voltage V_{t+}, corresponds to the size of the NMOS transistor, and conversely, the negative trip voltage V_{t-} is determined by the size of the PMOS transistor.

The Schmitt Trigger schematic is shown in Figure 4.11, and along with the two latching invertors consist of transistors MN_5-MN_6 and MP_5-MP_6. As described above, the size of the NMOS transistor MN_1-MN_3 determined the value of V_{t+} and the size of the PMOS transistors MP_1-MP_3 contribute to the value of V_{t-}.

The circuit model shown in Figure 4.12 is used to find the positive trip point valueV_{t+}. At the instance right before the input voltage reaches V_{t+}, transistor MN_2 is off and MN_1 and MN_3 are operating in the saturation region. Consequently, the node voltage V_{fn}, at this instant, is expressed as

$$V_{fn} = V_{in} - V_{tn} \tag{4.21}$$

Transistor MN_3 is operating as an enhancement load in the saturated region and transistor MN_1 is also operating in saturation region. Consequently, the two currents I_{ds1} and I_{ds3} are equal and written as

$$\frac{kn'}{2}\left(\frac{W}{L}\right)_3 (V_{gs3} - V_{tn})^2 = \frac{Kn'}{2}\left(\frac{W}{L}\right)_1 (V_{gs1} - V_{tn})^2 \tag{4.22}$$

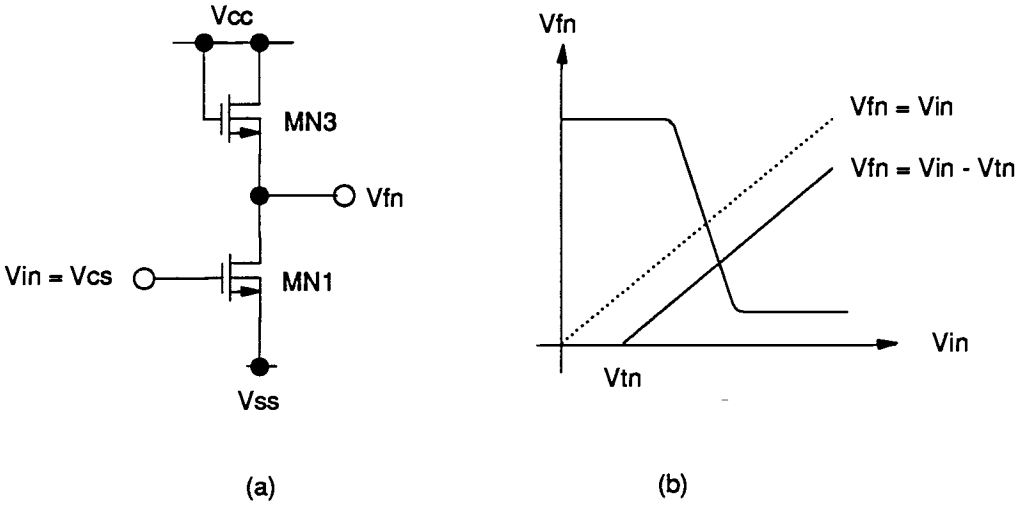

Figure 4.12 Model used for Vt+ calculation

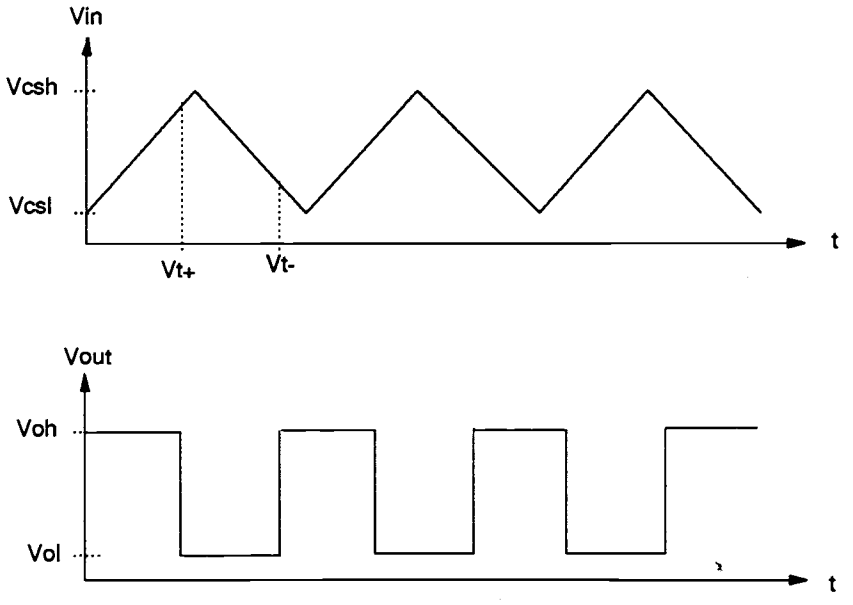

Figure 4.13 Schmitt Trigger input and output relationship

In the above equation, the NMOS threshold voltage is V_{tn}, the transconductance is K_n' and V_{gs} is the transistor gate source voltage. Since the input voltage is related to V_{fn} as indicated in equation 4.21, the equation above can be rewritten as

$$V_{cc} - V_{fn} - V_{tn} = (V_{in} - V_{tn}) (\beta)^{1/2} \qquad (4.23)$$

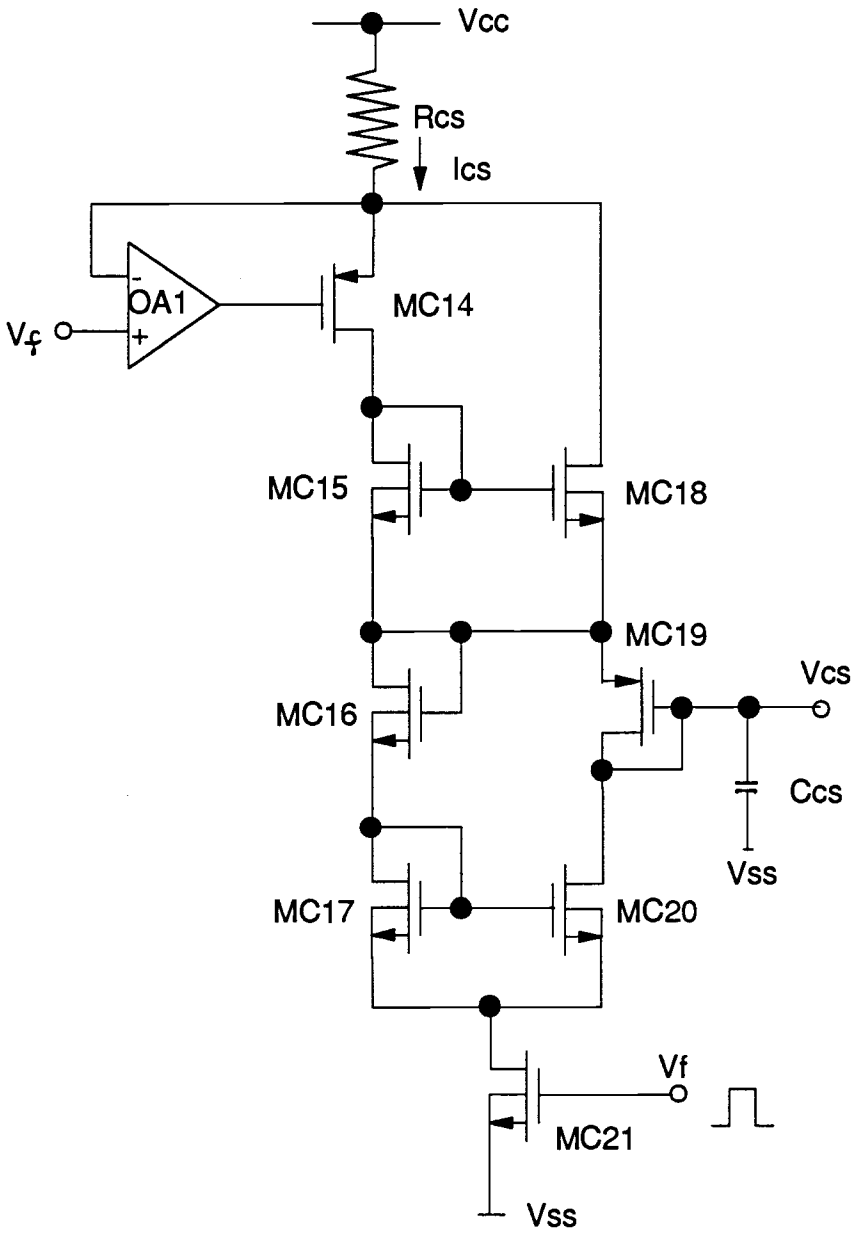

Figure 4.14 CMOS current source circuit

Note that β is the transistors size ratio as indicated in the following equation

$$\beta = \frac{(W/L)_{MN1}}{(W/L)_{MN3}} \qquad (4.24)$$

Subsequently, the input voltage trip point V_{t+} is derived from equation 4.23 as

$$V_{t+} = V_{in} = \frac{V_{cc} + V_{tn}(\beta)^{1/2}}{1 + (\beta)^{1/2}} \qquad (4.25)$$

From the known values of the supply voltage Vcc, the transistor threshold voltage Vtn, and by properly choosing the ratio of transistor width and length for MN1 and MN3, the corresponding trip point voltage Vt+ can then be found . Similarly, the negative trip point voltage V_{t-} is obtained by choosing the PMOS transistor sizes accordingly.

Figure 4.13 shows the Schmitt Trigger circuit input and output relationship. The output signal is shaped like a square waveform because of the hard turn on and turn off characteristic of the Schmitt Trigger. The input signal to this circuit is actually the output from the current source which charges and discharges the externally connected capacitor.

4.3.2 Current Source

The current source circuit of the voltage-controlled oscillator circuit is shown in Figure 4.14. It combines an operational amplifier and an externally connected resistor R_{cs} to generate current Ics which charges and discharges an externally connected capacitor C_{cs} [9]. The ability to choose the value of R_{cs} and C_{cs} enables the VCO's free running oscillation frequency to be varied to demodulate the input signal with various carrier frequencies.

As diagrammed in Figure 4.14, the operational OA1, the transistor MC_{14} and the resistor R_{cs} together generate a bias charging and discharging current Ics. This bias current is a function of the VCO control voltage V_f which can be written as

$$I_{cs} = \frac{V_{cc} - V_f}{R_{cs}} \qquad (4.26)$$

The above equation indicates that the currrent source generated is proportional to the VCO's control voltage V_f. This charging and discharging of capacitor C_{cs} depends on the clock pulse at the gate input of transistor MC_{21}. This transistor resembles an open circuit when the pulse voltage V_f is low and current I_{cs} charges up capacitor C_{cs} through transistors MC_{15} - MC_{18}. The voltage level V_{cs} stored at the capacitor rises and eventually reaches the Schmitt Trigger positive trip point voltage V_{t+}. This in turn switches the Schmitt Trigger circuit output voltage from low to high which then turns on and short circuits the transistor MC_{21}. The process repeats itself and the output of the Schmitt Trigger subsequently becomes the oscillation frequency.

When the gate voltage at transistor MC_{21} is high, the transistor resembles an open circuit. The capacitor voltage Vcs at that instance is low and the bias current Ics flows through transistors MC_{14}-MC_{15} and MC_{18}-MC_{19} to charge up capacitor C_{cs}. This capacitor voltage rises and switches the Schmitt Trigger output to the high level and this output then turns on transistor MC_{21}. The bias current Ics subsequently flows through MC_{14} -MC_{17} and sinks the same amount of current from the capacitor C_{cs} through transistor MC_{20} because of the current mirror configuration. This bias current Ics is related to the free running oscillating frequency as

$$f_o = \frac{I_{cs}}{C_{cs}\,\Delta V_{cs}} = \frac{V_{cc} - V_f}{R_{cs}\,C_{cs}\,\Delta V_{cs}} \qquad (4.27)$$

The voltage V_{cc} - V_f at the free running frequency is biased at around 1.5V and the voltage swing at capacitor C_{cs} is the difference between the trip voltages for the Schmitt Trigger and is equal to 2V. The free running frequency can then further be rewritten as

$$f_o = \frac{1.5}{2 R_{cs} C_{cs}} \qquad (4.28)$$

If the resistor Rcs is choosen to be fixed at 4K ohm, a linear relationship between the free running oscillating frequency and capacitor values exists as shown in Figure 4.15. By choosing the capacitor value differently, the PLL can be programmed to demodulate the input signal with various carrier frequencies of up to or above 500K Hz by adjusting the VCO's free running frequency.

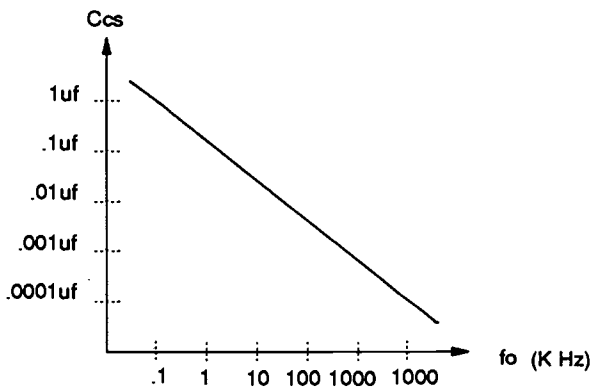

Figure 4.15 The linear relationship between fo and Ccs

The voltage-controlled oscillator conversion gain, Ko, can be expressed (in terms of the change in frequency) as the function of the change in the controlled voltage. It can be written as

$$K_O = \frac{\partial \omega}{\partial v_f} = 2\pi \frac{\partial f}{\partial I_{cs}} \frac{\partial I_{cs}}{\partial v_f} \qquad (4.29)$$

The capacitor charging current related to the controlled-voltage can then be expressed as a small signal current gain

$$\frac{\partial I_{cs}}{\partial v_f} = \frac{i_o}{v_f} = \frac{gm\,(MC14)}{1 + gm\,(MC14)\,R_{cs}} = .000165 \qquad (4.30)$$

The VCO conversion gain can be written in terms of the charging currents I_o at the free running frequency f_o. Equation 4.29 can thus be rewritten as

$$K_O = 2\pi \frac{f_o}{I_o} (.000165) = 2.76\, f_o \qquad (4.31)$$

Consequently, the overall loop gain of the Phase-Locked Loop is expressed as

$$K_v = K_d\, A\, K_O = 2.64\, f_o \text{ rad/sec} \qquad (4.32)$$

The capture range and the lock range of the phase-locked loop can then be found once the loop gain value is known. For the second-order loop, the capture range is 1.87 times the free running frequency and the lock range is 4.15 times the free running oscillating frequency as indicated by equation 3.32 and equation 3.35.

CHAPTER 5

CIRCUIT SIMULATION

The CMOS Phase-Locked Loop circuit is divided into four major blocks. The first block is the phase comparator that accepts input from the VCO and the external input signal. The second block includes the amplifier and loop filter which combines the loop filtering function along with the amplification of the phase comparator output. The voltage controlled oscillator, which is a combination of a current source circuit and a Schmitt Trigger, is the third block. Lastly, the fourth block is a bias voltage generator that provides all the neccessary bias voltages and currents for the various circuit blocks.

5.1 CIRCUIT SIMULATION RESULTS

As diagrammed in Figure 5.1, the phase comparator circuit is described as follows. The input signal which appears across node 2 and node 3 is of the magnitude $2V_{p\text{-}p}$, where the voltage at node 2 is DC biased externally at approximately 4 Volts. The DC voltage level at node 12 is the output waveform from the VCO with a magnitude of $4V_{p\text{-}p}$, and node 16's DC voltage level is biased at 5 volts. Transistors M_1-M_6 are for the Gilbert multipling cell and all have the same transistor width and length. M_9-M_{10} are load transistors for the Gilbert multipling cell. The diode connecting transistors are labelled as M_7 and M_8 which limit the differential output swings of the multiplier circuit to approximately 1.5 volts. Note that the transistor sizes for the phase comparator are shown in Table 5.1 and the input and output relationship from the SPICE simulations are shown in Figure 5.2.

Shown in Figure 5.3 is the amplifier circuit for the PLL system and includes the following devices. The resistor labelled Rf is set equal 4K ohm and can be used in conjunction with a single externally connected capacitor as a single-pole loop filter or it can be used as part of any higher order passive or active filter network for loop filtering. Transistors M_{17}-M_{20}

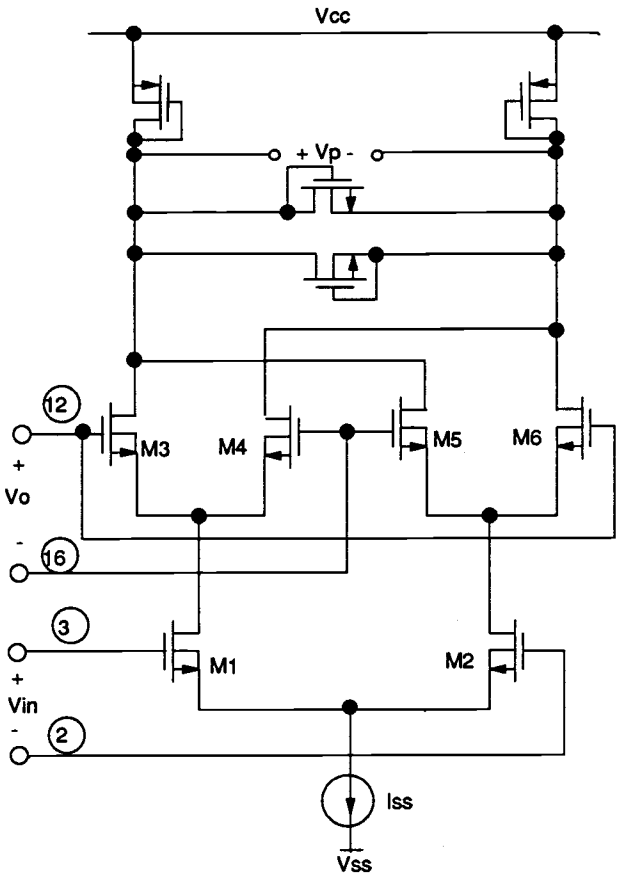

Figure 5.1 Phase comparator circuit

TRANSISTOR	W (um)	L (um)
M1	120	5
M2	120	5
M3	120	5
M4	120	5
M5	120	5
M6	120	5
M7	25	5
M8	25	5
M9	80	5
M10	80	5
M13	40	5

Table 5.1 Transistor sizes for phase comparator circuit

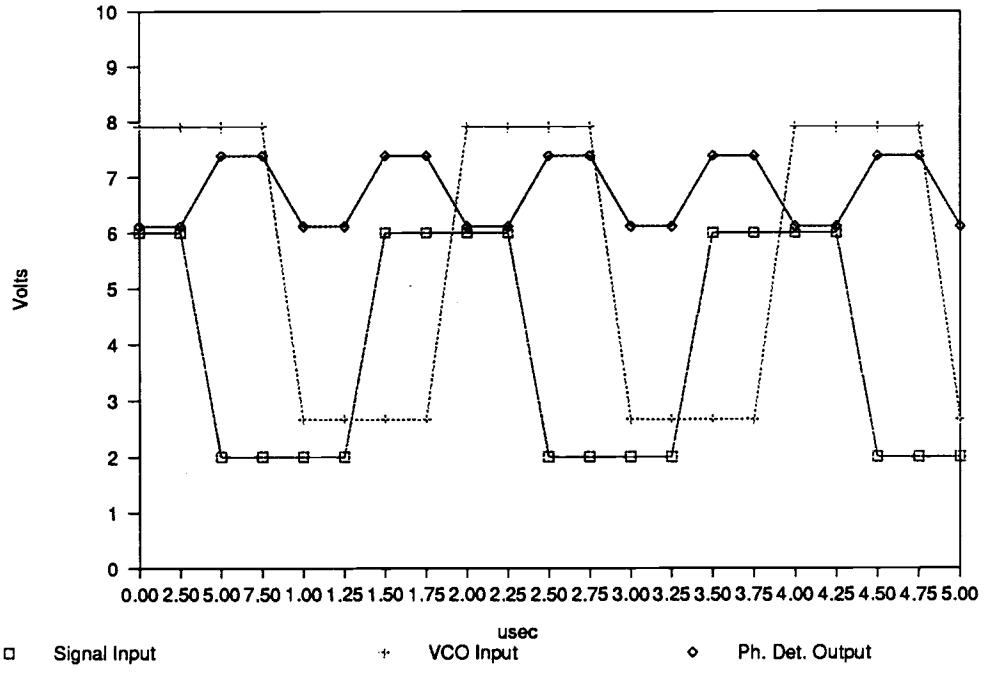

Figure 5.2 SPICE simulation output for phase comparator

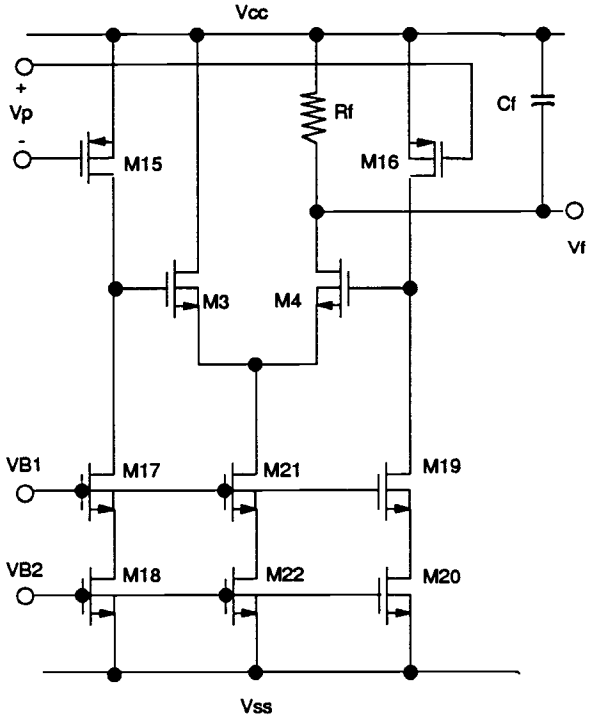

Figure 5.3 Amplifier circuit

provides the bias current for the amplifier and the bias voltages V_{b1} and V_{b2} come from the bias voltage generator circuit. The input voltage V_o is the differential output voltage from the phase comparator. Transistors M_{13}-M_{16} convert and amplify the differential input signal to a single end output V_f. This output voltage has a DC level of 8.5V and has a maximum voltage swing of $3V_{p\text{-}p}$. The SPICE simulation of the amplifier input and output waveforms are shown in Figure 5.4 and the transistor sizes are listed in Table 5.2.

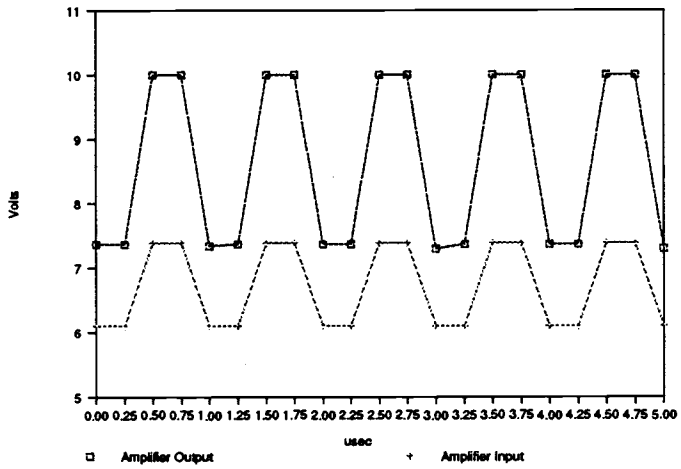

Figure 5.4 SPICE simulation output for amplifier circuit

TRANSISTOR	W (um)	L (um)
M13	80	5
M14	80	5
M15	80	5
M16	80	5
M17	18	5
M18	18	5
M19	18	5
M20	18	5
M21	18	5
M22	18	5
Rf	4 K ohm	

Table 5.2 Transistor sizes for amplifier circuit

The voltage -controlled oscillator circuit is a combination of a current source and Schmitt Trigger as shown in Figure 5.5. The VCO control voltage V_f is the output from the loop filter and is of the magnitude range from 7V to less than 10V. This voltage appears at the operational amplifier input and forces the voltage at node 83 to follow and equal this control voltage value. This effect is due to the fact that the amplifier OA1 and transistor MC_{14}, along with resistor R_{cs}, is connected in the unity gain configuration. The bias current I_{cs} generated by this configuration is the direct result of the control voltage V_f. The bias current ranges depend on the value of V_f and functions as a charging and discharging current to the externally connected capacitor C_{cs}. Transistor MC_{21}, which is twice the size of the current mirror transistor pair of MC_{19}-MC_{20}, an equal amount of bias current I_{cs} to flow through

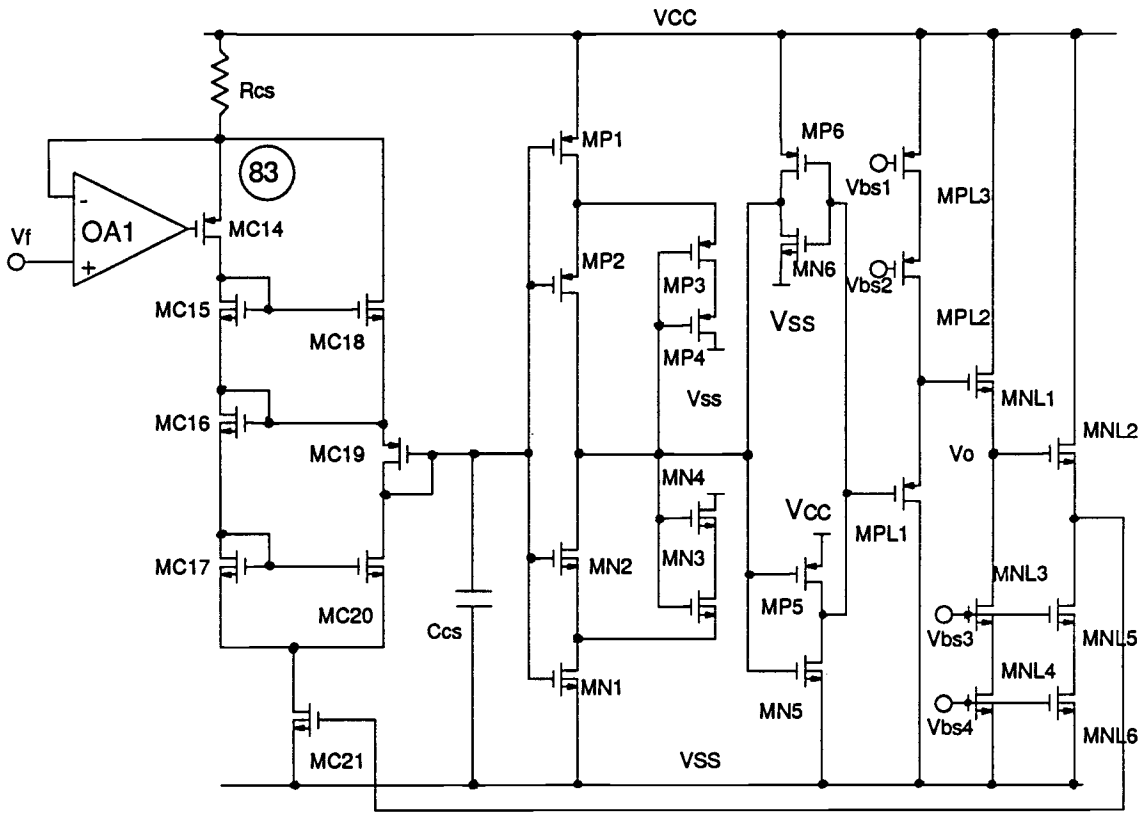

Figure 5.5 Voltage Controlled-Oscillator circuit

the current mirror pair. The current source circuit transistor sizes for this circuit are shown in Table 5.3.

TRANSISTOR	W (um)	L (um)
MC14	75	4
MC15	75	4
MC16	75	4
MC17	75	4
MC18	75	4
MC19	75	4
MC20	75	4
MC21	150	4

Table 5.3 Transistor sizes for the current source circuit

The schematic for the operational amplifier OA1 is shown in Figure 5.6. This is a single gain stage amplifier with NMOS transistors MA_1 and MA_2 as the input pair and both MA_{3A} and MA_{3B} providing the bias tail current. The NMOS transistors are used for input and tail current biasing because this configuration allows the positive output range to swing up to V_{cc} - V_{dsat} of transistor MA_{11}. The maximun output swing is important on the positive side because the operational amplifier has to operate with the output as close to V_{cc} as possible in order to provide the bias current I_{cs} when the control voltage value is kept close to V_{cc}. Transistors MA_{13}-MA_{18} provide either bias currents or bias voltage functions for the amplifier and MA_6-MA_9 are cascade transistors to provide a higher gain for the amplifier. Along with MA_{3A} and MA_{3B}, these transistors also serve to limit the channel length modulation of the current source by limiting the V_{ds} voltage swing for the output transistors.

A compensation capacitor C_1 of 3pf is placed at the output of the amplifier to ensure amplifier stability in the unity gain operation. Figure 5.7 shows the SPICE simulation output

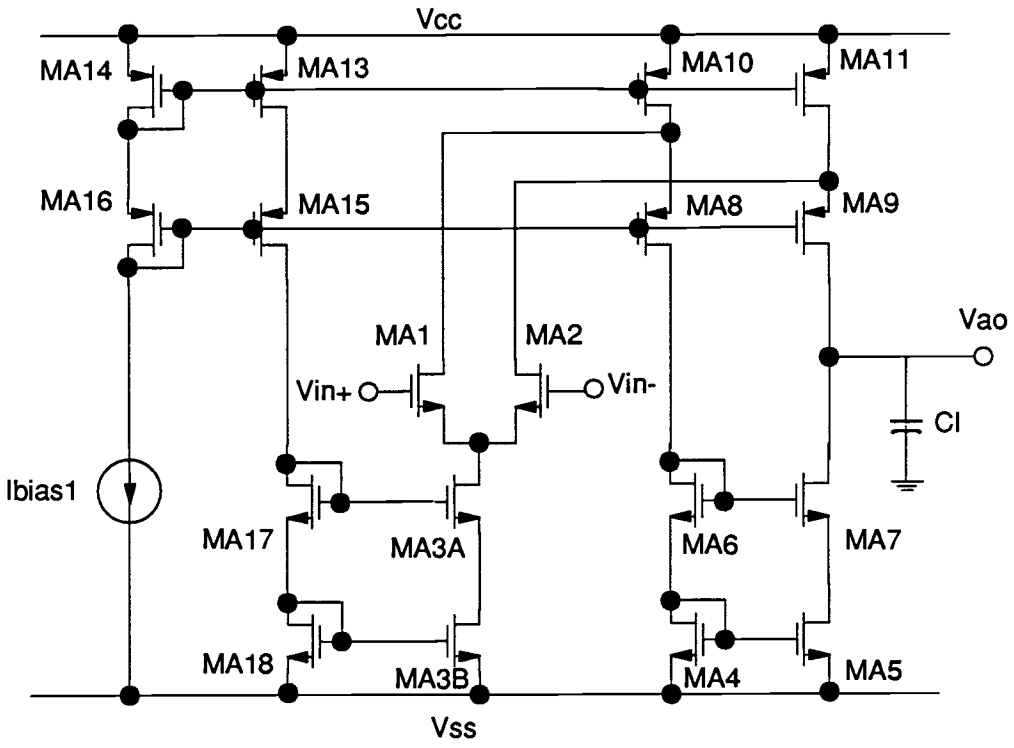

Figure 5.6 Operational Amplifier

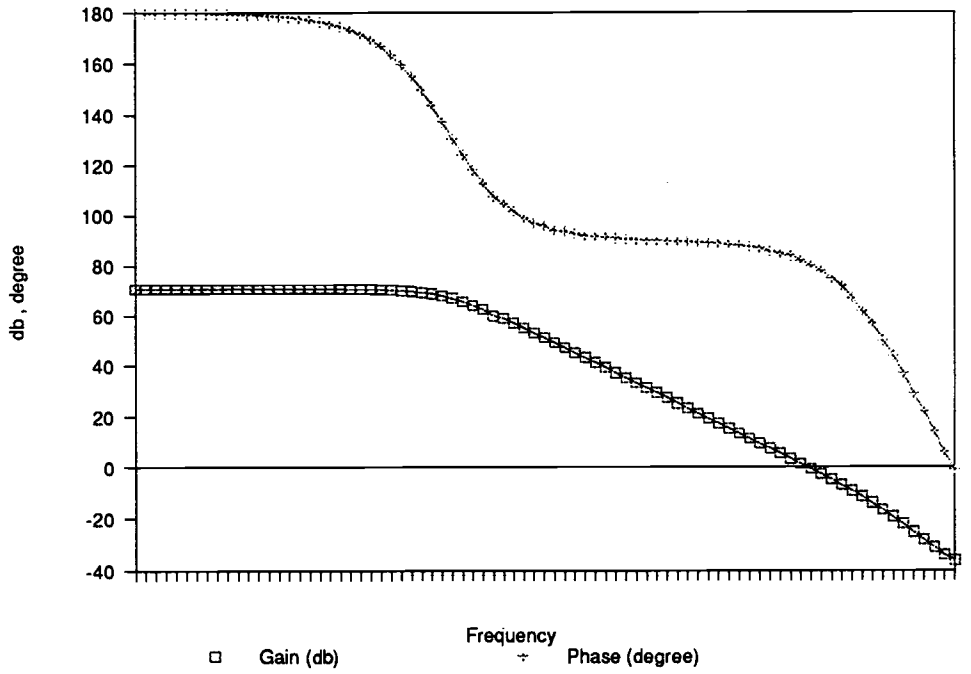

Figure 5.7 SPICE output of the frequency and phase response

of the frequency and phase response of the single gain stage amplifier. Table 5.4 lists all the transistor sizes for the amplifier OA1.

TRANSISTOR	W (um)	L (um)
MA1	200	3
MA2	200	3
MA3A	60	4
MA3B	60	4
MA4	60	4
MA5	60	4
MA6	60	4
MA7	60	4
MA8	120	4
MA9	120	4
MA10	120	4
MA11	120	4
MA13	120	4
MA14	120	4
MA15	20	4
MA16	20	4
MA17	60	4
MA18	60	4

Table 5.4 Transistor sizes for amplifier OA1

The basic Schmitt Trigger circuit is composed of transistors MN_1-MN_4 and MP_1-MP_4 as shown previously in Figure 5.5. Transistors MN_5-MN_6 and MP_5-MP_6 are the latch invertors whose functions are to ensure proper output polarity and latching. MPl_1-MPl_3 and MNl_1-MNl_6 provide the appropriate DC level shifiting such that one of the resulting output voltages is feed to the phase comparator and the other output voltage is used to turn transistor

MC_{21} on and off. The complete listing of the Schmitt Trigger and level shifter transistor sizes are listed in Table 5.5.

TRANSISTOR	W (um)	L (um)
MN1	25	5
MN2	35	5
MP1	25	5
MP2	35	5
MN3	25	5
MN4	25	5
MP3	25	5
MP4	25	5
MN5	50	20
MP5	50	20
MN6	10	20
MP6	10	20
MPL1	10	5
MPL2	18	5
MPL3	18	5
MNL1	20	5
MNL2	20	5
MNL3	20	5
MNL1	20	5
MNL2	20	5
MNL3	20	5

Table 5.5 Transistor sizes for schmitt trigger circuit

A simulation output of the VCO oscillating waveform at the capacitor node and theVCO output is shown in Figure 5.8. The resistor and capacitor value used for simulation is 4K ohm and 10nf respectively and the resulting oscillating frequency is approximatly 14K Hz.

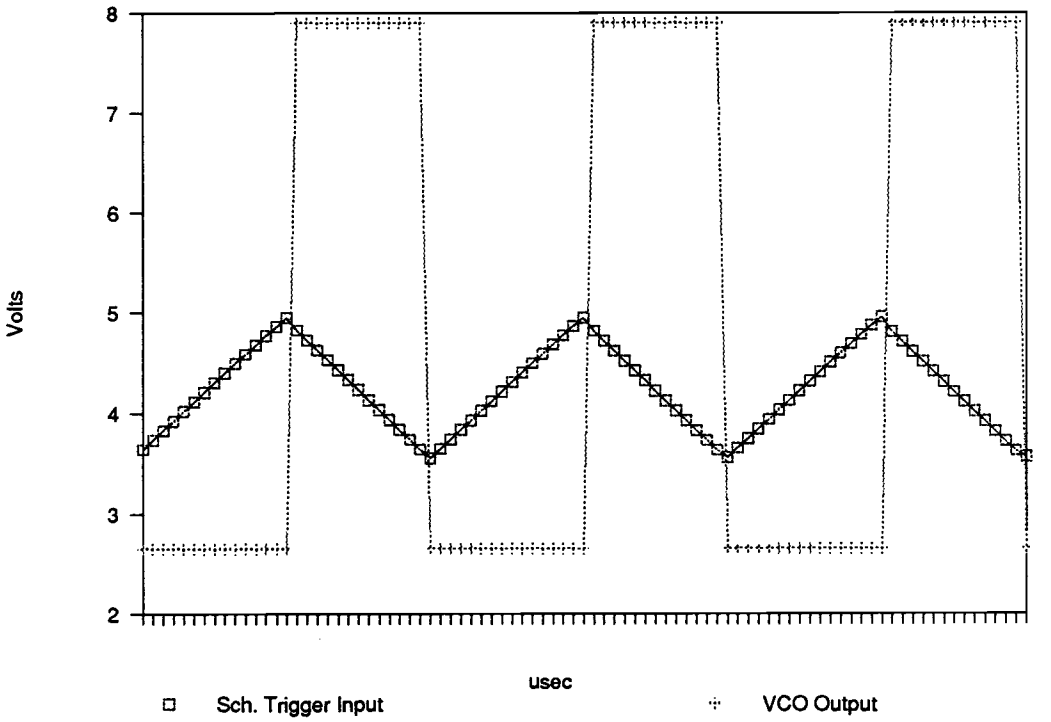

Figure 5.8 SPICE simulation of VCO oscillation waveforms

The bias voltage and current generation circuit is shown in Figure 5.9 where the resistor Rb is externally connected to provide the appropriate bias current to transistors MB_1 and MB_2. The result is the generation of the voltages Vbs3 and Vbs4 which are used to bias the level shifting circuit of VCO. The bias current is also "mirrored" by transistor MB_4 and MB_5 to provide the bias voltages Vbs_1 and Vbs_2 to the operational amplifier OA1. Futhermore, transistors MB_5 - MB_{12} produce the bias voltages VB_1 and VB_2 that are fed to the amplifier circuit. The complete list of transistor and its sizes are shown in Table 5.6.

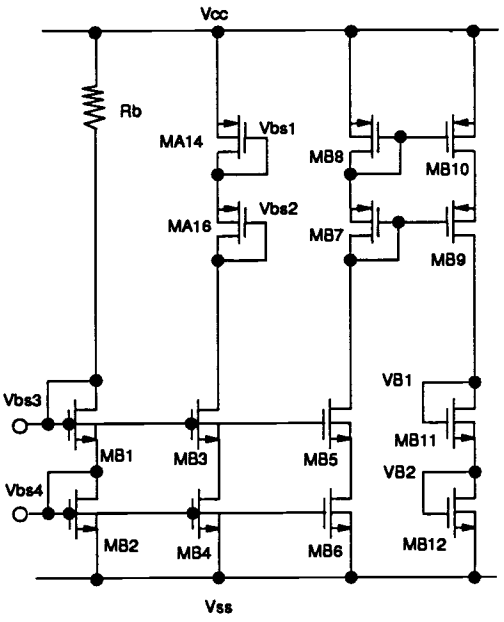

Figure 5.9 Bias voltages and currents generation circuit

TRANSISTOR	W (um)	L (um)
MB1	20	5
MB2	20	5
MB3	20	5
MB4	20	5
MB5	100	5
MB6	100	5
MB7	16	5
MB8	16	5
MB9	160	5
MB10	160	5
MB11	18	5
MB12	18	5
MA14	60	4
MA16	18	4

Table 5.6 Transistor sizes for bias voltages generator

The Phase-Locked Loop circuit is layed out in 2-um double-metal CMOS technology. The circuit is divided into six blocks and each block is plotted individually in appendix A. The layouts use layer-1 for p-well, layer-2 for active, layer-6 for poly, layer-8 for p+ implant, layer-10 for contact, layer-11 for first metal, layer-12 for via contact, layer-13 for second metal and layer-63 is used for text.

Figures in appendix A are described as follows. Figure A.1 is the plot for the layout of the phase detector. The loop amplifier is plotted in Figure A.2 and the layout for the bias generator circuit is shown in Figure A.3. The operational-amplifier plot is shown in Figure A.4 and the current source layout is plotted in Figure A.5. and finally, the Schmitt Trigger circuit and the level shifting devices layout are shown in Figure A.6.

CHAPTER 6

CONCLUSIONS

The objectives of this thesis is to present the modeling, circuit design, and layout technique for an analog CMOS Phase-Locked Loop circuit. The major goal is to provide a basic understanding of the modeling of the PLL system and its relationship to circuit design and applications. Subsequently, the analog CMOS PLL circuit was designed based on these concepts.

The PLL system was first modeled as a non-linear feedback system to illustrate the system condition before the loop is locked into the input signal. The results of this combination is that the output of the system has a sum and difference component of the two mixed signals in which the high freguency component is eventually filtered out by the loop filter. The difference comonent of the output signal is then fed into the VCO to force the PLL to lock to the input signals.

The PLL system is then modeled as a linear feedback system when the loop is locked to the input signal. This system is a first-order feedback system with a cutoff frequency which is proportional to the loop gain K_V when it has no loop filter present. However, a loop filter is always reuired because the -3_{db} cutoff frequency of this filter is usually less than the loop gain frequency. A large capture and lock range is desired to provide the system with a wide operating frequency and these ranges are proportional to K_V. Therefore, a large K_V is normally needed for the PLL system.

The loop filter, which is always present in a PLL system, provides a lower cutoff frequency to allow only the difference frequency to pass through and feed back into the loop to adjust the VCO oscillating frequency. A first-order feedback system can provide a lower cutoff frequency but is only marginally stable. An extra capacitor added to the first-order filter provides an additional zero to stablize the system. Second or higher order passive or active filter can also be used to provide a lower cutoff frequency for the PLL system.

The integrated analog CMOS PLL circuit was designed to work as a general-purpose device where its applications are limited to frequencies below 1000Khz. It has a flexibility of selecting a free-running oscillating frequency within this range by using an external capacitor and resistor. The circuit also has a relatively large loop gain, K_v, for a large capture and lock range.

There are many potential applications for the integrated CMOS PLL circuit. It can be used in frequency-shift-keying demulators, FM demodulation, and frequency-multiplication just to name a few applications. (The VCO protion of the PLL circuit can also be used as a FM modulator, waveform generator, or a clock generator). The PLL circuit's potential in other applications can also be enhanced when other system components are integrated into the same chip to decrease the original system size and cost. Therefore, further research can be done based on this information to design and integrated various types of communication systems that can be made smaller in area and be much more cost effective.

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APPENDICES

APPENDIX A

CIRCUIT LAYOUT

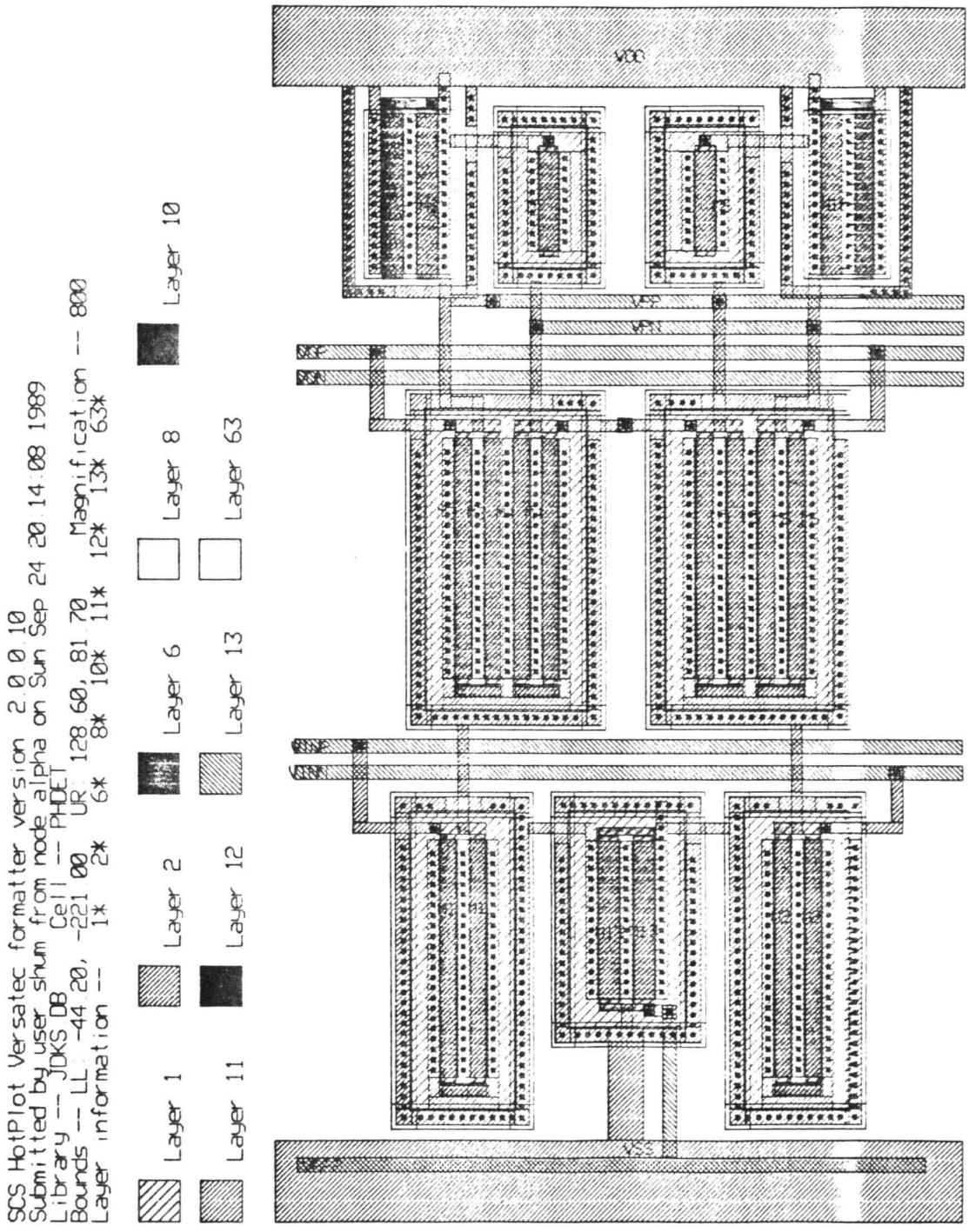

Figure A.1 Phase detector circuit layout

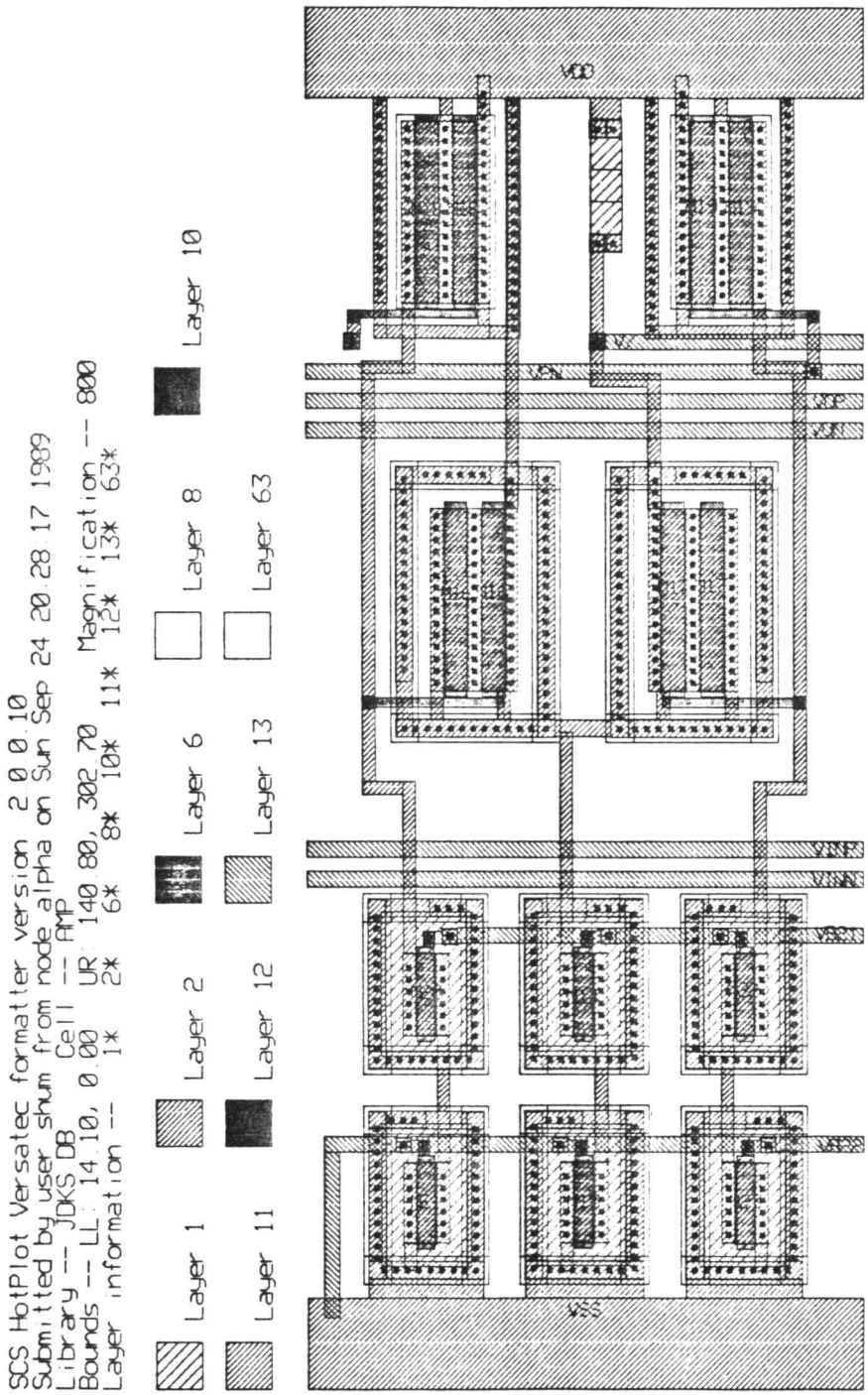

Figure A.2 Loop amplifier circuit layout

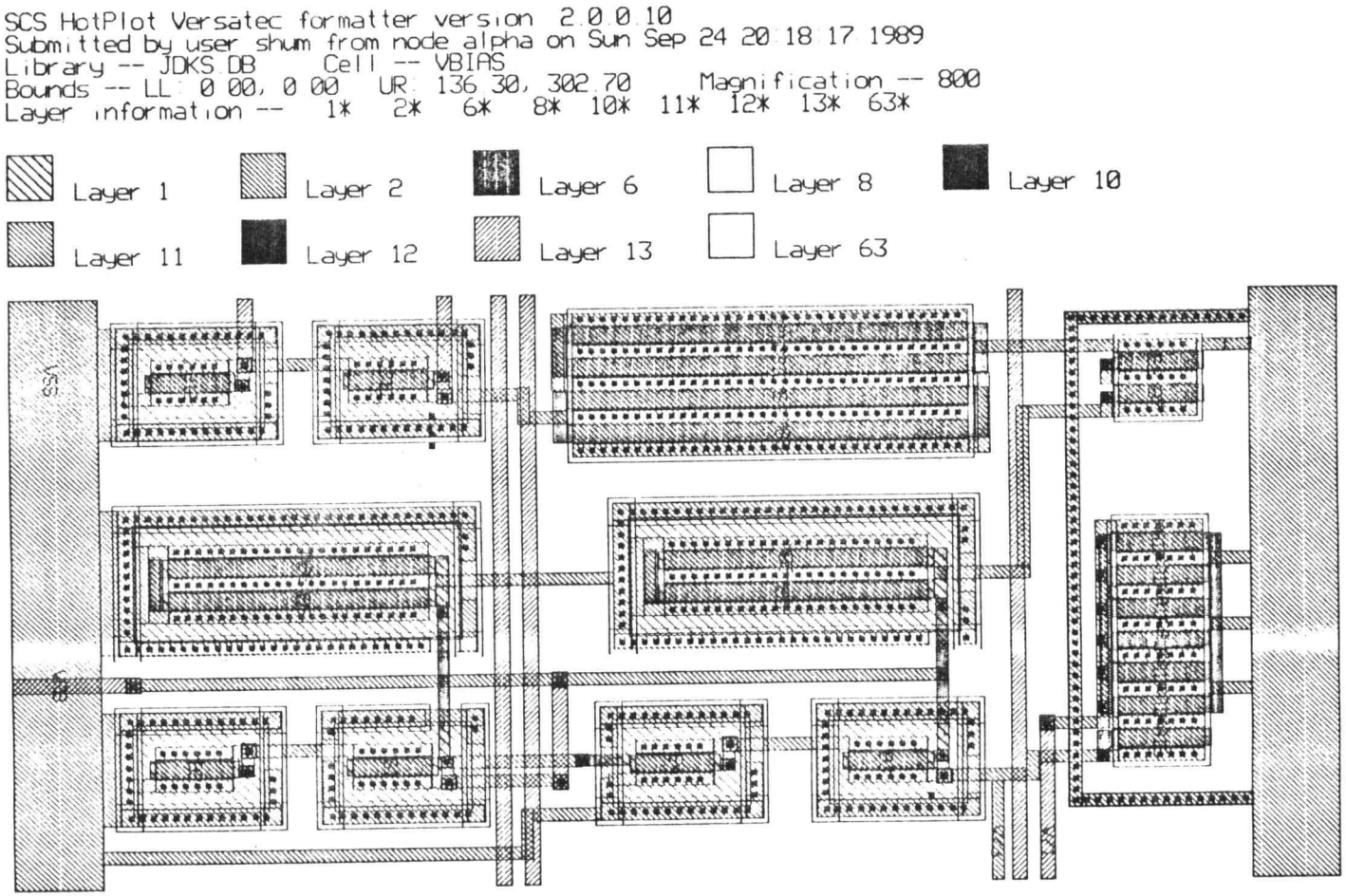

Figure A.3 Bias generator circuit layout

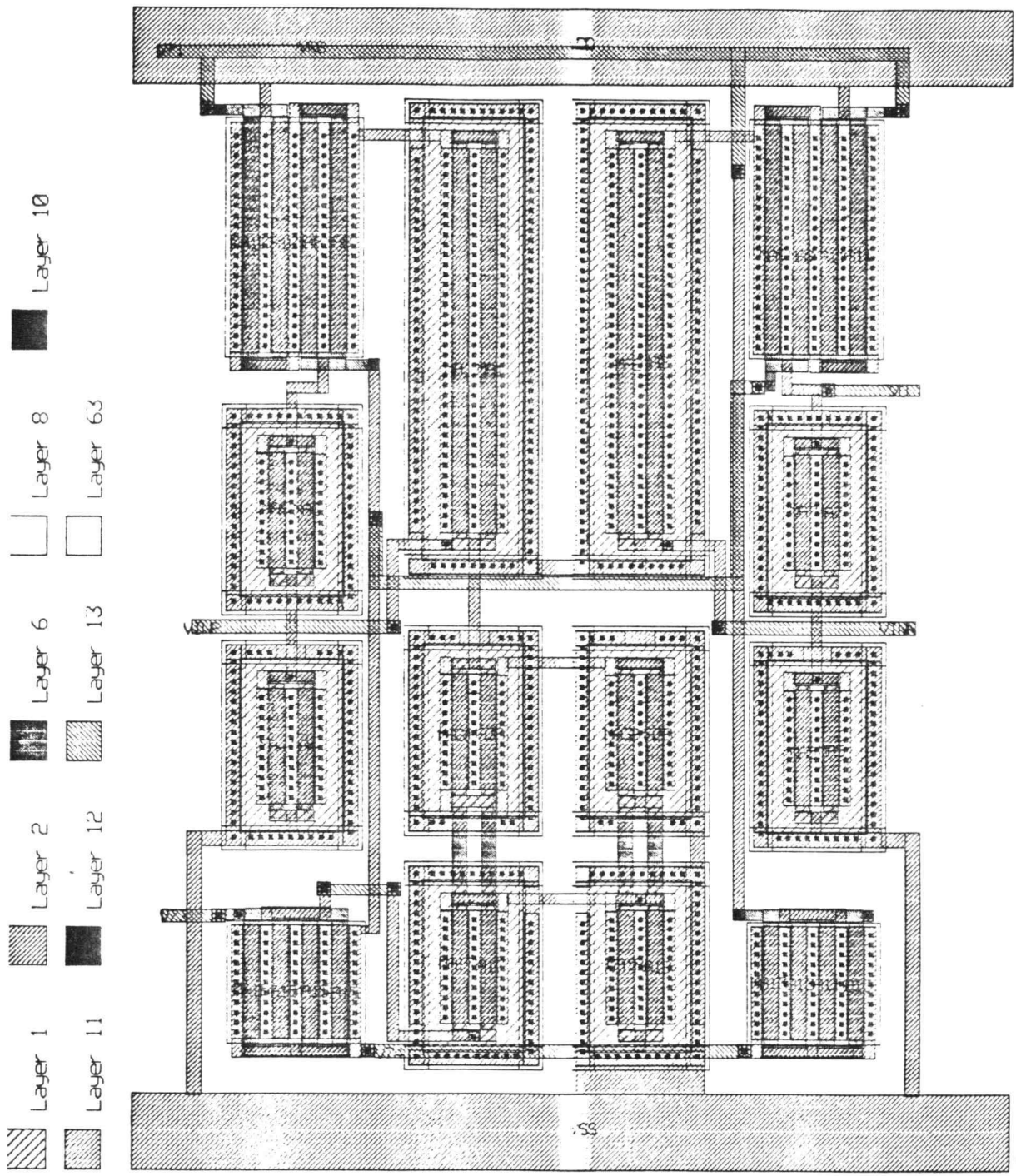

Figure A.4 Operational-Amplifier circuit layout

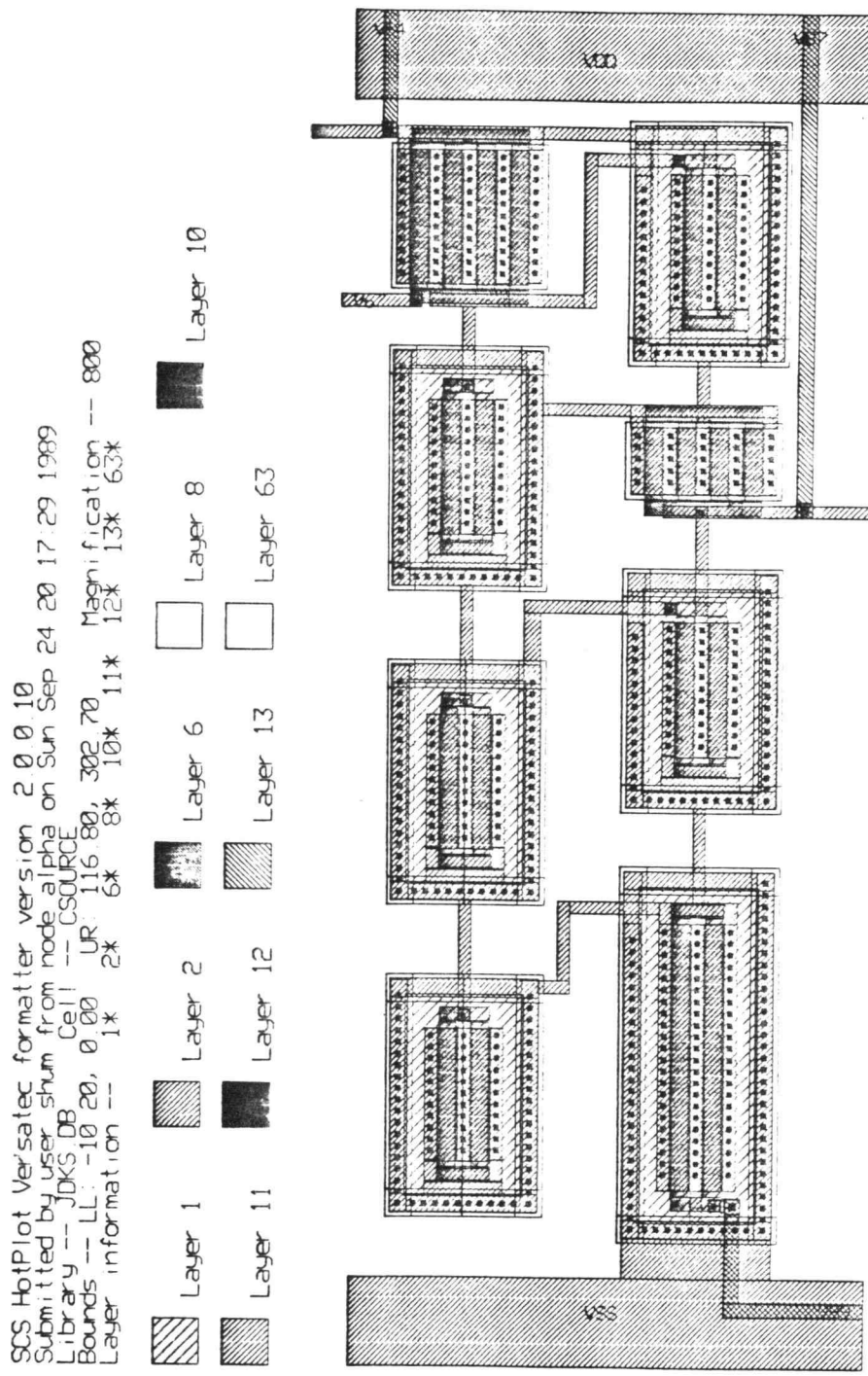

Figure A.5 Current Source circuit layout

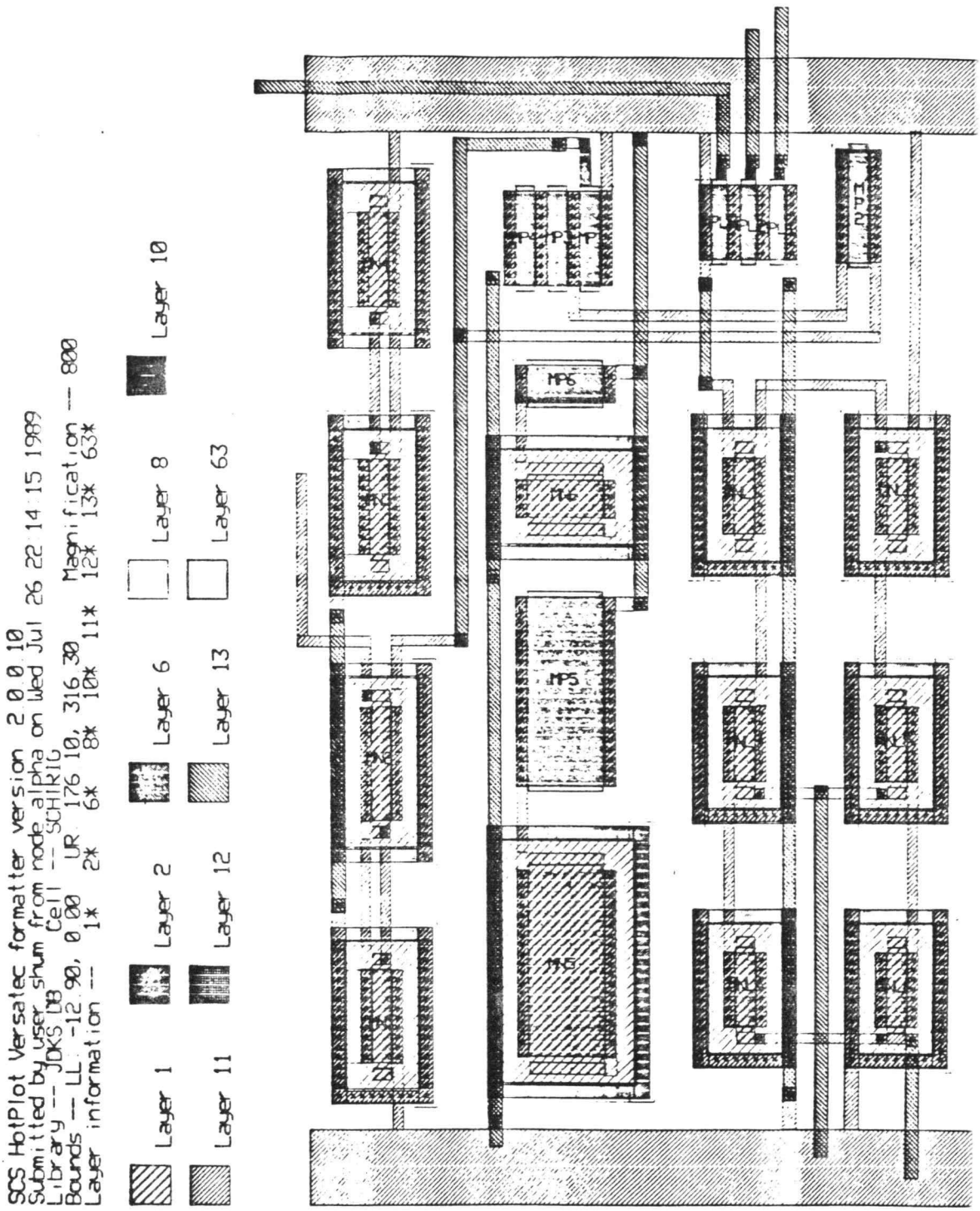

Figure A.6 Schmitt Trigger and level shifter circuit layout