Sinusoidal Clock Sampling for Multi-Gigahertz ADCs

Rui Bai, Jingguang Wang, Lingli Xia, Feng Zhang, Zongren Yang, Weiwu Hu, Patrick Chiang, *Member, IEEE*

***Abstract*—Current multi-gigahertz ADC performance is limited by the sampling clock timing jitter. This paper describes the effects of clock transition time on the spurious-free dynamic range (SFDR) of a CMOS T/H circuit. A signal-dependent nonlinearity model is first introduced that provides insight on the effect of finite clock transition time, and presents the use of sinusoidal signal as the sampling clock to improve SFDR. Whereas a square-wave clock exhibits a shorter transition time but more jitter susceptibility, sinusoidal clocking provides a longer transition time but a lower jitter spectrum. To verify this concept, an 8GS/s, 4b flash ADC with a sinusoidal clock is designed and experimentally measured, achieving a Figure-of-Merit of 0.86pJ/conv-step based upon ERBW (Effective Resolution Bandwidth), and 0.2pJ/conv-step based upon sampling rate.**

***Index Terms*—Flash ADC, sinusoidal clock, jitter, SFDR**

I. Introduction

HIGH-speed Analog-to-Digital Converters (ADC) are used in many communication and signal processing applications, such as UWB systems [1], SerDes receivers [2], and optical communication systems [3]. For an ADC with a sampling rate above GS/s, a high speed Track-and-Hold (T/H) circuit is typically used in the front-end, followed by time-interleaving sub-ADCs [2-7]. In order to meet the stringent performance requirements of such ADCs (multi-gigahertz sampling rate, 5-8 bits resolution), the T/H circuit requires high linearity and wide bandwidth. Furthermore, the performance of the ADC is usually limited by the jitter of the sampling clock [7-9]. Even a small sampling uncertainty can introduce a large error in the sampled voltage, resulting in harmonic distortion at the output. If other non-idealities are ignored, with a sinusoidal input, the signal-to-noise ratio (SNR), due to a sampling clock with RMS jitter ε_{rms}, is given by [4, 10]:

$$SNR = -20\log(2\pi \cdot f_{in}\varepsilon_{rms}) \quad \text{dB} \tag{1}$$

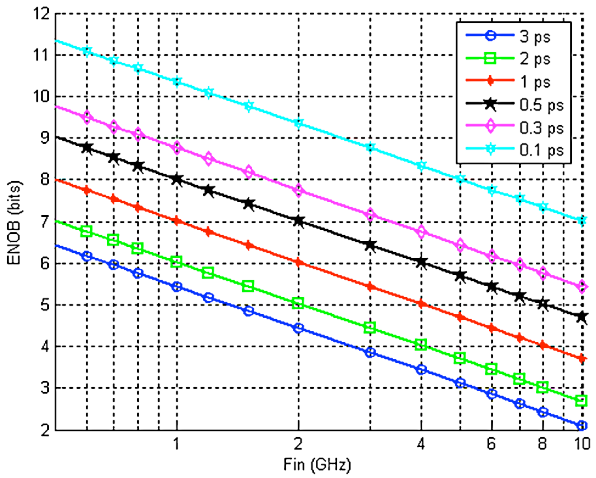

Fig. 1 ENOB versus signal frequency with varying RMS clock jitter values

where f_{in} is the input sinusoidal signal frequency. The Effective Number of Bits (ENOB) of the ADC versus input signal frequency with different RMS jitter values is plotted in Fig. 1. For example, in order to build an ADC with 2GHz signal bandwidth and 6-bit resolution, the clock jitter must be less than 1ps.

Typically, a short transition time square-wave signal is usually used as the sampling clock, generated by a chain of inverter buffers. The problem with these clock buffers is that they are susceptible to supply noise [11], especially when the ADC needs to share supply grid and substrate with noisy digital blocks on the same die.

Alternatively, if a low-jitter sinusoidal clock is generated locally to directly drive (or through a single stage of current-mode logic (CML) buffering) the T/H circuit in the ADC, the sampling uncertainty will be reduced. For example, a sinusoidal clock generated by an on-chip LC-VCO is the lowest jitter, multi-gigahertz source in a standard CMOS process. Unfortunately, compared with square-wave clock, the sinusoidal clock exhibits a slow slew rate during the clock transition, introducing an input signal dependent sampling error. This sampling error may then cause further distortion in the high speed T/H circuit [12].

In section II of this paper, the signal-dependent sampling error resulting from finite clock transition time will be analyzed mathematically, followed by a comparison between

Manuscript received January 1, 2011.

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the calculated and simulated results. And then, the simulated

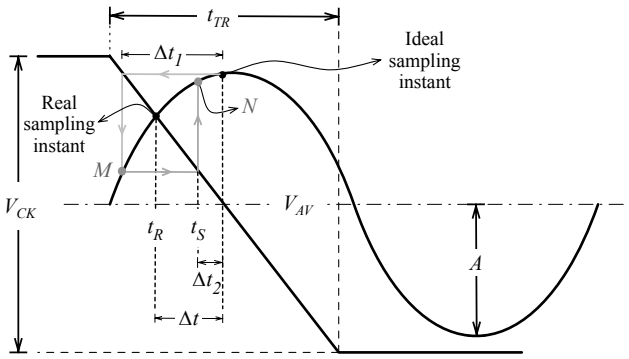


Fig. 2 Non-linearity model for an input-dependent sampling instant

SFDR of a realistic, high-speed NMOS T/H circuit with varying amounts of sampling clock transition time is presented, where the effects of signal-dependent nonlinearity on the SFDR are discussed. Section III presents the performance of this T/H circuit with a sinusoidal sampling clock. Section IV and V then introduce a new architecture of multi-gigahertz ADCs using sine-wave sampling, based on the above analyses. Section VI draws the conclusion.

II. Signal-dependent sampling error

Consider a NMOS T/H switch with its gate controlled by the clock, and source (or drain) connected to the input. When V_{gs} is larger than the V_{th} of the NMOS switch, the switch turns on and the output will track the input signal; otherwise the switch is turned off and the output holds the sampled signal. Fig. 2 shows the clock transitioning downwards, and its sampling position in the time domain. For the purpose of simplicity, the V_{th} is assumed to be zero, such that the switch is turned off when the clock signal is lower than the input signal. If there is no input signal dependency, the sampling point will always occur when the clock reaches V_{AV}, annotated by t_S in Fig. 2. However, in reality, the sampling instant takes place at t_R because that is the time when the clock voltage is the same as the input signal. Therefore for different input signal voltages, the sampling point will be different, resulting in signal level-dependent sampling error [10, 12].

A. Nonlinearity Model for Input-dependent Sampling

Because of the input-dependent Δt change at each sampling instance, the output of the T/H is:

$$V_{out}(t_S) = A\sin\omega(t_S - \Delta t) \tag{2}$$

where Δt is equal to $t_S - t_R$ as shown in Fig. 2. The crossing point between the input sine-wave and the clock falling edge is found from the solution to the following equations:

$$\begin{cases} y = A\sin\omega t \\ y = \dfrac{V_{CK}}{t_{TR}}(t - t_s) \end{cases} \tag{3}$$

Here we assume the input sine-wave exhibits a swing of A and frequency of ω, the square-wave clock amplitude is V_{CK}, and the transition time is t_{TR}. In order to calculate Δt, we need to find the expression of t in term of t_S. Unfortunately, there is no mathematical solution for equation (3). Therefore we use an approximation method to find an estimation of Δt.

First, the sinusoidal value at time t_S is defined as $A\sin(\omega t_S)$. By putting this same value to the line expression of the clock falling edge, we can calculate Δt_1 as shown in Fig. 2, where the time difference for the sampling clock and sampled signal to reach $A\sin(\omega t_S)$ is:

$$\Delta t_1 = \frac{A\sin(\omega \cdot t_S)\cdot t_{TR}}{V_{CK}} \tag{4}$$

Δt_1 is a good estimation of Δt, but we can bring this estimation even closer. From equation (2) and (4), we can obtain that the sinusoidal curve expression at point M is:

$$V_M(t_S) = A\sin\omega\cdot\left(t - \frac{A\sin(\omega\cdot t_S)\cdot t_{TR}}{V_{CK}}\right) \tag{5}$$

Similar to what was used to calculate Δt_1, if V_M is substituted into the line expression for a falling clock edge, we can calculate Δt_2 as shown in Fig. 2:

$$\Delta t_2 = \frac{V_M(t_S)\cdot t_{TR}}{V_{CK}} \tag{6}$$

With this value of Δt_2 we can obtain an expression for the value of point N on a sinusoidal curve:

$$V_N(t_S) = A\sin\omega\cdot\left[t_S - \frac{A\sin\omega\cdot\left(t_S - \dfrac{A\sin(\omega\cdot t_S)\cdot t_{TR}}{V_{CK}}\right)\cdot t_{TR}}{V_{CK}}\right] \tag{7}$$

By carrying out this search recursively, a better estimation of the actual sampling point can be reached. Because N is already close enough to calculate the 3rd order harmonic, the Taylor series expansion on the right side of equation (7) gives:

$$V_N(t_S) = \left(A + \frac{17}{8}\frac{A^3\omega^2 t_{TR}^2}{V_{CK}^2}\right)\sin\omega t_S - \frac{3}{8}\frac{A^3\omega^2 t_{TR}^2}{V_{CK}^2}\sin 3\omega t_S + \cdots \tag{8}$$

The 3rd order harmonic is usually the dominant distortion component for a differential input, so for a T/H circuit with input-dependent sampling error, the SFDR can be estimated as:

$$SFDR = \frac{A + \dfrac{17}{8}\dfrac{A^3\cdot\omega^2\cdot t_{TR}^2}{V_{CK}^2}}{\dfrac{3}{8}\dfrac{A^3\cdot\omega^2\cdot t_{TR}^2}{V_{CK}^2}} \approx \frac{8\cdot V_{CK}^2}{3\cdot A^2\cdot\omega^2\cdot t_{TR}^2} \tag{9}$$

Observe that the SFDR is proportional to the square of the clock amplitude V_{CK}, inversely proportional to the square of

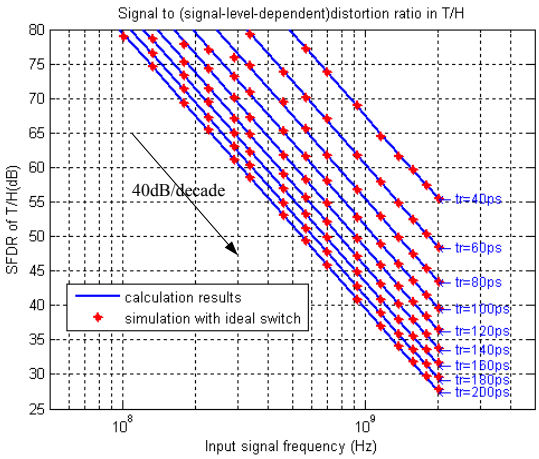


Fig. 3 SFDR limited by signal-dependent sampling error, with calculated and simulated results (clock amplitude 1.5Vp-p, input signal swing 0.8Vp-p)

the clock transition time t_{TR}, input signal swing A, and input signal frequency ω.

B. *Calculated result versus simulated result*

In order to verify the nonlinearity model derived above, we use an ideal switch where only the signal dependent sampling nonlinearity is considered.

Fig. 3 shows the derived and simulated results for different clock transition times and input signal frequencies. With the same clock and signal amplitude, the model matches the simulation results very well, as the SFDR rolls-off by 40dB/decade as expected when the input signal frequency increases. Note that the 3rd harmonic distortion deteriorates by about 12dB as the clock transition time doubles. For a wide-band ADC, the sampling clock with a long transition time will limit the resolution. For example, if the clock transition time is 120ps and the input signal frequency is 2GHz, the signal-dependent sampling error limits the SFDR to approximately 36.5dB.

C. *SFDR Limitation in T/H Circuits*

Besides the signal-dependent sampling nonlinearity, a real T/H circuit exhibits distortions and noise from other sources such as charge injection, switch turn-on resistance modulation, and clock feed-through, further deteriorating the SFDR. In order to find out the dominant non-ideality within a high speed T/H, as well as determine the minimum requirement of the clock transition time for a multi-gigahertz ADC (i.e. 6-bit 2GHz signal bandwidth ADC), a differential NMOS T/H circuit is designed within a 90nm CMOS process, as shown in Fig. 4.

M1 and M2 are the differential sampling switches driven by clk. The dummy transistors M3-M6, controlled by clk_bar, are used to reduce the charge injection when M1/M2 switch from track mode to hold mode [13]. M3-M6 are half the size of M1/M2. M7 and M8 are introduced to provide signal feed-through compensation in hold mode. In this T/H simulation, the clock and input signals are characterized similar to the

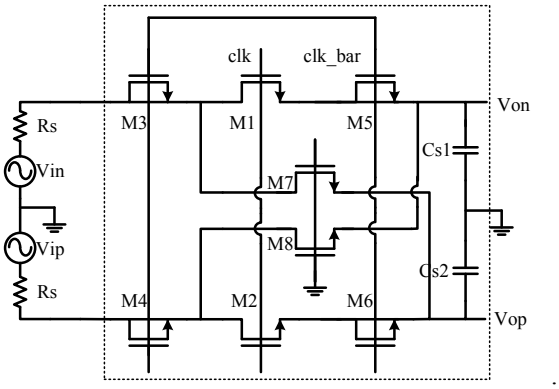


Fig. 4 Schematic of a differential NMOS T/H circuit

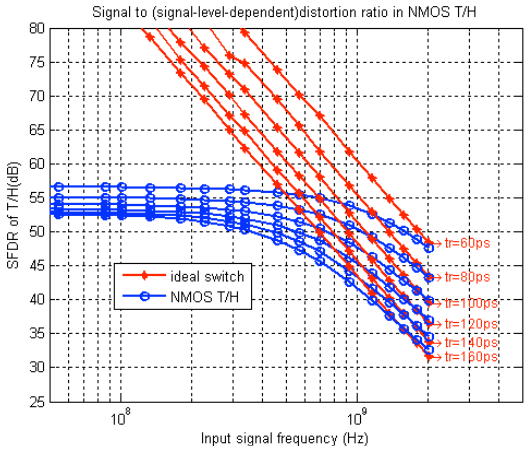


Fig. 5 SFDR simulations of an ideal switch versus NMOS T/H switch across varying clock rise time

preceding ideal switch simulation.

Fig. 5 shows the simulation results comparing the NMOS T/H circuit with the ideal switch T/H circuit. Considering only the signal-dependent sampling error, we can observe the following:

- At low frequency (f_{in}<500MHz), the signal dependent sampling error is not significant compared to other nonlinearity effects, but it dominates at higher frequency because it increases by 40dB/decade.
- Other nonlinearity issues like switch turn-on resistance modulation is also dependent on clock transition time. For example, at low frequency, the SFDR with a 60ps clock transition time is about 4 dB higher than that with a 160ps clock transition time. In other words, clock transition time only slightly affects those nonlinearities.
- Although the signal-dependent sampling nonlinearity dominates at high frequency, with reasonable clock transition time and input signal swing, the introduced distortion can still be smaller than that caused by increased clock jitter.

III. Sinusoidal Clock Sampling T/H Circuits

In Fig. 5, the SFDRs of the T/H circuit with varying clock

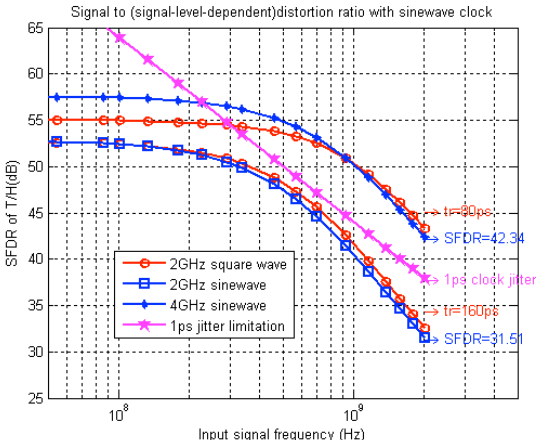


Fig. 6 SFDR of NMOS T/H circuits with both sine-wave and square-wave clocking (input signal swing 0.8Vp-p, clock swing 1.5Vp-p)

transition times are compared. If a sinusoidal signal is used as the sampling clock instead, the slew rate of the clock is:

$$SR = \frac{\mathrm{d}(A\sin\omega t)}{\mathrm{d}t} = A\omega\cos(\omega t) \tag{10}$$

The slew rate (SR) is proportional to the clock frequency, and a maximum slew rate occurs when $\omega t = n\pi, (n = 0, \pm 1, \pm 2\cdots)$. For multi-gigahertz clocks, the slew rate of a sine-wave clock is comparable to that of a square-wave clock, which is limited by the loading capacitance and the buffer current in real implementation. For example, a 4GHz sine-wave clock has almost the same slew rate as a square-wave clock with 80ps transition time and the same voltage swing.

Fig. 6 shows the SFDR of the T/H circuit with a sine-wave clock and a square-wave clock. At high frequency, the SFDR of the 4GHz sine-wave clock is close to that of the 80ps transition time square-wave clock. This is expected because they have comparable slew rates. In Fig. 6, we also plot the SNR limit in a T/H circuit when 1ps RMS jitter is present in the sampling clock. As observed, for a 6-bit 2GHz bandwidth ADC, the clock jitter should be smaller than 1ps. Since the ADC is typically used in a system-on-a-chip with noisy digital blocks, it may be non-trivial to generate a square-wave clock with such small jitter, and a low-noise clock buffer can also be power hungry. Instead, if a 4GHz sine-wave is used as the sampling clock, a lower clock jitter can be utilized at the expense of a larger input-dependent sampling error. As shown in Fig. 6, using a 4GHz sine-wave sampling clock limits the SFDR to approximately 42dB for a 2GHz input bandwidth. This is still 6dB higher than the SNDR required for a 6-bit ADC.

IV. Design Example: Flash ADC Incorporating Sine-wave Sampling

Based on our previous analysis on the advantages of sine-wave sampling, an 8Gs/s flash ADC is proposed that incorporates a sine-wave clock source. Fig. 7 shows the overall schematic of the ADC. The input data is directly sampled by 15 comparators, each followed by a SR-latch to generate a 15b thermometer code. To reduce the probability of errors caused by comparator metastability, a bubble correction stage is used. Finally a 4-bit Gray code is generated by the ROM-based decoder.

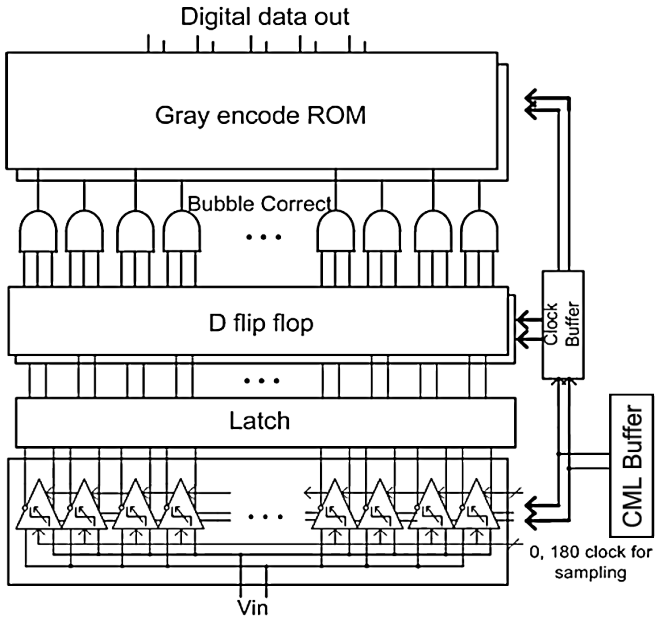


Fig. 7 Architecture of proposed Flash ADC

The sine-wave clock source can be generated using an on-chip LC-VCO, which either directly drives the capacitance loading of the comparators through resonant clocking [11], or using a single-stage CML buffer that separates the LC-VCO from possible noise kick-back. Using a resistively loaded CML buffer adds to power consumption, as large static current is needed to achieve near full-rail clock swing. Alternatively, an injection-locked VCO can be used as a clock buffer to drive the entire load capacitance. However, accurate control of the actual resonant clock frequency due to the presence of parasitic loading of the large wiring/gate capacitance is difficult in practice [11].

Fig. 8 shows the schematic of the comparator used in the ADC. Current steering is shared between two comparators working in bang-bang mode at 4GHz, realizing an effective sampling rate of 8GS/s. Each comparator is folded into two stages in order to operate under a low supply [6].

The first stage works as both a sampler and a pre-amplifier. It is followed by the latch stage. The PMOS load in the first stage is turned off in sampling mode in order to achieve a higher sampling bandwidth. After the comparator has completed sampling, the PMOS load turns on to reset the latch. Another advantage of this comparator is that clock kickback is eliminated because the switches are connected to the common mode point in the signal path.

Fig. 9 here shows the simulated results of comparator quantization delay for different input amplitudes, for both a 4GHz sine-wave clock and a 20ps rise-time square wave clock.

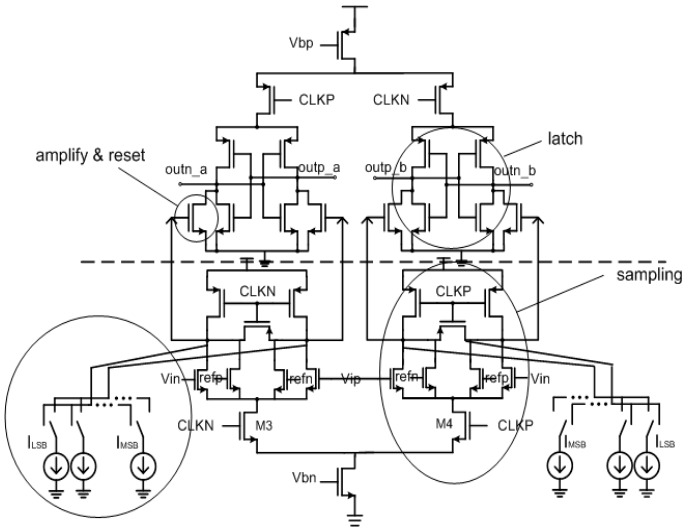


Fig. 8 Schematic of comparator with offset calibration

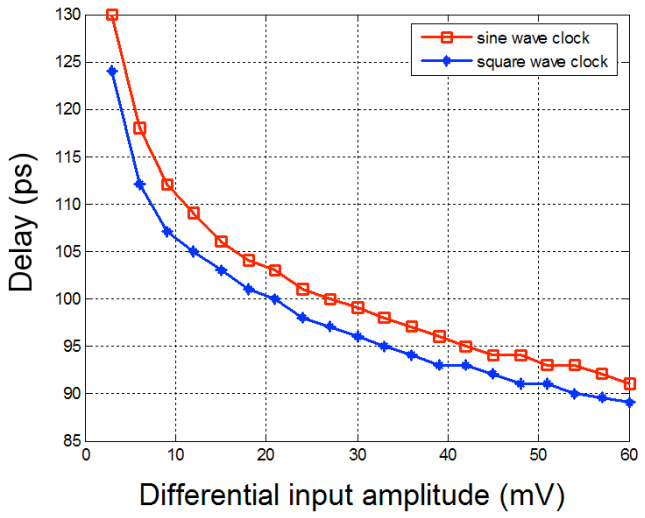


Fig. 9 Comparator delay with various input amplitude

The difference in quantizer delay is less than 5ps for all input signals. This delay degradation is minimized due to the current steering nature of the complementary quantizers, where absolute clock voltage is less important than the ability for the differential pair to hard switch the current from one branch to the other.

In deep submicron CMOS processes, the mismatch and process variation is a critical limitation. Monte-Carlo analysis indicates that 3-sigma variation introduces about +/- 40mV of input-referred offset in our design. In this design, a digitally controlled 6-bit current source provides extra current for the output nodes of the first stage in order to introduce an intentional offset and hence, process variation calibration [14].

One possible concern is whether the sinusoidal clock exhibits a fast-enough sampling bandwidth, compared to the conventional, square-wave clock. We simulate the pulse sensitivity function to evaluate the sampling bandwidth of the comparator. As shown in Fig. 10, only a 0.2dB difference exists in the transfer function at 4GHz when sampled by either the sinusoidal clock or 20ps rise/fall time clock. Therefore, a sinusoidal sampling clock does not significantly affect the

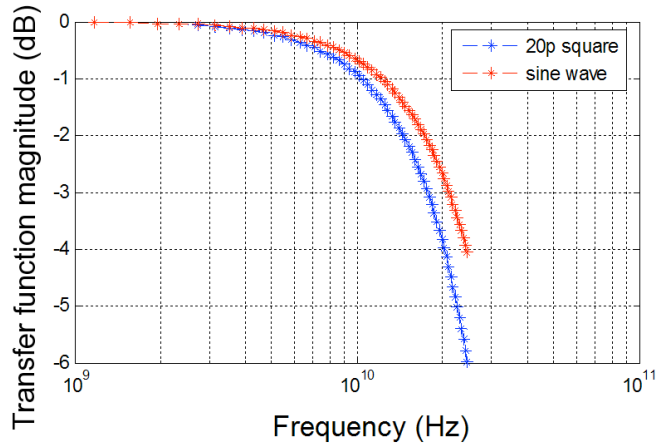


Fig. 10 Comparator sampling bandwidth, comparing a sine-wave with square wave clocking

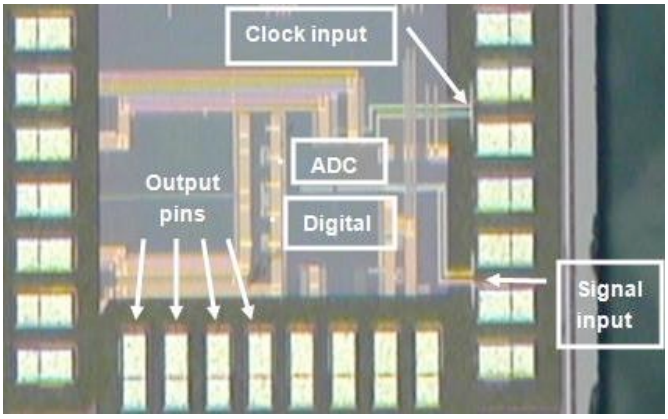


Fig. 11 Die microphotograph

performance of this ADC up to the Nyquist bandwidth.

V. Experimental Measurements

The ADC was fabricated in a standard 65 nm CMOS technology. Fig. 11 shows the micrograph of the ADC. The ADC was wire-bonded using chip-on-board to a PCB. While great care was taken initially to maintain a large input bandwidth, several problems manifested during the measurement testing, resulting in severely degraded performance. First, ESD devices were not incorporated into the original design in order to improve bandwidth. Unfortunately, the thin oxide of this 65nm-CMOS process is severely sensitive to ESD, preventing reliable measurements. Hence, off-chip ESD packages of size 2.7pF had to be incorporated into a second board revision, loading the input impedance. Second, a wideband balun was designed to enable single-ended to differential conversion from the off-chip sinusoidal signal generator. Unfortunately, the balun low-pass filtered input frequencies below 1MHz (such as a slow linear ramp), preventing calibration and cancellation of DC offsets in the comparators. Hence, the balun was eliminated and a 1cm shorting wire was employed to connect the input traces. Finally, small AC coupling capacitors were utilized in the signal chain in order to independently set the input common-

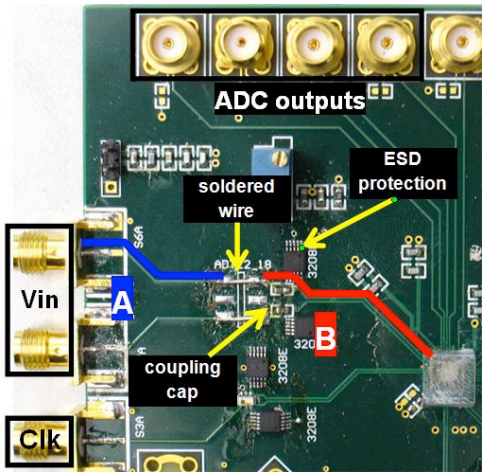


Fig. 12 PCB layout of the differential input impedance and associated discontinuities

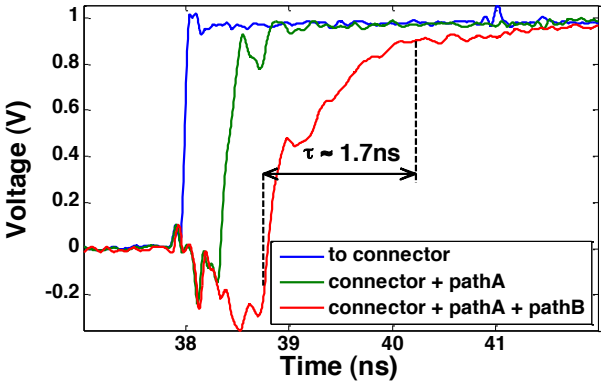


Fig. 13 Step response from a measured time-domain reflectometer at: a) PCB input; b) before soldered wire interface; c) after soldered wire and ESD connection, directly to the chip input.

mode, also degrading input bandwidth.

All of these non-ideal discontinuities result in significant distortion in the step response for the PCB differential input. Shown in Fig. 13 above is the step response at various places on the PCB after performing a TDR (Time-Domain Reflectometer). Here, the final signal bandwidth at the input to the chip, after wave propagation through these multiple discontinuities, shows a rise time and estimated input bandwidth of less than 1GHz.

The prototype operates with a 1 V analog and 1.2 V digital supply voltage. The output of the ADC is decimated by 64 before going off-chip to the logic analyzer. Before/after calibration, the measured DNL is 2.39/0.16 LSB while the INL is 1.51/0.16 LSB, respectively.

Shown in Fig. 16 is the measured ADC performance for a 2.6MHz input, exhibiting a SNDR of 24.93 dB, and 20.72 dB with a 1.2 GHz input. Note that while the Nyquist rate after 64x decimation is 31.25 MHz, the higher frequency distortion components fold back to below this range, such that the SNDR remain unchanged after decimation.

Measured SFDR/SNDR across varying input frequencies is shown in Fig. 17. At near DC (2.6MHz), the measured ENOB is 3.9b. Between 940–1500MHz, the ENOB degrades to 3.3-

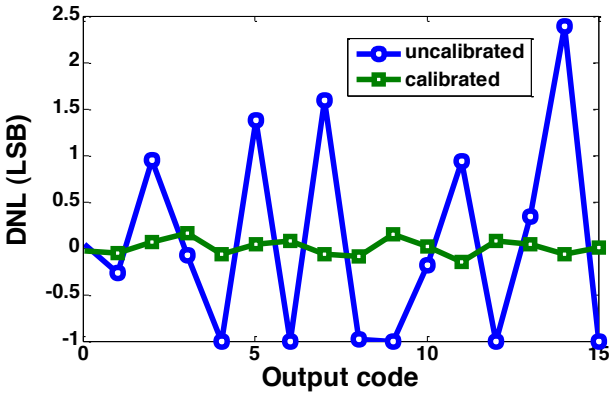


Fig. 14 DNL before/after calibration

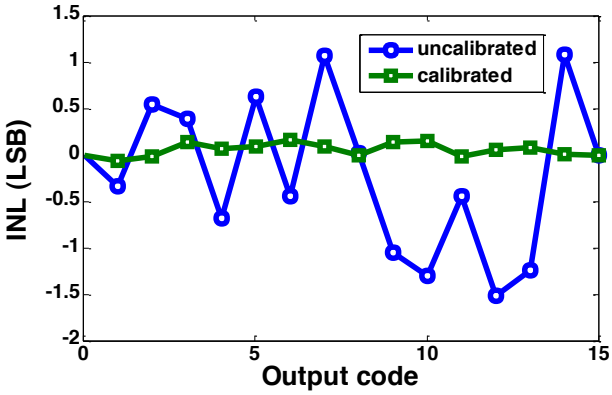
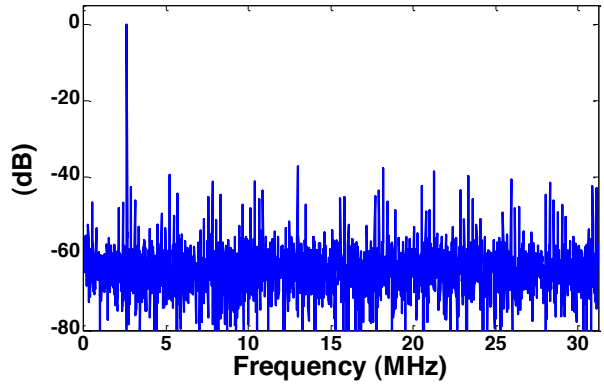
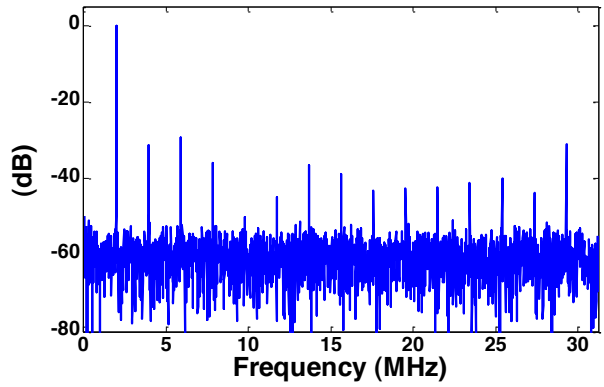


Fig. 15 INL before/after calibration



(a)



(b)

Fig. 16 Measured SNDR performance, after decimation by 64x, with f_{IN}: a) 2.6MHz; b) 1.2GHz

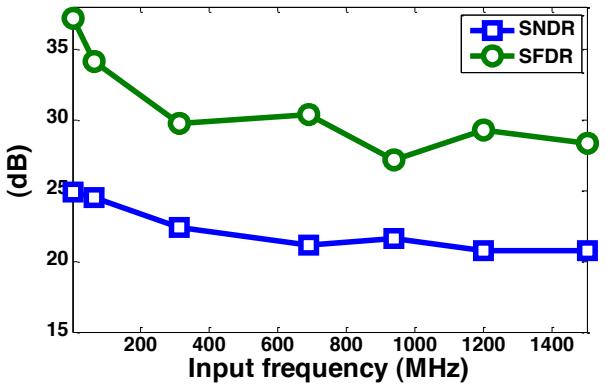


Fig. 17 SNDR/SFDR across varying input frequencies

3.15b, due to the input impedance discontinuities mentioned earlier.

Table 1 below summarizes the performance of the measured chip results.

Table 1. Performance of the proposed flash ADC

Process	65nm-CMOS
Resolution	4
Speed	8 Gs/s
DNL (before/after calibration)	2.39/0.16
INL (before/after calibration)	1.51/0.16
SNDR (f_{in}=2.6MHz)	24.93 dB
Supply	1V (analog) 1.2V(digital)
Input Range	0.26 V_{pp} (differential)
Power (analog)	11.2 mW
Power (CML clock buffer)	12 mW
Power (divider)	18.8 mW
Power (digital, output buffer)	24.6 mW
ERBW (Effective Resolution Bandwidth)	940 MHz
FOM ($\frac{P}{2^{ENOB}\cdot 2\cdot ERBW}$)	0.86 pJ/conv.

The FoM (Figure-of-Merit) of this Flash ADC is compared with recent multi-gigahertz Flash ADCs in Fig. 18. Note that in order to normalize the power consumption relative to other works, only the analog power is factored in here, consisting of the clock buffer and comparator power. At this high sample rate, the clock power is comparable to the dynamic comparator power. The measured FoM of 0.86pJ/conv-step compares competitively with other designs, even with the low ERBW caused by the poor input impedance matching. If we consider sampling rate instead of ERBW in the Figure-of-Merit, the energy consumed per conversion step is 0.2pJ/conv-step.

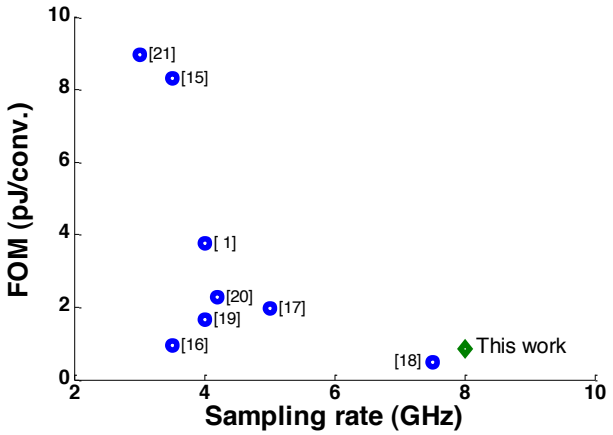


Fig. 18 Comparison of the energy-efficiency of this work versus recent multi-gigahertz Flash ADCs

VI. Conclusion

The effect of clock transition time for high-speed, multi-gigahertz T/H circuits is analyzed using a proposed signal-dependent, nonlinear model. Based on this analysis, a sine-wave sampling clock is proposed as an alternative to a traditional square-wave sampling clock for jitter-limited high speed ADCs. As an example, an 8Gs/s 4-bit Flash ADC in 65nm-CMOS is built that incorporates this sine-wave sampling clock. Measurement results show that competitive energy efficiency is achievable for this sine-wave ADC when compared with conventional high-speed flash ADCs.

Acknowledgement

This work is supported by NSF, the National Natural Science Foundation of China under grant no.60736012 and 60921002. The authors would like to thank Tao Jiang and Kangmin Hu for discussions and help in testing.

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