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Shivani Gupta for the degree of Master of Science in Electrical & Computer Engineering presented on February 24, 1995.

Title: A 1-mW, 14-bit ΣΔ A/D Converter with 10-KHz Conversion Rate

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Oversampled analog-to-digital converters (ADC) based on sigma-delta (ΣΔ) modulation are attractive for CMOS VLSI implementation because of their high tolerance to circuit non-idealities and component mismatch. Higher-order modulators are shown to not only greatly reduce the oversampling requirements for high resolution conversion applications, but also randomize the quantization noise to avoid the need of dithering. However, potential stability has always been a limitation to higher-order modulators. Use of a multibit internal quantizer makes realization of stable higher-order converters feasible, but the performance of multibit converters is generally degraded by the internal component mismatch in the digital-to-analog converter (DAC). Several digital correction and dynamic element matching techniques have been introduced to minimize this degradation. In this thesis, the design of a low-power third-order ΣΔ converter with a 4-bit internal quantizer is presented. A new architecture is proposed to realize a power-conservative converter that will enable the use and testing of various dynamic element matching schemes. Simulations show that the overall stability of the 3^{rd}-order modulator is greatly enhanced by the use of a 4-bit quantizer and a signal-to-noise ratio (SNR) of 90 dB is achieved with the combination of 3^{rd}-order modulation and 4-bit quantization at 256 KHz clock frequency. Low-power design strategies are presented for this ΣΔ A/D converter.

A 1-mW, 14-bit $\Sigma\Delta$ A/D Converter with 10-KHz Conversion Rate

by

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Shivani Gupta, Author

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Chapter 1
INTRODUCTION

The scaling of integrated circuits is fast becoming a popular trend due to the recent advances in fine-line CMOS VLSI technologies. This scaling is especially promising for digital integrated circuits which result in the realization of more complex functions and higher speeds on a single chip. However, it has some disadvantages for analog circuits, such as reduction in dynamic range, degraded matching, reduction in the output resistance of the devices, and so on. Therefore, *digital signal processing* has replaced many functions that were originally implemented by analog circuits. Signals of particular interest are audio, Integrated Services Digital Network (ISDN), and video signals. Since the signals are inherently analog in nature, the interface circuitry that performs data conversion are the key elements in signal processing. The oversampled analog-to-digital converter (ADC) based on sigma-delta ($\Sigma\Delta$) modulation is one of the candidates which can overcome the disadvantages of analog circuits. A $\Sigma\Delta$ converter samples the input much above the Nyquist rate which results in translating the quantization noise frequencies well above the signal band. This noise is later eliminated by a digital low-pass filter which also down-samples the modulator output to the Nyquist rate. Single-bit $\Sigma\Delta$ ADCs are very suitable for MOS VLSI because of its insensitivity to process variation and component mismatch. However, sigma-delta converters with multi-bit quantizers embedded in the feedback provide a number of advantages over single-bit quantizers:

1. The quantization noise is lowered for a given oversampling ratio,

2. Stability of higher-order loops is greatly improved, and

3. Quantization noise introduced by the coarse quantizer is more random (hence the commonly used white noise assumption is more applicable).

The lowering of quantization noise is attributed to the signal-to-noise-ratio (SNR) improvement by 6 dB/bit. Thus, incorporating multi-bit quantizers into low-power, low-voltage designs compensates for the loss in dynamic range.

The main disadvantage of having a multi-bit loop is that the overall linearity is limited by the feedback digital-to-analog converter (DAC) since any non-ideality in the feedback DAC appears at the input of the modulator and is aliased into the baseband as noise which places stringent matching requirement on the DAC elements. There have been past attempts to correct the feedback DAC non-linearities by using *digital self-calibration* and *dynamic element matching* techniques.

As more measurement instruments are becoming battery operated portable units, the drive for high resolution is increasingly accompanied by the requirement for low-power. A design that focusses on the twin issues of precision and low power consumption is presented in this thesis. A third-order low-power (1mW) $\Sigma\Delta$ ADC with a 4-bit quantizer embedded in the feedback loop was designed to test various existing dynamic element matching techniques to correct DAC distortion.

Chapter 2 introduces the basic concept of oversampled $\Sigma\Delta$ A/D conversion followed by a brief discussion of various existing architectures for the optimization of power and performance. The design objectives are summarized in this chapter. In Chapter 3, an optimal architecture is proposed. Some background of dynamic element matching is presented along with a short discussion of the various algorithms. Chapter 4 focusses mainly on the implementation and power saving methodologies that were adopted at the circuit-level. In Chapter 5, simulation results are presented along with the suggested testing of the chip. In the last chapter, conclusions are stated and some suggestions for the future research are made.

Chapter 2
ARCHITECTURES

In this research, a variety of architectures were evaluated against the resolution and power specifications. The simplest form of a $\Sigma\Delta$ modulator is illustrated in Fig. 2.1 [2]. It contains a summer at the input, an integrator, a coarse ADC followed by a decimator. The modulator section, shown in Fig 2.1 consists of a DAC in the feedback loop to convert the coarse quantized output to an analog signal which can now be subtracted from the input.

One way to view the behavior of the modulator is that the ADC forms a fast-changing coarse approximation, Y(t), that oscillates around the slow-changing value of X(t). The integrator will constantly force this approximation to move in a direction that brings the integrator's own input toward a zero average. Consequently, the dc error between the analog input and the digital output approaches zero. Analyzing the operation of a $\Sigma\Delta$ modulator quantitatively is done by modeling the integrator by it's discrete-time equivalent and replacing the quantizer by a unity-gain element with an additive noise source, E(z), as shown in Fig. 2.2. E(z) is treated as an uncorrelated white noise [14]. With this linearized model of the $\Sigma\Delta$ modulator, it can be shown that

$$\begin{aligned} A(z) &= X(z) - Y(z), \\ B(z) &= \frac{z^{-1}}{1 - z^{-1}} \cdot A(z), \\ Y(z) &= B(z) + E(z), \\ Y(z) &= z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z). \end{aligned}$$

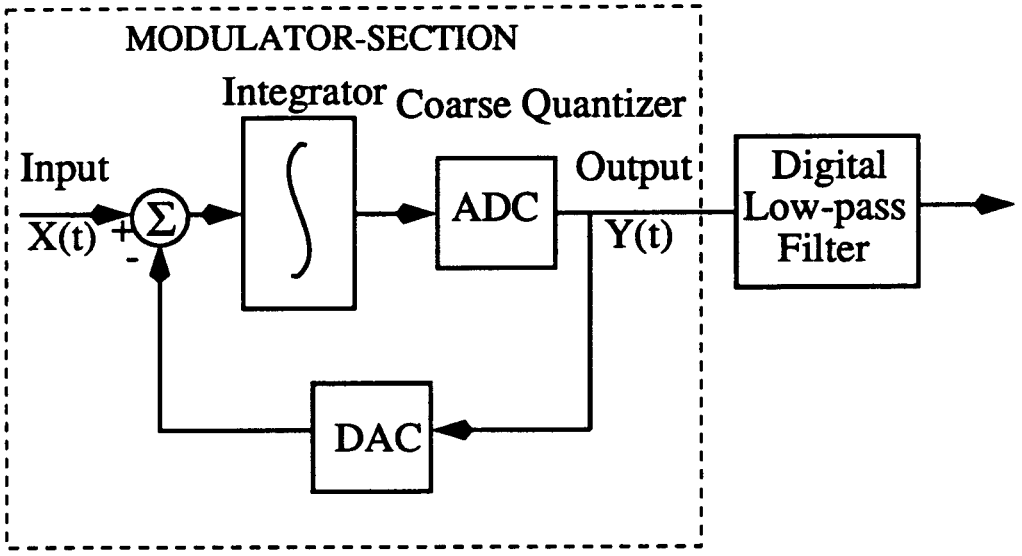

Figure 2.1. Block diagram of a first-order ΣΔ converter.

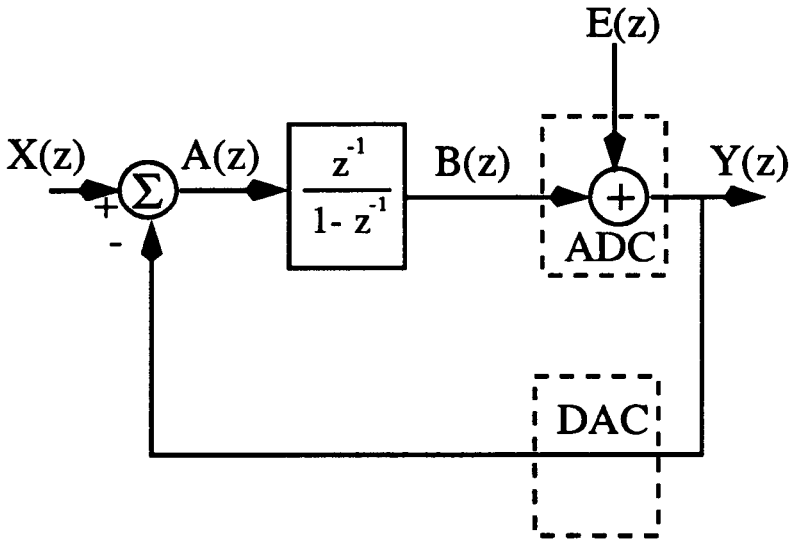

Figure 2.2. Discrete-time representation of a first-order ΣΔ modulator.

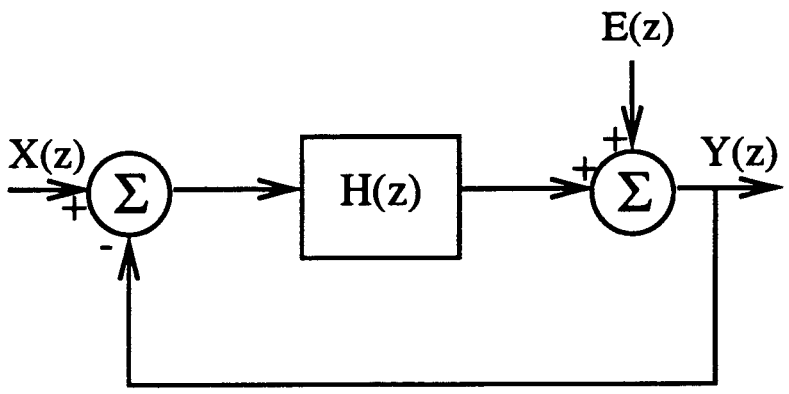

Figure 2.3. Linear feedback-system analogy for noise-shaping loop of a ΣΔ modulator.

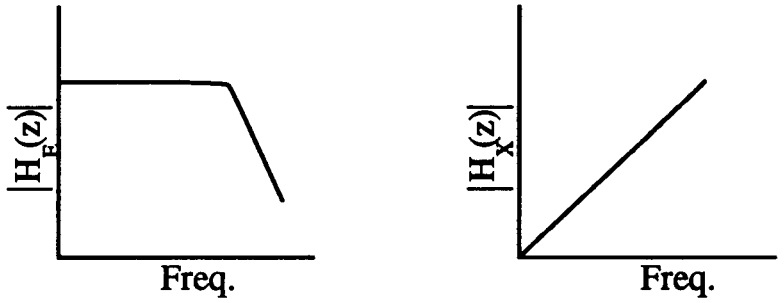

Figure 2.4. Frequency response of $|H_X(z)|$ and $|H_E(z)|$.

This is analogous to a linear feedback filter based on the additive quantization error model [17] as shown in Fig 2.3. The overall output of the modulator is,

$$Y(z) = \underbrace{\frac{H(z)}{1+H(z)}}_{H_X(z)} \cdot X(z) + \underbrace{\frac{1}{1+H(z)}}_{H_E(z)} \cdot E(z),$$

where $H_X(z)$ is the *signal transfer function* and $H_E(z)$ the *noise transfer function*, which link the output to the signal input and to the quantization noise, respectively. Figure 2.4 illustrates how a low-pass frequency response in H(z) causes white quantization error, E(z) to produce a high-pass spectrum. Thus, ΣΔ modulators are also called "noise-shaping" coders.

Finally, the decimator suppresses frequencies above the baseband of interest to yield a finer resolution digital replica of the analog input, but at a reduced rate.

Table 2.1. Design objectives.

Power Dissipation	1mW
Resolution	14 bits
Conversion Rate	10 KHz

Our design objectives are listed in Table 2.1. To achieve a resolution of 14-bits with a first-order modulator, prohibitively large oversampling ratio is needed. Consequently, higher-order architectures were considered for this design.

2.1 The Higher-order (Embedded) $\Sigma\Delta$ Modulator

To obtain moderate performance from a first-order modulator, prohibitively large oversampling ratios are needed. The recent drive toward increasing the bandwidth of converters makes large OSRs impractical. In higher-order loops, the quantization noise is shaped by a higher-order filter which suppresses the quantization noise at low frequencies and causes it to rise more sharply at higher frequencies.

The embedded structure is shown in Fig. 2.5. This architecture is characterized by several cascaded first-order integrators combined with a ADC and DAC.

An issue associated with higher-order loops is stability [5]. Instability results when at any instance, the signal-level (amplitude) exceeds the maximum tolerable limit and overloads the following stage in the structure. This can be prevented by

1. Minimizing delays in the loops,

2. Lowering integrator gains, and

3. Employing multibit quantization.

Including a delay in each integrator allows all integrators to have one clock cycle settling time, but it also jeopardizes system stability. On the other hand, having

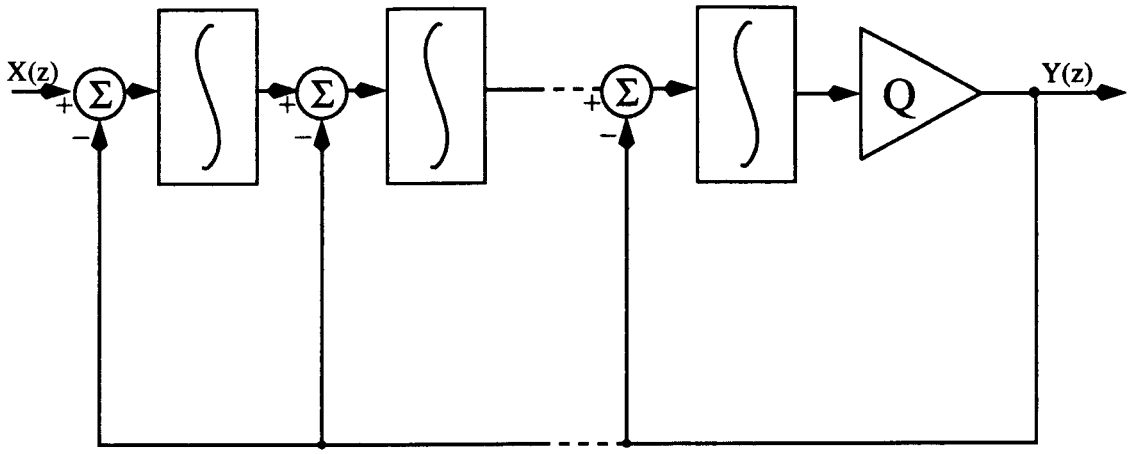

Figure 2.5. Higher-order (embedded) ΣΔ modulator.

delayless integrators imposes fast settling requirements on the op-amps. This is due to the fact that delayless signal paths result in bandwidth shrinkage [Appendix B] of the system. Consequently, to compensate for the loss of bandwidth, faster integrators are required. The speed of the op-amp, which is the key element in the integrator, is proportional to the square-root of the bias current. This implies that to increase the speed by a factor of 2, four times more power is required. Thus, this relationship necessitates including delays in the integrators.

High integrator gains result in the overloading of the integrators. However, choosing low gains helps stabilize the system, but deteriorates the dynamic range (DR). Proper selection of integrator gains to yield a stable system and utilize full dynamic range is critical.

Multibit quantization in higher-order modulators enhance the stability of the higher-order loop as opposed to a 2-level quantizer. Also the increase in DR is achieved which is given by $20 \cdot log_{10}2^{(N-1)}$, where N is the number of bits in the quantizer. Hence, when a 4-bit quantizer is used in lieu of a 1-bit quantizer, approximately 18 dB improvement in DR is possible. This additional DR can only be realized if the feedback DAC is highly linear.

Other higher-order architectures were also explored and simulated. They include

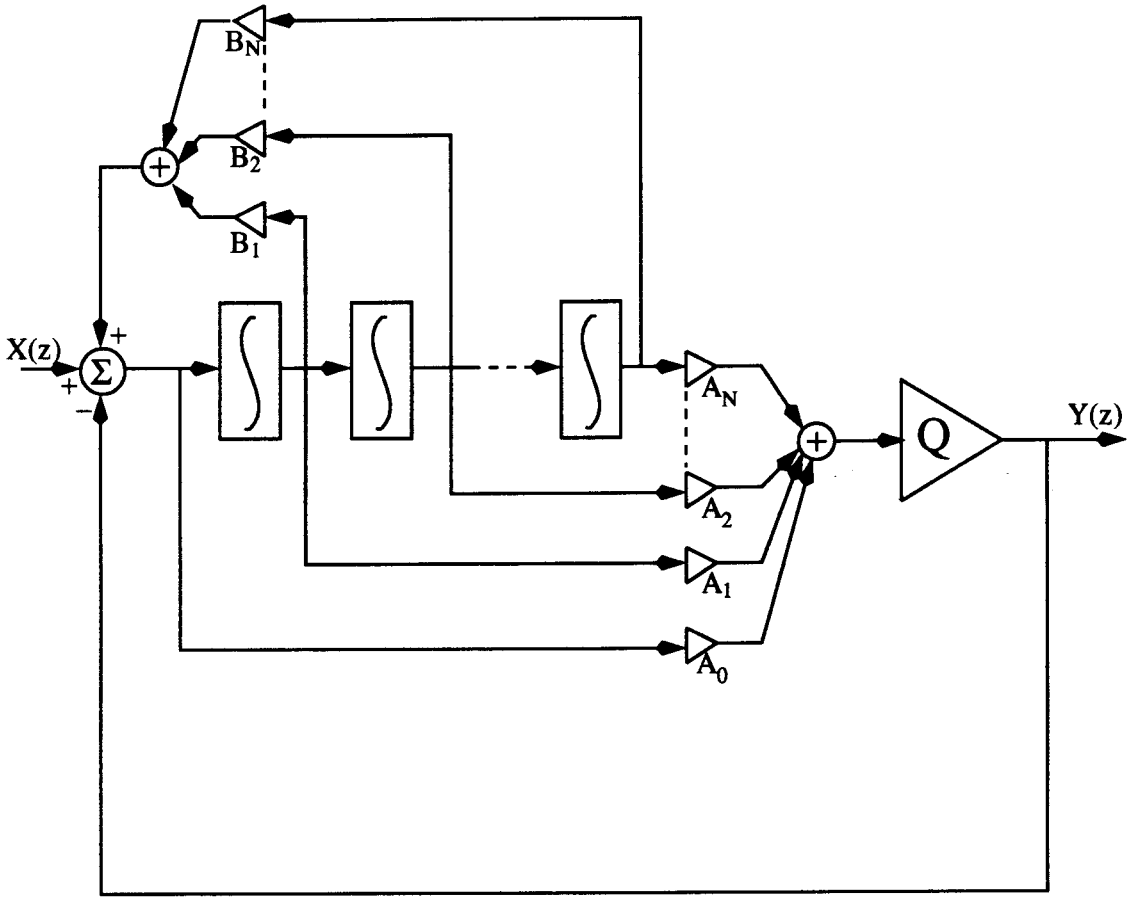

Figure 2.6. N^{th}**-order interpolative structure with feedforward coefficients** $A_0, \ldots, A_N$ **and feedback coefficients** $B_0, \ldots, B_N$**.**

- Interpolative architecture with feedback and feedforward coefficients, and
- MASH structure with a cascaded multibit stage.

2.2 The Interpolative Structure

An N^{th}-order topology is shown in Fig. 2.6 [3]. The interpolative structure is characterized by the feedforward structure with loop coefficients $A_0, \ldots, A_N$ and a feedback structure with coefficients $B_0, \ldots, B_N$. The system output $Y(z)$ can be expressed in terms of the input $X(z)$ and the quantization noise E(z).

$$Y(z) = H_X(z) \cdot X(z) + H_E(z) \cdot E(z), \tag{2.1}$$

where

$$H_X(z) = \frac{\sum_{i=0}^{N} A_i(z-1)^{N-i}}{z[(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}] + \sum_{i=0}^{N} A_i(z-1)^{N-i}}, \tag{2.2}$$

is the signal transfer function, and

$$H_E(z) = \frac{(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}}{z[(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}] + \sum_{i=0}^{N} A_i(z-1)^{N-i}}, \tag{2.3}$$

is the noise transfer function. These transfer functions are derived by assuming that all one-delay integrators are employed and that a z^{-1} delay is associated with the internal ADC. The feedforward and the feedback coefficients allow stabilizing the overall system and also move the quantization noise energy further out of the signal band. This is achieved by choosing the coefficients in such a manner that all system Z-domain poles are inside the unit circle and the zeros are moved away from dc($z = 1$). Treating the loop as a quantization noise filter allows linear filter design techniques to be used to determine the coefficients. Lee *et. al.* chose to use a high-pass Butterworth response to find the A_i's which determines the placement of the poles. The B_i's were found using Chebyshev polynomials for equiripple response. These feedback coefficients, B_i's, move the system transmission zeros away from dc. The system shows close proximity in simulations to the quantitative analysis. With coefficient errors of 5-30 % only a 3 dB loss of SNR is produced. Another major advantage of this architecture is that all N integrators can have delays and still comprise a stable system owing to the fact that the system stability is enhanced by choosing A_i's such that the poles are within the unit circle. However, the main drawback of this architecture is the moderate SNR achieved for low oversampling ratios (OSR). Low OSR is a desirable feature for achieving reasonable conversion rates. The modest performance at low OSRs is due to the fact that the system poles are placed away from the origin of the unit circle and the transmission zeros are moved away from dc. This results in spreading more quantization noise in the baseband before it rises out of the baseband region non-monotonically. Another disadvantage of this structure is the difficulty faced in implementing the loop coefficients as small

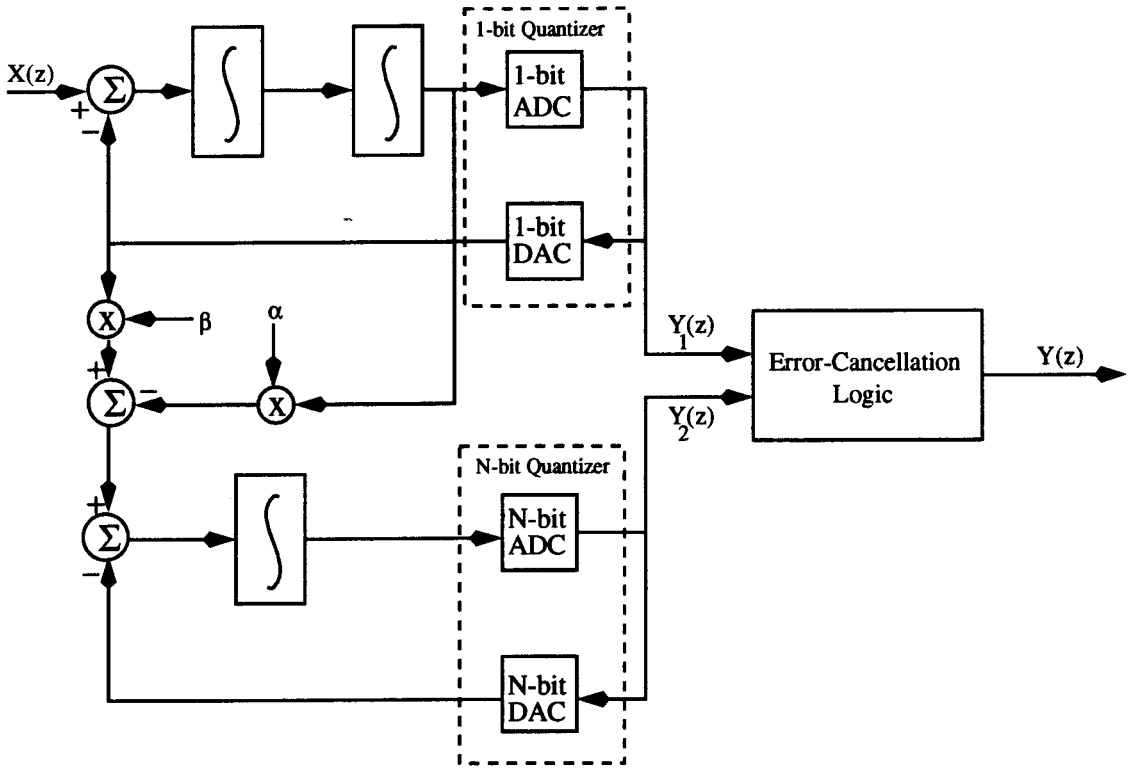

Figure 2.7. Cascaded multibit MASH ΣΔ modulator.

as 10^{-6} on-chip using capacitor ratios. If small coefficients are neglected, it further degrades the system performance. The fourth-order system constructed on a bread-board in [3] uses discrete components and continuous-time integrators. The small values of the coefficients are realizable using discrete resistor ratios, but would be very area inefficient if realized on-chip.

2.3 MASH ΣΔ Modulator with a Cascaded Multibit Stage

The Multi-stAge noise SHaping (MASH) structure is illustrated in Fig. 2.7 [4]. Its salient features are a second-order modulator with a two-level quantizer followed by a first-order modulator with a multibit quantizer comprising the first and the second stages, respectively, of the MASH structure. This architecture is insensitive to the second-stage multibit DAC's non-linearities because the output of the multibit DAC

does not enter the modulator at its input. The more critical first-stage quantizer has a 1-bit DAC and is inherently linear. The input to the second-stage is a weighted difference of the output and the input of the first-stage quantizer. The output of the quantizer is just the sum of its input and the quantization error. This implies that the input to the second stage is the quantization noise from the first-stage. Two coupling coefficients, α and β, which are less than or equal to unity prevent overloading of the second-stage by attenuating large amplitude signals. Error-cancellation logic is incorporated to combine the digital outputs from the two stages. Replacing the quantizers of the two stages by quantization error sources allows the linearized quantitative analysis of the architecture. The output of the first-stage is

$$Y_1(z) = z^{-1} \cdot X(z) + (1 - z^{-1})^2 \cdot E_1(z), \tag{2.4}$$

where $E_1(z)$ is the quantization error of the first stage 1-bit quantizer. Equation (2.4) indicates that the input X(z) gets delayed from the input to the output of the modulator, while the quantization noise of the first-stage undergoes second-order shaping. Assuming that $E_2(z)$ and $E_D(z)$ represent nonlinearities of the second stage multibit A/D and D/A respectively, the output of this stage, $Y_2(z)$ is

$$Y_2(z) = z^{-1}(E_1(z) - E_D(z)) + (1 - z^{-1}) \cdot E_2(z). \tag{2.5}$$

The error cancellation logic combines Eqs. (2.4) and (2.5) according to

$$Y(z) = z^{-1} \cdot Y_1(z) - (1 - z^{-1})^2 \cdot Y_2(z), \tag{2.6}$$

which further gives the overall modulator output as

$$Y(z) = z^{-2} \cdot X(z) + z^{-1}(1 - z^{-1})^2 \cdot E_D(z) - (1 - z^{-1})^3 \cdot E_2(z). \tag{2.7}$$

Equation (2.7) shows that the system output Y(z) is the sum of the delayed input and the quantization noise of the second stage which has undergone third-order shaping. The quantization noise from the first-stage does not even appear at the output of the modulator and gets cancelled at some intermediate stage. A major advantage

of this architecture is that the performance of the third-order noise-shaping sigma-delta is enhanced by a cascaded second-stage with a multibit quantizer in the loop. The increase in dynamic range (DR) is given by $20 \cdot log(2^N - 1)$ dB, where N is the number of bits of the quantizer. Another important feature of this architecture is that the overall system is insensitive to the multibit DAC's non-linearities. As stated before, the objective of this design is to test various dynamic element matching techniques that correct the DAC distortion. With this architecture, the resolution could be increased employing dynamic element matching. However, the embedded architecture provides a better basis for comparing the different DEM techniques because of its higher sensitivity to DAC linearities.

Chapter 3
THE OPTIMAL ARCHITECTURE

After comparing the merits and the drawbacks of the interpolative and the MASH architectures with the higher-order embedded topology, a third-order embedded structure with a 4-bit internal quantizer, shown in Fig 3.1, was chosen to give the desired performance.

3.1 Signal Transfer Function and Noise Transfer Function

A third-order embedded architecture with its switched-capacitor implementation is shown in Fig. 3.2. Based on the timing diagram shown in Fig. 3.3 (b), the signal transfer function and the noise transfer function are derived. Considering the first integrator as shown in Fig. 3.3 (a), during ϕ_2 the input voltage, V_1, is sampled on the input capacitor, C_1, while the feedback capacitor, C_2, retains its charge from the previous phase. Thus, during ϕ_2 the total charge in the first integrator is,

$$Q(t-\frac{T}{2}) = C_1 \cdot V_1(t-\frac{T}{2}) + C_2 \cdot V_2(t-\frac{T}{2}).$$

And during ϕ_1, C_1 samples the feedback voltage V_5 and the first integrator integrates the input charge to its output. The total charge during ϕ_1 is

$$Q(t) = C_1 \cdot V_5(t) + C_2 \cdot V_2(t-\frac{T}{2}).$$

The charge on C_1 and C_2 is conserved during both phases. Hence,

$$C_1 \cdot V_1(t-\frac{T}{2}) + C_2 \cdot V_2(t-\frac{T}{2}) = C_1 \cdot V_5(t) + C_2 \cdot V_2(t-\frac{T}{2}).$$

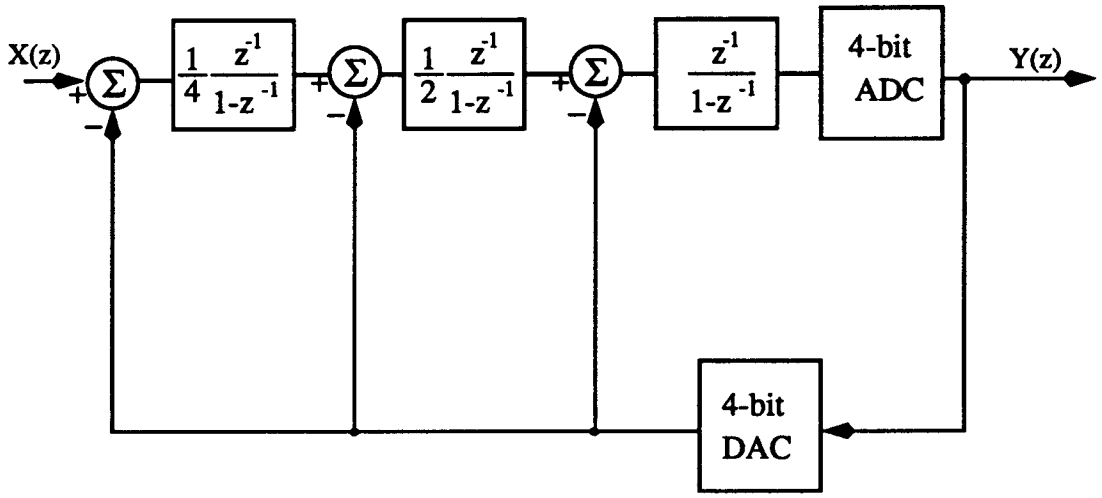

Figure 3.1. A third-order embedded architecture with a 4-bit in-loop quantizer.

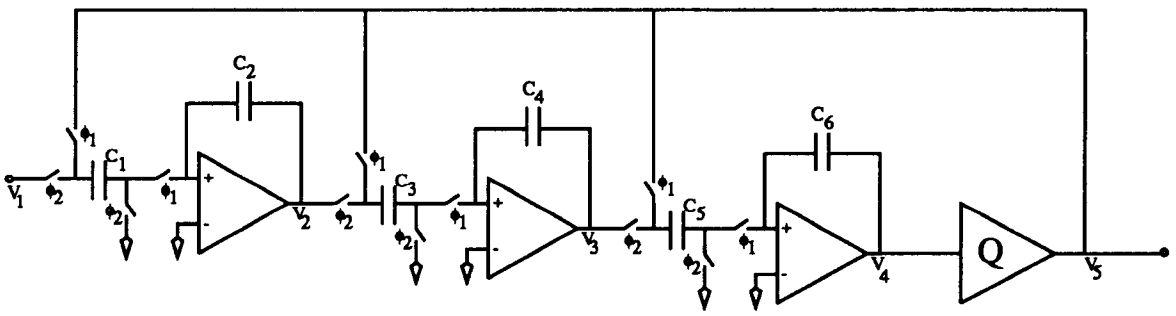

Figure 3.2. Switched-capacitor implementation of the third-order embedded $\Sigma\Delta$ modulator. ϕ_1 and ϕ_2 are the two non-overlapping clocks as shown in Fig. 3.2(b).

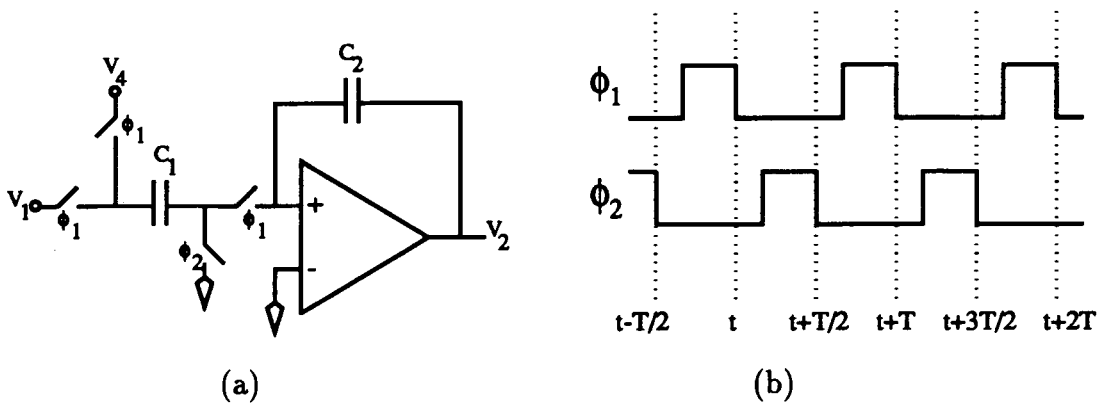

Figure 3.3. (a)First integrator's schematic and, (b) The timing diagram.

Translating the above time-domain equation into Z-domain yields

$$C_1 \cdot z^{-1/2} \cdot V_1(z) + C_2 \cdot z^{-1/2} \cdot V_2(z) = C_1 \cdot V_5(z) + C_2 \cdot z^{-1/2} \cdot V_2(z),$$

$$C_2 \cdot (1 - z^{-1}) \cdot V_2(z) = C_1 \cdot z^{-1} \cdot V_1(z) - C_1 \cdot z^{-1/2} \cdot V_5(z).$$

Solving for V_2 we get

$$V_2(z) = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_1(z) - \frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1 - z^{-1}} \cdot V_5(z). \tag{3.8}$$

Since all three integrators employ a similar clocking scheme, we can write voltages at the outputs of the 2^{nd} and the 3^{rd} integrators as

$$V_3(z) = \frac{C_3}{C_4} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_2(z) - \frac{C_3}{C_4} \cdot \frac{z^{-1/2}}{1 - z^{-1}} \cdot V_5(z), \tag{3.9}$$

$$V_4(z) = \frac{C_5}{C_6} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_3(z) - \frac{C_5}{C_6} \cdot \frac{z^{-1/2}}{1 - z^{-1}} \cdot V_5(z). \tag{3.10}$$

The quantizer is assumed errorless and so $V_4 = V_5$. Substituting $V_3(z)$ and $V_2(z)$ from Eqs. (3.8) and (3.9), respectively, into Eq. (3.10) yields

$$V_4(z) \cdot \{(z-1)^3 + \frac{C_1}{C_2}\frac{C_3}{C_4}\frac{C_5}{C_6} \cdot z^{1/2} + \frac{C_3}{C_4}\frac{C_5}{C_6} \cdot z^{1/2}(z-1) + \frac{C_5}{C_6} \cdot z^{1/2}(z-1)^2 = \frac{C_1}{C_2}\frac{C_3}{C_4}\frac{C_5}{C_6}.$$

The ratio $V_4(z)/V_1(z)$ is the signal transfer function (STF) of the overall system. Rewriting the above equation gives

$$\frac{V_4(z)}{V_1(z)} = \frac{C_1C_3C_5}{C_2C_4C_6} \times \tag{3.11}$$

$$\frac{z^{-3}}{z^{-4}(\frac{C_1}{C_2}\frac{C_3}{C_4}\frac{C_5}{C_6} - \frac{C_3}{C_4}\frac{C_5}{C_6} + \frac{C_5}{C_6}) - z^{-3} + z^{-2}(\frac{C_3}{C_4}\frac{C_5}{C_6} + 3 - 2 \cdot \frac{C_5}{C_6}) - 3z^{-1} + (1 + \frac{C_5}{C_6})}.$$

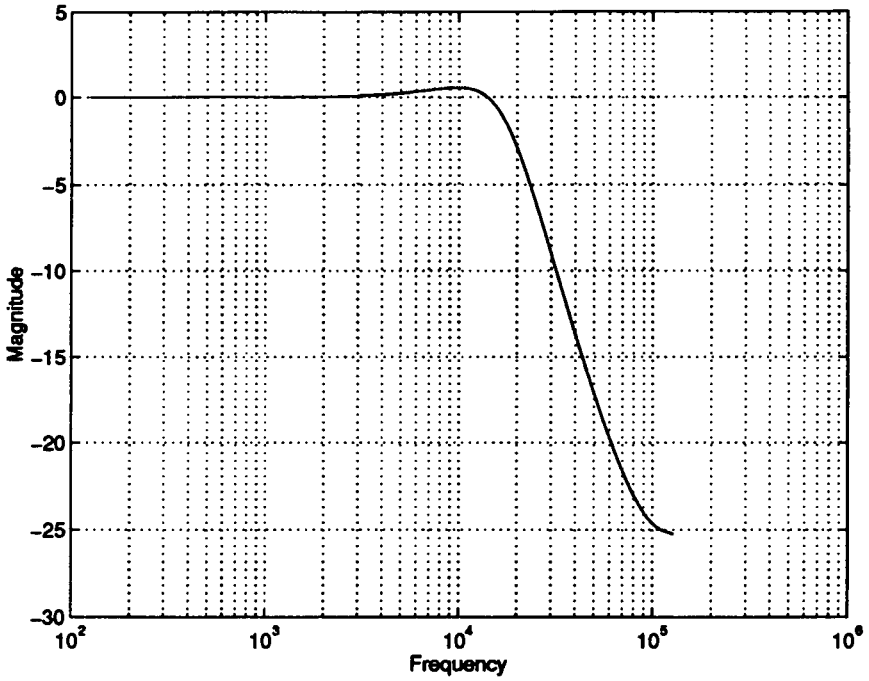

Figure 3.4. Signal transfer function of the 3^{rd} order $\Sigma\Delta$ modulator with f_{clk} of 256 KHz.

A plot of the signal transfer function is shown in Fig. 3.4. The signal has flat characteritics at low frequencies while attenuates at higher frequencies. As apparent from Eq. (3.12), the pipelined implementation of this architecture results in one clock period delay per integrator.

For the derivation of the noise transfer function, an additional error source is added in place of the quantizer as shown in Fig. 3.5 and the input is grounded. This source represents the quantization noise W(t). Based on the timing diagram shown in Fig. 3.3 (b), for the first integrator during ϕ_2, we have,

$$Q(t - \frac{T}{2}) = C_2 \cdot V_2(t - T).$$

During ϕ_1,

$$Q(t) = C_1 \cdot V_4(t - \frac{T}{2}) + C_1 \cdot W(t) + C_2 \cdot V_2(t - \frac{T}{2}).$$

$V_5(t) = W(t) + V_4(t)$. Again equating the two equations since the charge during both phases is conserved, then translating the resulting equation into Z-domain and

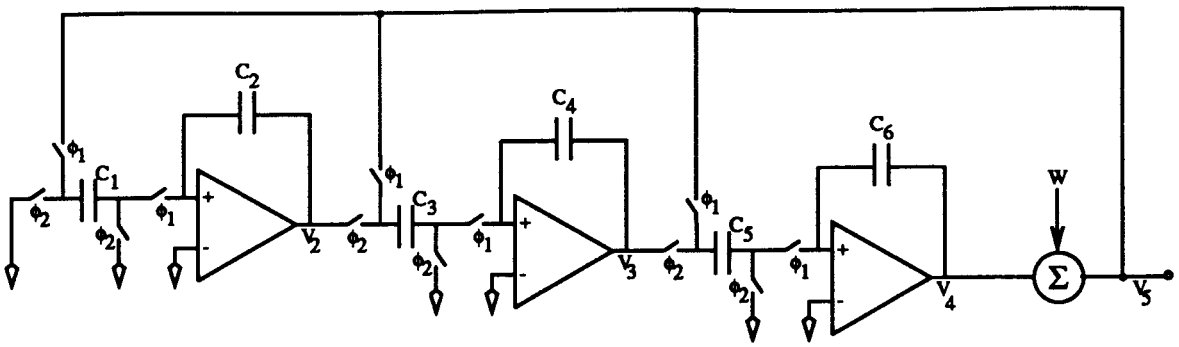

Figure 3.5. Third order switched-capacitor implementation with the quantizer replaced with a quantization error source W.

solving for V_2 gives

$$V_2(z) = -\frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1-z^{-1}} \cdot V_4(z) - \frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{1-z^{-1}} \cdot W(z). \tag{3.12}$$

Similarly, V_3 and V_4 are determined as,

$$\mathrm{V_3(z)} = \frac{\mathrm{C_3}}{\mathrm{C_4}} \cdot \frac{\mathrm{z^{-1}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{V_2(z)} - \frac{\mathrm{C_3}}{\mathrm{C_4}} \cdot \frac{\mathrm{z^{-1/2}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{V_4(z)} - \frac{\mathrm{C_3}}{\mathrm{C_4}} \cdot \frac{\mathrm{z^{-1/2}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{W(z)}, \tag{3.13}$$

$$\mathrm{V_4(z)} = \frac{\mathrm{C_5}}{\mathrm{C_6}} \cdot \frac{\mathrm{z^{-1}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{V_3(z)} - \frac{\mathrm{C_5}}{\mathrm{C_6}} \cdot \frac{\mathrm{z^{-1/2}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{V_4(z)} - \frac{\mathrm{C_5}}{\mathrm{C_6}} \cdot \frac{\mathrm{z^{-1/2}}}{1-\mathrm{z^{-1}}} \cdot \mathrm{W(z)}. \tag{3.14}$$

Substituting Eqs. (3.13) and (3.14) in Eq. (3.12) gives the ratio $V_4(z)/W(z)$. Apparently from Fig. 3.5, $V_5(z) = V_4(z) + W(z)$. Thus, the noise transfer function, $V_5(z)/W(z)$ is found as

$$\frac{V_5(z)}{W(z)} = 1 + \frac{V_4(z)}{W(z)}, \tag{3.15}$$

which gives

$$\frac{\mathrm{V_5(z)}}{\mathrm{W(z)}} = \{\frac{-(1-z^{-1})^3}{z^{-4}(\frac{C_1C_3C_5}{C_2C_4C_6} - \frac{C_3C_5}{C_4C_6} + \frac{C_5}{C_6}) - z^{-3} + z^{-2}(\frac{C_3C_5}{C_4C_6} + 3 - 2\cdot\frac{C_5}{C_6}) - 3z^{-1} + (1+\frac{C_5}{C_6})}\}$$

The noise transfer function is plotted in Fig. 3.6. The noise shaping can be seen in this plot. As expected, the quantization noise exhibits high-pass characteristics. At

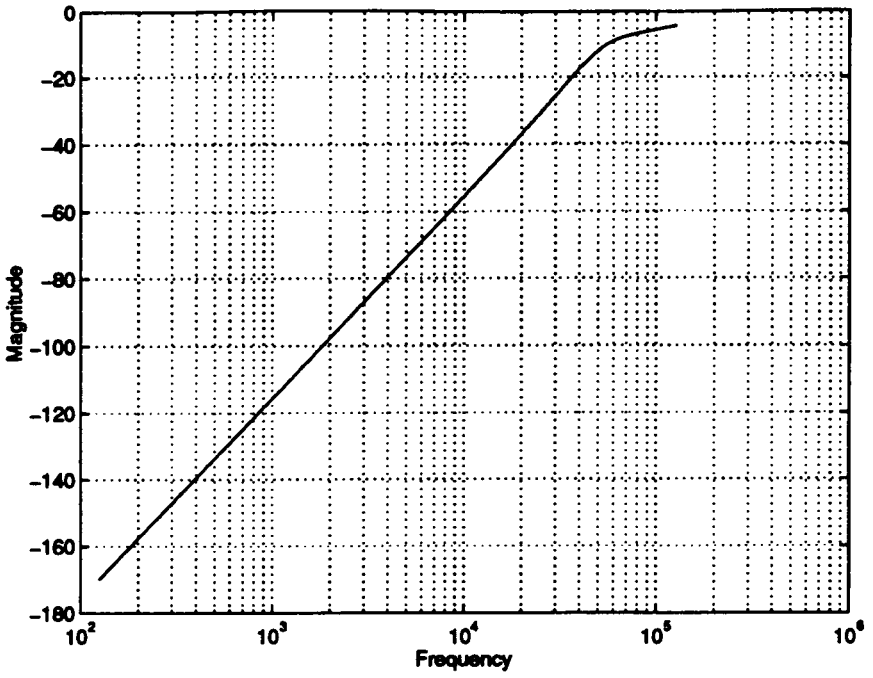

Figure 3.6. Noise transfer function of the 3^{rd}-order $\Sigma\Delta$ modulator with f_{clk} of 256 KHz.

5 KHz, the SNR is approximately 70 dB which is equivalent to a resolution of about 11 bits for for a 10 KHz conversion rate. These plots do not consider the resolution enhancement by the multibit quantizer. An additional 3 bits of resolution is obtained by employing a 4-bit quantizer resulting in a total of 14 bits of resolution. The power spectral density of the output, Y(z), is shown in Fig. 3.7. The input is a sinusoid of frequency 500 Hz. The plot is a result of performing an FFT on a large number of output data points. The high-pass nature of the quantization is seen in this plot.

3.2 Dynamic Element Matching

The main concern with a 4-bit quantizer embedded in the feedback loop of a $\Sigma\Delta$ converter is that the DAC non-linearities due to the element mismatch limit the performance of the modulator. This is because these non-linearities appear at the input of the modulator and do not get shaped like the quantization noise. Various digital

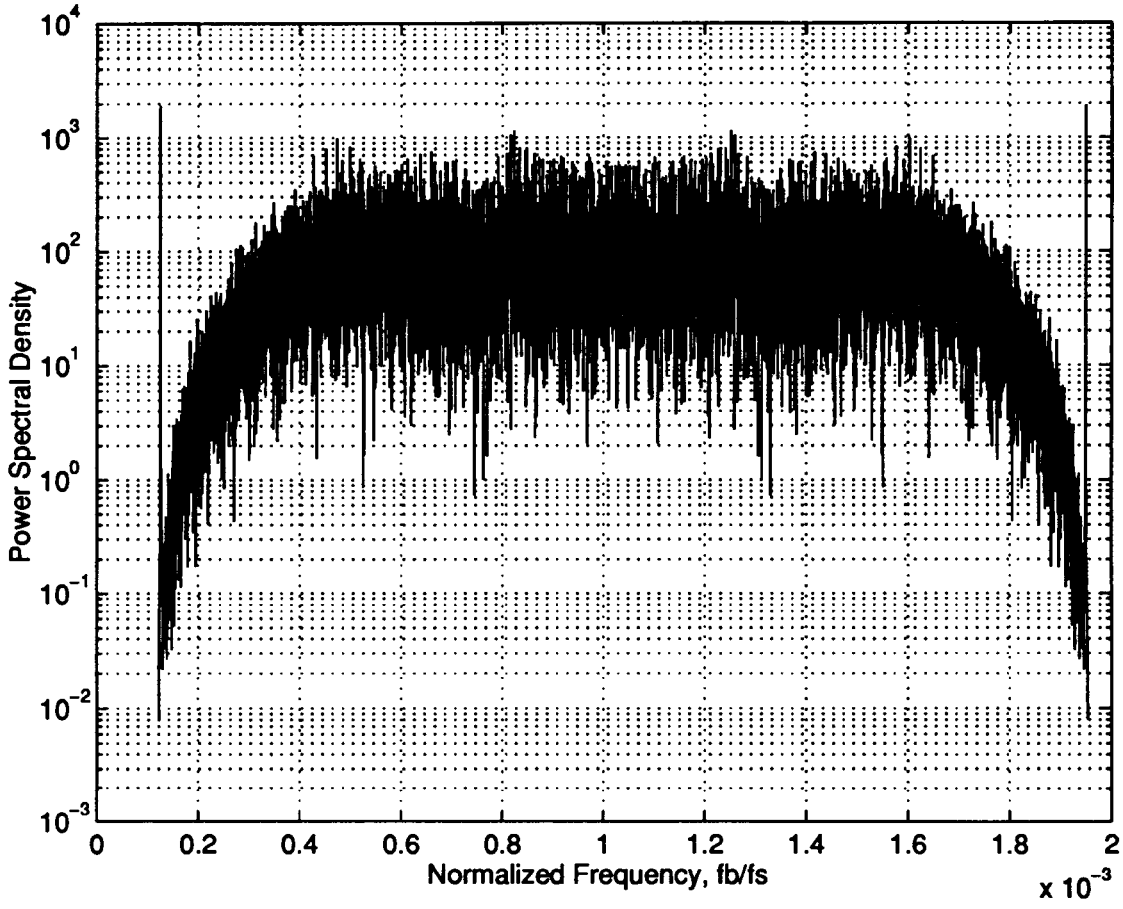

Figure 3.7. Power spectral density of the output, Y(z).

Figure 3.8. DAC output for a 2-element DAC with dynamic element matching.

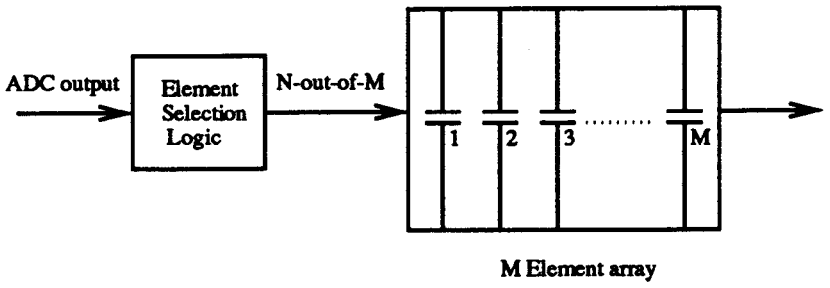

Figure 3.9. Element selection logic implementing various DEM techniques.

self-calibration [9] and dynamic element matching (DEM) techniques [7] [10] [8] have been implemented to correct the DAC errors in $\Sigma\Delta$ modulators. A major disadvantage of digital self-calibration is the significant increase in the digital filter area since the initial filter stages must process more bits.

The basic concept of DEM [16] can be understood by considering a 2-element DAC. Assuming that one element is 1% high and the other one is 1% low, then by alternately selecting the elements results in the average output which is illustrated in Fig. 3.8. All DEM techniques are based on choosing *N-out-of-M* elements for any incoming code. The element selection varies for different algorithms but they all result in redistributing the DAC distortion.

In the randomization technique [7], the output of the internal ADC is fed to the randomizer. This randomizer generates a pseudorandom sequence in which the DAC elements are chosen. Randomization results in converting DAC distortion to white noise and spreads it uniformly over the entire spectrum. The result is an increase in the baseband noise.

Clocked averaging [10] relies on periodically permuting DAC elements at a mini-

mum rate at every clock period. This minimum rate is f_{clk}/(total number of elements, M). Referring to Fig 3.9, first, the top $\frac{M}{2}$ elements are swapped by the bottom $\frac{M}{2}$ elements at a rate of f_{clk}. Then the $\frac{M}{4}$ top elements are swapped by the bottom $\frac{M}{4}$ and so on. Results show that the harmonic distortion have been modulated to mulitple frequencies of f_{clk}/M.

Individual level averaging [6] employs a unique starting index for each DAC input. For instance, if a set of N elements are active for a present code, another set of N elements are selected at the recurrence of the same code the next time. Consequently, if a negative error is introduced for the present input, a positive error is introduced in the next period, nulling the previous one. This averaging over time preserves some of the noise shaping.

Data weighted averaging [8] relies on using all DAC elements at the maximum possible rate by employing a "barrel shifting" algorithm. This is accomplished by sequentially selecting the DAC elements, always beginning with the next available element. Using elements at a maximum possible rate ensures that the DAC errors will quickly sum to zero, moving distortion to higher frequencies. Simulations [8] have shown close proximity in the noise-shaping of a third-order modulator with an ideal DAC and a system that employs data-weighted averaging. Another objective of this project is to verify these simulation results.

3.3 The Test-Chip

Fig. 3.10 is the block diagram of the test-chip. It shows the components that were implemented on-chip interfacing with a micro-controller which is off-chip. The 4-bit output of the ADC is forwarded to a μ-controller. The μ-controller will implement various dynamic element matching algorithms and depending on the code and the algorithm implemented, send 16 control lines back on-chip.

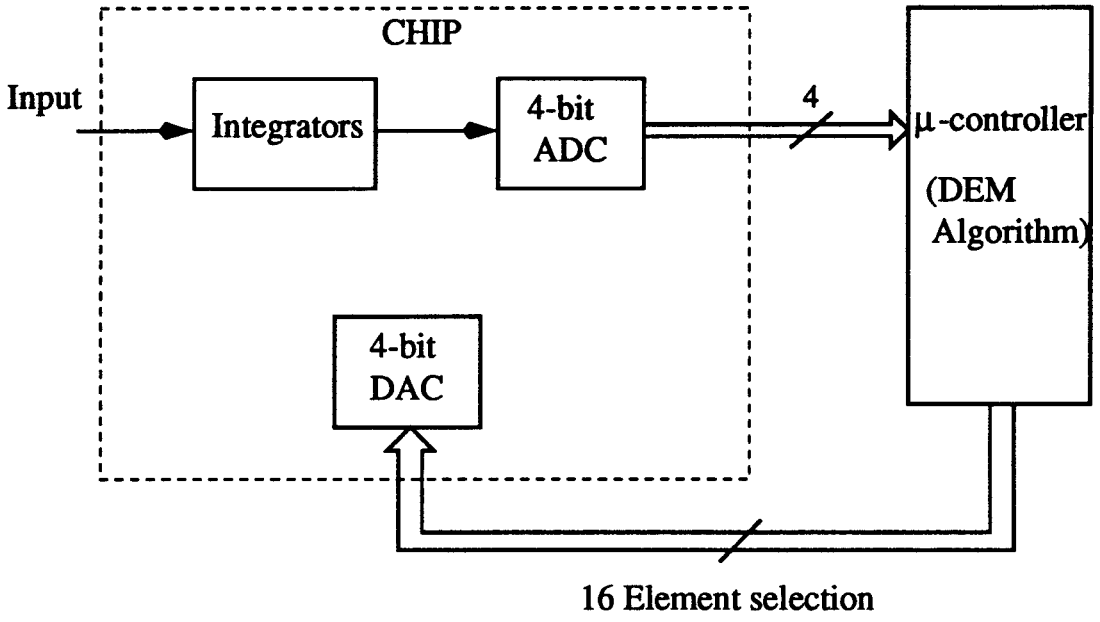

Figure 3.10. The test-chip.

Chapter 4
IMPLEMENTATION

For a given oversampling ratio, R, the quantization noise is approximately given by

$$n_0 = \frac{e_{rms}\pi^N R^{N+\frac{1}{2}}}{\sqrt{2N+1}}, \tag{4.16}$$

$$e_{rms} = \frac{\Delta}{\sqrt{12}}. \tag{4.17}$$

where Δ is the step size of the quantizer and N is the order of the modulator. From the above argument and for R=24, a 3^{rd}-order modulator is chosen to achieve the desired 14 bits of resolution. The design is capable of operating at a supply voltage of 3.0 V while dissipating 1 mW of power. Low power design considerations were emphasized for the realization of the modulator.

4.1 Power Optimization for the Modulator

The rough power distribution estimate for the whole topology is given in Table 4.1. The final power dissipation of the integrator, the ADC and the DAC was different from what shown, but the total dissipation did not increase the budget. The minimum current required in the integrator is a function of slewing and linear settling requirements and the clock frequency determines how fast the integrators must settle. A major power saver is delays in the integrators which allow one clock period settling time for the integrators. A folded-cascode topology is chosen for the amplifier. In such circuits, assuming the maximum amplifier slewing to be $\frac{1}{10}th$ the clock period and requiring 3 τ to settle determines how much current is needed to fulfill large-signal requirements. The bias current is,

$$I_{bias} = \frac{P_{mod}}{V_{supply}}, \tag{4.18}$$

Table 4.1. Power budget (V_{dd} = 3V).

Components	Power(in μW)
Integrators	250
4-bit Flash ADC	250
4-bit DAC	250
Digital Filter	250

and the slew rate of the amplifier is,

$$SR = \frac{I_{bias}}{C_L}. \tag{4.19}$$

To minimize the slewing time of the amplifier, smaller values of load capacitance are desirable but the lower bound of the capacitance value is set by the kT/C noise. The effective bandwidth of the amplifier is,

$$UGF = \frac{g_m}{C_L}, \tag{4.20}$$

and the open-loop gain is,

$$A_{dc} = \frac{g_m}{g_{out}}. \tag{4.21}$$

The above stated calculations give us the specifications of the amplifier.

Another prominent block in the circuit is the 4-bit ADC and DAC. Flash-type ADC and charge-redistribution type DAC are chosen. The flash ADC consists of a resistive voltage divider string which has power dissipation given by,

$$P_{res-string} = \frac{V^2}{R}. \tag{4.22}$$

As apparent from Eq. (4.22), this power dissipated is reduced by choosing large resistors. The power dissipated in the DAC is chiefly due to the charging of the capacitor array and is given by,

$$P_{cap-array} = CV^2 f. \tag{4.23}$$

Table 4.2. Design specifications.

I_{bias}	20 μA
SR	40 V/ μs
UGF	4 MHz
A_{dc}	60 dB
R	2.4 KΩ
C	0.4pF

Small valued capacitors reduce the dissipation but with minimum size, good matching is difficult to obtain. The final choices for the amplifier design and the resistor and the capacitor values for the ADC and the DAC, respectively, are listed in Table 4.2.

4.2 Implementation

Fig. 4.1 shows the fully-differential, switched-capacitor CMOS implementation of the third-order $\Sigma\Delta$ modulator with 4-bit quantizer. It consists of three parasitic-insensitive integrators, a 4-bit ADC and a 4-bit DAC. The fully-differential topology results in increased dynamic range and lowered common-mode noise. The modulator operates on a two-phase non-overlapping clock consisting of a sampling phase and an integration phase as already discussed in a previous section.

4.3 Clocking Scheme

The modulator operates using a two-phase non-overlapping clock scheme as shown in Fig. 4.1. During phase 2, switches ϕ_2 and ϕ_{2d} conduct so that the differential input to the modulator is sampled onto the left plates of the input sampling capacitors, while the right plates are connected to V_{ss}. The comparator is strobed during the same

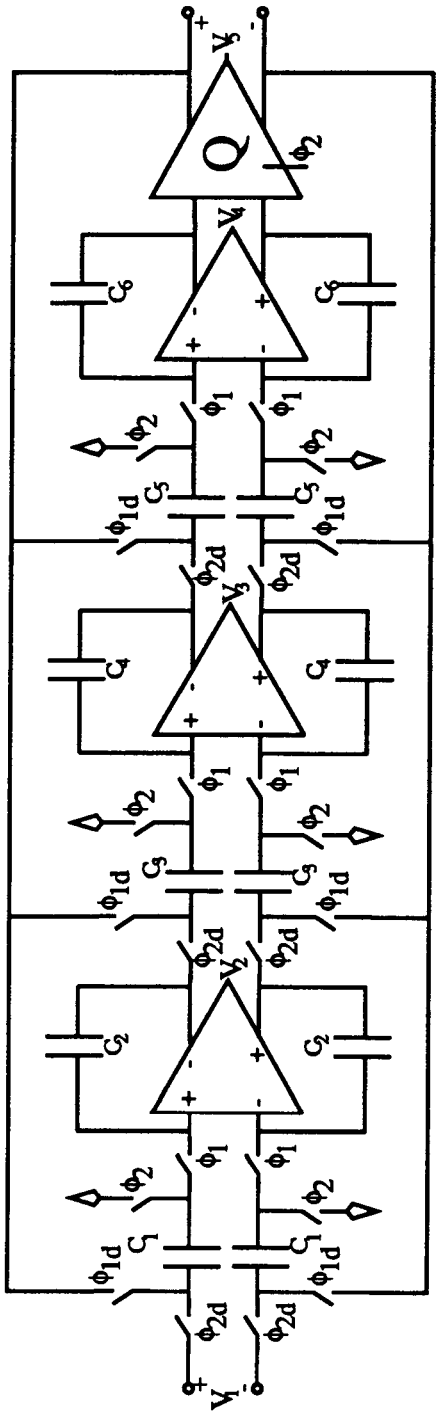

Figure 4.1. Fully differential, switched-capacitor CMOS implementation of the third order $\Sigma\Delta$ modulator with 4-bit quantizer. The capacitor values are $C_1 = C_3 = C_5 = C_6 = 0.5pF$, $C_2 = 2pF$ and $C_4 = 1pF$.

phase 2 when the output of the third integrator is not changing. At the end of phase 2, ϕ_2 is opened slightly ahead of ϕ_{2d} to reduce *signal-dependent charge injection* onto the sampling capacitors. Any residual charge on these capacitors is integrated by the feedback capacitors which can cause overloading of the integrators. But with this topology, since ϕ_1 and ϕ_2 are either connected to V_{ss} or the virtual ground, the capacitors discharge the left-over charge before sampling new one. During phase 1 the output voltage of the feedback DAC is sampled onto the left side of the sampling capacitors and the difference between the input voltage and the feedback voltage is integrated by the feedback capacitor. Again ϕ_1 is opened slightly ahead of ϕ_{1d} to prevent charge injection from the sampling capacitors to the feedback capacitors.

4.4 Integrator Gains

The integrators gains of $\frac{1}{4}$, $\frac{1}{2}$ and 1 are chosen for the first, second and third integrators, respectively. These ratios result in a stable system by ensuring that the signal level at any instance does not exceed and overload the modulator. These gain values were implemented by the capacitor ratios.

The integrators contain an external reset signal for the cases when a large signal appears at the input and saturates the modulator. It is implemented as a switch across the feedback capacitors.

4.5 Capacitors Values and Thermal Noise

The input sampling capacitor being the dominant noise source at the input of the modulator needs careful selection. The thermal noise power is given by

$$\sigma_{th}^2 = \frac{2KT}{C_1}, \tag{4.24}$$

where K is the Boltzmann's constant and T is the absolute temperature. In a conventional $\Delta\Sigma$ A/D converter, this thermal noise is scaled by the oversampling ratio,

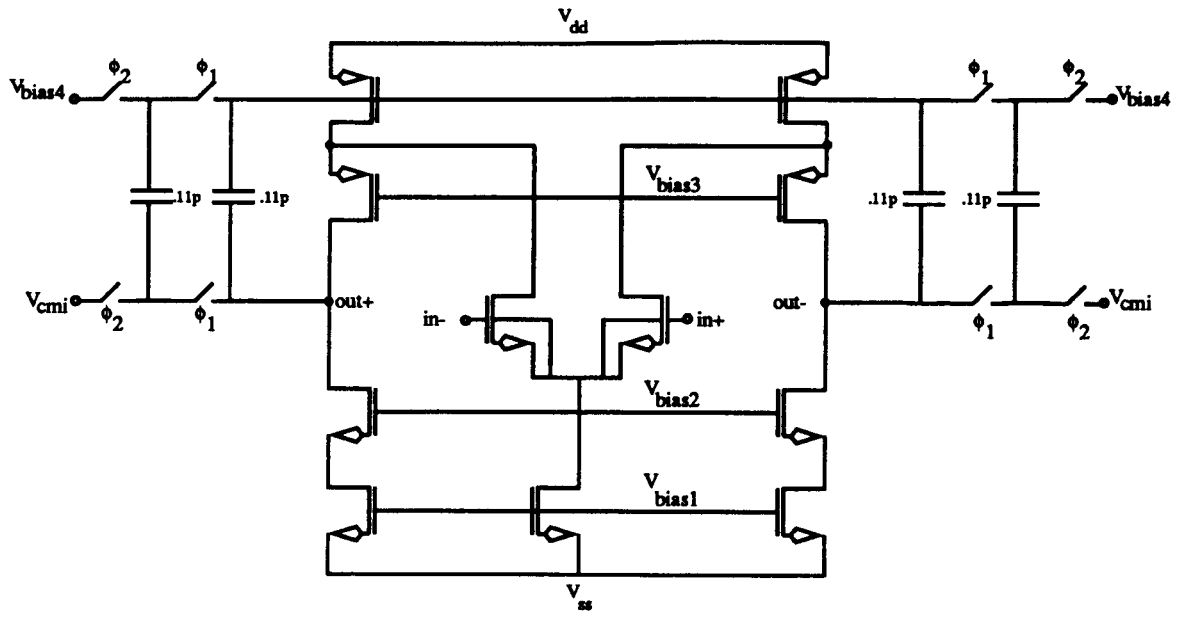

Figure 4.2. Folded-cascode amplifier with dynamic common-mode feedback.

OSR, as

$$\sigma_{th}^2 = \frac{2KT}{OSR \cdot C_1}. \tag{4.25}$$

Therefore, the thermal noise can be reduced by either increasing the value of the sampling capacitor or by increasing the oversampling ratio. Capacitors of 0.5 pF were chosen to give the desired resolution of 14 bits.

4.6 Amplifier

The need for fast settling coupled with a relatively modest gain to suppress leakage of quatization error [1] from the first-stage encouraged the use of a folded-cascode operational amplifier as shown in Fig. 4.2. The common-mode output level of the amplifier is maintained by the switched-capacitor feedback circuitry. All capacitors are equal in value and form a voltage divider to drive the gates of the top PMOS

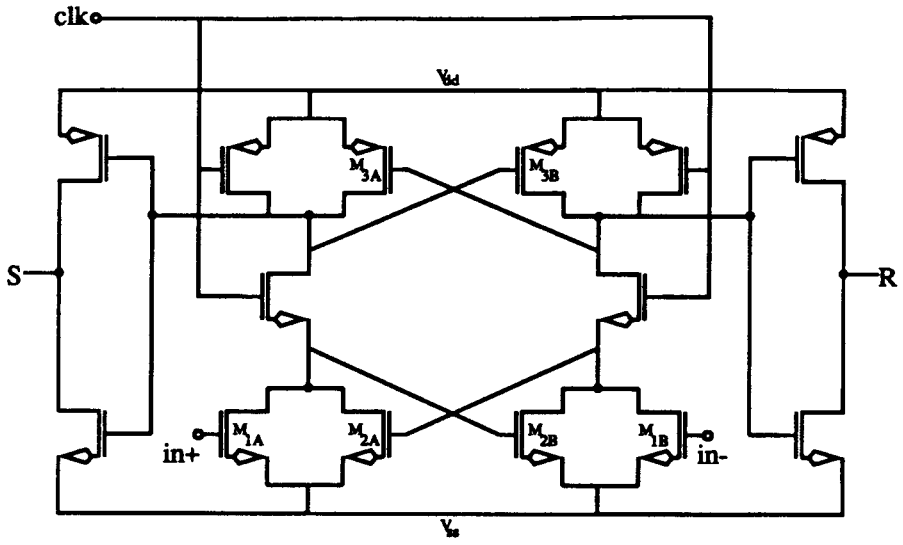

Figure 4.3. Regenerative feedback comparator.

current source transistors. Drifts in common-mode voltage are coupled to this node, which returns the output nodes to the desired level through negative feedback.

4.7 The ADC

A simple regenerative latch shown in Fig. 4.3 is chosen for its high speed. The modulator performance is relatively insensitive to offset and hysteresis of the comparator as the effects of these impairments are attenuated by third-order noise shaping. Nevertheless, the cross-coupled transistors are made large by choosing non-minimum lengths for good matching. Special care was taken in the layout to maintain good symmetry between the two-halves of the latch. The 4-bit flash A/D [4] is shown in Fig. 4.4 with the comparators represented as triangular blocks. The operation of this fully-differential A/D converter is complicated by the fact that it must compare the differential output of the third-stage integrator to fifteen differential reference voltages. This is accomplished by charging fifteen pairs of capacitors to unique differential voltage derived from a reference resistor string during ϕ_1. During ϕ_2, the capacitors sample the output volatge of the third-stage integrator. Fifteen com-

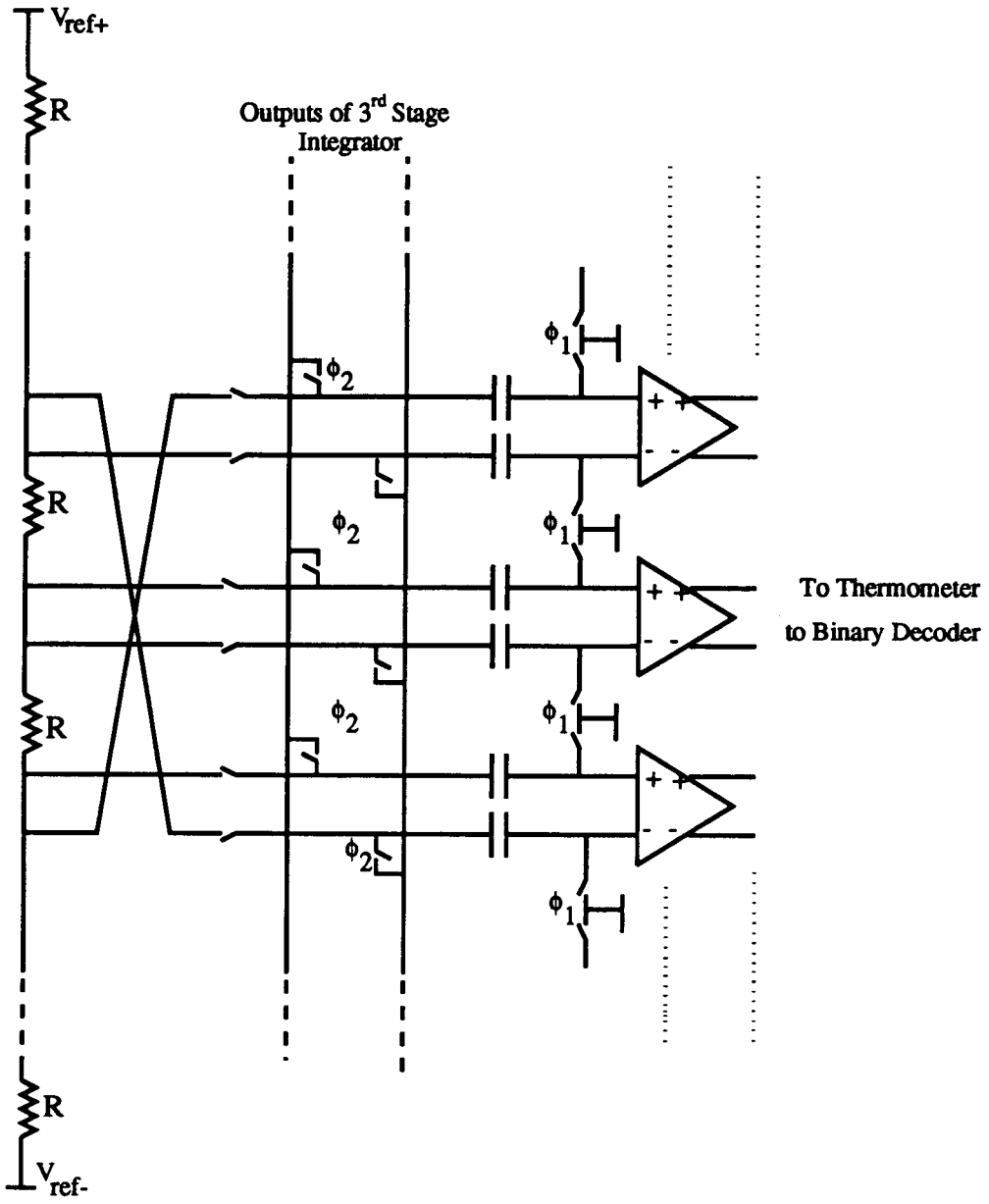

Figure 4.4. Flash A/D converter.

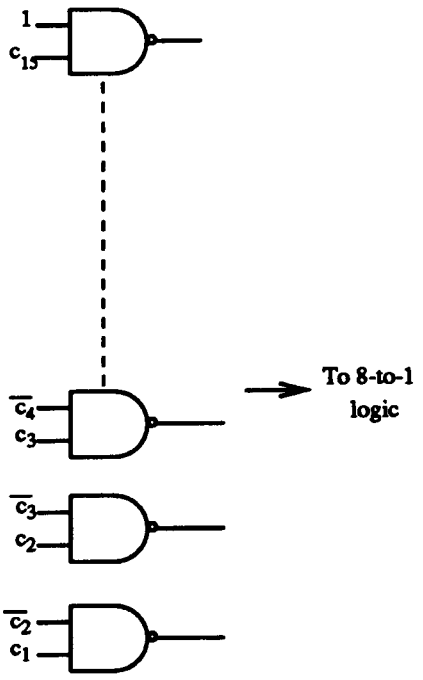

Figure 4.5. Thermometer-to-binary decoder. The four 8-to-1 logic gates produces the 4 output bit words.

parators that are strobed at ϕ_2 perform the comparison and produce a thermometer code for output. This thermometer code is converted to a 4-bit binary word by the thermometer-to-binary decoder shown in Fig 4.5.

4.8 The DAC

Figure 4.6 shows the 4-bit DAC and the off-chip DEM implementation that controls the gates of the switches in the array. Each capacitor charges up to either $+V_{ref}$ or $-V_{ref}$ depending on the incomming code and the implemented DEM algorithm. The operation of the 4-bit DAC is straightforward. The array of capacitors is a voltage divider that depends on the input that closes switches to charge the bottom plates to either $+V_{ref}$ of $-V_{ref}$. For example, if the output of the 4-bit flash is such that 14-out-of-15 plates connect to $+V_{ref}$, then the total charge at point A will be $-\frac{14}{15}CV_{ref}$. This charge is transferred over to the feedback capacitor which brings the output

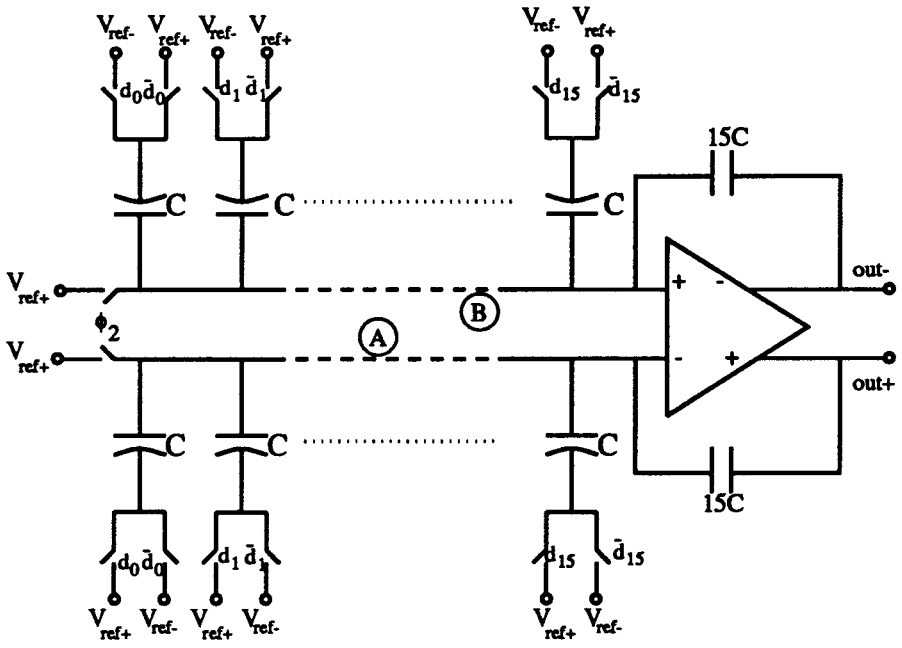

Figure 4.6. Capacitor array type 4-bit DAC.

node to the same voltage as the input with a negative sign. During ϕ_2, the sampling capacitors at the input of the integrators are not sampling the DAC output. So this phase is utilized to reset the capacitors in the array. This is shown in Fig. 4.6 by a switch that connects the top plates to V_{ref} during ϕ_2. The bottom plate switch is controlled off-chip and so can easily be connected to V_{ref} during phase 2. The reason for doing this is that any stray charge trapped between the plates appears as a potential at points A and B. This results in voltage appearing at the nodes which should essentially be the virtual ground. Hence, the capacitor array is reset at the end of each clock phase.

Chapter 5
SIMULATION RESULTS

The third-order modulator with 4-bit internal quantizer was simulated in Spice for one conversion cycle to assess its performance including stability. The simulation was carried out under the conditions stated in Table 5.1. Referring back to Fig. 4.1,

Table 5.1. Simulations conditions.

Supply voltage V_{dd}	3V
Input sinusoid voltage	500mV (−6dB)
Number of bits of the internal quantizer	4
Sampling frequency	256 KHz
Input sinusoid frequency	500Hz

the voltages at outputs of the modulator, first, second and third integrators, V_5, V_2, V_3 and V_4, respectively, are plotted as shown in Fig.5.1(a), (b), (c) and (d). These simulations were done assuming an ideal 4-bit DAC.

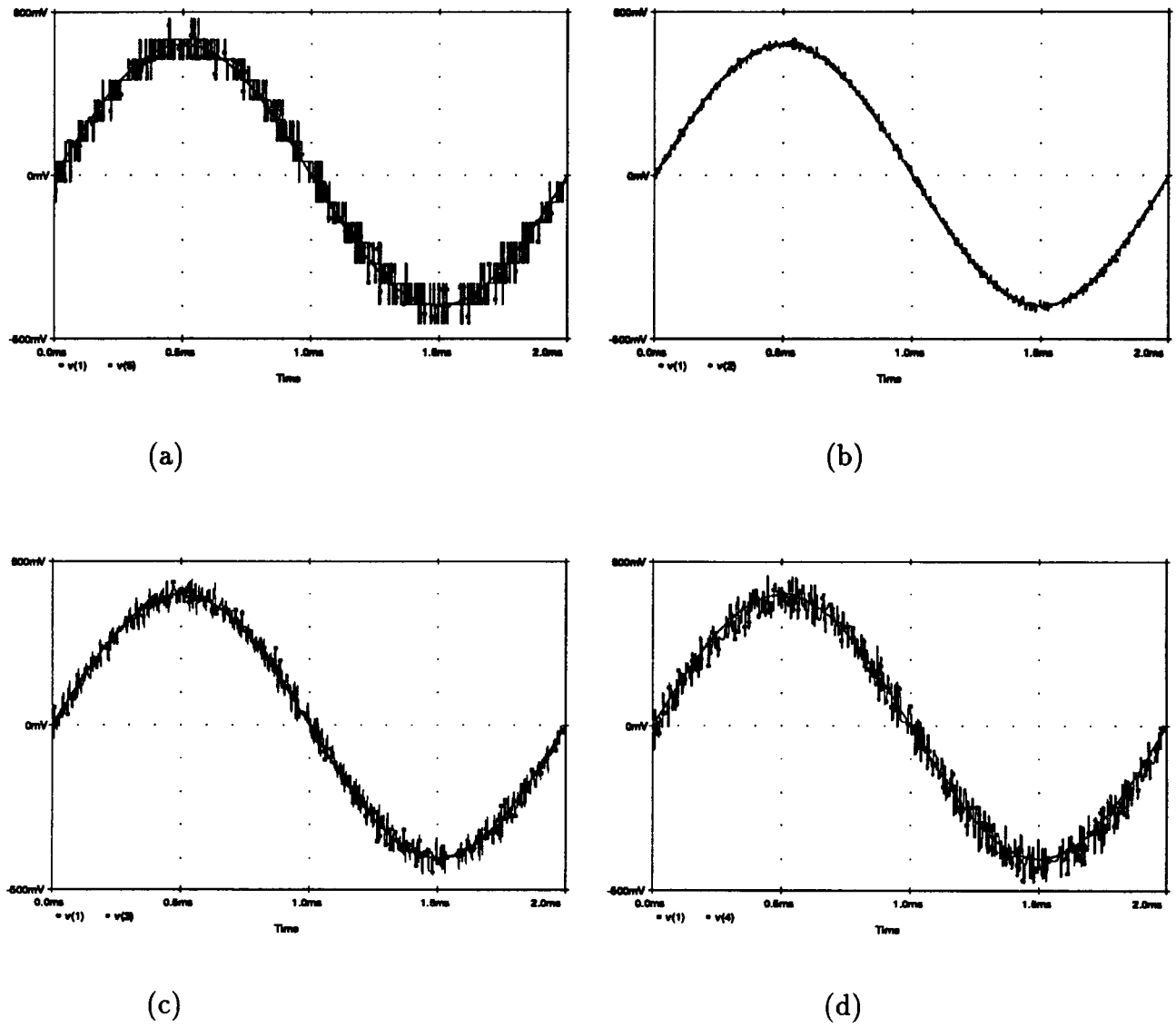

Figure 5.1. Plots showing response at the output of (a) the modulator, (b)the first integrator, (c)the second integrator and (d)the third integrator.

The chip-layout is shown in Fig. 5.2. Special care was taken during the layout to isolate sensitive analog circuitry from switching noise. The layout for the input differential pairs of the op-amps was made inter-digitized for good matching. A serpentine-type resistor string is in the lower left corner of the die.

The 4-bit output of the ADC is taken off-chip and will be forward to a μ-controller. This μ-controller will generate the logic for implementing various dynamic element matching algorithms. Thus, depending on the DEM algorithm, the 16 switches of the DAC will be controlled. In other words, the gates of the MOSFETs that employ the DAC switches will be controlled through external control based on the output of the ADC and the DEM algorithm.

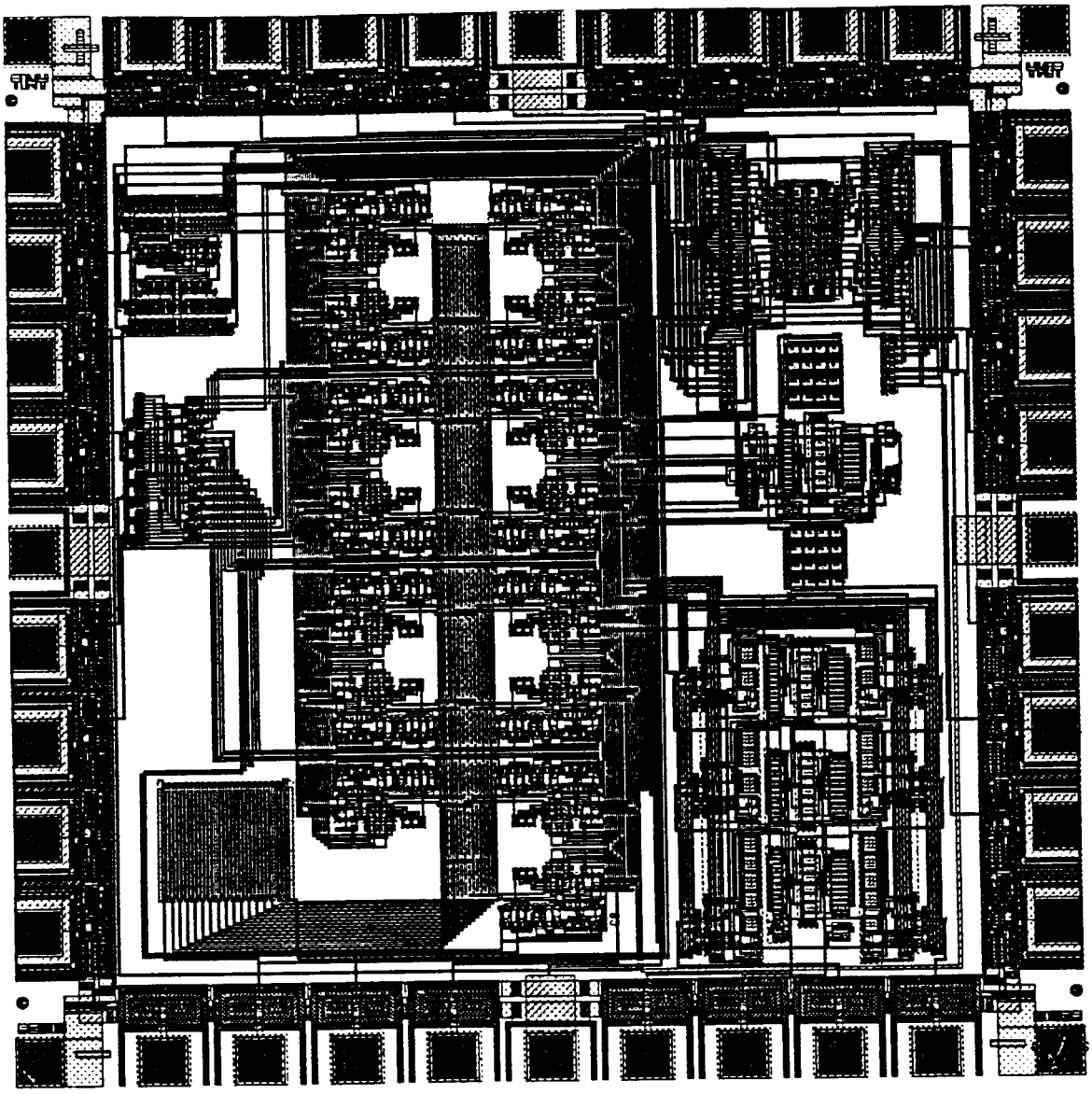

Figure 5.2. Chip-layout.

Chapter 6
CONCLUSIONS

Although single-bit $\Sigma\Delta$ are very attractive for medium-speed and moderate-conversion, their perfomance is not sufficient for low-power and high-resolution conversion. We propose a stable low-power 3^{rd}-order $\Sigma\Delta$ A/D converter with a 4-bit internal quantizer in the feedback loop that provides the flexibility of implementing and testing various dynamic element matching techniques to correct the DAC error. Simulations have shown that a resolution of 11-bits is achieved from a third-order system. A boost in the resolution of 3-bits is obtained by the 4-bit in-loop quantizer. Also some other results that were obtained by investigation are:

- The requirement for the op-amp open-loop gain didn't change by replacing the one-bit quantizer by a multibit quantizer.
- The slew-rate requirement of the op-amp for the 4-bit modulator is more relaxed because each step-size between two quantization levels is smaller.
- Low-power design methodologies were discussed. Various DEM algorithms that will be implemented and tested off-chip were discussed briefly.

The future research consists of testing the chip performance and comparing it with the simulation results. Implementation of the DEM algorithms will be done off-chip and verified on this prototype chip.

The proposed future improvements are the following:

- Implementation of DEM on-chip.
- Exploration of op-amps operating in the subthreshold conduction regions.

- Exploration of use of other types of ADCs, for example successive-approximation type to further reduce the power consumption.

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APPENDICES

Appendix A
Amplifier's Large-Signal Response

When an op-amp experiences a step at its input as shown in Fig. A.1, the output node experiences a sudden voltage change [15]. This is because the input sampling capacitor tries to dump as much charge on C_L as possible in a short period of time. Because of the feedforward coupling, the initial voltage jump is always in the opposite direction of the final voltage which worsens the slewing time. The capacitive voltage divider equivalent circuit of a slewing op-amp is shown in Fig. A.2. The op-amp is removed as V_o is not influenced by the op-amp when slewing. The voltage jump

$$V(0^+) = V_{in} \cdot \frac{C_1 C_2}{C_{in}(C_2 + C_L) + C_L(C_2 + C_1) + C_1 C_2}. \tag{A.26}$$

In order to reduce this voltage jump, a smaller value of C_1 is necessary. However, kT/C_1 and capacitor mismatch issues usually dictate a lower bound for C_1.

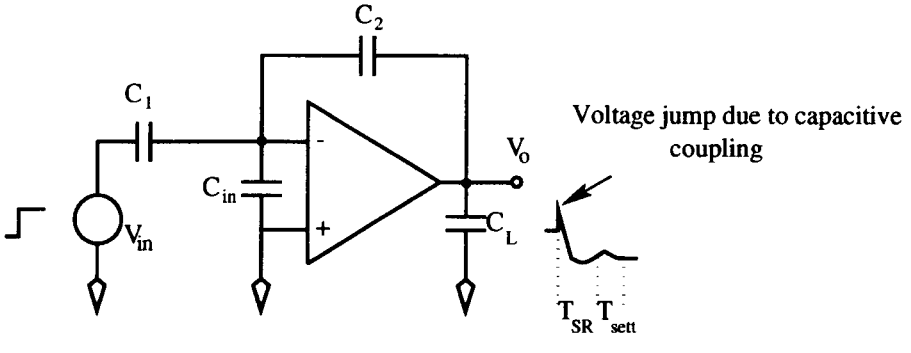

Figure A.1. A slewing op-amp with a large step at the input.

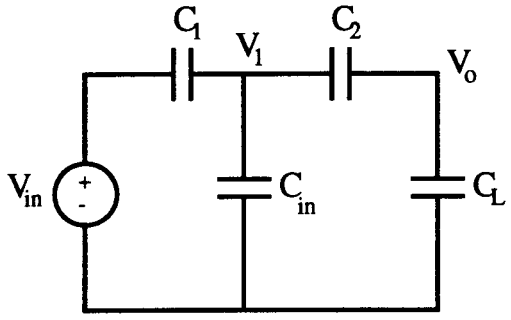

Figure A.2. Equivalent capacitance for a slewing op-amp in SC applications.

Appendix B
Bandwidth Shrinkage in Delay-less Modulators

The small-signal response of an op-amp assuming a single pole system as shown in Fig. B.1, is given as

$$A(s) = -A_0 \frac{1 - s/w_z}{1 - s/w_p},$$

where A_0 is the dc gain of the amplifier and w_z and w_p are the zero and the pole frequencies, respectively. $w_p = w_{-3dB}$. The unity gain frequency of the amplifier, w_0 is found by assuming $w_p \ll w_0 \ll w_z$. Therefore, setting the magnitude of $A(s)$ to unity and substituting $s = jw_0$ leads to

$$|A(w_0)| = 1 \approx A_0 \frac{1}{|\frac{w_0}{w_p}|},$$

which produces

$$w_0 \sim A_0 \cdot w_p.$$

Ignoring the dc-gain for now simplyfies the calculations. Thus, for a single first-order pole system,

$$w_0 = w_p. \tag{B.27}$$

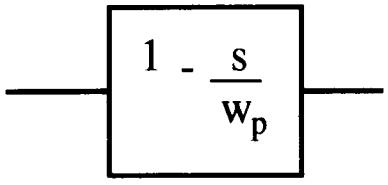

Figure B.1. Single-pole system.

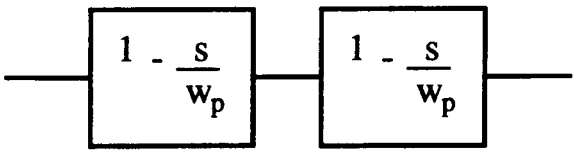

Figure B.2. Two-pole system.

On the other hand, in a system comprising of two op-amps with their dominant poles at the same frequency shown in Fig B.2, $w_p = w_{-6dB}$. This implies that the magnitude of each pole has increased by

$$|1 - \frac{s}{w_p}| = \sqrt{2}.$$

Substituting $s = jw_0$ yields

$$\begin{aligned} 1 + \frac{w_0^2}{w_p^2} &= \sqrt{2}, \\ w_0 &= 0.64 \cdot w_p. \end{aligned} \tag{B.28}$$

Comparing Equations (B.27) and (B.28), the unity-gain bandwidth of the second system has reduced or shrunk by about 36%. This shrinkage in the bandwidth becomes worse if the number of cascaded op-amps is increased. Consequently, higher-order $\Sigma\Delta$ modulators with no delays in their integrators suffer from bandwidth shrinkage which requires the op-amps to be faster than expected. To avoid this undesirable phenomena, higher speed op-amps and hence more bias current is required or alternatively, delays are included in the modulator.

Appendix C
Design Methodologies

C.1 Amplifier

The amplifier was designed to achieve the following

1. A slew rate of $40V/\mu s$.
2. An output swing of $2V$ differentially.
3. An open loop gain of 70dB.
4. Unity Gain Bandwidth of 4MHz.

C.2 Slew Rate

A large time constant for the settling of the integrators is acceptable provided that the settling process is linear [1]. In other words, the settling must not be slew rate limited. There is a sharp increase in quantization noise and harmonic distortion when the slew rate is less that $\frac{1.1\Delta}{T}$, where Δ is the step size and T is the sampling period in seconds. Because of 4-bit quantizer, Δ is 16 times smaller than the Δ of a 1-bit quantizer. Also since the system is clocked at 256KHz, the sampling period is large, thus providing enough time for the amplifier to recover from a large signal.

C.3 Output Swing

The first, second and the third integrator gains of $\frac{1}{4}$, $\frac{1}{2}$ and 1, respectively, result in the clipping of large amplitude inputs. These gain values are chosen to stabilize the

system. However, to use the full dynamic range of the integrators, further clipping is prevented by ensuring good output swing of the amplifier. The cascode transistors at the output stage are made as wide as possible to reduce their V_{Dsat}.

C.4 Bandwidth

If the amplifier is assumed to have a single dominant pole, the impulse response is exponential with time [Boser and Wooley]. Thus, for the first integrator,

$$\tau = \frac{1+\frac{1}{4}}{2\pi f_u}, \tag{C.29}$$

where 1/4 is the gain of the first integrator and f_u is the unity gain bandwidth of the amplifier. In order to guarantee stability of the modulator, the integrator is required to settle within 10% of C_1/C_2, so that

$$1 - e^{\frac{2\tau}{T}} = 0.025. \tag{C.30}$$

For $T = 3.9\mu secs.$, the unity gain bandwidth is estimated as $f_u = 4MHz$. For a folded cascode, the unity gain bandwidth is assumed as,

$$f_u = \frac{g_m}{C_L}, \tag{C.31}$$

where g_m is the transconductance of the input devices. Higher bandwidth than required is not recommended as it results in a great amount of input-referred noise to be aliased in the signal band.

C.5 Open-loop Gain

The open-loop gain of an amplifier is given as,

$$A_v = \frac{g_m}{g_{out}}, \tag{C.32}$$

where g_{out} is the output conductance. The op-amp is designed to have high dc-gain so as to reduce the amount of "integrator leakage". The leakage results in the increase of the in-band noise.

C.6 Final Choices in Amplifier design

The design methodology progressed in the following manner.

1. Input sampling capacitors were chosen equal to 0.5pF to reduce the thermal noise floor allowing 18 bits of resolution.

2. A tail current of 40μA was chosen to keep the power consumption low but ensure that the amplifier is not slew rate limited.

3. The input devices were made non-minimum lengths to minimize offsets due to device mismatches. They were made large also to reduce the amount of input-referred flicker noise and to increase the parasitics at the input node. As discussed in appendix B, large capacitance at the input helps reduce the voltage jump when the amplifier experiences a large input.

Appendix D
Floorplan

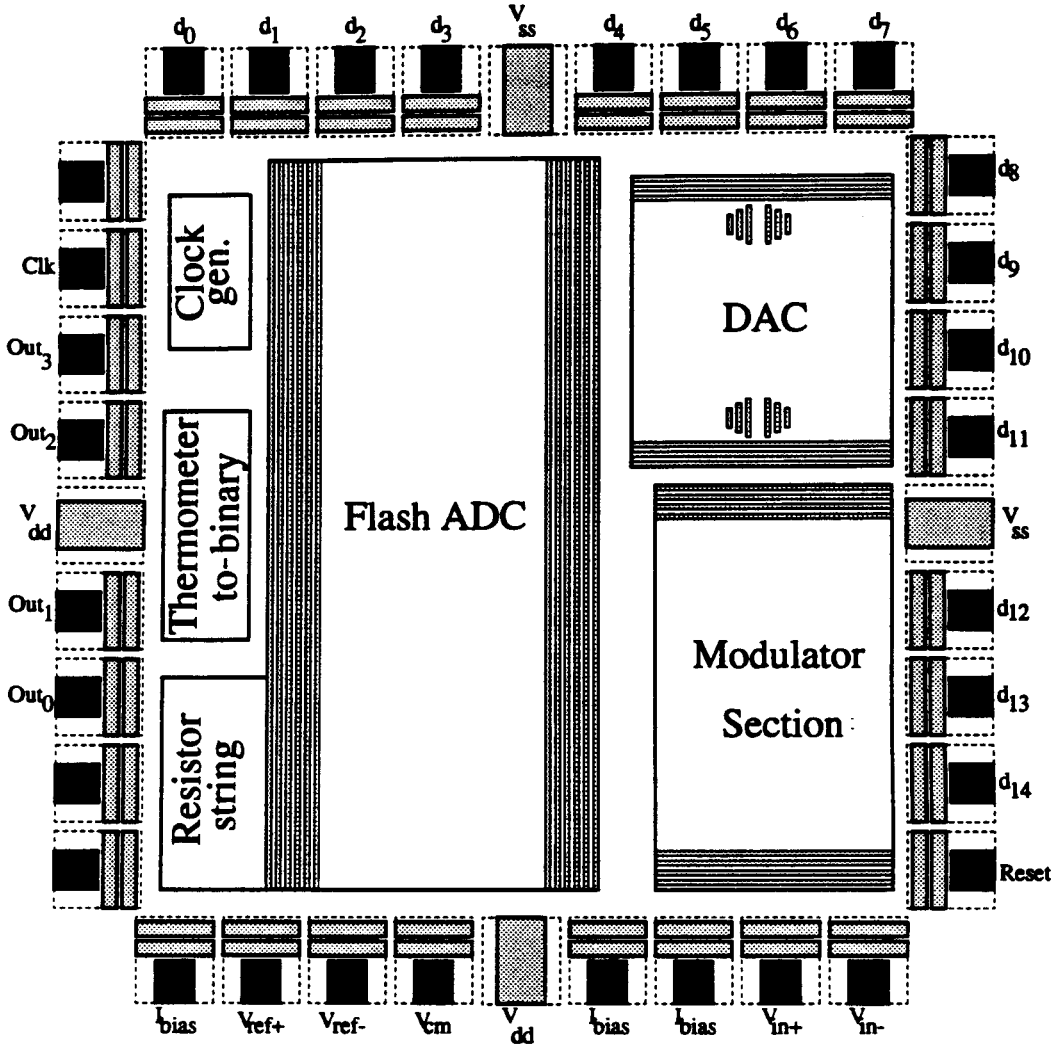

Figure D.1. Floorplan and the pin-assignment