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Title: DESIGN AND SIMULATION OF A DC-TO-DC HIGH-FREQUENCY SERIES-RESONANT CONVERTER

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A DC-to-DC power converter was designed on the basis of pulse-area modulation which is applied to a series-resonant circuit with internal frequency of 10 Khz. The series-resonant circuit was placed directly in the energy path which provides a means for the thyristors to be naturally commutated.

The design was tested by simulation of the converter with the ElectroMagnetic Transients Program (EMTP). It was found that the converter operates only with a unique reference signal (4.0 Amps). Deviations from this signal failed to produce a DC waveform at the

output terminal. This problem is resolved by including a PEAK CURRENT LIMITER to the controller.

DESIGN AND SIMULATION OF A DC-TO-DC HIGH-FREQUENCY SERIES-RESONANT CONVERTER

by

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DESIGN AND SIMULATION OF A DC-TO-DC HIGH-FREQUENCY SERIES-RESONANT CONVERTER

1. INTRODUCTION

A power electronic converter is a device which converts electric energy of a certain form into electric energy of another form. This difference of form pertains to the waveform of voltage and current at the input and the output of the converter. The waveforms of a DC-to-DC converter are essentially DC.

The converter operates with a high internal frequency of 10 Khz in order to exploit the use of modulation processes and replace the need for a bulky and expensive filter to establish the desired output accuracy. The improvement of solid-state switching elements makes the process of high-frequency switching possible, which basically is dependent upon the turn-off characteristic of thyristors. The thyristor or silicon controlled rectifier is a four layer device which consists of three junctions; the gate, anode and cathode [1]. The thyristor can be considered as two transistors: one p-n-p and one n-p-n. The collector of the n-p-n transistor is connected to the base of the p-n-p transistor [2]. Natural

current commutation of the thyristors is obtained by the use of a series-resonant circuit inserted in the direct energy path. The control strategy of the series-resonant converter is based on pulse-area modulation, a concept originally developed at the Delft University of Technology in the Netherlands.

The input voltage is connected to the output terminal through a series-resonant circuit. The input source is also connected to an input low-pass filter capacitor and the input switch matrix. The input switch matrix generates a high-frequency current through the series-resonant circuit. The resonant current is carried through the output switch matrix which detects the desired output waveform through selected rectification. In a one-way energy transfer, the output switch matrix consists simply of a diode bridge. The high-frequency ripple on the rectified resonant current is eliminated by the output low-pass filter capacitor which is connected to the output terminal. The result is a low-frequency output current and an output voltage over the load.

The input switch matrix consists of a combination of four thyristors and four diodes. The diodes are connected antiparallel to the thyristors. When the diodes are conducting, energy is transfered back to the source if the

resonant circuit contains an excess of energy. Another function of the diodes is the minimization of the switching losses during the turn-off process of the thyristors by maintaining the voltage across the thyristor equal to the forward voltage of the diode.

The main part of the converter is the controller. The controller determines the scheduling of the firing signals for control of the energy-flow through the series-resonant current. The control strategy can be heuristically explained as follows.

A current sensor senses the resonant current from the series-resonant circuit and feeds this signal into a summing amplifier. The algebraic sum of this signal with the reference signal is fed through an integrator. The firing signal occurs when the area under the rectified resonant current equals the area under reference current[3]. This causes the rectified resonant current to be proportional to the reference signal with an accuracy determined by the frequency of the resonant current. The higher the frequency, the higher the accuracy. Since the output current for a DC-to-DC converter equals the rectified resonant current, the output current will be proportional to the reference signal. Therefore, the magnitude of the output current is deterministically controlled to follow

the controllable reference signal. The system can be operated either as a current limited voltage source or as a voltage limited current source [4].

Chapter 2 explains the operation and the design of the system. The design consists of four major components: 1) Power circuit, 2) Sensor circuit, 3) Controller, and 4) SCR trigger logic.

Chapter 3 explains the simulation of the system, of which is an important part the design of the PEAK CURRENT LIMITER. The simulation of the system was done by using the ElectroMagnetic Transients Program (EMTP) [5].

2. DESIGN

The DC-to-DC converter can be viewed as consisting of four major components: (1) Power circuit, (2) Sensor circuit, (3) Controller, and (4) SCR trigger logic. These components are schematically depicted as blocks in figure 2.1 and are respectively numbered 60, 50, 70 and 80.

2.1 THE POWER CIRCUIT

The power circuit contains an optocoupler, the switch matrices, the filter capacitors, and a series-resonant circuit. The switch matrix "SM1" consists of the thyristors and diodes, as indicated by blocks 631, 632, 633 and 634. The switch matrix "SM2" consists of a diode bridge. The power circuit of the converter takes care of the bulk energy transfer from input to output.

The semiconductor optocoupler (TIL119) consists of a light sources, usually an infrared emitting diode, and a light detector, usually a silicon semiconductor, coupled by a transparent dielectric path within an nontransparent housing. It is widely used to electrically isolate one portion of an electronic circuit from another while providing one way information flow, via the light beam of

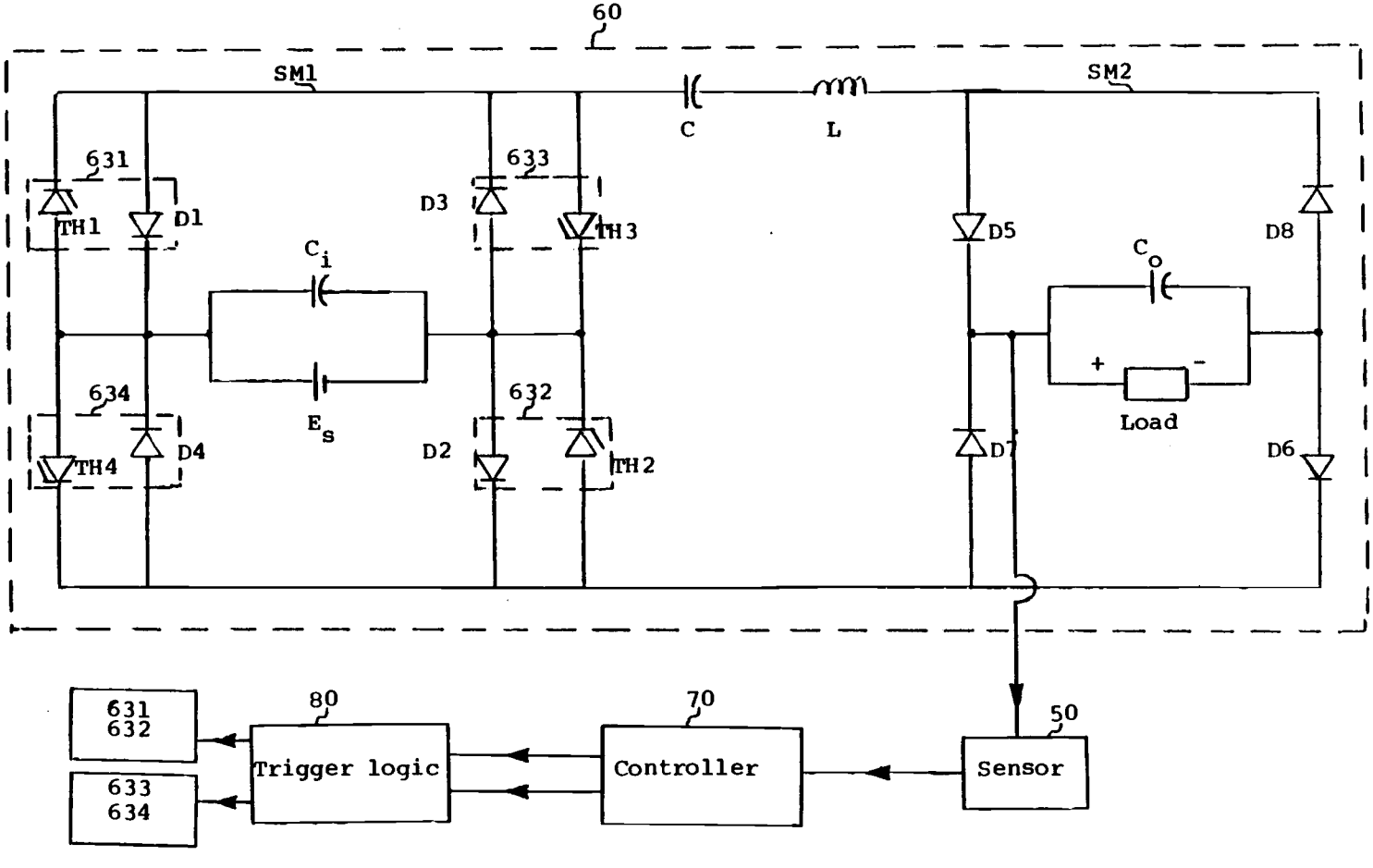


Figure 2.1. The DC-to-DC high-frequency series-resonant converter.

the optocoupler. A pair of thyristor and a diode with the TIL119 is shown in figure 2.1.1.

The current flows from the positive terminal of the voltage source to its other terminal when the thyristors TH1 and TH2 are conducting (refer to figure 2.1). The thyristors conduct until the resonant current changes polarity. Then, the diodes D1 and D2 limit the voltage over their respective thyristors after they are turned off. The magnitude of the voltage-current product during this process is very limited and this results in minimal switching losses. The diodes D1 and D2 continue to conduct until the thyristors TH3 and TH4 receive a signal from the controller to be turned on. The diodes D3 and D4 again limit the voltage over their respective thyristors after they turn off. The sequence of the topological changes caused by changing switch conditions are shown in figure 2.1.2.

We will make the following calculations to find the values of (a) the series-resonant capacitor "C" and (b) the series-resonant inductor "L". It is assumed that the input source is 100 volts DC, the desired output power is 400 watts and the interval frequency is 10 Khz. This frequency is attained at full power operation when the converter operates at its highest efficiency. Thus, the maximum output current is 4 AMPs.

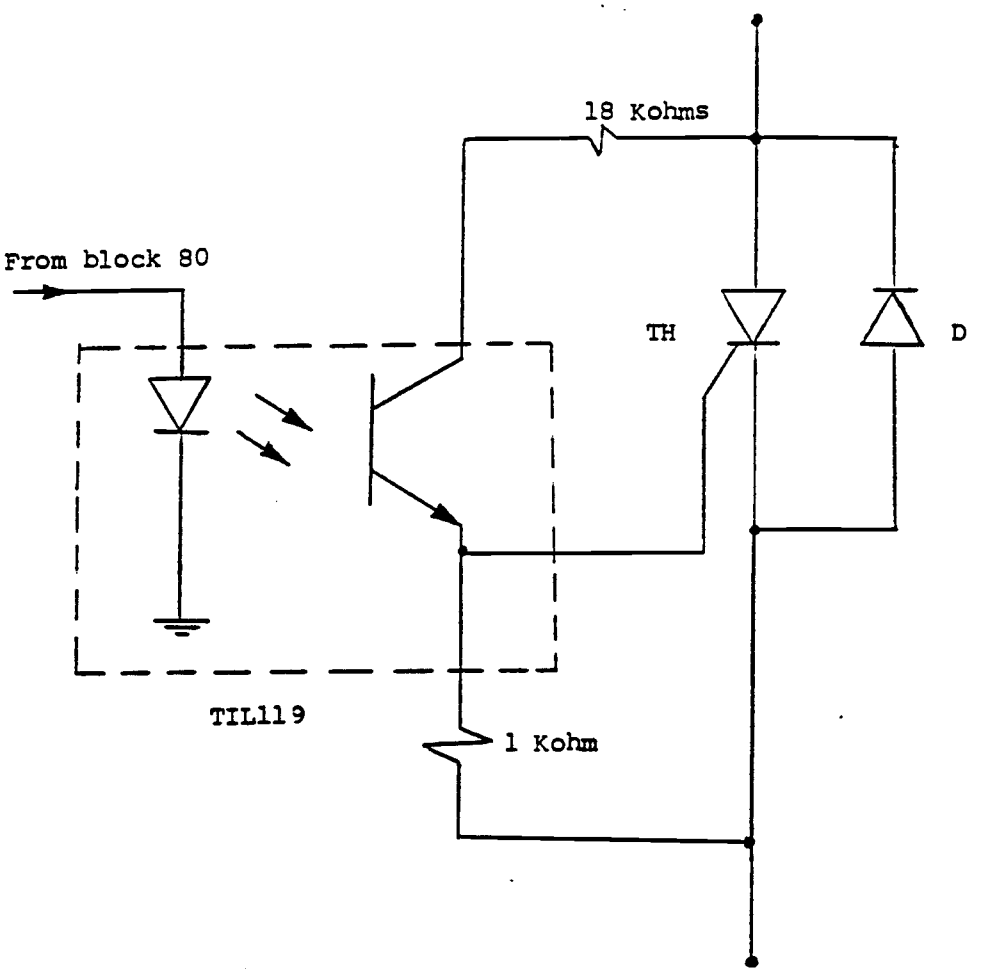


Figure 2.1.1. The protection system for a thyristor and a antiparallel diode.

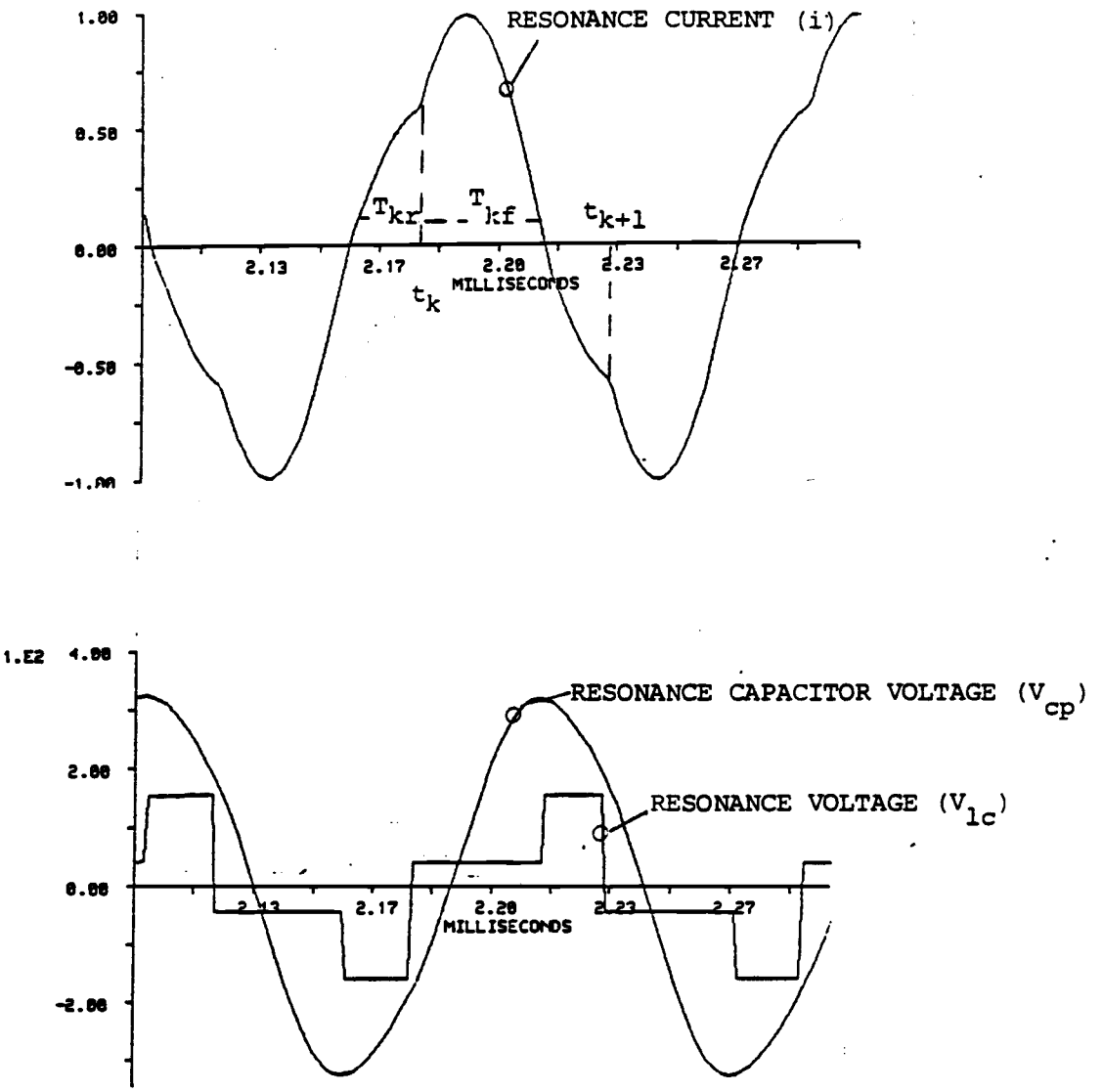


Figure 2.1.2. Expected waveforms for the DC-to-DC converter.

(a) The peak voltage " V_{cp} " of the series-resonant capacitor has to exceed more than the combined voltages of the input source "E_s" and the output voltage "V_o", i.e., when the voltage "V_{lc}" across the series-resonant elements is minimal.

This voltage "V_{lc}" is determined by the switching mode of operation. Thus, when the thyristors are conducting during the time interval T_{kf}, the value of V_{lc} is:

$$V_{lc} = E_s - V_o, \tag{1}$$

and when the diodes are conducting during the time interval T_{kr}, the value of V_{lc} is:

$$V_{lc} = E_s + V_o. \tag{2}$$

V_{lc} is minimum when "E_s" is almost equal to "V_o". This causes the peak voltage over the seies-resonant capacitor to exceed twice the input voltage $V_{cp}>2*E_s$. It follows that the peak to peak voltage of the series-resonant capacitor exceeds the input voltage more than four times ($V_{cpp}>4*E_s$). The relationship between the peak to peak voltage over the series-resonant capacitor and the resonant current is:

$$V_{cpp} = 1/C \int_{t_k}^{t_{k+1}} |i| \, dt \, . \qquad (3)$$

It follows from the above that the series-resonant capacitor (C) is equal to:

$$C = |i|_{avg} * T_{ok} / (4 * E_s). \qquad (4)$$

We need to calculate the values of the average resonant current "$|i|_{avg}$, and the time interval" T_{ok} ".

The series-resonant current must satisfy the following equation at all times:

$$\int_{t_k}^{t_{k+1}} |i| \, dt = K_r \int_{t_k}^{t_{k+1}} i_r \, dt. \qquad (5)$$

This control strategy is called pulse-area modulation. Assuming that the reference current $K_r * i_r$ is constant over the period from t_k to t_{k+1}, this relationship can be rewritten as:

$$|i|_{avg} = K_r * i_r. \tag{6}$$

The magnitude of the output current "i_o" is determined by the reference current $K_r * i_r$ so that:

$$i_o = K_r * i_r . \tag{7}$$

We conclude out of equations (6) and (7) that:

$$|i|_{avg} = i_o = 4.0 \text{ AMP}. \tag{8}$$

The instants of time at which the switches are triggered are defined as:

$$t_{k+1} - t_k = T_{kf} + T_{kr} = T_{ok} . \tag{9}$$

The time interval T_{kf} specifies the time when thyristors 1 and 2, or 3 and 4 are conducting,(see figure 2.1) which occurs when the energy flows from the source to the resonant circuit. The time interval T_{kr} determines the time when antiparallel diodes 1 and 2, or 3 and 4 are conducting and happens during a reversed flow of enery from the resonant circuit to the source. The time ratio of these conduction periods:

$$T_{kr} / T_{kf} \approx 1/4, \tag{10}$$

is a useful value for maximum power operation [6].

By substituting T_{kf} into equation (9), we obtain:

$$T_{ok,min} = T_{kr,min} + 4*T_{kr,min} = 5*T_{kr,min}. \tag{11}$$

The converter frequency $f_{i,max}$ in the K^{th} interval is:

$$f_{i,max}(K) = 1/(2 * T_{ok,min}). \tag{12}$$

The internal frequency for the converter at full power operation is assumed to be 10 Khz. By substituting this value into equation (12), we obtain:

T_{okmin} = 50 micro seconds.

Substituting the average current $|i|_{avg}$, the time interval T_{okmin} and the input voltage in equation (4) yields:

$C = (4*5*10^{-6}) / (4*100) = 5*10^{-7}$ = 0.5 micro F.

The amplitude of the voltage is minimal when the angular frequency " W_o " is:

$$W_o = 1/ (L * C)^{1/2} . \tag{13}$$

The relationship between frequency f_o, angular frequency W_o and the period T_o is given by:

$$f_o = 1/ 2 * T_o = W_o / 2 * \pi . \tag{14}$$

By substituting the angular frequency from equation (13) into equation (14), we obtain:

$$T_o = \pi / W_o = \pi * SQRT(L*C). \tag{15}$$

Equation (9) shows that $T_{kf,min}$ is the minimum time interval during which the thyristors are conducting. During this period, the voltage over the series-resonant capacitor is miniminal. Therefore, $T_{kf,min}$ is almost equal to T_o. Thus, substiting this value into equation (9), it follows that:

$$T_{ok,min} \approx T_{kr,min} + T_o . \tag{16}$$

By substituting $T_{ok,min}$ and $T_{kf,min}$ from equations

(10) and (11) into equation (16), we obtain:

$$T_o = 4 * T_{kr,min} = 40 \text{ micro seconds.}$$

From equation (15), the series-resonant inductor is:

$$L = (T_o / \pi)^2 / C \ , \qquad (17)$$

and therefore:

$$L = (40/3.14)^2 / 0.5*10^{-6} = 325 \text{ micro henry.}$$

The only unknown values are the sizes of filter capacitors. The filter capacitors C_s and C_o are connected to the input voltage source and the load respectively. These capacitors should be chosen to minimize the effect of the source and the load impedances on the performance of the resonant current, which obviously should be primairly dependent on the inserted resonant inductor and capacitor. For example, the value of 10 micro farad appear to be a reasonable choice for the input and output filter capacitors.

2.2 THE SENSOR CIRCUIT

A sensor circuit consists of a shunt resistor and a full-wave rectifier as shown in figure 2.2.1. The shunt resistor is connected to the output of the diode bridge "SM2". This resistor senses the resonant current from the power circuit and the voltage across this resistor is fed as a signal into the full-wave rectifier.

The full-wave rectifier contains three operational amplifiers (LM741) and a diode bridge as shown in figure 2.2.1. When the input voltage increases above 0 V, D_{fw4} turns ON, and the negative voltage causes diode D_{fw2} to turn OFF. When the input voltage is negative, diode D_{fw2} turns ON while diode D_{fw4} turns OFF. Amplifier U_3 is a summing amplifier with an output voltage of:

$$V_L = -V_i - 2*V_r. \qquad (18)$$

The diodes fw1 and fw3 are used for balancing the current at the output terminal of the operational amplifiers in the back-bias mode.

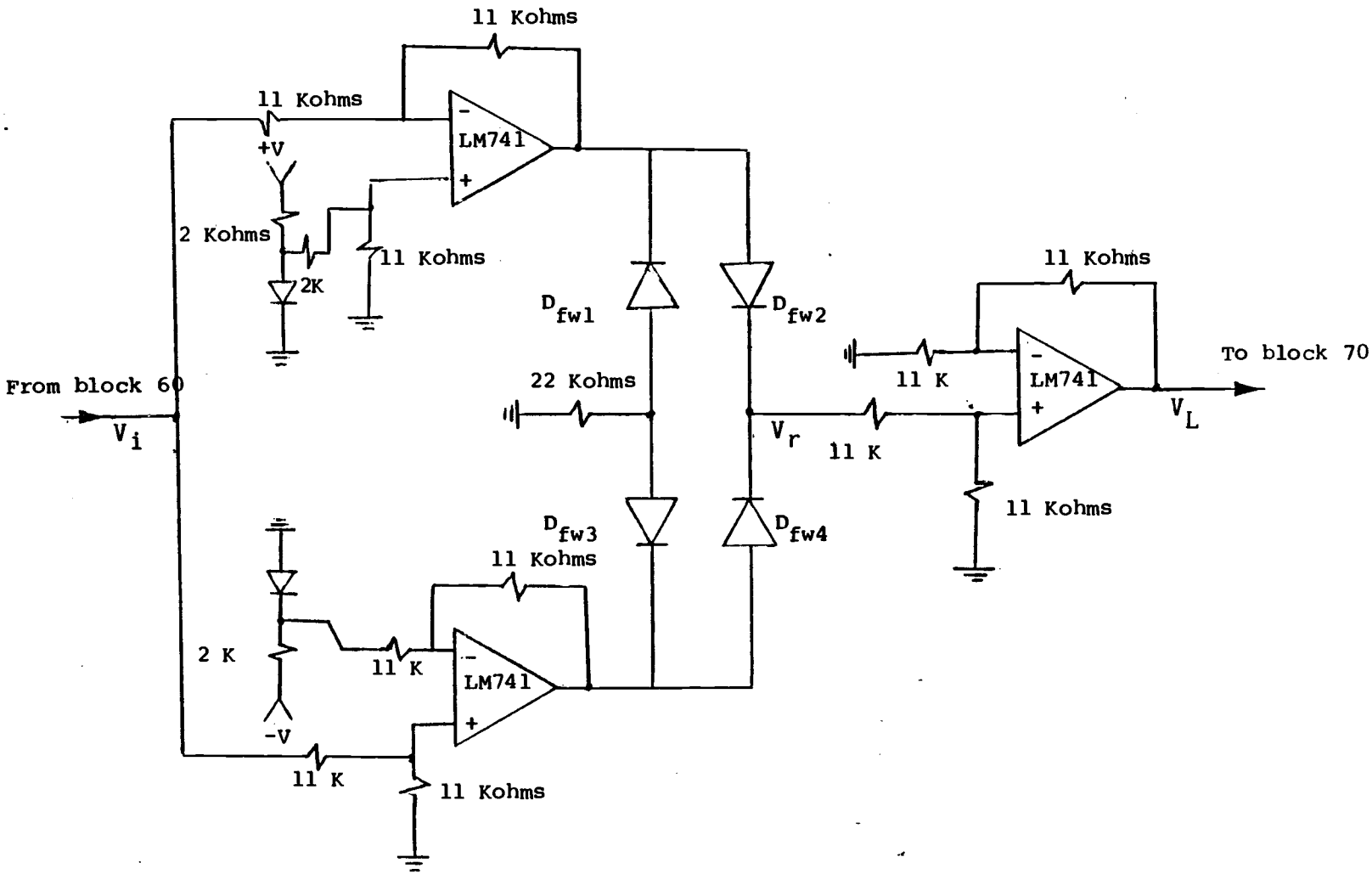


Figure 2.2.1. The Sensor.

2.3 CONTROLLER

The function of the controller is to facilitate the efficient and stable energy-transfer through the power circuit. In designing the power controller, four basic elements are distinguished; (a) the integrator, (b) the summing amplifier, (c) the comparator, and (d) the trigger reset. Figure 2.3.1 shows the connection between these devices.

(a) The series-resonant signal " i " from block 50 feeds into an operational amplifier in block 70. An operational amplifier also can be used to implement active filters like an integrator. As it is shown in figure 2.3.1, two integrators are used, one connected to the output of block 50 and the other to a DAC (V_{ref}). These circuits provide an output voltage proportional to the integral of the input voltage where:

$$V_{oI} = -1/(R*C_I) * \int^{t} v(j)\, dj. \qquad (19)$$

The capacitor " C_I " is usually paralleled with an FET switch which is closed when the capacitor is discharged. It is opened when the capacitor is charged, i.e., performing an integration. Initial voltage can

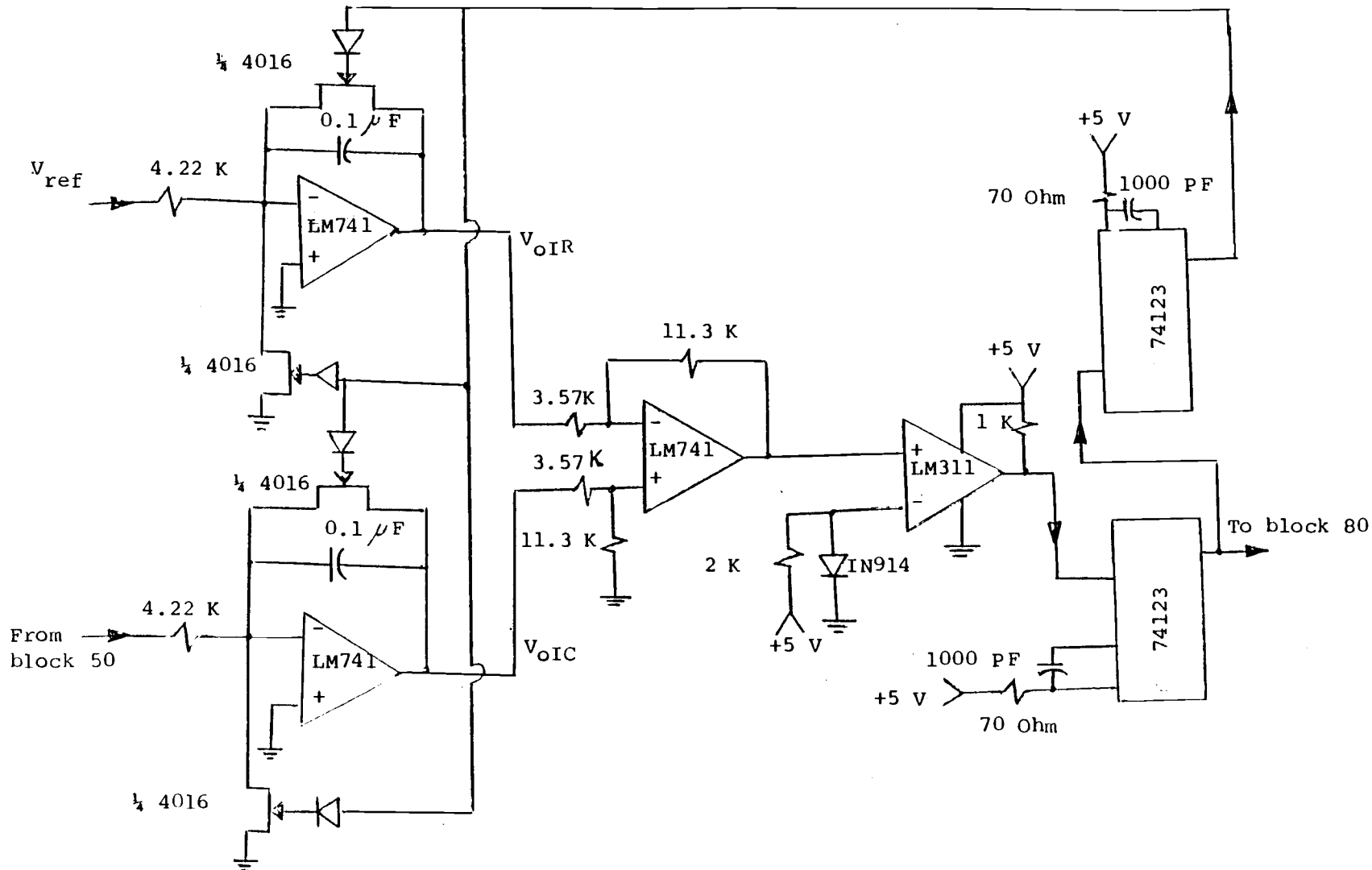


Figure 2.3.1. The Controller for the system.

be applied to the capacitor by putting the voltage in series with the switch. In this case, the Retriggerable Monostable Multivibrator (LM74123) feeds back the voltage signal from the output of the power controller into the input of the switches.

(b) The output voltage of the summing device is proportional to the sum of the input voltages which are the two signals " V_{oIC} " and " V_{oIR} " from the integrators. That is:

$$V_{osum} = (11.3 / 3.57) * (V_{oIC} - V_{oIR}) \qquad (20)$$

(c) The " LM311 " is a single high-speed voltage comparator. It is designed to operate at a supply voltage of 5 volt. If the input voltage is higher than zero the output signal will be almost 5 volts.

(d) The Retriggerable Monostable Multivibrator (LM74123) is a device with an output pulse primarily a function of the external capacitor and resistor . The pulse duration can be changed by selecting the sizes of the capacitor and the resistor. The duration of this pulse follows from:

$$T_w = K_d * R_t * C_{exp}(1+0.7/R_t). \qquad (21)$$

T_w is the time period determined by the value of the external resistor and capacitor. K_d is a constant value which is 0.28. C_{exp} and R_t are the external capacitor and resistor respecitively.

Let T_w be 20 micro seconds and the external capacitor be 1000 PF. Therefore, the value of the external resistor is:

$$R_t\ (\ 1+0.7/R_t) = 20*10^{-6}/0.28*1000*10^{-9}$$
$$=70 \text{ ohms.}$$

2.4 SCR TRIGGER LOGIC

This component of the DC-to-DC converter has the function of properly firing the thyristors corresponding to the chosen control strategy. The logic contains a JK flip-flop and two AND gates as shown in figure 2.4.1. The J and the K terminal are kept logically high. The clock of this JK flip-flop is connected to the output of the Retriggerable Monostable Multivibrator (LM74123). Thus the output changes only during the transient operation of the flip-flop, triggered by the **trailing edge** of the clock. This flip-flop transfers information from the input to the output only at the beginning (or end) of each clock pulse. The outputs of this JK flip-flop are connected to

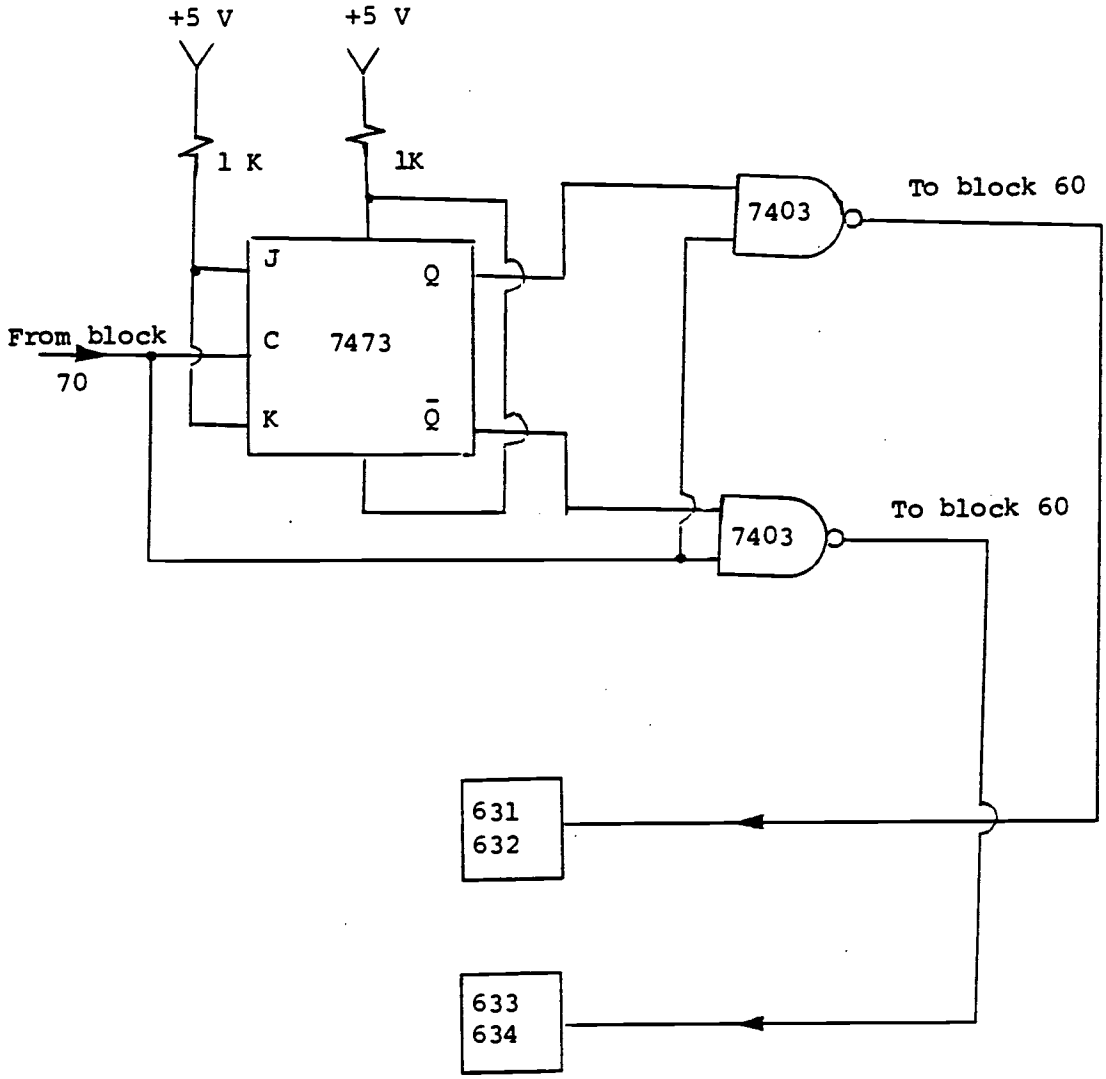


Figure 2.4.1. The thyristors trigger logic.

the inputs of the AND gates. The other input of these AND gates is the signal from the LM74123. Thus, the outputs of these AND gates are high if the input signals are high. The output of these AND gates are connected to the blocks 631, 632, 633, and 634.

3.SIMULATION

The system is simulated for understanding the performance of critical variables, so that final protective measures can be included to the actual design. Thus, from the simulation we can obtain a means for non-destructive testing of the overall performance of the converter. Another important purpose of the simulation is to verify the effectiveness of the proposed control strategy and to conduct possible fine-tuning before actual design efforts are undertaken.

A power software proposed for this simulation is the ElectroMagnetic Transients Program (EMTP) which is used here. In particular the Transients Analysis of Control System (TACS) module can be exploited for the design of the controller.

3.1 TACS HYBRID

TACS HYBRID simulates the dynamic interaction between a control system and an electrical network in the EMTP. The TACS was used to design the controller for triggering the thyristors.

The TACS sends the triggering signal when the area under resonant current "i" is equal to the area under

reference current "$K_r * i_r$", that is:

$$\int_{t_k}^{t_{k+1}} |i|\, dt = \int_{t_k}^{t_{k+1}} K_r * i_r\, dt \qquad (1)$$

Since this equation should hold for all operating conditions, a PEAK CURRENT LIMITER has been designed to facilitate this condition from time t_k to t_{k+1}. If the PEAK CURRENT LIMITER is not included, a cyclic instability is introduced causing the resonant current to become excessively high. The basic reason for this cyclic instability is excessive accumulation of charge on the capacitor if the pulse area modulation (ASDTIC) [7] control would not permit the diodes to conduct. It is recalled that during the period of diode conduction energy accumulated in resonance circuit will be pumped back into the source. The PEAK CURRENT LIMITER controls the phase angle of the resonant current from pulse to pulse such that a minimal period of diode conduction is secured. This in essence is equivalent to limiting the resonance current within certain limits. The phase angle is extrapolated from the initial conditions at the instants when the thyristors are fired. As a result, the PEAK CURRENT LIMITER also avoids any excessive current stress at each

pulse interval. The value of resonant current with reference to figure 2.1.2 is:

$$i(t)= \frac{V_{lc} - V_{c(0)}}{Z_{lc}} * \sin W_n * t + I_0 * \cos W_n * t, \tag{2}$$

with

$$Z_{lc} = (L/C)^{1/2}, \tag{3}$$

and

$$W_n = 1/SQRT(L*C), \tag{4}$$

where V_{lc} is the voltage across the series-resonant circuit, $V_{c(0)}$ is the initial voltage of the series-resonant capacitor. I_0 is the initial value for the series-resonant current, L is the resonant inductor and C is the resonant capacitor.

If the series-resonant current "i" is at a peak value "I_p", the time "t" should be at "t_p". This leads to:

$$I_p=I_t*\sin W_n*t_p+I_0*\cos W_n*t_p, \tag{5}$$

where

$$I_t = \frac{V_{lc}-V_{c(0)}}{Z_{lc}}, \qquad (6)$$

$$\sin W_n * t_p = I_t/(I_0^2+I_t^2)^{1/2},$$

and (7)

$$\cos W_n * t_p = I_0/(I_0^2+I_t^2)^{1/2}.$$

Substituting equation (7) into equation (5), we obtain:

$$I_p=(I_0^2+I_t^2)^{1/2}. \qquad (8)$$

Therefore this value could not exceed more than the value of "$K_r * i_r$".

The thyristors are conducting when the capacitor is charging. When the diodes are conducting, the capacitor is discharged. Thus, the thyristors should be triggered at a moment such that enough capacitor voltage V_{cap} will be available for the diodes to conduct at the next cycle. This determines the maximum angle for diodes D1 and D2 before the thyristor TH3 and TH4 are triggered (refer to figure 2.1).

The value of V_{cap} will be compared with the value of V_{cmax1}. If V_{cap} is higher than the V_{cmax1}, the thyristors are triggered as shown in figure 2.1.2. V_{cmax1} is determind from:

$$V_{cmax1} = V_{lc} + | 2* V_{lc(0)} | , \qquad (9)$$

where $V_{lc(0)}$ is the voltage across the series-resonant circuit when the thyristors are conducting and V_{lc} is the voltage across the resonant circuit when the diodes are conducting.

In other words the controller sends a signal to trigger the thyristors if the peak value of resonant current is smaller than the reference signal and the value of capacitor voltage is higher than the value of V_{cmax1}. Notice that this control logic is an added logic which overrides the "ASDTIC" control logic, i.e., the thyristors are fired when the area under resonant current is equal to the area under reference signal.

3.2 THE SWITCHES

The use of diodes and thyristors in the EMTP leads to a problem which is refered to as HASH in this thesis. This problem is not dependent on the firing control strategy

nor on the configuration type of converter. The problem is caused by the one integration-step error introduced by the EMTP. When the current becomes smaller than zero, the diodes and the thyristors should turn-off. In the EMTP this ideal turn-off will take one additional integration step leading to what is known as the HASH problem.

The HASH problem can be resolved by connecting an inductor in series with the thyristor and a snubber network parallel to the thyristor. The snubber network is a series connection of a capacitor and a resistor.

This circuit is recommended when switches are used in the EMTP [8]. This circuit is implemented into the series-resonant circuit of the DC-to-DC converter.

Figure 3.2.1 shows the DC-to-DC converter which indicates the inclusive of a small resistor connected to the switches. This is to satisfy the EMTP requirement that two switches can not be directly connected to one node.

3.3 SOURCES

The EMTP requires one terminal of the sources to be grounded. Thus the source in the DC-to-DC converter is connected to both sides of the switches. However, this problem can be resolved by using a Norton Equivalent

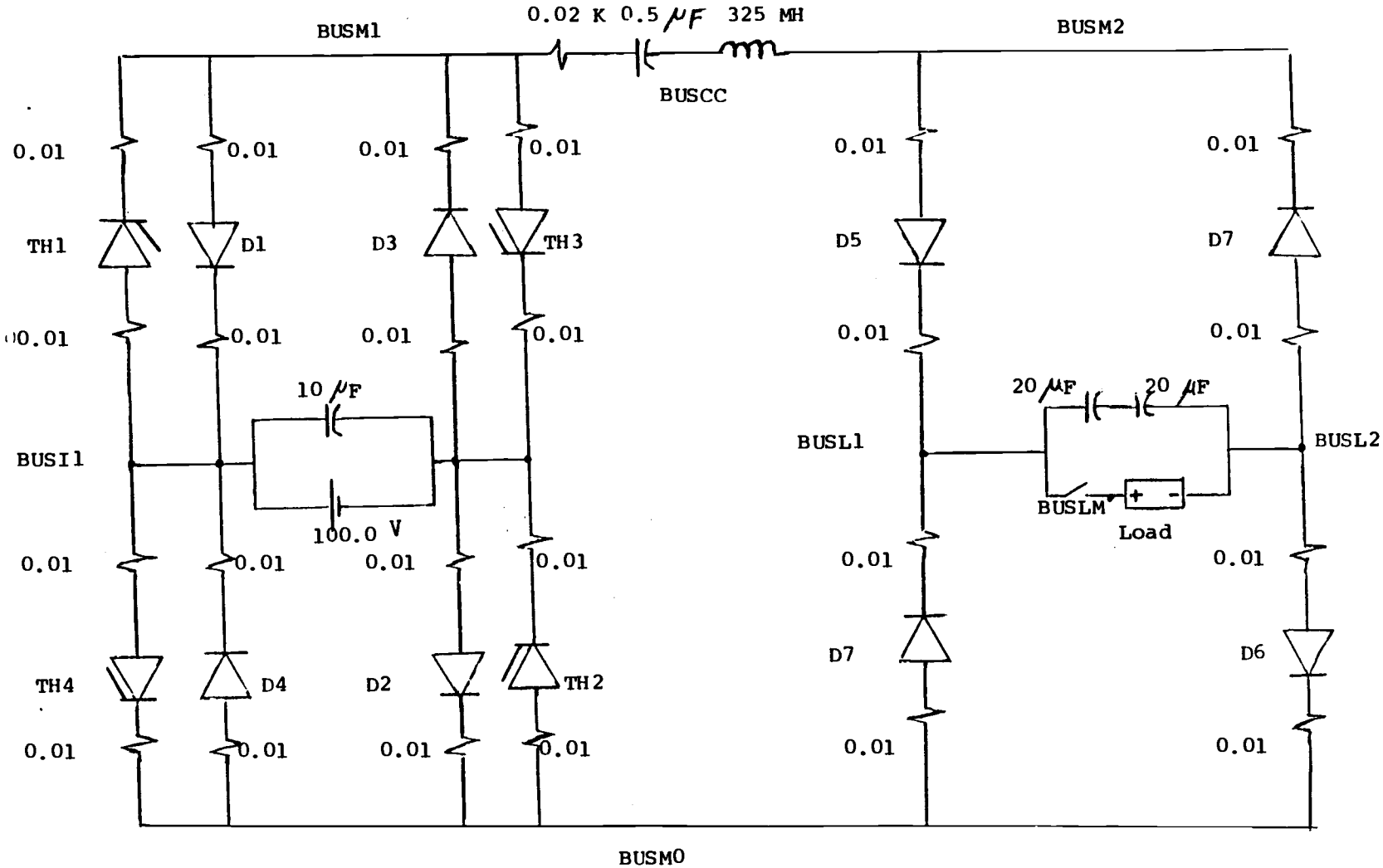


Figure 3.2.1. The connection of the system in the EMTP.

as shown in figure 3.3.1. The value of the resistor in the Norton Equivalent is taken so small that it does not affect the load current.

The simulation of the DC-to-DC converter is explained in more detail in Appendix I.

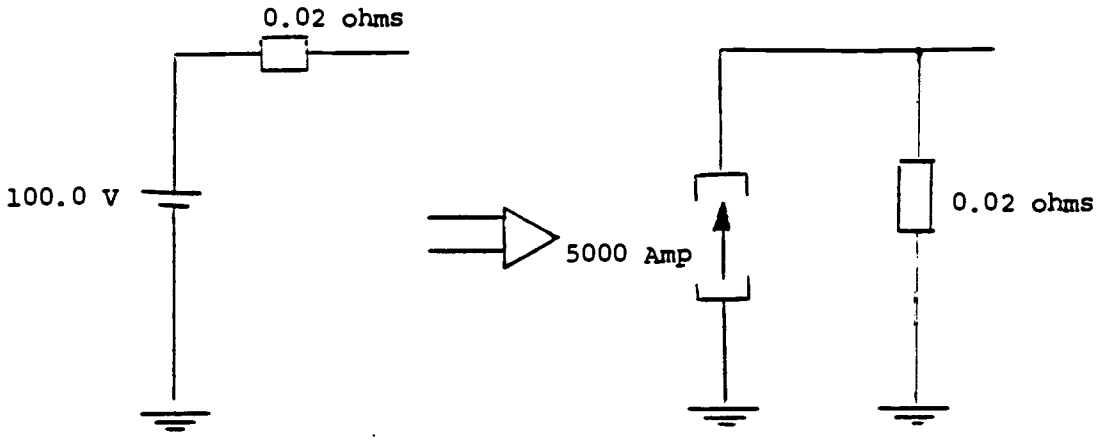


Figure 3.3.1. The Norton Equivalent of the source.

4. RESULTS AND CONCLUSIONS

The DC-to-DC converter was designed and tested with the ElectroMagnetic Transients Program (EMTP). The basic idea is to sense the resonant current from the EMTP and supply this signal to the Transients Analysis of Control system (TACS) as a means of providing the controller with the information for proper triggering the thyristors. Four different parts of the EMTP data case can be discerned in the simulation (see Appendix I): 1) The TACS, 2) The power circuit elements, 3) The electric-network switches, and 4) The sources.

1) The TACS senses voltage and current from the EMTP through the TACS source (types 90 and 91) as shown in Appendix I. All the calculations can be done by means of the supplemental variables and devices. The supplemental variable (type-98) will transfer the information from TACS to the EMTP electric-network elements such as supplying the trigger signal determined in TACS to the EMTP switches representing the converter thyristors.

2) The elements of the circuit should be connected into different nodes as shown in figure 3.2.1. The attached

listing of the data case in Appendix I shows these connection starting at the line provided with the comment card: "SM1".

3) Two types of EMTP switches are used to simulate the diodes and thyristors of the converter. The Thyristors are represents by the type 11 switch, which conducts when the triggering signal from the TACS is equal to zero or greater than zero. The diodes are simulated by either a type 11 switch or a type 13 switch, which conducts when the triggering signal from the TACS is greater than zero. Type 11 switches are used for the diodes of the input switch matrix, whereas the diodes of the output switch matrix are represented by the type 13 switches. This is to avoid the diodes in parallel to the thyristors to be conducting simultaneously.

4) The EMTP source (type 14) can be utilized either a voltage source or a current source. The EMTP will take the value in the source card as a current source when "-1" is punched in columns 9 and 10 of the source card.

The simulation was run on DEC-20 of Department of Electrical and Computer Engineering at Oregon State University. The required computing time to simulate the DC-to-DC converter is reasonable. The execution time for

32 resonance cycles is about 540 seconds (9.0 minutes).

The triggering signal (ASDTIC) will occur when the area under resonant current is equal to the area under reference signal. It was found that the converter operates only with a unique reference signal (4.0 Amps). Deviations from this signal failed to produce the triggering signal (ASDTIC) for the thyristors as shown in figure 4.1. As the reference signal changes, ASDTIC needs more time to equate the area under reference signal to the area under resonant current.

As shown in figure 4.1 the ASDTIC is positive at point A in the first half cycle which triggers thyristors 1 and 2 (refer to figure 2.1). After completion of the natural commutation process of these thyristors, the ASDTIC is negative and not ready to trigger thyristors 3 and 4, causing diodes 1 and 2 to be conducting at point B. This state is maintained for almost 2.00 microseconds, after which the ASDTIC becomes positive and triggers thyristors 3 and 4. The thyristors conduct for almost half a cycle, causing the area under the resonant current to exceed the area under the reference signal by a negative value. This prevents thyristors 1 and 2 from being fired and allows diodes 1 and 2 to conduct for half a cycle. The conduction of diodes pumps the energy back into the

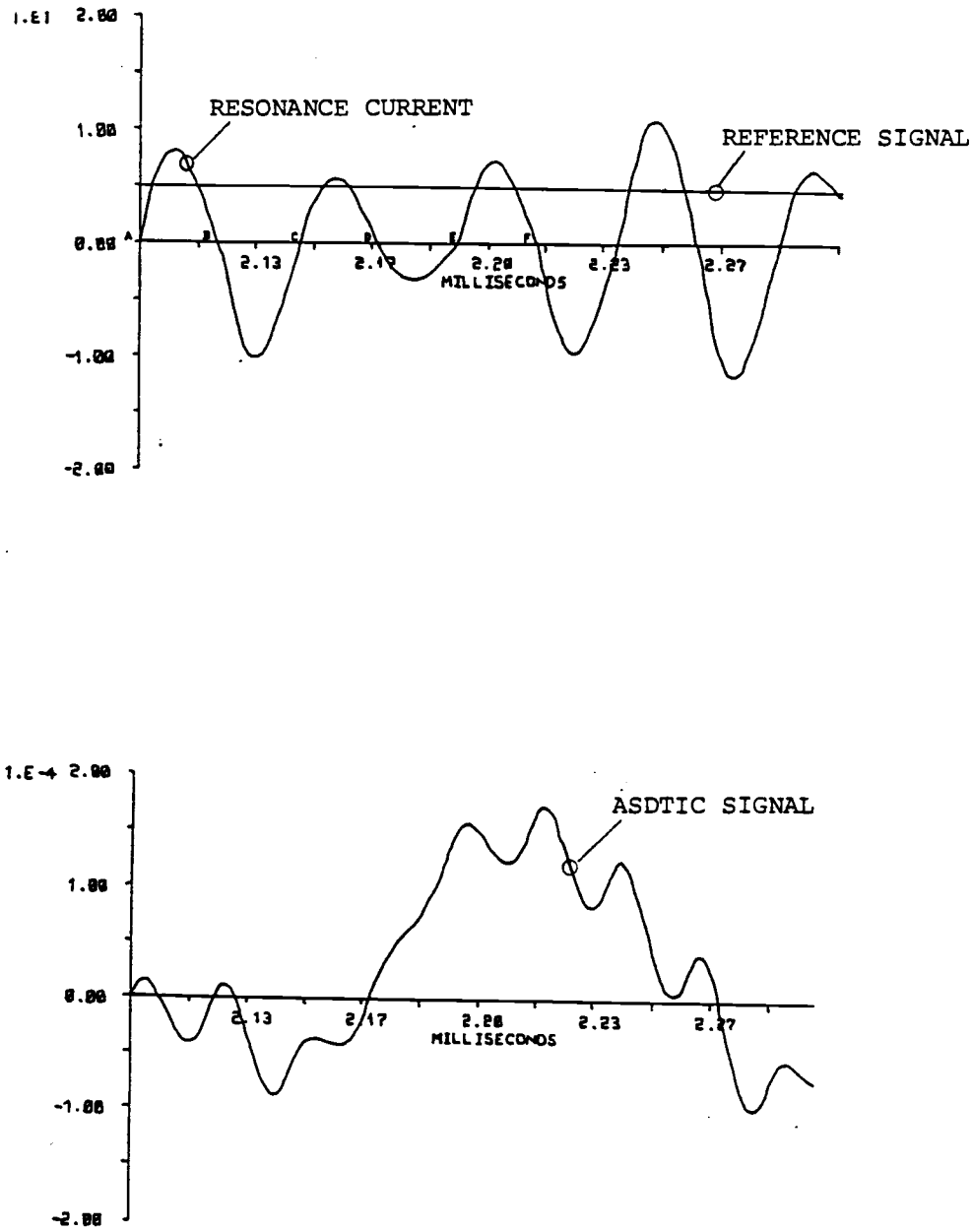


Figure 4.1. The waveforms before designing the PEAK CURRENT LIMITER.

source as the result of the discharge of the series-resonant capacitor. The resulting positive current leads to an excessive value of ASDTIC signal. At point D in figure 4.1, ASDTIC is positive and thyristors 3 and 4 are triggered causing the series-resonant capacitor to be recharged. This limits the growth of the resonant current. Figure 4.1 shows the consequence of this limited development on the growth of the ASDTIC. The value of ASDTIC is positive when the natural commutation of thyristors 1 and 2 occur, allowing thyristors 3 and 4 to conduct without being preceded by a period of conduction of the diodes.

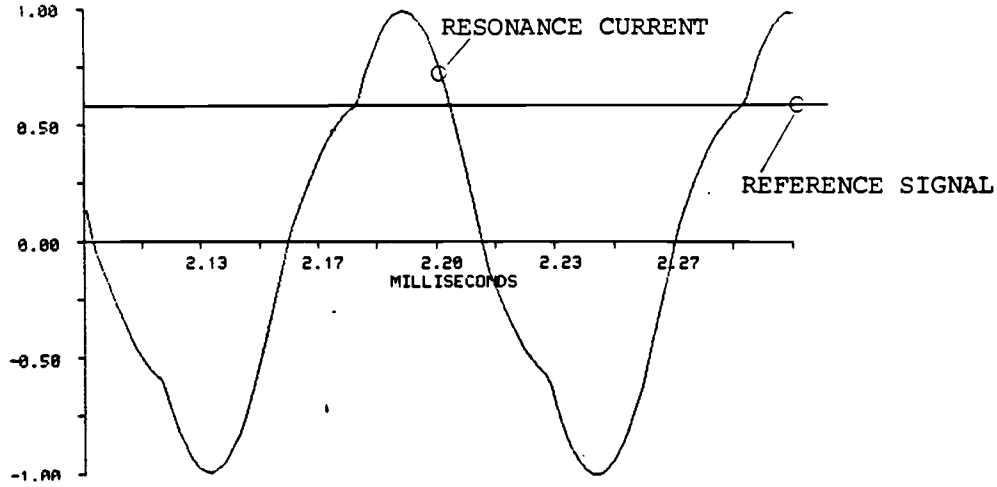
This explains why the design fails except for a unique reference signal and how, as explained in chapter 3, the problem is overcome by introducing a PEAK CURRENT LIMITER in the circuit.

The peak value of resonant current is calculated in the TACS and will be compared with the value of $K_r * i$, where $K_r = 1.707$ and i_r is the reference signal. If the peak value of resonant current is greater than $K_r * i_r$, the thyristors are not allowed to conduct, even if the ASDTIC signal would require these thryistors to conduct.

The ASDTIC continues to compare the area under resonant current and reference signal. If they are equal

the triggering signal will be sent to the EMTP to permit the thyristors to conduct as shown in figure 4.2. The programming steps of the above are detailed in Appendix I.

In conclusion, by inserting the PEAK CURRENT LIMITER to the design, the controller becomes operational with an arbitrary reference signal. It can also be concluded that the proposed feedback control strategy is "self-protecting". Any fault in the system that disrupts the resonant current signal would also deactivate the controller, thereby protecting the devices in the system.



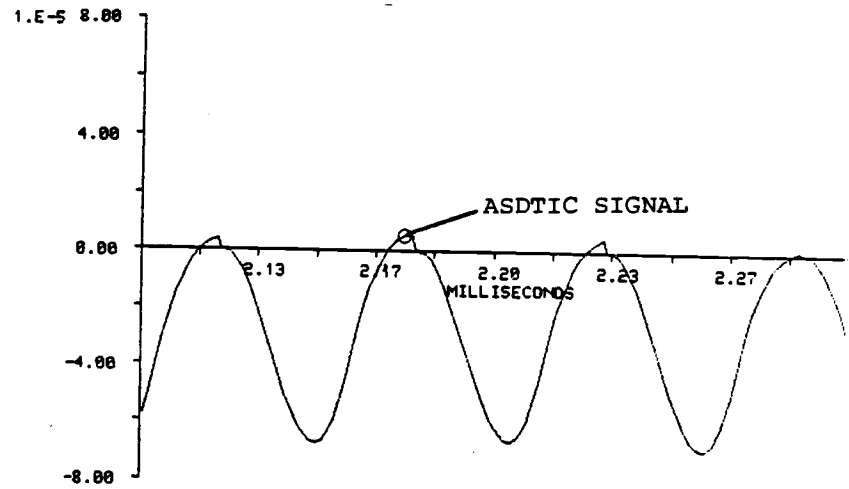


Figure 4.2. The waveforms after designing the PEAK CURRENT LIMITER.

BIBLIOGRAPHY

[1] Dewan, S. B., "Power Semiconductor Circuits", John Wiley & Sons, 1975.

[2] Csaki, F., Ganszky, K., Ipsits, I., Marti, S., "Power Electronics", Akademial Kiado. Budapest, 1975.

[3] Schwarz, F. C. and Klaassens, J. B., "A 95-Percent Efficient 1-KW DC Converter with an Internal Frequency of 50 KHZ", IEEE Transactions on Industr. Electr. and Contr. Instr., Vol. IECI-25, No.4, Nov. 1978, pp. 326-333.

[4] Schwarz, F. C., "An Improved Method of Resonant Current Pulse Modulation for Power Converters", IEEE Transactions on Industr. Electr. and Contr. Instr., Vol. IECI-23, No.2, May 1976, pp. 133-141.

[5] "ElectroMagnetic Transients Program (EMTP) Rule Book", June 1984.

[6] Schwarz, F. C. and Klaassens, J. B., "A Controllable 45-KW Current Source for Machines", IEEE Transactions on Industr. Applic., Vol. IA-15, No.4, July/August 1979, pp. 437-444.

[7] Schwarz, F. C., "Analog Signal to Discrete Time Interval Converter", U.S. Patent Nr. 3,659,184, April 1972.

[8] Lauw, H. K., "Design Recommendations for Numerical Stability of Power Electronic Converters", EMTP News, Vol.5, Nov. 1980.

APPENDIX

APPENDIX I

```
STORE
BEGIN NEW DATA CASE
ABSOLUTE TACS DIMENSIONS
       6      120      133       26       70      460      466      110
C  MISCELLANOUS DATA CARD
  1.0E-6 4.20E-3
       1        1        1        0        0       -1        0        1
      10      990      100      100
TACS HYBRID
C        The voltage and switch current are sensing
C        from the EMTP to the TACS by code numbers 90
C        and 91 as shown in figure 3.2.1.
90BUSC
90BUSCC
90BUSM1
90BUSM2
C        Sensing the diode currents for the PEAK
C        CURRENT LIMITER :
91DIK1
91DIK3
C        Sensing the load current to desgin the accelerated
C        starting for the PEAK CURRENT LIMITER :
91BUSLM
C        Establishing the resonance capacitor voltage from
C        the node voltage of BUSC and BUSCC refere to figure 3.2.1.
99VCAP     =BUSC - BUSCC
C        These are the value of elements in the resonant circuit
C        for finding the value of impedance for the calculation
C        of PEAK CURRENT LIMITER.
88CRES     = 0.5 * PLUS1
88LRES     = 400.0 * PLUS1
C        This is the value of reference signal.
88IRF      = 6.0 * PLUS1
C        Measuring the voltage across the series-resonant
C        circuit and the power flow in the circuit.
88ULC      =BUSC  -  BUSM2
88PFLOW    = ULC  *  IRS
C        This is the intial condition for the diode 5 and
C        6 when the resonance current initialy start to conduct.
                                                          -1.000        6.0E-6
11STEPSG   +1000.0
C        The value of firing signal.
88TWONEG   = - 2.0*PLUS1
88TENPOS   = + 10.0*PLUS1
C        All the sources must be input it to type 99.
99DIK1I    =DIK1
99DIK3I    =DIK3
99STEP     =STEPSG
C        Sensing the resonance current from a  small resistor
C        which is connected to the series-resonant circuit in
C        the EMTP.  The value of this resistor is 0.02 ohms.
99BUSR     =BUSM1 -  BUSC
99IRS      =BUSR  /  .020
C        Finding the absolute value of the resonance current.
88IRSSQR   =IRS    **2
88IRSABS   =SQRT(IRSSQR)
C        Signals for controlling the output diodes.
99FIRE56   = IRS    +  STEP  +0.0001*T12FIR
99FIRE78   = -FIRE56
```

```
C       Resetting the ASDTIC signal at the triggering time.
88ASDDIF59-T12FIR -T34FIR                                    1.0E-7
88SIGASD  =ASDDIF + 0.001
C       This is the ASTIC signal and a zero block.
88ASDPRE58-IRSABS +IRF                                  0.0     0.0   1.0   SIGASD
  ASDTIC  +ASDPRE
C             "DETERMINATION OF FIRING SIGNALS"                                ASDTIC
88TFIR  60+TWONEG +TENPOS +TENPOS                                              VCAP
88T12MFL60+TFIR   +TWONEG +TWONEG                                              VCAP
88T34MFL60+TWONEG +TWONEG +TFIR
C                    "PEAK CURRENT LIMITER"
88ILDRF   = BUSLM - IRF
88ILDRFS  = ILDRF * ILDRF
88ILDRFA  = SQRT(ILDRFS)
88ILIM1   = 0.5 * PLUS1
88TWOPOS  = 2.0 * PLUS1                                                        ILIM1 ILDRFA
88ISTART60+TWOPOS +PLUS1  +PLUS1
88IPEAKL  = 1.707 * IRF * ISTART
  FIR12M  -T12FIR
  FIR34M  -T34FIR                                                                    FIR12M
88ULCHT162+ULC                                                                       FIR34M
88ULCHT362+ULC
88LCRAT   = LRES/CRES
88SQRTLC  = SQRT(LCRAT)
88IAUX11  = DIK3I * DIK3I
88IAUX12  = (- ULCHT3 - VCAP)/SQRTLC
88IAUX13  = IAUX12 * IAUX12
88IAUX14  = IAUX11 + IAUX13
88IPEAK1  = SQRT(IAUX14)
88IAUX31  = DIK1I * DIK1I
88IAUX32  = (- ULCHT1 - VCAP)/SQRTLC
88IAUX33  = IAUX32 * IAUX32
88IAUX34  = IAUX31 + IAUX33
88IPEAK3  = SQRT(IAUX34)                                                       IPEAK1IPEAKL
88T12SET60+T12MFL +T12MFL +TWONEG                                              IPEAK3IPEAKL
88T34SET60+T34MFL +T34MFL +TWONEG
C                  "LOGIC FOR MAXIMUM DIODE CONDUCTION ANGLE"
11VDRIVE    5.0                                                      -1.000
99VCMAX1  = + ULC - 2.0*ULCHT3 - VDRIVE
99VCMAX3  = + ULC - 2.0*ULCHT1 + VDRIVE                                        DIK1I
88D12CON60+T34SET +T34SET +TENPOS                                              DIK3I
88D34CON60+T12SET +T12SET +TENPOS                                              VCAP  VCMAX1
88T12PRE60+T12SET +T12SET +D34CON                                              VCAP  VCMAX3
88T34PRE60+D12CON +T34SET +T34SET
C                    "THE PROTECTION AGAINST THE SHORTING THE SOURCE"           IRS
88T12FIR60+TWONEG +T12PRE +T12PRE                                              IRS
88T34FIR60+T34PRE +T34PRE +TWONEG
C               "PROTECTION AGAINST THE SHORTING THE SOURCE BY EMTP"            T34FIR
88D12PRE60+ZERO   +ZERO   +TWONEG                                              T12FIR
88D34PRE60+ZERO   +ZERO   +TWONEG
C       Code 98 will output the firing signals from TACS to EMTP.
98FIRE12  =T12FIR
98FIRE34  =T34FIR
98FIRD12  =D12PRE
98FIRD34  =D34PRE
98SIGPOS  =TENPOS
C       The outputs which are desired from the TACS.
33ULCHT1ULCHT3T12FIRIRS   IRF   ASDTICVCAP  T34FIRSIGASD
```

```
33VCMAX1VCMAX3T12MFLT34MFLPFLOW ULC   IRGABSD12PRED34PRE
BLANK CARD ENDING ALL TACS DATA
C                        "POWER CIRCUIT ELEMENTS"
C             "SM1"
  BUSI1 SCRA1                  0.01
  SCRK1 BUSM1                  0.01
  BUSM1 DIA1                   0.01
  DIK1  BUSI1                  0.01
  BUSM0 SCRA2 BUSI1 SCRA1
  SCRK2       SCRK1 BUSM1
        DIA2  BUSM1 DIA1
  DIK2  BUSM0 DIK1  BUSI1
  BUSM1 SCRA3 BUSI1 SCRA1
  SCRK3       SCRK1 BUSM1
        DIA3  BUSM1 DIA1
  DIK3  BUSM1 DIK1  BUSI1
  BUSI1 SCRA4 BUSI1 SCRA1
  SCRK4 BUSM0 SCRK1 BUSM1
  BUSM0 DIA4  BUSM1 DIA1
  DIK4  BUSI1 DIK1  BUSI1
C             "SM2"
  BUSM2 DIA5                0.01
  DIK5  BUSL1               0.01
  BUSL2 DIA6  BUSM2 DIA5
  DIK6  BUSM0 DIK5  BUSL1
  BUSL2 DIA7  BUSM2 DIA5
  DIK7  BUSM2 DIK5  BUSL1
  BUSL1 DIK8  DIK5  BUSL1
  BUSM0 DIA8  BUSM2 DIA5
C          "THE SERIES RESONANT CRICUIT"                              2
  BUSC  BUSCC                        0.50
  BUSCC BUSM2                  0.40
C           "THE LOAD"                                                3
  BUSLM BUSL2               10.0
C           "THE ELEMENT IN CASE OF FLOATING SOURCE"
  BUSM2                     1.0E+5
C             "THE RESONANT RESISTOR"
  BUSM1 BUSC                0.02
C               "INPUT FILTER CAPACITOR"                              1
  BUSI1                              10.0
C               "OUTPUT FILTER CAPACITORS"                            1
  BUSLC BUSL2                       200.00
  BUSL1 BUSLC                       200.00
BLANK CARD ENDING ALL BRANCHES
C               "THE ANTI-PARALLEL DIODES (SM1)"
11DIA1  DIK1                                              FIRD12  13
11DIA2  DIK2                                              FIRD12  1
11DIA3  DIK3                                    CLOSED    FIRD34  13
11DIA4  DIK4                                    CLOSED    FIRD34  1
C               "THE OUTPUT BRIDGE DIODES (SM2)"
13D1A5  DIK5                                    CLOSED    FIRE56  13
13D1A6  DIK6                                    CLOSED    FIRE56  1
13DIA7  DIK7                                              FIRE78  13
13DIA8  DIK8                                              FIRE78  1
C                 "THE THYRISTORS (SM1)"
11SCRA1 SCRK1                                     FIRE12          13
11SCRA2 SCRK2                                     FIRE12          13
11SCRA3 SCRK3                                     FIRE34          13
```

```
11SCRA4 SCRK4                                                    FIRE34          13
C          "LOAD CURRENT MEASUREMENT FOR ACCELERATED STARTER"
13BUSL1 BUSLM                                                    CLOSED          SIGPOS  1
BLANK CARD ENDING SWITCHES
C            "THE DC SOURCE VOLTAGE"
14BUSI1       100.0       1.000      0.0                                -1.0000
BLANK CARD ENDING SOURCES
$ LISTON
  BUSM1 BUSM2
BLANK CARD ENDING NODE VOLTAGE OUTPUT REQUEST
BLANK CARD ENDING PLOT CARDS
BEGIN NEW DATA CASE
BLANK CARD ENDING DATA CASE
12345678911234567892123456789312345678941234567895123456789612345678971234567898
```