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Title: A Test Fixture and Deembedding Procedure for
High-Frequency Substrate Characterization

Abstract approved:

Terri Fiez Karti Mayaram

At frequencies exceeding 1-2 GHz, the substrate network models used in substrate coupling simulation must account for the reactive nature of the substrate. Unlike at low frequencies, where the purely resistive substrate models can be validated through DC resistance measurements, these high-frequency models, comprising reactive components, must be validated through high-frequency network analyzer measurements. Accurately obtaining such measurements requires careful design of both a measurement test fixture as well as a measurement deembedding procedure.

A test fixture has been fabricated and a deembedding procedure designed to enable high-frequency (up to 20 GHz) network parameter measurements of a silicon substrate. A test chip, containing a variety of substrate test structures has been fabricated in a 0.35 μm CMOS process on a heavily-doped substrate. The design of the test fixture, test chip, and deembedding procedure has been validated through extensive simulations in HFSS. Measurements have been made

on the test chips mounted in the test fixture. The performance of the test fixture and measurement deembedding procedure has been evaluated, and suggestions for future improvements in this area are presented.

A Test Fixture and Deembedding Procedure for High-Frequency Substrate Characterization

by

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Kyle M. Webb, Author

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

Figure Page

Figure Page

LIST OF TABLES

Table Page

LIST OF APPENDIX FIGURES

Figure Page

A Test Fixture and Deembedding Procedure for High-Frequency Substrate Characterization

1. INTRODUCTION

1.1. Background and Motivation

With the exploding market for portable electronic devices, such as cell phones, PDAs, and digital music players, comes a drive toward making those products smaller, less expensive, and more power efficient. These goals can be accomplished, in part, by higher levels of integration. That is, integrating more and more functionality on single integrated circuits (ICs). Often this means the integration of sensitive analog circuitry, such as the front end of wireless transceiver, with a high-speed, noisy digital signal processing block, all on a single IC.

With sensitive analog blocks and noisy digital blocks fabricated on a common silicon substrate, noise coupling from the digital to analog circuitry becomes a concern. This coupling can occur through several interdependent paths, including the power supplies, interconnect and package parasitics, and through the silicon substrate itself [1], [2].

The Silencer! tool developed at Oregon State University enables mixed-signal circuit designers to predict, through simulation, the coupling that will occur between analog and digital blocks in a circuit layout [3]. Given a circuit layout in a specified IC process, Silencer! extracts an equivalent substrate network to model the coupling between regions of the layout, which are specified by the circuit designer. The extracted equivalent substrate network consists of resistive

pi-networks connecting all pairs of specified substrate contacts. This resistive substrate network is then inserted into the circuit netlist, enabling the inclusion of substrate coupling effects in circuit simulation.

It has been shown that for lower frequencies, below roughly 1-2 GHz, the substrate can be adequately modeled as purely resistive [4]. At these frequencies, the extracted substrate network connecting two p+ substrate contacts is shown in Figure 1.1.

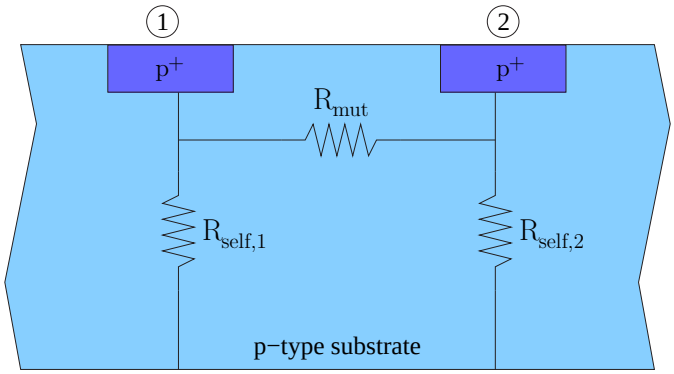


FIGURE 1.1. Low-frequency resistive substrate network model.

In this pi-network, R_{mut} represents the mutual resistance between the two substrate contacts, while $R_{self,1}$ and $R_{self,2}$ represent the self resistances of each contact to the back side of the die. While the resistive network is adequate at lower frequencies, at higher frequencies, in excess of 2 GHz, it becomes necessary to account for the dielectric nature of the substrate. At these higher frequencies, a more accurate equivalent substrate network would include both resistive and reactive components [5], [6], as shown in Figure 1.2 [7].

Similar to the low frequency model, the high frequency model is a pi-network, with self and mutual resistances being replaced by self and mutual admittances. For both models a common node at the backside of the substrate is assumed. This is a valid assumption for heavily-doped logic processes, fabricated

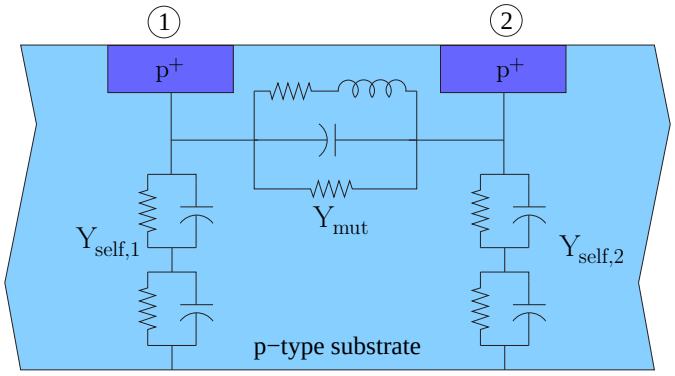


FIGURE 1.2. High-frequency substrate network model.

on very low resistivity substrates, and for any die which is conductively bonded to a package ground plane.

The extraction of a substrate network from an IC layout is accomplished by the use of models developed for the given IC process. These models are formulae, which compute the network component values based on the geometries of the substrate contacts in question. When developing and refining these models, it is essential to have the means to validate them through physical measurements. At lower frequencies the resistive models can be validated through DC resistance measurements made on test structures laid out in a die. These test structures consist of pairs of p^+ substrate contacts of various dimensions and spacings. DC resistance measurements can then be made whereby the values of R_{self} and R_{mut} can be determined. Figure 1.3 shows that the pairs of substrate contacts can be thought of as two-port networks, which can be characterized by any set of network parameters, such as open-circuit impedance parameters (Z-parameters) or short-circuit admittance parameters (Y-parameters).

The two-port network itself comprises the silicon substrate surrounding the two p+ contacts. The backside serves as a common reference node for both

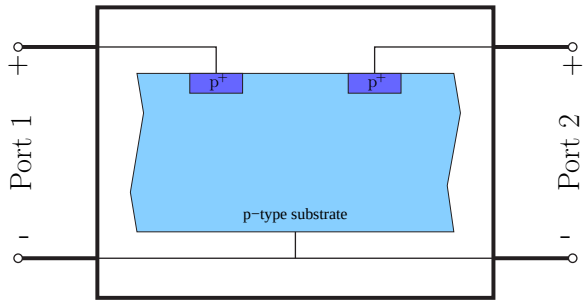


FIGURE 1.3. The substrate as a two-port network.

ports. The potential at port 1 is defined as the potential between contact 1 and the equi-potential backside of the substrate, and the potential at port 2 is defined similarly. Z- or Y-parameters for the resistive two-port substrate network can be extracted by DC measurements. At frequencies exceeding 2 GHz, where the two-port network begins to look reactive, DC measurements no longer suffice, and it becomes necessary to characterize the two-port substrate network as a function of frequency. At the higher frequencies, which are of interest here, the two-port network is best characterized with S-parameters measured with a network analyzer.

Conceivably, the process of characterizing the low-frequency, resistive two-port substrate network with DC measurements, could be extended to network analyzer measurements which characterize the two-port substrate network over a range of higher frequencies. The ability to accurately take such measurements would represent a valuable step in the development of substrate models, which will enable accurate simulation of high-frequency substrate coupling effects in integrated circuits.

1.2. Thesis Outline

This thesis details the design of test structures, a test fixture, and a measurement methodology for the characterization of the two-port substrate network, connecting pairs of p^+ substrate contacts, at frequencies up to 20 GHz. Chapter 2 provides an overview of prior works and efforts to make high-frequency substrate coupling measurements. Chapter 3 describes the design of the test fixture used to make the high frequency network parameter measurements of the substrate network, as well as the design of the test chip, on which the test structures are fabricated. Also discussed in Chapter 3 is the network theory and measurement methodology that enables the extraction of data from network parameter measurements, which may be dominated by test fixture parasitics. This data extraction process is known as deembedding. A four-step deembedding procedure developed for the substrate network measurements taken with this test fixture is detailed in Chapter 4. The test fixture design, including the on-chip test structures, along with the deembedding procedure were validated through extensive simulations. These simulations are the topic of Chapter 5. Measurement results are presented in Chapter 6, and finally, conclusions and suggestions for future work are offered in Chapter 7.

2. AN OVERVIEW OF PRIOR WORK

Previous works have attempted to characterize the two-port substrate network between pairs of substrate contacts with varying degrees of success. These can be separated into two categories: those which directly measure the network parameters of the substrate [5], [8], and those which characterize the substrate indirectly, by sensing and amplifying coupled signals [9], [10].

A direct measurement method, if feasible, is preferred, because it eliminates the uncertainty and additional calibration requirements associated with the on-chip circuitry used in an indirect measurement scheme. Substrate characterization through direct network analyzer measurements is the focus of this work.

Direct measurements, such as [5] and [8], as well as previous measurement attempts made at Oregon State University, have all been similar in that each was performed by probing specially designed on-chip test structures with 50Ω RF micro-probes connected to a network analyzer. In each case probe pads were laid out on a test chip to allow for on-chip probing with the ground-signal-ground (G-S-G) micro-probes. Previous attempts at measurements of this kind at Oregon State University utilized test structures like those shown in Figure 2.1.

In the case of the test structures of Figure 2.1, as well as some of those used in [5] the probe ground leads connect only to each other through metal traces on the test chip; they make no connection to the silicon substrate. The probe ground leads are the point of connection between the measurement system ground of the network analyzer and the reference ground of the two-port network under test. As far as the measurement is concerned, the probe grounds *are* the two-port reference ground. So, in the case of the test structures of Figure 2.1, the reference node of the substrate network being measured becomes the metal ground traces on top of

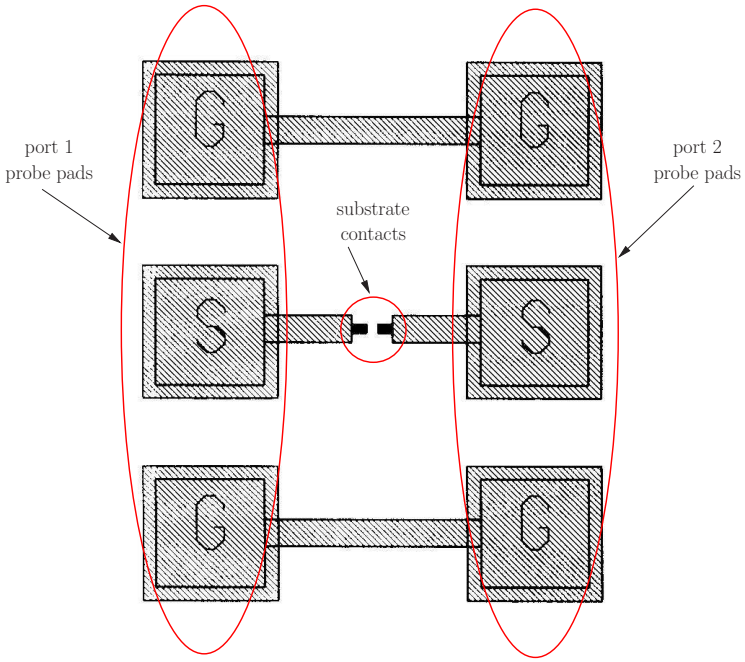


FIGURE 2.1. Test structures used for previous measurements at OSU.

the chip. As explained in Chapter 1, it is desirable to have the back side of the die serve as the reference node for the two-port substrate network.

In other similar works, such as [8] the probe ground pads connect to the substrate with p^+ substrate contacts. In that case the ports of the substrate network are defined between the p^+ substrate contacts being excited and those connected to the probe ground leads.

Measurements of the test structures of Figure 2.1 failed to yield meaningful data, because they were dominated by interactions with the probe station chuck on which the die being tested was situated. This effect was also alluded to in [5]. In that work, however, the problem was eliminated by separating the die from the chuck with a sufficiently thick piece of glass. It was found that the effects of interaction with the probe station chuck could not be eliminated from the measurements on the test structures of Figure 2.1, regardless of the spacing from

the chuck. It is believed that interactions with the chuck are exacerbated by the fact that the backside of the die is not grounded and that the substrate is not directly connected to the probe and measurement system ground.

The circuit models presented in [7], and used by Silencer! [3] for substrate coupling simulation, assume that the reference node for the two-port substrate network is the backside of the die. For accurate high-frequency measurements, as well as measurements which will correlate to the models used in simulation, it is therefore essential to make a good low-impedance connection between the probe grounds and the backside of the die. To the author's best knowledge, this is something that has not been done in previous work.

3. TEST FIXTURE DESIGN

3.1. Off-Chip Probing

Because the backside of the die is the reference node of the two-port substrate network, it is essential to make a low-impedance connection between the probe grounds and the grounded backside of the die. Actually, it is essential to make either a low-impedance connection, or a connection whose impedance can be accurately characterized.

The use of on-chip probing means that the probe grounds are by necessity on the top surface of the substrate. It would therefore be desirable to connect the probe ground pads on the topside of the die to the metallized backside with the use of vias directly through the entire substrate. Unfortunately, this is not an option in a standard IC process.

Another possible method, and the one pursued here, for making the connection between the probe and two-port grounds, is to move the probe points off-chip. By conductively bonding the test chip to a ground plane on some sort of substrate (e.g. PCB or ceramic), the probe grounds can be made to connect directly to the same ground plane, to which the backside of the die is attached. This scheme is illustrated in Figure 3.1.

This conceptual drawing shows the test chip, with test structures similar to those in Figure 2.1, attached to a ground plane on a ceramic substrate. The test structures are still probed with the same 50 Ω G-S-G micro-probes, but now the probe points have been moved off-chip. This allows an intimate connection, via the ground plane, between the ground of the two-port substrate network and the ground of the measurement system. The probes would connect to the on-chip

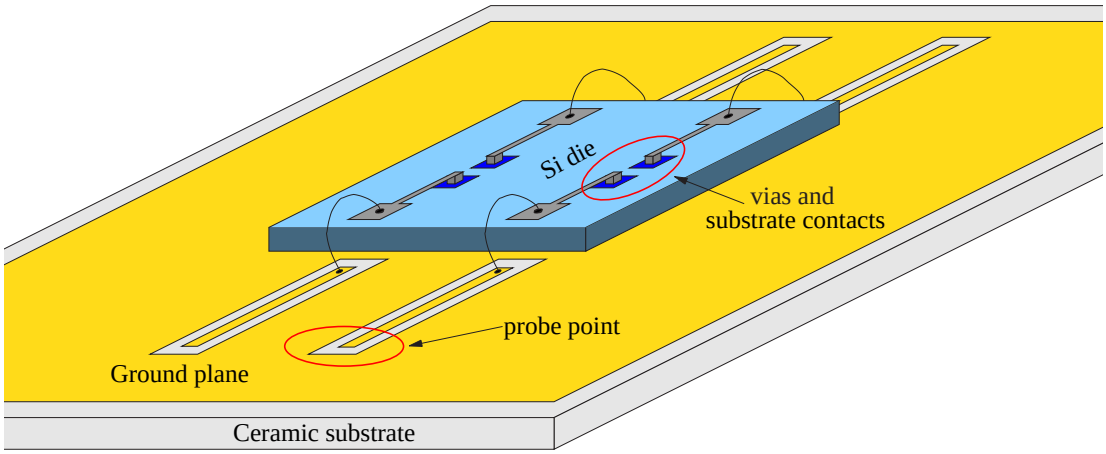


FIGURE 3.1. Preliminary test fixture concept.

test structures through off-chip transmission lines, bondwires, and on-chip metal traces.

While the problem of making a low-impedance ground connection is solved by the setup of Figure 3.1, another problem is introduced. By moving the probe points off-chip, and further away from the actual on-chip test structures, which are the subject of the measurements, significant test fixture parasitics are introduced into the circuit being measured. These parasitics can, in fact, dominate the measurements, obscuring the desired network parameters of the substrate network. A procedure is needed which allows for the characterization of test fixture parasitics and the removal of their effects from the measurements. This procedure is known as deembedding. Because the process of deembedding, and the ability to do so accurately, played a central role in the design of the test fixture, the theory behind deembedding will be discussed briefly in the following section, prior to further discussion of the test fixture itself.

3.2. Deembedding Theory

Deembedding is the process of characterizing the parasitics of the test fixture in terms of series impedances, shunt admittances, or a set of any convenient two-port network parameters, then using these parameters to remove the test fixture effects from the measurements. This process allows the obscured network parameters of the device-under-test, in this case the substrate network, to be extracted from the measured data. When developing a deembedding procedure, it is first necessary to develop an equivalent circuit model for the test fixture. This is done by decomposing the test fixture into smaller sections, which appear in series or shunt with the substrate network, and which, through either direct or indirect measurements, can be isolated and characterized.

Sections of the test fixture and the parameters that characterize them, fall into three categories: series impedances, shunt admittances, and more complex sections characterized by general network parameters, appearing in series with the substrate network.

3.2.1. Series Impedances

Parts of the test fixture may present impedances, which appear in series with the network being measured. Simple examples of this may be contact resistance of the probe, the impedance of a metal trace leading to the network being measured, or the series impedance presented by a bondwire. Figure 3.2 illustrates how these impedances appear in the test setup. Note that this network, like all other networks considered here, is assumed to be symmetric.

The measured network parameters of the entire two-port network of Figure 3.2 can be expressed in terms of impedance parameters as

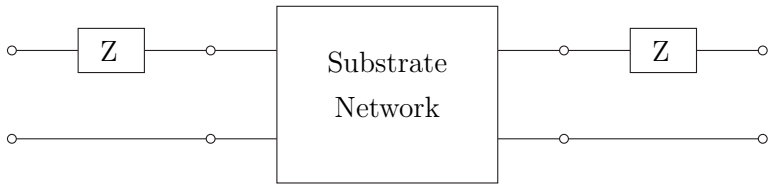


FIGURE 3.2. Parasitic impedance in series with the network being measured.

$$\mathbf{Z}_m = \begin{bmatrix} Z_{11,m} & Z_{12,m} \\ Z_{21,m} & Z_{22,m} \end{bmatrix} \tag{3.1}$$

The measured impedance parameters, $\mathbf{Z}_m$, can equivalently be expressed in terms of the series impedance, Z, and the impedance parameters of the substrate network, $\mathbf{Z}_{sub}$.

$$\mathbf{Z}_m = \begin{bmatrix} Z_{11,sub} + Z & Z_{12,sub} \\ Z_{21,sub} & Z_{22,sub} + Z \end{bmatrix} \tag{3.2}$$

From (3.2) it is clear that extracting the Z-parameters for the substrate network is simply a matter of determining the value of the series impedance, Z, and subtracting that from $Z_{11,m}$ and $Z_{22,m}$. Or, equivalently,

$$\mathbf{Z}_{sub} = \mathbf{Z}_m - \begin{bmatrix} Z & 0 \\ 0 & Z \end{bmatrix} \tag{3.3}$$

If portions of the test fixture can be modeled as lumped series impedances, and those impedances can be measured, then their effects can be removed from the measured network parameters using Eq. (3.3).

3.2.2. Shunt Admittances

The second category of test fixture parasitics, whose effects can be removed from the measured data, consists of shunt admittances. These are admittances

that appear in parallel with the substrate network, either shunting its ports to ground or one port to the other. Figure 3.3 illustrates a physical example of the origin of such admittances. Metal traces, with vias down to the p^+ substrate

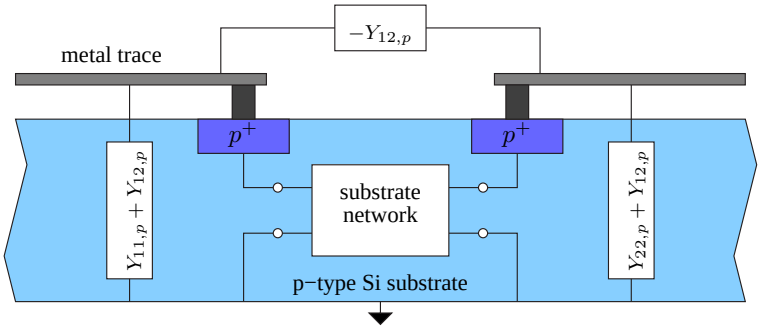


FIGURE 3.3. An example of parasitic shunt admittances associated with the test fixture.

contacts, have parasitic admittances to ground and across the gap between the substrate contacts. The measured admittance parameters, resulting from both the substrate network and the parasitic admittances, are

$$\mathbf{Y}_m = \begin{bmatrix} Y_{11,m} & Y_{12,m} \\ Y_{21,m} & Y_{22,m} \end{bmatrix} \tag{3.4}$$

The substrate network can similarly be characterized in terms of its Y-matrix, $\mathbf{Y}_{sub}$. A symmetric two-port network can be represented as a pi-network, described by its Y-parameters, so the parallel combination of the substrate network and the shunt admittances of the test fixture can be drawn as the network of Figure 3.4. Figure 3.4 shows that the measured admittance parameters can be expressed in terms of the admittance parameters of the substrate network, $\mathbf{Y}_{sub}$, and the admittance parameters which characterize the shunt admittances of the test fixture, $\mathbf{Y}_p$.

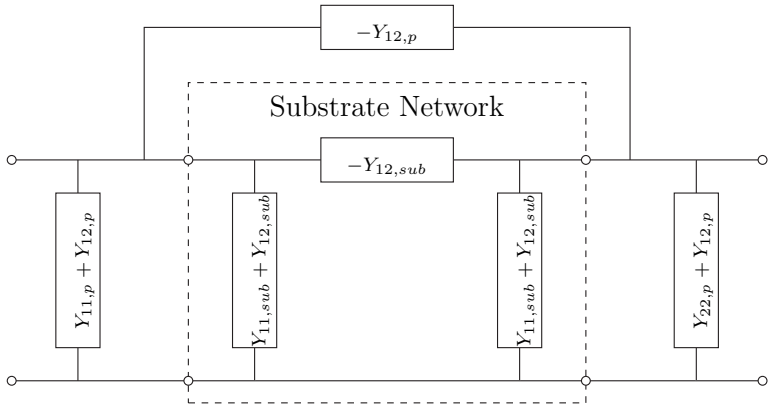


FIGURE 3.4. Pi-network representation of the substrate network and the parasitic test fixture admittances which shunt it.

$$\mathbf{Y}_m = \begin{bmatrix} Y_{11,sub} & Y_{12,sub} \\ Y_{21,sub} & Y_{22,sub} \end{bmatrix} + \begin{bmatrix} Y_{11,p} & Y_{12,p} \\ Y_{21,p} & Y_{22,p} \end{bmatrix} = \begin{bmatrix} Y_{11,sub} + Y_{11,p} & Y_{12,sub} + Y_{12,p} \\ Y_{21,sub} + Y_{21,p} & Y_{22,sub} + Y_{22,p} \end{bmatrix} \tag{3.5}$$

If the Y-parameters of the parasitic shunt admittances are known, then, according to (3.5), the Y-parameters for the substrate network can be extracted from the measurements by a simple Y-matrix subtraction.

$$\mathbf{Y}_{sub} = \mathbf{Y}_m - \mathbf{Y}_p \tag{3.6}$$

3.2.3. Series Two-Port Test Fixture Sections

The third, and most general, category of test fixture parasitics are those which appear in series with the substrate network-under-test, and which are best characterized by any type of two-port network parameters. Typical examples of test fixture sections which would fall into this category are sections of trace, either on-chip or off, which lead from the probes toward the test structure, and are not

adequately characterized by lumped impedances or admittances. These sections may be treated as two-port networks and characterized by their chain parameters. This scenario is illustrated in Figure 3.5.

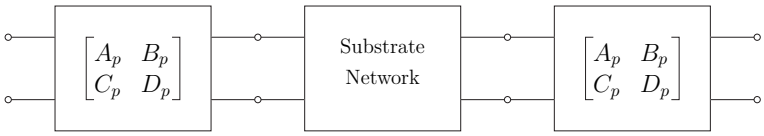


FIGURE 3.5. Chain parameter representation of test fixture parasitics appearing in series with the substrate network.

The chain parameters of a cascade of series-connected two-port networks are given by the product of the chain parameters of the individual two-ports. So the chain parameters of the network of of Figure 3.5 would be

$$\mathbf{T}_m = \mathbf{T}_p \cdot \mathbf{T}_{sub} \cdot \mathbf{T}_p \tag{3.7}$$

$$\mathbf{T}_m = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} \begin{bmatrix} A_{sub} & B_{sub} \\ C_{sub} & D_{sub} \end{bmatrix} \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} \tag{3.8}$$

If the chain parameters describing the series section of test fixture parasitics, $\mathbf{T}_p$, are known, then their effects on the measurement may be eliminated by simply right and left multiplying the measured chain parameters by the matrix inverse of the chain parameters for the parasitics, $\mathbf{T}_p^{-1}$.

$$\mathbf{T}_{sub} = \mathbf{T}_p^{-1} \cdot \mathbf{T}_m \cdot \mathbf{T}_p^{-1} \tag{3.9}$$

3.3. Test Fixture Assembly

A test fixture was designed to enable high-frequency network parameter measurements of two-port substrate network test structures fabricated on a test chip. The test fixture shown in Figure 3.6 comprises three main components: the

silicon die, on which the test structures are fabricated, a thin ceramic substrate, with thin film traces on one side and a ground plane on the other, and a solid copper block.

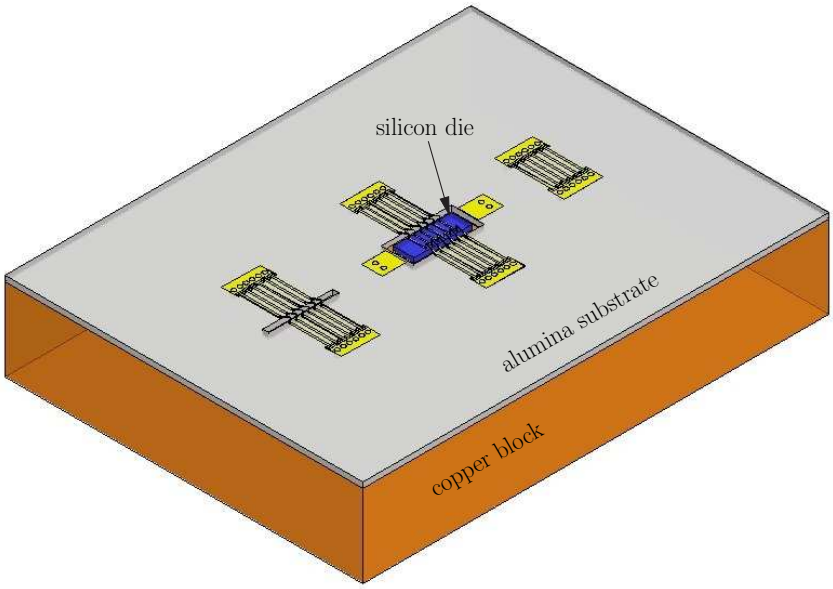


FIGURE 3.6. Test fixture assembly.

3.3.1. The Test Chip and On-Chip Test Structures

A test chip was designed and fabricated through MOSIS using a 0.35 μm TSMC process. The chip is roughly 2 mm x 5 mm and contains four sub-dice, which were singulated after receiving the larger die from MOSIS. Each of the smaller sub-dice is roughly 1 mm x 2 mm, and contains four substrate test structures and two structures to be used for deembedding. Four sub-dice, each with four distinct test structures, yield a total of 16 unique test structures. Each test structure consists of a pair of p^+ substrate contacts. The size of the substrate

TABLE 3.1. Dimensions of the on-chip test structures.

Test Structure	**Contact Size**	**Spacing**
1	10 μm x 10 μm	20 μm
2	60 μm x 60 μm	20 μm
3	10 μm x 60 μm	20 μm
4	50 μm x 100 μm	20 μm
5	10 μm x 10 μm	50 μm
6	60 μm x 60 μm	50 μm
7	10 μm x 60 μm	50 μm
8	50 μm x 100 μm	50 μm
9	10 μm x 10 μm	100 μm
10	60 μm x 60 μm	100 μm
11	10 μm x 60 μm	100 μm
12	50 μm x 100 μm	100 μm
13	10 μm x 10 μm	200 μm
14	60 μm x 60 μm	200 μm
15	10 μm x 60 μm	200 μm
16	50 μm x 100 μm	200 μm

contacts, and the distance that separates them, is varied from one contact to the next. Each sub-die has four different-sized contacts, all at a single spacing. Table 3.1 lists the dimensions of all 16 test structures.

Top metal traces (metal-4), 60 μm wide, run straight in from the bond pads at each edge of the die to the substrate contacts, where they make contact

to the p^+ diffusions with vias. A photograph of one of the sub-dice is shown in Figure 3.7.

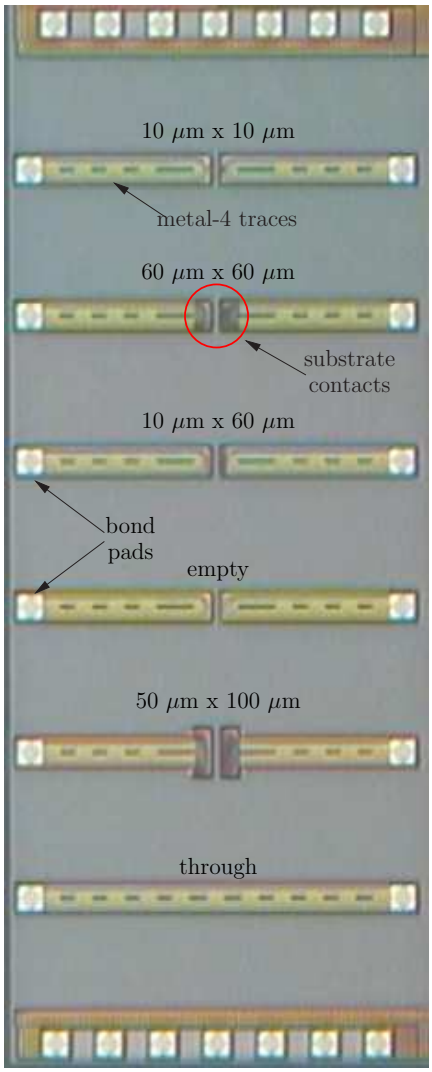


FIGURE 3.7. Die photo of the test chip, showing four test structures and two deembedding structures.

Note that along with the four test structures the layout includes an empty structure, which contains identical metal traces to the other structures, but no substrate contacts, and a through structure, which is simply a 60 μm-wide metal-4

trace running straight across the die. These two structures are used for deembedding, and their function is described in Sections 4.4 and 4.5.

3.3.2. The Ceramic Substrate

The ceramic substrate is 0.010" (254 μm) thick, and is made of alumina (Al_2O_3). A solid metal ground plane covers the bottom side of the substrate. A thin-film circuit consisting of probe pads and transmission lines is fabricated on the top side. The probe ground pads on the top side connect to the back side ground plane through vias.

The alumina substrate contains a cutout, which is sized to be slightly larger than the die. The substrate is soldered onto the copper block, which then becomes the ground plane for the substrate. Attaching the substrate to the copper block transforms the cutout to a cavity, the bottom of which is the exposed ground plane of the copper block. The die is conductively bonded to the copper block inside the cavity. The die and the ceramic substrate are roughly the same thickness, so the surface of the die lies flush with the surface of the ceramic. A closer view of the die, mounted in the cavity, is provided by Figure 3.8.

The test structures on the die connect, via metal-4 traces, to bond pads on the edge of the die (see Figure 3.7). These bond pads are wire-bonded to transmission lines on the top side of the ceramic. The transmission lines lead away from the die to the probe pads. There, they become the signal pads for the G-S-G probes, and are interdigitated with the probe ground pads. The probe ground pads connect directly to the backside ground plane through nearby vias.

The transmission lines, which are probed with the 50 Ω G-S-G microprobes, are 100 μm wide. The dimensions of the traces were dictated by the

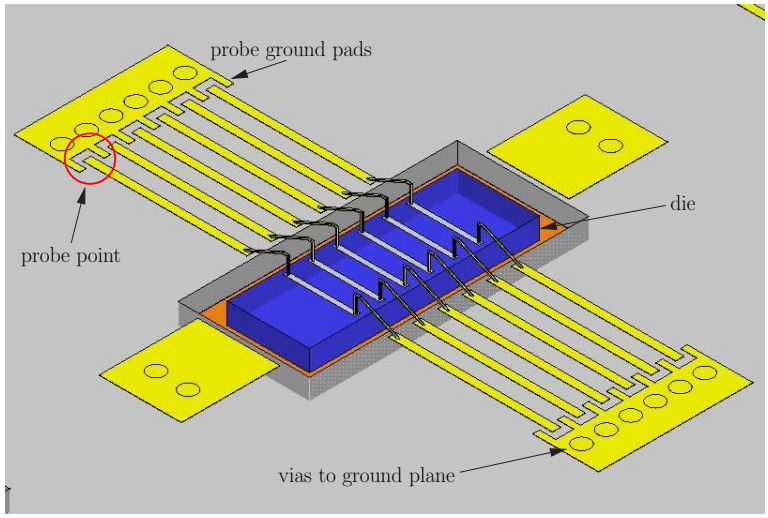


FIGURE 3.8. Close-up view of the die mounted in the cavity.

dimensions of the probes, whose leads are on a 150 μm pitch, and by metal-to-metal spacing requirements. Given these constraints, 100μm-wide traces, were the widest allowable. This width provides a characteristic impedance of approximately 70 Ω, presenting a mismatch to the the 50 Ω probes. This is not a concern, because the characteristics of the traces will be calibrated out as part of the deembedding process.

Along with the cavity and the traces for mounting and making connections to the die, the ceramic substrate contains two sets of deembedding structures, which are used for test fixture characterization. The first, shown in Figure 3.9, is a set of transmission lines identical to those which connect to each side of the die. Unlike the transmission lines connecting to the die, these lines have probe pads on both ends. This allows them to be probed and characterized with two-port network analyzer measurements. Once characterized, their network parameters can be used in the deembedding process.

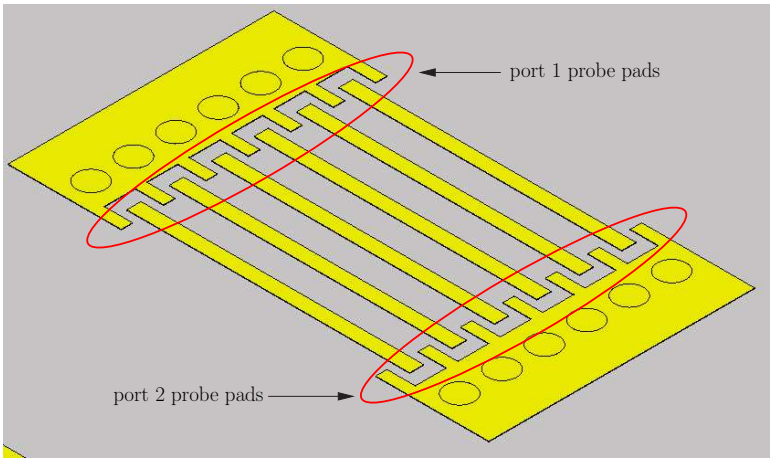


FIGURE 3.9. Transmission line characterization structures.

The second set of deembedding structures, shown in Figure 3.10, comprises two sets of probe pads and transmission lines, identical to those which connect to the die. The two sets of transmission lines are separated by a trench. The trench,

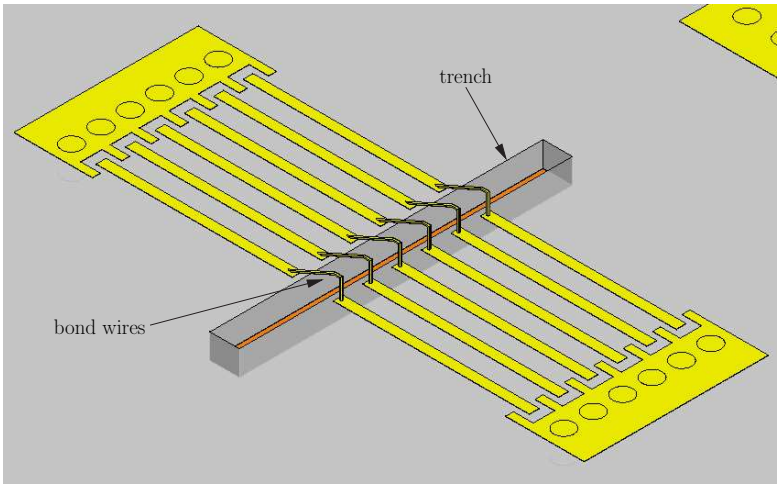


FIGURE 3.10. Bondwire characterization structures.

like the cavity in which the die is mounted, is formed by a cutout in the ceramic substrate. The trench is sized so that its narrow dimension is the same as the gap which surrounds the die in the cavity. Transmission lines on opposite sides of the trench connect via bondwires, which span the trench. These bondwires are

intended to be identical to those which connect the transmission lines to the bond pads on the die. These structures enable the characterization of the bondwires by allowing them to be probed and measured with the network analyzer. The network parameters of the bondwires measured here can then be used later in the deembedding process.

Both the transmission line and bondwire characterization structures comprise six sets of adjacent traces, similar to those which connect to the chip. The proximity of neighboring traces and bondwires will result in different traces and bondwires having different two-port parameters depending on their location in the group. The traces and bondwires on the outside of the group will be characterized by different two-port parameters than those which characterize the traces and bondwires located one in from the outside, whose two-port parameters will in turn differ from those characterizing the inner-most traces or bondwires. Due to the symmetry of the six-trace-wide structures, they can be completely characterized with three sets of two-port parameters. These structures will allow bondwires and transmission lines to be characterized more accurately than would be possible if the bondwire and transmission line characterization structures consisted only of single traces and bondwires.

The bondwire characterization structures of Figure 3.10 make clear the motivation for mounting the die in a cavity, such that its surface is flush with the surface of the ceramic. Were the die to be mounted on top of a ground plane on the topside of the substrate, as shown in the preliminary conceptual drawing of Figure 3.1, then it would be much more difficult to accurately replicate, for the purpose of characterization, both the length and configuration of the bondwires that make contact to the die.

4. A FOUR-STEP DEEMBEDDING PROCEDURE

The first step in the design of a deembedding procedure is to develop a model that adequately describes the important parasitics of the test fixture surrounding the network being measured. The model may consist of lumped impedances and admittances, along with two-port blocks, characterized by two-port network parameters. Once a model has been established, the next step is to design a set of deembedding test structures, along with a measurement procedure that allows the impedance, admittance, and the two-port network parameter values, that characterize the model, to be obtained.

The simplest and most frequently used deembedding procedure for on-chip measurements is Y-parameter subtraction. The Y-parameter subtraction scheme assumes that the test fixture can be adequately modeled as admittances that shunt the network under test, as in Figures 3.3 and 3.4. The parasitic shunt admittances are measured from an empty structure, which is a test structure that does not contain the network under test. The measured Y-matrix of the empty structure is subtracted from the measured Y-matrix of a full test structure, yielding the deembedded two-port parameters for the network under test. For certain test fixtures, networks under test, and measurement frequency ranges, simple Y-parameter subtraction may provide suitable deembedding accuracy.

Recognizing the limits of the simple test fixture model associated with Y-parameter subtraction, particularly at higher frequencies, other more rigorous deembedding procedures have been developed [11–15]. These deembedding schemes are based on test fixture models that more accurately account for the most significant parasitics.

4.1. Test Fixture Model

Prior to taking any measurements the network analyzer will be calibrated to the probe tips in a separate calibration procedure. All parts of the test fixture between the 50 Ω probe tips and the substrate contacts become part of the measurement, and therefore must be accounted for in the equivalent circuit model for the test fixture.

The test fixture between the probe tips and the substrate contacts consists of three main components: the micro-strip transmission lines on the ceramic substrate, the bondwires connecting those lines to the on-chip traces, and the on-chip traces themselves. An equivalent test fixture circuit model, which accounts for these components is given in Figure 4.1.

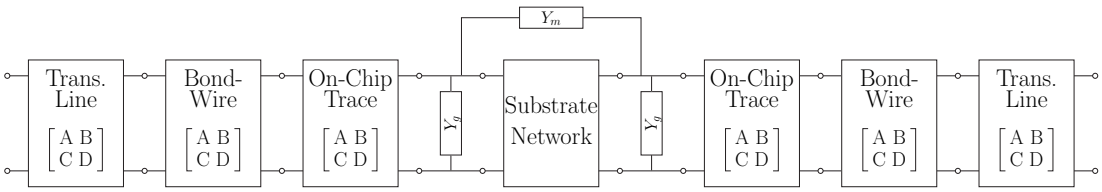


FIGURE 4.1. Test fixture model used for deembedding.

Three of the blocks, the micro-strip transmission lines, the bondwires, and the on-chip sections of trace, are treated as series-connected two-port networks, and are characterized using their chain parameters. The final section of the test fixture model comprises the admittances that shunt the substrate network to ground, Y_g, and from port to port, Y_m. This block is characterized using its admittance matrix. In the center of the model is the substrate network which will ultimately be described with any desired set of two-port network parameters. The network parameters of the substrate will be extracted from the measured data as the effects of the other blocks are stripped away in four steps.

4.2. Step One: Micro-Strip Transmission Lines

The outer-most block in the model comprises the micro-strip transmission lines, which lead from the probe pads to the bondwires. The transmission line block is characterized by its chain parameters. Network analyzer measurements taken on the micro-strip transmission lines of Figure 3.9 yield S-parameters for the lines, which can be converted into the corresponding chain parameters. Once the chain parameters are known, it is a simple matter to remove the effects of the transmission lines from the measured data, as described in Section 3.2.3. Simply left- and right-multiply the measured chain parameter matrix, $\mathbf{T}_m$, by the inverse chain parameter matrix of the micro-strip lines, $\mathbf{T}_{tl}^{-1}$.

$$\mathbf{T}_1 = \mathbf{T}_{tl}^{-1} \cdot \mathbf{T}_m \cdot \mathbf{T}_{tl}^{-1} \tag{4.1}$$

The result, $\mathbf{T}_1$, is the chain parameter matrix for the substrate coupling measurement following the first deembedding step. The subscript denotes the number of deembedding steps the data has undergone, incrementally increasing with each successive step, as more and more of the test fixture effects are peeled away. Figure 4.2 shows a model of the physical network corresponding to the measured data after the first deembedding step.

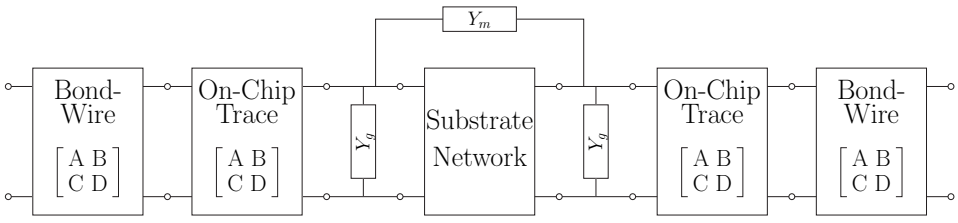


FIGURE 4.2. Model of the network corresponding to the data after step one of the deembedding procedure.

4.3. Step Two: Bondwires

The next block of test fixture parasitics to be removed, according to Figure 4.2, is that of the bondwires. Bondwires tend to look primarily inductive, and in many applications they are adequately modeled as lumped inductances. Simulations, however, demonstrated that in this case treating the bondwires as simple lumped inductances introduces unacceptable errors into the deembedding process. If they are to be modeled with simple lumped elements, a CLC pi-network is more appropriate. Equivalently, the bondwires can be characterized in terms of general two-port parameters.

Network analyzer measurements taken on the structures of Figure 3.10 yield a set of S-parameters. These S-parameters describe a network including not only the bondwire, but also the series sections of the transmission line connected to each port of the bondwire. Written in terms of chain parameters, the measured network parameters of the bondwire characterization structure can be expressed as

$$\mathbf{T}_{bw,m} = \mathbf{T}_{tl} \cdot \mathbf{T}_{bw} \cdot \mathbf{T}_{tl} \tag{4.2}$$

Clearly, the chain parameters for the bondwires can be extracted by applying the first deembedding step to the measured data.

$$\mathbf{T}_{bw} = \mathbf{T}_{tl}^{-1} \cdot \mathbf{T}_{bw,m} \cdot \mathbf{T}_{tl}^{-1} \tag{4.3}$$

Now that the bondwire chain parameters have been deembedded, the second deembedding step is completed by left- and right-multiplying the data from step one, $\mathbf{T}_1$, by the inverse of the bondwire chain parameter matrix, $\mathbf{T}_{bw}^{-1}$.

$$\mathbf{T}_2 = \mathbf{T}_{bw}^{-1} \cdot \mathbf{T}_1 \cdot \mathbf{T}_{bw}^{-1} \tag{4.4}$$

The data that results from this second deembedding step, $\mathbf{T}_2$, corresponds to the physical network modeled by Figure 4.3.

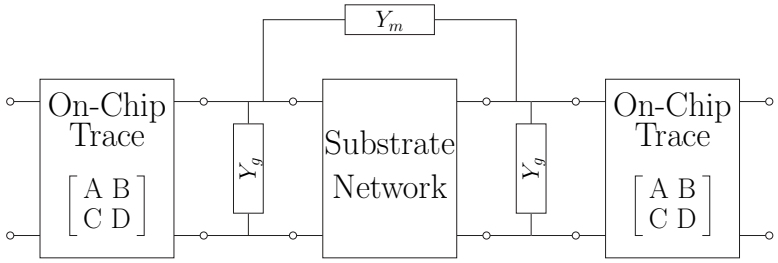


FIGURE 4.3. Model of the network corresponding to the data after step two of the deembedding procedure.

4.4. Step Three: On-Chip Traces

The third deembedding step involves removal of the effects due to the on-chip traces. Again, the first step in this process will be taking measurements of deembedding structures, that will allow the network parameters for these traces to be obtained. Along with the four substrate coupling test structures on each chip, are two structures dedicated solely for the purpose of deembedding. One of these, as shown in figure 3.7, is a through trace, spanning the width of the die. Network analyzer measurements of the through structure yield S-parameters, which are then converted to chain parameters. These chain parameters correspond to a network consisting of not only the on-chip through trace, but also the bondwires and micro-strip transmission lines. These chain parameters can be expressed as

$$\mathbf{T}_{thru,m} = \mathbf{T}_{tl} \cdot \mathbf{T}_{bw} \cdot \mathbf{T}_{thru} \cdot \mathbf{T}_{bw} \cdot \mathbf{T}_{tl} \tag{4.5}$$

The chain matrix for the on-chip through trace alone can be retrieved from the measured chain parameters, $\mathbf{T}_{thru,m}$, by passing the data through deembedding steps one and two. First, the effects of the micro-strip lines are removed.

$$\mathbf{T}_{thru,1} = \mathbf{T}_{tl}^{-1} \cdot \mathbf{T}_{thru,m} \cdot \mathbf{T}_{tl}^{-1} \tag{4.6}$$

Then, the bondwire effects are stripped away, yielding the chain parameters for the through trace.

$$\mathbf{T}_{thru} = \mathbf{T}_{bw}^{-1} \cdot \mathbf{T}_{thru,1} \cdot \mathbf{T}_{bw}^{-1} \tag{4.7}$$

This chain matrix, $\mathbf{T}_{thru}$, applies to the entire length of the through trace that spans the die. What is needed to proceed with the deembedding process, however, is the chain parameter matrix for only the short sections of trace leading up to the substrate contacts. Figure 4.4 shows the dimensions of both the through trace and the shorter segments of the trace leading to the substrate contacts.

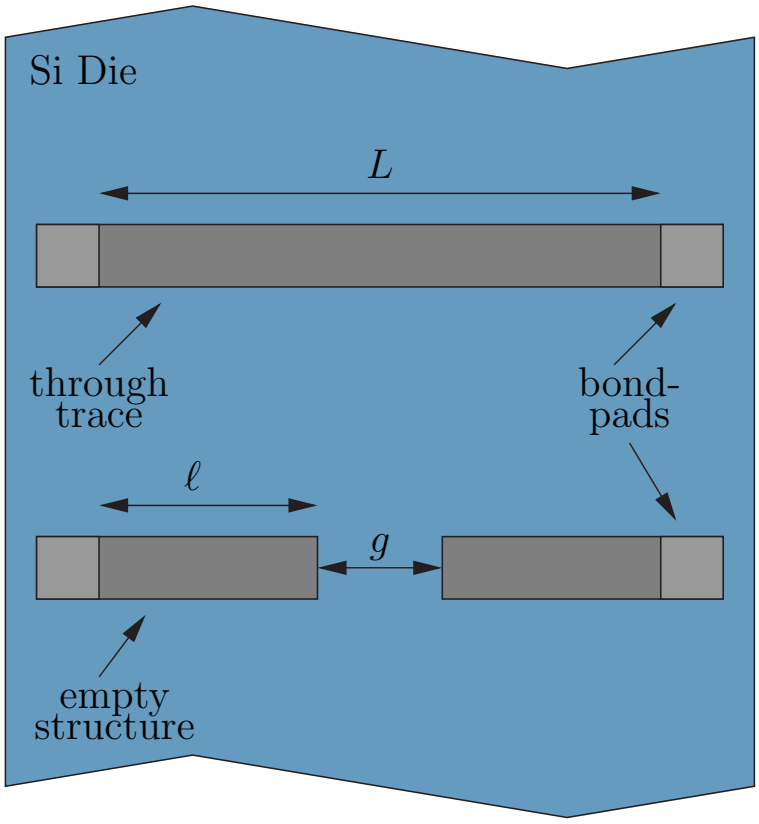


FIGURE 4.4. Dimensions of the through trace and trace segments.

The deembedded chain matrix, $\mathbf{T}_{thru}$, represents a trace of length L. A procedure is therefore needed to convert $\mathbf{T}_{thru}$ into a set of chain parameters describing a trace of length ℓ. This will be accomplished through a procedure that will be referred to as chain parameter factorization.

4.4.1. Chain Parameter Factorization

Given a trace of length L with chain matrix, $\mathbf{T}_L$, there exists a chain matrix, $\mathbf{T}_{\frac{L}{2}}$, such that

$$\mathbf{T}_L = \mathbf{T}_{\frac{L}{2}} \cdot \mathbf{T}_{\frac{L}{2}} \tag{4.8}$$

where $\mathbf{T}_{\frac{L}{2}}$ is the chain matrix for a trace of length $\frac{L}{2}$. This chain matrix can in turn be factored into the product of two identical chain matrices representing traces of length $\frac{L}{4}$.

$$\mathbf{T}_L = \mathbf{T}_{\frac{L}{4}} \cdot \mathbf{T}_{\frac{L}{4}} \cdot \mathbf{T}_{\frac{L}{4}} \cdot \mathbf{T}_{\frac{L}{4}} \tag{4.9}$$

This factorization procedure could be carried out n times, resulting in the chain matrix for a trace of length $\frac{L}{2^n}$.

The length of the through trace in Figure 4.4 is L, the length of the shorter trace segments are ℓ, and the length of the gap between the trace segments is g. The ratio of the length of the gap, g, to the length of a shorter segment, ℓ, may then be expressed as

$$\frac{g}{\ell} = \frac{g}{\frac{L-g}{2}} = \frac{m}{k} \tag{4.10}$$

where m and k are the smallest integers satisfying the equation. The required number of successive factorizations of the chain parameters of the trace of length, L, is then given by

$$n = log_2(m + 2k) \tag{4.11}$$

Following the n successive factorizations, the resulting chain parameters, $\mathbf{T}_{\frac{L}{2^n}}$, represent a trace of length $\frac{L}{2^n}$, or, equivalently, length $\frac{\ell}{k}$. They can then be used to obtain the chain matrix of the shorter segment of trace of length ℓ.

$$\mathbf{T}_\ell = \mathbf{T}^k_{\frac{L}{2^n}} \tag{4.12}$$

The procedure just described is useful only if a method is available that allows the chain parameters for a given length of trace to be factored into chain parameters for a trace of half that length. The method used for this factorization makes use of the fact that the on-chip trace is a network that is both symmetric and reciprocal. Symmetry of the on-chip trace implies that

$$A_{thru} = D_{thru} \tag{4.13}$$

and the reciprocal nature of the network implies that

$$|\mathbf{T}_{thru}| = A_{thru} \cdot D_{thru} - B_{thru} \cdot C_{thru} = 1 \tag{4.14}$$

which says that the determinant of the chain matrix is unity [16]. Using these properties, it is possible to express the chain parameters for the full through trace, of length L, in terms of the chain parameters of halved sections of trace, of length $\frac{L}{2}$.

$$\mathbf{T}_{thru} = \begin{bmatrix} A_{\frac{L}{2}} & B_{\frac{L}{2}} \\ C_{\frac{L}{2}} & D_{\frac{L}{2}} \end{bmatrix} \cdot \begin{bmatrix} A_{\frac{L}{2}} & B_{\frac{L}{2}} \\ C_{\frac{L}{2}} & D_{\frac{L}{2}} \end{bmatrix} \tag{4.15}$$

$$\mathbf{T}_{thru} = \begin{bmatrix} 2A^2_{\frac{L}{2}} - 1 & 2A_{\frac{L}{2}}B_{\frac{L}{2}} \\ 2C_{\frac{L}{2}}D_{\frac{L}{2}} & 2D^2_{\frac{L}{2}} - 1 \end{bmatrix} \tag{4.16}$$

What's shown in (4.16) is a set of four equations, which can be solved for the chain parameters of the halved trace sections as follows:

$$A_{\frac{L}{2}} = \sqrt{\frac{A_{thru}+1}{2}} = D_{\frac{L}{2}} \tag{4.17}$$

$$D_{\frac{L}{2}} = \sqrt{\frac{D_{thru}+1}{2}} = A_{\frac{L}{2}} \tag{4.18}$$

$$B_{\frac{L}{2}} = \frac{B_{thru}}{2A_{\frac{L}{2}}} \tag{4.19}$$

$$C_{\frac{L}{2}} = \frac{C_{thru}}{2D_{\frac{L}{2}}} \tag{4.20}$$

This factorization process is carried out n times, where n is given by (4.11), resulting in the chain parameters for a trace of length $\frac{L}{2^n}$, $\mathbf{T}_{\frac{L}{2^n}}$. The chain parameters for the length-ℓ section of trace, $\mathbf{T}_t$, are then given by a cascade of k $\mathbf{T}_{\frac{L}{2^n}}$ matrices, as described by (4.12).

$$\mathbf{T}_t = \mathbf{T}_{\frac{L}{2^n}}^k \tag{4.21}$$

The third deembedding step, the removal of the effects of the on-chip trace segments, can now be completed. Simply left- and right-multiply the chain parameters of (4.4), $\mathbf{T}_2$, which describe the network of Figure 4.3, by the inverse of the chain matrix of the on-chip trace segments, $\mathbf{T}_t^{-1}$.

$$\mathbf{T}_3 = \mathbf{T}_t^{-1} \cdot \mathbf{T}_2 \cdot \mathbf{T}_t^{-1} \tag{4.22}$$

Figure 4.5 shows the physical network, which corresponds to the data resulting from this third deembedding step.

4.5. Step Four: Shunt Admittances

As evident from Figure 4.5, the final parasitic test fixture elements remaining are the admittances shunting the substrate network. The value of these admittances can be obtained through a measurement of the empty structure. Shown in the chip layout of Figure 3.7, the empty structure is identical to the full

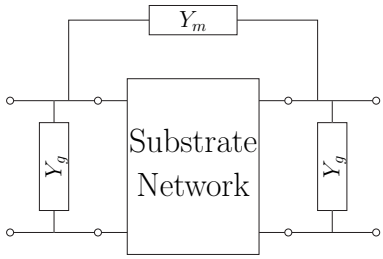


FIGURE 4.5. Model of the network corresponding to the data after step three of the deembedding procedure.

test structures, except that it contains no p^+ substrate contacts. The length, g, of the gap between the traces of the empty structure (Figure 4.4) is identical to that of all other structures, but the traces do not via down to make contact with the substrate.

Measurements of the empty structure can be used to obtain the values of the parasitic admittances, Y_g and Y_m. Once the values of these admittances are determined, the corresponding Y-matrix can be subtracted from the Y-matrix resulting from the third deembedding step, $\mathbf{Y}_3$. This step, described in Section 3.2.2, is referred to as Y-parameter subtraction. It often represents the extent of the deembedding performed when taking on-chip measurements, and is the deembedding procedure used when measurements were taken on the test structures shown in Figure 2.1.

The admittance values needed to complete the deembedding are described by what will be referred to as the Y-parameters of the empty structure, $\mathbf{Y}_e$. The empty structure is, however, surrounded by the same parasitics that surround the full test structures. The Y-matrix of the empty structure, $\mathbf{Y}_e$, will therefore have to be deembedded from the measured data using deembedding steps one through

three. The measured chain parameters for the empty structure, $\mathbf{T}_{e,m}$, can be expressed as

$$\mathbf{T}_{e,m} = \mathbf{T}_{tl} \cdot \mathbf{T}_{bw} \cdot \mathbf{T}_t \cdot \mathbf{T}_e \cdot \mathbf{T}_t \cdot \mathbf{T}_{bw} \cdot \mathbf{T}_{tl} \tag{4.23}$$

First, the effects of the micro-strip transmission lines are removed.

$$\mathbf{T}_{e,1} = \mathbf{T}_{tl}^{-1} \cdot \mathbf{T}_{e,m} \cdot \mathbf{T}_{tl}^{-1} \tag{4.24}$$

Then, the bondwire effects are stripped away, yielding the chain parameters for the entire on-chip portion of the empty structure.

$$\mathbf{T}_{e,2} = \mathbf{T}_{bw}^{-1} \cdot \mathbf{T}_{e,1} \cdot \mathbf{T}_{bw}^{-1} \tag{4.25}$$

In the third step, the effects of the on-chip trace segments are eliminated, yielding the chain parameters of the empty structure.

$$\mathbf{T}_e = \mathbf{T}_t^{-1} \cdot \mathbf{T}_{e,2} \cdot \mathbf{T}_t^{-1} \tag{4.26}$$

The resulting chain parameters, $\mathbf{T}_e$, are then converted to the Y-matrix, $\mathbf{Y}_e$, representing the admittances that shunt the substrate network as shown in Figure 4.5.

The fourth, and final, step of the deembedding procedure is completed by subtracting the Y-parameters of the empty structure from the Y-parameters resulting from step three.

$$\mathbf{Y}_{sub} = \mathbf{Y}_3 - \mathbf{Y}_e \tag{4.27}$$

The resulting Y-parameters, $\mathbf{Y}_{sub}$, correspond to the substrate network itself, with the effects of all test fixture parasitics eliminated from the data.

5. SIMULATION

Extensive simulations greatly aided the design of the test fixture, the on-chip test structures, and the four-step deembedding procedure. Two categories of simulations were performed, each using a different simulator. The first group of simulations included the entire test fixture, from probe tip to probe tip, and was performed using Ansoft's HFSS (High Frequency Structure Simulator), a three-dimensional, electromagnetic field solver [17]. In order to ease memory requirements, the model for the silicon chip was greatly simplified in these simulations. The simplified model does not account for the behavior of the lossy silicon substrate or of the actual substrate networks themselves. The purpose of this first group of simulations was to enable the design and validation of the physical test fixture, including the on-chip interconnects, as well as the equivalent circuit model and step-by-step deembedding procedure outlined in Chapter 4.

The second category of simulations included the substrate test structures fabricated in a heavily-doped silicon substrate from a TSMC 0.35 μm process. These simulations, which included only the on-chip substrate contacts surrounded by the heavily-doped substrate, were performed in EPIC (Extraction of Parasitics in Integrated Circuits), a Green's Function-based substrate simulator [18]. The test fixture, as well as the on-chip interconnects, were excluded from these simulations. The objective of these simulations was to obtain network parameter data for the substrate networks defined by the pairs of substrate contacts of Table 3.1.

This two-part simulation plan allowed for design and validation of both the on-chip and off-chip portions of the test fixture, without exceeding the memory available for simulation. It also provided simulated two-port substrate network parameters that can be compared to the data obtained from measurements.

5.1. Probe-to-Probe Test Fixture Simulations

The purpose of the first group of simulations was the design of the test fixture, including the on-chip interconnects, as well as the development of the test fixture model and the deembedding plan. The model used for these simulations includes the entire test fixture, but substitutes a greatly simplified model for the silicon substrate.

The real test chip is fabricated in a heavily-doped substrate, with a low-resistivity bulk. For the purposes of simulation the substrate can be modeled as having three discrete layers, each with a different resistivity. This substrate model will be discussed in Section 5.2, which covers the simulation of the on-chip test structures. The finite-element mesh generated by HFSS for such a substrate model becomes quite dense, resulting in prohibitively large memory requirements when included in the model of the entire test fixture. Memory requirements for this first set of simulations were eased by replacing the model for the silicon substrate with a uniform block of lossless dielectric, whose dielectric constant was arbitrarily chosen to be that of silicon dioxide. Because the substrate is modeled as a lossless dielectric, it is not possible to include, as the networks under test, the actual substrate contacts and substrate networks in these full test fixture simulations. Instead, the substrate network was replaced with a variety of other simple networks such as transmission lines, resistors, and capacitors. Figure 5.1 shows the 3-D HFSS structure used for the simulation of a test fixture containing a 1 KΩ, 60 μm x 60 μm resistor.

The structure shown is a cut-away section of the full test fixture. It is kept as small as possible to limit the memory and time requirements for the simulation, while still being large enough to allow the simulator to arrive at an accurate

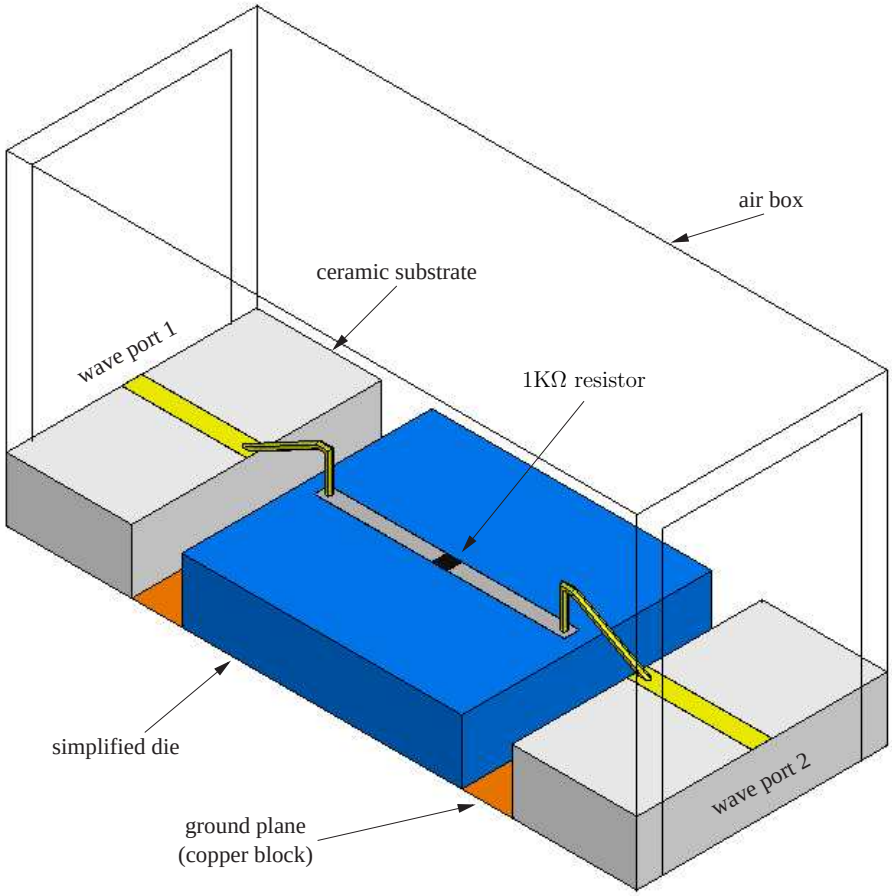


FIGURE 5.1. HFSS structure for the simulation of a 1 KΩ resistor embedded in the test fixture.

solution. Any volume of material added to the structure will be included in the finite-element mesh, and will increase the amount of memory required for the simulation. All unnecessary material, such as the full thickness of the copper block, has therefore been excluded from the simulation. The structure is surrounded by an air-box, which defines the volume over which the electromagnetic fields will be calculated. Stimuli are applied to the network through wave ports, which are defined by rectangles at the ends of the structure and the ends of the micro-strip traces.

Two-port network parameter measurements were simulated for the full test structure, containing the network under test, and for each of the on- and off-chip deembedding structures described in Chapter 3. The results of these simulations represent the complete set of data that will be obtained from actual network analyzer measurements on the physical test fixture. Simulated data is stored as S-parameters in Touchstone-formatted files, as it will be for measured data. The S-parameter files from the simulated measurements are fed into a Matlab program, which performs the deembedding and outputs network parameters for the substrate network, or, in the case of these simulations, a resistor.

Simulation facilitates the test fixture and deembedding procedure design by allowing the simulation ports to be placed at various points in the test fixture, yielding network parameters for isolated test fixture sections. For example, the accuracy of the first step of the deembedding procedure, elimination of the effects of the micro-strip transmission lines, can be evaluated by submitting the network parameters obtained from a simulation of the complete structure in Figure 5.1, to the first deembedding step, and comparing the resulting network parameters to those obtained from a simulation with the micro-strip lines removed from the structure.

In other words, the structure of Figure 5.1 is simulated and the effects of the micro-strip lines are stripped from the simulation by the first deembedding step. The resulting data is then compared to the network parameters obtained from a simulation of the structure shown in Figure 5.2(a). This structure serves as the reference network for the validation of the first deembedding step, and sets the standard by which the accuracy of this part of the deembedding process is judged. Similarly, the second step of deembedding can be evaluated by comparing the

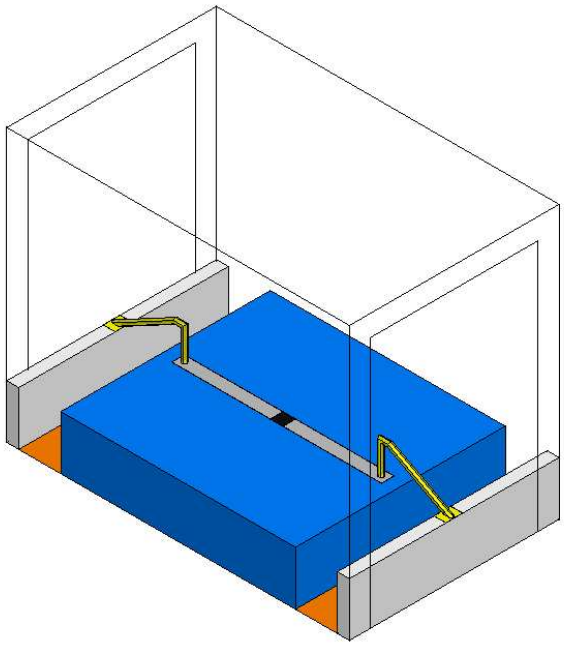
resulting network parameters to those obtained from simulation of the structure shown in Figure 5.2(b).

Discrepancies between the deembedded data and the data from the simulation of the corresponding reference network indicate problems either with the test fixture model (Figure 4.1), the deembedding procedure, or both. Discrepancies due to errors in the model can be remedied by either changing the model to more accurately reflect the test fixture, or by altering the test fixture design to better match the model. As the model becomes more complex, more measurements and perhaps additional deembedding test structures may be needed in order to obtain the parameters that characterize that model. For this reason, it is often preferable to alter the test fixture to conform to the simplest possible model.

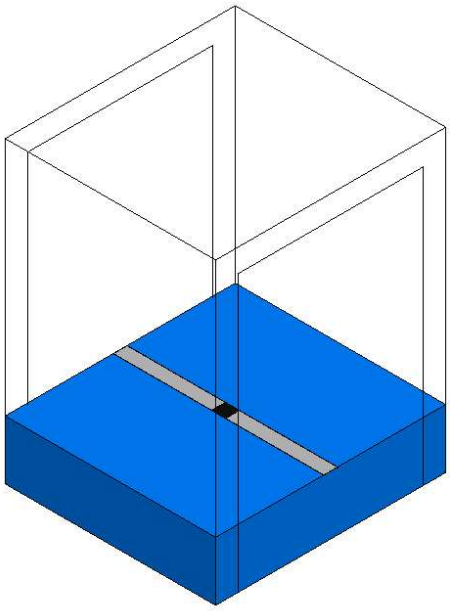
5.1.1. Simulations of a 1 KΩ Resistor

HFSS simulations of simple networks embedded in the test fixture, such as the 1 KΩ resistor of Figure 5.1, shaped the design of the test fixture and deembedding plan. This section will present the simulated S-parameters for that 1 KΩ resistor as the data progresses through each successive deembedding step.

Figure 5.3 shows the S-parameters resulting from simulation of the structure of Figure 5.1. These results represent the S-parameters that would be obtained from measurements taken of the 1 KΩ resistor embedded in the test fixture. Also plotted are the reference S-parameters for the resistor. The reference S-parameters, available due to the fact that these are simulations, represent the end goal of the deembedding procedure, and the standard by which its effectiveness will be judged.

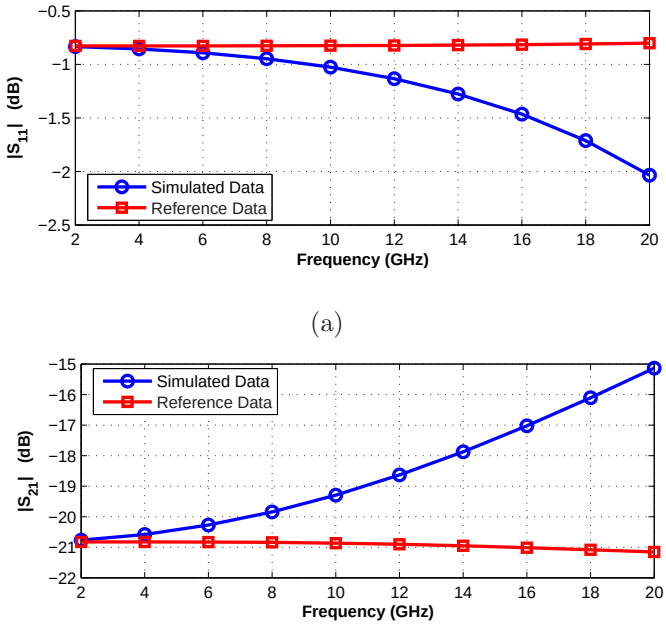


(a)



(b)

FIGURE 5.2. Reference networks for the (a) first and (b) second deembedding steps.



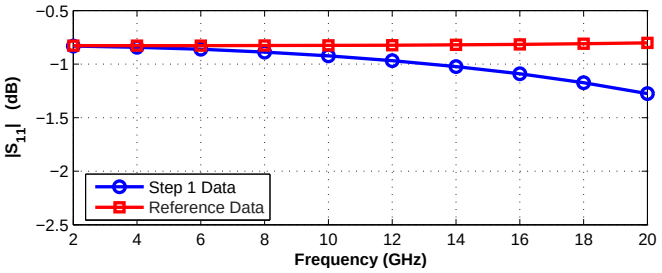
(a)

(b)

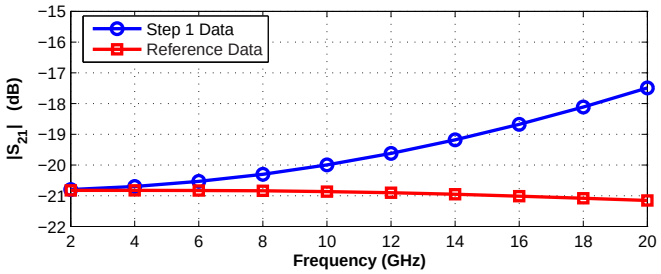
FIGURE 5.3. Simulated S-parameters for a 1 KΩ resistor embedded in the test fixture. (a) S_{11}, (b) S_{21}.

While the simulated data agree quite well with the reference S-parameters at 2 GHz, as the frequency increases and the parasitic effects of the test fixture become important, the simulated data diverge from the reference S-parameters. Note that the reference S-parameters are about what would be expected for an electrically small 1 KΩ resistor: $S_{21} \approx -21$ dB and $S_{11} \approx -0.8$ dB. Because the resistor is electrically small, even at 20 GHz, its S-parameters remain relatively constant over the frequency range.

Figures 5.4 through 5.7 show how the simulated S-parameters evolve throughout the deembedding procedure. The effectiveness of the deembedding procedure is illustrated as, with each successive deembedding step, the S-parameters converge to the reference S-parameters. The S-parameters following



(a)

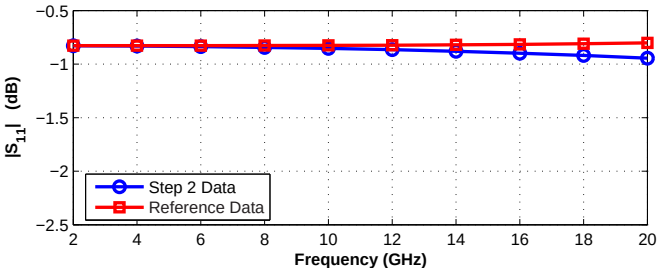


(b)

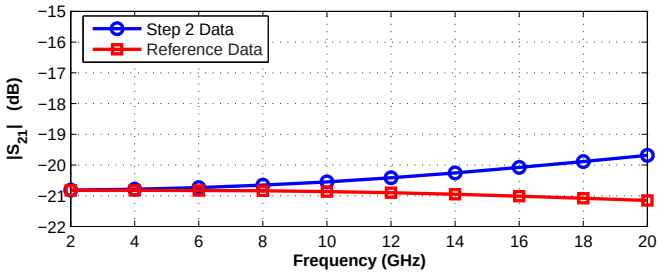
FIGURE 5.4. Simulated S-parameters for a 1 KΩ resistor following the first deembedding step. (a) S_{11} after step 1. (b) S_{21} after step 1.

the final deembedding step (Figure 5.7) show very good agreement with the refernce S-parameters.

The data in Figures 5.3 through 5.7 are presented in terms of S-parameters, because these are the two-port parameters directly obtained from network analyzer measurements, both real and simulated. However, it is the Y-parameters, and the corresponding self and mutual admittances, that are of most interest when developing and evaluating a model such as that of Figure 1.2. The deembedded self admittance, Y_{self}, and mutual admittance, Y_{mut}, for the resistor of Figure 5.1 are plotted in Figure 5.8.



(a)



(b)

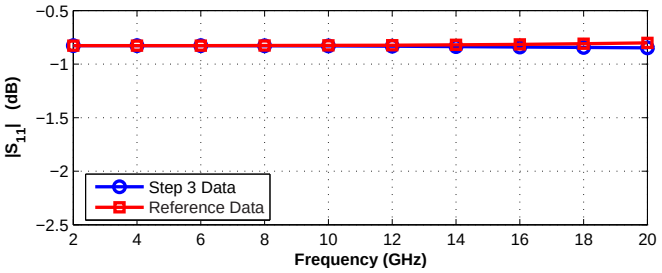
FIGURE 5.5. Simulated S-parameters for a 1 KΩ resistor following the second deembedding step. (a) S_{11} after step 2. (b) S_{21} after step 2.

Self admittance is the admittance of the shunt branches of an equivalent pi-network, and mutual admittance is the admittance of the series branch. These admittances can be expressed in terms of Y-parameters as follows:

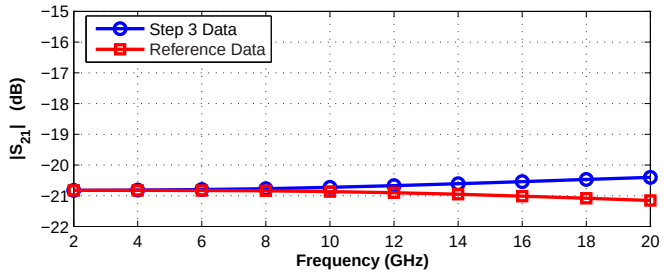
$$Y_{self} = Y_{11} + Y_{21} \tag{5.1}$$

$$Y_{mut} = -Y_{21} \tag{5.2}$$

The 1 KΩ, 60 μm x 60 μm resistor is electrically small over this frequency range, so it can be expected that its equivalent pi-network would essentially be a resistor, perhaps with some small amount of capacitive susceptance in the shunt legs. Since the resistor is placed on a lossless dielectric substrate, the self conductance should be zero. Additionally, it can be expected that the mutual conductance would decrease slightly from its low frequency value of 1 mS, due to the



(a)



(b)

FIGURE 5.6. Simulated S-parameters for a 1 KΩ resistor following the third deembedding step. (a) S_{11} after step 3. (b) S_{21} after step 3.

skin effect. These expectations are borne out in the plots of Figure 5.8. While there appears to be a significant discrepancy between the reference and deembedded self susceptance, B_{self}, note that the self susceptance of the reference network corresponds to a shunt capacitance of less than 2 fF, so it is not a large error.

5.2. Simulations of On-Chip Test structures

The second category of simulations, which were performed in EPIC, included only the on-chip substrate contacts and the heavily-doped silicon substrate that surrounds them. Neither the on-chip interconnects, nor off-chip test fixture were included. For these simulations, the simplified substrate model of Section 5.1

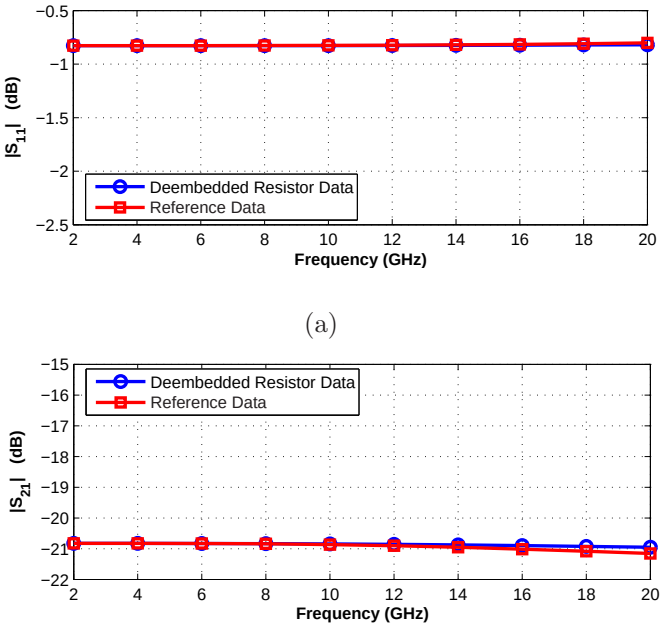
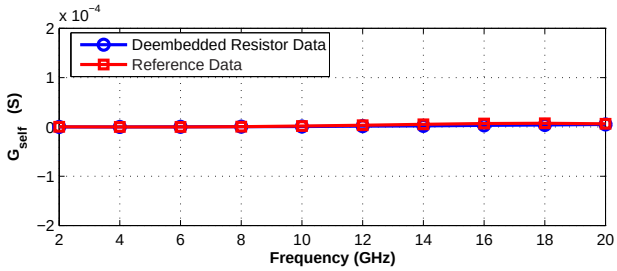


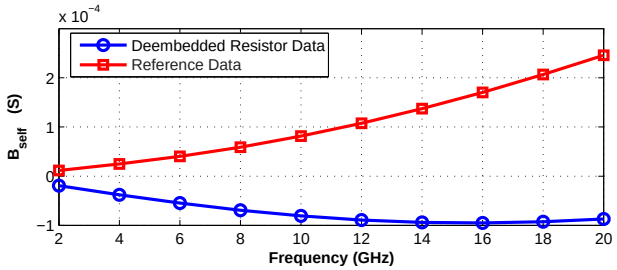
FIGURE 5.7. Simulated S-parameters for a 1 KΩ resistor following the final deembedding step. (a) S_{11} after step 4. (b) S_{21} after step 4.

was replaced with a more accurate model of the heavily-doped silicon substrate, on which the test chip is fabricated.

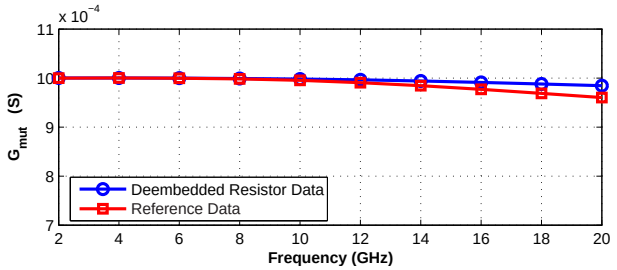
The heavily-doped substrate used in the TSMC 0.35 μm logic process can be modeled as comprising three discrete layers, as illustrated in Figure 5.9 [19]. This substrate profile is typical of substrates used for mixed-signal systems on chip, which may contain large, noisy digital blocks, along with sensitive analog circuitry. The bulk layer is a 245 μm-thick heavily-doped layer. This low-resistivity layer aids latchup prevention in the digital circuitry. The 4 μm-thick epitaxial layer has a higher resistivity of 10 Ω·cm, and serves to provide some degree of isolation between circuits on the chip. The top layer is the 1 μm-thick, 2 Ω·cm channel stop



(a)



(b)



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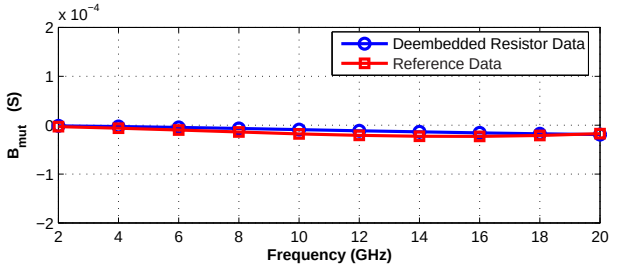


(d)

FIGURE 5.8. Simulated deembedded self and mutual admittances for the 1 KΩ resistor. (a) Self conductance, (b) self susceptance, (c) mutual conductance, and (d) mutual susceptance.

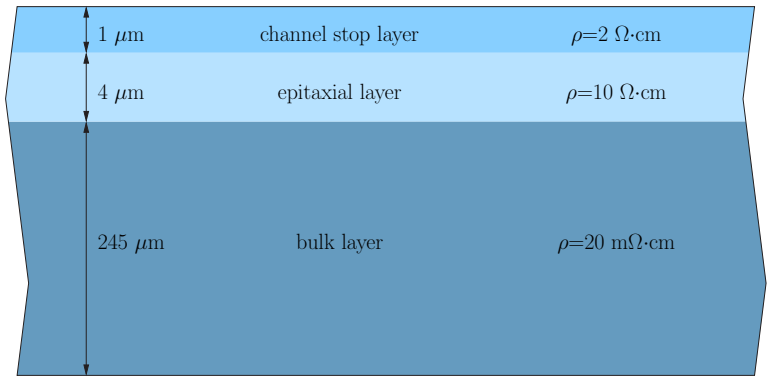


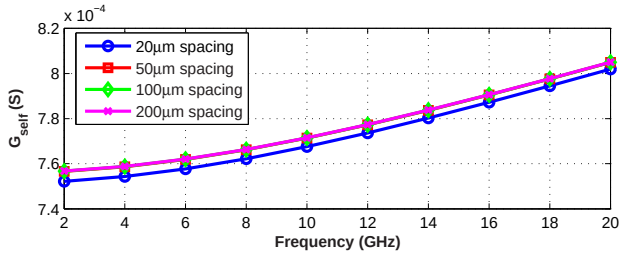
FIGURE 5.9. Three-layer substrate used for simulation.

layer. The three-layer model of Figure 5.9, served as the substrate upon which the pairs of substrate contacts were modeled for simulation in EPIC.

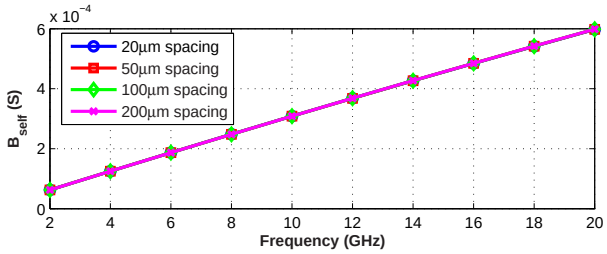
EPIC simulations were run for each of the test structures of Table 3.1. Deembedded mutual and self conductances and susceptances for each contact dimension are plotted, parameterized by contact spacing, in Figures 5.10 through 5.13.

Inspection of the simulated admittances shown in Figures 5.10-5.13, reveals several trends. The self conductance, G_{self}, and self susceptance, B_{self}, both show little to no variation with substrate contact spacing for the separations of 50 μm or greater. However, the tendency of G_{self} to decrease slightly for contact separations of 20 μm or less is illustrated, particularly for the smaller area contacts. Both G_{self} and B_{self}, are proportional to contact area. G_{self} increases slightly over the frequency range, while B_{self} shows the behavior of a nearly constant-valued capacitance, increasing linearly with frequency.

The mutual conductances, G_{mut}, and mutual susceptances, B_{mut}, are generally several orders of magnitude lower than G_{self} and B_{self}. Mutual conductance,



(a)



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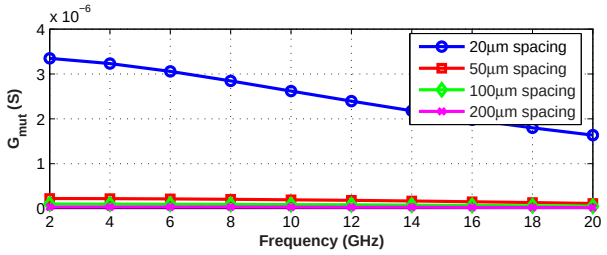

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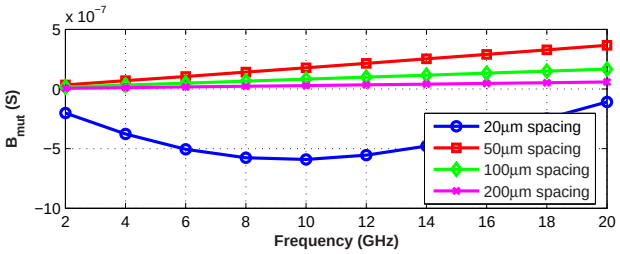
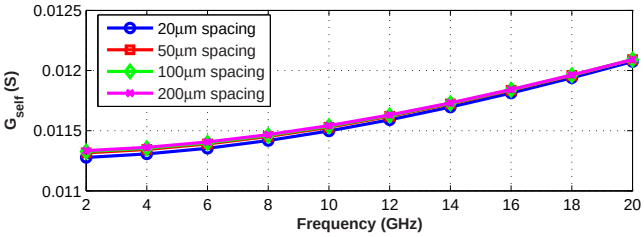
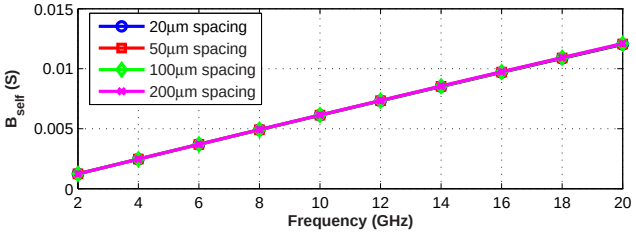


(d)

FIGURE 5.10. Simulated deembedded self and mutual admittances for a pair of 10μm x 10μm substrate contacts. (a) Self conductance, (b) self susceptance, (c) mutual conductance, and (d) mutual susceptance.



(a)



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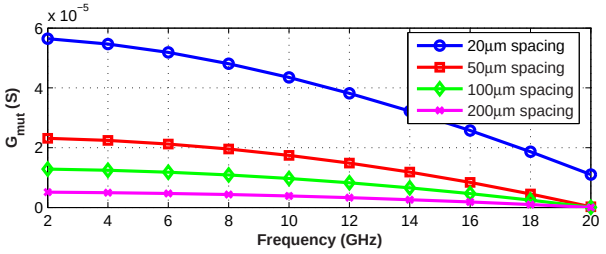

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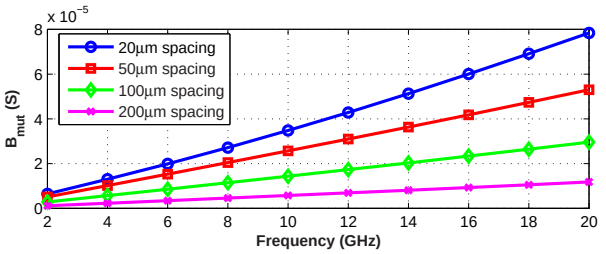
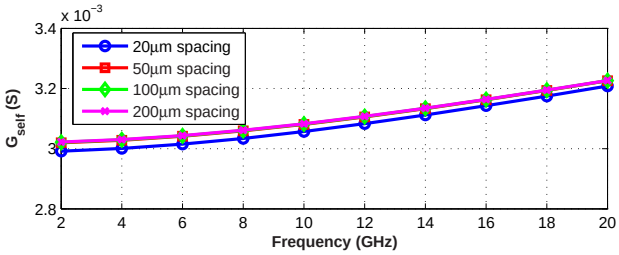
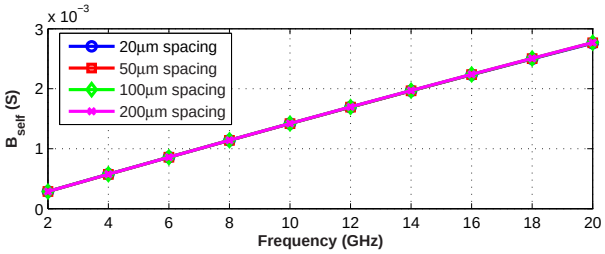


(d)

FIGURE 5.11. Simulated deembedded self and mutual admittances for a pair of 60μm x 60μm substrate contacts. (a) Self conductance, (b) self susceptance, (c) mutual conductance, and (d) mutual susceptance.



(a)



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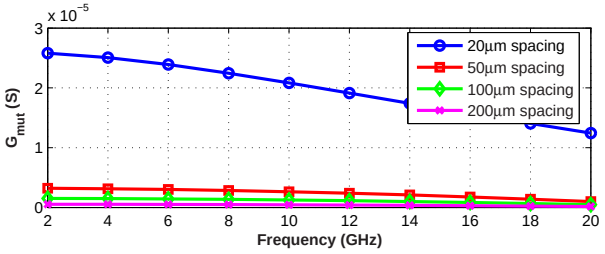

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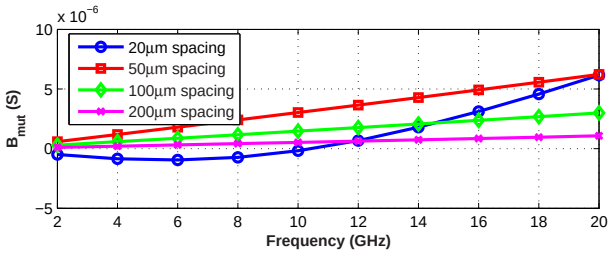
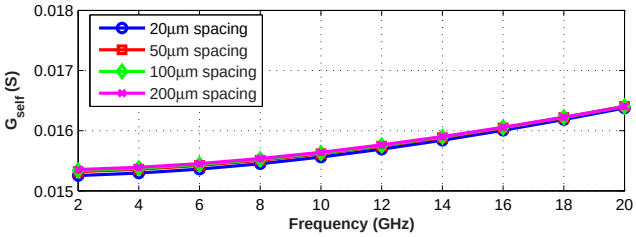
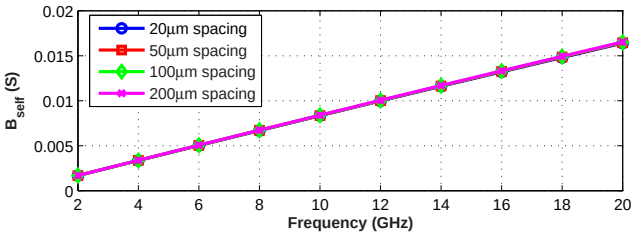


(d)

FIGURE 5.12. Simulated deembedded self and mutual admittances for a pair of 10μm x 60μm substrate contacts. (a) Self conductance, (b) self susceptance, (c) mutual conductance, and (d) mutual susceptance.



(a)



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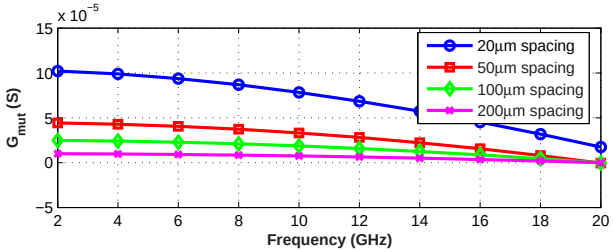

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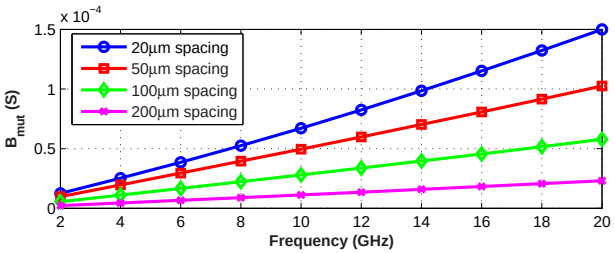


(d)

FIGURE 5.13. Simulated deembedded self and mutual admittances for a pair of 50μm x 100μm substrate contacts. (a) Self conductance, (b) self susceptance, (c) mutual conductance, and (d) mutual susceptance.

G_{mut}, drops off rapidly for the contact separations larger than 20 μm, and tends to decrease with increasing frequency.

For most of the substrate test structures, B_{mut} exhibits a nearly linear relationship with frequency, and is inversely proportional to contact spacing. Figures 5.10(d) and 5.12(d), however, show that, at smallest contact separation of 20 μm, B_{mut} can exhibit the behavior of a parallel RLC network, and can, in fact, appear inductive at some frequencies. This behavior is the basis for the high-frequency substrate network model of Figure 1.2. Closer inspection of Figures 5.11(d) and 5.13(d), reveals that while the mutual susceptance remains capacitive over the frequency range, B_{mut} for the contacts with 20 μm separations does not have a linear relationship with frequency, and and must also be modeled as parallel RLC network.

6. MEASUREMENTS

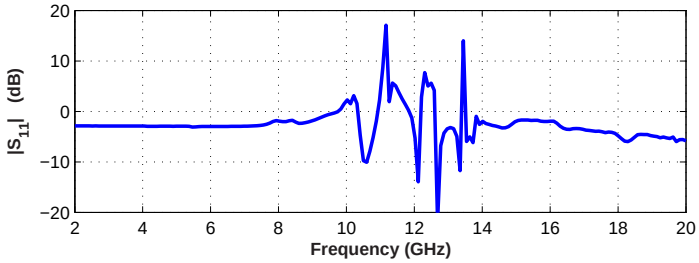
6.1. Test Setup

S-parameter measurements of the substrate and deembedding test structures were taken using an Agilent 8720ES vector network analyzer [20]. The test fixtures were placed on the probe station chuck, and were probed with 150 μm-pitch G-S-G RF wafer probes from Cascade Microtech [21]. Prior to taking any measurements, the network analyzer was calibrated using a short-open-load-through (SOLT) calibration procedure. An impedance standard substrate (ISS) from Cascade Microtech provided the short, through, and 50 Ω load structures necessary for calibration. This calibration placed the measurement reference plane for the network analyzer at the G-S-G probe tips.

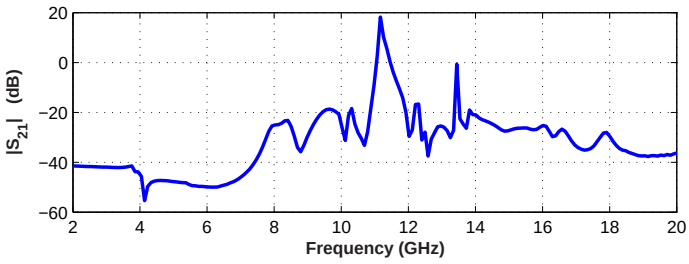
6.2. Initial Measurements

Initial measurements taken on the test fixtures revealed that the test fixtures did not perform as desired, or as predicted by simulations. This is made clear by the plots of Figure 6.1, which show the deembedded S-parameters for a pair of 10 μm x 10 μm contacts. Deembedded S-parameters greater than 0 dB provide the first indication that the measurement and deembedding procedure has failed. The large resonances present in the deembedded data indicated resonances and coupling mechanisms in the test structures that were not accounted for in the test fixture model or in the simulations.

It was determined that the failure of the deembedding process is due to an inability to accurately deembed the two-port parameters for the bondwires, which was caused by a significant amount of coupling between adjacent transmission lines

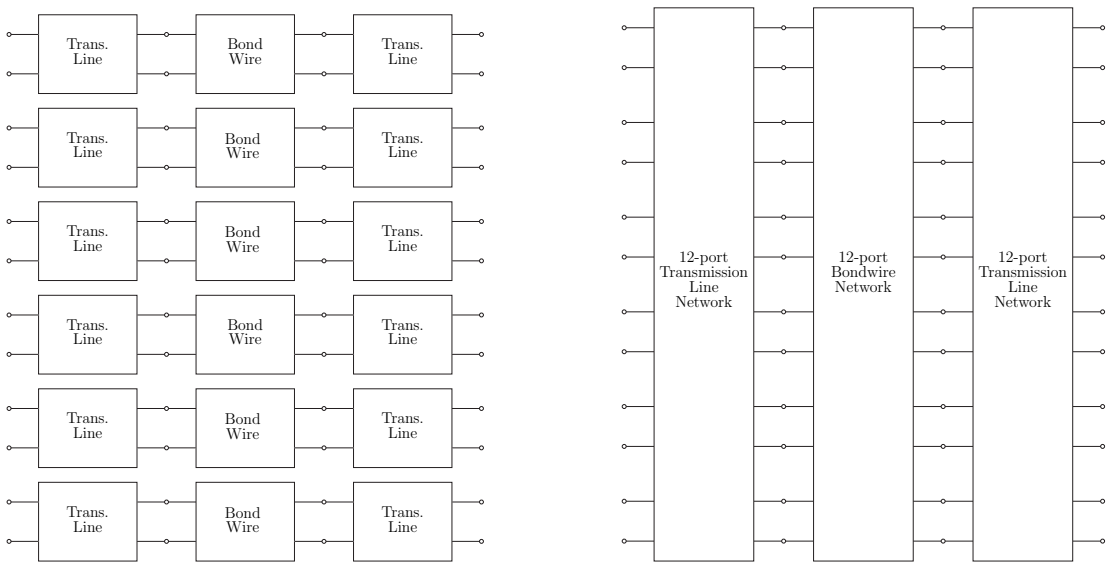


(a)



(b)

FIGURE 6.1. S-parameters from the initial measurements, showing the failure of the measurement and deembedding procedure. (a) S_{11}, (b) S_{21}.



(a) (b)

FIGURE 6.2. (a) The deembedding procedure assumes that the transmission lines and bondwires can be modeled as isolated two-port networks. (b) A more realistic model accounts for coupling, and treats the traces and bondwires as 12-port networks.

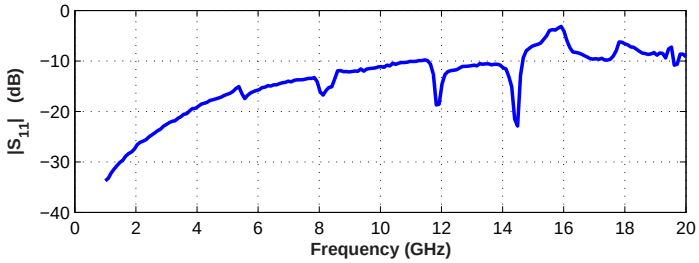
and bondwires. The fact that coupling occurs between traces and bondwires was not unexpected, as was explained in Section 3.3.2. It was, however, unexpected that the geometric consistency between the deembedding and test structures did not result in this coupling being effectively cancelled out in the deembedding process.

The measurement and deembedding procedures' lack of immunity to the trace-to-trace and bondwire-to-bondwire coupling can be explained by first recognizing that the first through third deembedding steps assume the series connection of isolated two port networks. Following this assumption, the bondwire characterization structure, for example, can be modeled as shown in Figure 6.2(a). This model, however, treats each trace and each bondwire as an isolated two-port net-

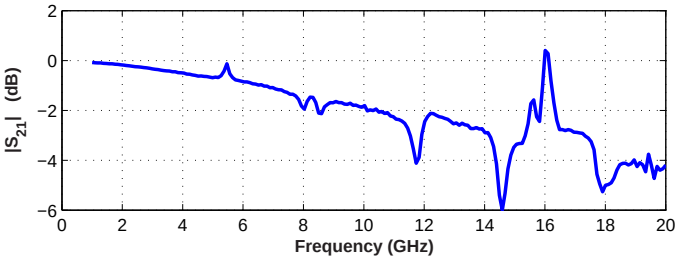
work, ignoring the coupling that occurs from one trace to another and from one bondwire to another. Figure 6.2(b) shows a more realistic model for the bondwire characterization structure, which accounts for this coupling, and models the transmission lines and bondwires as 12-port networks.

In an effort to provide the necessary isolation between test structures, bondwires adjacent to the on-chip through trace, as well as those in the corresponding positions in the bondwire characterization structure, were removed from one of the test fixtures one at a time. After removing each successive bondwire, measurements were taken of the on-chip through trace, and the outer-most bondwire in the bondwire characterization structure, whose adjacent bondwires were also being incrementally removed. The network parameters for the on-chip through trace were then deembedded. Even the removal of all five adjacent bondwires on each side of the chip, and all five adjacent bondwires in the bondwire characterization structures, did not provide sufficient isolation between adjacent structures. The deembedded S-parameters of the through trace with all other bondwires removed are shown in Figure 6.3. These S-parameters are clearly not characteristic of a through trace, containing many resonances and even exceeding 0 dB.

It was therefore determined that attaining sufficient isolation would require removing not only bondwires, but adjacent transmission line traces as well. Because the removal of traces on the ceramic substrate is not as easily accomplished as removing bondwires, experiments to determine which traces must be removed in order to provide the necessary isolation, are best conducted through simulation. Performing such simulations first required that the cause of the failure of the simulations presented in Chapter 5 be identified and corrected.



(a)



(b)

FIGURE 6.3. S-parameters for the on-chip through trace deembedded from measurements taken after removing all other bondwires. (a) S_{11}, (b) S_{21}.

6.3. Revised Simulations

6.3.1. Correlation with Measurements

The simulations used for the design of the test fixture and deembedding procedure, as described in Chapter 5, greatly simplified each simulation structure in order to limit the amount of required memory. With the memory available it was only possible to simulate isolated slices of the test fixture. Structures adjacent to the one being simulated were left out of the HFSS structure, under the assumption that, while coupling would certainly occur, it would be accounted for in the deembedding process. It was this simplification that concealed the shortcomings of the test fixture design.

Since the design and fabrication of the test fixtures, the memory available for simulation has been doubled from 4 GB to 8 GB, which allows for much more accurate simulations of the structures on the test fixture. It is now possible to simulate the transmission line and bondwire characterization structures in their entirety. The structure comprising the cavity-mounted test chip, along with the transmission lines and bondwires that connect to it, can be simulated in its entirety as well, however it is still necessary to substitute a lossless dielectric for the silicon substrate. Figure 6.4 shows a revised HFSS structure used for simulation of the bondwire characterization structure. Similar structures were used for the simulation of the transmission line characterization structures as well as the on-chip test structures.

The goal of these revised simulations was to achieve some degree of correlation between simulations and measurements. Once the simulations are made to accurately predict reality, they can be used to determine how best to mod-

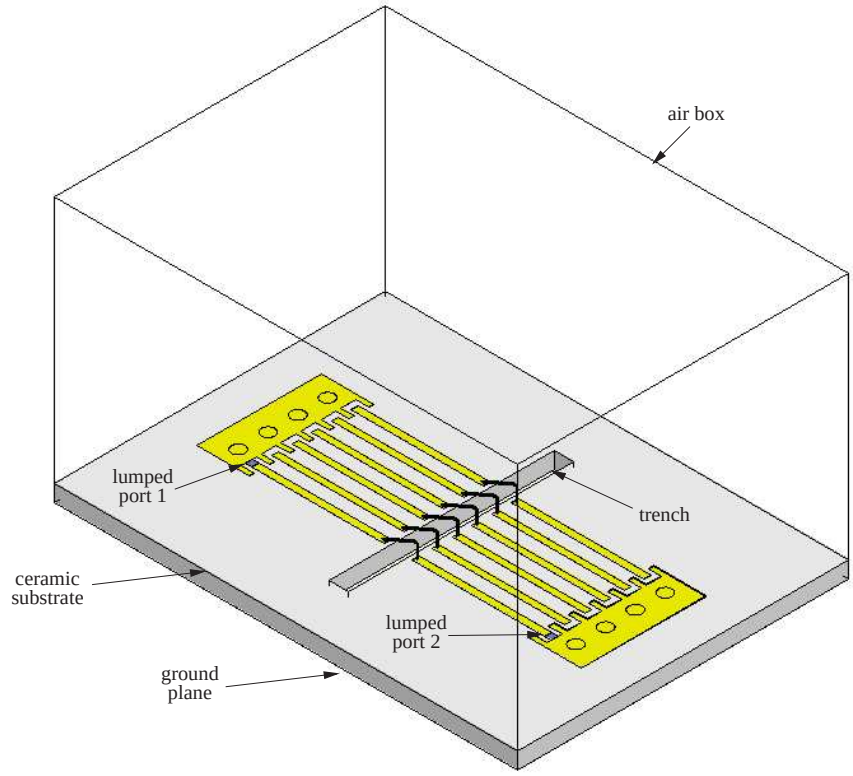
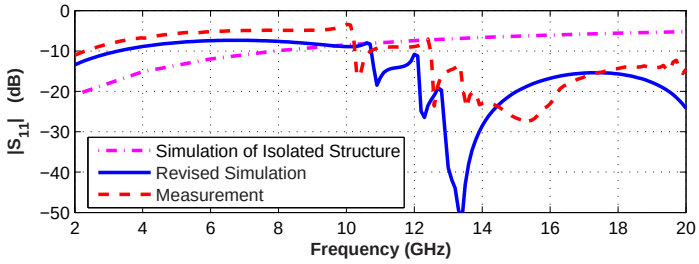


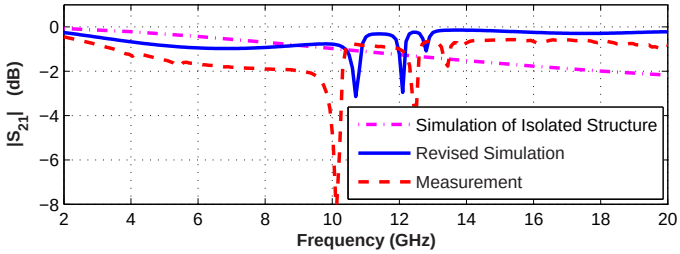
FIGURE 6.4. Revised HFSS structure for the simulation of the bondwire characterization structure.

ify or redesign the test fixtures, so that accurate substrate measurements can be obtained.

Because all test structures are measured through transmission lines and bondwires, the ability to accurately characterize both the transmission lines and bondwires is essential to deembedding the network parameters of any on-chip structures. The transmission line and bondwire characterization structures were therefore the initial focus of the revised simulations. Figure 6.5 plots measured and simulated S-parameters for the outermost transmission lines and bondwire in the characterization structure modeled by Figure 6.4. These plots illustrate both the inadequacy of the original simulations, which modeled only isolated slices of



(a)



(b)

FIGURE 6.5. S-parameters from the initial simulations, revised simulations, and measurements for the outer-most bondwire of the bondwire characterization structure. (a) S_{11}, (b) S_{21}.

the test structures, as well as the reasonably good correlation achieved between the measurements and the revised simulations.

Stimuli are applied to the simulation structure in HFSS through lumped terminal ports, which establish boundary conditions for the simulation. The boundary conditions defined by these ports differ from the real boundary conditions applied by the coplanar waveguide G-S-G micro-probes. It is this discrepancy in boundary conditions which is the most likely cause for the remaining disagreement between the revised simulations and measurements. Increased simulation accuracy could be attained by including a model for the micro-probes in the HFSS simulation structure. This would, of course, come at the cost of much greater memory requirements.

6.3.2. Simulations of Test Fixture Modifications

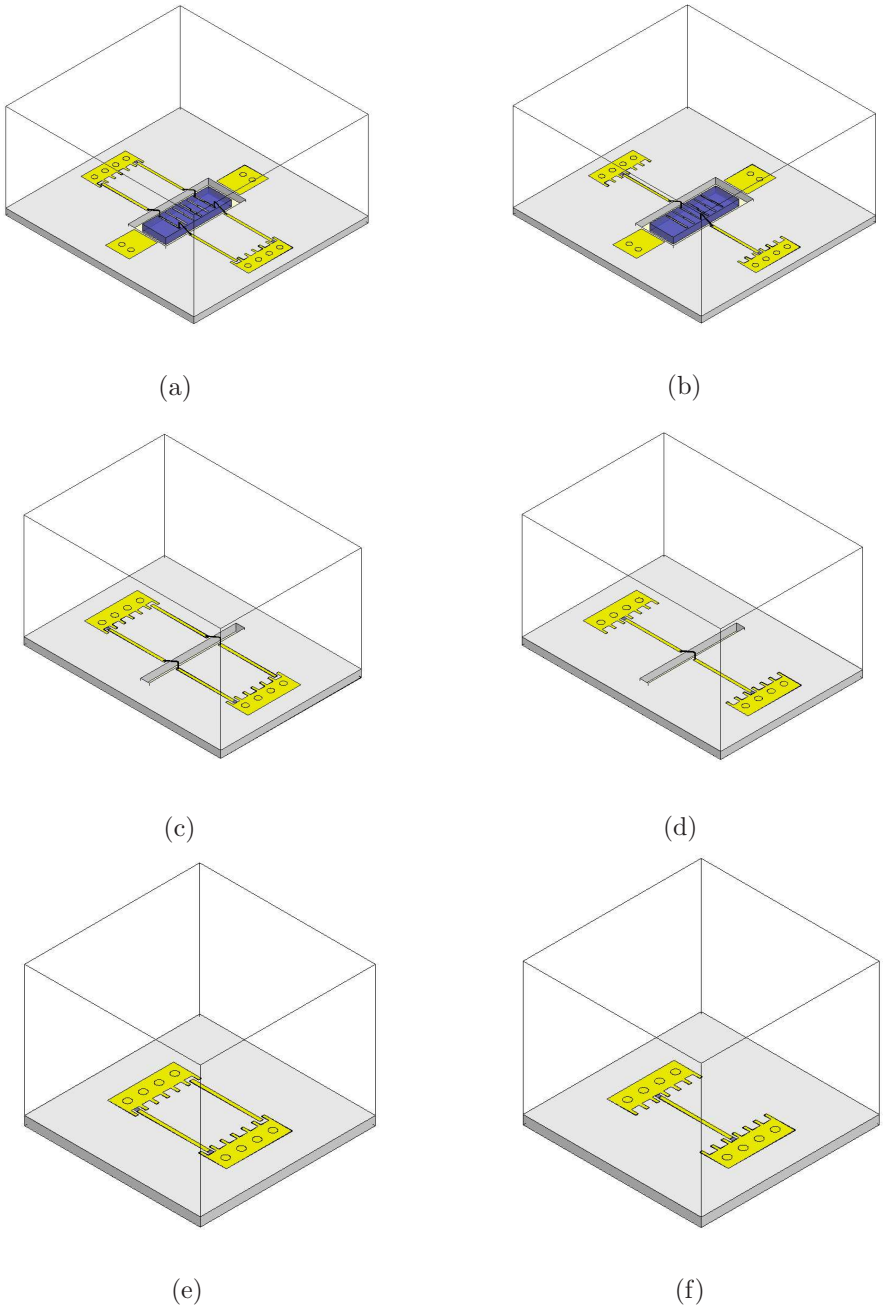
In order to make the test fixture more closely resemble the model of Figure 6.2(a), the coupling between adjacent traces and bondwires must be reduced. This reduction in coupling can be achieved by removing bondwires and transmission lines adjacent to the structure being measured. These modifications were easily accomplished and evaluated through HFSS simulations. Traces and bondwires were removed from the simulation model incrementally, until sufficient isolation was achieved, at which point the structures could accurately be modeled as isolated, series-connected, two-port networks, as in Figure 6.2(a).

Simulations showed that in order to achieve such isolation, it would be necessary to remove either all but the outer two transmission lines and bondwires of each structure, or all but any one set of transmission lines and bondwires. This means that on any single test chip, at most two structures can be measured. Due

to their location on the ends of the test chip those two structures are the through structure and the 10 μm x 10 μm substrate structure. Measurement of any other on-chip structure requires the use of an entire chip for that measurement alone. All traces and bondwires, except those connecting to the test structure to be measured, must be removed.

Deembedding a substrate test structure's network parameters requires not only measurement of that test structure, but measurements of both the on-chip through and on-chip empty structures as well. Obtaining measurements of both on-chip deembedding structures, along with a single substrate test structure, would require two test chips mounted in two separate test fixtures. The first test fixture would have all inner transmission line traces and the corresponding bondwires removed from the chip, as well as from the bondwire and transmission line characterization structures. The second test fixture would have all bondwires and traces removed except those connecting to the on-chip empty structure, and those in the corresponding position in the bondwire and transmission line characterization structures.

HFSS simulations of a 1 KΩ resistor embedded in the test fixture were used to verify this revised measurement scheme using modified test fixtures. As with previous simulations, it was necessary to replace the lossy silicon substrate with a uniform block of lossless dielectric, in order to ease memory requirements. The traces on the lossless dielectric have the identical geometries to those on the test chip having 20 μm separation between substrate contacts. This results in a resistor that is 20 μm long. Figure 6.6 shows the HFSS structures used for these simulations. Simulations of seven different structures represent the complete set of seven measurements, taken on two test fixtures, required in order to deembed the network parameters for the 10 μm x 10 μm substrate structure.

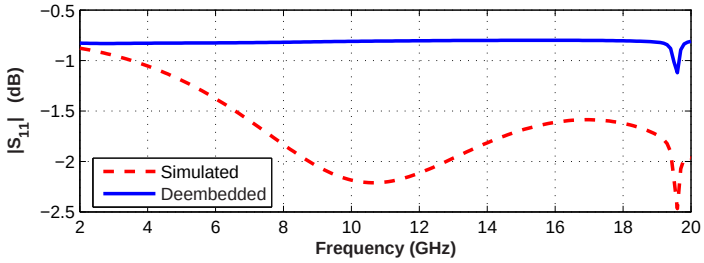


(a) (b)

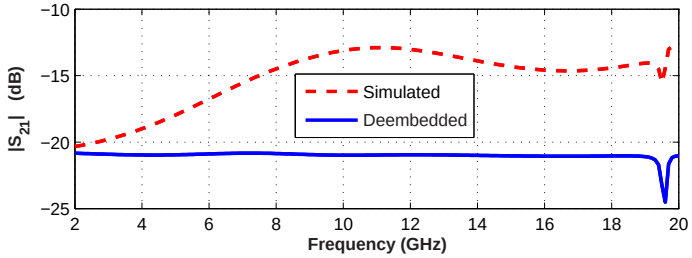
(c) (d)

(e) (f)

FIGURE 6.6. HFSS structures for the simulation and deembedding of a 1 KΩ resistor embedded in the modified test fixture. Structure for the simulation of (a) on-chip through trace and 1 KΩ resistor, (b) on-chip empty structure, (c) outer bondwires, (d) inner bondwire, (e) outer transmission line traces, and (f) inner transmission line trace.



(a)



(b)

FIGURE 6.7. Simulated and deembedded S-parameters for a 1 KΩ resistor embedded in the modified test fixture. (a) S_{11}, (b) S_{21}.

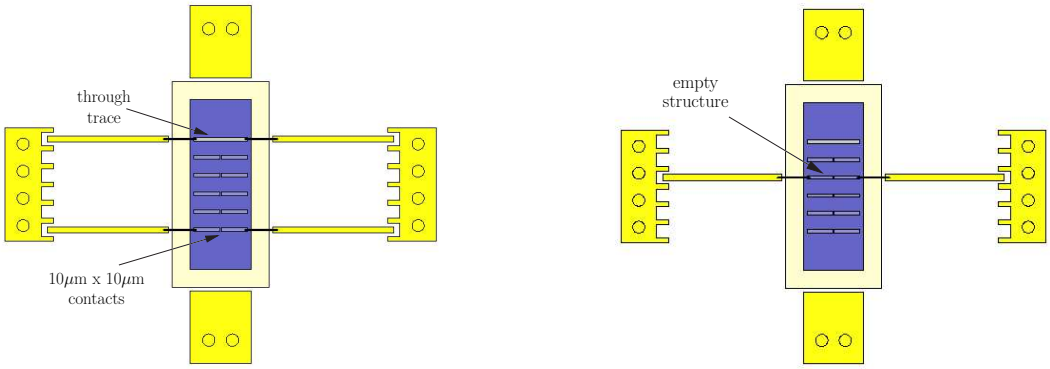
The simulated and deembedded S-parameters for a 1 KΩ resistor embedded in the modified test fixture, obtained from HFSS simulations of the structures in Figure 6.6, are shown in Figure 6.7. The deembedded S-parameters are just what would be expected for an electrically small 1 KΩ resistor, indicating that the modifications to the test fixture should, in fact, yield accurate results. There is a resonance present in the results near 19.5 GHz, which is due to the coupling that remains between the outer two bondwires and transmission lines on the modified structures. These simulations indicate that it will be possible to salvage a small set of useful measurements from the remaining test fixtures, if they can be modified as was done in the HFSS simulations and shown in Figure 6.6.

7. CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

7.1. Conclusion

A test fixture, test chip, and deembedding procedure have been designed to enable network parameter characterization of a silicon substrate up to 20 GHz. The test fixture utilizes off-chip probing, which represents an improvement over previous works, in that it enables the measurement system ground to be directly connected to the back side of the die. This is advantageous because it allows the measured substrate networks to more closely resemble the equivalent circuit models used in simulation, which typically assume the back side of the die as a reference node. Additionally, both simulations and measurements of this test fixture have shown that the off-chip probing scheme serves to eliminate the interactions with the probe station chuck, which have plagued some previous measurement attempts.

Measurements of the test chips mounted in the test fixture revealed shortcomings in the test fixture design. The problems seen in the measurements were replicated in HFSS simulations, and the cause identified as a lack of isolation between adjacent test structures. HFSS simulations were used to test modifications to the test fixtures which would help provide adequate isolation between test structures. Through these simulations, a plan was devised for the modification of the test structures, that would enable them to provide at least a small set of useful measurements.



(a) (b)

FIGURE 7.1. Modified test fixture structures for (a) measurement of the on-chip through structure and a 10 μm x 10 μm substrate structure, and (b) measurement of the on-chip empty structure. The bondwire and transmission line characterization structures on each substrate would have traces and bondwires removed to match the test chip measurement structures shown.

7.2. Suggestions for Future Work

The most immediate future work must be the modification of the remaining test fixtures, as described in Section 6.3.2, to enable the measurement of at least a small sub-set of the substrate test structures. These modifications are summarized in Figure 7.1. A measurement of a single substrate test structure requires two separate test fixtures, and only eight fixtures remain, so at most four different 10 μm x 10 μm substrate structures can be measured. These measurements can provide information that will be useful in the design of improved test fixtures in the future.

Future test fixture designs must take measures to ensure that sufficient isolation is provided between adjacent test structures. This can be achieved by

providing much greater separation between adjacent traces and bondwires on the ceramic substrate. The transmission lines on the ceramic can be made significantly shorter as well, which will also help to reduce coupling.

One possible solution for an improved test fixture would utilize a test chip similar to the one used here, which would then be sliced into very small dice, each containing only a single on-chip test structure. These dice would then be mounted alone in isolated cavities, similar to the one used in this design, but sized for the much smaller die. The single test structure on each chip would connect to a single set of transmission lines on the ceramic substrate, through a single pair of bondwires. Many of these single-structure, cavity-mounted test chips could be mounted on a single ceramic substrate. Each substrate would still have a bondwire and a transmission line characterization structure, which would now have only a single set of transmission lines and bondwires. Care must be taken to adequately separate all test structures on the ceramic substrate to ensure that the required isolation is provided.

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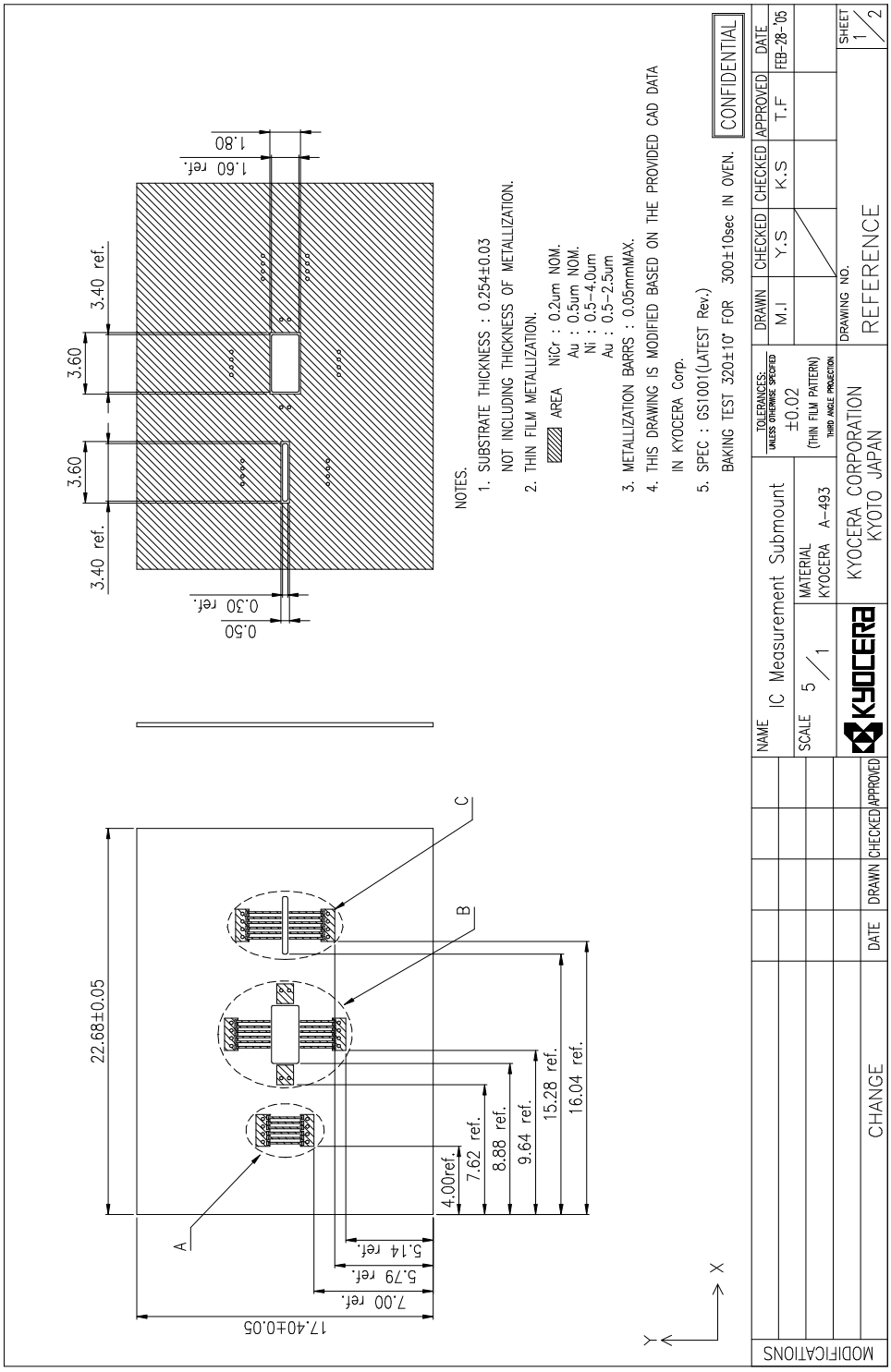
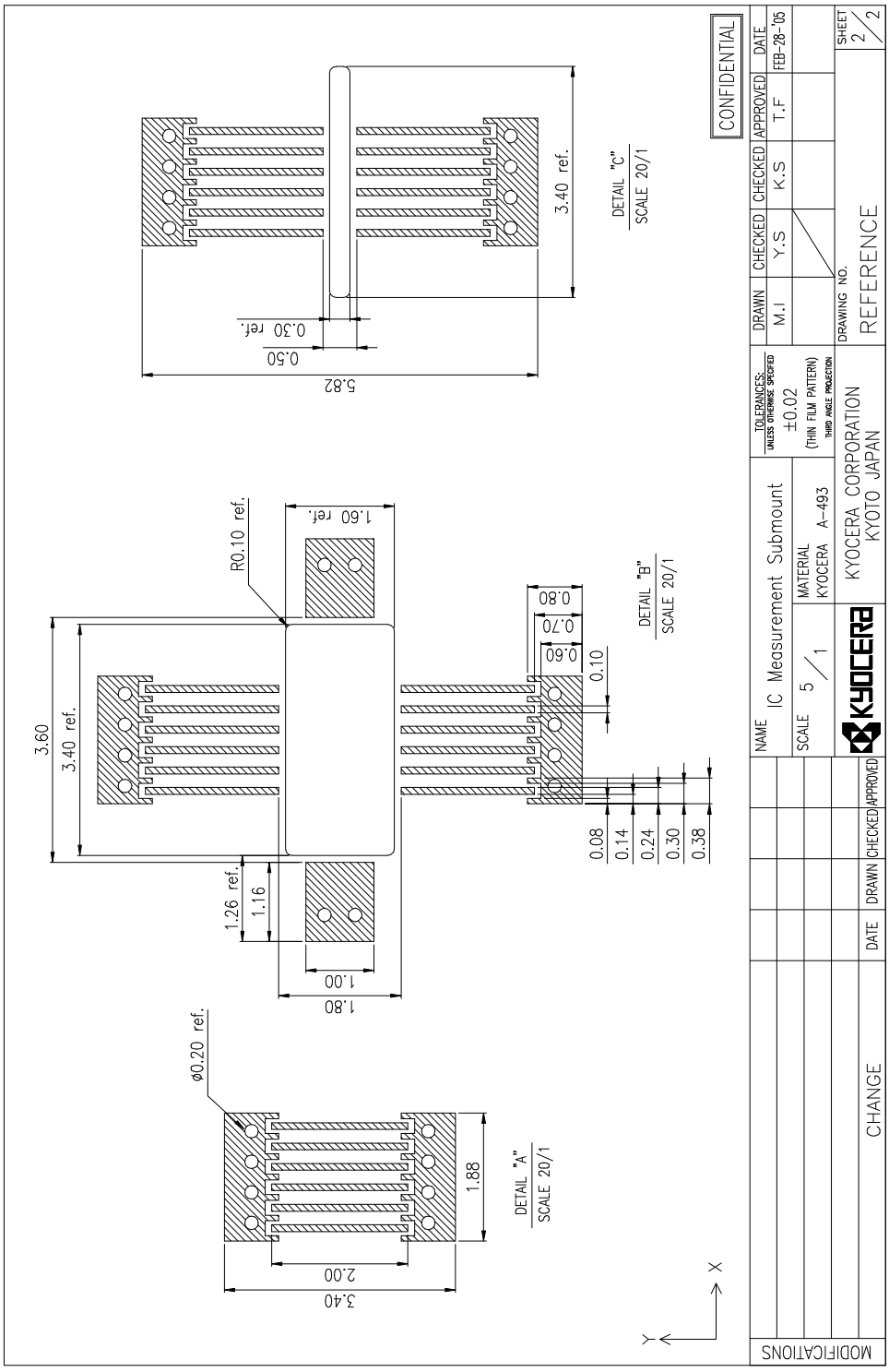
APPENDICES

APPENDIX A. Test Fixture Mechanical Drawings




CONFIDENTIAL
DETAIL "C"
SCALE 20/1
3.40 ref.
0.50
0.30 ref.
5.82
DETAIL "B"
SCALE 20/1
R0.10 ref.
1.60 ref.
0.80
0.70
0.60
0.10
3.60
3.40 ref.
1.26 ref.
1.16
1.00
1.80
0.08
0.14
0.24
0.30
0.38
DETAIL "A"
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ø0.20 ref.
1.88
2.00
3.40
X
Y
NAME IC Measurement Submount
SCALE 5/1
MATERIAL KYOCERA A-493
TOLERANCES: UNLESS OTHERWISE SPECIFIED ±0.02 (THIN FILM PATTERN) THIRD ANGLE PROJECTION
KYOCERA
KYOCERA CORPORATION KYOTO JAPAN
DRAWN M.I
CHECKED Y.S
CHECKED K.S
APPROVED T.F
DATE FEB-28-'05
DRAWING NO. REFERENCE
SHEET 2/2
MODIFICATIONS
CHANGE
DATE
DRAWN
CHECKED
APPROVED

APPENDIX B. Matlab Deembedding Code

B.1. Four Step Deembedding Function

```
function [f,s_deembedded] =fsd(s2p_in,s2p_out,position,sep)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% fsd.m
% Kyle Webb
% 2005
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This function performs deembedding of substrate network measurements
% taken on the substrate measurement test fixture.
%
% The following measurements are required:
%       1. mstrip(1-3): 50ohm (70ohm) microstrip trans line
%       2. bw(1-3): bondwires measured over trench
%       3. through: on-chip through trace
%       4. empty: on-chip empty structure
%       5. full: pair of substrate contacts of interest
%
% Deembedding of the full structure is performed in the following 4 steps:
%       1. remove microstrip traces
%       2. remove the bondwires
%       3. revove the on-chip trace sections
%       4. subtract out the admittances that shunt the substrate contact
%
% Inputs to the function are the name of the .s2p file containing the
% measured data to be deembedded, the name of the .s2p file to which the
% deembedded data will be written, the position (1-3) of the test structure
% (1: edge, 2: one in from edge, 3: two in from edge), and the separation
% between substrate contacts. The separation input is used to control the
% factorization of the on-chip through trace into the appropriate length
% segments of trace. (i.e. separation determines n and k)


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% First, extract parasitics from measurements of the deembedding
% structures.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Load the data for the deembed structures
mstrip1 = load('test_chip_meas/mstrip1_meas.s2p');
f_mstrip1 = mstrip1(:,1);
f = f_mstrip1;
s11_mstrip1 = mstrip1(:,2) + j*mstrip1(:,3);
s21_mstrip1 = mstrip1(:,4) + j*mstrip1(:,5);
s12_mstrip1 = mstrip1(:,6) + j*mstrip1(:,7);
s22_mstrip1 = mstrip1(:,8) + j*mstrip1(:,9);
s_mstrip1 = [s11_mstrip1, s21_mstrip1, s12_mstrip1, s22_mstrip1];

mstrip2 = load('test_chip_meas/mstrip2_meas.s2p');
f_mstrip2 = mstrip2(:,1);
f = f_mstrip2;
s11_mstrip2 = mstrip2(:,2) + j*mstrip2(:,3);
s21_mstrip2 = mstrip2(:,4) + j*mstrip2(:,5);
```

```
s12_mstrip2 = mstrip2(:,6) + j*mstrip2(:,7);
s22_mstrip2 = mstrip2(:,8) + j*mstrip2(:,9);
s_mstrip2 = [s11_mstrip2, s21_mstrip2, s12_mstrip2, s22_mstrip2];

mstrip3 = load('test_chip_meas/mstrip3_meas.s2p');
f_mstrip3 = mstrip3(:,1);
f = f_mstrip3;
s11_mstrip3 = mstrip3(:,2) + j*mstrip3(:,3);
s21_mstrip3 = mstrip3(:,4) + j*mstrip3(:,5);
s12_mstrip3 = mstrip3(:,6) + j*mstrip3(:,7);
s22_mstrip3 = mstrip3(:,8) + j*mstrip3(:,9);
s_mstrip3 = [s11_mstrip3, s21_mstrip3, s12_mstrip3, s22_mstrip3];

bw1 = load('test_chip_meas/bondwire1_meas.s2p');
f_bw1 = bw1(:,1);
s11_bw1 = bw1(:,2) + j*bw1(:,3);
s21_bw1 = bw1(:,4) + j*bw1(:,5);
s12_bw1 = bw1(:,6) + j*bw1(:,7);
s22_bw1 = bw1(:,8) + j*bw1(:,9);
s_bw1 = [s11_bw1, s21_bw1, s12_bw1, s22_bw1];

bw2 = load('test_chip_meas/bondwire2_meas.s2p');
f_bw2 = bw2(:,1);
s11_bw2 = bw2(:,2) + j*bw2(:,3);
s21_bw2 = bw2(:,4) + j*bw2(:,5);
s12_bw2 = bw2(:,6) + j*bw2(:,7);
s22_bw2 = bw2(:,8) + j*bw2(:,9);
s_bw2 = [s11_bw2, s21_bw2, s12_bw2, s22_bw2];

bw3 = load('test_chip_meas/bondwire3_meas.s2p');
f_bw3 = bw3(:,1);
s11_bw3 = bw3(:,2) + j*bw3(:,3);
s21_bw3 = bw3(:,4) + j*bw3(:,5);
s12_bw3 = bw3(:,6) + j*bw3(:,7);
s22_bw3 = bw3(:,8) + j*bw3(:,9);
s_bw3 = [s11_bw3, s21_bw3, s12_bw3, s22_bw3];

% select the proper mstrip and bondwire to use for the given test struct.
if (position == 1)
    s_mstrip = s_mstrip1;
    s_bw = s_bw1;
elseif (position == 2)
    s_mstrip = s_mstrip2;
    s_bw = s_bw2;
elseif (position == 3)
    s_mstrip = s_mstrip3;
    s_bw = s_bw3;
end

through = load('test_chip_meas/through_meas.s2p');
f_through = through(:,1);
s11_through = through(:,2) + j*through(:,3);
s21_through = through(:,4) + j*through(:,5);
s12_through = through(:,6) + j*through(:,7);
s22_through = through(:,8) + j*through(:,9);
s_through = [s11_through, s21_through, s12_through, s22_through];
y_through = s2y(s_through);

empty = load('test_chip_meas/empty_meas.s2p');
f_empty = empty(:,1);
```

```
s11_empty = empty(:,2) + j*empty(:,3);
s21_empty = empty(:,4) + j*empty(:,5);
s12_empty = empty(:,6) + j*empty(:,7);
s22_empty = empty(:,8) + j*empty(:,9);
s_empty = [s11_empty, s21_empty, s12_empty, s22_empty];

full = load(s2p_in);
f_full = full(:,1);
s11_full = full(:,2) + j*full(:,3);
s21_full = full(:,4) + j*full(:,5);
s12_full = full(:,6) + j*full(:,7);
s22_full = full(:,8) + j*full(:,9);
s_full = [s11_full, s21_full, s12_full, s22_full];


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% eliminate 50ohm traces from the measurements

s_bw1_1 = chain_strip(s_bw1,s_mstrip1);
s_bw2_1 = chain_strip(s_bw2,s_mstrip2);
s_bw3_1 = chain_strip(s_bw3,s_mstrip3);
s_bw_1  = chain_strip(s_bw,s_mstrip);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% use the through structure data to calculate the chain parameters for the
% on-chip sections of trace

% first, remove the effects of the 50ohm microstrip traces (mstrip1)
s_through_1 = chain_strip(s_through,s_mstrip1);

% next, remove the bondwires (bw1)
s_through_2 = chain_strip(s_through_1,s_bw1_1);

% factor the remaining section of through trace
abcd_through_2 = s2abcd(s_through_2);
if (sep == 20)
    abcd_sect = abcd_factor(abcd_through_2, 9, 250);  % l=395um, g=20um
elseif (sep == 50)
    abcd_sect = abcd_factor(abcd_through_2, 9, 240);  % l=380um, g=50um
elseif (sep == 100)
    abcd_sect = abcd_factor(abcd_through_2, 9, 224);  % l=355um, g=100um
else (sep == 200)
    abcd_sect = abcd_factor(abcd_through_2, 9, 193);  % l=305um, g=200um
end
s_sect = abcd2s(abcd_sect);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% deembed the measurement data for the empty structure to determine y_e

% first, remove the effects of the 50ohm trace (mstrip3)
s_empty_1 = chain_strip(s_empty,s_mstrip3);

% next, remove the bondwires
s_empty_2 = chain_strip(s_empty_1,s_bw3_1);


% then, remove the trace segments
s_empty_3 = chain_strip(s_empty_2,s_sect);
y_empty_3 = s2y(s_empty_3);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The final step is to deembed the substrate network parameters from the
% measurement of the full structure

% first, remove the effects of the 50ohm trace
s_full_1 = chain_strip(s_full,s_mstrip);

% next, remove the bondwires
s_full_2 = chain_strip(s_full_1,s_bw);

% remove the trace segments
s_full_3 = chain_strip(s_full_2,s_sect);

% finally, remove the empty structure admittances
y_full_3 = s2y(s_full_3);
y_full_4 = y_full_3 - y_empty_3;

% the network parameters for the substrate only
y_sub = y_full_4;
y11_sub = y_sub(:,1);
y21_sub = y_sub(:,2);
y12_sub = y_sub(:,3);
y22_sub = y_sub(:,4);

z_sub = y2z(y_sub);
z11_sub = z_sub(:,1);
z21_sub = z_sub(:,2);
z12_sub = z_sub(:,3);
z22_sub = z_sub(:,4);

s_sub = y2s(y_sub);
s11_sub = s_sub(:,1);
s21_sub = s_sub(:,2);
s12_sub = s_sub(:,3);
s22_sub = s_sub(:,4);

s_deembedded = s_sub;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% write s-parameters to file s2p_out

fid = fopen(s2p_out,'w');
% fprintf(fid,'# hz S ri R 50\n');

for i=1:length(f)
    fprintf(fid,...
     '%1.8e\t%1.8e\t%1.8e\t%1.8e\t%1.8e\t%1.8e\t%1.8e\t%1.8e\t%1.8e\n',...
        f(i),...
        real(s_sub(i,1)), imag(s_sub(i,1)),...
        real(s_sub(i,2)), imag(s_sub(i,2)),...
        real(s_sub(i,3)), imag(s_sub(i,3)),...
        real(s_sub(i,4)), imag(s_sub(i,4)));
end

fclose(fid);
```

B.2. Function to Remove Series Two-Port Blocks

```
function s_inner = chain_strip(s_casc,s_outer)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% chain_strip.m
% Kyle Webb
% 2005
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This function accepts two s-parameter matrices, s_casc and s_outer, and
% returns s_inner, where:
%   s_inner = inv(s_outer) * s_casc * inv(s_outer)

abcd_casc = s2abcd(s_casc);
abcd_outer = s2abcd(s_outer);

for i=1:length(s_casc(:,1))
   abcd_outer_fi = [abcd_outer(i,1),abcd_outer(i,2);...
                    abcd_outer(i,3),abcd_outer(i,4)];
    abcd_casc_fi = [abcd_casc(i,1),abcd_casc(i,2);...
                    abcd_casc(i,3),abcd_casc(i,4)];

    abcd_inner_fi = inv(abcd_outer_fi)*abcd_casc_fi*inv(abcd_outer_fi);

    abcd_inner(i,:) = [abcd_inner_fi(1,:),abcd_inner_fi(2,:)];
end

s_inner = abcd2s(abcd_inner);
```

B.3. Chain Parameter Factorization Function

```
function abcd_sect = abcd_factor(abcd_thru, n, k)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
% abcd_factor.m
% Kyle Webb
% 2005
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% This function calculates the abcd parameters for a section of trace (e.g.
% one half of the empty structure), given the abcd parameters for a longer
% section of trace (e.g. the thru structure).
%
% The longer section of trace is divided into 2^n shorter sections, each
% with abcd parameters, abcd_2n. The desired abcd parameters for the
% shorter section of trace are then given by abcd_sect = (abcd_2n)^k


a = abcd_thru(:,1);
b = abcd_thru(:,2);
c = abcd_thru(:,3);
d = abcd_thru(:,4);

for i=1:n
    a_2i = sqrt((a + 1)/2);
    d_2i = sqrt((d + 1)/2);
    b_2i = (b)./(2*a_2i);
    c_2i = (c)./(2*d_2i);

    a = a_2i;
    b = b_2i;
    c = c_2i;
    d = d_2i;
end

abcd_2n = [a,b,c,d];

for i=1:length(a)
    abcd_fi = [abcd_2n(i,1),abcd_2n(i,2);abcd_2n(i,3),abcd_2n(i,4)];
    abcd_sect_fi = abcd_fi^k;

    abcd_sect(i,:) = [abcd_sect_fi(1,:), abcd_sect_fi(2,:)];
end
```

APPENDIX C. Test Fixture Photomicrographs

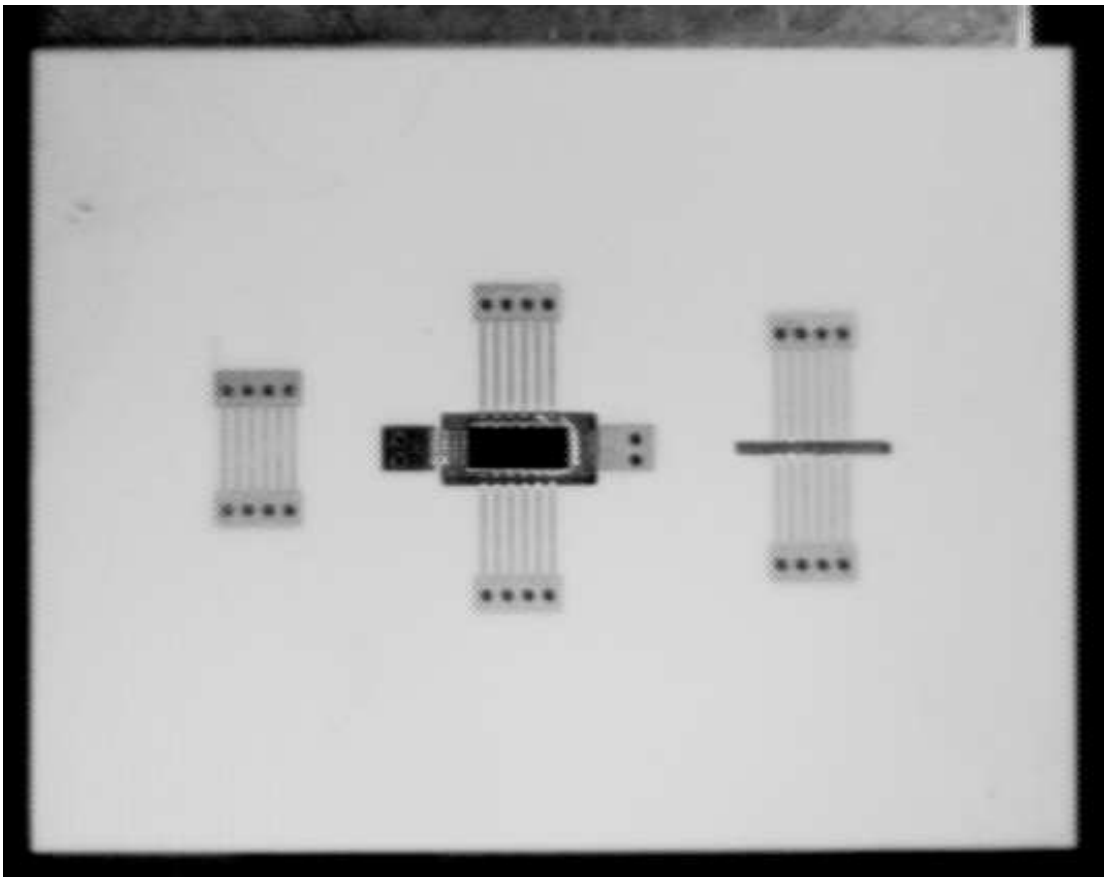

FIGURE C-1. Photomicrograph of the complete test fixture.

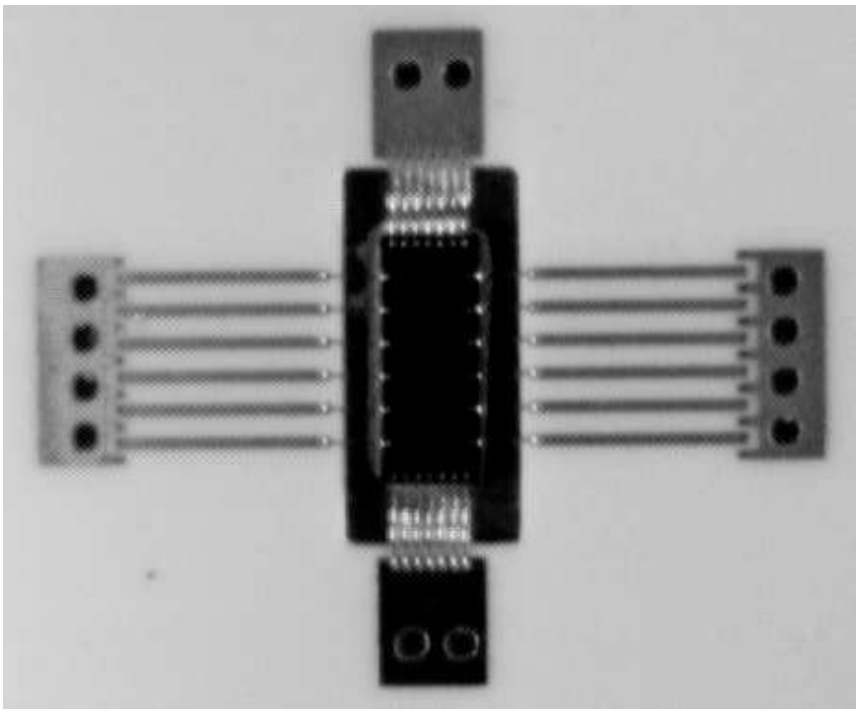

FIGURE C-2. Photomicrograph of the test chip mounted in the test fixture.

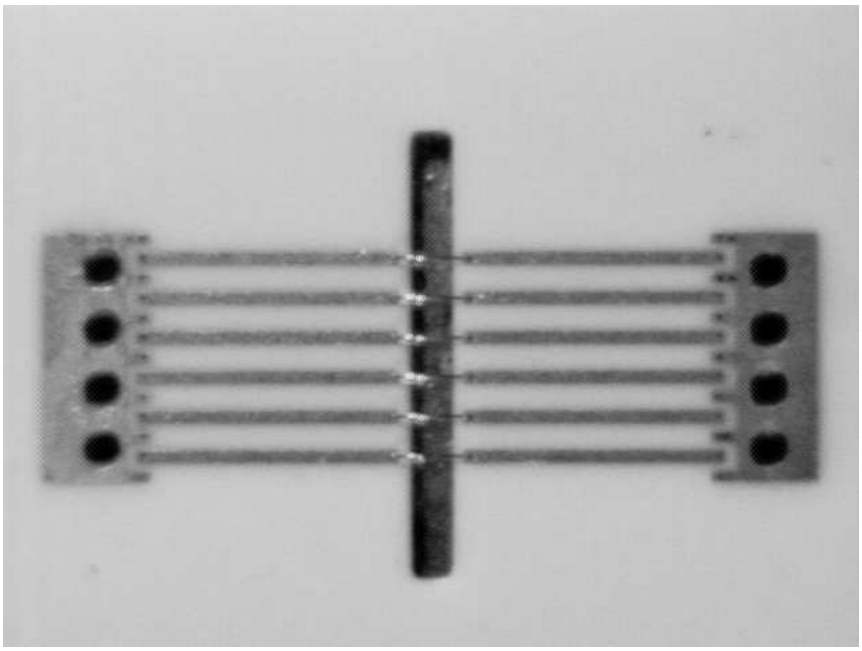

FIGURE C-3. Photomicrograph of the bondwire characterization structure.

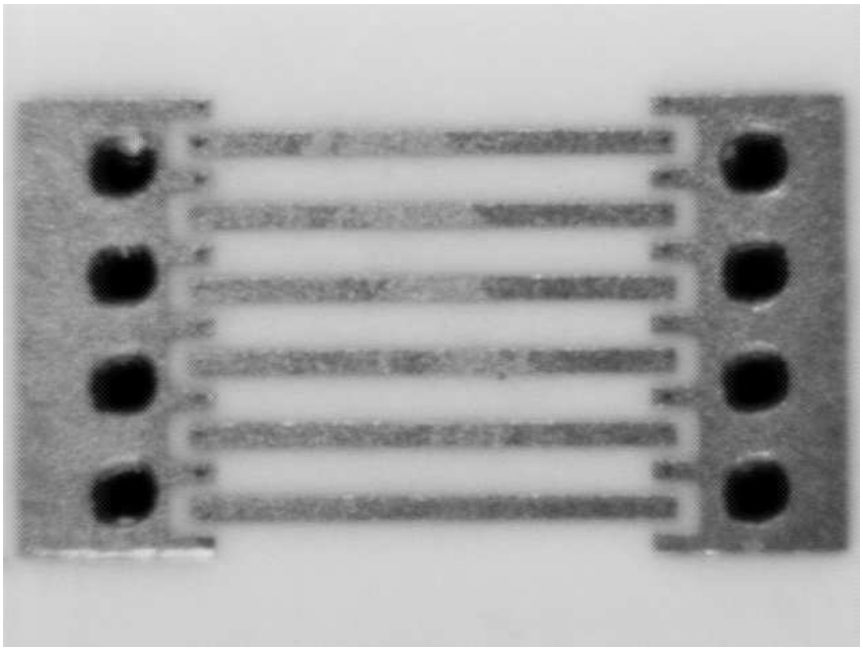

FIGURE C-4. Photomicrograph of the transmission line characterization structure.