AN ABSTRACT OF THE THESIS OF

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John F. Wager

The achievements of this thesis are the development of several models for the SPICE (Simulation Program with Integrated Circuit Emphasis) simulation of alternating-current thin-film electroluminescent (ACTFEL) devices, organic light-emitting devices (OLEDs), and polymer light-emitting devices (PLEDs). First, an ACTFEL model based on the built-in HSPICE Fowler-Nordheim tunneling diode is developed, which accurately reproduces the electrical characteristics of an evaporated ZnS:Mn device with only two adjustable parameters. This model is then expanded to match experimental trends over varying maximum applied voltages. Next, a device physics-based ACTFEL model is developed for SPICE in which interface emission of electrons can occur via both pure tunneling or thermal emission and in which occupancy of the interfacial trap is considered. This model is then expanded through the inclusion of first one and then two sheets of charge at specified locations within the phosphor layer. These sheets of charge are used to model space charge creation through either field emission or trap-to-band impact ionization. Device-physics features, such as field- and occupancy-dependent trapping of electrons at each sheet of charge, are included in the SPICE model for the first time. With the inclusion of static space charge, the double-sheet charge model is shown to model evaporated ZnS:Mn ACTFEL devices very well without artificially suppressing the interface trap depth or varying the model parameters for different maximum applied voltages. The

model displays transferred charge capacitance overshoot and other experimentally-observed trends. Next, a simple OLED model is developed which accurately accounts for the dc electrical behavior of these devices, and a method of modeling injection-limited behavior versus bulk-limited behavior is shown. Finally, a single-layer PLED SPICE model is developed, and a method for specifying the parameters is derived. The model accurately accounts for PLED dc I-V electrical behavior.

SPICE Modeling of ACTFEL Devices and OLEDs

by

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Jeffrey P. Bender, Author

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SPICE MODELING OF ACTFEL DEVICES AND OLEDS

1. INTRODUCTION

Luminescence is a phenomenon in which energy of one type is converted into electromagnetic radiation. [1] For instance, chemiluminescence results from the energy of a chemical reaction, triboluminescence occurs when certain substances (for example sugar) are ground or crushed, and photoluminescence is light emission stimulated by incident radiation ranging from visible light to x-radiation. Electroluminescence (EL) is luminescence caused by an electric potential. As with other classifications of luminescence, EL consists of several different phenomena. American scientist and statesman Benjamin Franklin first identified in 1752 the cause of the luminescence of lightning as an electric discharge through the air, for instance.

Naturally-occurring luminescent materials have been known since ancient times, but the first scientific investigation into the luminescence of prepared materials occurred in 1603 when Italian alchemist Vincenzo Cascariolo found that a heated mixture of barium sulfate and coal produced blue light at night, and could be "recharged" through exposure to sunlight. Although never very useful as a means of producing gold from base materials, as hoped by some alchemists, barium sulfide eventually become the first commercially-available phosphor material in 1870, along with calcium sulfide, four years after the first stable ZnS phosphor material was created. Cascariolo's original material was known by many names, including "phosphor," which means "light-bearer," and "phosphorescence" was thereafter used to describe the lingering glow associated with luminescent materials.

The photoluminescence of certain materials when exposed to ultraviolet light was first observed by the German physicist Johann Wilhelm Ritter in 1801. "Fluorescence" was coined in 1852 from the mineral name "fluorspar" to describe the behavior

of materials which absorb light of one wavelength and immediately re-emit light of another wavelength, the emission ceasing immediately upon removal of the excitation light source. Finally, in 1888, physicist and historian Eilhardt Wiedemann used the term "Luminescenz" to describe the "development of light in which an illumination is produced through external causes without an appropriate increase in the temperature," remarking that "we would then designate the illumination excited by incident light as Photoluminescenz." [2]

The German physicist Philipp Anton Lenard was in 1890 the first to describe the phosphor materials as activator ions which are distributed throughout a host crystal, following the work of Becquerel in France who experimented with alkali metal coactivation of phosphors.

In 1907, electroluminescence was observed in silicon carbide by Captain H. J. Round in England, and in 1936 Professor Georges Destriau at the University of Paris found that when zinc sulfide was suspended in oil on glass sheets and an ac voltage applied, the phosphor material glowed. The study of high-field EL was initiated, leading to the first commercial electroluminescent lamp being produced by GTE Sylvania in 1948 in Massachusetts. In the 1960s, with the advent of thin-film deposition technologies, research on powder-phosphor EL gave way to increased research on thin-film EL display devices, with the first ZnS:Mn alternating current thin-film electroluminescent (ACTFEL) display matrix produced in 1962 by Edwin Soxman of Servomechanisms in the United States. Research during the early 1970s in Japan led to the introduction of the first commercial ACTFEL display in 1983 by the Sharp Corp. The market has continued to grow worldwide during the last two decades.

The most important display at present is undoubtedly the cathode ray tube (CRT), which forms the basis for most televisions and computer monitors. The CRT employs cathodoluminescence, a type of EL which results from the impact of a beam of electrons. German physicist Karl Ferdinand Braun in 1897 produced an oscilloscope with a CRT as the display, the first practical use of the phenomenon, and Russian-

American electrical engineer Vladimir Kosma Zworykin demonstrated a television receiver in 1929 with more modern features than that shown by J. L. Baird in 1926 in England. CRT displays are ubiquitous today, with full color due to the availability of phosphors which emit in each of the three primary colors (silver-doped zinc sulfide for blue, manganese-doped zinc silicate for green, and europium-doped yttrium vanadate for red). In addition to this advantage, CRTs offer a high viewing angle, long life, high speed, relatively low cost, and can be used to make large area displays. However, several drawbacks, most notably high power consumption, a lack of ruggedness, and large physical size, have opened the door in recent years to competing technologies.

Almost all of these competitors are very thin flat-panel displays (FPDs). The current champion of these, the liquid crystal display (LCD), is found in many applications where size is important, ranging from computer monitors to "viewfinders" in digital cameras. In addition to their small size, LCDs are attractive as displays in clean rooms, and also exhibit full-color and consume little power. However, they retain the CRT's lack of ruggedness and sport a limited viewing angle, low speed (making them unsuitable for high-quality video display), and a restrictive range of operating temperatures.

A host of lesser-known challengers include the field emission display (FED), plasma display panel (PDP), and thin-film electroluminescent (TFEL) display, each of which has its advantages and disadvantages. It is possible that each of these technologies will ultimately occupy a portion of the display market for which it is best suited.

The focus of this thesis is on TFEL technology, specifically on the computer modeling of the electrical characteristics of alternating-current thin-film electroluminescent (ACTFEL) devices and organic light-emitting devices (OLEDs).

Advantages of ACTFEL technology include a very wide viewing angle, high resolution, moderate power consumption, and a long life. Furthermore, ACTFEL displays are rugged and operate properly over a wide temperature range. These at-

tributes have made ACTFEL displays attractive for military and other applications. The main drawback of ACTFEL technology is the lack of sufficiently efficient phosphor materials which emit in each primary color, precluding the development of a viable full-color display.

OLED's are a relative new-comer to the fray, with the impetus for research generally credited to an OLED proposed by Ching W. Tang and S. A. VanSlyke in 1986. The use of organic materials means a very large number of materials are available as possible phosphor layers, and the emission color is easily shifted through the incorporation of organic dyes into the device. High-brightness, high-efficiency devices with organic phosphor layers have been reported, but the major drawback to these devices is their lifetime.

The rest of this thesis is organized as follows. Chapter 2 provides an overview of ACTFEL device structure, operation, and electrical characterization as well as an introduction to SPICE and review of previously published literature on SPICE modeling of ACTFEL devices. Chapter 3 describes several ACTFEL SPICE models developed in the course of this thesis work, and Chapter 4 then presents the results of simulation using these models. Chapter 5 describes the structure and operation of OLEDs before presenting several SPICE equivalent circuits which model their electrical behavior. Chapter 6 concludes the thesis and gives suggestions for future work. Finally, sample SPICE code for the two main ACTFEL models presented in this thesis is included as appendices for reference.

2. ACTFEL BASICS AND LITERATURE REVIEW

This chapter presents useful background information concerning ACTFEL devices. First, the physical structure and ideal operation of ACTFEL devices are presented. Next, the testing and electrical characterization of devices are discussed. Finally, the SPICE electrical circuit simulation program and previous ACTFEL SPICE modeling efforts are reviewed.

2.1 ACTFEL Device Structure

The structure of the ACTFEL devices primarily used in this work is shown in Fig. 2.1. A layer of the n-type transparent conductor indium tin oxide (ITO) is first deposited on a glass substrate to act as the bottom contact of the ACTFEL device. ITO is chosen not only for its high conductivity, but also because of its transparency to visible light. Next, a layer of silicon oxynitride (SiON) is sputter-deposited to act as the bottom insulator. The phosphor layer of zinc sulfide doped with manganese (ZnS:Mn) is vacuum evaporated onto the bottom insulator, and another layer of SiON is sputtered on top of the phosphor material to form the top insulator. Finally, aluminum metal is patterned onto the top of the device through thermal evaporation to serve as the top contacts. Unlike the ITO bottom contact, the aluminum layer is reflective instead of transparent. Thus, light generated within the phosphor region is reflected by the aluminum contacts, and exits the device through the ITO and is viewable through the glass substrate.

2.2 ACTFEL Operation

An understanding of the basic operation of ACTFEL devices is required for any effective modeling effort. Therefore, the next two subsections describe device operation, first from an idealized standpoint and then from a more realistic standpoint in which the effects of space charge are considered.

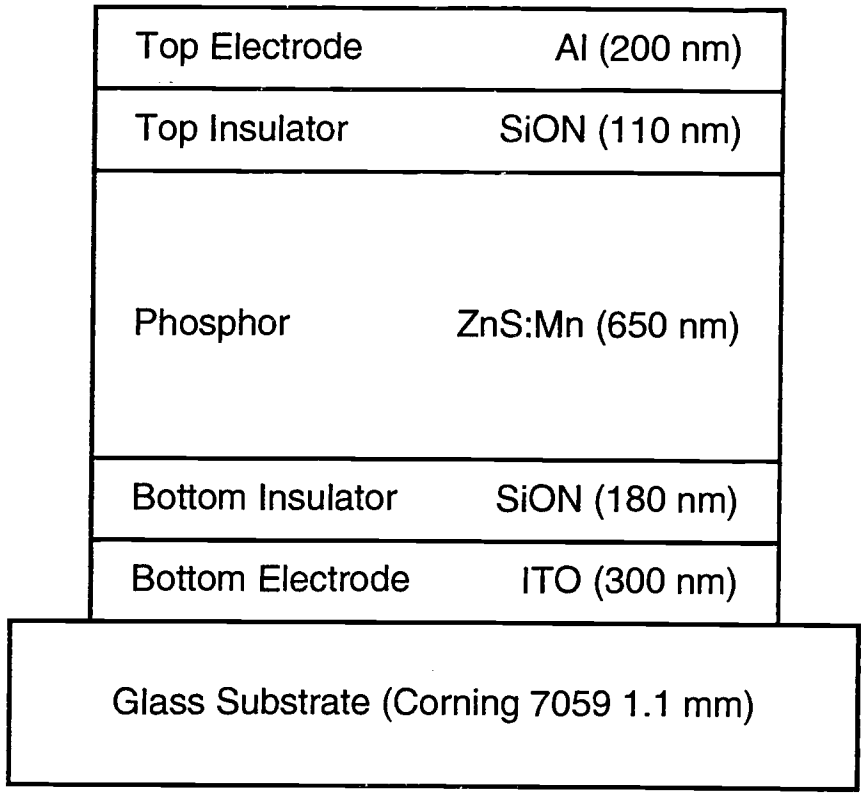

Figure 2.1: ACTFEL device structure.

2.2.1 Ideal Operation

Because the ACTFEL device consists of a phosphor region which is capacitively coupled to the two conductors, the device must be driven by an ac waveform. A number of different driving schemes are used by researchers and in commercial products, most notably bipolar trapezoidal waveforms, sine waves, and triangular waves. In this work, the bipolar trapezoidal waveform shown in Fig. 2.2 is used exclusively, and the polarity of the applied voltage waveform is always with respect to the top (Al) electrode. The letters shown in Fig. 2.2 correspond to important points of the waveform. Point A denotes the point in time when the applied voltage begins increasing. Tunnel-injection of electrons from the cathodic insulator-phosphor interface into the phosphor begins at point B. Points C and D denote the beginning and end of the plateau of the positive pulse of the waveform, where the applied voltage is maintained

at some maximum value. Finally, the voltage is decreased between points D and E; point E denotes the end of the positive pulse. Points F-J correspond to points A-E, but for the opposite voltage polarity. For this work the rise time is 5 μs, the plateau or hold time is 30 μs, and the frequency is usually 1 kHz and sometimes 60 Hz.

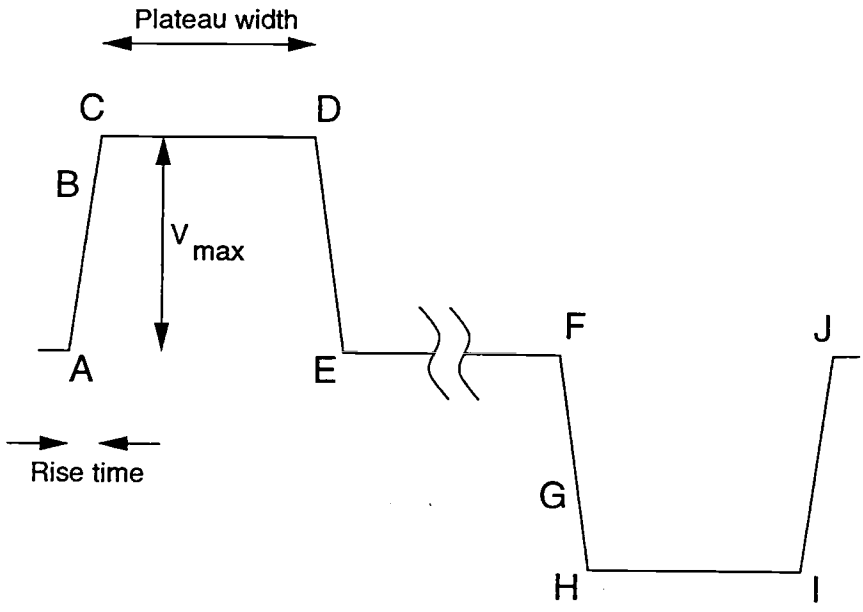

Figure 2.2: ac waveform used to drive ACTFEL devices.

At voltages insufficient to cause tunnel injection and subsequent charge transfer across the phosphor, ACTFEL devices behave electrically like simple capacitors. After the applied voltage exceeds the threshold voltage of a device, though, the behavior changes. The energy band diagram in Fig. 2.3 shows the basic processes that occur within the phosphor layer once the threshold voltage has been reached. First, the electric field at the negatively-driven phosphor-insulator interface (the cathode) becomes large enough that electrons are emitted from a discrete interfacial trap into the conduction band of the phosphor via tunneling. Due to the electric field across the phosphor, these injected electrons are accelerated and drift across the phosphor, as

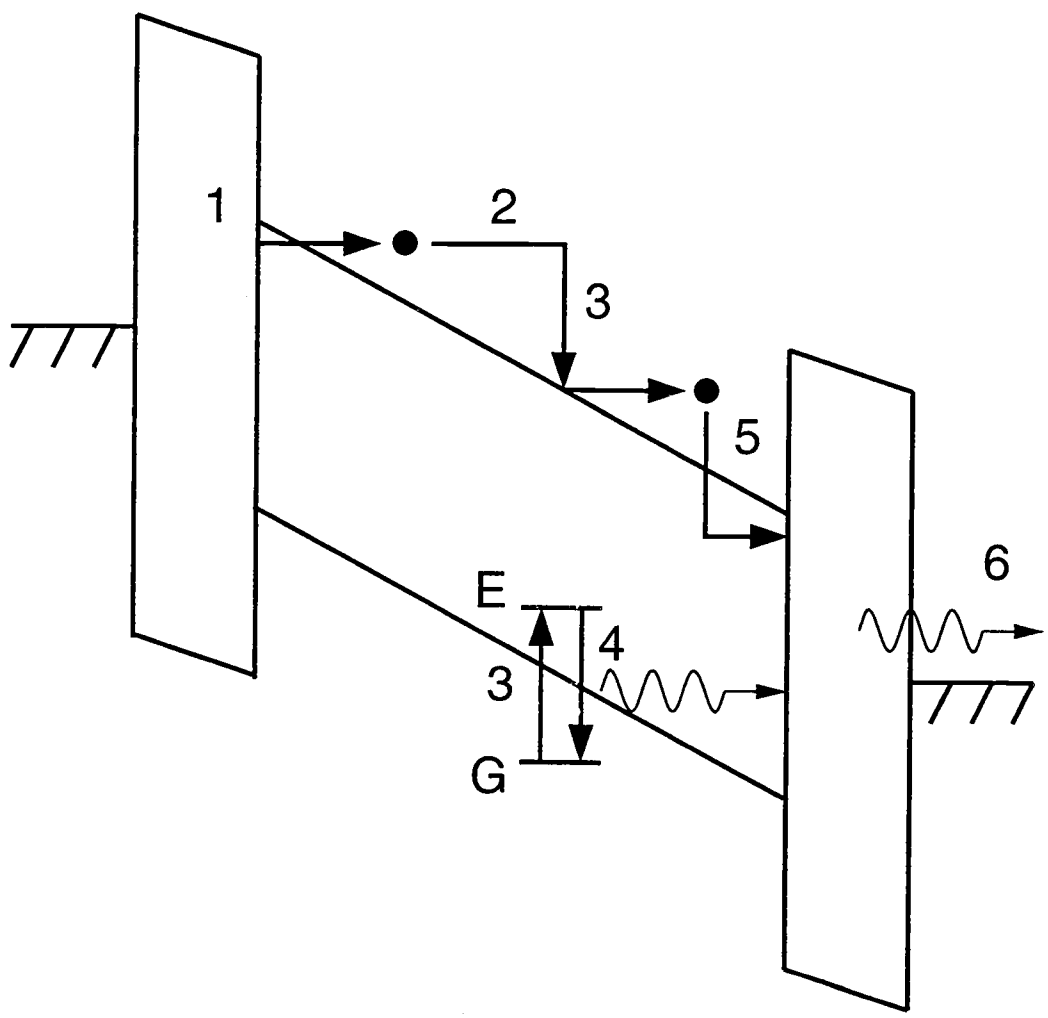

Figure 2.3: Basic processes which occur at applied voltages above threshold. Shown: (1) electrons are tunnel-emitted from a discrete trap at the cathodic insulator-phosphor interface, (2) gain energy from the field and traverse the phosphor region. (3) Some of these excite luminescent impurities from their ground states, which then (4) emit light when they relax back to the ground state. (5) Transferred electrons reach the anode and are retrapped, while (6) visible light is outcoupled from the device.

shown by process (2) in Fig. 2.3. Some of these electrons may collide with a luminescent impurity, such as a Mn atom in ZnS, with enough energy to excite the impurity into an excited state, as shown by process (3). This luminescent impurity will eventually relax back to its ground state. Possibly, the relaxation can occur nonradiatively through phonon emission, in which the excess energy is released as heat to the lattice, but hopefully, the relaxation will occur radiatively and a photon will be emitted, as in process (4) of Fig. 2.3. Process (5) in Fig. 2.3 shows electrons which have traversed the phosphor being retrapped at the positively-driven phosphor-insulator interface (the anode), while process (6) shows visible light being outcoupled from the device. These processes occur in the opposite direction when the external voltage polarity is reversed during the negative pulse portion of the driving waveform.

When electrons are emitted during conduction, a net positive charge is left on the cathode and a net negative charge is left on the anode which serves to counteract the applied electric field. In fact, if enough electrons are available at the interface to be tunnel-emitted, a negative feedback mechanism is created which limits the phosphor electrode field at a fixed value called the steady-state field.

After drifting across the phosphor, electrons emitted from the cathode end up trapped in interfacial traps at the anodic phosphor-insulator interface, creating a net negative charge at the anode. Thus, at the end of the positive voltage pulse, an imbalance of charge exists within the ACTFEL device, denoted "polarization charge." This results in an electric field (the "polarization field") across the phosphor even in the absence of an external voltage; as shown in Fig. 2.4, this field is opposite in direction to the field established during the previous applied pulse. There are two consequences of this field. The first is the phenomenon of leakage charge. During the portion of the applied waveform between the two pulses (between points E and F in Fig. 2.2), the ACTFEL device has an energy band similar to that shown in Fig. 2.4. Process (1) in Fig. 2.4 shows the re-emission of an electron back into the phosphor; this may occur through tunneling or some thermally-activated process, although the

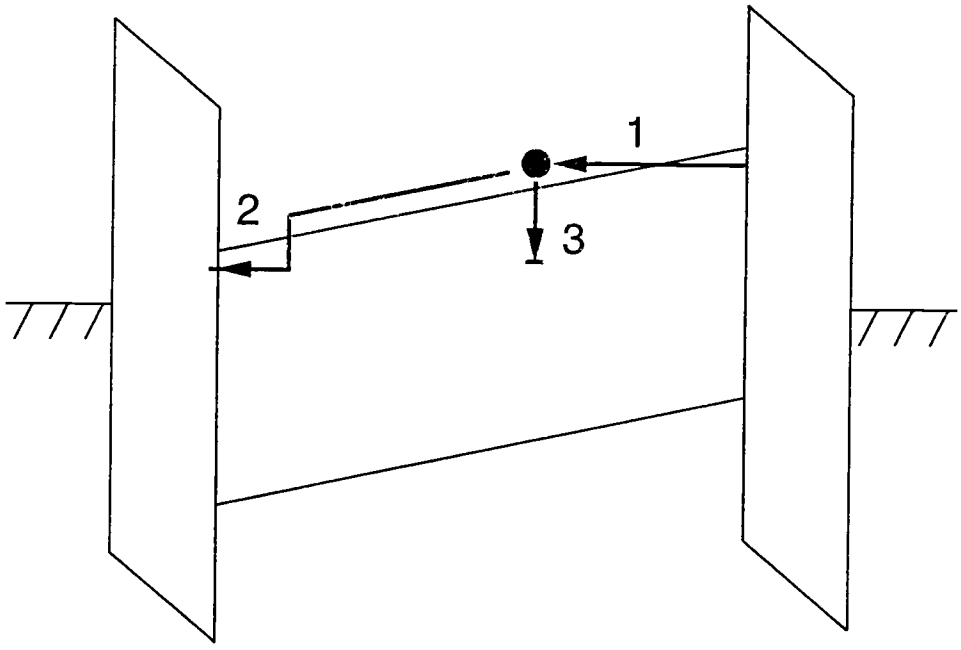

Figure 2.4: ACTFEL band structure during the interpulse interval, showing (1) tunnel emission of an electron from an interface trap, which (2) is retrapped at the opposite interface or (3) recombines with an ionized bulk trap.

precise nature of the re-emission is poorly understood. This electron then drifts back across the phosphor due to the residual electric field until it is retrapped at the opposite interface ((2) in Fig. 2.4) or recombines with an ionized trap within the bulk of the phosphor ((3) in Fig. 2.4).

The second consequence of the residual electric field is a lowering of the voltage necessary to operate the device. Because the polarization field is oriented in the same direction as the phosphor field to be established by the next pulse, less external voltage needs to be applied before the field is high enough to cause electron emission. Furthermore, more electrons are trapped at the cathodic interface at the beginning of a pulse than would be without the presence of polarization charge, increasing the likelihood of a tunneling event even at identical fields. The external voltage required for electron emission without the presence of a polarization field is termed the "threshold voltage," and the voltage required in the presence of polarization is

termed the "turn-on" voltage. The turn-on voltage is dependent on the degree of polarization present at the beginning of a given pulse and thus on both the maximum applied voltage and the frequency of the waveform.

2.2.2 Non-ideal Operation: Space Charge

In the previous discussion, it was assumed that the applied voltage which is dropped across the phosphor region establishes a uniform electric field across the phosphor. In real ACTFEL devices, the presence of space charge results in band-bending in the phosphor region of the energy band diagram, as depicted in Fig. 2.5.

The formation of space charge is usually thought of as most probably occurring through one of three processes. The first is the ionization of bulk traps. [3, 4, 5] Fig-

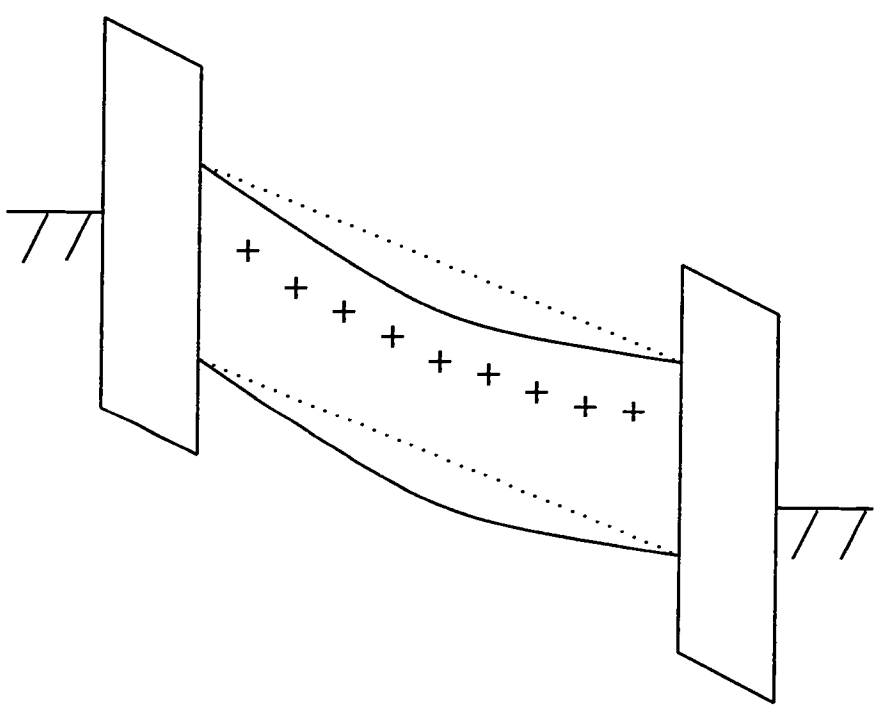

Figure 2.5: Space charge in the phosphor region results in a non-uniform electric field manifested by band-bending (solid lines). The dotted line shows the case without space charge (uniform electric field).

ure 2.6 shows a bulk trap being ionized. Such ionization could occur via field emission, in which the local electric field at the trap is high enough that an electron can tunnel from the trap into the phosphor conduction band, where it drifts to the anode under the influence of the electric field. The emitted electron leaves a localized positive charge behind at the trap that pushes the bands downwards. Alternatively, the ionization process illustrated in Fig. 2.6 could be accomplished via thermionic emission, in which an electron gains enough thermal energy to overcome the energy barrier, or via phonon-assisted tunneling, in which a thermally excited electron tunnels from the trap into the phosphor conduction band.

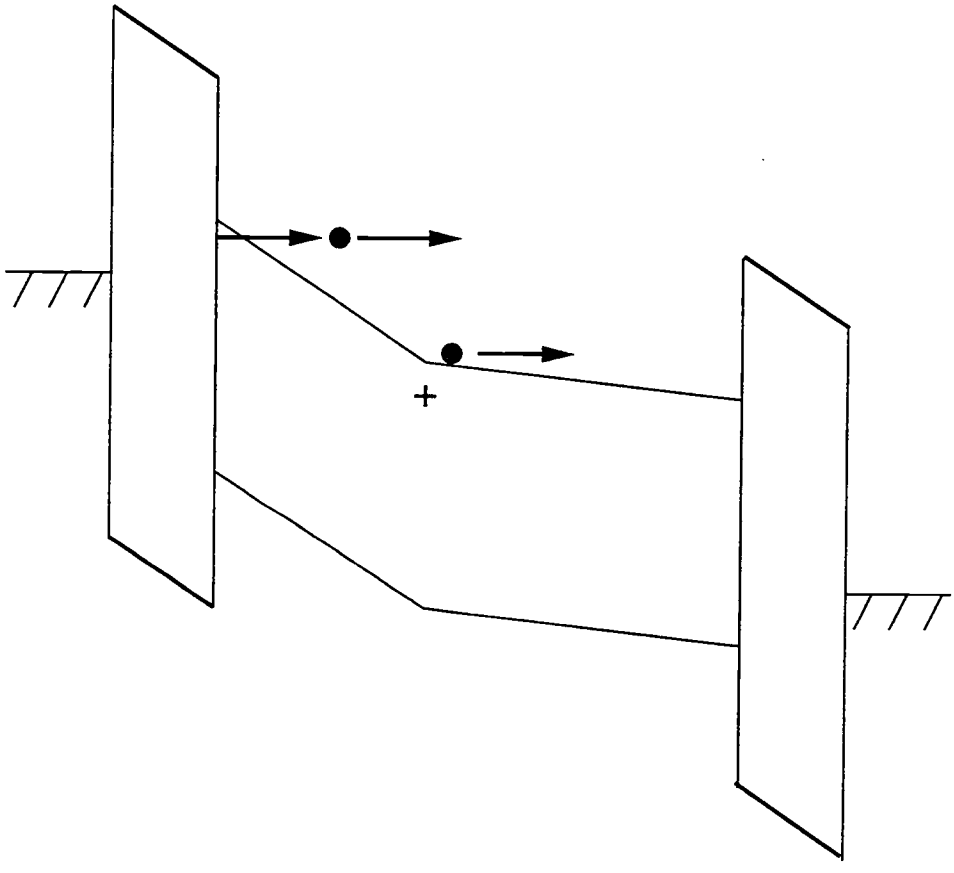

Figure 2.6: Space charge creation in the ACTFEL phosphor through field emission from a bulk trap.

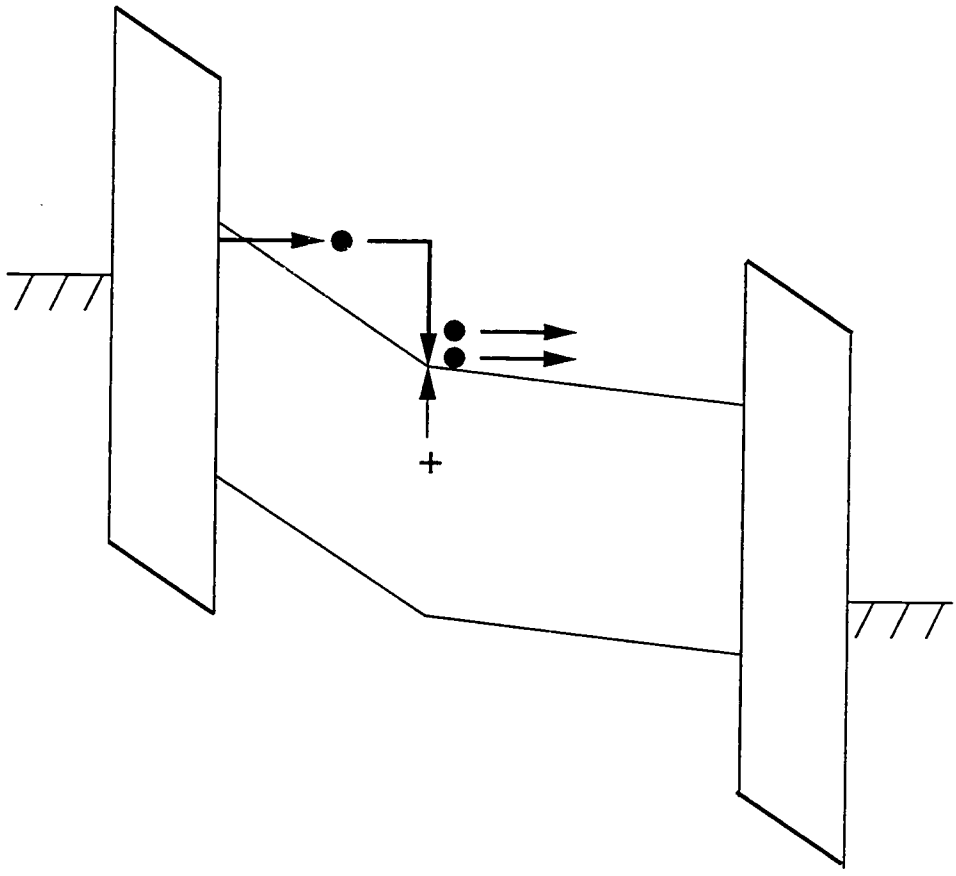

Figure 2.7: Space charge creation in the ACTFEL phosphor through trap-to-band impact ionization.

Figure 2.7 illustrates the second space charge formation mechanism, in which bulk traps are ionized through trap-to-band impact ionization. [5, 6, 7, 8] In this process, an electron is accelerated by the phosphor field as it drifts towards the anode. If the electron has enough kinetic energy when it collides with a trap, it may promote a second electron to the conduction band. Both electrons drift to the anode, leaving a localized positive charge at the trap.

The third widely assumed method of space charge creation is hole trapping. [9] In a similar process to trap-to-band impact ionization, an electron may be promoted to the conduction band and a hole concomitantly to the valence band through band-to-

band impact ionization. This impact ionization-induced hole may then drift towards the cathode until it is captured by a trap, also creating positive space charge.

The band-bending due to the presence of space charge has important effects on the operation of an ACTFEL device. First, the formation of positive space charge increases the field near the cathode, as evident from the increased slope of the bands near the cathode in Figs. 2.5–2.7. This makes electron emission from the cathode more efficient. Furthermore, it has been suggested that some device degradation may be caused or facilitated by energy released by hot electrons thermalizing to the bottom of the conduction band as they impinge on the anodic phosphor-insulator interface. [7, 10, 11] Due to the presence of space charge, the electric field is reduced at the anode, which results in a cooler electron distribution and may therefore reduce the rate of device degradation. On the other hand, electrons are accelerated by a significantly lower field during much of the phosphor due to the presence of space charge; this means that impact excitation of luminescent impurities becomes less and less efficient as the electrons approach the anode.

2.3 Electrical Characterization

In order to evaluate the validity of a computer model, the results of a simulation must be compared to experimentally measured data taken from an operating ACTFEL device. This section describes the most common electrical characterization techniques, which are employed in the rest of this work. First, the experimental test setup is described. Then, the external charge-voltage (Q-V), capacitance-voltage (C-V), internal charge-phosphor field (Q-F_p), and maximum charge-maximum voltage (Q_{max}-V_{max}) techniques are examined.

2.3.1 Experimental Setup

The experimental configuration used to obtain experimental data for this work is shown in Fig. 2.8. The ACTFEL device-under-test (D.U.T.) is connected in series

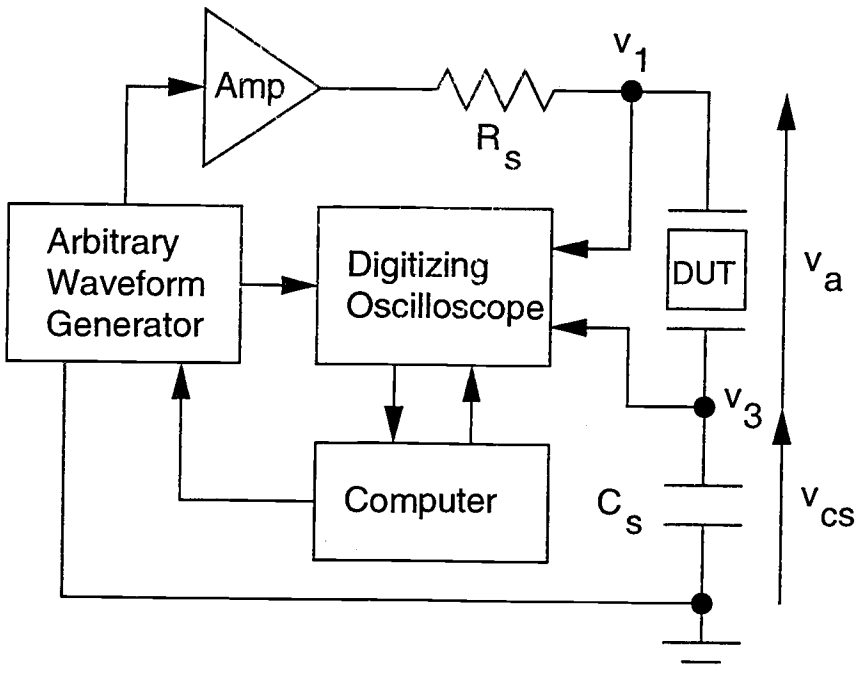

Figure 2.8: Typical ACTFEL experimental characterization setup.

with a sense capacitor C_s and a series resistance R_s. The computer is used to program the arbitrary waveform generator (Wavetek model 395) to output a low-voltage bipolar trapezoidal waveform. Since the Wavetek output is limited to a maximum of 5 V, a high-voltage amplifier (a dual Apex high-voltage operational amplifier configuration) is used to amplify the signal to a magnitude appropriate for ACTFEL operation. This high-voltage signal is applied to the R_s-ACTFEL device-C_s stack. The digitizing oscilloscope (Tektronix model TDS420) measures the voltages at either side of the ACTFEL device and sends this data to the computer for processing and analysis.

All of the standard electrical measurements rely on the presence of the sense capacitor in Fig. 2.8. The capacitor is chosen so that its capacitance is much larger than the capacitance of the ACTFEL device to minimize its effect on the measurement; typically, a capacitor on the order of 100 nF is used. The charge on C_s is measured as a function of the applied voltage across the ACTFEL device terminals to form the

basis of external charge versus voltage (Q-V) analysis, as discussed in the next subsection. The other common characterization techniques result from transformations of this data.

The series resistance R_s in Fig. 2.8 is typically 500 Ω and is included for two reasons. First, the resistor limits the current to the device in the case of catastrophic device failure, thereby protecting the expensive high-voltage amplifier from damage. Second, larger values of resistance have been associated with increased device durability. This is important especially during device aging over large time periods.

2.3.2 External Charge versus Voltage (Q-V) Analysis

The external charge-voltage (Q_e-V_e or Q-V) experiment [12, 13] is the most straight-forward of the standard electrical measurements. The external charge as seen at the terminals of the ACTFEL device is plotted against the applied voltage. The voltage applied to the device, v_a, is determined through subtraction of the two voltages measured by the oscilloscope, and, as mentioned in Sec. 2.3.1, the external charge of the device is determined by measuring the charge on the sense capacitor:

$$q_{ext} = v_3 \times C_s = v_{cs} \times C_s \tag{2.1}$$

and

$$v_a = v_1 - v_3 \tag{2.2}$$

By plotting q_{ext} against v_a, a Q-V plot similar to that in Fig. 2.9 is created.

The Q-V plot shown in Fig. 2.9 is from an evaporated ZnS:Mn device, which is in many respects very nearly an "ideal" ACTFEL device, making it attractive to use for illustrative purposes. The letters on the plot correspond to the letters in Fig. 2.2 and thereby show the correspondence between the applied waveform and the Q-V plot that results. Notice that point A is not coincident with the origin of the plot. This is due to the presence of polarization charge from the previous pulse,

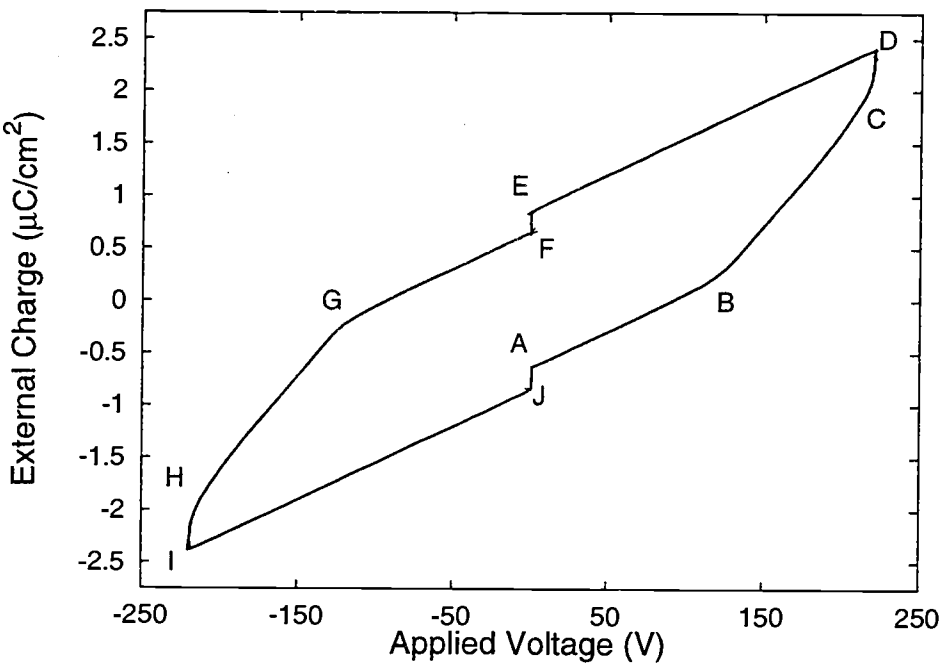

Figure 2.9: An experimental Q-V plot from a ZnS:Mn ACTFEL device driven 40 V above threshold.

as discussed in Sec. 2.2.1. The amount of polarization charge at point A from the previous negative pulse is termed Q^{-}_{pol}. As the voltage across the device is ramped up between points A and B, the external charge increases with a slope equal to the total device capacitance, C_t. At point B, the device turns on and conduction charge begins flowing through the phosphor region. In an ideal device, this charge transfer is equivalent to an infinite phosphor capacitance, so that it is shorted out of the circuit. Thus, between points B and C, q_{ext} increases with a slope equal to the capacitance of only the insulator layers of the device, C_i. Between C and D, the applied voltage is at its maximum value, and the charge that is conducted across the phosphor during this time is called relaxation charge, Q^{+}_{relax}. The voltage is decreased back to zero between points D and E, and the slope of the Q-V plot is once again equal to the total device capacitance. From point E to point F, the external applied voltage is zero, but charge transfer still occurs at a reduced rate due to charge leakage, as

described briefly in Sec. 2.2.1. These processes are repeated for the negative pulse, and the corresponding transferred charge and voltage values are labeled similarly to the positive-pulse values, but with the '+' and '−' signs interchanged.

2.3.3 Capacitance versus Voltage (C-V) Analysis

As discussed in Sec. 2.3.2, the slope of the Q-V plot yields information about the device capacitance. This can be used to generate a capacitance-voltage (C-V) curve. [13, 14, 15] Although other researchers have used a C-V technique utilizing a sense resistor to measure the current, it is convenient to simply take the derivative of the external charge with respect to the applied voltage:

$$C = C_s \frac{dv_{cs}}{dv_a} \simeq \frac{\Delta q_{ext}}{\Delta v_a} \tag{2.3}$$

The derivative of the Q-V data is taken numerically according to Eq. 2.3 for points between A and D and between F and I to form positive- and negative-polarity C-V plots, respectively.

Fig. 2.10 shows an experimental C-V curve from an evaporated ZnS:Mn device. Several features are apparent. First, notice that the capacitance is initially the total capacitance, C_t, before increasing to the insulator capacitance, C_i. Second, notice that the transition between these two regions is not abrupt. The slope of this transition as well as changes in the transition with prolonged device operation reveal important information about the nature of the ACTFEL device. Next, Fig. 2.10 shows the capacitance increasing to infinity as the device reaches its maximum voltage. This is caused by the vanishing of Δv_a during the hold time of the applied waveform. This point should correspond to point C on Fig. 2.2, but due to the RC time constant introduced by the experimental setup, it actually occurs between points C and D, necessitating taking the derivatives in Eq. 2.3 past point C. Finally, the capacitance increases from C_i shortly before the capacitance increases to infinity (around 170 V in Fig. 2.10). The point at which this increase occurs corresponds to the programmed

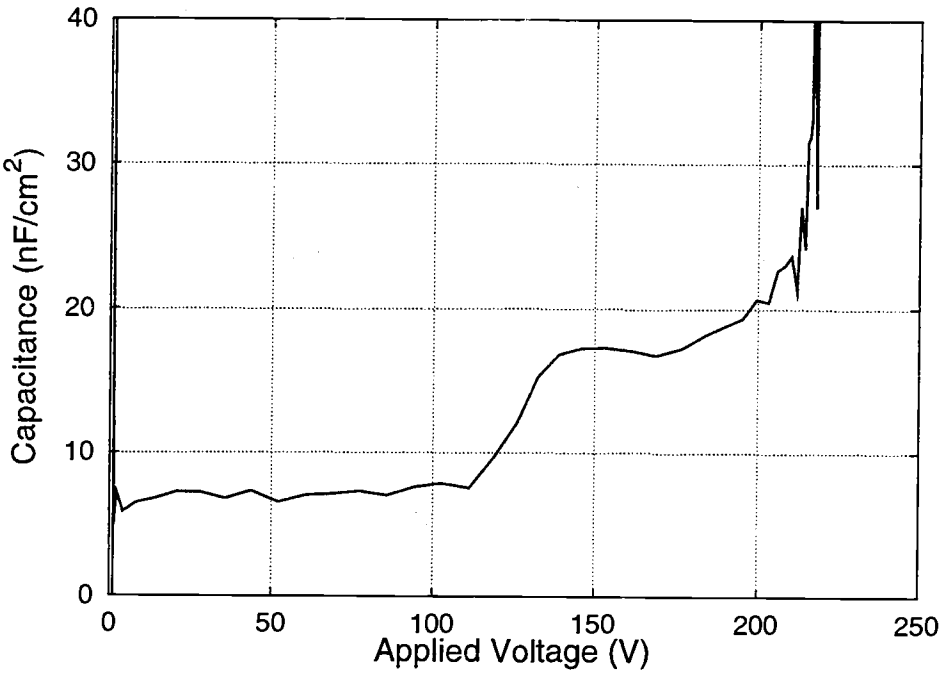

Figure 2.10: An experimental C-V plot from a evaporated ZnS:Mn ACTFEL device driven 40 V above threshold.

applied voltage reaching its maximum value and leveling off to the plateau portion of the waveform; in other words, this point corresponds to point C in Fig. 2.2.

In many ACTFEL devices, the 'insulator' capacitance shown in the C-V plot does not correspond precisely to the physical insulator capacitance value. [7] Most often, the capacitance overshoots the physical value. This is an indicator of positive dynamic space charge creation within the phosphor. Less often, the capacitance undershoots the physical value. This may be due to poor injection of electrons from the cathodic interface, bulk emission of electrons instead of interfacial emission (the capacitance is reduced since the bulk-emitted electrons do not traverse and "short out" the entire phosphor in this case), or the trapping of large numbers of injected electrons in the bulk instead of at the anodic interface.

2.3.4 Internal Charge versus Phosphor Field ($Q\text{-}F_p$) Analysis

Although Q-V analysis is convenient, the capacitive displacement charge is included in the plots due to the data's purely external nature. However, it is often more interesting to view device physics quantities associated only with the phosphor region, without including the voltage dropped across the insulators or the displacement charge. Thus, the externally measured data are often transformed to reflect internal quantities in internal charge-phosphor field ($Q\text{-}F_p$) analysis. The transformation is given by

$$q_{int} = \frac{C_i + C_p}{C_i} q_{ext} - C_p v_a \tag{2.4}$$

and

$$f_p = \frac{1}{d_p} \left[\frac{q_{ext}}{C_i} - v_a \right], \tag{2.5}$$

which follow from Bringuier's relation of ACTFEL physical processes. [16]

A $Q\text{-}F_p$ plot typical of an evaporated ZnS:Mn ACTFEL device is shown in Fig. 2.11. Note that following the letters on the waveform as was done in Sec. 2.3.2 leads clockwise around the $Q\text{-}F_p$ plot, instead of counter-clockwise as in the Q-V plot. This is a result of the sign convention adopted by Bringuier. [16] Several features of the $Q\text{-}F_p$ curve deserve comment. First, notice that the phosphor field between points B and C is constant, as explained in Sec. 2.2.1. This steady-state field value may vary with the maximum applied voltage to the device, or remain fixed over a large range of overvoltages. The latter case, in which a device is said to exhibit 'field clamping,' is observed for ZnS:Mn devices. In devices which exhibit a large amount of dynamic space charge, such as cerium-doped strontium sulfide (SrS:Ce) devices, the field between B and C 'overshoots' the steady-state field as a result of the processes described in Sec. 2.2.2. This overshoot is visible on the $Q\text{-}F_p$ plot and is related to C-V overshoot. Between points C and D, when the applied voltage is at a constant maximal value, charge continues to be transferred across the phosphor

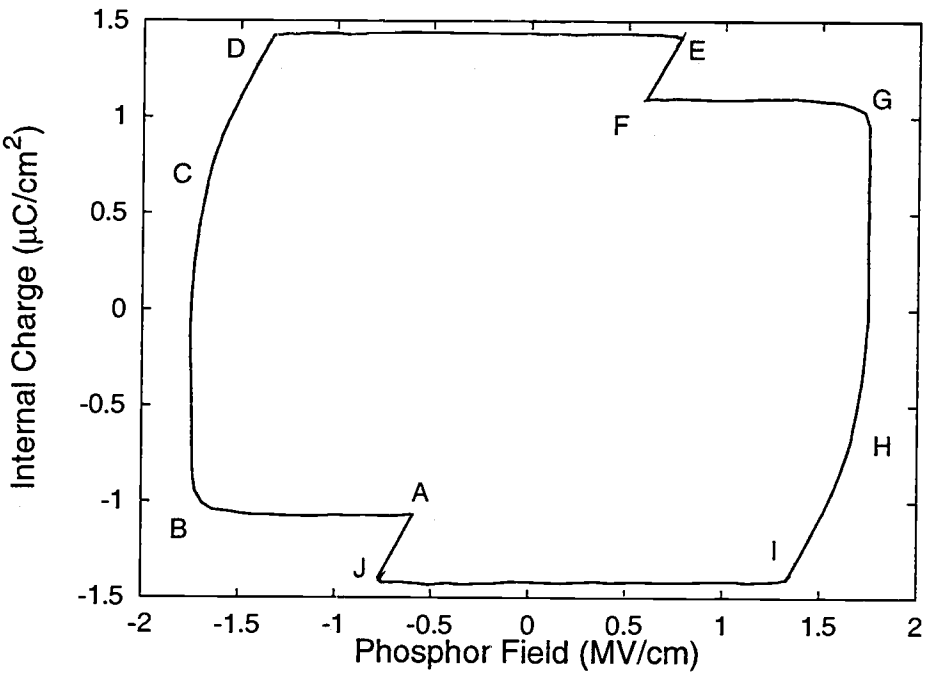

Figure 2.11: An experimental Q-F_p plot from a ZnS:Mn ACTFEL device driven 40 V above threshold.

at a reduced rate, and the phosphor field is reduced as a result; the amount of the reduction is termed the relaxation charge, Q^{+}_{relax}. During the period of no applied voltage between E and F, leakage charge is observed, as discussed in Sec. 2.2.1.

The largest problem with the Q-F_p technique is the extremely sensitive dependence on insulator and phosphor capacitance values in Eqs. 2.4 and 2.5. Generally, using the physical capacitances calculated from approximately-known device layer thicknesses and their corresponding dielectric constants leads to distorted Q-F_p curves. [7] For the more ideal devices, like ZnS:Mn, it is easy to extract the capacitance values from the slopes of the Q-V plot before using Eqs. 2.4 and 2.5. Additionally, uncertainty in the phosphor thickness is alleviated since the thickness can be back-calculated from the phosphor capacitance value. But, for devices that exhibit a large amount of space charge or other non-ideal behaviors, this process is not straight-forward. For the well-behaved evaporated ZnS:Mn devices, though, this

analysis can be used to verify capacitance values from the shape of the Q-F_p plot: if the total device capacitance is not accurate, the portions between A-B and D-E will not be horizontal, and if the phosphor capacitance is not accurate, the vertical sections will be skewed.

2.3.5 Maximum Charge versus Maximum Voltage (Q_{max}-V_{max}) Analysis

Maximum charge versus maximum applied voltage (Q_{max}-V_{max}) analysis, as the name implies, shows the maximum charge on the sense capacitor related to the maximum applied voltage. [17, 18, 19] Two flavors exist: in Q_{max}-V_{max} analysis the internal charge (from Eq. 2.4) is plotted versus the maximum external voltage. In a Q^e_{max}-V_{max} plot, only the external quantities are used. A sample Q^e_{max}-V_{max} plot is shown in Fig. 2.12 for an evaporated ZnS:Mn ACTFEL device. Notice from Fig. 2.12 that the slope of the plot below threshold is equal to the total device capacitance, while for large voltages the slope approaches the insulator capacitance value. Immediately after threshold, the slope of the Q^e_{max}-V_{max} plot is larger than the insulator capacitance. This is seen clearly as an overshoot on a differentiated Q^e_{max}-V_{max} plot, termed transferred charge capacitance overshoot, and has been previously thought to be evidence of metastable hole trapping or static space charge. [17]

2.4 Modeling in SPICE

This section describes the use of SPICE for simulating ACTFEL devices. First the SPICE program operation is described in general terms, and then motivation for the use of SPICE to simulate ACTFEL devices is presented. Next, previous ACTFEL SPICE models are discussed briefly. Finally, important issues to consider in using SPICE are examined.

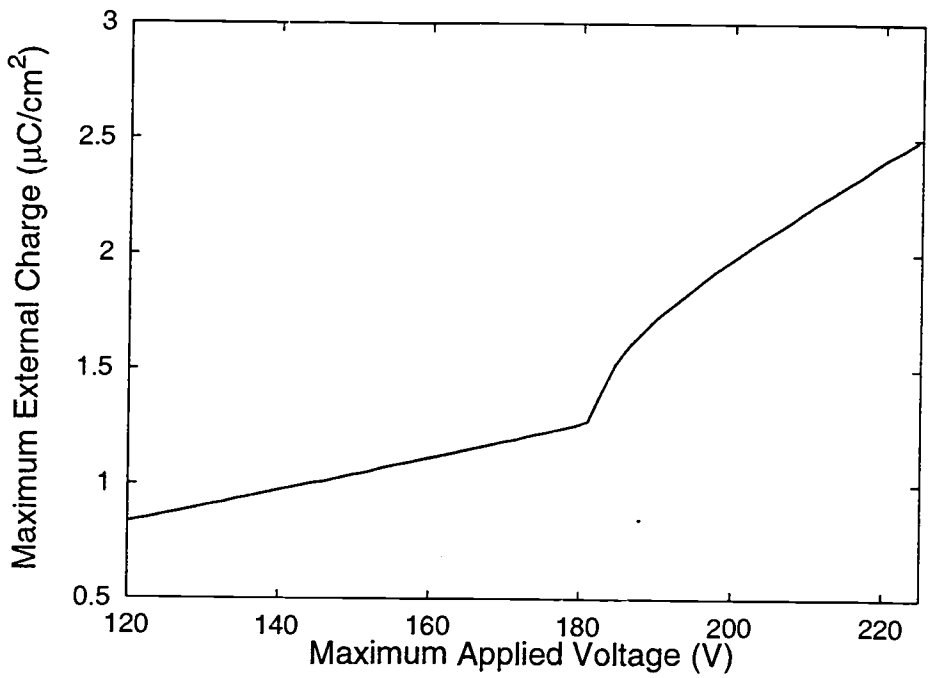

Figure 2.12: An experimental Q^e_{max}-V_{max} plot from a ZnS:Mn ACTFEL device driven at 1000 Hz.

2.4.1 The SPICE Program

SPICE (Simulation Program with Integrated Circuit Emphasis) is a computer-aided design program for circuit simulation, originally developed at the University of California at Berkeley. [20] Users may specify circuit elements in the input circuit descriptions, such as resistors, capacitors, inductors, independent and voltage- and current-dependent current and voltage sources, and transmission lines. Additionally, generic models for the basic active devices, such as diodes and various transistors, are also included. Many models of common semiconductor devices are freely available as well, often from the product vendors.

SPICE allows three modes of simulation. In dc analysis, SPICE open-circuits all capacitors and short-circuits all inductors before finding the dc solution. In ac analysis, SPICE first uses dc analysis to determine the dc operating point of a circuit before determining the frequency-dependent behavior of the circuit, outputting pa-

rameters such as voltage gain at a given frequency. Finally, transient analysis relates how the circuit behaves as a function of time. Dc analysis is again used to determine the condition of the circuit at the initiation of the simulation.

For all modes of operation, SPICE examines the circuit using a node-voltage oriented approach. For circuits containing only passive devices and simple sources, the equations describing the circuit are determined using Kirchhoff's current and voltage laws; these can then be solved using linear algebra. When non-linear circuit elements are added to the circuit under consideration (as is always the case in this discussion) SPICE is forced to linearize the non-linear elements using an iterated Newton-Raphson method. An initial guess of the node voltages (from the circuit's initial conditions or a previous iteration) is made and the linearized node-voltage equations evaluated. If both the node voltages and the non-linear branch currents converge to within certain user-adjustable parameters, the simulation moves forward to the next operation (i.e. the next time step in a transient analysis). Otherwise, the guesses are refined and a new solution calculated.

2.4.2 ACTFEL Modeling in SPICE

SPICE has proved valuable in ACTFEL simulation in several ways. First, simple models can be constructed very quickly in SPICE relative to device physics-based modeling approaches, and SPICE is somewhat more user-friendly and easy to learn, if one is not already familiar with typically C-programmed device physics-based simulation techniques. Second, since SPICE is commonly used by electrical engineers to simulate electronic circuits, it is convenient to have a SPICE-based ACTFEL model which can be used in the process of designing display driver electronics. Once a model for a single display element has been created in SPICE, it is easy to create any number of similar elements in an array and add driver electronics to the simulation, for instance. Third, common elements such as resistors are very easily included in a circuit netlist, allowing features of the laboratory test setup to be simulated. Including,

for instance, the series resistance R_s and ITO sheet resistance proved difficult in previous device physics-based modeling efforts and were generally either disregarded or added only after moderate difficulties. [8] Several important electrical characteristics of ACTFEL devices seen in laboratory measurements are only apparent in simulation when these series resistances are included.

Two approaches to modeling ACTFEL devices in SPICE have been undertaken in the past. The first approach is to build a model from scratch with the aim of simply modeling the electrical and/or optical characteristics of ACTFEL devices, without regard to actual physically-occurring processes. The second approach is to first develop a device physics-based simulation – a simulation in which known or probable physical processes are modeled using appropriate equations – and then to translate the device physics equations to dependent current sources in a SPICE model. The first approach is likely to provide a simpler model, which is convenient in terms of simulation time and external circuit design, while the second approach is more intellectually satisfying, since it is more "real." Which approach is used depends on the goal of the simulator, the degree of accuracy required in the simulation, and the amount of predictive power the model is expected to provide. The previous modeling efforts discussed in the following section used both approaches, but more or less separately; in this work, a combination of both approaches is generally used.

2.4.3 Previous ACTFEL Modeling in SPICE

One of the most common and most well-known ACTFEL equivalent circuit models was suggested by Smith, and is shown in Fig. 2.13. [21] In this model, the insulators are represented as capacitors and the phosphor layer is represented as a capacitor shunted by two back-to-back Zener diodes which account for the conduction across the phosphor. Although this model was not originally presented as a SPICE model, it became the basis for many later SPICE-based ACTFEL models and is therefore mentioned here.

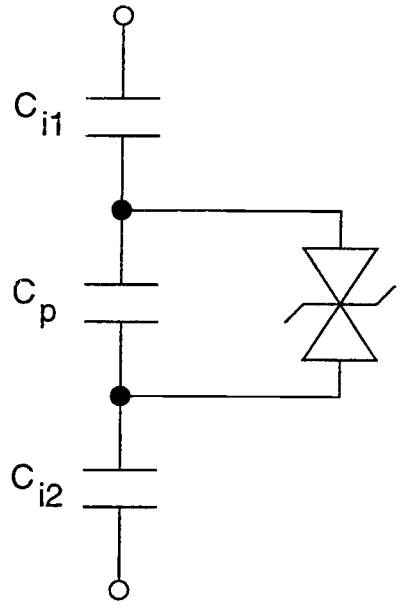

Figure 2.13: A basic ACTFEL SPICE model proposed by Smith consisting of two back-to-back Zener diodes.

One of these was the first ACTFEL SPICE model, which was reported by Davidson et al. and is shown in Fig. 2.14. [15, 22] Building on the capacitor stack and back-to-back Zener diodes of Smith's model, the model in Fig. 2.14 includes a phosphor shunt resistor R_p to account for leakage charge, a resistor R_{ITO} to account for the series resistance of the ITO electrode, and a resistance R_d, the inclusion of which leads to improved simulation results. Davidson used this model to compare experimental and simulated C-V characteristics of evaporated ZnS:Mn ACTFEL devices.

Douglas et al. expanded Davidson's model to include a parallel RC network in series with the back-to-back Zener diodes which shunt the phosphor capacitor, as shown in Fig. 2.15. [23, 24, 25] This RC network accounts for the dependence of the turn-on voltage and relaxation charge on the applied voltage waveform and improves the simulated transient phosphor field trends. In addition, Douglas created an optical SPICE model which works in conjunction with the model shown in Fig. 2.15. The

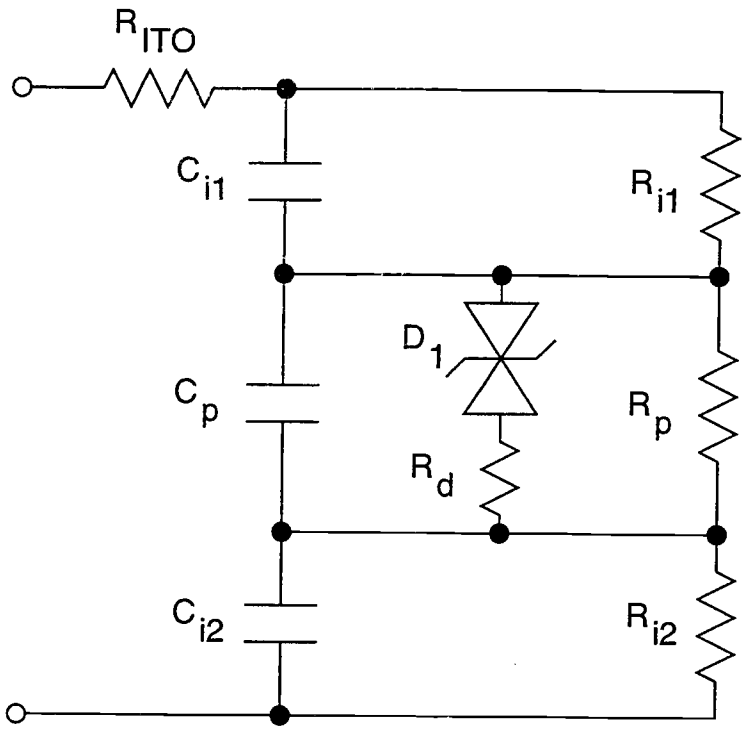

Figure 2.14: Davidson's ACTFEL SPICE model.

optical model predicts transient luminance (L(t)) and luminance-voltage (L-V) trends by using conduction current of the electrical SPICE model to drive an RC network.

Shown in Fig. 2.16 is an ACTFEL equivalent circuit model developed by Åberg. [26] This model has three different variations. If the impedance labeled 'X' in Fig. 2.16 is a resistor, the model can be used to simulate ALE ZnS:Mn ACTFEL devices which do not exhibit L-V hysteresis. If the impedance is a resistor and capacitor in series, the model can be used to simulate devices which do exhibit L-V hysteresis. Finally, if the impedance is an inductor, Åberg shows that the circuit can be used to account for dynamic space charge generation.

Figure 2.17 shows Keir's SPICE equivalent-circuit representation of his device physics-based single-sheet space charge model. [4, 5, 27] In this model, space charge is created via field emission at one localized sheet within the phosphor layer, giving rise to experimentally seen manifestations of space charge, such as C-V overshoot. A

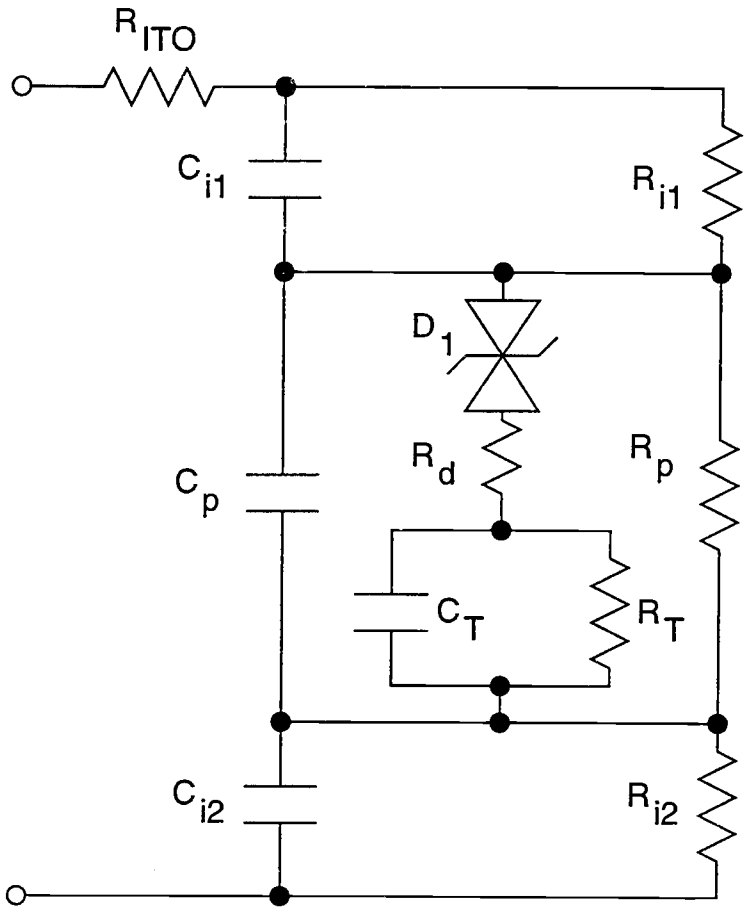

Figure 2.15: More complex ACTFEL SPICE model, proposed by Douglas, which is identical to Davidson's model except that a parallel RC network is inserted in the back-to-back Zener diode shunt path.

very similar model is discussed in depth in Section 3.3, in which a single-sheet charge SPICE model is developed as a stepping stone on the way towards a two-sheet charge model.

2.4.4 SPICE Simulation Issues

As with most computer-aided design tools, the use of SPICE can be quite complicated. This subsection covers some of the more important considerations when using SPICE for ACTFEL simulation, including the choice of SPICE versions, the

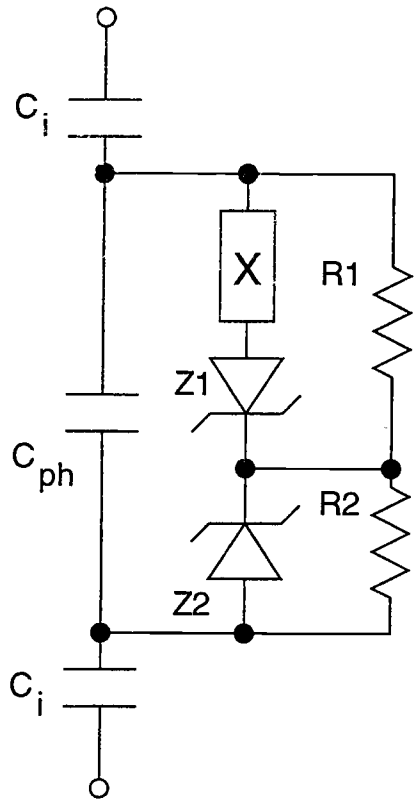

Figure 2.16: Åberg's equivalent circuit model for an ACTFEL device. The impedance labeled 'X' in series with the Zener diode can be a (i) resistor, (ii) a resistor and capacitor in series, or (iii) an inductor.

trade-off between simulation accuracy and speed, and the extraction of data from SPICE output files.

2.4.4.1 SPICE Flavor Selection

SPICE programs are available in a number of different packages. Versions of SPICE (SPICE2 and SPICE3 in several forms) based on source code originally developed at U. C. Berkeley are freely available to the public, but several companies also produce their own versions of SPICE-compatible programs. These are most notably OrCad's PSpice for IBM PC-compatible computers running the Windows operating system and Avant! Corportation's HSPICE for various UNIX-based computers. (PSpice and HSPICE were formerly available from MicroSim and Meta-Software, re-

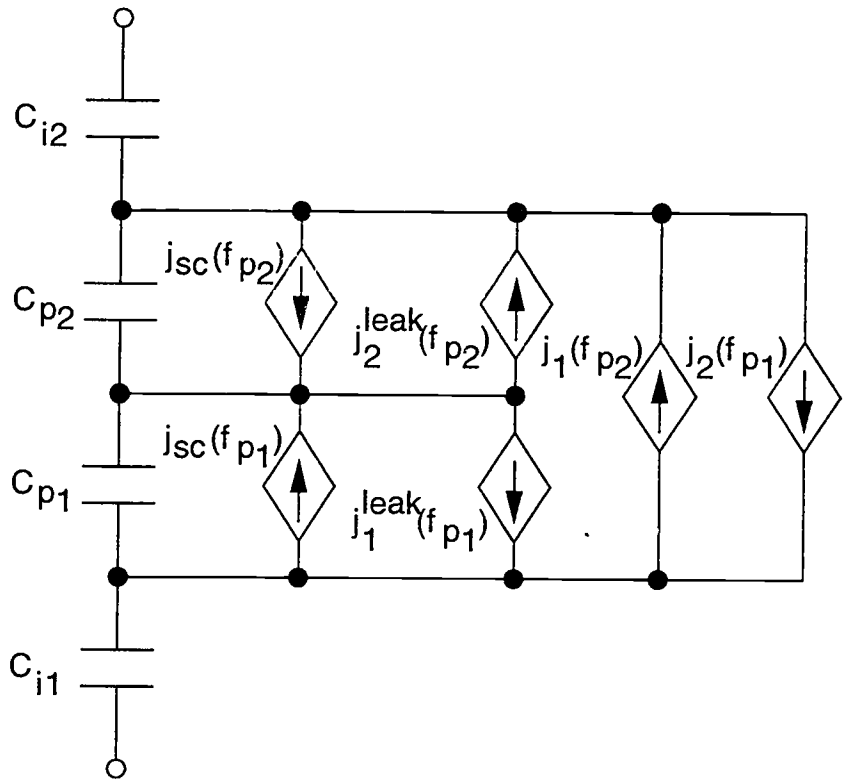

Figure 2.17: Keir's single-sheet space charge model equivalent circuit for an ACTFEL device in which space charge generation is assumed to occur via field-aided emission from bulk traps.

spectively.) These proprietary SPICE packages are generally compatible with SPICE2 and SPICE3 netlists, but add additional features such as circuit parameter optimization routines, semiconductor device libraries, or graphical interfaces for setting up simulations or viewing the results.

In this study, HSPICE is used exclusively for several reasons. First, HSPICE is already maintained by the College of Engineering at Oregon State University. Second, HSPICE provides a Fowler-Nordheim diode model (based on the Fowler-Nordheim tunneling equation) which is particularly useful for simple ACTFEL simulation. Third, HSPICE contains an algebraic interpreter which can be used to create more complex models – a parameter of the circuit can be defined as an equation

rather than a fixed quantity. Finally, HSPICE has improved simulation convergence as compared to SPICE2. [20]

2.4.4.2 Accuracy versus Speed

For all of the common experimental electrical characterization techniques used in this study, the ACTFEL device under excitation is subjected to many thousands of periods of the ac measurement waveform, so that the device is in a "steady-state" condition when measurements are taken. This means that, at the beginning of an applied voltage pulse, the static space charge in the phosphor has already been completely established, and that polarization charge from a previous, opposite-polarity pulse is present in a quantity identical to the amount that will be present at the beginning of the following same-polarity pulse. Thus, assuming device aging is negligible, measurements taken over one period will be identical to measurements taken over another period if the applied waveform has not changed.

Similarly, simulation experiments must be allowed to run long enough so that steady-state conditions have been met, but due to the amount of computer time needed for each period of simulation, the number of cycles simulated needs to be minimized. The usual procedure is to simulate a circuit over an increasing number of periods, note when the results change insignificantly from one cycle to the next, and use this number of periods in future simulations. The more complex the model being simulated is, the more periods are likely to be needed. In this work, it is found that simulation results for models excluding space charge creation mechanisms are stable after only two periods are simulated (that is, accurate steady-state data points are generated during the second period). Simulations are generally run for three periods (i.e. measurements are taken during the third period) to be safe.

An important simulation parameter is the size of the external timestep used during transient analysis. The external timestep is the amount of time between data points which are output by SPICE, as opposed to the internal timestep used by

SPICE to evaluate a circuit. The main effect of modifying the external timestep is to reduce the amount of data produced, thereby reducing the amount of information that needs to be written to disk or loaded into graphing programs and the number of calculations (for Q-F_p analysis, for instance) that need to be performed. In the experimental measurement setup, data for Q-V analysis is taken and stored only for the 40 μs of the positive and negative pulses (where everything usually of interest in Q-V analysis occurs) at timesteps of 0.2 μs per data point. In simulation, of course, it is easy to specify different timesteps for different portions of the applied voltage waveform. In the simulations conducted in this study, an external timestep of 0.1 μs per data point during applied pulses is used to ensure smooth curves, especially in the C-V graphs (which are derived using point-by-point numerical differentiation). Unlike in the experimental system, though, data points are taken even during the interpulse interval to allow full observation of time-dependent trends, but at a dramatically reduced frequency of 10 μs or more per data point. This reduction in the number of data points taken during the interpulse intervals results in a reduction in amount of data to be processed of over 90% for 1 kHz excitation while producing identical-looking plots.

Finally, probably the most important simulation parameters with regard to simulation time are the specification of the desired simulation accuracy. The user can tell SPICE how stringent the criteria for convergence should be, as well as which algorithms should be used for adjusting the size of the internal timestep between iterations, for instance. HSPICE provides an option, `accurate`, which automatically changes from the defaults both the criteria for convergence and the timestep algorithm. [28] Using this option results in more accurate results, but at a severe performance hit. One netlist, for example, simulated in under ten seconds using the default options, but took over ninety seconds using the `accurate` option. The option should only be used, then, if the increased accuracy is needed. In this study, Q-V, Q_{max}-V_{max}, and Q-F_p plots were generally not visibly altered either with or without

accurate specified, but obvious differences in C-V curves were apparent, as shown in Fig. 2.18. This is due to the capacitance values being calculated from the ratio of two derivatives – the derivative of the voltage across the ACTFEL device, and (basically) the derivative of the voltage across the sense capacitor in series with the device. (Remember that the external charge is simply the voltage across the sense capacitor multiplied by what are essentially constants.) One of the two convergence conditions in SPICE is that convergence has occurred when the node voltages of the circuit are within a tolerance specified by either a percentage (e.g. 0.1 percent) or an absolute voltage (e.g. 10 μV), whichever is larger. With the default settings, the two voltages – across the device and across the sense capacitor – apparently converge within the percentage-defined tolerance first, so that the two voltages vary from the previous timestep by the same, fixed percentage. This flaw is not apparent when the voltages are displayed as a Q-V plot, but is readily apparent as flat portions in the C-V plot. By increasing the accuracy of the simulation, the voltages are apparently forced to converge within the absolute limits, and no longer increase by the same percentage several timesteps in a row.

2.4.4.3 Data Extraction

One of the more tedious aspects of simulation is the extraction and presentation of large quantities of data from hundreds of simulation runs. Node voltages related by SPICE must be extracted from the simulation output file, which contains a lot of extraneous information about the simulation run. These voltages must be converted to useful quantities, such as charge per unit area, and finally, the quantities must be loaded into graphical display software for analysis.

Luckily, if HSPICE is used for simulation, a number of included features make the process easier. The algebraic parser built into HSPICE can perform the node voltage transformations internally, for instance, subtracting the two node voltages on either side of the sense capacitor, multiplying by the sense capacitor value, and

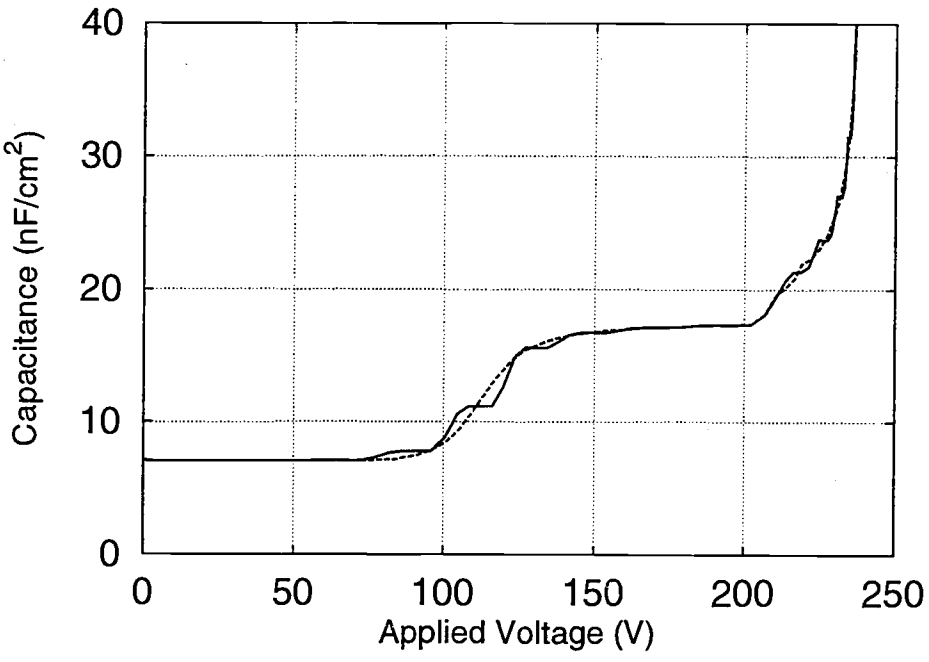

Figure 2.18: Simulated C-V curves using the default HSPICE options (solid line) and the `accurate` option (dashed line).

dividing by the device area so that the output is already in the desired units for external charge. Second, HSPICE provides a `.measure` statement which can be used to measure a variety of simulation output parameters at a certain time or frequency, for instance. In this work, the `.measure` statement is used to determine the maximum voltage on the sense capacitor and the corresponding maximum applied voltage during Q^e_{max}-V_{max} analysis. Unfortunately, as of this writing, HSPICE does not seem to allow algebraic quantities in the `.measure` statement, so that post-processing is still required for this type of measurement.

For any post-processing, such as stripping away extraneous information from the output file, external scripts written in PERL are generally used. This processing can be done in other languages, such as C, AWK, or even MATLAB scripting, but PERL is a scripting language specifically designed for data extraction and report formatting and is found to be both the easiest and best method, after using the other

listed approaches. Scripts are also useful for automating series of simulation experiments. For instance, a PERL script could run an experiment, extract the data of interest to a report file, change certain values in the SPICE input file, and then run another simulation. It is convenient to do Q^e_{max}-V_{max} analysis in this way. HSPICE too provides methods of varying (sweeping) certain circuit parameters, but by using external scripts, the user can change anything in the source file, including environmental parameters, in a completely arbitrary fashion – any number of parameters could be changed together, and not necessarily in a linear or logarithmic fashion. Also, controlling the series of simulation is more straight-forward and intuitive using external scripts, even when the variable sweeping is reasonable from within the HSPICE input file.

2.4.4.4 Parameter Optimization

After a computer model is mathematically specified, the problem remains of determining the best values to use for all of the input parameters. A number of approaches exist to solve this problem. First, many of the parameters are known at least approximately from physical knowledge or previous research; for instance, the device dimensions are known from the manufacturing specifications, and capture cross sections can be assumed within an order of magnitude depending on the charge relation between the trap and the carrier to be trapped.

Second, for simple models with limited parameter sets, a computer can be used to numerically find the parameter set which leads to the best fit to experimental data. For instance, HSPICE contains functionality to optimize a set of input variables to give the least-squares best fit to dc, ac, or transient data. The least-squares optimization of model parameters is used in Chapter 5 to determine the best-fit parameters for dc and steady-state transient OLED models. A least-squares model optimization for a device-physics based double-sheet charge ACTFEL model was developed by Bouchard. [8]

Third, model parameters can be adjusted manually. Typically, simulation parameters are varied with careful attention to the effects that the changes have on the model output, and the parameters thereby tuned to produce the desired results through repeated simulations. A more scientific approach to the problem of determining the best simulation parameters was undertaken by Grudzinsky, who used a design of experiments technique. [29] In this approach, a number of simulation outputs, such as the phosphor field at the maximum applied voltage, are measured for a number of simulations in which the input parameters are systematically varied. By inputting the results of each variation into a statistical mathematics computer program, the user is informed which input variables have the greatest effect on the output quantities. The generation of response surface plots within the software enables the user to determine the parameters which lead to the best fit to experimental data.

2.5 Summary

This chapter provides a review of ACTFEL technology necessary to develop the models presented in the next chapter. The ACTFEL device structure, simplified operation, and the electrical characterization of ACTFEL devices are discussed. Finally, issues pertaining to SPICE simulation of ACTFEL devices are considered, including an overview of previously developed SPICE models.

3. SIMULATING ACTFEL DEVICES IN SPICE

This chapter describes the SPICE simulation of ACTFEL devices using two approaches. First, the Fowler-Nordheim diode circuit element built into HSPICE is used to create an accurate model of ideal ACTFEL devices. Second, the use of voltage-controlled dependent current sources is demonstrated in constructing a more device-physics based model. This model is then expanded to include simulation of space charge distributed in one or two sheets of charge.

3.1 Fowler-Nordheim Diode Model

The circuit topology of the basic Fowler-Nordheim model is shown in Fig. 3.1. The two capacitors, C_{it} and C_{ib}, represent the capacitances of the top and bottom insulators, respectively, as in the previous SPICE-based models discussed in Sec. 2.4.3. In series with and sandwiched between these capacitors is a Fowler-Nordheim tunneling diode, which accounts for current transport across the phosphor. The 'phosphor resistance,' R_p, is added in parallel with the diode to account for leakage charge.

3.1.1 Derivation of Basic Model

The Fowler-Nordheim diode model is provided in HSPICE for modeling metal-insulator-semiconductor devices and consists of a voltage-dependent, non-linear current source in parallel with a fixed capacitance. The Fowler-Nordheim diode current-voltage characteristic is based on the equation for tunneling current through a triangular insulating barrier from a metal,

$$J_{FN} = \frac{q^2\mathcal{E}^2}{16\pi^2\frac{m^*}{m_0}\hbar\Phi_B}\exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{\frac{3}{2}}}{3q\hbar\mathcal{E}}\right], \tag{3.1}$$

where $\mathcal{E}$ is the electric field across the insulator, Φ_B is the metal-insulator barrier height in volts, and m^* is the effective mass of the tunneling carrier. [30, 31]

Since current injection in ACTFEL devices is usually thought of as the tunnel-emission of electrons from a discrete trap at the cathodic insulator-phosphor interface

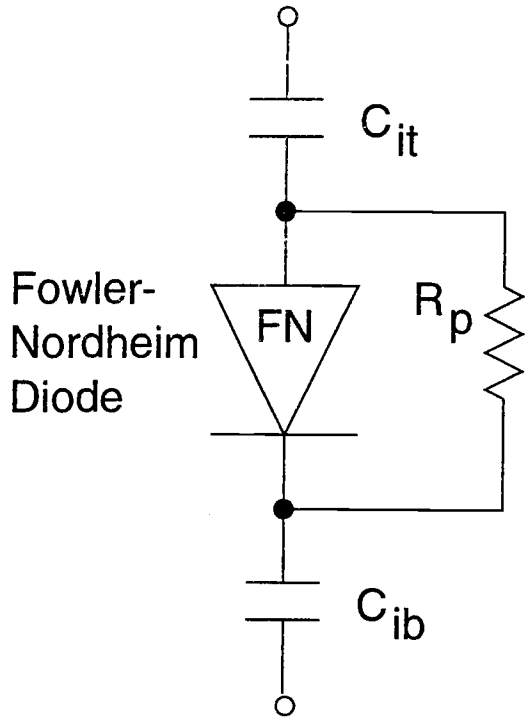

Figure 3.1: ACTFEL equivalent circuit using the SPICE Fowler-Nordheim diode model.

into the phosphor [16], the Fowler-Nordheim diode can be used to model this injection process in SPICE, if appropriate substitutions are made: the metal-insulator barrier height is replaced with the interfacial trap depth, the electric field across the insulator is replaced with the electric field across the phosphor, and the ZnS electron effective mass is used.

However, the Fowler-Nordheim HSPICE model characteristics are given in terms of lumped parameters useful for circuit engineering. In HSPICE, Eq. 3.1 appears as

$$i_d = A \cdot JF \cdot \left(\frac{v_d}{TOX}\right)^2 \exp\left[-\frac{EF \cdot TOX}{v_d}\right] \tag{3.2}$$

for forward applied biases, where A is the diode area, v_d is the voltage applied across the diode, TOX is the thickness of the 'oxide,' and JF and EF are lumped parameters called the forward current density and critical field, respectively. [28] Initial experimentation made it clear that using these built-in SPICE parameters to model

ACTFEL devices is unwieldy at best since the lumped parameters obscure the underlying physics. Therefore, it is necessary to relate the more familiar device physics quantities to the SPICE parameters using HSPICE's built-in algebraic features. To see how this is done, notice that Eqs. 3.1 and 3.2 are equivalent if

$$v_d = TOX \cdot \mathcal{E}, \tag{3.3}$$

$$EF = \frac{4\sqrt{2m^*}(q\Phi_B)^{\frac{3}{2}}}{3q\hbar}, \tag{3.4}$$

and

$$JF = \frac{q^2 m_0}{16\pi^2 m^* \hbar \Phi_B} \tag{3.5}$$

are chosen. Thus, the electron effective mass and interface trap depth are specified to characterize the model, and these values are translated to the necessary HSPICE parameters using equations following from Eqs. 3.3, 3.4, and 3.5 within the HSPICE input file. Analogous equations for the reverse-biased case (ER and JR) follow similarly.

Shunted across the voltage-controlled current source, the HSPICE Fowler-Nordheim model also includes a fixed capacitance whose value is

$$CD = \frac{\varepsilon_{OX}\varepsilon_0 A}{TOX}, \tag{3.6}$$

where ε_{OX} is the relative dielectric constant of silicon dioxide and ε_0 is the permittivity of free space. Unfortunately, the value of ε_{OX} is fixed in HSPICE and cannot be directly adjusted by the user to reflect materials other than silicon dioxide. [28, 32] However, a way to circumvent this limitation exists: the software interface adjusts the area parameter, A, so that the fixed capacitance is the same as it would be if ε_{OX} could be adjusted to the proper value:

$$A = \frac{A'\varepsilon'_{OX}\varepsilon_0}{\varepsilon_{OX}}, \tag{3.7}$$

where the primed values are the actual device values. Since A and JF both appear in Eq. 3.2 as proportionality constants, the effect this adjustment to the area has on

the current characteristics is offset by adjusting the JF parameter in the opposite direction:

$$JF = \frac{\varepsilon_{OX}}{\varepsilon'_{OX}\varepsilon_0} JF', \tag{3.8}$$

where JF' is the actual device value given by Eq. 3.5 and JF is the adjusted value. The current given by Eq. 3.2 thus remains unaffected by the change in area. An example HSPICE input file for this basic Fowler-Nordheim ACTFEL model is listed in Appendix A.

3.1.2 Specification of Model Parameters

Of the simulation parameters to be specified, most are known either from the literature and experimental circuit setup, or are determined from electrical characterization experiments or the processing parameters. The electron effective masses and the relative dielectric constants for a variety of phosphor materials have been reported in the literature. For ZnS, the electron effective mass has been reported to be 0.18 m_0 [33], and the relative dielectric constant is 8.3. Important experimental circuit parameters to be included are the series resistance of the test setup, the parasitic oscilloscope resistance, and the ITO series resistance. The device area is a known process parameter.

The remaining non-adjustable parameters can be determined in two ways. First, the thicknesses of the phosphor and insulator layers are approximately known process parameters. These values, together with the device area and the dielectric constants of each layer, can be used to determine the insulator and phosphor capacitance values. However, due to uncertainty in the thickness values, better fits to data result when the parameters are derived from characterization experiments. Typically, the total device capacitance is measured from the pre-turn-on slope of either a Q-V plot or the pre-threshold slope of a maximum charge versus maximum voltage (Q^e_{max}-V_{max}) plot, while the total insulator capacitance, $C_i = (C_{ib} \times C_{it})/(C_{ib} + C_{it})$, is measured from the post-turn-on slope of a Q-V or the post-threshold slope of a

Q^e_{max}-V_{max} plot at $40 - 60$ V over threshold. C_i can be attained this way provided no dynamic space charge exists, as is the case for evaporated ZnS:Mn devices. The phosphor thickness is determined using the measured phosphor capacitance value in conjunction with the phosphor dielectric constant and the insulator capacitance. The accuracy of the phosphor and insulator capacitances determined using either method is checked using the Q-F_p method: the Q-F_p plot of a ZnS:Mn device should be horizontal before turn-on during the rising portion of the waveform, and vertical after turn-on if the capacitance and thickness values are correct. [7]

This leaves only two simulation parameters that need to be adjusted in order to obtain a good fit to experimental data: the interface trap depth and the value of the phosphor shunt resistance.

The interface trap depth is first adjusted until good agreement is obtained between experimental and simulated Q-V curves for a particular maximum applied voltage. Once this interface trap depth is optimized, the experimental and simulated Q-V curves are very similar, except that there is no leakage in the simulated Q-V curve. To account for leakage charge in the simulated curve, the phosphor shunt resistance is reduced from infinity to some finite value. Since higher leakage results in a reduced polarization field at the beginning of the next pulse, the turn-on is shifted slightly toward higher voltages for small values of the phosphor resistance; therefore, the interface trap depth value may need to be readjusted slightly after the leakage is accounted for through the addition of the phosphor resistor.

3.1.3 Accounting for Coulombic Barrier Lowering

In the previous two subsections, the Fowler-Nordheim tunneling diode model provided in HSPICE is utilized to produce a simply-realized ACTFEL model which provides good accuracy for ideal ACTFEL devices but only requires a very limited parameter set. The model is limited in several respects, though. For instance, the model does not include Coulombic barrier lowering, an effect that results when the

tunneling probability is increased by a reduction in the potential barrier due to the electric field, so that Eq. 3.1 becomes [34]

$$J_{FN} = \frac{q^2\mathcal{E}^2}{16\pi^2\frac{m^*}{m_0}\hbar\Phi_B}\exp\left[\left(-\frac{4\sqrt{2m^*}(q\Phi_B)^{\frac{3}{2}}}{3q\hbar\mathcal{E}}\right)\left(1-\left(\frac{\Delta\Phi_B}{\Phi_B}\right)^{5/3}\right)\right] \tag{3.9}$$

where

$$\Delta\Phi_B = \left(\frac{q\mathcal{E}}{\pi\epsilon}\right)^{1/2} \tag{3.10}$$

and ϵ is the permittivity of the phosphor layer.

In order to implement Eq. 3.9 into the ACTFEL model, it is necessary to replace the built-in Fowler-Nordheim model with a user-defined model. This is most easily accomplished by defining a voltage-controlled current source defined by the current-voltage characteristic of Eq. 3.9 and replacing the Fowler-Nordheim diode in the netlist by a parallel combination of the newly-defined voltage-controlled current source and a fixed-value capacitor which corresponds to the phosphor capacitance.

3.2 Device Physics-Based Emission Model

Although the Fowler-Nordheim tunneling diode built-in to HSPICE is useful for simple modeling of the near-ideal evaporated ZnS:Mn system, it quickly becomes inadequate for applications in which more complex modeling is needed. Therefore, this section describes replacing the built-in model, as well as outlining the procedure for including thermally-activated emission and trap occupancy.

3.2.1 Reformulating the Tunneling Equation and Including the Thermal Emission Process

The tunneling characteristic used in the built-in HSPICE Fowler-Nordheim tunneling diode is unsuitable for more complex modeling which includes occupancy considerations or includes other emission processes other than tunneling. For these applications, it is useful to reformulate the tunneling equation used to better reflect the physics of ACTFEL operation while resulting in an expression in terms of the tunnel emission rate, rather than in terms of tunnel emission current.

The built-in Fowler-Nordheim model was provided specifically to model the tunnel-injection of electrons from a metal layer through an insulating layer of SiO_2. The pre-exponential factor in Eqs. 3.1 and 3.9, therefore, reflects tunneling from a continuous distribution of states in a metal, rather than from a discrete level with a limited occupation of carriers. When the prefactor is reformulated to reflect an emission rate (instead of a current) from a discrete Coulombic well, Eq. 3.9 becomes [34]

$$e_n^{PT} = \frac{q\mathcal{E}}{(32m^*q\Phi_B)^{1/2}} \exp\left[\left(-\frac{4\sqrt{2m^*}(q\Phi_B)^{\frac{3}{2}}}{3q\hbar\mathcal{E}}\right)\left(1-\left(\frac{\Delta\Phi_B}{\Phi_B}\right)^{5/3}\right)\right] \tag{3.11}$$

where e_n^{PT} indicates an electron emission rate due to pure tunneling and $\Delta\Phi_B$ is given by Eq. 3.10.

Instead of tunneling through the barrier, an electron may gain enough thermal energy to be thermally emitted over the barrier. This thermal emission rate is given by [34]

$$e_e^{thermal} = \sigma v_{th} N_c \exp\left[-\frac{\Phi_B - \Delta\Phi_B}{kT/q}\right], \tag{3.12}$$

where σ is the thermal emission cross section, v_{th} is the thermal velocity of the electron, N_c is the effective density of states, and kT/q is the thermal voltage (0.0259 V at room temperature).

These two emission processes sum to give the total emission rate from an interface:

$$e_n = e_n^{PT} + e_n^{thermal} \tag{3.13}$$

Except at very low fields, the pure tunneling component is expected to dominate the emission.

In device physics modeling, a third emission process, phonon-assisted tunneling, is often included in the model. Phonon-assisted tunneling can be visualized as a combination of thermionic emission and pure tunneling, in which an electron gains energy from the lattice before tunneling through the barrier from a higher energy state (where the barrier is thinner and the tunneling probability is therefore higher).

Like the previous two emission mechanisms, an analytic equation for the phonon-assisted tunneling rate has been reported. The emission rate due to phonon-assisted tunneling is given by [34]

$$e_n^{PAT} = e_n^{thermal} \int_{\frac{\Delta E_{it}}{kT}}^{\frac{E_{it}}{kT}} exp\left[z - z^{3/2}\left(\frac{4}{3}\frac{(2m^*)^{1/2}(kT)^{3/2}}{q\hbar f_p}\right)\left(1 - \left(\frac{\Delta E_{it}}{zkT}\right)^{5/3}\right)\right] dz. \tag{3.14}$$

This term, e_n^{PAT}, would be included in Eq. 3.13 to include injection by phonon-assisted tunneling. However, the integral in Eq. 3.14 makes inclusion of phonon-assisted tunneling in a SPICE model difficult (an external program to calculate the emission rate and the incorporation of a look-up table in the SPICE program would be required), so only pure tunneling and thermal emission are included in the SPICE model.

Note that Eq. 3.13 gives the emission rate at an interface, as opposed to the emission current as in Eq. 3.1. Since the emission rate has units of inverse time, the emission current density is given by

$$j_n(t) = qn_x(t)e_n(t), \tag{3.15}$$

where $n_x(t)$ denotes the number of electrons per area available at the interface of interest, x, at a given time, t.

3.2.2 Accounting for Occupancy

From Eq. 3.15 it is seen that the number of electrons per area available at the interface, $n_x(t)$, must be known to use the emission rate to find the emission current. We begin by noting that at zero-field conditions, a certain number per unit area of electrons will be trapped at the interface. This number is termed the no-field occupancy, $N_0 f_0$, for the interfaces. As the device is operated with the interface acting as the cathode, the number of the electrons at the interface will decrease as emission occurs. During opposite-polarity pulses, the interface acts as the anode and the number of electrons present will increase as more electrons are trapped. Thus,

the number of electrons per area present at interface x is the sum of the electrons present under zero-field conditions minus the number which have been emitted:

$$n_x(t) = N_0 f_0^x - q_x(t)/(-q), \tag{3.16}$$

where q_x is the amount of emitted charge per area for interface x and $-q$ is the charge of an electron. (A positive value of q_x therefore corresponds to excess trapped electrons.) q_x can be found by applying Gauß' Law to the interface. Consider the device structure shown in Fig. 3.2. Gauß' Law gives

$$-q_{ib}(t) = C_{ib} v_{ib}(t) - C_p v_p(t) \tag{3.17}$$

and

$$-q_{it}(t) = C_p v_p(t) - C_{it} v_{it}(t), \tag{3.18}$$

where the C's refer to the normalized capacitances of each layer and the v's refer to the voltage dropped across the layer. These equations are then inserted into Eq. 3.16 to give $n_{ib}(t)$ and $n_{it}(t)$.

Finally, it is assumed that all electrons which are emitted by the cathode traverse the phosphor layer and are retrapped at the anodic phosphor-insulator interface.

3.3 Single-Sheet Charge Model

As mentioned in Section 2.4.2, one approach to SPICE modeling is to first develop a device physics-based model, and then to map the device physics equations into corresponding dependent current sources in the SPICE model. This approach was pursued by Keir in mapping his device physics-based single-sheet charge model into SPICE. [4, 5] In this section, the mapping methodology is demonstrated on the simple single-sheet charge model as a prelude to mapping a double-sheet charge model in the next section.

In constructing a SPICE model of this type, it is useful to refer to an energy band diagram of the ACTFEL device under forward bias which shows the physical

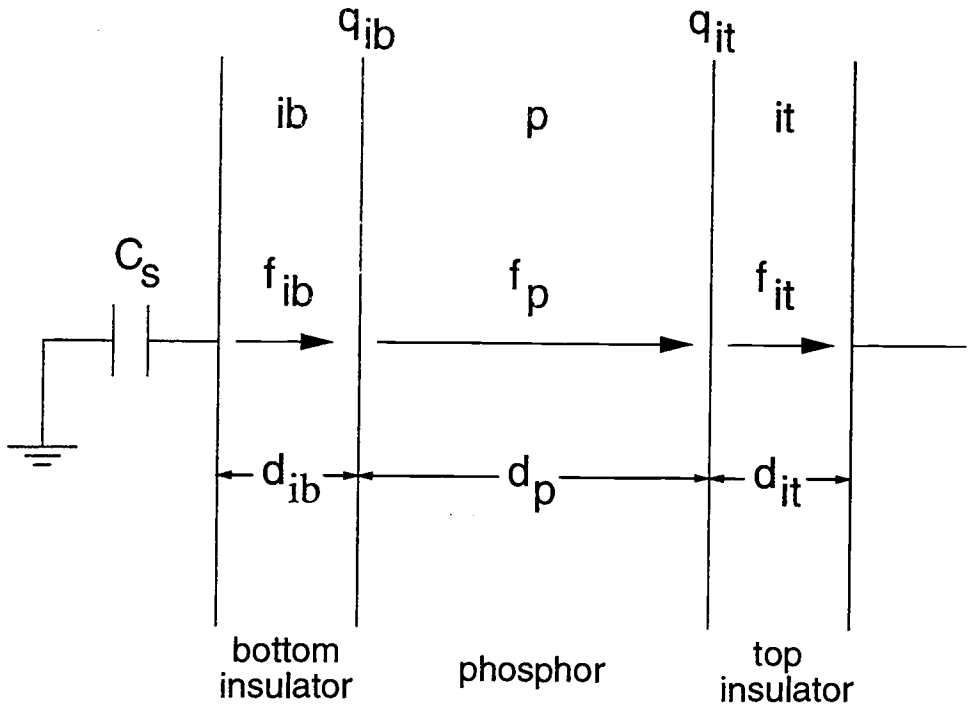

Figure 3.2: Sideview of an ACTFEL device for a simple model without space charge.

processes occurring within the device, such as Fig. 3.3. Figure 3.3 shows two processes occurring which need to be included in the model: electron emission, both from the cathodic phosphor-insulator interface and from the sheet of charge; and electron recapture at the sheet of charge and the opposite interface. (A third process, electron transport, is also shown in Fig. 3.3, but is assumed to occur instantaneously across the phosphor layer and therefore does not need special treatment in the model.)

The first process to be modeled, electron emission, occurs according to Eq. 3.13, where the sheet of charge is simply treated as a third interface located within the phosphor region. The emission current associated with each of these 'interfaces' is given by Eq. 3.15. These emission currents are dependent upon the occupancy of the trap from which electrons are being emitted, $n_x(t)$. This term is determined as follows. First, Fig. 3.4 shows a revision of Fig. 3.2 in which the phosphor layer of the ACTFEL device has been split into two regions, separated by a single sheet of

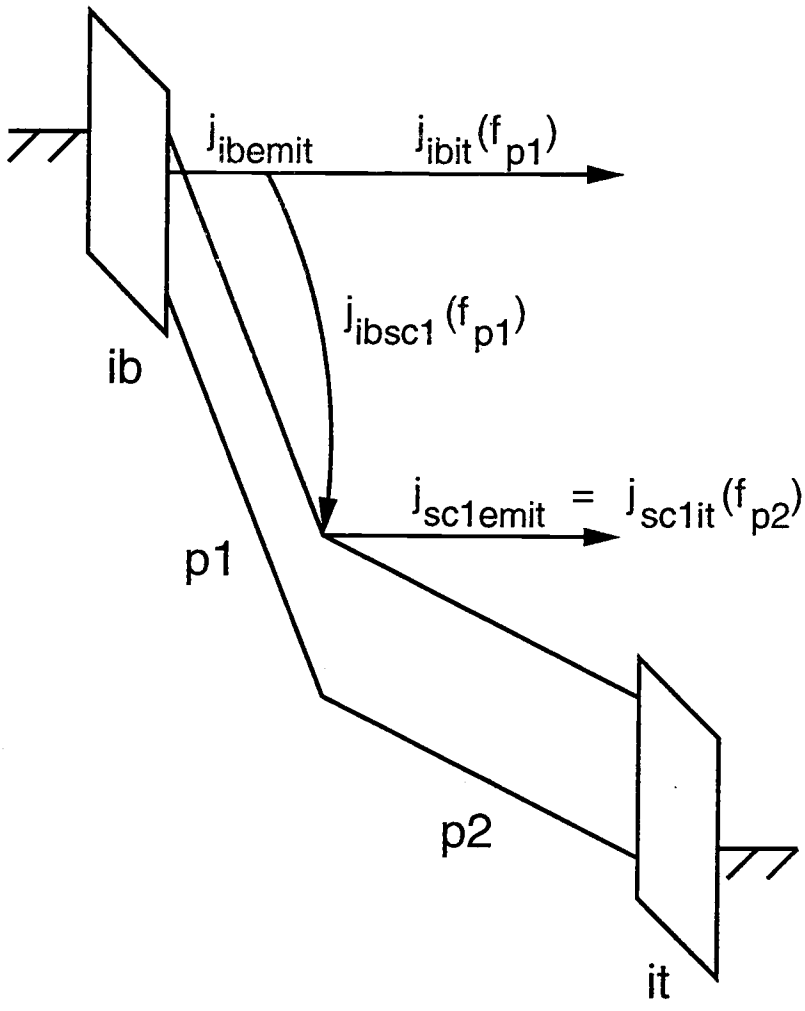

Figure 3.3: Energy band diagram representation of the conduction and space charge currents for an ACTFEL device in which space charge creation is limited to one discrete sheet in the phosphor bulk.

charge, q_{sc1}. The bottom portion of the phosphor has thickness d_{p1} and associated electric field f_{p1}; the corresponding terms for the top portion of the phosphor are d_{p2} and f_{p2}. Eqs. 3.17 and 3.18 become

$$-q_{ib}(t) = C_{ib}v_{ib}(t) - C_{p1}v_{p1}(t) \tag{3.19}$$

and

$$-q_{it}(t) = C_{p2}v_{p2}(t) - C_{it}v_{it}(t), \tag{3.20}$$

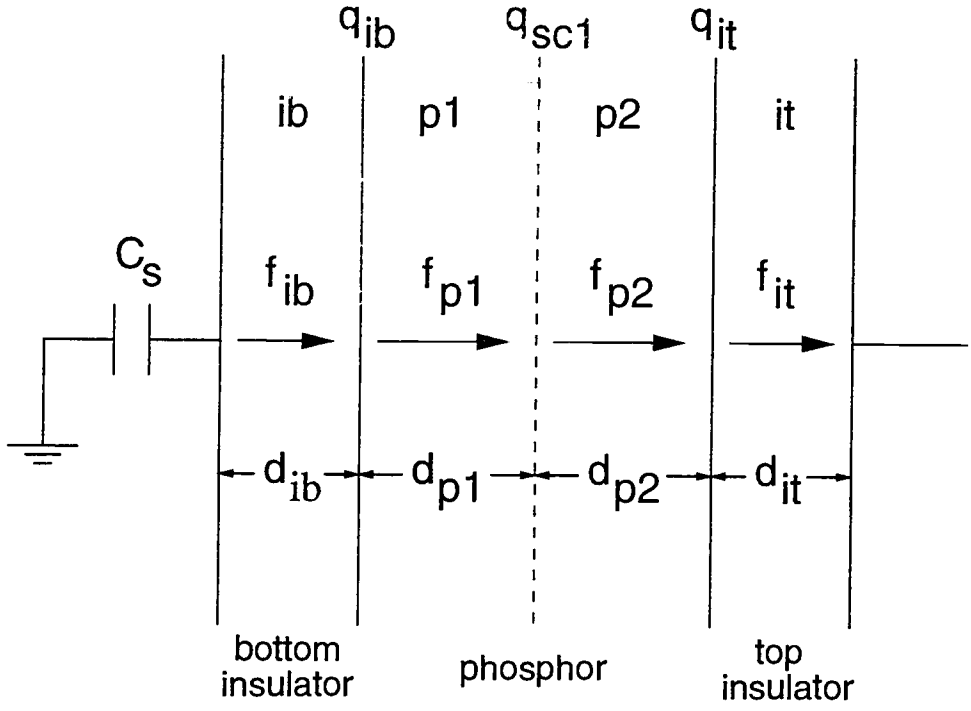

Figure 3.4: Sideview of an ACTFEL device, showing the space charge distribution modeled as one sheet of charge, q_{scl}.

and the amount of charge which has been emitted per area from the sheet of charge is, similarly,

$$-q_{scl}(t) = C_{p1}v_{p1}(t) - C_{p2}v_{p2}(t). \tag{3.21}$$

As in the model without space charge, these equations are inserted into Eq. 3.16 to give $n_{ib}(t)$, $n_{scl}(t)$, and $n_{it}(t)$.

As before, any electron which reaches the anodic phosphor-insulator interface is retrapped there, but now there is a non-zero probability that an electron which is emitted from the cathode will not traverse the entire phosphor, but be trapped first at the sheet of charge. This probability is termed the space charge capture factor for trap x, $sccf_x$, and varies between 0 and 1. Several possibilities for the formulation of $sccf_x$ are possible. The simplest is to simply assign a constant value, which can be fit to experimental data. However, electron capture is affected by two conditions. The

first of these is the electric field strength at the trap: capture is much more likely for a trap in a low field than for one in a high field. One formulation used by Bouchard *et al.* assumed the capture probability varied linearly with field, as in

$$sccf_x(f_p) \propto \left(1 - \left|\frac{f_p}{f_{0c}}\right|\right), \tag{3.22}$$

where f_{0c} is the critical field above which capture is not allowed, and f_p is taken as the average of the two phosphor fields existing on either side of the sheet of charge. [8] The second condition affecting electron capture at a bulk trap is the occupancy of the trap. Logically, the probability of capture should increase as the proportion of unfilled to filled traps increases. Additionally, device physics-based space charge modeling efforts typically assume the space charge is positive and preclude the possibility of negative space charge; as a consequence of this, the bulk traps cannot hold more electrons than in the no-field situation. Bouchard *et al.* account for both aspects of this second condition by multiplying Eq. 3.22 by an additional term, so that

$$sccf_x(f_p) = \left(1 - \frac{n_x}{N_t}\right)\left(1 - \left|\frac{f_p}{f_{0c}}\right|\right), \tag{3.23}$$

where n_x is given by Eq. 3.16 and Eqs. 3.19-3.21. As seen later, the number of electrons emitted from the trap relative to the total number available is quite small, so that the first term of Eq. 3.23, $(1 - n_x/N_t)$, approaches zero and thus forces the total capture factor towards zero. To counteract this effect, Eq. 3.23 is modified to

$$sccf_x(f_p) = \left[1 - \left(\frac{n_x}{N_t}\right)^y\right]\left(1 - \left|\frac{f_p}{f_{0c}}\right|\right). \tag{3.24}$$

If y is specified large enough, the main effect of the first term of Eq. 3.24 is to limit the occupancy of the trap to N_t but otherwise does not significantly affect the value of $sccf_x$. For small values of y, the occupancy of the trap becomes more important, but the overall value of $sccf_x$ is likely to be quite small and the trap will never be completely refilled. The latter results in an amount of positive space charge which is present during the entire applied voltage waveform; this could therefore be used to simulate static space charge.

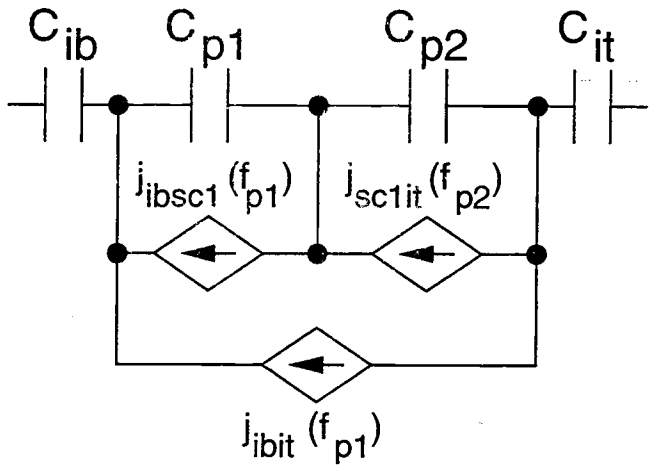

Figure 3.5: Equivalent circuit model for the one-sheet charge model under forward bias, in which the two emission and one space charge capture currents shown in Fig. 3.3 are represented by three voltage-controlled dependent current sources.

Now that the treatment of both emission and electron recapture has been described, the mapping of these processes into a SPICE model can proceed. Again referring to Fig. 3.3, notice that the ACTFEL device is divided into four regions: two insulators, and two segments of phosphors separated by the sheet of charge. These regions are first mapped as the four capacitors shown in Fig. 3.5, whose capacitance values are simply determined from the device area, the dielectric constants of the phosphor and insulator materials, and the thickness of each region. Next, each electron flux shown in Fig. 3.3 is mapped to the correspondingly-named dependent current source in Fig. 3.5, noting that the polarity of the current sources is opposite to that of the electron flux. Next, the mathematical characteristics of each current source are defined. The total electron emission current from the interface and each sheet of charge is given by Eq. 3.15 with the appropriate occupancy and field terms substituted in. Some portion of the electrons originating at the interface is trapped within the bulk and does not reach the anodic interface; the trapped electrons need to be subtracted out of each emission current. Referring to Fig. 3.3, the emission current from the cathodic interface given by Eq. 3.15 is denoted as J_{ibemit}. However,

$(sccf_1 \times 100)$ % of the emitted electrons are trapped at the first sheet of charge, leaving only $[(1 - sccf_1) \times 100]$ % of the electrons free to finish traversing the phosphor to the anodic interface. The current to the trap at sc_1 is thus

$$j_{ibsc1} = j_{ibemit}(f_{p1}) \cdot sccf_1, \tag{3.25}$$

and the current due to electrons traveling from the cathodic interface to the anodic interface is

$$j_{ibit} = j_{ibemit}(f_{p1}) \cdot (1 - sccf_1). \tag{3.26}$$

Finally, since none of the electrons emitted from $sc1$ are trapped before they reach the anode,

$$j_{sc1it} = j_{sc1emit}(f_{p2}). \tag{3.27}$$

The mapping process is repeated for the negative polarity of the applied voltage pulse to complete the model. Note that each applied voltage pulse polarity requires the use of three voltage-dependent current sources so that a total of six are required in the final single-sheet charge model.

3.4 Double-Sheet Charge Model

The construction of a two-sheet charge SPICE model proceeds analogously to the mapping of the single-sheet charge model described in the preceding section, so only a summary of the results are given here. For a separate derivation of the double-sheet charge SPICE model, the reader is directed to Ref. [35]. Derivations of the double-sheet charge device-physics ACTFEL model including quasi-statics and dynamics are provided by Keir [5] and Bouchard [8].

Figure 3.6 shows an energy band diagram representation of a forward-biased ACTFEL device where the space charge is assumed to be localized at two locations within the phosphor layer. As in the earlier models, each of the electron injection

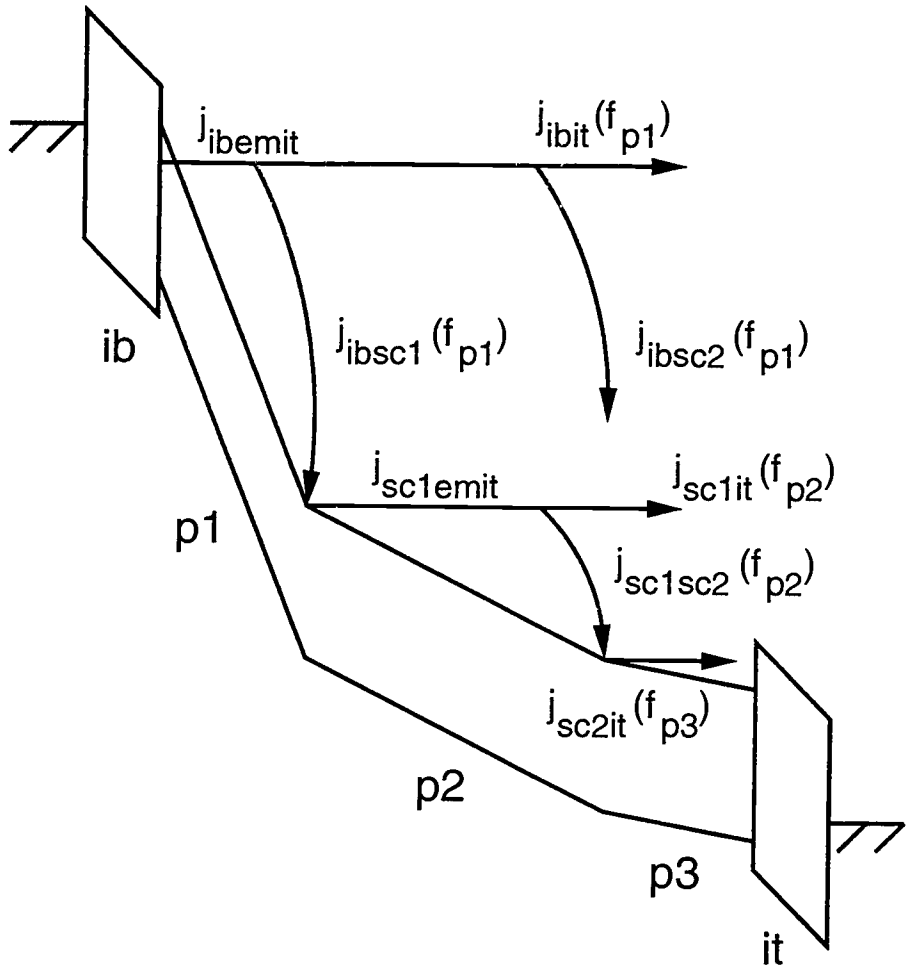

Figure 3.6: Energy band diagram representation of the conduction and space charge currents for an ACTFEL device in which space charge creation is limited to two discrete sheets in the phosphor bulk.

processes is assumed to occur via pure tunneling or thermal emission as governed by Eqs. 3.11-3.13, and the emission current is given by Eq. 3.15.

With the addition of a second sheet of charge, q_{sc2} the ACTFEL device is now represented as in Fig. 3.7. Eqs. 3.19 and 3.21 remain valid for the double-sheet charge model, but Eq. 3.20 is modified to

$$-q_{it}(t) = C_{p2}v_{p2}(t) - C_{it}v_{it}(t), \tag{3.28}$$

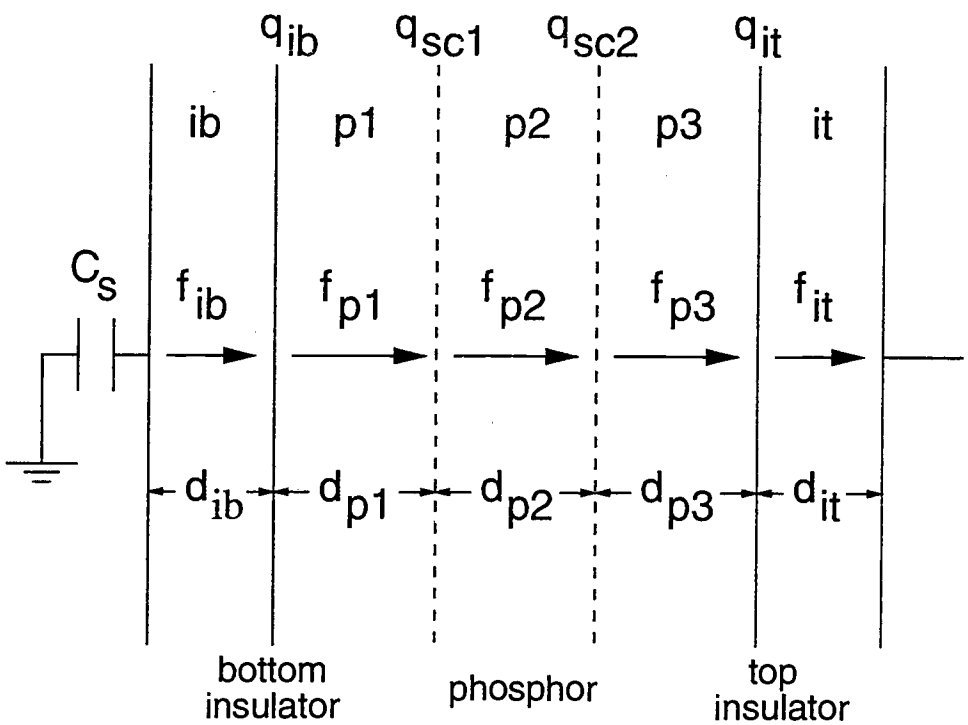

Figure 3.7: Sideview of an ACTFEL device, showing the space charge distribution modeled as two sheets of charge, q_{sc1} and q_{sc2}.

and the amount of charge which has been emitted per area from the second sheet of charge is

$$-q_{sc2}(t) = C_{p2}v_{p2}(t) - C_{p3}v_{p3}(t). \tag{3.29}$$

As before, these equations are inserted into Eq. 3.16 to give $n_{ib}(t)$, $n_{sc1}(t)$, $n_{sc2}(t)$, and $n_{it}(t)$.

The processes shown in Fig. 3.6 are mapped into a SPICE model for a forward-biased ACTFEL device as in the single-sheet case, resulting in the equivalent circuit

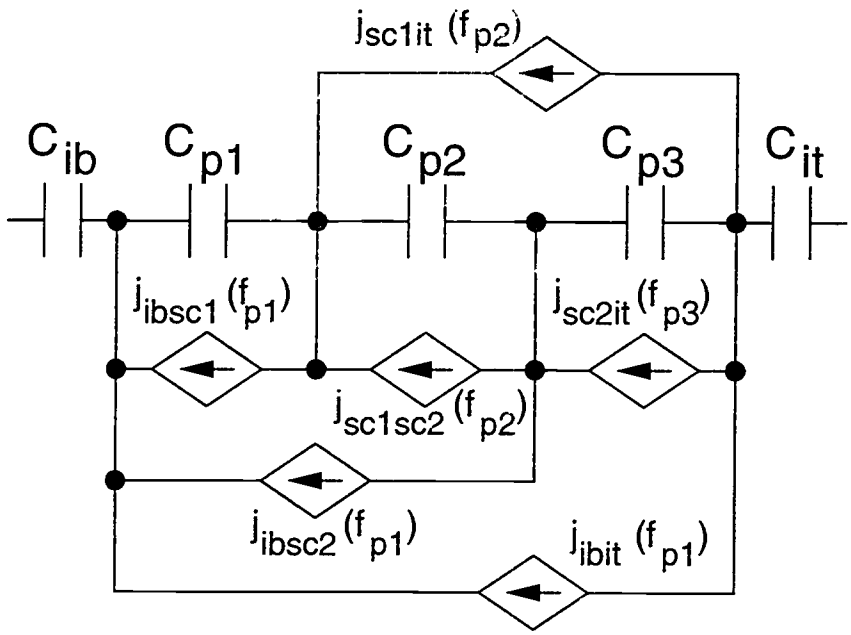

Figure 3.8: Equivalent circuit model for the two-sheet charge model under forward bias, in which the three emission and three space charge capture currents shown in Fig. 3.6 are represented by six voltage-controlled dependent current sources.

shown in Fig. 3.8. Subtracting out the trapped electrons, it can be shown that

$$j_{ibsc1} = j_{ibemit}(f_{p1}) \cdot sccf_1, \tag{3.30}$$

$$j_{ibsc2} = j_{ibemit}(f_{p1}) \cdot (1 - sccf_1) \cdot sccf_2, \tag{3.31}$$

$$j_{ibit} = j_{ibemit}(f_{p1}) \cdot (1 - sccf_1) \cdot (1 - sccf_2), \tag{3.32}$$

$$j_{sc1sc2} = j_{sc1emit}(f_{p2}) \cdot sccf_2, \tag{3.33}$$

and

$$j_{sc1it} = j_{sc1emit}(f_{p2}) \cdot (1 - sccf_2). \tag{3.34}$$

Finally, the mapping process is repeated for the negative polarity of the applied voltage pulse to complete the model. Note that each applied voltage pulse polarity requires the use of six voltage-dependent current sources so that a total of twelve are required in the final model. An example HSPICE input file for this double-sheet

charge ACTFEL SPICE model with space charge creation via field emission is listed in Appendix B.

3.5 Space Charge via Trap-to-band Impact Ionization

So far, space charge creation in the phosphor region has been via field emission. This section discusses altering the double-sheet charge model so that space charge is created instead by trap-to-band impact ionization.

As discussed in Section 2.2.2, trap-to-band impact ionization occurs when an electron gains enough energy from the field that, on colliding with a trap in the phosphor, it removes an electron from the trap, resulting in a second conduction band electron, and leaving a positive charge at the trap. (These traps could be an intentional or unintentional impurity in the lattice, or a defect. For ZnS for instance, it is thought that Zn vacancies or vacancy complexes could be at issue.) Thus, the trap-to-band impact ionization process results in electron multiplication across the phosphor. The total number of multiplied electrons which ultimately result from an electron emitted from the interface is dependent on the distance that it travels and on the field strength over that distance. We should expect a large number of multiplied electrons per unit length in high field regions, such as near the cathode during an applied voltage pulse, and a smaller amount of multiplication per unit length in lower field regions, such as exists near the anode.

In the double-sheet charge model, this multiplication and the concomitant positive space charge creation is of course restricted to the locations of the two sheets of charge. Thus, during a positive applied pulse, all of the multiplied electrons which are created in the region between the cathodic interface and the first sheet of charge are emitted from the first sheet of charge in the model, and the resultant positive charge is placed at the sheet. Similarly, all of the multiplied electrons created between the second sheet of charge and the anode are emitted from the second charge sheet. In the model, half of the multiplied electrons in the region between the two sheets are

assigned to each sheet of charge. The total multiplication of carriers seen at sheets 1 and 2 is denoted mf_1 and mf_2, respectively, and can be shown to be [8]

$$mf_1(f_{p1}, f_{p2}) = \exp\left[\alpha(f_{p1})d_{p1} + \alpha(f_{p2})d_{p2}/2\right] \tag{3.35}$$

and

$$mf_2(f_{p2}, f_{p3}) = \exp\left[\alpha(f_{p3})d_{p3} + \alpha(f_{p2})d_{p2}/2\right]. \tag{3.36}$$

These multiplication factors are to be understood as follows: for every n electrons which pass by the sheet of charge, $n{\cdot}(mf-1)$ electrons are emitted from the sheet, so that the total current seen is multiplied by a factor of mf.

With this in mind, the current-voltage equations which govern the voltage-controlled current sources in Fig. 3.8 can be written for trap-to-band impact ionization. Proceeding similarly to how Eqs. 3.25–3.27 were derived, it can be shown that

$$j_{ibit} = j_{ibemit}(f_{p1}){\cdot}(1-sccf_1){\cdot}(1-sccf_2), \tag{3.37}$$

$$j_{ibsc1} = j_{ibemit}(f_{p1}){\cdot}sccf_1, \tag{3.38}$$

$$j_{ibsc2} = j_{ibemit}(f_{p1}){\cdot}(1-sccf_1){\cdot}sccf_2, \tag{3.39}$$

$$j_{sc1sc2} = (mf_1-1){\cdot}(1-sccf_1){\cdot}j_{ibemit}(f_{p1}){\cdot}sccf_2, \tag{3.40}$$

$$j_{sc1it} = (mf_1-1){\cdot}(1-sccf_1){\cdot}j_{ibemit}(f_{p1}){\cdot}(1-sccf_2), \tag{3.41}$$

and

$$j_{sc2it} = (mf_2-1){\cdot}(1-sccf_2){\cdot}\left[j_{ibemit}(f_{p1}){\cdot}(1-sccf_1){\cdot}mf_1\right]. \tag{3.42}$$

The analogs of these equations for the negative applied voltage pulse are easily derived in a similar manner. Notice that the difference between Eqs. 3.37–3.42 and Eqs. 3.32–3.27 is that each $j_{scxemit}$ term has been replaced by a j_{ibemit} term which has been modified to take into account the multiplication and trapping prior to the sheet in

question; for instance, $j_{sclemit} = (mf_1 - 1)\cdot(1 - sccf_1)\cdot j_{ibemit}$ is inserted into Eq. 3.33 to yield Eq. 3.40.

We now need to know exactly what the mf_x function is, meaning a determination of $\alpha(f)$ is needed. The ionization function used in this thesis is repeated from Bringuier [36] and is given by

$$\alpha(f) = (qf/E_i)\exp[-(f_0/f)^n] \quad n = 1 \text{ or } 2, \tag{3.43}$$

where E_i is the effective ionization energy of the deep-level trap and f_0 is the characteristic field, or the field at which trap-to-band impact ionization becomes significant. This function is actually combined with a term which accounts for the reduction in ionization as traps in the phosphor become emptied, as in

$$\alpha(f) = \left(1 - \frac{n_{empty}}{N_t}\right)(qf/E_i)\exp[-(f_0/f)^n] \quad n = 1 \text{ or } 2, \tag{3.44}$$

where N_t is the concentration of deep level traps at each sheet of charge, and n_{empty} is the number of those traps which have been ionized. This acts as a negative feedback mechanism, helping ensure that the electron multiplication turns itself off as the available traps are emptied. Note that N_t is derived from the (uniform) concentration of traps located throughout the phosphor layer; one-half of these traps are assigned to each charge sheet, giving N_t in terms of traps per area. If a three-sheet charge model were created, one-third of the total number of traps in the phosphor layer would be assigned to each sheet, and so forth. With Eq. 3.44 inserted into Eqs. 3.35 and 3.36, the model for the positive applied voltage polarity is completed. To reiterate for the sake of clarity, in including the electron multiplication in the double-sheet charge model, only the equations governing the emission of charge from the sheets need be changed from the field emission model; the interface emission and space charge capture factor equations remain unchanged (although the parameters inserted in these equations to characterize the model may be different).

3.6 Summary

Several ACTFEL SPICE models of varying complexity are developed and described in this chapter. First, it is shown how the built-in Fowler-Nordheim diode can be used to model ACTFEL devices. Second, a device physics-based model is implemented in SPICE. Then, this model is expanded to include space charge creation via field emission from one or two discrete sheets of charge. Finally, the double-sheet charge model is modified to include space charge creation via electron multiplication due to trap-to-band impact ionization rather than by field emission.

4. ACTFEL SIMULATION RESULTS

Simulation results using the models described in Chapter 3 are presented. First, results from a simple model based on the Fowler-Nordheim tunneling diode are described. Then, the device physics-based emission model results are examined. Next, the single- and double-sheet charge models show the results of considering space charge creation in the ACTFEL device.

4.1 Fowler-Nordheim Diode Model

4.1.1 Results of Base Model

The accuracy of the Fowler-Nordheim diode model for a particular applied voltage is demonstrated in Fig. 4.1, which shows a Q-V curve of a 650 nm thick evaporated ZnS:Mn ACTFEL device driven 40 V over threshold. The values of the interface trap depth and phosphor resistance used in the simulation are $\Phi_B = 1.03$ eV and $R_p = 0.65$ MΩ, respectively. The experimental curve and the simulated curve are seen to be very nearly coincident, with the only notable difference occurring during the negative portion of the plot. Due to amplifier and ACTFEL stack asymmetries, the experimental C-V curve is not perfectly symmetrical with respect to the driving voltage polarity; for instance, in Fig. 4.1, the experimentally driven device is seen to have experienced a slightly higher voltage magnitude during the positive portion of the driving waveform than during the negative. In this study, the model parameters have been optimized with respect to the positive polarity, resulting in a slightly better correlation to the data from the positive half of the applied voltage waveform.

Figures 4.2 and 4.3 show the Q-F_p and C-V plots, respectively, which correspond to the Q-V plots in Fig. 4.1. The Q-F_p comparison between measured and simulated data shows that the model correctly accounts for the steady-state field and charge transfer in the ACTFEL device, whereas the C-V plots show the accuracy of

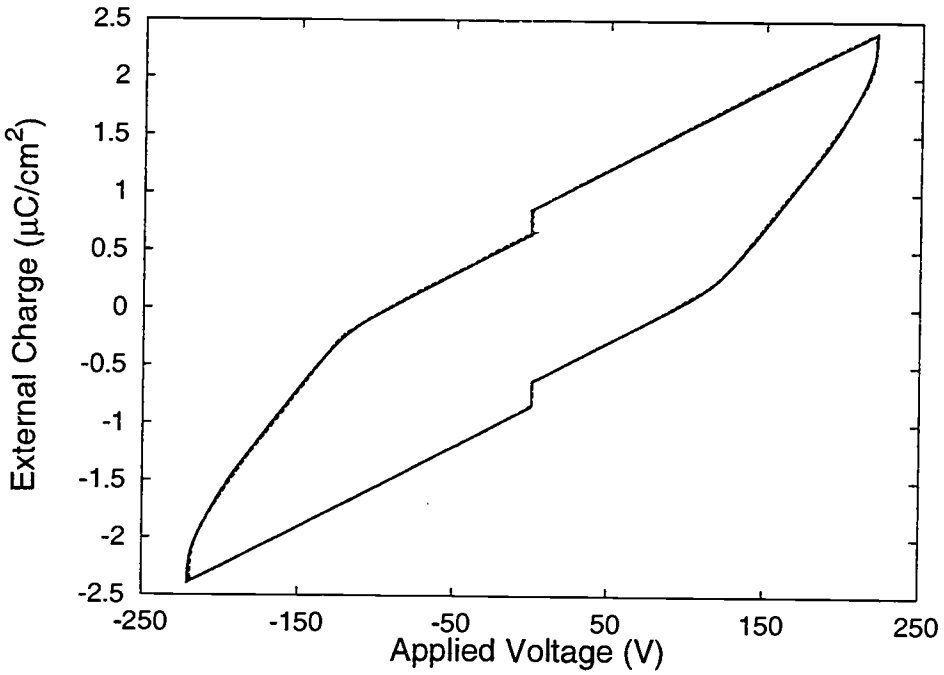

Figure 4.1: Q-V plot showing simulated (solid line) and measured (dashed line) data. The device is driven 40 V over threshold at 1000 Hz.

the simulated turn-on voltage. Achieving a close fit for both the turn-on voltage and the conduction charge magnitude is fairly sensitive to model parameters; a good fit to one or the other is possible using a wide range of parameter values, but obtaining good fits to both simultaneously is more restrictive of the parameter set. For the model parameters shown in this section, a good fit to all data features is achieved, but the parameters were optimized with a preference to accurate transferred charge fits over more accurate turn-on voltage fits for several reasons. Mainly, a utility feature of this model is likely to be the prediction of ACTFEL power consumption, which is given by the area enclosed by a Q-V plot. Therefore, to better match the Q-V areas between simulation and measurement, the accuracy of the maximum transferred charge is expected to be somewhat more important than the accuracy of the turn-on fit.

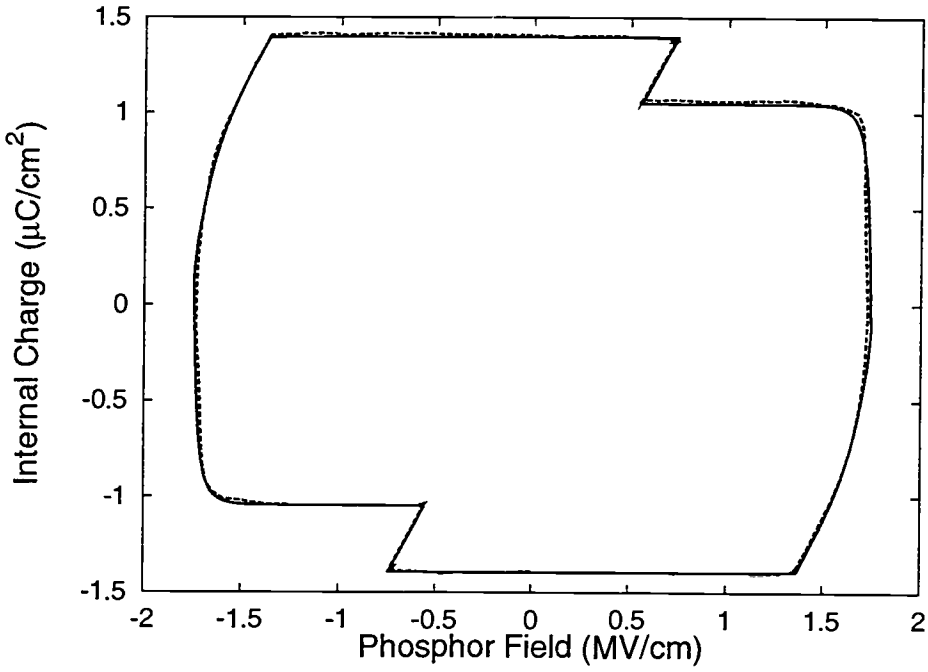

Figure 4.2: Q-F_p plot showing simulated (solid line) and measured (dashed line) data. The device is driven 40 V over threshold at 1000 Hz.

Since the standard electrical measurements are parametric plots which do not explicitly reveal the transient dynamic response, it is conceivable that a model with excellent Q-V agreement with measured data could nonetheless have poor agreement in the time domain. Simulated and measured transient charge [Q(t)] plots in Fig. 4.4 show that this is not the case for the model under consideration. The main weakness of the model is made more apparent in Fig. 4.4, however: the model turn-on is slightly more sluggish than in an actual device, and this sluggishness must be compensated by a slightly more aggressive sourcing of charge during the plateau portion of the driving voltage pulse in order to have transferred as much charge as a physical device by the end of the pulse. Secondly, the model is seen to exhibit less rounding in the Q(t) curve near the end of the fall portion of the pulse; this may simply be due to an RC effect of the experimental setup not accounted for in the model.

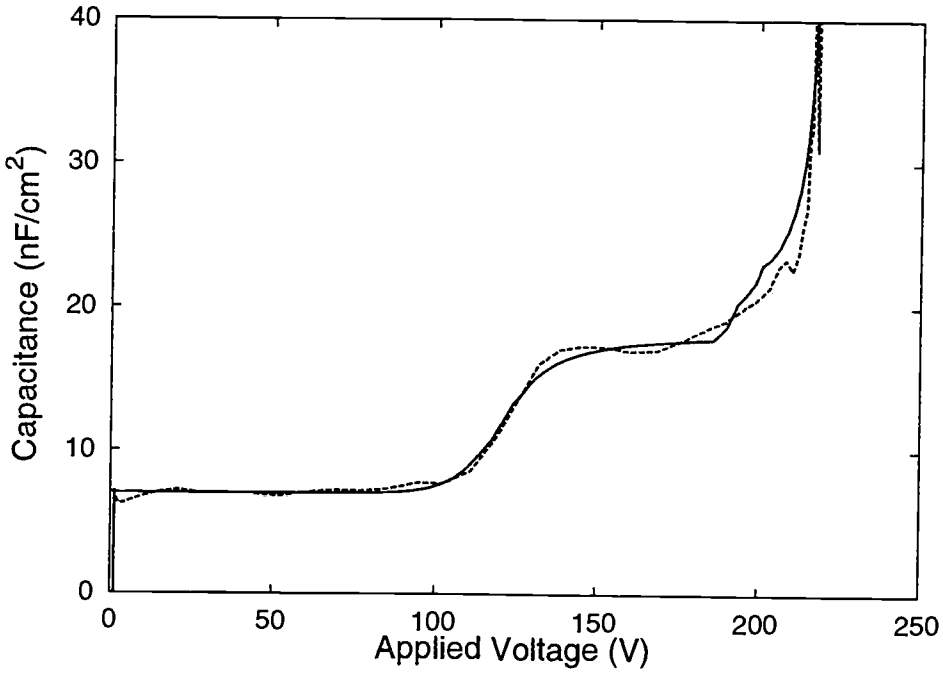

Figure 4.3: C-V plot showing simulated (solid line) and measured (dashed line) data. The device is driven 40 V over threshold at 1000 Hz.

4.1.2 Effects of Model Parameters

In order to efficiently optimize model parameters or expand the model, it is necessary to understand the effects individual parameters have on the model characteristics. Therefore, composites of Q-F_p and C-V plots simulated with varied model parameters are presented.

The two most important adjustable parameters are the relative effective mass m^* and the interface trap depth Φ_B. Figs. 4.5 and 4.6 demonstrate the trends due to these parameters. In either case, an increase in the parameter value results in a decrease of transferred charge, an increase in the steady-state field, and an increase of the turn-on voltage. That the trap depth and effective mass values should have such similar effects on the model performance is clear from Eq. 3.1, where m^* and Φ_B appear together in both the prefix and the exponential term. The additional factor of Φ_B in the exponential term makes it somewhat dominate over the effective mass

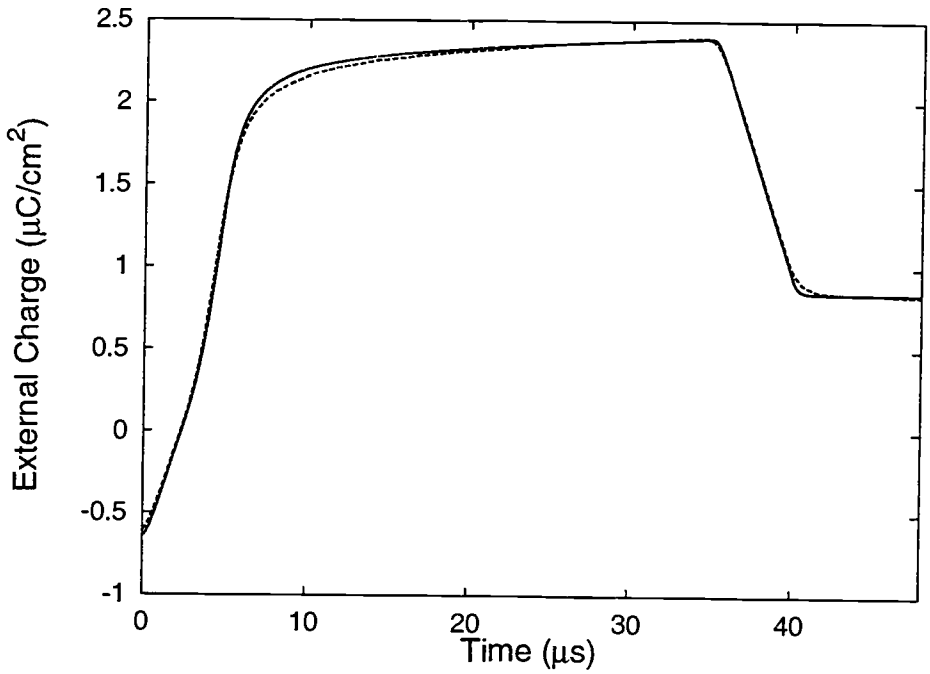

Figure 4.4: External charge vs. time plot showing simulated (solid line) and measured (dashed line) data. The device is driven 40 V over threshold at 1000 Hz.

term, so that the variation of electrical characteristics is larger in Fig. 4.6 than in Fig. 4.5 even though Φ_B is varied over a smaller range than m^*.

Fig. 4.7 shows the dependence of model parameters on the measurement circuit, namely the value of the series resistance R_s. Notice that with $R_s = 0\ \Omega$, the increase in capacitance near the maximum applied voltage, discussed in Sec. 2.3.3, does not occur. The corresponding Q-F_p plot also exhibits less rounding near points C and H than is seen experimentally. On the other hand, for large series resistance values, the Q-F_p plot is increasingly distorted and the C-V curve becomes more difficult to interpret. These plots show the importance of including the series resistance in ACTFEL simulations.

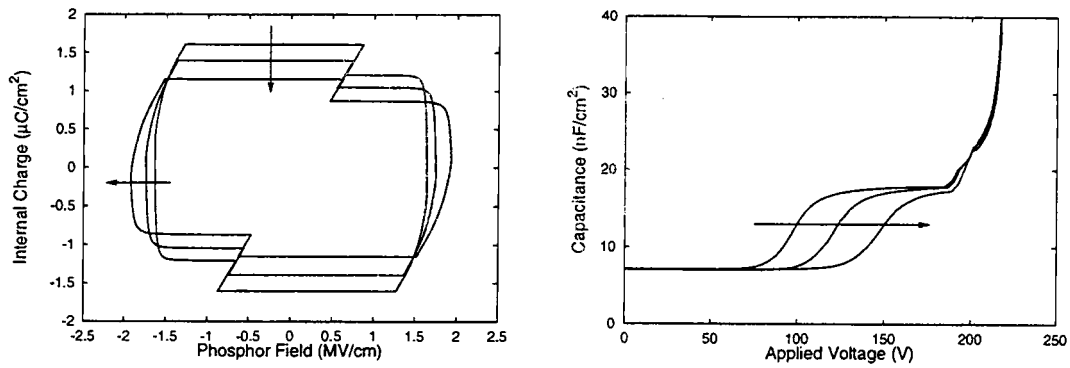

Figure 4.5: Q-F_p and C-V plots with relative effective mass $m^* = 0.15$, 0.18, and 0.21. Arrows indicate increasing m^*.

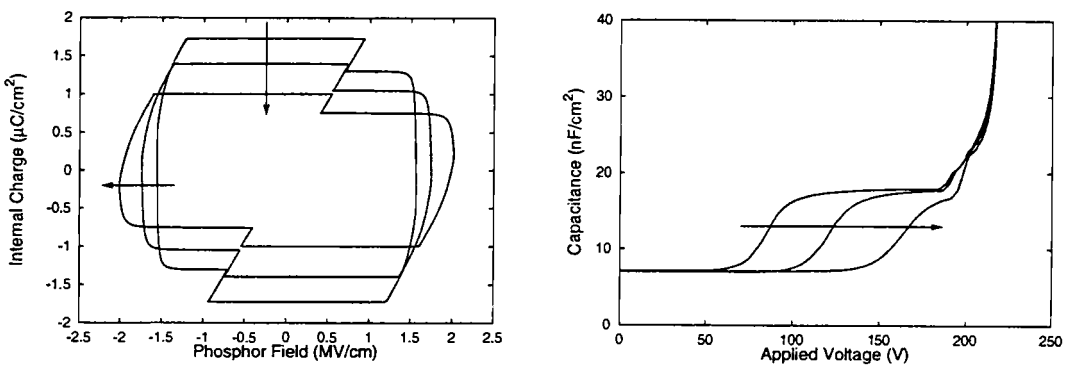

Figure 4.6: Q-F_p and C-V plots with trap depth $\Phi_B = 0.95, 1.05$, and 1.15 eV. Arrows indicate increasing Φ_B.

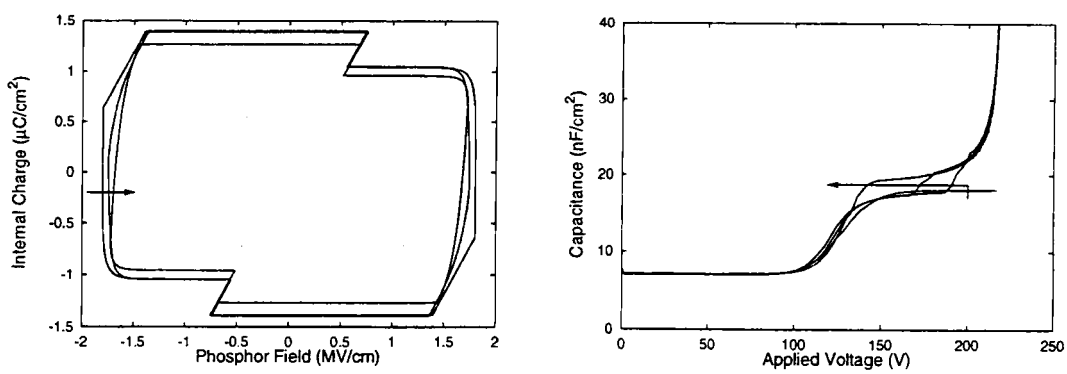

Figure 4.7: Q-F_p plots with series resistance $R_s = 0, 500$, and 3000 Ω and C-V plots with $R_s = 0, 500, 1000$, and 3000 Ω. Arrows indicate increasing R_s.

4.1.3 Scaling Model Parameters with Applied Voltage

Figures 4.1–4.4 show excellent agreement between simulated and experimental data, but the model parameters used, which were optimized for a particular V_{max}, do not produce similarly good agreement at other V_{max}'s.

The variation is easily seen in a Q^e_{max}-V_{max} plot. The simulated (dotted) Q^e_{max}-V_{max} curve in Fig. 4.8 was produced using the same model which produced Figs. 4.1–4.4 – a basic Fowler-Nordheim diode model optimized for 40 V over threshold operation. Notice that the fit to the measured data is excellent at 40 V over threshold (~220 V), reasonably good at adjacent maximum voltages (especially higher voltages), and increasingly poor as the curves near threshold. Significantly, the simulated threshold is ~ 40 V below the experimental threshold and is much softer. If the simulation only needs to be accurate at high overvoltages (40-60 V over threshold), this model may suffice. However, it would be better to have a model which yields a close fit for any maximum applied voltage.

One simplistic solution to the problem of adjusting the model to yield accurate results at all voltages is to simply optimize the model parameters at different maximum voltages, tabulate the results, and incorporate a "look-up" table into the model so that different parameters are used depending on the maximum applied voltage. Such a table for the 650 nm thick device operated at 1000 Hz is found in Table 4.1, which relates the phosphor resistance (in steps of 50 kΩ) and the interface trap depth (in steps of 5 meV) to the voltage over threshold. Notice that for both R_p and Φ_B, smaller variations occur between larger overvoltage values and increasingly larger variations occur between small overvoltages. The nature of the relationship immediately suggests an exponential dependence on overvoltage.

Figure 4.9 shows a plot of the data in Table 4.1, where the dots are the data points from the table, and the solid lines represent exponential fits of the form

$$y = A\exp(-OV/\tau) + B \tag{4.1}$$

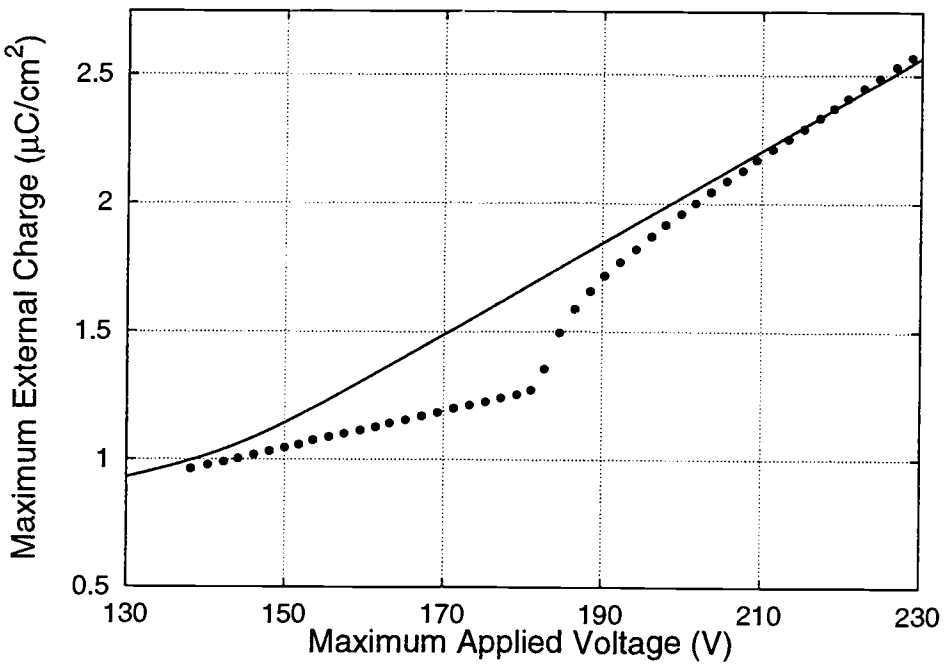

Figure 4.8: Q^e_{max}-V_{max} plot at 1000 Hz showing measured (dots) and simulated (solid line) data for 1000 Hz operation of a 650 nm thick ZnS:Mn device. The simulation is run using the basic Fowler-Nordheim model optimized for 40 V overthreshold.

where y is either R_p or Φ_B and OV is the overvoltage. The parameters A, B, and τ in Eq. 4.1 are determined using a least-squares algorithm, yielding

$$\Phi_B = 0.1022\exp(-OV/16.956) + 1.0186, \tag{4.2}$$

and

$$R_p = 2.098\exp(-OV/14.288) + 0.4975. \tag{4.3}$$

Equations 4.2 and 4.3 present a very good fit to the data in Table 4.1, as seen in Fig. 4.9, especially considering the limited precision of the best-fit parameters. These equations are added to the basic model so that the trap depth and phosphor resistance decay exponentially from their $OV = 0$ values when driven at voltages beyond threshold, resulting in the dashed line in the Q^e_{max}-V_{max} plot in Fig. 4.10.

The revised model is seen to present reasonable behavior above threshold. Two features of this curve are interesting, however. First, the post-threshold fit, although

Table 4.1: Best-fit Fowler-Nordheim diode basic model parameters for a 650 nm thick evaporated ZnS:Mn device operated at 1000 Hz.

Overvoltage (V)	R_p (MΩ)	Φ_B (V)
5	2.00	1.095
10	1.50	1.075
20	1.00	1.050
30	0.80	1.035
40	0.65	1.030
50	0.55	1.025
60	0.50	1.020

improved, is perhaps not as good as would be expected from Fig. 4.9. This is because the parameters (and thus the exponential fit) depend upon the overvoltage, but only the total applied voltage (i.e. the voltage applied across the series resistor, device, and sense capacitor) is available to the model. A possible solution to this problem would be to use the V_{max} value of the previous point to approximate the overvoltage of the next point, but this only makes sense in the context of a Q^e_{max}-V_{max} experiment. Other solutions would be to iteratively find the applied voltage if accuracy is very important, or to assume a capacitive voltage divider in determining which fraction of the applied voltage falls across the device.

The second interesting feature of the dashed curve in Fig. 4.10 is the poor behavior below threshold. The value of Φ_B below threshold is fixed at approximately 1.12 eV by Eq. 4.2, whereas a minimum value of approximately 1.30 eV is required to adequately prevent the device from turning on before the desired threshold voltage. Therefore, a simple solution to the poor threshold fit is to simply add 0.18 eV to the trap depth below threshold. This solution is unsatisfying, though, due to a

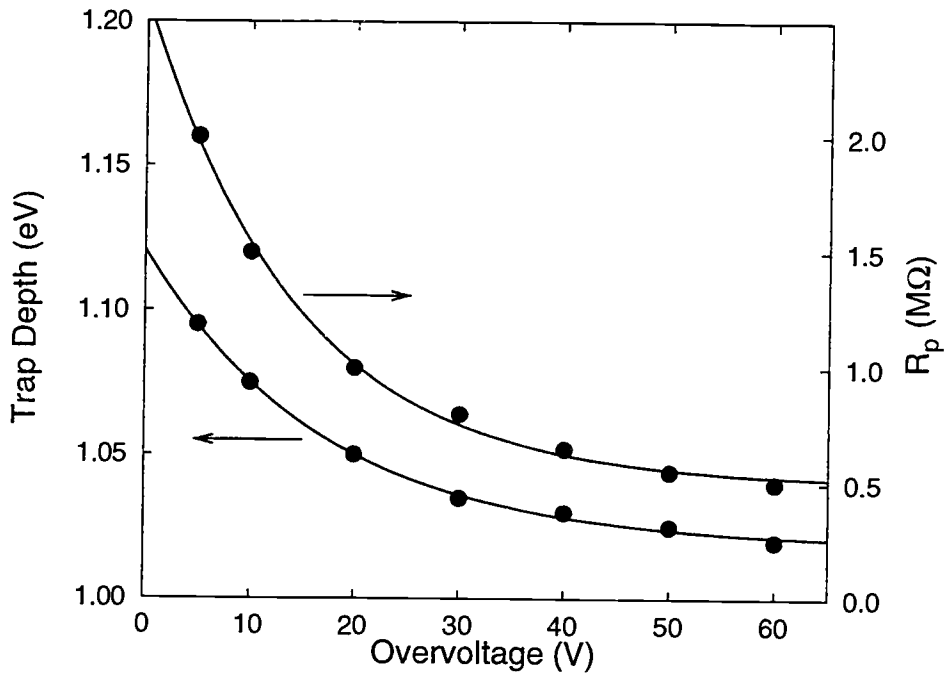

Figure 4.9: Best-fit parameters for a 650 nm thick evaporated ZnS:Mn device operated at 1000 Hz. The points are the data from Table 4.1, and the curves are the least-squares best-fit curves of the points to exponential functions.

resultant discontinuity – the device turns on very abruptly so that the transferred charge capacitance is infinite at threshold. It would be better to provide continuous behavior at threshold.

The first solution is to refit the trap depth model parameters while including a threshold value of Φ_B high enough to prevent subthreshold conduction. However, this was found to result in poor post-threshold fits to measured data. Alternatively, the parameters can be fit to an exponential equation with the form

$$\Phi_B = A\exp(-(OV + C)/\tau) + B, \tag{4.4}$$

again being sure to include a suitable value of Φ_B at threshold. This method produces better results. Better still are the results of adding a second exponential function to Eq. 4.2, as in

$$\Phi_B = 0.1022\exp(-OV/16.956) + 1.0186 + 0.18\exp(-OV/2). \tag{4.5}$$

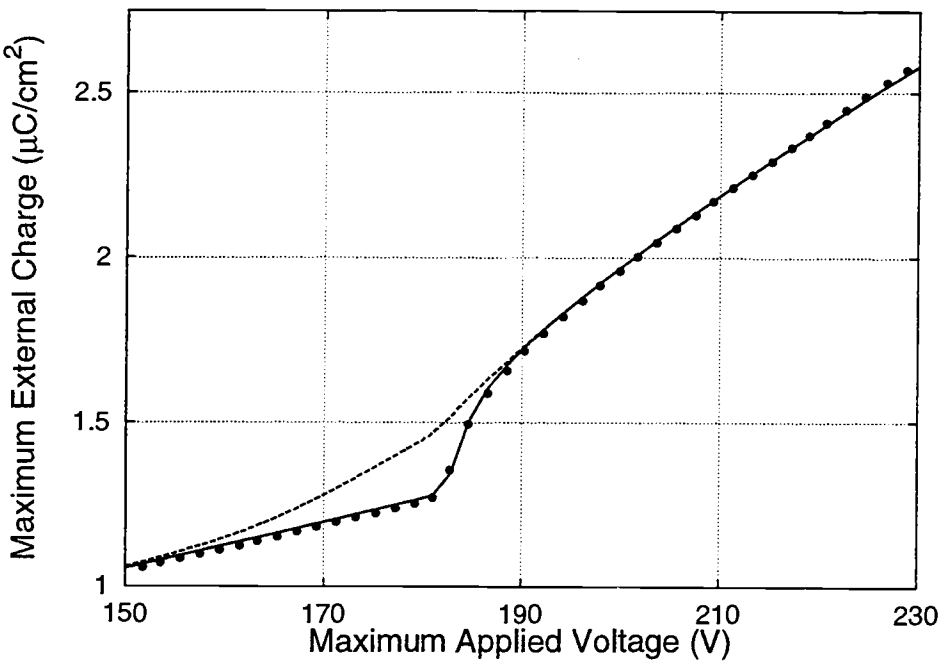

Figure 4.10: Q^e_{max}-V_{max} plots showing measured data (dots) and data simulated using two variations of the basic model. Variation of the interface trap depth is seen to produce trends consistent with post-threshold device operation, while failing to reproduce turn-on trends (dashed line). Adding a second exponential modulation to the model results in better near-threshold behavior (solid line).

The extra term increases the barrier height below threshold to the needed 1.30 V but decays quickly after threshold to reduce to Eq. 4.2. Adding Eq. 4.5 to the model results in the solid line curve shown in Fig. 4.10, which exhibits reasonable near-threshold and subthreshold behavior while maintaining post-threshold accuracy and providing a continuous-valued Φ_B at all voltages.

The difference between the two simulated and the measured curve in Fig. 4.10 below threshold also deserves comment. This difference is due to a mismatch in capacitance between the model and the physical device. The capacitance values used in the model are determined from a Q-V curve at 40 V over threshold. However, capacitance values are often seen to vary slightly with the overvoltage and with the technique used to determine them. For instance, it is routinely found that capacitances derived from C-V curves, Q^e_{max}-V_{max} curves, and the physical information

often differ. These discrepancies lead to the difference seen in Fig. 4.10; using capacitance values in the model more consistent with the Q^{e}_{max}-V_{max} plot would have resulted in reduced charge transfer post-threshold, so it was decided to focus on the post-threshold regime instead.

Finally, a brief discussion of some aspects of the physical nature of these parameters is warranted. First, consider the barrier height, Φ_B. Several researchers have estimated the theoretical value of the trap energy level. [16, 21, 37, 38] Aguilera et al. employed a technique in which current transient data is measured and used to estimate the interface electron energy distribution. The assumptions of no bulk trap contribution to the current (i.e. no space charge) and emission via pure tunneling led to an estimated trap energy peak of 1.03 eV for ZnS:Mn devices with SiON insulator layers [37], which is also the best-fit value of Φ_B in the basic Fowler-Nordheim SPICE model for the ZnS:Mn device employed in this thesis when operated at 40 V over threshold, as mentioned in Section 4.1.1. More recently, the physical value of Φ_B for these devices has been estimated as $\sim$1.5 eV from electrical characterization of ACTFEL devices with varying phosphor thicknesses. [38, 39] However, this calculation includes the effect of static space charge in the phosphor layer. As discussed in Sec. 2.2.2, in a physical device under excitation, the electric field near the cathode is higher than the average phosphor electric field due to the presence of static space charge throughout the phosphor, so that tunnel-emission from this interface is more probable than the externally measured phosphor field would imply. However, space charge is not considered in the Fowler-Nordheim model shown in Fig. 3.1. Additionally, the built-in Fowler-Nordheim tunneling diode model current-voltage characteristic given in Eq. 3.1 does not include Coulombic barrier lowering effects. For both of these reasons, the interface state depth must be artificially lowered to the values given in Table 4.1 in order to obtain a good fit to data in the simulations.

Next, consider the phosphor resistance, R_p. R_p is to be regarded primarily as an adjustable parameter which quantitatively accounts for leakage charge in simulated

Q-V curves. The physical significance of R_p (if any) is obscure. The resistivity of the ZnS phosphor has been reported as 10^8-10^{14} Ω·cm [40], corresponding to values of R_p ranging from 75 kΩ to 7.5×10^{10} Ω. While the best-fit values of R_p in the simulation are within this range, it is very doubtful whether this is in fact chiefly due to the low-field resistance of ZnS because of the uncertainty of the resistivity. In fact, the fact that the phosphor resistance value must be increased by a factor of twenty from the 1000 Hz best-fit values to fit 60 Hz values well argues strongly against this interpretation. R_p may instead account for emission from the interfaces via an unknown mechanism which is not included in the Fowler-Nordheim model. As mentioned briefly in Sec. 2.2.1, the origins of the leakage charge phenomenon are poorly understood; researchers have not been able to reproduce all of the experimental trends despite including interface emission through a number of processes, including a number of variations of thermal, tunnel, and photon-assisted tunnel emission. [41]

4.1.4 Inclusion of Coulombic Barrier Lowering

Replacing the built-in Fowler-Nordheim with a user-defined voltage-controlled current source following from Eq. 3.9 produces simulation results very similar to those discussed above, with one exception: the value of the barrier height Φ_B needed to match the simulations to experimental data is increased. For instance, although a value of $\Phi_B = 1.030$ eV was needed to match the simulation to data in Section 4.1.3, a value of $\Phi_B = 1.125$ eV produced a similar fit with barrier lowering included in the model. This is about what would be expected from Eq. 3.10; using $\varepsilon = 1.2$ MV/cm as the steady-state field value, Eq. 3.10 gives $\Delta\Phi_B = 0.091$ eV, and $1.125 - 0.091 = 1.034$ eV gives us the best-fit value without including the barrier lowering term. Additionally, a Q^e_{max}-V_{max} curve generated using a model with barrier lowering effects included is identical to a curve generated using the model without barrier lowering, except that the former is shifted rigidly along the voltage axis from the latter.

Including the barrier lowering correction brings the simulation value of Φ_B closer to the experimentally estimated value of 1.5 eV, with static space charge effects assumed to be responsible for the remaining discrepancy. However, this more "physically real" parameter value comes at a cost: the simulations take approximately twice as long to run using the user-defined model than the built-in model, apparently due to the internal programming of HSPICE, but the simulation results do not actually improve. It is therefore better to accept a lower best-fit value of Φ_B and to use the faster built-in model.

4.2 Device Physics-Based Emission Model

As discussed in Section 4.1.3, the value of the simulation interface trap depth of the Fowler-Nordheim ACTFEL SPICE model needs to be changed for different maximum applied voltages in order to obtain the best fit to experimental data for each V_{max}. The fact that the simulation trap depth needs to be only slightly changed for different maximum applied voltages was thought to possibly be due to trap occupancy considerations; this question was one motivation for developing the device physics-based SPICE model in Section 3.2. From a device physics standpoint, the emission rate of electrons from the interface is determined not only by the barrier height, cathode field, and effective mass, as in Eq. 3.1, but also by the occupancy of the discrete trap. For the basic Fowler-Nordheim model, though, the occupancy is assumed to be constant; given the accuracy of the fit to experimental data, this assumption seems justified. However, the occupancy of the cathodic trap just before a voltage pulse is applied is determined in part by the maximum applied voltage of the previous pulse, so that the emission rate is enhanced for larger values of V_{max}. Since occupancy is not included in the model, it was thought that this could possibly account for the need to reduce the simulation barrier height as V_{max} is increased in order to maintain the quality of the fit to data.

However, simulations run using the device physics-based model with occupancy included indicate that this is not the case. The interface trap depth still needs to be adjusted for each maximum applied voltage, and by the same amounts as in the Fowler-Nordheim diode model.

4.3 Single-Sheet Charge Model

The behavior of the single-sheet charge SPICE model is consistent with that of the original device physics model. Most importantly, asymmetric C-V overshoot is observed, with an increasing amount of overshoot as the sheet of charge is moved closer to one of the insulator/phosphor interfaces. The inner workings and the effects of the model parameters are similar to those of the double-sheet charge model; in fact, the single-sheet charge model is a special case of the double-sheet charge model. Since that model is discussed in some detail in the next section, further discussion of the single-sheet model is unnecessary.

4.4 Double-Sheet Charge Model

4.4.1 Results of twelve current source model

The most obvious benefit of the two-sheet charge model is the ability to model symmetric and asymmetric capacitance overshoot. Figure 4.11 shows the C-V characteristics for the twelve current source model described in Section 3.4, using the parameters listed in Table 4.2. Only the positive polarity is shown since the negative polarity C-V curve is identical for the parameters simulated. The effects of space charge are also apparent for both polarities as field overshoot in the Q-F_p plot of Fig. 4.12.

The internal operation of the model is most easily elucidated through an examination of the electronic occupancy of each interface or sheet of charge. Figure 4.13 shows the number of electrons trapped at the bottom phosphor-insulator interface

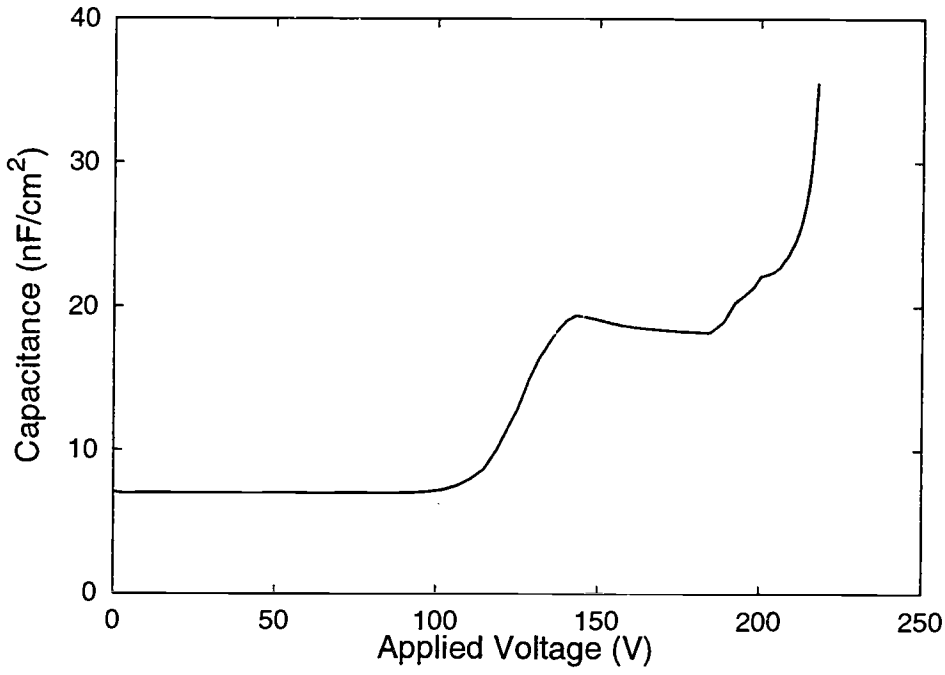

Figure 4.11: C-V plot showing capacitance overshoot in the two-sheet charge model with space charge creation via field emission. This overshoot is present for both applied voltage polarities.

(outer curve) and the first sheet of charge (i.e. the charge sheet near the bottom interface; inner curve) as a function of the applied voltage. First, note that both $N_0 f_0$ and N_T are set to 5×10^{13} cm^{-2}, as noted in Table 4.2. At the beginning of a positive pulse, the occupancy of the bottom interface is higher than this number, due to the accumulation of electrons emitted from the top interface during the previous negative half-cycle. As the applied voltage is ramped past the turn-on voltage, the interface begins to emit electrons, and the number of electrons trapped there decreases to a minimum at the end of the applied pulse. The trap is then refilled through a combination of leakage charge from the top interface during the interpulse interval and by electrons emitted from the top interface or sheets of charge during the negative portion of the applied voltage waveform. As seen in Fig. 4.13, electrons begin to be emitted from the first charge sheet approximately at the same time as interfacial emission begins. This "extra" emission, which is not expected in a device without

Table 4.2: Nominal double-sheet charge ACTFEL SPICE model simulation parameters.

Simulation Parameter	Value	Simulation Parameter	Value
Phosphor Thickness	650 nm	Interface Trap Depth	1.30 eV
Phosphor Dielectric Constant	8.3	Space Charge Trap Depth	1.25 eV
Total Insulator Capacitance	18 nF/cm^2	Electron Relative Effective Mass	0.18
Device Area	0.085 cm^2	Neutral Interface Trap Density	5×10^{13} cm^{-2}
Charge Sheet Distance from Interfaces	50 nm	Bulk Trap Density	5×10^{13} cm^{-2}
Rise Time	5 μs	Electron Capture Critical Field	2 MV/cm
Pulse Width	30 μs	Thermal Emission Cross Section	1×10^{-15} cm^2
Fall Time	5 μs	Temperature	300 K
Frequency	1000 Hz	Series Resistance	500 Ω
Cycles Simulated	3	Sense Capacitance	109.0 nF

space charge, is responsible for the overshoot seen in C-V characteristics. Alternatively, the emission from the sheet of charge acts to reduce the voltage dropped across the entire phosphor while the total amount of transferred charge is increased – the creation of space charge reduces the field at the anode while maintaining a relatively constant field at the cathode – leading to a negative differential capacitance; this negative capacitance is responsible for the C-V overshoot. Note that it is possible for charge emitted from the bottom interface to be trapped at the first charge sheet during this time, but the capture probability is very small due primarily to the high field near the sheet of charge, as seen in Fig. 4.14. However, notice that the occupancy of the first sheet of charge increases during the positive voltage pulse plateau portion of the waveform; this increase is a consequence of the flow of relaxation charge which reduces the field, which in turn increases the space charge capture factor. The traps

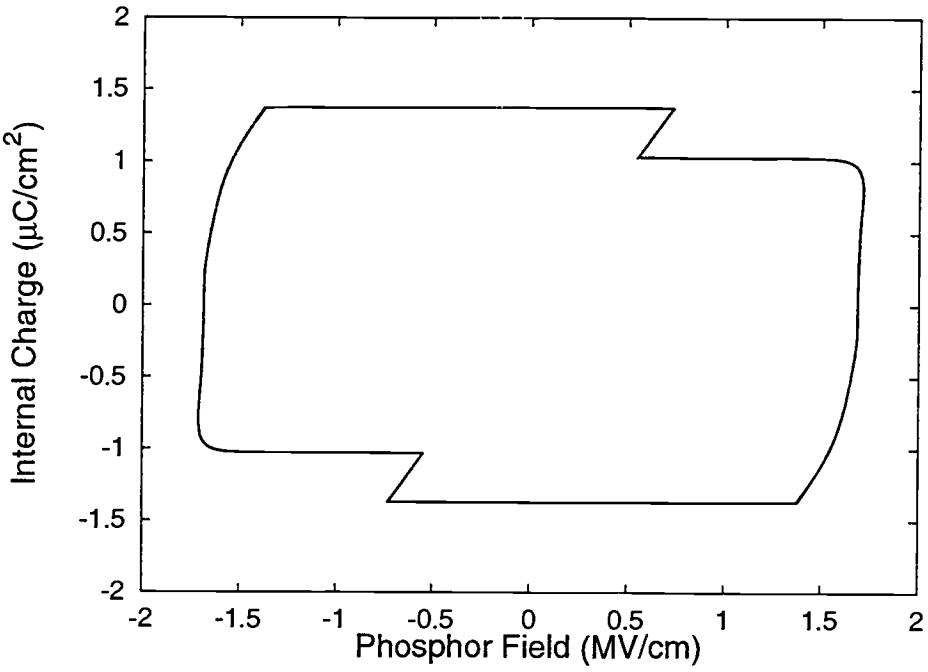

Figure 4.12: Q-F_p plot showing field overshoot in the two-sheet charge model with space charge creation via field emission.

in the first charge sheet are refilled during the negative portion of the applied voltage waveform by electrons emitted from the top interface or from the second sheet of charge. Finally, notice that the occupancy of the bulk trap does not exceed N_T as that of the interfacial trap exceeds $N_0 f_0$. In fact, depending on the value specified for the critical field for electron capture, or other simulation parameters, the charge sheet does not necessarily have to be refilled completely. Rather, a certain number of traps are unfilled at all times during the waveform. The positive space charge present due to these permanently unfilled traps could be used to simulate static space charge. For the simulation shown in Fig. 4.13, the parameters are set so that the charge sheet is fully refilled in order to increase the amount of C-V overshoot.

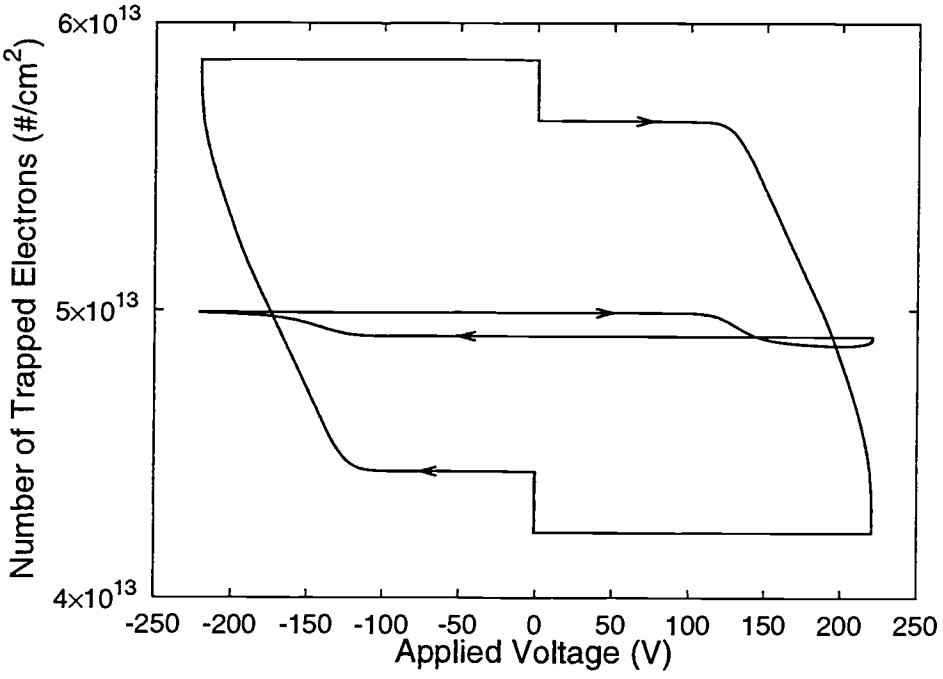

Figure 4.13: Plot showing the occupancy of the bottom insulator-phosphor interface (outer curve) and the first sheet of charge (inner curve). $N_0 f_0$ and N_T are both 5×10^{13} cm^{-2}.

4.4.2 Effects of Model Parameters

The simulation parameters used to create the double-sheet charge model output results presented so far are shown in Table 4.2. In the next several subsections these values are systematically varied in an effort to explore the simulation space and to understand each parameter's effect on the model.

4.4.2.1 Variation of space charge sheet locations

Figure 4.15 shows the dependence of the observed capacitance overshoot on the position of the sheets of charge. As found previously in device physics-based ACTFEL simulations and in the single-sheet charge model, the amount of capacitance overshoot seen increases as the sheets are moved closer to the insulator interfaces, and disappears when the sheets are placed close to the middle of the phosphor layer.

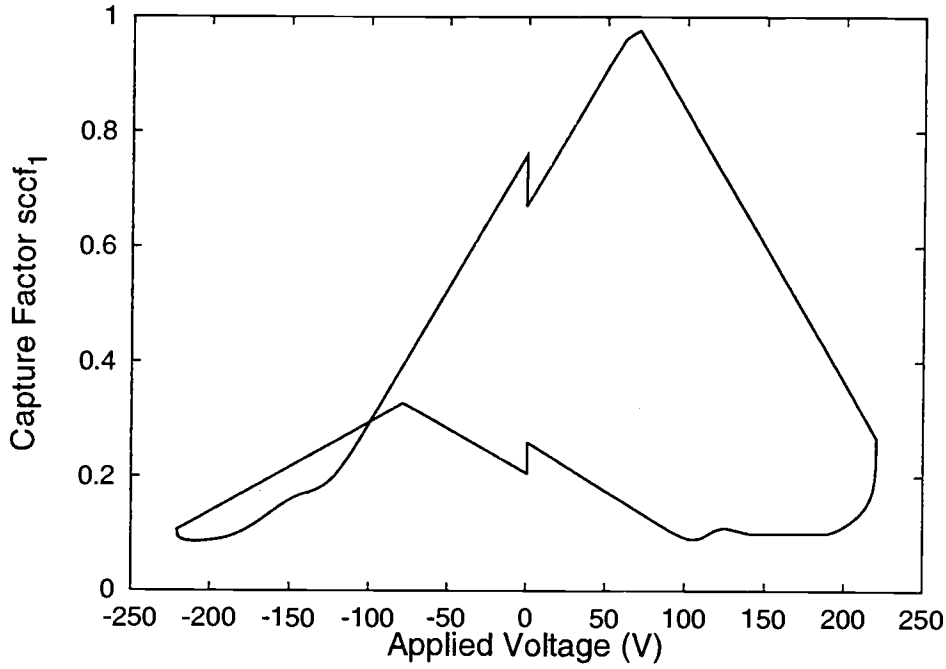

Figure 4.14: The space charge capture factor for the first sheet of charge, $sccf_1$, plotted against the applied voltage.

4.4.2.2 Variation of trap depths

As in the other SPICE ACTFEL models discussed previously, the electron trap depth is an important parameter in the double-sheet charge model. As before, the magnitude of the insulator-phosphor interface trap depth affects not only the turn-on voltage of the device but also the amount of transferred charge and the magnitude of the steady-state field. The energy of the bulk traps in the double-sheet charge model have similarly important effects on the model output. Figure 4.16 shows the Q-F_p and C-V plots for increasing values of the bulk trap depth, with the interface trap depths fixed. Several trends are of interest. First, notice that a decrease in the bulk trap depth leads to a reduction in turn-on voltage. It is obvious from Eq. 3.11 that if the bulk trap depth is lower, emission from these traps will occur at lower fields and thus at lower applied voltages. As emission occurs, an increasing positive charge is left at the charge sheet, which pushes the energy bands downward. This

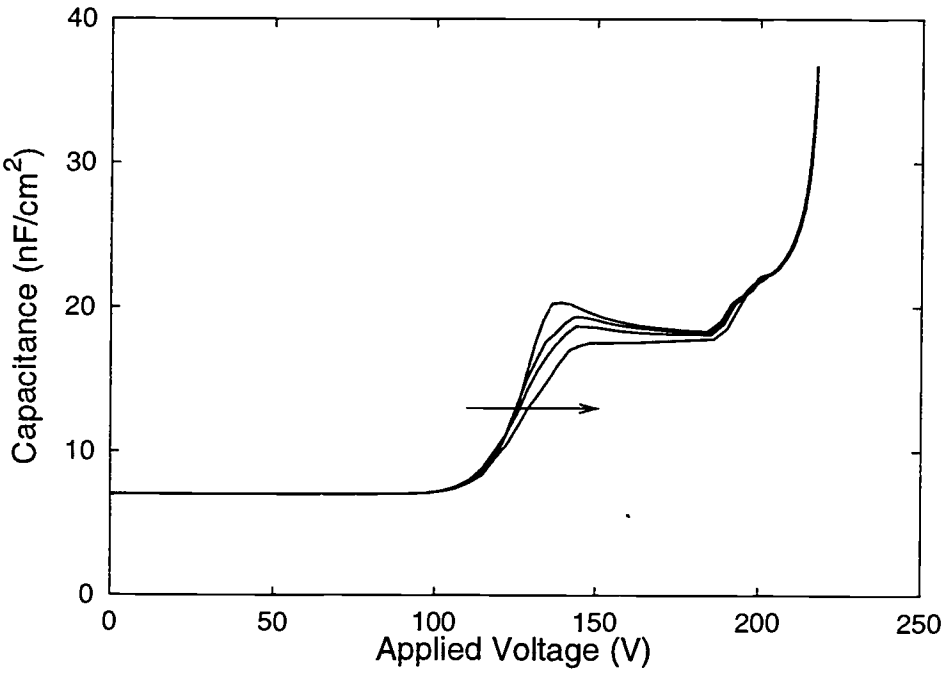

Figure 4.15: C-V plots with the two space charge sheets located 100, 500, 1000, and 2000 Å from the top and bottom insulator-phosphor interfaces. The phosphor thickness is 6500 Å.

acts to reduce the field in the phosphor region on the anode side of the charge sheet, retarding further emission from the sheet, while concomitantly increasing the field in the phosphor region on the cathode side. This increase prompts earlier emission from the cathodic interface, even if the interfacial trap depth is not lowered.

The second feature worthy of discussion in Fig. 4.16 is the reduction in the amount of C-V overshoot with the increase in bulk trap depth. This is understood from Fig. 4.17, which shows the occupancy of the bottom interface and the first sheet of charge. Notice that as the bulk trap depth is decreased, a larger amount of charge is emitted from the sheet of charge, and also that this emission occurs over a smaller voltage range (that is, the magnitude of the derivative dn_{scl}/dv_a is larger during the emission). Both of these factors lead to larger overshoot. There is a point of diminishing returns, however: if the bulk trap depth is made much smaller than the interface trap depth, there is an increasingly large difference between the voltage

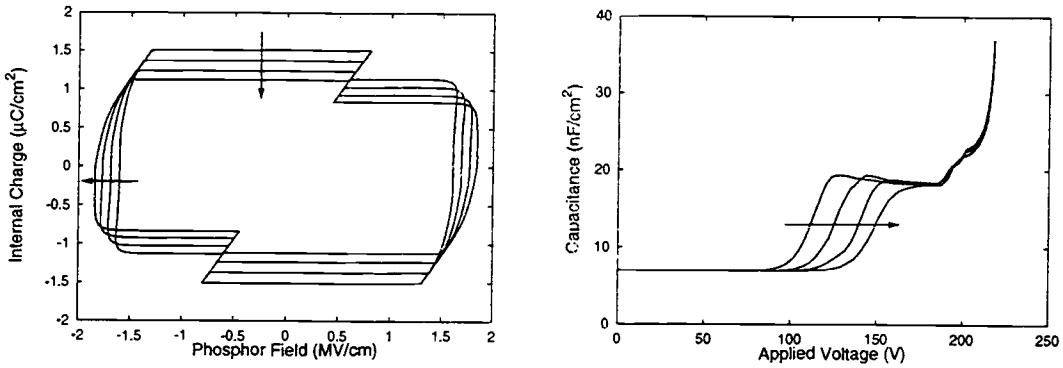

Figure 4.16: Q-F_p and C-V plots with bulk trap depth Φ_{Bt} = 1.20, 1.25, 1.30, and 1.35 V and interface trap depth Φ_B = 1.30 V. Arrows indicate increasing Φ_{Bt}.

at which the sheet of charge begins emitting and the voltage at which the interface begins emitting. A larger overshoot will result when the concurrent emission from both the interface and the charge sheet is maximized. The difference in voltages for the beginning of emission leads to less emission overlap, and therefore reduces the observed overshoot; thus, in Fig. 4.16, the overshoot exhibited for Φ_{Bt} = 1.20 V is roughly the same as for Φ_{Bt} = 1.25 V, although the device turns on earlier and exhibits more charge transfer.

If the bulk trap depth is specified to be larger than the interface trap depth, the sheet of charge will begin emission later than the interface and emit much less charge, and the amount of overshoot becomes negligible. In the limit, the specification of a significantly larger bulk trap depth causes the double-sheet charge model to be reduced to the model without space charge presented in Section 3.2.

4.4.2.3 Variation of bulk trap concentration

Due to their appearance in Eq. 3.11, the energy of the bulk traps and the electron effective mass are important parameters affecting the emission rate from the sheets of charge. Likewise, the number of states available at a sheet of charge is an important emission parameter due to the relation in Eq. 3.15. Figure 4.18 shows the Q-F_p and C-V plots which result when the bulk trap density is varied while the inter-

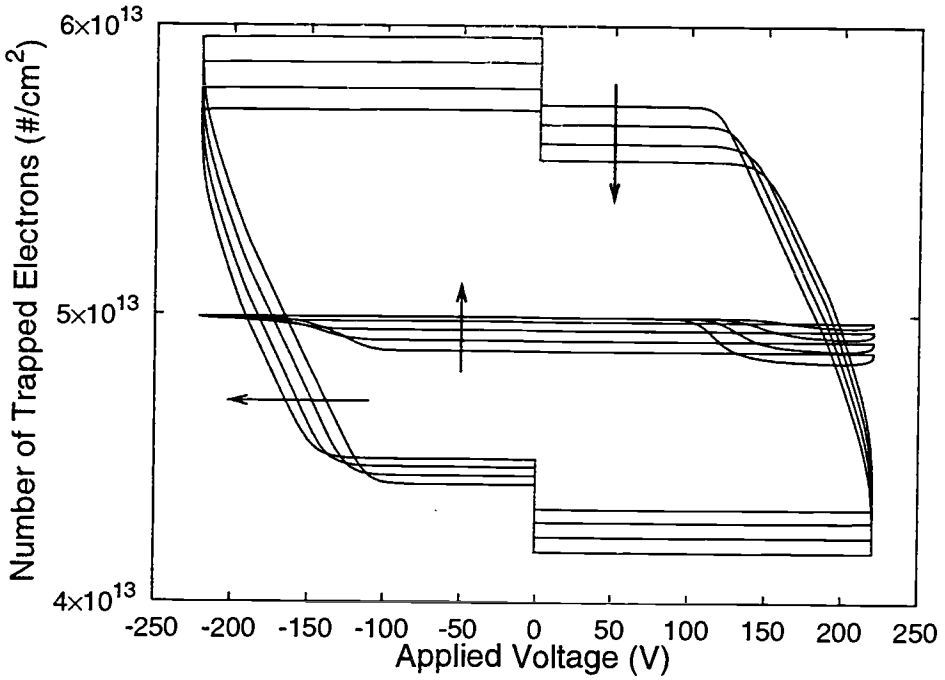

Figure 4.17: Plot showing the occupancy of the bottom insulator-phosphor interface and the first sheet of charge for bulk trap depth Φ_{Bt} = 1.20, 1.25, 1.30, and 1.35 V and interface trap depth Φ_B = 1.30 V. Arrows indicate increasing Φ_{Bt}. $N_0 f_0$ and N_T are both 5×10^{13} cm^{-2}.

face trap density is held constant. The amount of C-V overshoot observed increases with increasing N_t, since a larger amount of space charge is created. For illustration, the maximum change in the occupancy of a sheet of charge corresponding to the simulation results shown in Fig. 4.18 when N_t is set to 5×10^{12}, 5×10^{13}, and 5×10^{14} cm^{-2} is approximately 0.05×10^{13}, 0.12×10^{13}, and 0.17×10^{13} cm^{-2}, respectively. Note also that the bulk trap concentration N_t is also important in determining the value of the space charge capture coefficient $sccf_x$, as seen in Eq. 3.23.

4.4.2.4 Variation of occupancy and capture factors

The parameters discussed in the previous subsections primarily affected the model behavior through a modification of the emission of electrons from either the insulator-phosphor interface or from the sheets of charge. Several other parameters also play a significant role in the operation of the model by modifying the way in

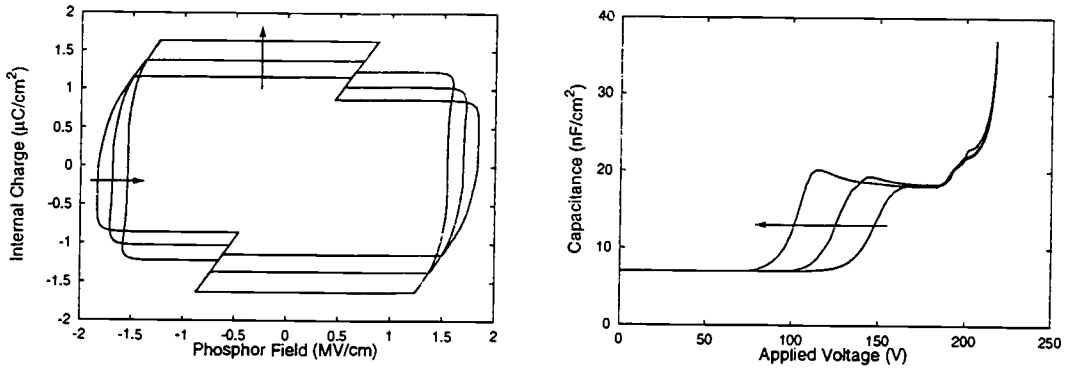

Figure 4.18: Q-F_P and C-V plots with bulk trap density $N_t = 5 \times 10^{12}$, 5×10^{13}, and 5×10^{14} cm^{-2}. Arrows indicate increasing N_t.

which emitted electrons are recaptured. These are the parameters which appear in Eq. 3.24 for the field- and occupancy-dependent space charge capture factor $sccf_x$, namely the critical capture field f_{0c} above which no electron can be captured by a bulk trap and y, which governs how important the occupancy of the trap is in determining the capture coefficient.

Figure 4.19 shows the Q-F_P and C-V plots which result from setting f_{0c} to 1.5, 2.0, and 3.5 MV/cm. From Fig. 4.20, it is seen that increasing f_{0c} results in an increase in $sccf_x$ for all voltages, since $\left|\frac{f_P}{f_{0c}}\right|$ in the right term of Eq. 3.24 approaches zero for large f_{0c}, forcing the right term to 1. Conversely, a small critical capture

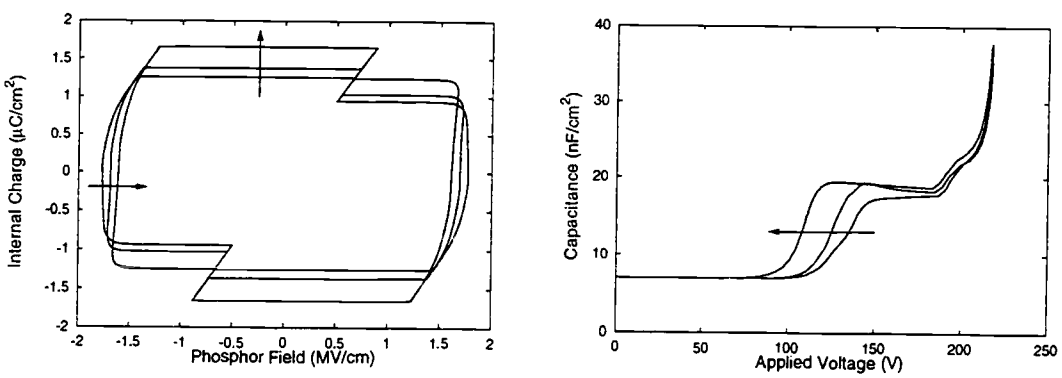

Figure 4.19: Q-F_P and C-V plots with electron capture critical field f_{0c} = 1.5, 2.0, and 3.5 MV/cm. Arrows indicate increasing f_{0c}.

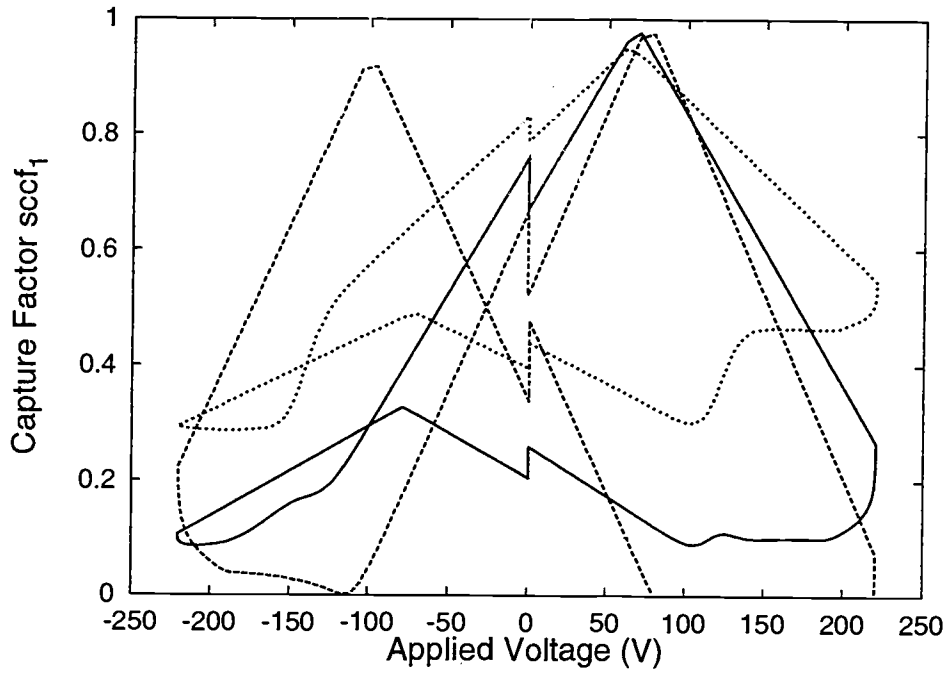

Figure 4.20: Plot of the space charge capture factor for the first sheet of charge $sccf_1$ as a function of the applied voltage for electron capture critical field $f_{0c} = 1.5$ (dashed line), 2.0 (solid line), and 3.5 (dotted line) MV/cm.

field results in a smaller right term and therefore a smaller capture coefficient. For $f_{0c} = 1.5$ MV/cm in Fig. 4.20, $sccf_1$ is equal to zero during the rising edge of the applied voltage, and no electrons emitted from the interface are captured at the first sheet of charge. The capture factor is low enough throughout the entire waveform that the sheet of charge is never fully refilled to its zero-field value. Therefore, in post-threshold steady-state operation, an amount of positive charge is present at each sheet of charge for all values of applied voltage; this is therefore a model of static space charge.

Variation of the other important parameter in Eq. 3.24, the exponent y, leads to the Q-F_p and C-V plots shown in Fig. 4.21, in which y is set equal to 1, 10, and 100. As seen from Fig. 4.13, the number of occupied states at a sheet of charge, n_x, is quite large in relation to the total number of states N_t at all times, so that $\frac{n_x}{N_t}$ in Eq. 3.24 is very nearly unity for all voltages. If $y = 1$, $sccf_x$ is therefore forced towards

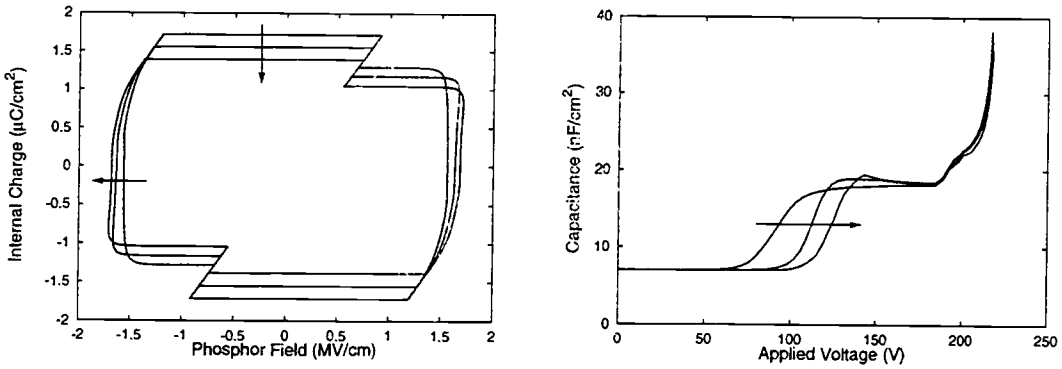

Figure 4.21: Q-F_p and C-V plots with $y = 1$, 10, and 100, where y is the exponent in Eq. 3.24. Arrows indicate increasing y.

zero. In this case, each sheet of charge will emit electrons during the first one or two simulation cycles, but since the capture factor is so small, the charge sheets never recapture an appreciable number of electrons. The result is the presence of static, but no dynamic, space charge during operation. Thus, no C-V or Q-F_p overshoot is observed, but the turn-on voltage of the device is nevertheless decreased due to the cathodic field enhancement as a result of the static space charge. As y is increased, $\left(\frac{n_x}{N_t}\right)^y$ in Eq. 3.24 becomes increasingly smaller and thus the capture factor becomes increasingly larger; only when n_x is very nearly equal to N_t does $sccf_x$ become zero due to the left term in Eq. 3.24. As a result, more electrons are able to be recaptured, and thus the amount of dynamic overshoot and the observed C-V overshoot increase.

As just mentioned, setting $y = 1$ results in the formation of static space charge in the model, since the capture factor is too small to lead to refilling of the charge sheets. Thus, the value of the interface trap depth Φ_B can be increased towards its experimentally estimated value of 1.50 V. Figure 4.22 shows the result of simulation with $y = 1$, $dp1 = dp2 = 100$ Å, $N_t = 1 \times 10^{14}$ cm^{-2}, $\Phi_B = 1.50$ V, and $\Phi_{Bt} = 1.38$ V. It is no longer necessary to artificially suppress the depth of the interfacial trap to achieve good fits to experimental data. The model has the additional benefit of modeling device behavior over a wide range of applied voltages better than the models

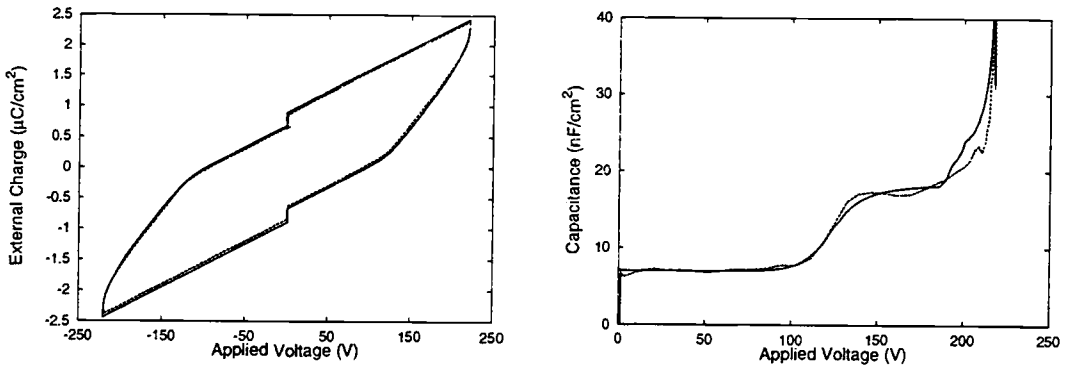

Figure 4.22: Q-V and C-V plots showing simulated (solid line) and measured (dashed line) data. The simulation was run using the double-sheet charge model with $y = 1$ to simulate static space charge, allowing the experimentally estimated value of 1.50 eV to be used for the interfacial trap depth.

discussed earlier. Figure 4.23 shows a Q^e_{max}-V_{max} curve corresponding to the model used to generate Fig. 4.22, as compared to experimental data and output from the basic Fowler-Nordheim model. Although the double-sheet charge model still begins transferring charge somewhat early, the pre- and near-threshold behavior is obviously much improved over previous models. In fact, the reduction in error between the measured and simulated curves for different applied voltages implies that the need to adjust model parameters in Section 4.1.3 for different maximum voltages was a result of the lack of space charge modeling in the Fowler-Nordheim model. The double-sheet charge model also exhibits transferred charge capacitance overshoot, as evidenced by the fact that the slope of the curve immediately after threshold is higher than the insulator capacitance. This overshoot is more clearly seen in the solid line in Fig. 4.24, in which the derivative of Q^e_{max}-V_{max} plots of the double-sheet space charge model and an evaporated ZnS:Mn ACTFEL device are plotted. This is consistent with the interpretation of the overshoot in terms of the presence of static space charge in the device. It should be noted that when the model is simulated using the parameters listed in Table 4.2 (which leads to a miniscule concentration of static space charge) a comparatively very small amount of transferred charge derivative overshoot is seen.

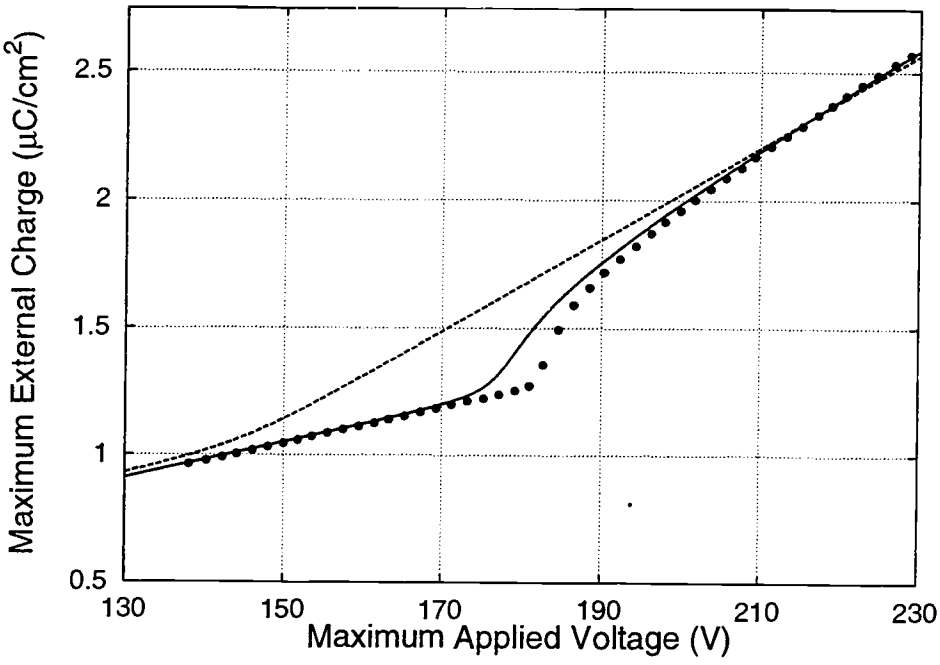

Figure 4.23: Q^e_{max}-V_{max} plot showing measured data (dots), output from the basic Fowler-Nordheim ACTFEL SPICE model (dashed line), and output from the double-sheet charge model (solid line). Notice that the double-sheet charge model exhibits transferred charge capacitance overshoot.

Interestingly enough, the double-sheet charge ACTFEL SPICE model with static space charge modeled also reproduces experimental data which results from the electrically reset transferred charge measurements conducted by Hitt. [38] In this analysis method, a large number of bipolar trapezoidal waveforms which have a maximum voltage amplitude in excess of the device threshold voltage are applied to the ACTFEL device, in order to preset the polarization charge in the device to a controlled standard value. Then, a measuring pulse is applied to the device, and the amplitude of this measuring pulse and the maximum external charge are recorded. For the next measurement, an identical train of setting pulses is again applied, followed by another measurement pulse with an increased amplitude, and so on. The derivatives of the resulting electrically reset transferred charge curves no longer exhibit overshoot. When this experiment is simulated using the double-sheet charge

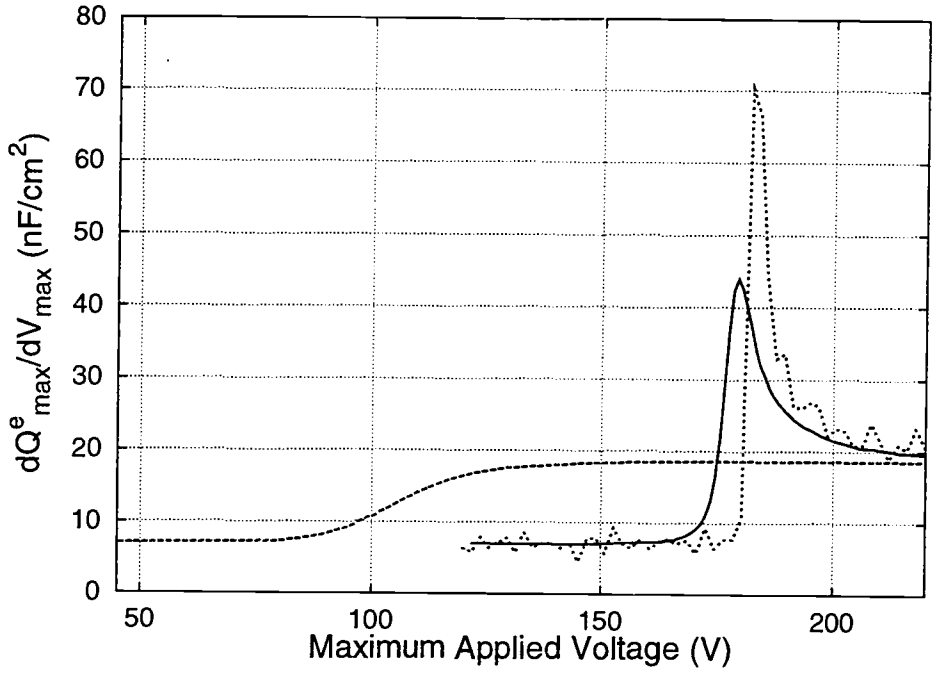

Figure 4.24: Transferred charge derivative curves for a real evaporated ZnS:Mn device (dotted line) and the double-sheet charge SPICE model with static space charge (solid line). The dashed line shows the behavior of the model with static space charge when a series of setting pulses with V^{sp}_{max} = 200 V is applied to the model before the measuring pulse with V_{max} is applied.

model, the dashed curve in Fig. 4.24 results; no overshoot is seen. Furthermore, the model predicts a reduction in the transferred charge derivative threshold voltage of approximately 80 V for setting pulses with V^{sp}_{max} 30 V above the device threshold and a reduction in the slope of the curve near this 'threshold.' Both of these behaviors are also seen in experimental data. Hitt also showed experimentally than most, if not all, of the overshoot seen in transferred charge derivative curves is due to overshoot in relaxation charge derivative curves. He thus speculated that ACTFEL devices driven by applied voltage waveforms with no plateau width would not exhibit transferred charge capacitance overshoot, although this experiment produced inconclusive results due to noise in the data. However, when this zero pulse-width experiment is simulated using the double-sheet charge ACTFEL SPICE model with static space charge modeled, there is indeed no overshoot in the transferred charge derivative curve, im-

plying that all of the overshoot seen experimentally is in fact due to overshoot in the relaxation charge derivative curve.

Finally, although the double-sheet charge model curve in Fig. 4.23 is not perfect, it is reasonable to believe that the fit between experimental Q^{e}_{max}-V_{max} data and the double-sheet charge model output can be further improved through additional adjustment of the model parameters.

4.4.3 Model Simplification

The equivalent circuit for the SPICE two-sheet charge model shown in Fig. 3.8 is appropriate for the most general case; that is, all possible connections between different phosphor nodes are established and appropriate mathematical relationships between them are modeled using voltage-dependent current sources. This is appropriate in device physics modeling, where the simulations should reflect physical reality as much as possible. However, each additional current source that is included in the SPICE model increases the simulation time. Therefore, it may be desirable to create a simpler two-sheet charge model by eliminating unnecessary current sources from Fig. 3.8. As seen from Fig. 4.13, the role that cathodic phosphor-insulator interface emission plays in refilling the traps in the closest sheet of charge is minor due to the high field in this region; thus, j_{ibsc1} can be eliminated. Since the number of electrons emitted from bulk traps is much smaller than the number emitted from interfaces, the role that these electrons play in refilling the other sheet of charge is small also; therefore, j_{sc1sc2} can be removed. Finally, since the sheet of charge located closest to the anode is expected to be in a low-field region, emission from that sheet is likely to be small, and j_{sc2it} can be omitted. Three sources are left, which are required for proper operation of the model: j_{ibit} accounts for most of the conduction charge, j_{sc1it} accounts for C-V overshoot, and j_{ibsc2} is needed to refill the second charge sheet. Repeating the elimination process for the other applied voltage polarity leads to a model which has only six current sources, reduced from twelve.

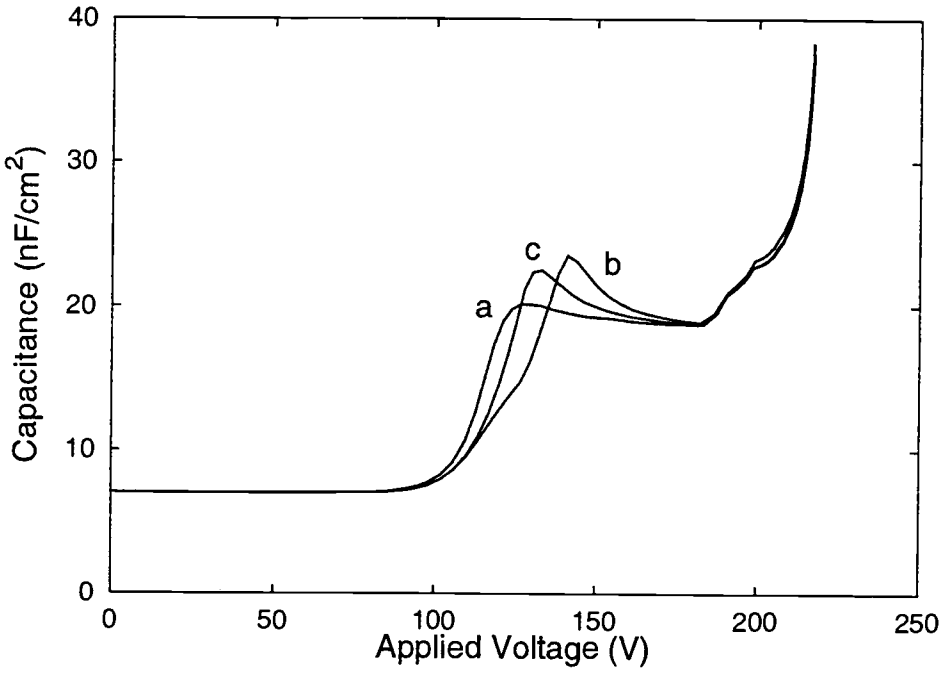

Figure 4.25: C-V plots showing capacitance overshoot in simplified six-current source two-sheet charge models. The models which produce these curves differ only in the handling of the charge capture coefficient. The model which produces curve (a) uses a field-dependent space charge capture factor and does not allow negative space charge. Curve (b) is similar to (a), except negative space charge is allowed in the model. Curve (c) results when a constant capture factor $sccf = 0.15$ is used.

C-V plots produced using this simplified six-current source model are shown in Fig. 4.25. Curve (a) exhibits a similar amount of overshoot to that shown in Fig. 4.11 yet this model requires only one-third of the computing time as the twelve-source model. Curve (a) uses a field-dependent space charge capture factor and does not allow negative space charge. Eliminating the stipulation that no negative space charge be allowed results in a modest computer time savings, as the current source equations are simplified. This has the added benefit of increasing the amount of C-V overshoot, since more charge is available at the cathodic charge sheet to be emitted, as seen in curve (b) of Fig. 4.25. Note that Fig. 4.25(b) exibits a reduced slope at the onset of turn-on, which can be understood in terms of the following. The excess electrons trapped at the 'overfull' sheet of charge result in the energy bands being pushed

upward compared to the limited-occupancy case, which serves both to reduce the field at the cathodic interface and to increase the field at the sheet of charge. Thus, electron emission from the interface is more difficult than before, while emission from the sheet of charge is easier. Thus, the sheet of charge now begins emitting electrons before the interface does. A similar effect is seen when the trap depth at the sheets of charge are specified as significantly lower than the trap depth at the interfaces. Finally, the space charge capture factor can be replaced by a constant, resulting in a model which simulates in only one-sixth the time of the original twelve-current source model. For $sccf = 0.15$, curve (c) in Fig. 4.25 results.

4.4.4 Space Charge via Trap-to-Band Impact Ionization

Although field emission as a space charge creation mechanism can result in a moderate amount of capacitance and field overshoot and can usefully model ZnS:Mn systems, it is unable to account for the often very large amounts of overshoot seen in certain other material systems, such as devices employing a SrS:Ce phosphor layer. Furthermore, the relative graduality of space charge formation via field emission does little to explain the large spikes often seen in the current transients of devices such as those with Zn_2GeO_4:Mn phosphor layers. Carrier multiplication is widely used to explain such phenomena.

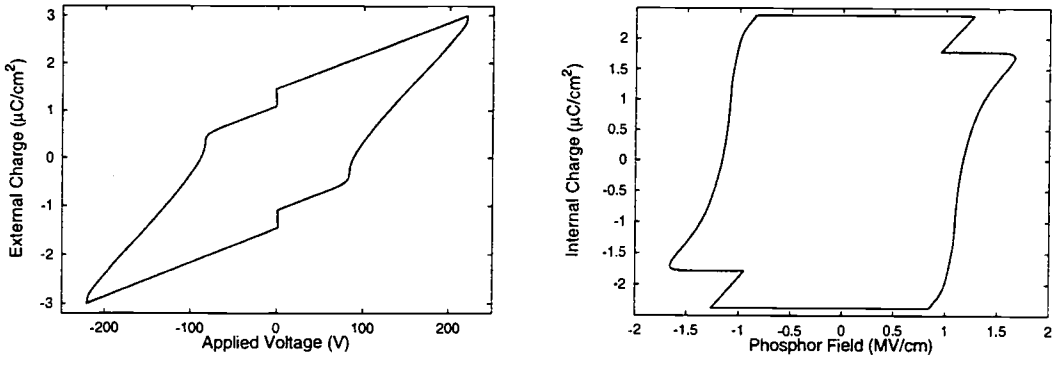

Figure 4.26: Q-V and Q-F_p plots created using the double-sheet charge model with space charge creation via trap-to-band impact ionization.

Figure 4.26 shows sample Q-V and Q-F_p which result when impact ionization is used as the space charge creation mechanism instead of field emission; the simulation parameters used are the same as those in Table 4.2, with the addition that the effective ionization energy of the deep-level trap is specified as $E_{ion} = 2.6$ eV.

The ability of carrier multiplication to account for large capacitance overshoot is demonstrated by the C-V curves shown in Fig. 4.27, in which the solid curve corresponds to the curves in Fig. 4.26. Figure 4.27 again demonstrates the importance of including external circuit elements in the model. As the series resistance R_s is increased from 500 Ω to 1000 Ω and finally 1500 Ω in Fig. 4.27, the observed C-V overshoot increases dramatically.

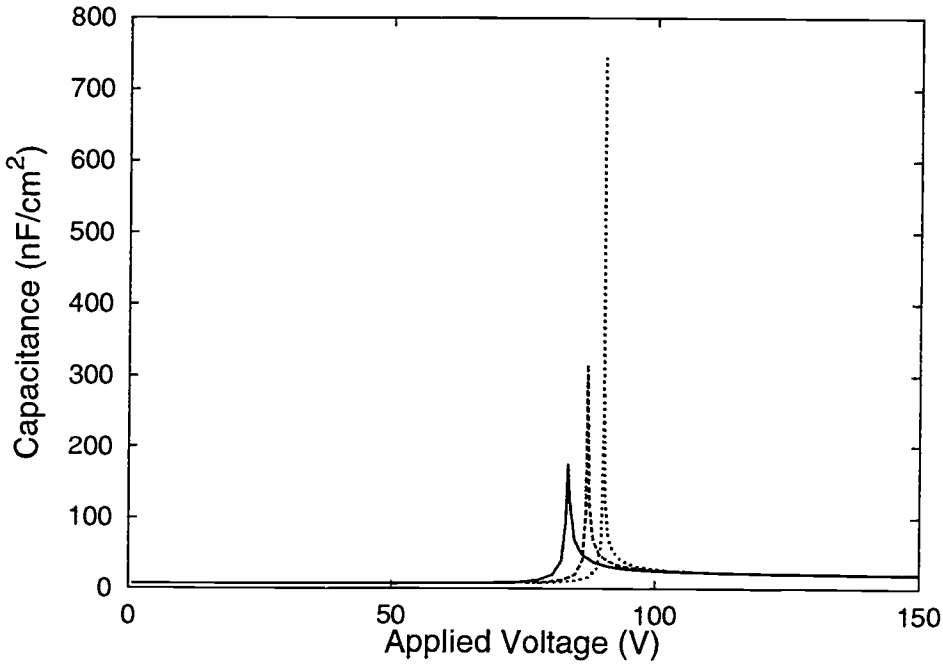

Figure 4.27: C-V curves generated using the double-sheet charge model with trap-to-band impact ionization showing the effect of the series resistance R_s value on the observed C-V overshoot. The values of R_s used are 500 Ω (solid line), 1000 Ω (dashed line), and 1500 Ω (dotted line).

The reason for the ability of the trap-to-band impact ionization mechanism to produce such dramatic amounts of overshoot as well as its sensitivity to the series resistance value, as compared to the field emission model, is seen in the occupancy curves of Fig. 4.28. By comparison with Fig. 4.13, which showed the same curves for the field emission case, it is clear that the emission of charge due to carrier multiplication is much more sudden than for field emission; more charge is emitted in a shorter time period.

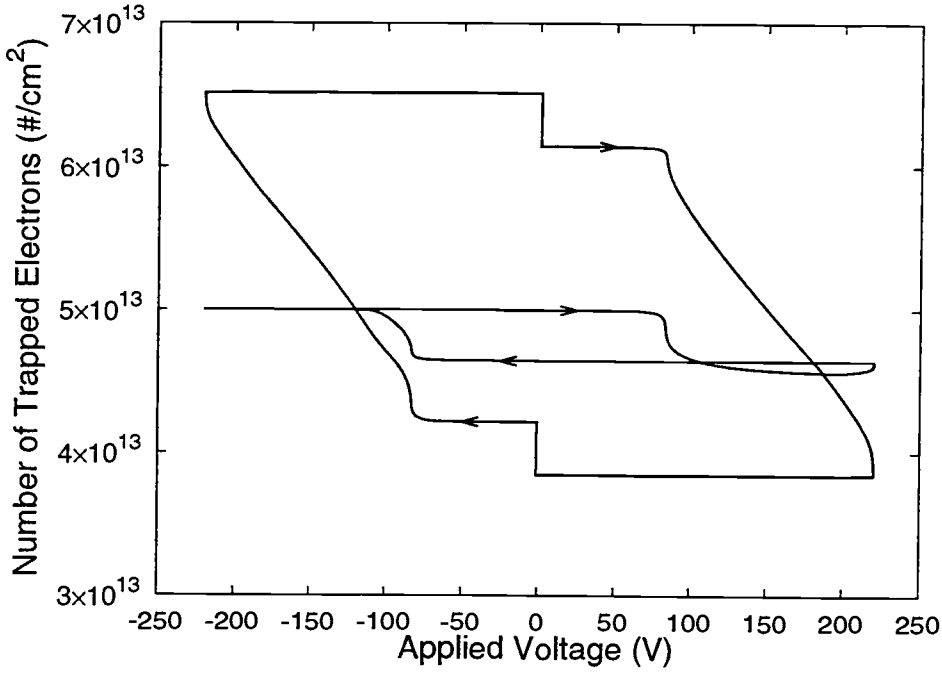

Figure 4.28: Plot showing the occupancy of the bottom insulator-phosphor interface and the first sheet of charge for the double-sheet charge model with trap-to-band impact ionization.

4.5 Summary

This chapter presents the simulation result for each of the models developed in the previous chapter. For each model, example data are presented which illustrate the capabilities of the model. Then, the parameter set of the models is explored and the effect of parametric variation is illustrated.

5. SIMULATING OLEDS IN SPICE

This chapter describes simple SPICE modeling of organic light-emitting devices (OLEDs) and polymer light-emitting devices (PLEDs). The chapter begins with a brief overview of the OLED technology. Then, a short literature review is conducted, with an focus on the relevant device structures. Finally, several simple SPICE models for various OLEDs and PLEDs are developed and then simulation results are demonstrated.

5.1 Organic Light-Emitting Devices

Organic light-emitting devices (OLEDs) have increasingly attracted attention in recent years as an efficient and inexpensive alternative for full-color displays. [42, 43] OLEDs offer many of the advantages of ACTFEL technology, such as wide viewing angle, but have the added advantages inherent of direct injection devices. Specifically, dc voltage excitation can be used instead of ac, and only modest driving voltages are required ($\sim$ 10 V). Furthermore, the number of organic molecules potentially suitable as phosphor materials is considerable, and the color of the emitted light is relatively easily customized via the addition of dyes to the phosphor layer. [44] The nature of the organic materials also makes it possible to deposit the devices on a wide variety of substrate materials, including flexible plastics. The main drawback to the technology has been the short lifetime of the devices, which are susceptible to moisture-induced degradation and rapid brightness degradation with aging.

5.2 OLED Device Structures

OLEDs can be roughly classified into one of two general categories. The first to appear, historically, are the small-molecule or heterojunction OLEDs. The multilayer OLED to be modeled in this chapter was manufactured by the Eastman-Kodak Company [45] and is shown in Fig. 5.1. Each device consists of a glass substrate coated

with a transparent indium-tin-oxide (ITO) anode, on which a copper phthalocyanine (CuPc) hole injection layer (HIL), a naphthyl-substituted benzidine derivative (NPB) hole transport layer (HTL), and an 8-tris-hydroxyquinoline aluminum (Alq_3) electron transport layer (ETL) are vapor-deposited. The top layer is a Mg cathode which has been doped with $\sim$ 10% Ag in order to reduce degradation due to moisture-induced oxidation of the Mg metal.

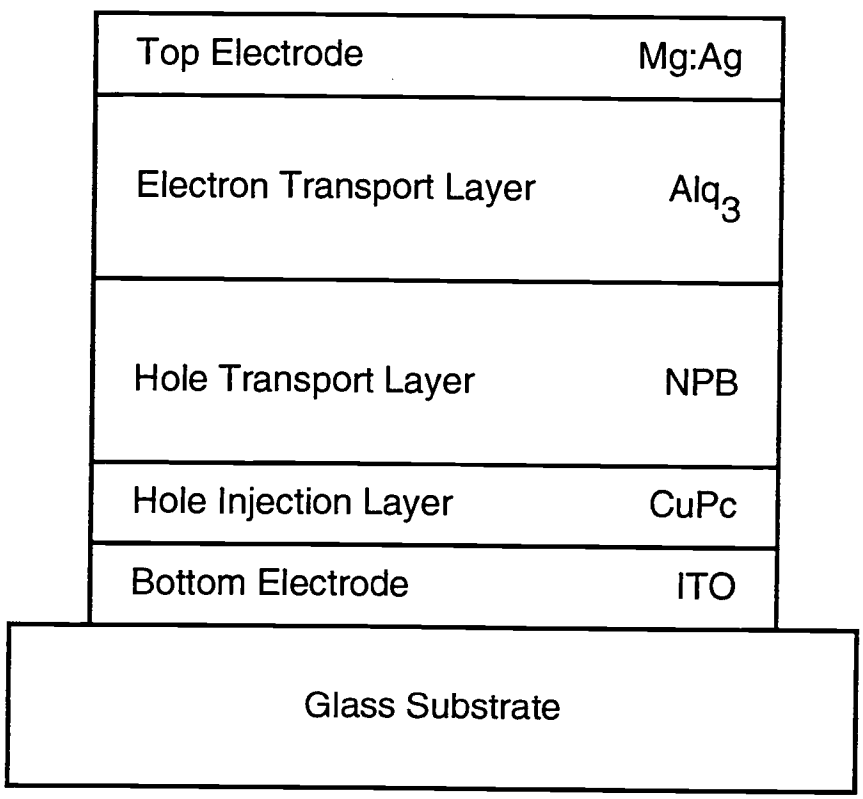

Figure 5.1: OLED device structure.

Recently, an increasing amount of research interest has been focused on another class of organic light-emitting devices, termed polymer light-emitting devices (PLEDs). PLEDs are structurally somewhat simpler than the small-molecule OLEDs, consisting of only one polymeric phosphor layer. The PLED used experimentally in

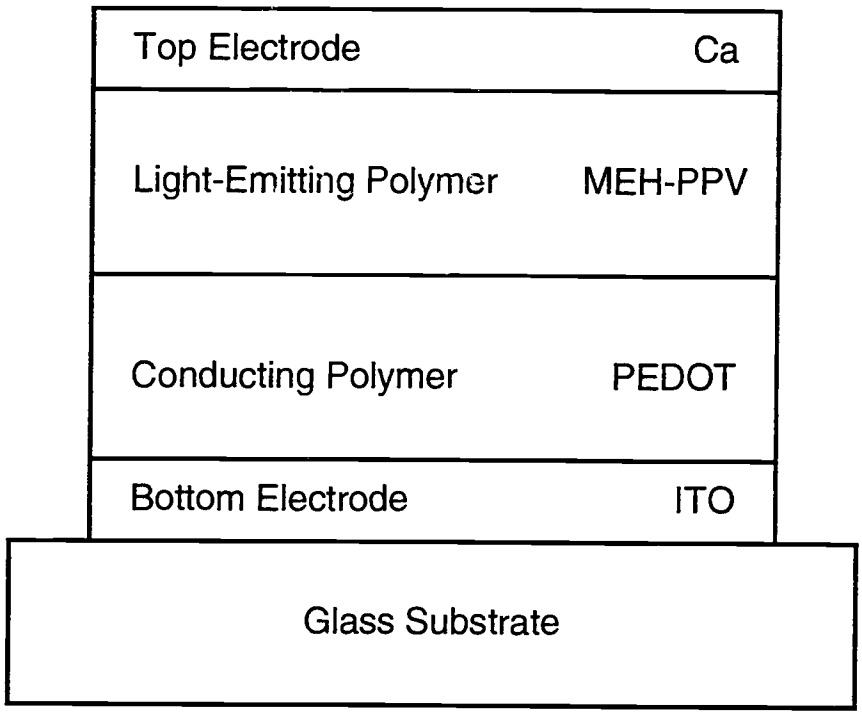

Figure 5.2: PLED device structure.

this chapter was manufactured by the UNIAX Corporation. The structure of a typical PLED is shown in Fig. 5.2. The anode is again ITO deposited on glass, although a conductive polymer is also deposited on top of the ITO contact. The polymer phosphor layer is poly(2-methoxy,5-(2′-ethyl-hexyloxy)-1,4-phenylene vinylene) (MEH-PPV), and finally a Ca cathode is deposited as the top contact.

5.3 OLED Operation

Figure 5.3 shows an energy band diagram of an OLED under forward bias and the most important processes which occur at applied potentials greater than the threshold voltage. The basic operation of the device can be understood as follows. Process (1) in Fig. 5.3 shows the direct injection of electrons into the ETL and the injection of holes into the HTL. Process (2) shows the subsequent transport of carriers across their respective regions in the device. As holes reach the ETL/HTL interface,

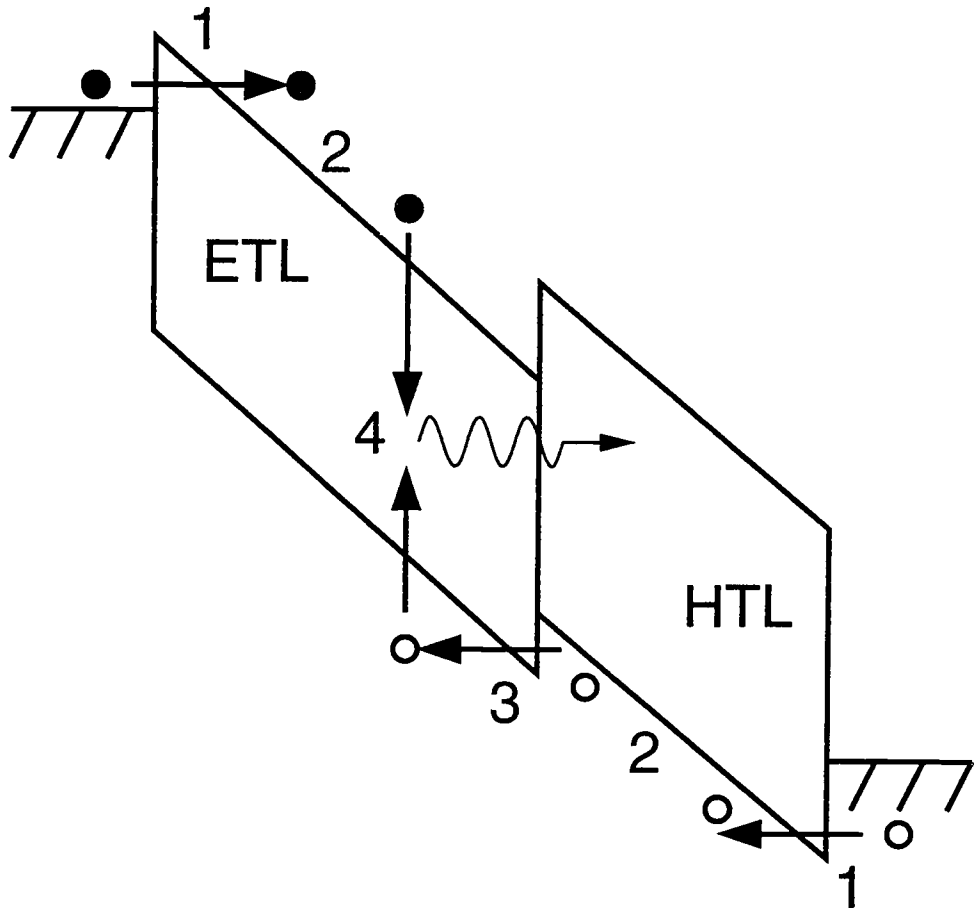

Figure 5.3: Idealized representation of the most basic processes which occur inside an OLED under forward bias. Shown: (1) electrons and holes are injected into the ETL and HTL, respectively, and (2) are transported across each region; then (3) holes are injected from the HTL into the ETL, where (4) the electrons and holes recombine to emit light.

they must overcome a small energy barrier to be injected into the ETL, as shown in process (3). Electrons are largely confined to the ETL side of the device and are not likewise injected into the HTL. Finally, process (4) shows an electron and hole recombining near the ETL/HTL interface and emitting light.

Thus, unlike ACTFEL devices, which are capacitively-coupled devices and therefore require the use of an ac driving waveform, OLEDs are direct-injection devices and may be driven by dc excitation. However, there are several reasons why ac excitation may be desired. First, the aging behavior of the devices may be improved

when devices are subject to reverse as well as forward bias operation. [45] Second, the use of ac voltage excitation is useful from an experimental point of view, since several experimentally-observable phenomena, such as charge storage effects, are not apparent from dc measurements.

The OLED SPICE models are developed using data taken from experiments in which OLEDs are subjected to both dc and ac voltage excitation. The experimental setup is very similar to that in Fig. 2.8 used for ACTFEL characterization, except that the sense element C_s is replaced by a resistor, the amplifier is a low-voltage single 751 operational amplifier, and the series resistance R_s is no longer needed since high voltages are not used. For both ac and dc analysis, the current through the sense resistor is measured versus the voltage applied across the device. The ac experimental data is derived using steady-state transient voltage-transient current [i(t)-v(t)] analysis. [46] In this type of experiment, an OLED is driven by a bipolar piece-wise linear voltage waveform similar to that shown in Fig. 2.2, although V_{max} is on the order of 10 V and the rise/fall times and the plateau width are generally longer for OLED characterization than for ACTFEL characterization. Also, in OLED characterization, the interpulse interval between points E and F in Fig. 2.2 is set to zero, so that the voltage decreases linearly from the maximum at point D to the minimum at point F.

5.4 Small-Molecule OLED SPICE Modeling

In a manner analogous to the mapping of the single-sheet charge ACTFEL structure to a SPICE model in Section 3.3, each individual phosphor layer in the heterojunction OLED is initially modeled as a capacitor shunted by a series combination of a resistor and a diode as shown in Fig. 5.4. The capacitor represents the physical capacitance of the layer; this needs to be included for the modeling of ac excitation. The value of each capacitor is calculated from the thickness of the corresponding layer and the dielectric constant of the organic material (which is assumed

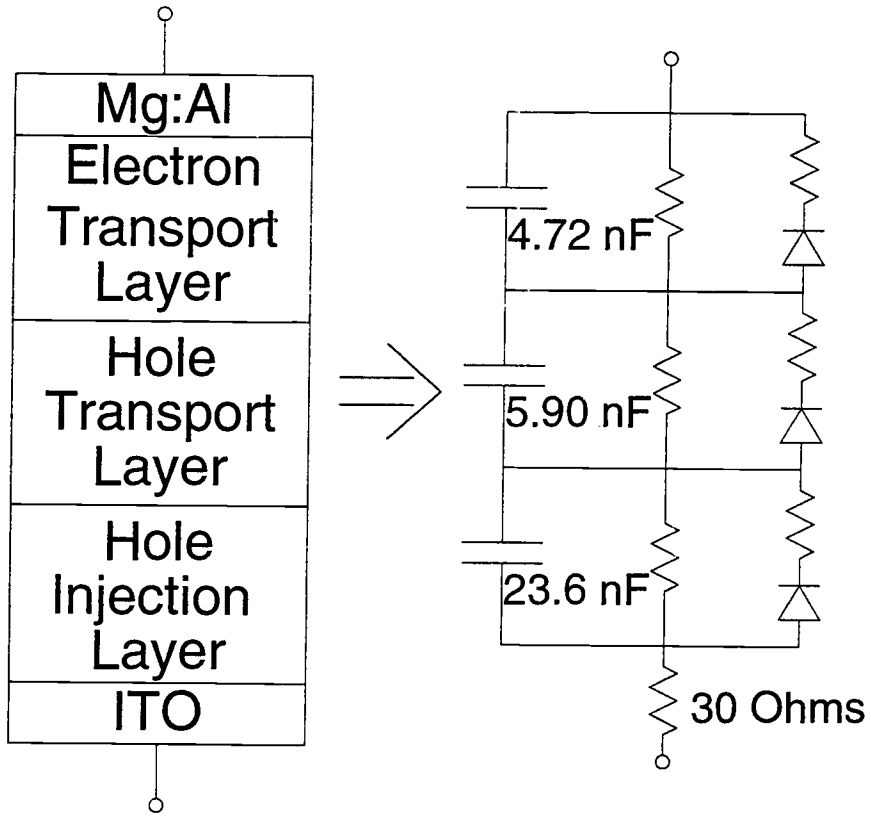

Figure 5.4: OLED SPICE model creating by mapping each layer of the OLED as a parallel combination of a capacitor, pn diode, and resistor.

to be 4). The shunt resistors account for the relatively large bulk series resistance associated with an OLED layer; large series resistances are an inevitable consequence of employing materials with extremely low mobilities. Each diode accounts for the rectifying nature of an individual OLED layer. An additional resistor is placed in series with the stack of modeled layers to account for the sheet resistance of the ITO anode and external resistance.

The parameters of this multiple-diode model can be varied by the HSPICE optimization routine until the fit between simulation data and experimentally measured data is optimal. However, simpler models are able to approximate OLED behavior as well as the more complex multiple-diode model. As shown in Fig. 5.5, a simpler model consists of a capacitor shunted by a diode in series with a resistor. The diode

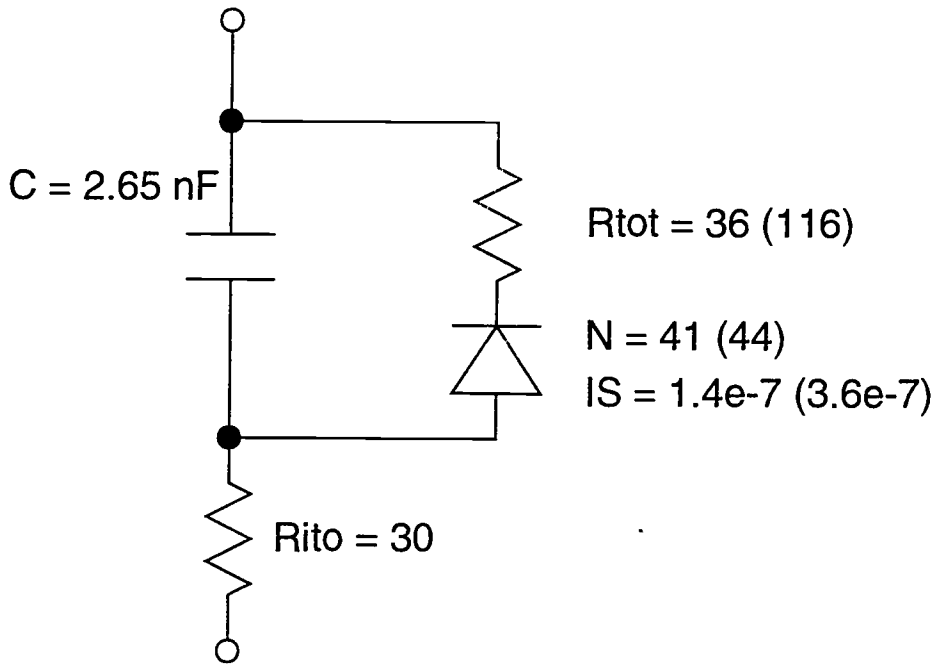

Figure 5.5: A single-diode OLED model consists of a *pn* junction diode in parallel with a capacitor which represents the total device capacitance. A resistor is added in series with this combination to account for the ITO sheet resistance. The values shown are the DC best-fit parameter values, followed by the AC best-fit parameter values in parentheses.

now represents the total rectified current flow in an OLED, the capacitor is the total OLED stack capacitance, and the shunt resistor accounts for the total bulk resistance of all the OLED layers. Again, the parallel combination of the diode and resistor and the capacitor is placed in series with a resistor which accounts for the ITO sheet resistance.

The diode and shunt capacitor model is characterized by five parameters: the diode ideality factor, N; the diode reverse saturation current, IS; the total 'bulk resistance,' R_{tot}; the total device capacitance, C_t; and the series resistance R_{ITO}. Of these, C_t is calculated from the device thickness and dielectric constants, and R_{ITO} is specified as a reasonable value, leaving three parameters for HSPICE to fit simulated to experimental data using a least-squares curve-fitting technique, as described in Section 2.4.4. The model is first fit to dc experimental data, as shown in Fig. 5.6.

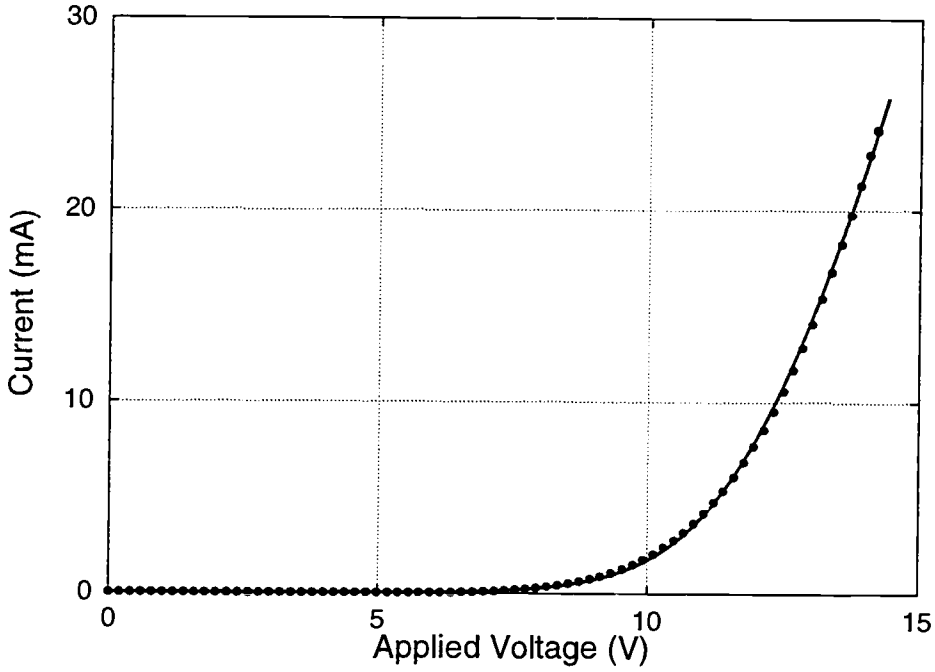

Figure 5.6: Comparison of measured (dots) and SPICE-simulated (solid line) dc current-voltage characteristics of an OLED using a single diode OLED SPICE model for the simulation.

The dc best-fit values of the model parameters are shown in Fig. 5.5; in order to obtain good agreement between experimental and simulated data, it is necessary to use exceedingly large diode ideality factors on the order of $N \sim 40$. (In a two-diode model in which one diode is used to model current flow in each transport layer of the OLED, the best fit to data occurs with $n \sim 15$ for each diode.) These extremely large ideality factors indicate that the charge transport physics is not very realistically accounted for in the *pn* junction diode model, which is based on the drift-diffusion equation. Moreover, these large ideality factors underscore the comparatively low mobility and poor transport properties of the organic layers employed in OLEDs compared to that of single crystal semiconductors.

Once the dc model parameters have been optimized, the dc-fit parameters are modified through a series of optimization simulations to fit experimental i(t)-v(t) data, resulting in the ac fit shown in Fig. 5.7. The fit to the ac data is not as good as

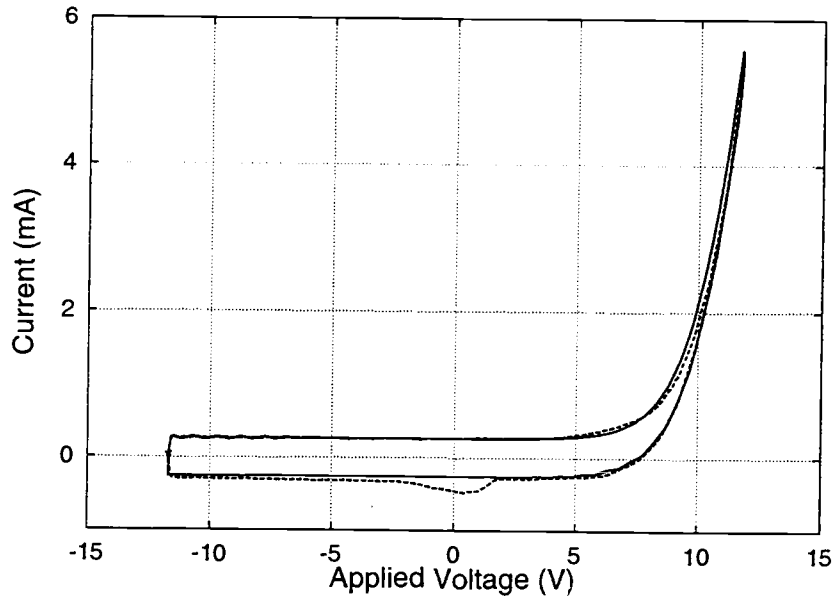

Figure 5.7: Comparison of measured (dashed line) and simulated (solid line) i(t)-v(t) characteristics of an OLED using a single diode OLED SPICE model for the simulation.

for the dc case. Furthermore, the fact that two different sets of parameters are needed for ac and dc modeling underscores a basic inadequacy of the model. This limitation is attributed to the fact that charge trapping and de-trapping are not accounted for in the OLED models. The presence of charge storage via trapping and/or charge accumulation at the heterointerface is evidenced by the presence of a 'bump' near zero volts in the left-going trace of the experimental i(t)-v(t) curve shown in Fig. 5.7. This 'bump' is attributed to trap re-emission. [46] Note that no 'bump' is present in the simulated i(t)-v(t) curve shown in Fig. 5.7 since charge storage is not included in the model.

Current transport in a device can be injection- (contact-) or bulk-limited. In the injection-current-limited regime, the charge transport is limited by the efficiency of carrier injection into a material; this is determined by such factors as the interfacial barrier height. In the bulk-limited regime, the charge transport is limited by the properties of the bulk, such as the presence of space charge or the number and depth

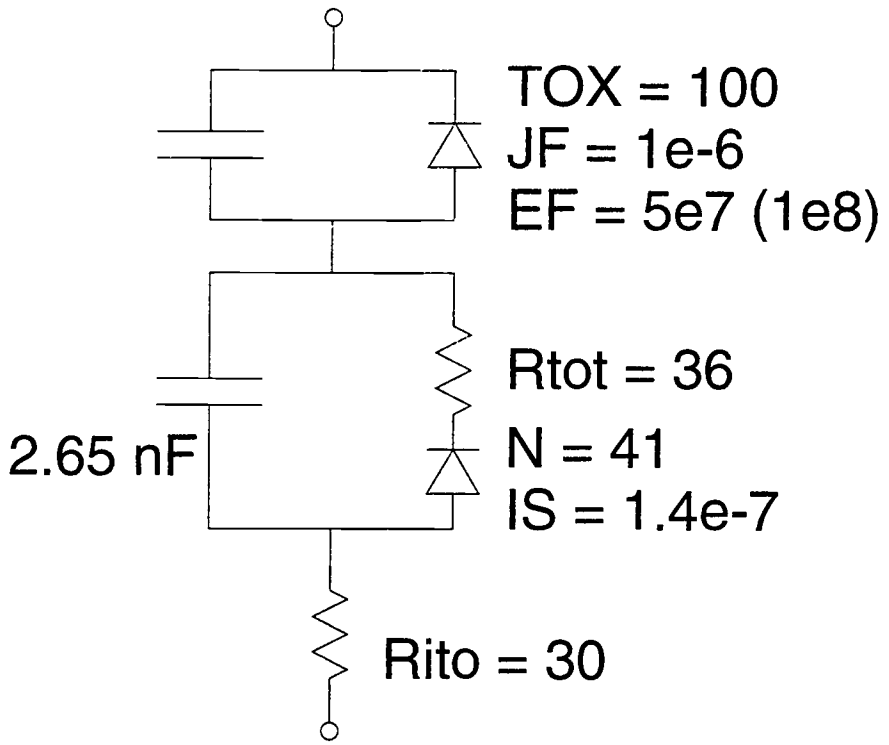

Figure 5.8: Injection-limited OLED model using a Fowler-Nordheim diode. The Fowler-Nordheim diode parameters indicated are employed in the simulation of curves (b) and (c) of Fig. 5.9.

of traps. A simple model accounting for both regimes of operation in an OLED has been created using SPICE.

The simulation model shown in Fig. 5.5 corresponds to bulk-limited transport since the large ideality factor used in the SPICE model approximates the power-law dependence of current on voltage exhibited by trapped-charge-limited conduction. [43] Next, in order to illustrate injection-limited OLED operation, a Fowler-Nordheim diode is added to the model, as shown in Fig. 5.8, to simulate tunnel injection of charge into the OLED. Using "reasonable" Fowler-Nordheim parameters (TOX=10 nm, JF=1×10^{-6} A/V^2, EF=1 MV/cm) no change is visible in the simulated DC I-V curve shown in Fig. 5.9(a). However, by increasing either the critical field, EF, or oxide thickness parameter, TOX, the current level at a given voltage is reduced so that the OLED operates in an injection-limited regime, as shown in

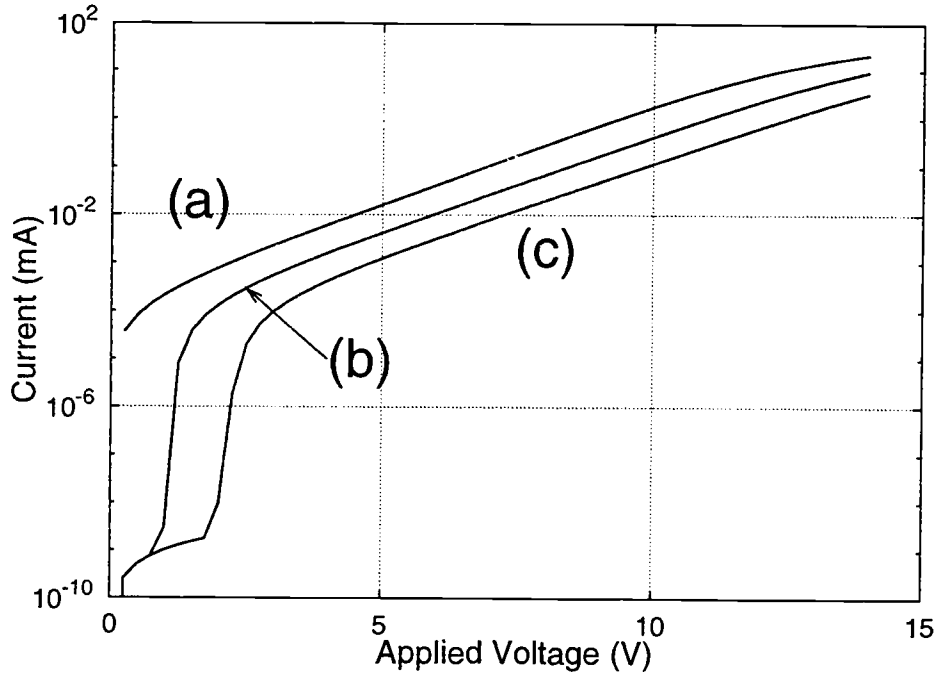

Figure 5.9: Simulated DC I-V characteristics illustrating (a) bulk-limited and (b, c) interface-limited conduction. Curve (a) is simulated using the single diode OLED SPICE model. Curves (b) and (c) are simulated using the injection-limited (Fowler-Nordheim diode) OLED model and choosing the critical field as 5×10^7 and 1×10^8 V/cm for (b) and (c), respectively.

curves (b) and (c) of Fig. 5.9. Thus, both injection-limited and bulk-limited OLED operation can be modeled using SPICE simulation. Curve (b) of Fig. 5.9 is replotted as curve (c) in Fig. 5.10 along with the current-voltage trends of the Fowler-Nordheim diode interface and pn diode bulk sections of the model plotted separately as curves (a) and (b), respectively. This figure demonstrates that the total I-V characteristic is dominated by the Fowler-Nordheim interface at low voltages and the pn diode at higher voltages.

5.5 PLED Modeling

A dc model for PLEDs is developed as follows. First, a dc I-V curve is experimentally measured. The I-V curve is shifted to the left by subtracting a constant

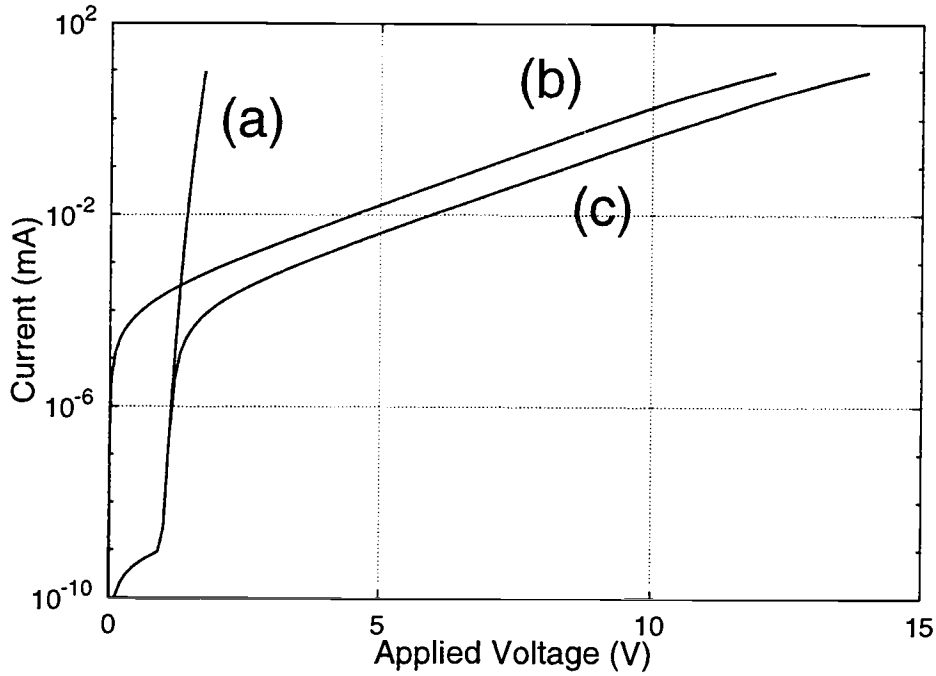

Figure 5.10: Simulated DC I-V characteristic of Fig. 5.9(b) showing current plotted against the voltage across (a) the Fowler-Nordheim interface, (b) the pn diode-resistor shunt branch, and (c) the entire model.

value from the voltage data, so that the resulting shifted curve has a threshold voltage approximately the same as that of a *pn* diode, as shown in Fig. 5.11. A least-squares technique is used to fit this shifted data set to the Shockley diode equation,

$$I = I_0 \left[\exp\left(\frac{V_d}{nV_t} - 1 \right) \right], \tag{5.1}$$

where I is the diode current, I_0 is the reverse saturation current, V_d is the diode voltage, n is the ideality factor, and V_t is the thermal voltage. The model shown in Fig. 5.12 then uses these best-fit values as the diode parameters, where the dc voltage source accounts for the voltage shift performed on the data. Another, SPICE-based optimization simulation is run to tune the model parameters, which are not optimal due to the incorporation of the series resistance in Fig. 5.12. The resulting model output is shown by the dashed line in Fig. 5.11.

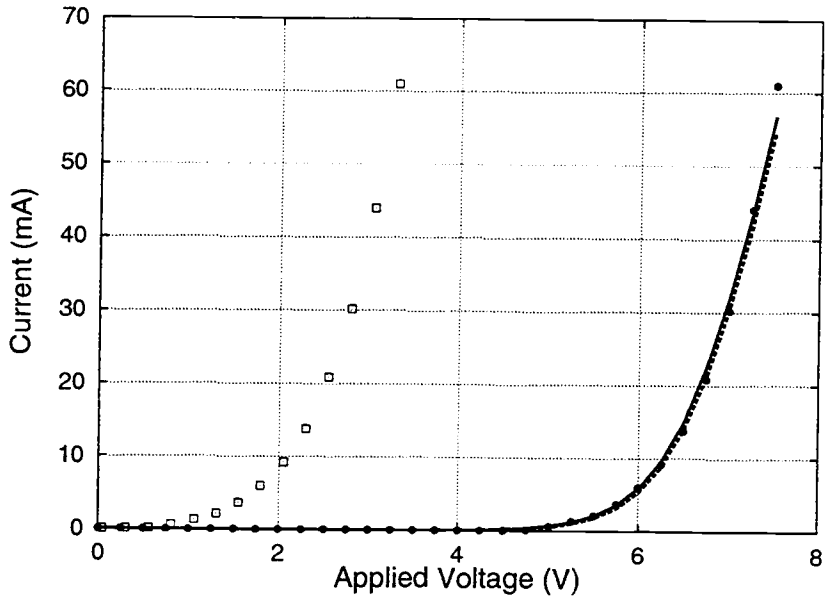

Figure 5.11: Comparison of experimental (dots) and simulated (lines) dc current-voltage characteristics of a PLED. The solid dots are the experimentally measured characteristic, while the open squares show the shifted characteristic used to determine the best-fit SPICE model parameters. The dashed line results from the offset model, and the solid line results from the model resulting from Eq. 5.7.

This model is undesirable for two reasons. First, the shifted I-V characteristic of the diode leads to reverse conduction at positive applied voltages. Second, the addition of a source is an added layer of model complexity. To eliminate the source, as in the small molecule OLED model shown in Fig. 5.5, we can incorporate the voltage offset into the *pn* diode model. Begin with the Shockley diode equation:

$$I = I_0 \left[\exp\left(\frac{V_d}{nV_t} - 1 \right) \right]. \tag{5.2}$$

Solving for voltage and assuming the -1 factor is negligible,

$$V_d = nV_t \ln\left(\frac{I}{I_0} \right) \tag{5.3}$$

The offset voltage is added to each side, giving

$$V_d + \Delta V = nV_t \ln\left(\frac{I}{I_0} \right) + \Delta V \tag{5.4}$$

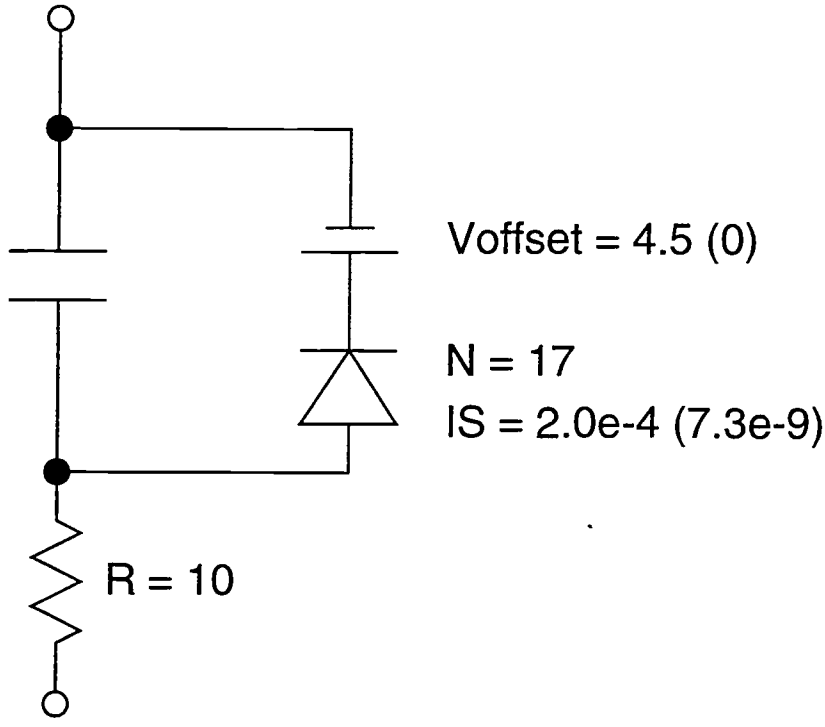

Figure 5.12: A PLED model which uses a voltage source to shift the I-V characteristics towards higher applied voltages. The voltage source can be eliminated if the reverse saturation current is altered to incorporate the voltage shift.

If the offset voltage is assumed to be of the form

$$\Delta V = nV_t \ln(K), \tag{5.5}$$

then

$$V_d + \Delta V = nV_t \ln\left(\frac{I}{I_0 K^{-1}}\right). \tag{5.6}$$

Therefore, the voltage shift ΔV is realized by changing I_0 (IS in SPICE) by a factor of K^{-1}, where K is determined through the solution of Eq. 5.5 for the relevant voltage shift, ideality factor, and temperature. For the model above, we then have

$$IS = I_0 \left[\exp\left(\frac{\Delta V}{nV_t}\right)\right]^{-1} \tag{5.7}$$

$$= (2.0\times10^{-4}) \left[\exp\left(\frac{4.5}{17\cdot0.0259}\right)\right]^{-1} \tag{5.8}$$

$$= 7.3\times10^{-9} \tag{5.9}$$

This value of IS is used in the model shown in Fig. 5.12 with the voltage offset set to 0, resulting in the solid line in the dc I-V curve shown in Fig. 5.11.

5.6 Summary

This chapter begins with a description of basic OLED and PLED organic light emitting diode structures and idealized operation. Next, a simple model using standard SPICE components is presented which accounts for dc OLED operation, and it is shown that the model can be made to be either injection- or bulk-limited through the addition of a Fowler-Nordheim diode. Finally, a basic PLED model is presented which accounts for PLED electrical trends.

6. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

This chapter summarizes the major accomplishments demonstrated in this thesis and provides some suggestions for future work.

6.1 Achievements

A major achievement of this thesis is the demonstration of a very simple ACTFEL SPICE model which nonetheless models the behavior of the most industrially important ACTFEL devices, those with evaporated ZnS:Mn phosphors. The basic Fowler-Nordheim model was shown to accurately match experimental data for a particular maximum applied voltage, using a limited parameter set. Furthermore, a procedure for determining these few parameters to fit a particular device's performance was outlined, so that only a few electrical experiments need be run to entirely specify the model. It was also shown how the model could be made more accurate over a range of maximum applied voltages by exponentially varying the interfacial trap depth.

A significant accomplishment achieved in this thesis is the elimination of three of the "Recommendations for Future Work" with regard to SPICE modeling given at the end of Keir's Master's Thesis. [5] Specifically, these are the extension and simplification of the SPICE model presented by Keir, and also the incorporation of trap-to-band impact ionization as a space charge creation process. First, the single-sheet charge ACTFEL SPICE model was extended to include features of the earlier device physics-based simulations which were excluded from the original single-sheet SPICE model, such as the inclusion of field- and trap occupancy-limited space charge capture factors. This model was then extended into a full double-sheet charge model which incorporates the full functionality of the field emission models presented by Keir and Bouchard [8], with the exception of phonon-assisted tunneling as an emission mechanism. The model was used to investigate a number of experimentally ob-

served behaviors. Methods of simplifying the model in SPICE, leading to improved simulation time while still producing useful transient current-voltage characteristics, were investigated. These include altering the number of simulation cycles that need be run, changing the convergence requirements in SPICE, eliminating current sources that are not necessary to model operation, eliminating thermal emission as generally unimportant, and modifying the complexity of the space charge capture factor formulation. Finally, trap-to-band impact ionization as a space charge creation mechanism was added to the double-sheet SPICE model. With this addition, the SPICE models are able to incorporate almost all of the features included in the device physics models of Keir and Bouchard (the notable exception is band-to-band impact ionization).

The last chapter of this thesis presents several SPICE circuits which can be used to model the current-voltage characteristics of OLEDs and PLEDs. For OLEDs, a simple model has been presented which accurately reproduces the dc current-voltage characteristics, and a possible way of modeling injection-limited behavior of OLEDs was demonstrated. A procedure for the modeling of PLEDs was outlined and shown to reproduce dc I-V trends very well.

6.2 Recommendations for Future Work

The Fowler-Nordheim model should be made to reflect changes in frequency as well as maximum applied voltage. Devices should be characterized at a number of different frequencies and the model parameters varied as a suitable function of frequency, similar to the function of maximum applied voltage by which they are already modified.

Next, a subcircuit should be incorporated into the model, similar to Douglas' optical SPICE model, which would model the light output of the ACTFEL device.

With the frequency-dependence and optical model done, hopefully a procedure can be established in which a researcher can take two or three electrical tests and

use these to characterize the model, which would then be able to accurately predict device electrical and optical behavior under different conditions.

With regard to the double-sheet ACTFEL SPICE model, some suggestions for future work are as follows:

First, an effort should be made to incorporate the last two suggestions remaining from Keir's Master's Thesis. An optical SPICE model for ACTFEL devices exhibiting space charge should be created. This could be done using a current source whose current characteristics are controlled by the field, number of luminescent impurities, and the amount of current present in each phosphor region, and governed by appropriate relationships among these three quantities. Phonon-assisted tunneling could also be added as an emission mechanism through the incorporation of an external program which produces a look-up table for use in the SPICE model. Also, a better method of modeling the leakage charge should be implemented. At present, a simple resistor is used to shunt the top and bottom phosphor-insulator interfaces to augment the very modest leakage seen as a result of the current sources; the value of the resistor must be adjusted for different frequencies and is not representative of a reasonable physical process. Furthermore, recombination of leakage charge with ionized bulk traps is not modeled.

OLED modeling has perhaps the greatest potential for future work. Several suggestions for this are listed below:

State-space modeling [35] should be attempted for OLEDs and PLEDs; the dc nature of the devices and the relative ease with which elements like resistors are added in the state-space approach make this the obvious choice over other device-physics methodologies.

An effort should be made to model multi-pixel OLED/PLED displays in SPICE, either using models similar to those presented in Chapter 5 or more advanced models which fall out of the device-physics modeling effort. The ultimate point of SPICE modeling is to enable circuit engineers to design the product for manufacture, and

to this end the electrical behavior of the OLED pixels and their interactions with neighboring pixels should be modeled. [26, 47]

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APPENDICES

A. SPICE INPUT FILE FOR THE BASIC FOWLER-NORDHEIM ACTFEL MODEL

```
Transient SPICE Model of a TFEL ZnS:Mn device
* The model makes use of a Fowler-Nordheim tunneling diode to
* simulate charge injection into the device.  This SPICE file
* transforms device physics parameters into the SPICE FN diode
* parameters.
*
* Jeff Bender
* Department of Computer and Electrical Engineering
* Oregon State University
* Corvallis, OR 97331
*
* Original File
*   December 9, 1998     -- pp. 38-40 in lab notebook
* Many changes up to now
*      - added top and bottom insulators, instead of just one lumped
*        capacitance (doesn't matter here, but changed to be
*        consistant with sheet-charge models, offset-producing
*        models, etc.)
*      - insulators shunted by 100MEG resistors, not 10MEG; important
*        at 60 Hz
*      - added '.OPTION accurate' to improve C-V smoothness
*      - restructured output statements
*      - added 60 Hz waveform
*      - etc.
*   September 9, 1999
*
.OPTIONS
+ post                          $ enable post-processing
+ brief                         $ don't repeat source
+ ingold=1                      $ exponential output format
+ badchr                        $ warn about unprintable chars
+ co=132                        $ wide output
+ accurate
*
*Driving Waveform
*
*.PARAM d1=8293.3e-06 rise=5e-06 pw=30e-6 d2=8293.3e-6 mag=196 $60 Hz
.PARAM d1=460e-6 rise=5e-06 pw=30e-06 d2=460e-6 mag=242.5    $1000 Hz
.PARAM T='d1+4*rise+d2+2*pw'     * waveform period
Vdev Va 0 PWL (0 0 'rise' 'mag' 'rise+pw' 'mag' '2*rise+pw' 0
+ '2*rise+pw+d1' 0 '3*rise+pw+d1' '-mag' '3*rise+2*pw+d1' '-mag'
```

```
+ '4*rise+2*pw+d1' 0 'T' 0 R 0)

*
* Components
*
Rseries Va  Va2 Rseries
Ci1 Va2 1   'ci*2'
Ri1 Va2 1   100MEG
Dp1 1   4   DMOD W=W L=L
Rp1 1   4   .65MEG
Ci2 4   3   'ci*2'
Ri2 4   3   100MEG
Cs  3   0   cs
Rs  3   0   10MEG

.MODEL  DMOD    D LEVEL=2 TOX=TOX JF=JF JR=JF EF=EF ER=EF

* CIRCUIT PARAMETERS
.param ci   = 'ci_p*1e-9*a_p*10000'      $ insulator capacitance (F)
.param cs   = 109.0n                     $ sense capacitance (F)
.param cp_p = '(eox_p*8.8514e-14)*(1e9)/(tox_p*100)'    $ phosphor c>
    <apacitance (nF/cm^2)
.param Rseries  = 500   $ series resistance (Ohms)

* PHYSICAL CONSTANTS
.param mo = 9.108e-31       $ electronic mass (kg)
.param pi = 3.14159         $ pi...
.param q = 1.602e-19        $ electronic charge (C)
.param h = 6.625e-34        $ Planck's constant (J-s)
.param eo = 8.8514e-12      $ permittivity of free space (F/m)
.param h_bar = 1.054e-34    $ Planck's constant / 2pi (J-s)

*****************************************************************
* DEVICE PARAMETERS
*****************************************************************
.param m_r = 0.18       $ carrier effective mass relative to mo
.param phi_b = 1.03     $ injection barrier height (V)
.param tox_p = 6439e-10 $ phosphor thickness (m)
.param eox_p = 8.3      $ phosphor relative dielectric constant
.param a_p = 8.5e-6     $ physical device area (m^2)
.param ci_p = 18.05     $ total insulator capacitance (nF/cm^2)
*****************************************************************
* LUMPED DEVICE PARAMETERS
.param m_star = 'm_r*mo'        $ carrier effective mass (kg)
.param EF_p = '((4/3)*1e15/q)*sqrt(2*m_star)*pwr(q*phi_b,1.5)/(h_bar>
    <*1e15)' $ V/m
```

```
.param JF_p = '(1/m_r)*q*1e15*q/(16*pi*pi*phi_b*(1e15*h_bar))'      >
    <    $ A^2/V^2
.param AREA = '(eox_p/3.9)*a_p' $ m^2

* SPICE FN DIODE PARAMETERS
.param EF = 'EF_p/100'          $ V/cm
.param JF = '(3.9/eox_p)*JF_p'  $ A^2/V^2
.param TOX = 'tox_p*(1e10)'     $ Angstroms
.param W = 'sqrt(AREA)'         $ m
.param L = 'W'                  $ m

.DC vdev 0 1 2

.PRINT DC jf=PAR('JF'), ef=PAR('EF'), area=PAR('AREA'),
+ cpp=PAR('cp_p')

*.TRAN  .2U '5*T'   '4*T'
*.TRAN  .1U '3*T'   '2*T'

.TRAN .1U 'T' .1U '2*T'.1U '2*T+2*rise+pw+10U' 10U '2*T+2*rise+pw+d1'
+ .1U '2*T+4*rise+2*pw+d1+10U' 10U '3*T' START='2*T'

.MEASURE TRAN Vmax FIND V(Va2,3) AT='2*T+rise+pw'
.MEASURE TRAN Vcsmax FIND V(3,0) AT='2*T+rise+pw'

.PRINT TRAN
+ Vapp=PAR('V(Va2,3)')          $ voltage applied accross device (V)
+ qe=PAR('V(3,0)*cs*1MEG/(a_p*10000)')  $ external charge (uF/cm^2)
+ qi=PAR('((ci_p+cp_p)/ci_p)*V(3,0)*cs*1MEG/(a_p*10000) - cp_p*V(Va2>
    <,3)/1000')  $ internal charge (uF/cm^2)
+ fp=PAR('(1/(tox_p*100))*((cs/ci)*V(3,0) - V(Va2,3))/1e6')     $ ph>
    <osphor field (MV/cm)
+ ia=PAR('V(Va,Va2)/Rseries')
*
.END
```

B. SPICE INPUT FILE FOR THE TWO-SHEET CHARGE ACTFEL MODEL

```
Transient SPICE Model of a TFEL device
* The model uses user-defined voltage-controlled current sources to
* simulate charge injection into the device as well as space
* charge creation via field emission.  The space charge is confined
* to two sheets of charge within the phosphor layer.
*
* Jeff Bender
* Department of Computer and Electrical Engineering
* Oregon State University
* Corvallis, OR 97331
*
* File created, modeled after earlier FN model files
*  October 31, 1999 -- All Hallow's Eve --
* Added thermal emission
*  November 15, 1999
* Added sheet of charge
*  - charge available at sc1
*  - pure tunnel emission from sc1
*  November 28-29, 1999
* Added second sheet of charge
*  - simplest 6 source model
*  December 23, 1999
* Added two more sources for refilling sc traps from opposite sc
*   emission
* Added limitation on refilling sheets of charge.
*  December 28, 1999
* Added remaining sources for full 12-current source model
*  January 14, Y2K

.OPTIONS
+ post                    $ enable post-processing
+ brief                   $ don't repeat source
+ ingold=1                $ exponential output format
+ badchr
+ co=132
+ accurate

* USER-DEFINED FUNCTIONS
.param u(x)='(abs(x)+x)/(2*x+1e-30)'          * unit step, u(0)=0
.param ue(x)='(abs(x)+x+1e-30)/(2*x+1e-30)' * unit step, u(0)=1
```

```
**
* EMISSION PARAMETERS
**
** Pure tunneling prefactors
*.param pfPT = 'q/sqrt(32*m0*q)'       $ constant tunneling prefactor
.param pfPT = 74139                    $ evaluated constant
.param pfPTi = 'pfPT/sqrt(m_r*phi_b)'  $ interface tunneling prefact>
    <or
.param pfPT1 = 'pfPT/sqrt(m_r*phi_b1)' $ sc1 tunneling prefactor

** Pure tunneling / PAT exponential factor
*.param ef = '4*sqrt(2*m0*q)/(3*h_bar)'   $ constant tunneling exp. >
    <factor
.param ef = 6.8337e9                     $ evaluated constant
.param efi = 'ef*sqrt(m_r*phi_b)*phi_b'   $ interface tunneling exp.>
    < factor
.param ef1 = 'ef*sqrt(m_r*phi_b1)*phi_b1' $ sc1 tunneling exp. factor

** Coulombic Barrier Lowering
*.param cblf = 'sqrt(q/(pi*e0))'          $ constant CBL factor
.param cblf = 7.5895e-5                   $ evaluated constant
.param cblfi = 'cblf/(sqrt(erp)*phi_b)'   $ interface CBL factor
.param cblf1 = 'cblf/(sqrt(erp)*phi_b1)'  $ sc1 CBL factor

** PT emission
.param enptib(vp1) = '(pfPTi*abs(vp1)/dp1)*exp(-efi*dp1/abs(vp1)*(1->
    <pwr(cblfi*sqrt(abs(vp1)/dp1), 5/3)))'
.param enptit(vp3) = '(pfPTi*abs(vp3)/dp3)*exp(-efi*dp3/abs(vp3)*(1->
    <pwr(cblfi*sqrt(abs(vp3)/dp3), 5/3)))'

.param enptsc1it(vp2) = '(pfPT1*abs(vp2)/dp2)*exp(-ef1*dp2/abs(vp2)*>
    <(1-pwr(cblf1*sqrt(abs(vp2)/dp2), 5/3)))'
.param enptsc2ib(vp2) = '(pfPT1*abs(vp2)/dp2)*exp(-ef1*dp2/abs(vp2)*>
    <(1-pwr(cblf1*sqrt(abs(vp2)/dp2), 5/3)))'

.param enptsc2it(vp3) = '(pfPT1*abs(vp3)/dp3)*exp(-ef1*dp3/abs(vp3)*>
    <(1-pwr(cblf1*sqrt(abs(vp3)/dp3), 5/3)))'
.param enptsc1ib(vp1) = '(pfPT1*abs(vp1)/dp1)*exp(-ef1*dp1/abs(vp1)*>
    <(1-pwr(cblf1*sqrt(abs(vp1)/dp1), 5/3)))'

** Thermal emission
.param enthib(vp1) = 'sigma*vth*Nc*exp(-1*(phi_b-cblf*sqrt(abs(vp1)/>
    <(dp1*erp)))/(k*Temp))'
.param enthit(vp3) = 'sigma*vth*Nc*exp(-1*(phi_b-cblf*sqrt(abs(vp3)/>
    <(dp3*erp)))/(k*Temp))'
```

```
** Charge available at interfaces
.param qib(vp1,vib) = 'q*A*N0f0b + cp1*vp1 - cib*vib'
.param qit(vp3,vit) = 'q*A*N0f0t + cit*vit - cp3*vp3'

** Charge available at sc1
.param qsc1(vp2,vp1) = 'q*A*Nt1 + cp2*vp2 - cp1*vp1'
.param qsc2(vp3,vp2) = 'q*A*Nt1 + cp3*vp3 - cp2*vp2'

** Space Charge Capture Factor
** Field-dependent full-trap limited sccf
.param sccf1(vp2,vp1) = '(1 - (abs((vp1/dp1 + vp2/dp2)/(2*f0c)))*((a>
    <bs(1-(abs((vp1/dp1 + vp2/dp2)/(2*f0c))))+1-(abs((vp1/dp1 + vp2/>
    <dp2)/(2*f0c))))/(2*(1-(abs((vp1/dp1 + vp2/dp2)/(2*f0c))))+1e-30>
    <))-(abs((abs((vp1/dp1 + vp2/dp2)/(2*f0c))-1))+(abs((vp1/dp1 + v>
    <p2/dp2)/(2*f0c))-1)+1e-30)/(2*(abs((vp1/dp1 + vp2/dp2)/(2*f0c))>
    <-1)+1e-30))*(1-pwr((q*A*Nt1 + cp2*vp2 - cp1*vp1)/(q*A*Nt1),250)>
    <)'

.param sccf2(vp3,vp2) = '(1 - (abs((vp2/dp2 + vp3/dp3)/(2*f0c)))*((a>
    <bs(1-(abs((vp2/dp2 + vp3/dp3)/(2*f0c))))+1-(abs((vp2/dp2 + vp3/>
    <dp3)/(2*f0c))))/(2*(1-(abs((vp2/dp2 + vp3/dp3)/(2*f0c))))+1e-30>
    <))-(abs((abs((vp2/dp2 + vp3/dp3)/(2*f0c))-1))+(abs((vp2/dp2 + v>
    <p3/dp3)/(2*f0c))-1)+1e-30)/(2*(abs((vp2/dp2 + vp3/dp3)/(2*f0c))>
    <-1)+1e-30))*(1-pwr((q*A*Nt1 + cp3*vp3 - cp2*vp2)/(q*A*Nt1),250)>
    <)'
** Field-dependent sccf
$.param sccf1(vp2,vp1) = '1 - abs((vp1/(2*dp1) + vp2/(2*dp2))/f0c)'
$.param sccf2(vp3,vp2) = '1 - abs((vp2/(2*dp2) + vp3/(2*dp3))/f0c)'
** Full-trap limited sccf
*.param sccf1(vp2,vp1) = '(1-(q*A*Nt1 + cp2*vp2 - cp1*vp1)/(q*A*Nt1)>
    <)'
*.param sccf2(vp3,vp2) = '(1-(q*A*Nt1 + cp3*vp3 - cp2*vp2)/(q*A*Nt1)>
    <)'
** Constant sccf
*.param sccf1(vp2,vp1) = '0.15+vp2*0+vp1*0'
*.param sccf2(vp3,vp2) = '0.15+vp3*0+vp2*0'

**
* Driving Waveform
**
*.PARAM d1=8293.3e-06 rise=5e-06 pw=30e-6 d2=8293.3e-6 mag=196 *60 Hz
.PARAM d1=460e-6 rise=5e-06 pw=30e-06 d2=460e-6 mag=222.5    *1000 Hz
*
.PARAM T='d1+4*rise+d2+2*pw'
Vdev Va 0 PWL (0 0 'rise' 'mag' 'rise+pw' 'mag' '2*rise+pw' 0
+ '2*rise+pw+d1' 0 '3*rise+pw+d1' '-mag' '3*rise+2*pw+d1' '-mag'
```

```
+ '4*rise+2*pw+d1' 0 'T' 0 R 0)

*
* Components
*
Rseries Va  Vap Rseries
Cit Vap it  cit
Rit Vap it  100MEG
Cp1 ib  sc1 cp1
Rp1 ib  sc1 100MEG
Cp2 sc1 sc2 cp2
Rp2 sc1 sc2 100MEG
Cp3 sc2 it  cp3
Rp3 sc2 it  100MEG
Rp  it  ib  .65MEG

* Interface  PT + Thermal Emission
Gibit   it  ib  cur='u(v(sc1,ib))*(1-sccf1(v(sc2,sc1),v(sc1,ib)))*(1>
    <-sccf2(v(it,sc2),v(sc2,sc1)))*qib(v(sc1,ib),v(ib,cs))*(enptib(v>
    <(sc1,ib))+enthib(v(sc1,ib)))'
Gitib   ib  it  cur='u(v(sc2,it))*(1-sccf2(v(it,sc2),v(sc2,sc1)))*(1>
    <-sccf1(v(sc2,sc1),v(sc1,ib)))*qit(v(it,sc2),v(vap,it))*(enptit(>
    <v(sc2,it))+enthit(v(sc2,it)))'

* Charge capture by SC1
Gitsc1  sc1 it  cur='u(v(sc2,it))*(1-sccf2(v(it,sc2),v(sc2,sc1)))*sc>
    <cf1(v(sc2,sc1),v(sc1,ib))*qit(v(it,sc2),v(vap,it))*(enptit(v(sc>
    <2,it))+enthit(v(sc2,it)))'
Gsc2sc1 sc1 sc2 cur='u(v(sc1,sc2))*sccf1(v(sc2,sc1),v(sc1,ib))*qsc2(>
    <v(it,sc2),v(sc2,sc1))*enptsc2ib(v(sc1,sc2))'
Gibsc1  sc1 ib  cur='u(v(sc1,ib))*sccf1(v(sc2,sc1),v(sc1,ib))*qib(v(>
    <sc1,ib),v(ib,cs))*(enptib(v(sc1,ib))+enthib(v(sc1,ib)))'

* Charge capture by SC2
Gibsc2  sc2 ib  cur='u(v(sc1,ib))*(1-sccf1(v(sc2,sc1),v(sc1,ib)))*sc>
    <cf2(v(it,sc2),v(sc2,sc1))*qib(v(sc1,ib),v(ib,cs))*(enptib(v(sc1>
    <,ib))+enthib(v(sc1,ib)))'
Gsc1sc2 sc2 sc1 cur='u(v(sc2,sc1))*sccf2(v(it,sc2),v(sc2,sc1))*qsc1(>
    <v(sc2,sc1),v(sc1,ib))*enptsc1it(v(sc2,sc1))'
Gitsc2  sc2 it  cur='u(v(sc2,it))*sccf2(v(it,sc2),v(sc2,sc1))*qit(v(>
    <it,sc2),v(vap,it))*(enptit(v(sc2,it))+enthit(v(sc2,it)))'

* SC1 PT emission only
Gsc1it  it  sc1 cur='u(v(sc2,sc1))*(1-sccf2(v(it,sc2),v(sc2,sc1)))*q>
    <sc1(v(sc2,sc1),v(sc1,ib))*enptsc1it(v(sc2,sc1))'
Gsc1ib  ib  sc1 cur='u(v(ib,sc1))*qsc1(v(sc2,sc1),v(sc1,ib))*enptsc1>
```

```
    <ib(v(ib,sc1))'

* SC2 PT emission only
Gsc2ib  ib  sc2 cur='u(v(sc1,sc2))*(1-sccf1(v(sc2,sc1),v(sc1,ib)))*q>
    <sc2(v(it,sc2),v(sc2,sc1))*enptsc2ib(v(sc1,sc2))'
Gsc2it  it  sc2 cur='u(v(it,sc2))*qsc2(v(it,sc2),v(sc2,sc1))*enptsc2>
    <it(v(it,sc2))'

Cib ib  cs  cib
Rib ib  cs  100MEG
Cs  cs  0   cs
Rs  cs  0   10MEG

*****************************************

* CIRCUIT PARAMETERS
.param ci   = 'ci_p*1e-9*a*10000'   $ insulator capacitance (F)
.param cs   = 109.0n        $ sense capacitance (F)
.param cp1  = '(erp*e0)*a/dp1'  $ phosphor cap. 1 (F)
.param cp2  = '(erp*e0)*a/dp2'  $ phosphor cap. 2 (F)
.param cp3  = '(erp*e0)*a/dp3'  $ phosphor cap. 3 (F)
.param cit  = 'ci*2'        $ top insulator cap. (F)
.param cib  = 'ci*2'
.param Rseries  = 500           $ series resistance (Ohms)

* PHYSICAL CONSTANTS
.param m0 = 9.108e-31       $ electronic mass (kg)
.param pi = 3.14159     $ pi...
.param q = 1.602e-19        $ electronic charge (C)
.param h = 6.625e-34        $ Planck's constant (J-s)
.param e0 = 8.8514e-12      $ permittivity of free space (F/m)
.param h_bar = 1.054e-34    $ Planck's constant / 2pi (J-s)
.param k = 8.61738e-5       $ Boltzmann constant (eV/K)
*.param vth = 'srqt(3*k*Temp*q/(m0*m_r))'   $ thermal velocity (m/s)
.param vth = '6.74306e3*sqrt(Temp/m_r)'
*.param Nc = '2*pwr(2*pi*q*k*m0*m_r*Temp/pwr(h,2),1.5)' $ effective
.param Nc = '4.8354e21*pwr(Temp*m_r,1.5)' $density of states (#/m^3)

*****************************************************************
* DEVICE PARAMETERS
*****************************************************************
.param m_r = 0.18   $ carrier effective mass relative to mo
.param phi_b = 1.3  $ interface injection barrier height (V)
.param phi_b1 = 1.25    $ sc1 trap depth (V)
.param dp = 6439e-10    $ phosphor thickness (m)
.param dp1 = 500e-10    $ location of charge sheet from ib (m)
```

```
.param dp2 = 5439e-10   $ location of charge sheet 2 from sc1 (m)
.param dp3 = 500e-10    $ location of top interface from sc2 (m)
.param erp = 8.3     $ phosphor relative dielectric constant
.param a = 8.5e-6    $ physical device area (m^2)
.param ci_p = 18.05 $ total insulator capacitance (nF/cm^2)
.param N0f0b = 5e17 $ no field occupancy, bottom interface (#/m^2)
.param N0f0t = 5e17 $                     top interface (#/m^2)
.param Nt1 = 5e17   $                     sc1 (#/m^2)
.param sigma = 1e-18 $ therm. emission e- capture cross section (m^2)
.param Temp = 300    $ temperature (K)
*.param sccf1 = 0.3 $ space charge capture factor, sc1
.param f0c = 200MEG $ critical capture field, V/m
*************************************************************
.param a_p = 'a*10000'          * area, cm^2
.param dp1_p = 'dp1*100'        * phosphor thickness 1, cm
.param cp1_p = '(erp*e0)*(1e5)/(dp1)'   $ phosphor cap. 1 (nF/cm^2)
.param dp2_p = 'dp2*100'        * phoshpor thickness 2, cm
.param cp2_p = '(erp*e0)*(1e5)/(dp2)'   * phosphor cap. 2 (nF/cm^2)
.param dp3_p = 'dp3*100'        * phosphor thickness 3, cm
.param cp3_p = '(erp*e0)*(1e5)/(dp3)'   $ phosphor cap. 3 (nF/cm^2)
.param dp_p = '(dp)*100'        * total phosphor thickness, cm
.param cp_p = '(erp*e0)*(1e5)/(dp)' * total phosphor capacitance
                                *  (nF/cm^2)

.DC vdev 0 1 2

.TRAN  .1U 'T' .1U '2*T'.1U '2*T+2*rise+pw+10U' 10U
+ '2*T+2*rise+pw+d>1' .1U '2*T+4*rise+2*pw+d1+10U' 10U '3*T'
+ START='2*T'
*.TRAN   .1U 'T' .1U 'T+2*rise+pw+10U' 10U 'T+2*rise+pw+d1' .1U
+ 'T+4*rise+2*pw+d1+10U' 10U '2*T' START='T'
*.TRAN  .1U '2*rise+pw+10U' 10U '2*rise+pw+d1' .1U
+ '4*rise+2*pw+d1+10U' 10U 'T'

*.MEASURE TRAN Vmax FIND V(Va2,3) AT='2*T+rise+pw'
*.MEASURE TRAN Vcsmax FIND V(3,0) AT='2*T+rise+pw'

.PRINT TRAN
+ Vapp=PAR('V(Vap,cs)')          $ voltage applied accross device (V)
+ qe=PAR('V(cs,0)*cs*1MEG/(a_p)')   $ external charge (uC/cm^2)
+ qi=PAR('((ci_p+cp_p)/ci_p)*V(cs,0)*cs*1MEG/(a_p) - cp_p*V(Vap,cs)/>
    <1000')  $ internal charge (uC/cm^2)
+ fp=PAR('(1/(1e6*dp_p))*((cs/ci)*V(cs,0) - V(Vap,cs))')            >
    <$ phosphor field (MV/cm)
*+ ia=PAR('V(Va,Vap)/Rseries')
+ qib=PAR('(N0f0b + (cp1*v(sc1,ib) - cib*v(ib,cs))/(q*A))/10000')   >
```

```
    <$ number of e-'s available at bottom interface
+ qsc1=PAR('(Nt1 + (cp2*v(sc2,sc1) - cp1*v(sc1,ib))/(q*A))/10000')  >
    <$ e-'s/cm^2 at sc1
+ qsc2=PAR('(Nt1 + (cp3*v(it,sc2) - cp2*v(sc2,sc1))/(q*A))/10000')  >
    <$ e-'s/cm^2 at sc2
+ sccf1=PAR('sccf1(v(sc2,sc1),v(sc1,ib))')
.END
```