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The focus of this thesis is developing materials for thin-film transistors (TFTs). Cu_3SbS_4 is explored as p-channel layer. Cu_3SbS_4 TFTs show p-type, depletion-mode behavior with a small amount of gate-controlled modulation of the channel conductance. This behavior is consistent with Hall measurements indicating a mobility of 17 $cm^2V^{-1}s^{-1}$ and hole carrier concentration of 10^{17} cm^{-3}. Simulations employing the comprehensive depletion-mode model (CDMM) are used to extract TFT channel interface and bulk mobility, along with carrier concentration. The extracted values from CDMM simulations are in close agreement with Hall-effect measurements of carrier concentration and TFT incremental mobility.

TFTs are fabricated employing solution-processed thin films spin-coated with electrochemically prepared solutions. Dual active-layer TFTs utilizing solution-processed IZTO-IGZO active layers demonstrated the highest average mobility, exceeding that of control sputtered IGZO TFTs.

Sputtered IGZO TFTs are studied using solution-processed Al_2O_3 and $LaAlO_3$ gate insulator layers. The solution-processed Al_2O_3 gate exhibits high subthreshold swing compared to employing a thermally grown SiO_2 gate insulator layer.

Material Development for Thin-film Transistors

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Kevin Alexander Archila, Author

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1. INTRODUCTION

In the 1950s, Jack Kilby and Robert Noyce, working independently at Texas Instruments and Fairchild, respectively, developed the foundations for monolithic integrated circuit (IC) manufacturing, bringing with it the genesis of the information age. The IC, a non-trivial invention, has drastically changed the course of human evolution to the point that modern civilization depends heavily on many indispensable electronics relying on IC technology (e.g., the personal computer). At the core of an IC is a transistor, a three- or four-terminal electronic switching device, which gives an electronic circuit designer the ability to turn on or off current. The transistor allows for the realization of digital logic circuits for computation, which are predominantly designed using complementary metal-oxide-semiconductor (CMOS) technology. At the forefront of high-performance computing in digital circuits is CMOS-based on silicon metal-oxide-semiconductor field-effect transistors (MOSFET). CMOS is a fast, low-cost, and low-power technology that makes use of p-type and n-type MOSFETs to realize digital logic gates used to perform Boolean logic computation.

Large-area electronics and flexible electronics are industries in which silicon MOSFET technology is unsuited. Therefore, this role is more appropriately played by lower-cost and low-temperature manufacturing achieved by thin-film transistor (TFT) technology. A signature application for TFTs proposed by Lechner *et al.* in 1971 is flat-panel displays, an industry segment dominated by TFTs based on hydrogenated amorphous silicon (a-Si:H) [2]. However, the end of the road for a-Si:H is soon approaching (due to its low mobility of < 1 $\mathrm{cm^2V^{-1}s^{-1}}$), as consumer demand for bigger screens with ultra-high definition increases.

Recently, the emergent technology of transparent TFTs (TTFTs) based on amorphous oxide semiconductors (AOS) is disrupting the flat-panel display market by providing high-performance (mobilities > 10 $cm^2V^{-1}s^{-1}$), enabling higher pixel density and low power consumption at low manufacturing costs. However, AOS are intrinsically n-type, and currently there is no p-type AOS solution compatible for high-volume manufacturing which would facilitate development of an AOS-based CMOS-like technology. Organic TFTs are an alternative technology, but the same challenge faced by AOS technology is encountered in an opposite direction: organic materials are strongly p-type with no simple solution to make an n-type organic semiconductor. Moreover, organic materials face more serious limitations, such as poor mobility (< 2 $cm^2V^{-1}s^{-1}$) and poor TFT device stability. Hence, there is a need for the development of p-type inorganic semiconducting materials for TFTs.

We also live in times where the impact of human-induced climate change is alarmingly high and non-renewable energy consumption is unsustainable. The development of sustainable fabrication methods has never been more appealing, not only from a cost-benefit context, but also from an low environmental impact perspective.

The goal of this thesis is to develop p-type inorganic thin-films and TFTs intended for complementary TFT (CTFT) technology, and to contribute to sustainable solution-processed TFT fabrication techniques using innovative chemistry emerging from the Center for Sustainable Materials Chemistry (CSMC).

The organization of this thesis is as follows. Chapter 2 contains a literature review and technical background outline relevant to this work. Chapter 3 presents an overview of the experimental techniques used for this research. Chapter 4 and Chapter 5 summarizes and discusses results of electrical and material characterization of p-type Cu_3SbS_4 and solution-processed TFTs, respectively. Finally, Chapter 6 contains conclusions from experimental results and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

This chapter contains a background relevant to the work presented in this thesis. The first section focuses on thin-film transistors (TFTs) current-voltage characteristic models. The emphasis is on the effect of the TFT channel-layer mobility and carrier concentration on device functionality and performance, with insight attained from device simulation of TFT current-voltage characteristic equations. The second part is a review of p-type semiconductors involving sulfides and oxides, which are selected for demonstrating electronic properties suitable for TFT applications.

2.1 Thin-film transistor square-law models

A thin-film transistor is a field-effect electronic device that can be deposited onto a variety of substrates, which is a unique advantage that provides low-cost and large-area manufacturability. Commercially, the primary application for TFTs has been in the flat-panel industry where TFTs function as switches for display pixels. Figure 2.1 shows a cross-sectional view of a staggered bottom-gate TFT structure. The constituent layers consist of a gate electrode and insulator, semiconductor, and source and drain contacts. Other structure configurations are discussed in Ref. [3].

The general concept of a field-effect transistor (FET) was first conceived in a patent written by Julius Edgar Lilienfeld in 1925. In 1934, 13 years before the invention of the transistor, Heil proposes a guideline for selecting a semiconductor material that may lead to the realization of an FET electronic device. Hail was unsuccessful in his efforts to find such a material to yield a functional TFT. In the 1940s, further efforts are attempted by Shockley to make a germanium TFT, but negligible conductivity modulation was observed. Working with germanium ultimately led to the invention of the bipolar junction transistor (BJT) in 1947, leading to the abandonment of further FET development [4].

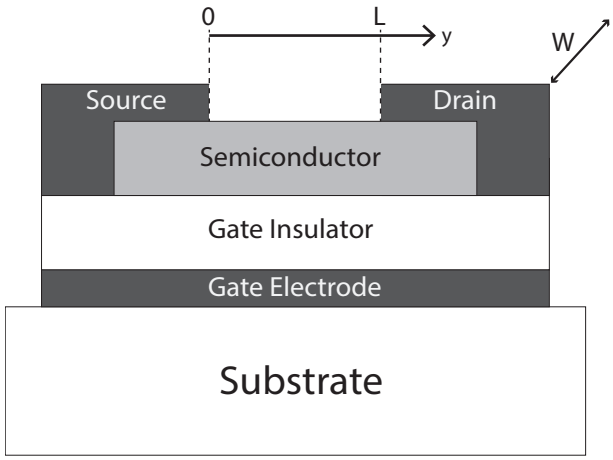

Figure 2.1: Cross-sectional schematic of a staggered bottom-gate TFT structure.

Transition to focus on BJTs development lagged the eventual massive success of FETs. It wasn't until the early 1960s that research interest on FETs reemerged, namely, TFTs and the metal-oxide-semiconductor FET (MOSFET). Although the silicon MOSFET triumphed over TFTs as the FET technology adapted, it was the TFT work on device operation theory and complementary inverters by Weimer what set the groundwork for MOSFETs current-voltage (I-V) models and CMOS technology [5, 6].

The TFT device operation theory developed by Borkan and Weimer is based on the gradual channel approximation (GCA), introduced by Shockley in the analysis of a junction FET (JFET). The developed I-V characteristic model is known as the ideal square-law. Modern derivations of the TFT ideal square-law model is presented in Ref. [3, 7, 8]. The I-V characteristics measured in a FET are modeled by the square-law in three regions: cut-off, pre-pinch-off, and post-pinch-off. The defining equations and constrains depend on the voltage applied to the gate and drain voltage terminals, i.e., $I(V_G, V_D)$. Table 2.1 presents the square-law model equations for each region of operation. Figure 2.2 shows I-V characteristics obtained from simulations employing ideal square-law equations and constraints.

Table 2.1: Ideal square-law model regions of operation

Variable	Units	Description
I_D	A	Drain current
W	cm	Channel width
L	cm	Channel length
μ	$\mathrm{cm^2V^{-1}s^{-1}}$	mobility
C_I	$\mathrm{Fcm^{-2}}$	Insulator capacitance
V_G	V	Gate voltage
V_D	V	Drain voltage
Region	Equation	Constraint
Cut-off	I_D=0	$V_G < V_{ON}$
Pre-pinch-off	$I_D = \frac{W}{L}\mu C_I \left[(V_G - V_{ON})\, V_D - \frac{V_D^2}{2}\right]$	$V_G \geq V_{ON}$ $V_D \leq V_G - V_{ON}$
Post-pinch-off	$I_D = \frac{W}{2L}\mu C_I \left(V_G - V_{ON}\right)^2$	$V_G \geq V_{ON}$ $V_D \geq V_G - V_{ON}$

2.2 P-type TFT semiconductor materials

In this section, an overview is presented of p-type semiconducting materials that are selected for exhibiting electrical characteristics that meet basic requirements to develop, in principle, a functional TFT device (i.e., reasonable mobilities and carrier concentration $< 10^{17}$ $\mathrm{cm^{-3}}$).

2.2.1 SnS material review

Tin monosulfide (SnS) is an earth-abundant and non-toxic p-type semiconductor with properties that captivate research interest for the fabrication of low-cost photovoltaic applications. Other applications proposed for SnS include photodetectors, near-infrared detectors, lithium micro-batteries, and commercial semiconductor sensors [9]. SnS has been grown using various methods, such as spray pyrolysis, electrodeposition, chemical bath deposition, chemical vapor deposition, electron beam [10, 11], RF sputtering [12, 13], molecular beam epitaxy (MBE) [14], atomic layer deposition (ALD) [15], thermal evaporation [16, 17], and vapor transport deposi-

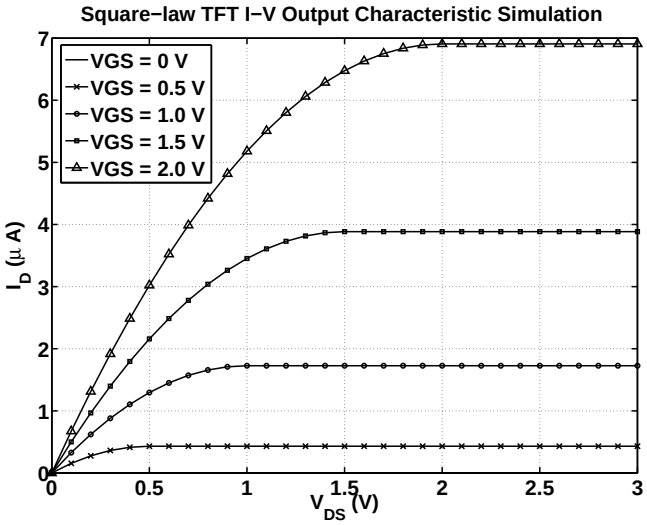

Figure 2.2: Square-law TFT current-voltage output characteristic simulation. An n-type semiconductor is assumed, with model parameters of $\mu = 10$ cm^{2}V^{-1}s^{-1}, $V_{ON} = 0$ V, and SiO_2 gate thickness of 100 nm. The drain voltage, V_{DS} is varied from 0-3 V in 0.1 V increments, with varying gate voltage, V_G, of 0-2 V in 0.5 V increments.

tion (VPD) [18]. There is wide variation on the reported properties of SnS, mainly dependent on the employed deposition method and processing conditions.

The bandgap of SnS has been reported to be direct and indirect and varying from 0.9 eV to 1.79 eV [19], while theoretical band structure calculation predicts an indirect bandgap of 1.07 eV [20]. Experimental work in the Physics department at Oregon State University reports optical measurements with indirect and direct absorption onsets of 1.16 eV and 1.31 eV, respectively, for approximately 100 nm thick thin films grown using pulsed laser deposition [21]. The type of semiconductor bandgap (indirect or direct) is relevant in photovoltaic applications, due to higher thin film thickness requirements in indirect semiconductors for complete absorption. In TFT applications, free carrier mobility plays a more important role in predicting device performance.

Table 2.2: Summary of SnS Hall-effect measurements.

Fabrication Method	Mobility $[cm^2V^{-1}s^{-1}]$	Carrier Concentration $[cm^{-3}]$	Ref.
Evaporation	0.8-31.6	10^{15}-10^{16}	[16]
PLD[a]	4-16	$3 \times 10^{14} - 7 \times 10^{15}$	[21]
ALD[b]	15.3	6.9×10^{15}	[15]
MBE[c]	20	3×10^{16}	[14]
PVD[d]	34.14	1.52×10^{15}	[22]
Distilled crystals	90	3×10^{17}	[23]
Sprayed pyrolysis	130	10^{15}	[24]
VTD[e]	385	10^{17}	[18]
Evaporation	400-500	6.3×10^{14}-1.2×10^{15}	[17]

[a]Pulsed laser deposition
[b]Atomic layer deposition
[c]Molecular beam epitaxy
[d]Physical vapor deposition
[e]Vapor transport deposition

Table 2.2 presents a summary of SnS properties published in literature, showing reported mobilities of 0.8-500 $cm^2V^{-1}s^{-1}$ for samples fabricated from various processing methods and conditions. Variation in SnS process growth conditions yields a hole carrier density of 10^{14}-10^{17} cm^{-3}. The p-type nature of SnS is the result of acceptor levels from energetically favorable double-ionized tin vacancies, confirmed by theoretical and experimental work presented in Ref. [20]. Change in SnS conductivity from p-type to n-type is possible by producing Sn-rich films (achieved by high temperature growth), a property with the potential to realize p-n junctions or complementary TFT circuits based on SnS.

Earlier investigations from 1961 of SnS crystals determined a mobility dependent on the crystal direction in which a sample is measured, showing that $\mu_a < \mu_b < \mu_c$ as measured from the Hall effect of distilled SnS single crystals bars [23]. More recent studies on the structural properties of SnS indicate that the mobility of SnS is 0.8-31.6 $cm^2V^{-1}s^{-1}$, as obtained from Hall-effect measurements of 690 nm SnS thin films grown via vacuum evaporation [16]. The highest mobility of 31.6 $cm^2V^{-1}s^{-1}$ is

obtained for samples annealed at a temperature of 300 °C, with predominant peaks in the (101) and (111) direction indicated by XRD data.

2.2.2 p-type oxide semiconductors

The arrival of transparent TFTs (TTFTs) and the development of transparent electronics more than a decade ago exposed exciting new territory for creative and innovative research [25]. The materials that make TTFTs possible need to have a wide bandgap, E_G, so that the visible portion of the electromagnetic spectrum is transmitted. The visible spectrum covers wavelengths of about 400 nm to 700 nm, which correspond to an energy of 1.77-3.1 eV. Consequently, maximum transparency is achieved using materials with an $E_G > 3.1$ eV, as illustrated with an ideal optical transmittance plot in Fig. 2.3.

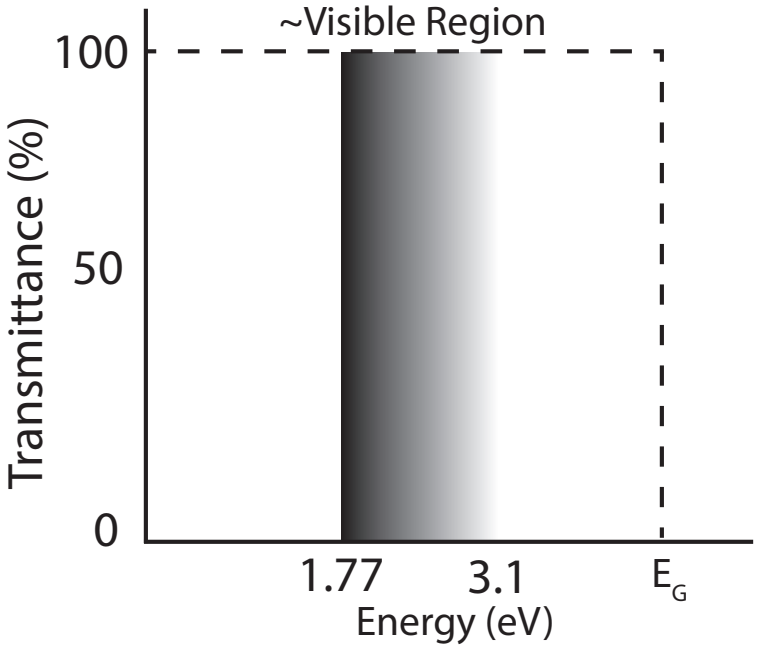

Figure 2.3: Ideal optical transmittance plot of a transparent medium.

Commercially, the leading TTFT is based on IGZO, an n-type AOS with attractive electrical performance and manufacturability. However, due self-compensation effects, p-type doping of IGZO is ineffective. Ineffective ambipolar doping is not a limitation unique to IGZO. In general, a wide band gap material will exhibit asymmetric p vs. n doping due to self-compensation [26]. Moreover, a semiconductor with small electron affinity, or a valence band far from the vacuum energy level (high photoelectric threshold) cannot be easily doped n-type or p-type, respectively [27]. Mathematically, self-compensation can be described by the energy of formation for a defect, ΔH_f, defined as [26]

$$\Delta H_f\left(E_F\right) = c + qE_F, \tag{2.1}$$

where c is a constant, E_F is the Fermi level. In Eq. 2.1, the value of q is negative (positive) for an acceptor-like (donor-like) defect. Adding acceptor dopants will move the Fermi level towards the valence band. However, this modulation of the Fermi level makes it more energetically favorable to spontaneously create a donor-like defect since its formation energy is lowered. Thus, acceptor doping results in the formation of self-compensated donor defects, rather than an increase in the hole concentration, as normally expected. Self-compensation is discussed further by Hoffman in Ref. [28].

A wide bandgap semiconductor is prone to self-compensation. Thus, n- and p-type TTFTs, as required for a CMOS-like TFT technology, is challenging. Some of the p-type semiconductors proposed for TTFTs are reviewed in this section.

2.2.2.1 Cuprous Oxide

Cuprous oxide (Cu_2O) is a material known since the infancy of solid-state electronics, before terminology existed for semiconductors, and before the invention of transistors. In 1926, a new rectifier based on Cu_2O was reported by Grondahl, a technological advancement beyond vacuum tubes, facilitating solid state conversion of alternating current to direct current [29]. Early research on Cu_2O serves as a foun-

dation for the development of the theory of semiconductor materials and electronic devices.

Cu_2O is a p-type semiconductor with a direct bandgap of 2-2.6 eV. Cu_2O fabrication has been reported using various techniques, e.g., molecular beam epitaxy, radio frequency-magnetron sputtering, chemical vapor deposition, and spray pyrolysis [30, 31, 32, 33]. Cu_2O has polycrystalline structure with a surface roughness upwards of 5 nm [34]. In Cu_2O, negatively charge copper vacancies (V_{Cu}) has been associated as the cause for its p-type characteristic. Unlike most metal oxides, the top of the valence band in Cu_2O is dominated by Cu d states, giving rise to high bulk mobility, as opposed to O 2p orbitals where mobility is low due to hopping conduction [35].

The Cu_2O bulk mobility and carrier concentration is 47.5-256 $cm^2V^{-1}s^{-1}$ and 10^{14}-10^{17} cm^{-3}, respectively, where property variations depend on deposition method and processing conditions employed [36, 34, 37]. In thin film form, Cu_2O higher hall mobility is demonstrated to improve from < 1 $cm^2V^{-1}s^{-1}$ to ~ 18 $cm^2V^{-1}s^{-1}$, correlated to a bigger polycrystalline grain size observed after subjecting as-deposited samples to a 200 °C temperature anneal for 10 hours [38]. However, as summarized in Table 2.3, the field-effect mobility of enhancement-mode Cu_2O TFTs is found to be < 2.4 $cm^2V^{-1}s^{-1}$. Table 2.3 presents a summary of Cu_2O TFT performance reported in recent publications.

Table 2.3: Summary of Cu_2O TFT performance.

Fabrication Method	Gate Insulator	Mobility [$cm^2V^{-1}s^{-1}$]	V_{ON} [V]	$I_D^{ON\text{-}OFF}$	S[a] [V/dec]	Year	Ref.
RFS[b]	Al_2O_3/TiO_2	1.2×10^{-3}	-12	2×10^2	-	2012	[35]
RFS	SiO_2	0.06	-6.7	1.8×10^4	1.6	2012	[37]
RFS	AlN	2.4	-	4×10^4	< 5	2012	[39]
RFS	SiO_2	0.05	-11.6	10^4	3.3	2013	[40]
Spin-coat	SiO_2	0.16	-	1×10^2	-	2013	[41]

[a]Subthreshold swing
[b]Radio-frequency sputtering

2.2.2.2 Tin monoxide

Tin monoxide (SnO) is p-type semiconductor with a direct optical bandgap of $\sim$ 2.7 eV [42], and an optical transmission of 67% to 86% [43, 44]. The p-type conductivity of a SnO thin film is attributed to Sn vacancies, as determined from first principle calculations of native defects [45]. Fabrication of SnO thin films have been reported using various techniques, e.g., radio-frequency sputtering (RFS) [46, 47, 48, 49, 50], electron beam evaporation (e-beam) [51, 44], pulsed laser deposition (PLD) [42], and solution-processing [52].

The deposition process gas and temperature have been shown to play a dominant role to produce phase-pure SnO thin films with a p-type character. Amorphous SnO is formed as-deposited, and it changes to a polycrystalline structure at a processing temperature above 200 °C. Crystalline SnO_2, having an n-type conductivity, is formed when a process temperature above 500 °C is employed [44]. Re-evaporation begins to occur at a temperature above 600 °C. Moreover, a reducing atmosphere is necessary to produce SnO thin films, but it is only achieved within a narrow oxygen process pressure (P_O). In a high P_O, SnO_2 is formed, while Sn precipitates at lower P_O, producing films exhibiting properties of metallic Sn [42, 49].

Table 2.4 presents a summary of Hall-effect measurement results of SnO thin films, as well as TFT performance reported in literature. The Hall mobility and carrier concentration is found to be < 4 $cm^2V^{-1}s^{-1}$ and $\sim$ 10^{16}–10^{18} cm^{-3}, respectively. The relatively high concentration of holes measured in SnO thin films have resulted in depletion-mode TFT behavior with large off drain current and on-to-off drain current ratio of $< 10^4$ [35]. SnO TFTs are shown to have a depletion-mode field-effect mobility of < 2 $cm^2V^{-1}s^{-1}$, threshold voltage of 5-50 V, on-to-off drain current of $< 10^4$, and subthreshold swing of 2-11 V/dec. In contrast to n-type oxide TFTs, the performance of SnO TFTs is quite poor.

2.3 Solution-processed semiconductors and dielectrics

The solution-processed fabrication of thin film materials that are intended for large-area and macroelectronic applications that demand modest performance (e.g., FPDs, photovoltaics, or RFID tags), provide certain advantages unattainable from traditional vacuum and advanced microelectronic manufacturing. One of the most prominent benefits is the manufacturing cost reduction. To put things in perspective, it is estimated that a modern 300 mm wafer fabrication facility costs upwards of $3 billion, while a macroeletronic facility (e.g., roll-to-roll manufacturing facility) is expected to cost as least an order of magnitude less ($\sim$ $300 million). It is also estimated that the microelectronic manufacturing cost per unit area is in the range of $10,000/ft^2, while $100/ft^2 for macroelectronics [54].

The cost benefit of solution-processing of materials is clear. However, there are other advantages, such as low-temperature processes (enabling the fabrication of flexible electronics), large throughput over large areas, and sustainable manufacturing from efficient material utilization and energy-efficient techniques [54, 55]. Therefore, in this section, a review of solution-processed indium-gallium-zinc-oxide (IGZO) amorphous oxide semiconductor (AOS) is presented. Furthermore, a review of solution-processed dielectrics that have emerged from laboratory collaborations at Oregon State University (OSU) is preesented as well.

2.3.1 Introduction to amorphous oxide semiconductors

In the realm of flat-panel display (FPD) technology, amorphous hydrogenated silicon (a-Si:H) dominates the market as the semiconductor of choice for thin-film transistors (TFT) backplanes. Demand for displays with increased size and resolution requires TFTs with high mobility, e.g., a display with a 4k x 2k resolution and 120 Hz refresh rate requires a mobility of 4 $cm^2V^{-1}s^{-1}$, so that a-Si:H with a mobility of < 1 $cm^2V^{-1}s^{-1}$ is no longer a viable option [56]. An amorphous oxide

semiconductor (AOS) TFT exhibits a mobility upwards of 10 $cm^2V^{-1}s^{-1}$ and, along with low-temperature polysilicon, is a class of materials emerging to replace a-Si:H.

The advantages of an AOS that emanate from its amorphous nature, are lack of grain boundaries, highly smooth surfaces (important to avoid integration issues like interface traps and scattering centers), and low temperature processing. These properties make the AOS an appealing material for large-area and low-cost manufacturing, and possible flexible electronic applications. Furthermore, AOS materials are composed of metal cations that readily react with oxygen, forming metal oxides that are thermodynamically and environmentally stable; meaning an AOS can be processed in air [57].

In an AOS, the electron conduction pathway is the conduction band minimum (CBM), which is composed of overlapping, spherically symmetric, vacant metal cation s-states. Due to the spherical geometry of the metal cation s-states, large overlap occurs between orbitals independent of bond angles, resulting in a large dispersion of the conduction band (i.e., low effective mass), this being the source of AOS high mobility. Subsequently, since s-state spatial overlap is predominantly determined by the quantum number, n, heavy post-transition metal cations with an electronic configuration of $(n\text{-}1)d^{10}ns^0$, where $n > 5$, are the candidate materials of choice high mobility AOS material design [58].

Some of the AOS material systems that have been developed, primarily via vacuum deposition routes, are amorphous indium gallium zinc oxide (a-IGZO), zinc indium tin oxide (ZITO), zinc tin oxide (ZTO), and indium zinc oxide (IZO). However, AOS solution-processed methods are still in a very early stage of research. Thus, in this section, current work of early development spin-coated deposition methods of IGZO is reviewed, as it pertains to the theme of this thesis.

2.3.1.1 Solution-processed IGZO

In 2004, Hosono et al. reported an a-IGZO TFT deposited by pulsed laser deposition on a flexible substrate [59]. Since then, a-IGZO has been a prevalent research topic, with a primary focus on development for backplane TFTs in FPDs. To date, a-IGZO is the leader AOS technology successfully on its route towards commercialization. Physical vapor deposition (PVD) tools have been developed, e.g., by Applied Materials, that are capable of depositing a-IGZO with thickness uniformity of $< \pm 9\%$ on large-area glass substrates of 2200 x 2500 mm (Gen8.5 glass) [60]. A comprehensive material review of IGZO is presented in Ref. [61, 35, 62], outlining chemical, physical, and electrical characteristics of a-IGZO.

While commercialization of a-IGZO is imminent, inherent operational cost of vacuum equipment and facilities merits the effort to explore solution-processing alternatives. Work on solution-processing shows TFT with various electrical performance obtained from diverse solution precursors, In:Ga:Zn composition, and processing conditions. Table 2.5 summarizes various TFT performance obtained from solution deposited a-IGZO, tabulated by composition, annealing temperature, mobility, turn-on voltage (V_{ON}), and drain current on-to-off ratio ($I_D^{ON\text{-}OFF}$).

A highlight from Table 2.5 is the work published in Ref. [64], in which a high pressure annealing (HPA) processing condition is employed in order to decrease the processing temperature. It is found is that by using HPA, TFT performance improves compared to air annealing at temperatures as low as 220 °C. The improved TFT performance is attributed to a reduced interfacial roughness between the channel and insulator from 1.25 nm to 0.95, originating from a shrinkage of the thin film from a thickness of 28 nm to 23 nm, for the samples anneal in air and the HPA process, respectively. A key comment is missing regarding the improved density and porosity of the HPA-processed IGZO films. Although no data is shown about the IGZO film density and porosity, a mobility about four times higher is observed for the reported

indium zinc oxide (IZO) films. The density and porosity is enhanced for the IZO films from 4.3 g/cm^3 to 4.6 g/cm^3 and the porosity from 19% to 11% for the films anneal in air and HPA, respectively.

It appears that film density plays an important role in improving solution-processed TFT performance and stability. However, it is unfortunate that the majority of publications do not report film density along with TFT transfer curves.

2.3.2 Solution-processed dielectrics

This section presents a review solution-processed dielectrics that have emerged from OSU laboratory research collaborations. The emphasis is in the performance demonstrated in TFT applications. Table 2.6 presents a summary of film quality and TFT performance obtained from solution-processed gate dielectric of aluminum oxide phospate (AlPO), TiO_2-AlPO nanolaminates, hafnium oxide sulfate (HafSOx), and HfO_2.

In 2007, work on spin-coated aluminum oxide phosphate (AlPO) thin films is reported by Meyers et al., a medium-κ oxide-dielectric [68]. The approach listed for the solution synthesis involves promoting metal-hydroxide-metal (M–$(OH)_x$–M) interactions in a aqueous solution precursor by controlling pH, limiting high-volume ligands and non-functional counterions (ions that keep charge neutrality), and preventing formation of large sol particles [68]. The result is the prompt condensation of AlPO films upon application of heat, exhibiting morphologies ($<$ 2 nm surface roughness) and electrical characteristics that generally would only be possible via high-vacuum processes [68]. Conversely, a typical solution preparation would involve the synthesis of a sol-gel precursor containing large hydroxide nanoparticles (tens of nanometers), yielding porous films with rough surfaces that limit TFT performance [55].

RF-sputtered ZnO TFTs are demonstrated utilizing 135–185 nm of solution-processed AlPO films annealed at 1000 °C as the gate dielectric. The TFT perfor-

mance is reported to have an incremental mobility of 3 $cm^2V^{-1}s^{-1}$, turn-on voltage of -1 V, and drain current on-to-off current ratio of 10^6. In comparison, using a thermal grown SiO_2 dielectric yielded an incremental mobility of 6 $cm^2V^{-1}s^{-1}$, turn-on voltage of 1 V, and drain current on-to-off ratio of 10^7. Furthermore, in 2012 Jiang et al. reported the work on TiO_2–AlPO nanolaminates [69]. TFTs are fabricated with 150 nm of TiO_2–AlPO nanolaminates annealed at 350 °C as a gate dielectric, with a solution-processed IGZO for the semiconductor layer. TFT perfomance is reported to have a peak incremental mobility of 3.2 $cm^2V^{-1}s^{-1}$ at $V_{GS} = 5.5$ V, turn-on voltage of 0 V, drain current on-to-off current ratio of $> 10^5$, and subthreshold swing of 0.3 V/dec.

Finally, to conclude this section, Anderson et al. in 2007 fabricates solution-processed HafSOx thin film dielectrics employing a comparable approach for solution synthesis utilized by Meyers. TFTs are fabricated using HafSOx as a gate dielectric and zinc-indium-oxide (ZIO) for the semiconductor layer [70]. The TFTs exhibited a drain current on-to-off current ratio $>10^6$, with low gate current leakage in the nA/cm^2 range. Moreover, in 2011 Jiang et al. developed solution-processed HfO_2 dielectric films [71]. From x-ray reflectivity, Jiang measured a density of 87% for films annealed at 600 °C, and a surface density of $\sim$ 0.15 nm for films annealed above 500 °C. The performance of TFTs measured using a solution-processed HfO_2 gate dielectric and rf-sputterd IGZO semiconductor layer showed a peak incremental mobility of 13.1 $cm^2V^{-1}s^{-1}$ at a $V_{GS} = 25$ V, turn-on voltage of 8.5 V (compared to $V_{ON} = 2$ for a thermally grown SiO_2 gate dielectric), drain current on-to-off ratio $> 10^7$, and subthreshold swing of 0.3 V/dec.

Table 2.4: Summary of SnO Hall-effect measurements and TFT performance.

Fabrication Method	T_{max} [°C]	p [cm^{-3}]	μ_{Hall} [$cm^2V^{-1}s^{-1}$]	μ_{FE} [$cm^2V^{-1}s^{-1}$]	V_t [V]	$I_D^{ON\text{-}OFF}$	S[a] [V/dec]	Ref.
RFS[b]	300	2-9×10^{17}	0.4-0.6	0.24	30	10^2	-	[46]
RFS	500	4.3×10^{17}	0.64	-	-	-	-	[47]
RFS	250	-	-	0.24	2.5	10^3	2	[53]
RFS	400	2.6×10^{17}	1.2	-	-	-	-	[48]
RFS	200	10^{16}-10^{18}	4.8	1.1	5	10^3	-	[49]
RFS	250	10^{17}-10^{18}	1-4	1.8	50	10^3	-	[50]
EBPVD [c]	600	-	1.6	0.87	3.5	2×10^2	11	[51]
PLD[d]	575	2.5×10^{17}	2.4	1.3	4.8	10^2	-	[42]

[a]Subthreshold swing
[b]Radio-frequency sputtering
[c]Electron-beam physical vapor depostion
[d]Pulsed laser deposition

Table 2.5: Summary of solution-processed a-IGZO TFT performance.

Composition In:Ga:Zn	Temperature [°C]	Mobility [$cm^2V^{-1}s^{-1}$]	V_{ON} [V]	I_D^{ON-OFF}	Ref.
63:10:27	400	0.85	17	1×10^6	[58]
2:1:1	400	0.07	0.55	8×10^4	[63]
3:0.5:1	220	0.05	0	7×10^6	[64]
3:1.4:2	450	0.05	0.2	1×10^6	[65]
4:1:5	500	1.13	-5	1×10^6	[66]
5:1:2	400	1.25	-5	4×10^6	[67]

Table 2.6: Summary of solution-processed dielectrics and TFT performance.

	Dielectric Properties			TFT Performance			
	ϵ_r	J_{leak}[a] [nA/cm^2]	Breakdown[b] [MV/cm]	Channel	μ_{inc} [cm^{2}V^{-1}s^{-1}]	V_{ON} [V]	I_D^{ON-OFF}
AlPO	4.8	< 10	> 7	ZnO	3	-1	10^6
TiO_2-AlPO	8	< 10	≥ 3.5	IGZO	3.2	0	10^5
$HafSO_x$	-	< 50	4-6	ZIO	-	-	$> 10^6$
HfO_2	12-13	≤ 10	≥ 3.5	IGZO	13.1	8.5	$> 10^7$

[a] Measured at a field strength of 1MV/cm

[b] Defined at a leakage current density exceeding 10 μA/cm^2

3. EXPERIMENTAL TOOLS TECHNIQUES

In this chapter, a brief discussion of the experimental techniques used for the fabrication and characterization of p-type thin films and devices is presented. Three main topics are discussed: 1) thin film deposition and processing, 2) thin film characterization, and 3) TFT device characterization.

3.1 Thin film deposition and processing

This section addresses the thin-film deposition techniques employed in the experiments presented in thesis, as well as post-deposition annealing processing to improve film and material quality.

3.1.1 Radio-frequency sputtering

Figure 3.1 is an schematic representation of the essential components in a radio-frequency sputtering system. Material deposition via RF sputtering is achieved by the bombardment of a target material with highly energized ions from the plasma of a gaseous discharge [72]. Ejected atoms with sufficient energy will impinge on a sample substrate and coat it with a condensed thin film. Formation of a glow discharge is initiated by impact ionization from electrons present in the process gas (typically argon), accelerated by an electric field from an RF power supply, commercially operated at 13.56 MHz. Newly released electrons maintain the plasma by the continual formation of ion-electron pairs via an avalanche ionization process, which typically requires process gas pressures of 1-15 mTorr to sustain the plasma.

An important aspect of RF sputtering is the DC self-bias (VDC) that builds up near the target (the cathode). Coupling a capacitor in series with the cathode to block the flow of DC current forms a VDC. In principle, an insulating target itself works as a capacitor, but in most matching network units a dedicated blocking capacitor is added to allow RF sputtering of conducting target materials and to efficiently transfer

RF power to the target. Electrons are accelerated to oscillate with the RF signal and build up a negative potential near the target due to the blocking capacitor. However, argon ions are too heavy to react to voltage changes from the RF power supply at frequencies > 1 MHz. Ionized argon atoms are therefore accelerated towards the target by the VDC during the RF negative cycle in the cathode. Monitoring of the VDC values is vital to maintain efficient sputtering depositions, and to keep track of the target lifetime. As the target source is consumed, the VDC will start decrease.

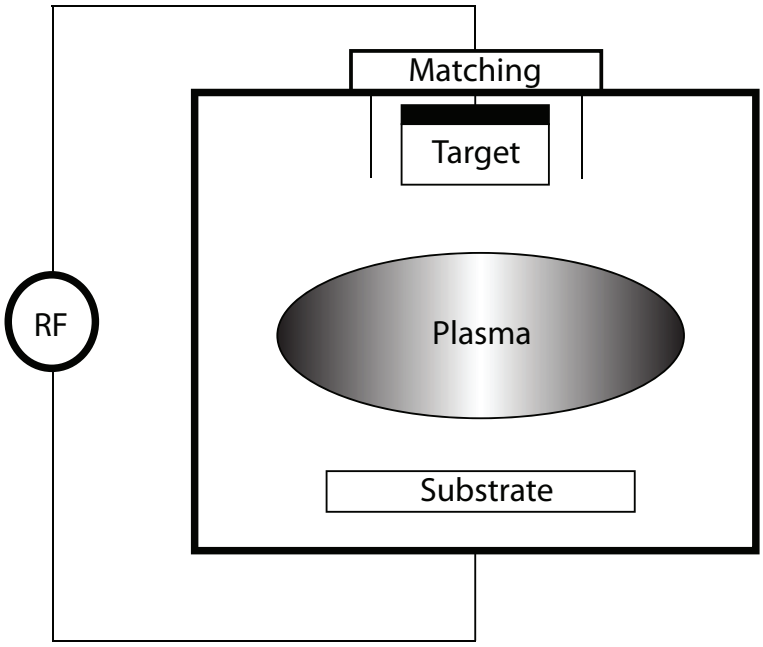

Figure 3.1: Schematic of the essential components of an RF sputtering system.

3.1.2 Pulsed electron deposition

Pulsed electron deposition (PED) is a PVD process that relies on a high power pulsed electron beam created in gas discharge under low-pressure conditions. Some of the electron beam characteristics include a short pulse (100 ns), high energy

density (10 J/cm^2) that are delivered to the target by low-energy electrons (10-20 keV). The electron beam penetrates a distance of approximately 1 mm into the target material, resulting in a rapid evaporation and plasma formation of a target material. Plasma stoichiometric composition is achieved from non-equilibrium removal of the target material. Figure 3.2 shows an schematic of a pulsed electron deposition (PED) system, consisting of a vacuum chamber, an electron beam source, target holder, and substrate holder.

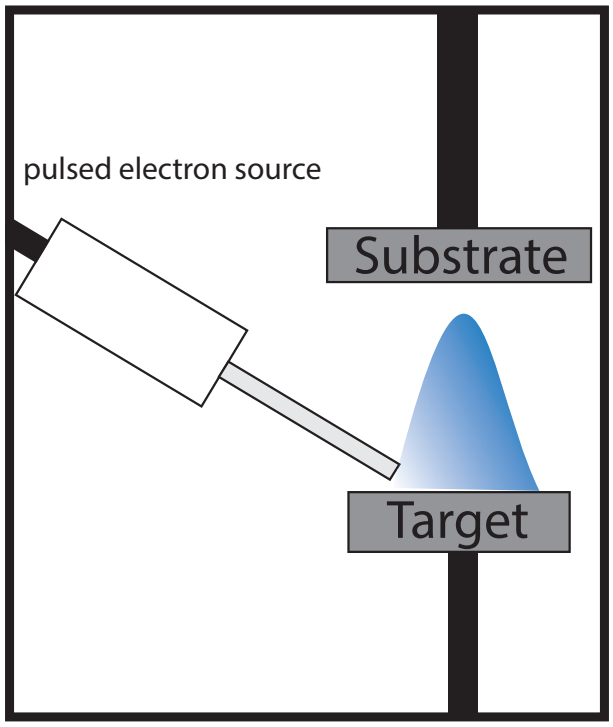

Figure 3.2: General schematic of a pulsed electron depostion system.

A PED is comparable to a pulsed laser deposition (PLD). However, a PED system can process a wider range of solid state materials than a PLD system, which is limited by the laser wavelength transparency to a material. PED growth advantages,

similar to that of a PLD, include a simple system set-up, easily controllable thin film thickness, deposition of complex multi-component material with stoichiometry nearly identical to that of the target material, and a relatively high deposition rate without rapidly consuming the target [73].

Thin film growth process conditions for desired material properties are determined experimentally for different target materials. The electron beam source utilized in this thesis is a Neocera PEBS-20, capable of varying the number of pulses, pulse rate (up to 15 Hz), and the beam electron energy from 8-20 keV. Other process parameter variables include process gas pressure (1-20 mTorr), substrate heating (up to 950 °C), substrate rotation speed, and target raster speed.

3.1.3 Thermal evaporation

In this thesis metals are used to make contact with a thin film when current injection and extraction is required. In order to deposit such a metal contact, a thermal evaporation process is employed. Thermal evaporation is a vacuum process that involves applying a current to a resistive wire coil or basket to heat a metal source. When the metal is heated to its evaporation temperature, the metal vaporizes and subsequently deposits onto the sample surface. Typical pressures for the metals deposited in this work are around 5×10^{-6}-7×10^{-6} Torr. This process is better suited for metals with low melting and evaporation temperatures; otherwise an electron beam evaporation process can be used for materials demanding higher power. A more detailed discussion of thermal evaporation of thin films can be found in Ref. [72]

3.1.4 Electron-beam evaporation

Figure 3.3 shows an schematic representation of an electron-beam (e-beam) evaporation system similarly used in this thesis experiments. The important components include a high-vacuum stainless steel chamber, substrate holder, an electron

beam filament, and a target material crucible. Material evaporation in an e-beam process is initiated by the transfer of kinetic energy to thermal energy from thermionic emitted beam of electrons emanating from a hot filament. The beam of electrons is accelerated by an applied potential, and redirected in the direction of the source material by the Lorentz force of an applied magnetic field. Furthermore, the highly energized beam of electrons (5-30 keV) heats up the source material to initiate vaporization, which condensates on a substrate. A drawback of e-beam evaporation is the potential damage on a previously deposited thin film by the generated x-rays from the electron beam [74].

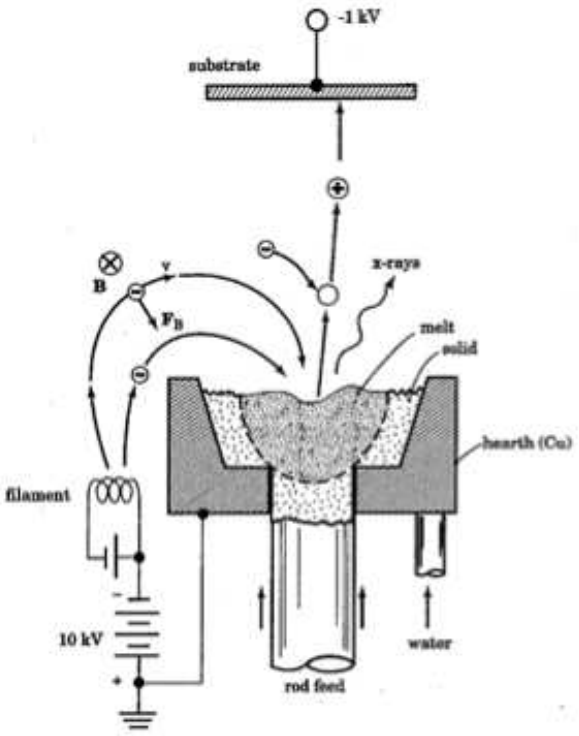

Figure 3.3: Electron-beam evaporation system configuration [75].

3.2 Thin film characterization

This section summarizes the key thin-film characterization techniques utilized to assess the materials studied in this thesis, including: Hall measurements, Seebeck coefficient, optical characterization, and x-ray diffraction and reflectivity.

3.2.1 Hall-effect measurement

The Hall-effect measurement is a common characterization technique to determine electronic properties of solids. Four important thin film properties of interest are determined from a Hall measurement: 1) carrier density, 2) carrier type, 3) resistivity, and 4) mobility [76]. In this section, an overview of the Hall effect and a simple thin-film Hall measurement experimental configuration is discussed.

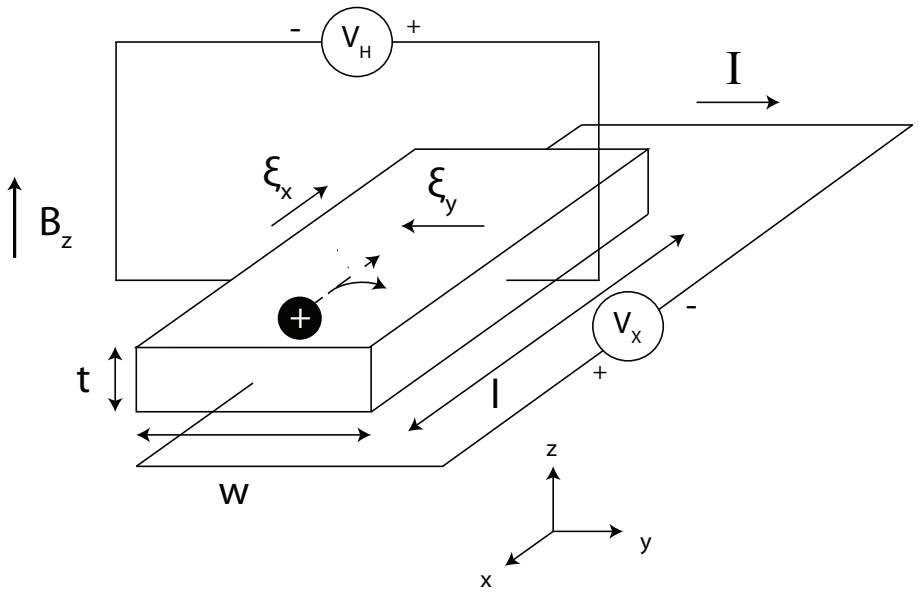

Figure 3.4: Experimental configuration of a p-type material Hall measurement.

The Lorentz force acting on a charged particle in a current-carrying material, generated by an applied magnetic field, is the basis of the Hall effect. Figure 3.4

illustrates an experimental configuration to measure the Hall effect for a p-type material of dimensions $l \times w \times t$, where l, w, t refer to the length, width, and thickness, respectively, of the material under test. A current I_x, driven by a potential V_x, is injected into the sample. A magnetic field $\vec{B}$ directed in the positive z-direction, deflects I_x towards the positive y-direction via the Lorentz force. Deflecting current towards one side of the material gives rise to a space-charge region, which results in a potential difference (the Hall voltage, V_H) across the sample that is perpendicular to both the applied magnetic field and current flow [77].

Raw data from Hall-effect measurements is used to calculate the Hall coefficient (R_H), resistivity (ρ) when $B = 0$, and Hall mobility (μ_H) [78]. The Hall voltage is calculated from the defining equation,

$$R_H = \frac{V_H t}{B_z I_x}, \tag{3.1}$$

where V_H is the measured Hall voltage, t the sample thickness, B_z the magnetic field, and I_x the applied current. The sign of the Hall coefficient identifies material carrier type, being positive for p-type material and negative for n-type. Carrier concentration is derived from the Hall coefficient for p-type materials with p >> n from

$$R_H = \frac{r}{qp}, \tag{3.2}$$

where r is the Hall factor that can take values between 1 and 2. r, will approach unity at high magnetic fields. The magnetic fields for the equipment used for this thesis (0 to 20 kG) are not sufficient for r to approach unity, and it is therefore assumed to be unity. Assuming that r is unity typically introduces an error of less than 30% [79]. Furthermore, carrier concentration for n-type materials with n >> p can be determine by

$$R_H = -\frac{r}{qn}. \tag{3.3}$$

Resistivity is characterized using a van der Pauw method for measuring resistivity of uniform, flat samples of arbitrary shapes [80].

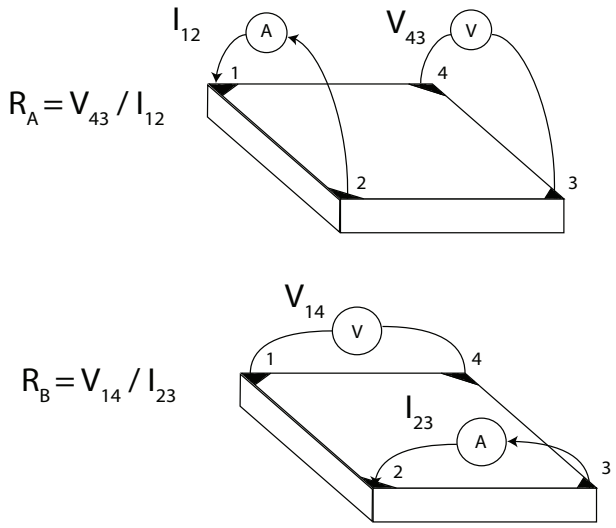

Figure 3.5: van der Pauw configuration used to determine characteristic resistances, R_A and R_B.

Figure 3.5 illustrates a van der Pauw configuration from which two characteristic resistances are measured, R_A and R_B. Sheet resistance, R_S, is numerically calculated using R_A and R_B via the van der Pauw equation,

$$\exp\left(-\pi R_A/R_S\right) + \exp\left(-\pi R_B/R_S\right) = 1, \tag{3.4}$$

from which resistivity is subsequently calculated using

$$\rho = R_s t. \tag{3.5}$$

Knowing R_H and ρ allows the Hall mobility, μ_H, to be estimated as,

$$\mu_H = \frac{|R_H|}{\rho}. \tag{3.6}$$

3.2.2 Seebeck coefficient

A Seebeck coefficient, also known as thermoelectric power, is a measure of electromotive force (emf) generated by a temperature gradient in a material. The sign of the Seebeck coefficient determines carrier type, formulated to designate an n-type material when it is negative, and a p-type when it is positive [76]. The magnitude of the Seebeck coefficient is inversely related to carrier concentration [81]. Therefore, a high free carrier concentration in a metal results in a low Seebeck coefficient (< 10 $\mu V/K$). The Seebeck coefficient increases for more insulating materials with fewer carriers [82].

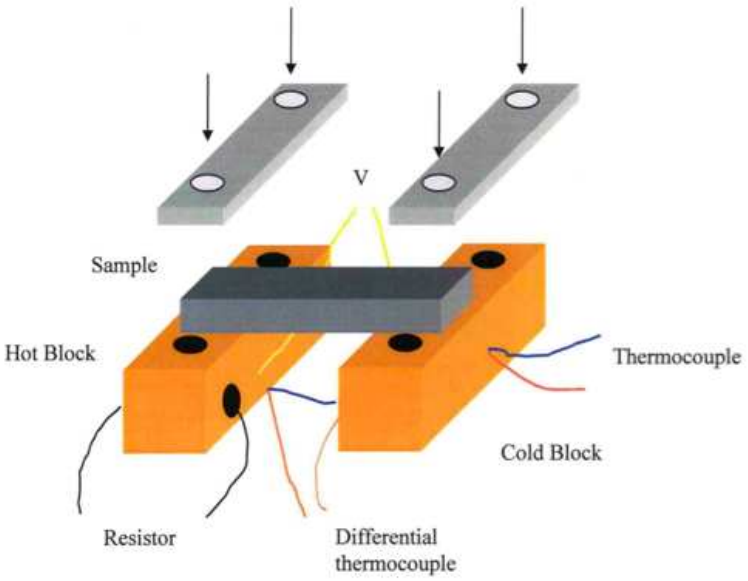

Figure 3.6: Experimental configuration for a Seebeck-effect measurement [83].

Figure 3.6, illustrating the Seebeck effect, shows an n-type material with a heat source applied to the left side to create a thermal gradient in the sample. Thermal energy from the heat source generates excess free carriers in the hot side, which begin to diffuse towards the cold side where there is a deficit of electrons in order to establish thermal equilibrium [83]. Accumulation of majority carriers in the cold side produces an electric field which opposes the diffusion of carriers from the hot side. A steady-state condition is reached when the strength of the electric field prevents further diffusion of electrons from the hot side. A potential difference is established between the accumulated electrons on the cold side and the positive ions on the depleted hot side. The Seebeck coefficient can be calculated using the measured voltage by,

$$S = -\frac{\Delta V}{\Delta T}, \tag{3.7}$$

and the carrier concentration derived from the Seebeck coefficient is given by,

$$S = \frac{k_B}{q}\left[\left(\frac{5}{2} - s\right) + \ln\left(\frac{N_V}{p}\right)\right], \tag{3.8}$$

where S is the Seebeck coefficient, k_B is Boltzmann's constant, q is the electronic charge, s is the scattering parameter, N_V is the valence band density of states (DOS), and p is the hole density. Equation 3.8 requires detail band structure and transport scattering information about the material in question [84], but to first order, carrier density can be estimated by assuming N_V is the order of $10^{19} cm^{-3}$, and letting $s = \frac{5}{2}$ by employing the assumption that ionized impurities are the main material transport scattering mechanism. Making these assumptions, the hole density may be estimated from the Seebeck coefficient as,

$$p = N_V e^{-qS/k_B} = 10^{19} e^{-1.16\times10^4 S}\left(cm^{-3}\right), \tag{3.9}$$

where S is expressed in units of V/K. Table 3.1 shows Seebeck coefficient estimation values for different hole carrier concentrations, calculated using Eq. 3.9.

Table 3.1: Hole carrier density vs. Seebeck coefficient calculated using Eq. 3.9

p (cm^3)	**S** ($\mu V/K$)
10^{13}	+1190
10^{14}	+992
10^{15}	+793
10^{16}	+595
10^{17}	+397
10^{18}	+198
10^{19}	0

3.2.3 X-ray diffraction

X-ray diffraction (XRD) is a non-destructive technique employed in material characterization to determine atomic structure and composition of crystalline solids and powders. Elastic scattering of incident x-rays on a crystal will produce a unique diffraction pattern that is used to deduce the phases present in the material. Figure 3.7 shows an example XRD plot showing the intensity counts of different phases at a particular angle of detection. A phase is a fingerprint of a an specific chemistry and atomic arrangement, and the peak intensity in an XRD plot gives a quantitative analysis of the phases present in a sample. Chemical composition is determined from collected XRD data by matching phase peaks against the Powder Diffraction File (PDF) database, which is maintained by the International Centre of Diffraction Data (ICDD).

X-rays with energies between 3 and 8 keV correspond to wavelengths of 1.5 to 4 Å, which are on the length scale of inter-atomic distances. Therefore, x-rays meet the geometric requirement for diffraction of electromagnetic radiation from periodic

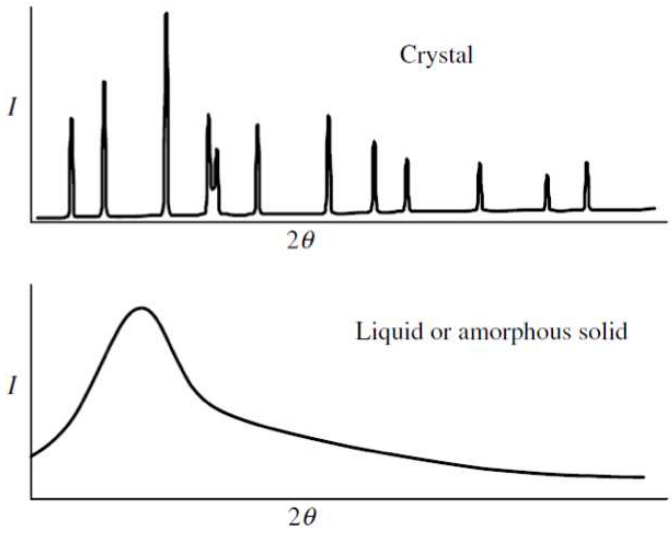

Figure 3.7: Intensity vs. 2θ XRD example plot of a crystalline and amorphous sample [85].

structures [86]. Figure 3.8 shows the elastic scattering of x-rays from parallel crystal planes separated by a distance d. Incident x-rays are exposed to the surface at an angle θ. Diffraction peaks occurs when the condition of constructive interference of reflected x-rays is satisfied, which is determined by the Bragg's law,

$$2d\sin(\theta) = n\lambda, \tag{3.10}$$

where n is an integer representing the order of the diffraction peak, and λ is the x-ray wavelength. An x-ray in an amorphous structure will scatter in arbitrary directions, so that broad diffraction peaks are measured [87].

A typical $\theta/2\theta$ scan consists of sweeping the angle of incident x-rays between 5° to 30°, while simultaneously moving the detector by 2θ. However, this method is not ideal for thin films since x-ray penetrate distances between 10 to 100 μm, resulting in a diffraction pattern highlighting the substrate characteristic diffraction while burying the thin film intensity peaks. To circumvent this problem, a Grazing Incident XRD

(GIXRD) is employed as an alternative configuration technique for thin-film phase identification. In a GIXRD, the incident x-ray is fixed at an angle slightly above the critical angle (ω) for total reflection, while a 2θ scan is performed on the detector side.

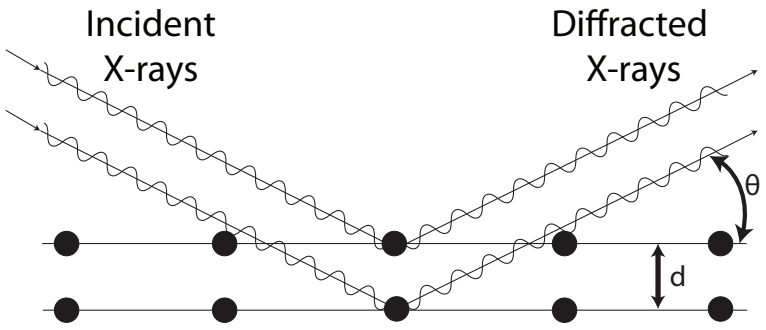

Figure 3.8: Diffraction of x-rays from a crystal structure.

3.2.4 Optical transmission and reflection

The direct and indirect band gap of a thin film is determined by analysis of the absorption spectrum obtained from a transmission and reflection measurement. The reflection coefficient, R, is the ratio of the power reflected to the power incident on the thin film surface, and the transmission coefficient, T, is the ratio of the transmitted power to the incident power [88]. The absorption coefficient, α, is calculated at each incident photon wavelength using Beer's law,

$$\frac{T}{1-R} = e^{-\alpha d} \tag{3.11}$$

where d is the thin film thickness. Figure 3.9 shows an example of what an absorption spectrum might look for a direct and indirect bandgap material. The bandgap and bandgap type is determined by the lowest x-intercept between the linear fit of an α^2

vs. energy or an $\alpha^{1/2}$ vs. energy plot, corresponding to a direct or indirect bandgap, respectively. Figure 3.10 illustrates the extraction procedure used to determine a material's bandgap.

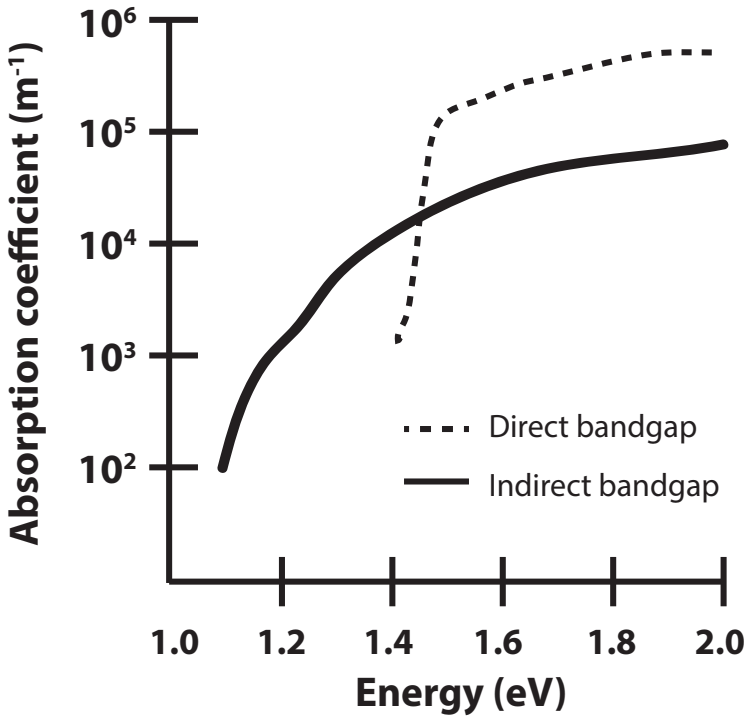

Figure 3.9: Thin film optical absorption spectrum from transmission and reflection measurements for a direct (solid line) and indirect (dashed line) bandgap material.

Figure 3.10 shows a schematic representation of the experimental setup utilized in this thesis to obtained the transmission and reflection coefficient parameters. The incident light source consists of a halogen lamp for the near-infrared (NIR) measurements, and a separate halogen and deuterium lamp for ultraviolet/visible (UV/Vis)

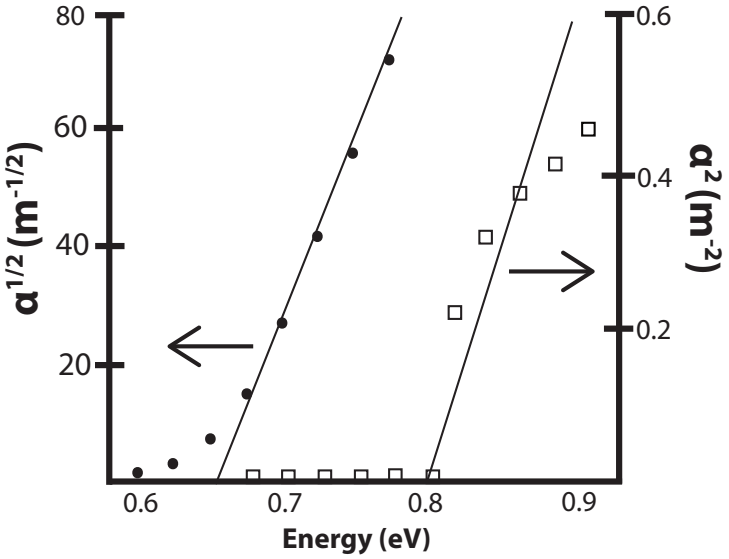

Figure 3.10: Bandgap extraction procedure obtained from thin film optical absorption spectrum data.

measurements. InGaAs and Si detectors are utilized for NIR and UV/Vis measurements, respectively.

3.3 TFT device characterization

TFT performance is assessed from a transfer curve measurement. As illustrated in Fig. 3.12, a transfer curve is the logarithm of drain current plotted as a function of gate voltage ($\log(I_D) - V_G$), while the drain voltage (V_D) is fixed at a $V_D \leq 0.1V$. The very low drain voltage is necessary to ensure that the TFT operates in the linear pre-saturation regime, where $V_D << V_{DSAT} << V_G - V_{ON}$. The performance metrics extracted from a transfer curve are the turn-on and threshold voltage, V_{ON} and V_T, respectively, channel mobility, μ, and drain current on-to-off ratio, I_D^{ON-OFF}.

Qualitative validation of TFT performance can be obtained from an output curve measurement (Fig. 3.13). In an output curve, I_D is plotted as a function V_D, while keeping a fixed V_G bias. An important parameter extracted from an output

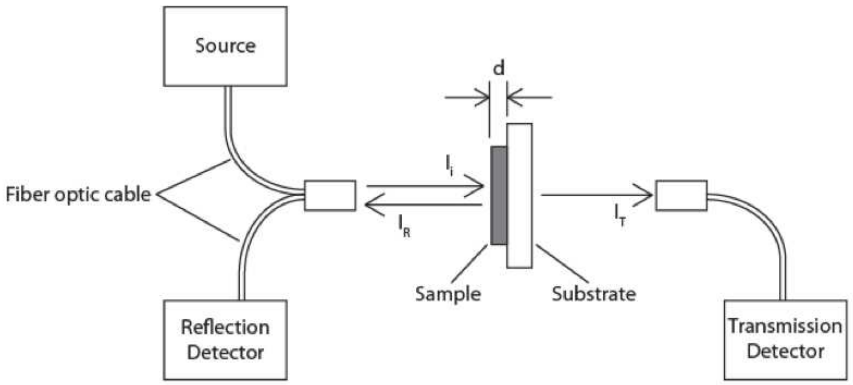

Figure 3.11: Schematic of the experimental setup for the measurement of the optical transmission and reflectance parameters [89].

curve is the drain saturation voltage (V_{DSAT}), the voltage at which the channel is fully depleted and the drain current saturates.

3.3.1 Turn-on and threshold voltage

The turn-on voltage corresponds to the flat-band voltage of the metal-insulator-semiconductor TFT gate terminal. In an n-type TFT, charge accumulation at the insulator-semiconductor interface is accomplished by applying a V_G in excess of the V_{ON}. The charge accumulated is then transported by the drain-to-source potential difference. Hence, V_{ON} is the V_G in a transfer curve where drain current flow begins to increase. Figure 3.12a shows the graphical method to estimate V_{ON} from a $\log(I_D) - V_G$ transfer curve for a depletion-mode device (i.e., $V_{ON} < 0$), and an enhancement-mode device (i.e., $V_{ON} > 0$).

The threshold voltage is the V_G in which significant TFT drain current flows. As shown in Fig. 3.12b, V_T the horizontal axis intercept of a transfer curve straight-line fit. Threshold voltage is of most interest in circuit design, where it used to define a circuit bias for proper operating conditions [90].

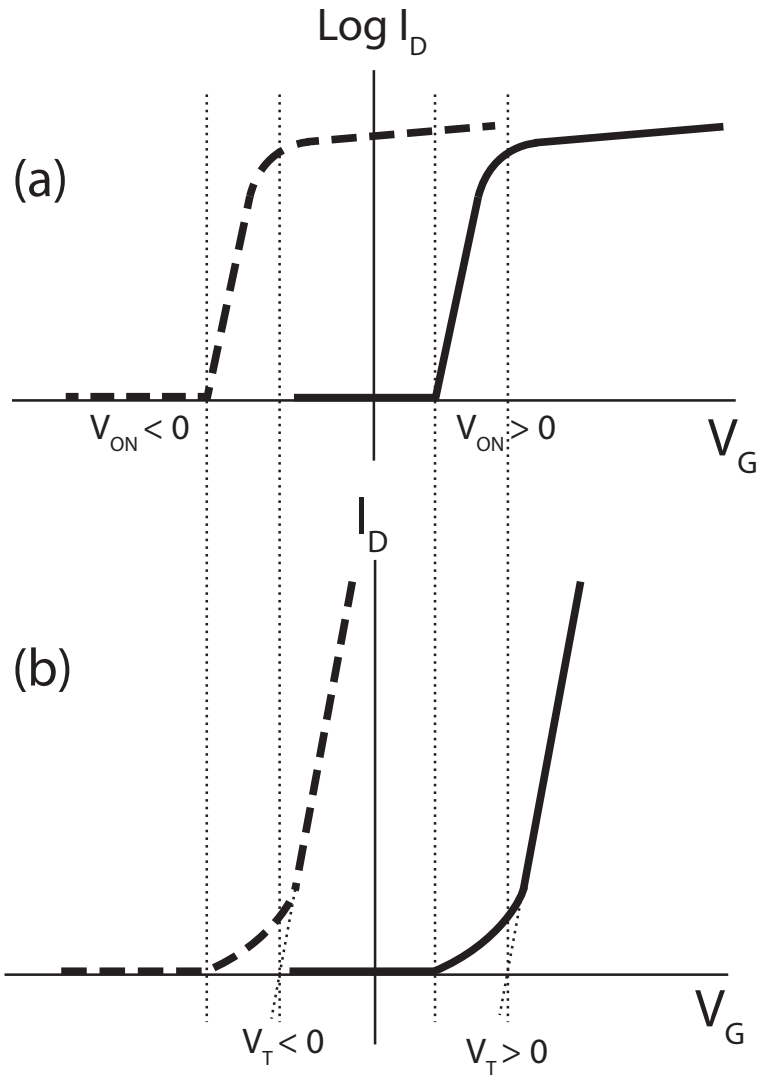

Figure 3.12: Graphical method for estimating the V_{ON} and V_T of a TFT. a) V_{ON} estimation for a depletion- and enhancement-mode device from a $\log(I_D)-V_G$ transfer curve, b) V_T estimation for a depletion- and enhancement-mode device from a I_D-V_G transfer curve.

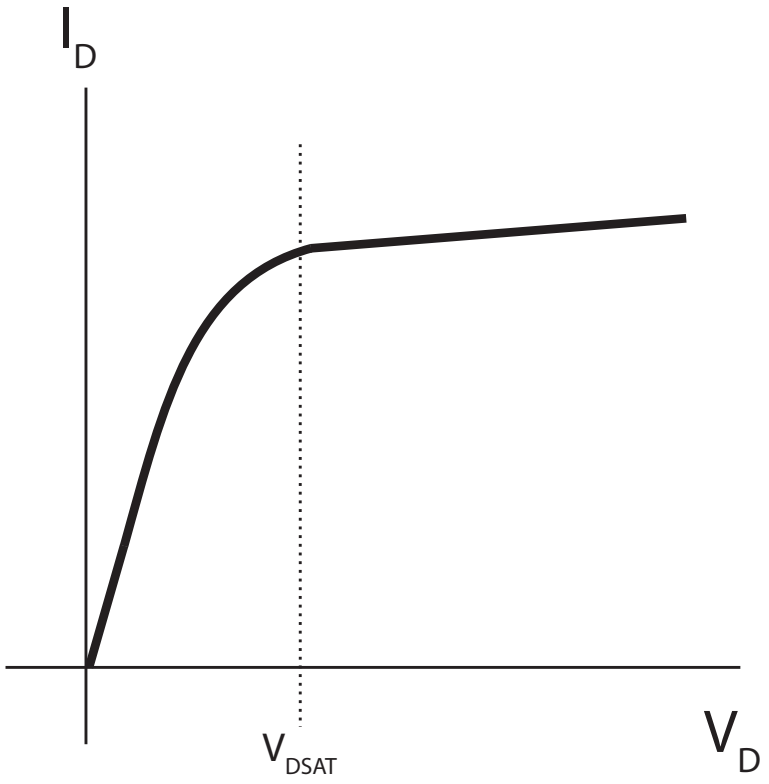

Figure 3.13: Graphical estimation of V_{DSAT} from a TFT output curve.

3.3.2 Channel mobility

Mobility is extracted from a low-drain-source transfer curve to ensure TFT operation in the linear region, i.e., where $V_D \ll V_{DSAT} \ll V_G - V_{ON}$. Two types of mobility are extracted using this method, namely, incremental mobility, μ_{INC}, and average mobility, μ_{AVG}. The μ_{INC} examines the mobility of carriers as they are incrementally accumulated in the channel, therefore it gives insight into channel carrier transport [7]. The equation employed to extract μ_{INC} from experimental data is

$$\mu_{INC} = \left. \frac{\frac{\Delta G_D}{\Delta V_G}}{\frac{W}{L} C_{ins}} \right|_{V_D \ll V_{DSAT}} \tag{3.12}$$

where G_D is the channel conductance

$$G_D = \frac{I_D}{V_D} \tag{3.13}$$

W is the channel width, L is the channel length, and C_{ins} is the insulator capacitance.

The μ_{AVG} is a more general metric to quantify the device performance of interest, mainly, transistor current drive. From experimental data, μ_{AVG} is calculated by

$$\mu_{AVG} = \frac{G_D}{\frac{W}{L} C_{ins} \left(V_{GS} - V_{ON} \right)} \tag{3.14}$$

3.3.3 Drain current on-to-off ratio

The I_D^{ON-OFF} is extracted from a high-drain-source $\log\left(I_D\right) - V_G$ transfer curve, to ensure the TFT operates in the saturation region, where $V_D \geq V_{DSAT} \equiv V_G - V_{ON}$. The I_D^{ON-OFF} can be calculated by

$$I_D^{ON-OFF} \equiv \frac{\max(I_D)}{I_D|_{V_G < V_{ON}}} \tag{3.15}$$

An I_D^{ON-OFF} of 10^6 is considered acceptable, transistors with lower values are impractical due to large amounts of energy wasted from high current conduction during the off state [91].

4. P-TYPE Cu_3SbS_4 THIN-FILM TRANSISTORS

Copper antimony sulfite (Cu_3SbS_4) is a p-type semiconductor primarily studied for its exceptional absorption characteristics that makes it of interest for solar cell applications. Specifically, Cu_3SbS_4 is being studied for the realization of drift-based thin-film solar cells (TFSC) [92]. One way to produce a drift-based solar cell is to engineer a low-doped absorber material. This generates a depletion width and built-in electric-field in the junction of the solar cell that extends over the entire thickness of a thin film absorber. Carriers generated in the absorber layer drift over a larger portion of its thickness, as opposed diffusing towards the eletric field in the space-charge region. Potentially, solar cell efficiency is improved by reducing electron-hole recombination. In this context, p-type absorbers for drift-based TFSCs share a common material exploratory criterion of electrical characteristics to that of TFTs: 1) adequate mobility, and 2) carrier concentration below 10^{16} cm^{-3}. In this chapter, preliminary results of material and TFT characterization are presented for RF sputtered Cu_3SbS_4, and the effect of Zn doping as a mechanism to reduce carrier concentration is explored.

4.1 Methods

Thin films were deposited by RF sputtering on a custom built stainless steel vacuum system at the Oregon State University advanced materials lab. The principle of RF sputtering is discussed in Section 3.1.1. In this work, a custom targets of Cu_3SbS_4 with density $> 99\%$ purchased from Kurt J. Lesker Company. A plasma glow discharge was initiated at a pressure of 15 mTorr using an Ar process gas flow of 15 sccms. Thin films were deposited on 1" x 1" 1737 glass substrates for 105 min. at a process pressure near 5 mTorr. The RF power was varied from 65-95 W using an approximate ramp up/down rate of 5 W/min. Figure 4.1 shows the thickness

and deposition rate measured by surface profilometry using a Tencor AlphaStep 100 profilometer.

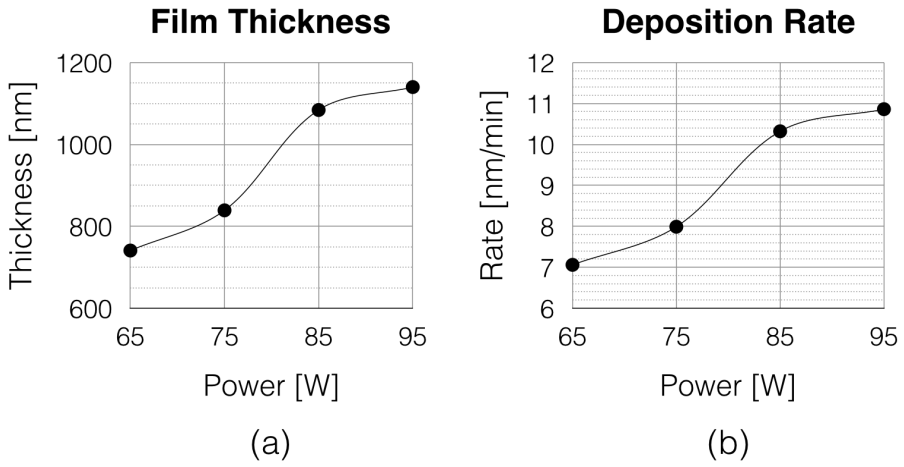

Figure 4.1: Cu_3SbS_4 sputtered thin film a) surface profilometry thickness and b) deposition rate as a function of RF power variation.

Finally, films were subjected to a post-deposition sulfurization anneal. The setup consisted of a furnace equipped with a quartz tube, and Ar gas flow. Samples were placed on a sulfur boat, and the annealing process consisted of 15 min. or 30 min. at a temperature of 275 °C or 300 ° C.

Thin-film transistors were fabricated by RF sputtering on 10 x 15 mm p-type Si substrates with 100 nm of thermally grown SiO_2 on top and bottom Au/Ta gate electrode, and subsequently annealed in sulfur at 275-300 °C. The substrates are cleaned with acetone, isopropropanol, and deionized water (rinsed in the order listed), and subsequently dried in a hot plate for $>$ 10 minutes at a temperature of $\sim$ 220 ° C. The TFT channel dimmensions are W/L = 2000 μm/200 μm, defined by shadow mask. A Au metal is employed for source and drain electrodes, which are thermally

evaporated and shadow-mask defined. Figure 4.2 shows a schematic representation of a) cross-sectional and b) top view of the TFT structure utilized.

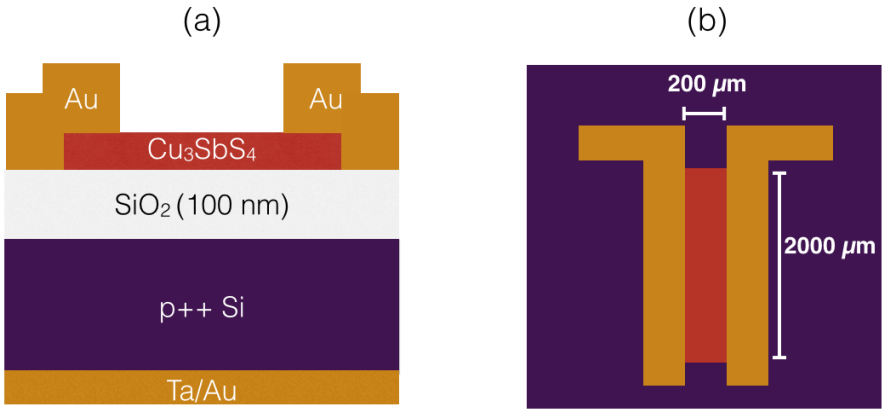

Figure 4.2: Schematic of structural a) cross-sectional and b) top view of a Cu_3SbS_4 TFT.

4.2 Results

4.2.1 Hall-effect characterization

Electrical characteristics of Cu_3SbS_4 thin films were determined from Hall-effect measurements. Hall-effect measurements are discussed in Section 3.2.1. Results presented in this thesis were obtained using a Lakeshore 7504 Hall Measurement System (courtesy of Prof. Janet Tate's Lab, Department of Physics). The Hall-effect system features an electromagnet with a capability to produce magnetic fields up to ~2 T. Figure 4.3 shows a schematic representation of the van der Pauw configuration employed for resistivity measurements, where thermally evaporated Au contact were patterned by shadow mask.

Figure 4.4 shows measured (a) average resistivite, ρ, (b) carrier concentration, p, and (c) Hall mobility, μ_{Hall}. The Hall-measurement is obtained using Cu_3SbS_4

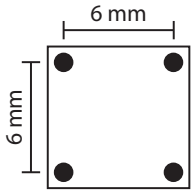

Figure 4.3: Schematic of the van der Pauw configuration utilized for Cu_3SbS_4 Hall-effect measurements. The black dots represent shadow-mask-patterned thermally-evaporated Au electrodes.

thin films with a thickness of $\sim 1\mu$m. The deposition conditions consist of a 5 mTorr process pressure and RF power of 65 W. The post-deposition processing consists of a 30 min anneal at 300 °C using Ar gas flow, and placing the samples on a sulfur boat. There is a consistency in measured values of ρ, p, and μ_{Hall} for negative and positive magnetic fields, so that a variation of < 5 % in average values is observed at applied magnetic flux density between -20 kG and 20 kG. Table 4.1 summarizes the Hall-effect results measured using various sputtering RF power depositions. The Cu_3SbS_4 thin film samples have a thickness of ~ 1 μm, which were deposited at a process pressure of 5 mTorr, and later annealed for 30 min. at 275 °C or 300 °C.

Table 4.1: Cu_3SbS_4 thin film Hall-effect results measured using various sputtering RF power depositions.

Power [W]	Resistivity [mΩ-cm]		Carrier Concentration [cm^{-3}]		Mobility [$cm^2V^{-1}s^{-1}$]	
	275 °C	300 °C	275 °C	300 °C	275 °C	300 °C
65	299	470	1.70×10^{18}	7.65×10^{17}	12.3	17.2
75	279	288	1.44×10^{18}	1.55×10^{18}	15.7	14.0
85	233	291	2.60×10^{18}	1.50×10^{18}	10.3	14.3
95	61	324	6.20×10^{18}	2.10×10^{18}	16.5	9.1

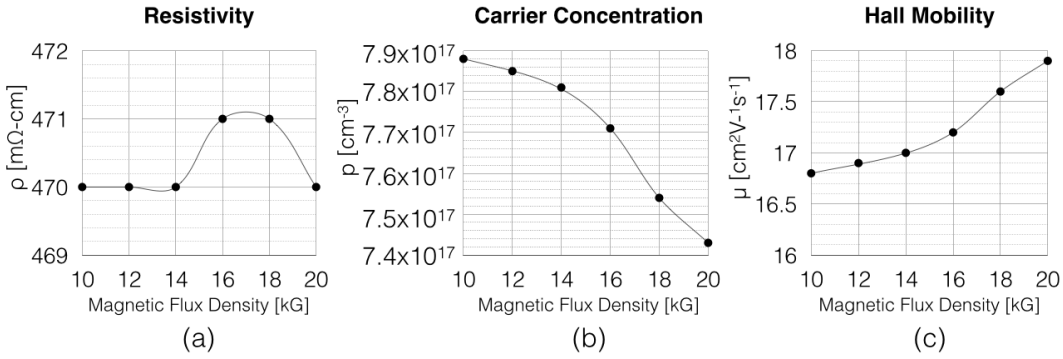

Figure 4.4: Cu_3SbS_4 thin film Hall-effect measurement results of (a) resistivity, (b) carrier concentration, and (c) Hall mobility for a thickness of $\sim$1 μm. The deposition condition are: process pressure of 5 mTorr, and sputtering RF power of 65 W. The post-deposition processing consists of a 30 min furnace anneal at 300 °C using Ar gas flow, and placing the samples on a sulfur boat.

4.2.2 Thin-film transistor I-V characteristics

Figure 4.5 shows the a) output and b) transfer curve characteristics, and c) incremental mobility of a Cu_3Sb_4 TFT. The RF sputtered Cu_3SbS_4 TFTs are fabricated on 10 x 15 mm p-type Si substrates with 100 nm of thermally grown SiO_2 on top. The sputtering conditions are: power = 65 W, 15 sccm Ar gas flow, and pressure = 5 mTorr. The profiled thickness is 6-8 nm as deposited, and it increases to $\sim$ 20 nm after annealing in sulfur at 275 °C for 15 min.

The output and transfer curves shown in Fig. 4.5 exhibit p-type I-V behavior. The maximum output drain current increases as a more negative gate voltage is applied, which is evidence that the gate terminal is able to modulate the channel conductance. However, the channel modulation is very poor, showing a change in drain current at V_D = -20 V from -1.4$\times10^{-4}$ A to only -2.2$\times10^{-4}$ A for V_G = -0.1 V and V_G = -20 V, respectively (Fig. 4.5a). The transfer curve shows that the TFT operate in depletion-mode, revealing that the semiconductor channel has high a carrier concentration (Fig. 4.5b). The maximum incremental mobility, drain current

hysteresis, and subthreshold swing is measured to be ~ 0.5 cm^{2}V^{-1}s^{-1}, > 7 V, and ~ 70 V/dec, respectively.

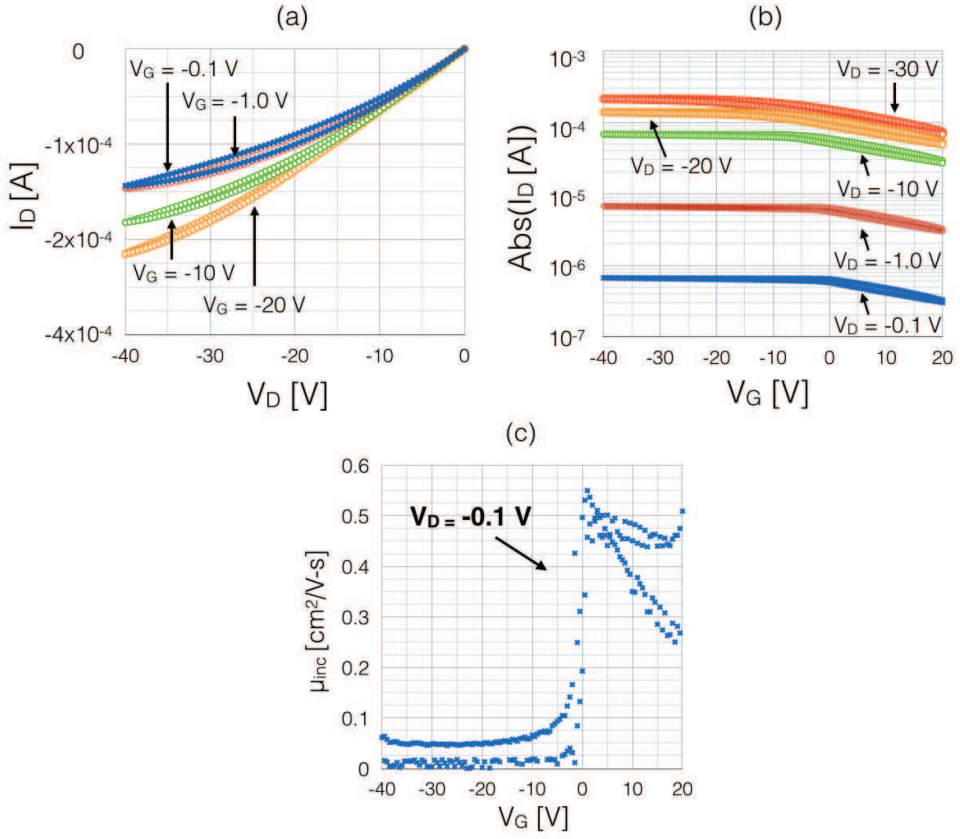

Figure 4.5: Cu_3SbS_4 thin-film transistor a) output and b) transfer curves, and c) incremental mobility for a $\sim$ 20 nm thick channel. TFTs are fabricated by RF sputtering on 10 x 15 mm p-type Si substrates with 100 nm thermally grown SiO_2 on top, and subsequently annealed at 275°C for 15 minutes in a sulfur environment. Depositions conditions are: power = 65 W, 15 sccm Ar gas flow, and pressure = 5 mTorr.

Figure 4.6 shows a Cu_3SbS_4 TFT a) transfer curve, where the gate voltage sweep is increased up to 60 V in order to explore the V_G necessary to deplete the channel and turn off the device. The drain current does not saturate to a minimum

off current, suggesting that the turn-off voltage is beyond V_G = 60 V, where dielectric catastrophic breakdown occurs. The average mobility (Eq. 3.14) cannot be determined without knowledge of the turn-on voltage. Hence, only the incremental mobility is reported (Fig. 4.5c).

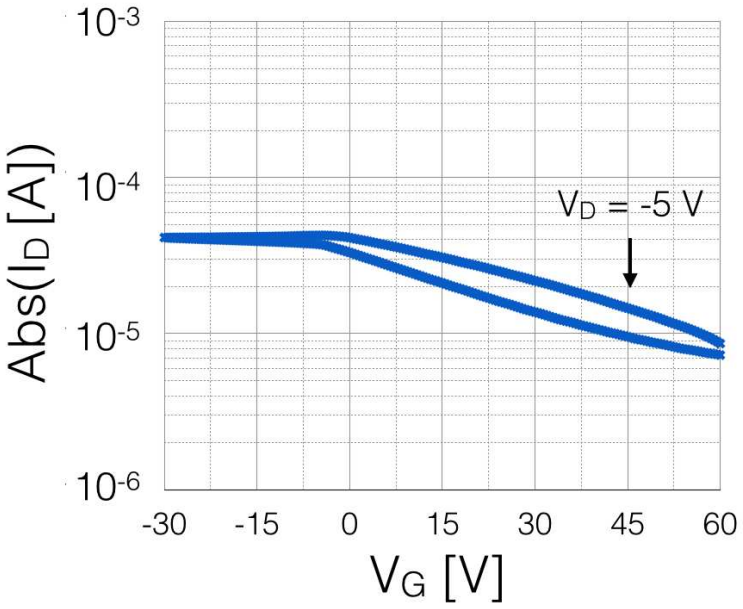

Figure 4.6: Cu_3SbS_4 thin-film transistor transfer curves for a $\sim$ 20 nm thick channel, fabricated by RF sputtering on 10 x 15 mm p-type Si substrates with 100 nm thermally grown SiO_2 on top, and subsequently annealed at 275°C for 15 minutes in a sulfur environment. Depositions conditions are: power = 65 W, 15 sccm Ar gas flow, and pressure = 5 mTorr.

4.2.3 Comprehensive depletion-mode modeling

The TFT transfer curves reported in Section 4.2.2 is further analyzed using the comprehensive depletion-mode model (CDMM) [1, 3]. The CDMM can be used to gain knowledge of carrier concentration and understanding of interface mobility and bulk mobility.

There are two main p-channel TFT regions of operation in the CDDM: 1) depletion region ($V_G > 0$), and 2) accumulation region ($V_G < 0$). The depletion and accumulation regions are divided into further regions of operation. In the depletion region there is: 1) pre-saturation region, and 2) saturation region. In the accumulation region there is: 1) pre-saturation region, 2) depletion region, 3) and saturation region. Table 4.2 summarizes the drain current equations and constraints defined in the CDMM.

Simulations using the CDMM are complemented using subpinchoff and off drain current contributions, where the procedure is summarized in Table 4.3. The lowest measured current in the depletion region is taken to be the drain off-current, since the off-current of the TFTs reported herein is undetermined from experimental measurements.

Figure 4.7 shows the transfer curve simulation results using the CDMM. The simulation parameters are μ_{bulk} = 0.45 $cm^2V^{-1}s^{-1}$, $\mu_{interface}$ = 0.04 $cm^2V^{-1}s^{-1}$, carrier concentration = 4×10^{18} cm^{-3}, channel thickness of 22 nm, and semiconductor relative dielectric constant of 18.5. The simulations provide a close fit to experimental transfer curves, with the exception of the transfer curves with V_D = -20 V, and V_D = -30 V. The poor fit is attributed to non-idealities that prevent the Cu_3SbS_4 TFT channel to be depleteded of carriers, as the CDDM predicts in the ideal case. The extracted carrier concentration from CDDM simulations is shown to be in close agreement with Hall-effect measurements.

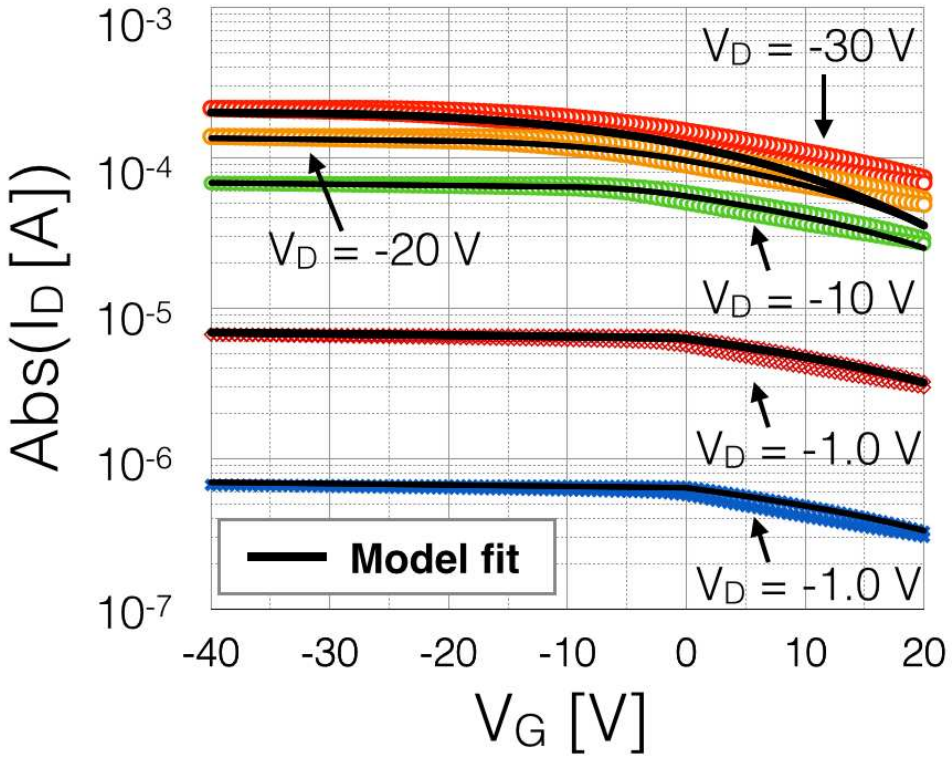

Figure 4.7: Cu_3SbS_4 thin-film transistor experimental transfer curves (colored), and simulation fit (black) using the comprenhensive depletion-mode model. TFTs are fabricated by RF sputtering on 10 x 15 mm p-type Si substrates with 100 nm thermally grown SiO_2 on top, and subsequently annealed at 275°C for 15 minutes in a sulfur environment. Deposition conditions are: power = 65 W, 15 sccm Ar gas flow, and pressure = 5 mTorr. The simulation parameters are $\mu_{bulk} = 0.45$ $cm^2V^{-1}s^{-1}$, $\mu_{interface} = 0.04$ $cm^2V^{-1}s^{-1}$, carrier concentration = 4×10^{18} cm^{-3}, channel thickness of 22 nm, and semiconductor relative dielectric constant of 18.5.

Table 4.2: Summary of p-channel TFT drain current equations and voltage constraints defined by the comprehensive depletion-mode model [1].

Equation	Voltage Constraint
Depletion region	
$I_{D,PRESAT}^{DEP} = \frac{W}{L}\sigma h\left\{\left(1+\frac{C_S}{C_G}\right)V_D - \frac{2}{3}V_P\left[\left(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P}\right)^{3/2} - \left(\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P}\right)^{3/2}\right]\right\}$	$0 < V_G \leq V_{PO}$, $V_D < V_{DSAT}$
$I_{D,SAT}^{DEP} = \frac{W}{L}\sigma h\left\{\left(1+\frac{C_S}{C_G}\right)V_{DSAT} - \frac{2}{3}V_P\left[\left(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P}\right)^{3/2} - \left(\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P}\right)^{3/2}\right]\right\}$	$0 < V_G \leq V_{PO}$, $V_D \geq V_{DSAT}$
Accumulation region	
$I_{D,PRESAT}^{ACC} = \frac{W}{L}\left[-\mu_{interface}C_G\left(V_G V_D - \frac{V_D^2}{2} + \sigma h V_D\right)\right]$	$V_G \leq 0$, $V_D < V_G < V_{DSAT}$
$I_{D,PRESAT}^{ACC-DEP} = -\frac{W}{2L}\mu_{interface}C_G V_G^2 - \frac{W}{L}\sigma h V_G - \frac{W}{L}\sigma h\left\{\left(1+\frac{C_S}{C_G}\right)(V_D - V_G) - \frac{2}{3}V_P\left[\frac{C_S^3}{C_G^3}, -\left(\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P}\right)^{3/2}\right]\right\}$	$V_G \leq 0$, $V_G \leq V_D < V_{DSAT}$
$I_{D,SAT}^{ACC} = -\frac{W}{2L}\mu_{interface}C_G V_G^2 - \frac{W}{L}\sigma h V_G - \frac{W}{L}\sigma h\left\{\left(1+\frac{C_S}{C_G}\right)(-V_{PO}) - \frac{2}{3}V_P\left[\frac{C_S^3}{C_G^3}, -\left(\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P}\right)^{3/2}\right]\right\}$	$V_G < 0$, $V_D > V_{DSAT}$

Model Parameters	Equation
Channel conductance	$\sigma = \mu_{bulk} q p_{vo}$
Threshold voltage	$V_T = -\frac{q p_{to} h}{2C_S} - \frac{q p_{to} h}{C_G}$
Pinch-off voltage	$V_{PO} = V_P + \frac{q p_{vo} h}{C_G}\left(V_P = \frac{q p_{vo} h}{2C_S}\right)$
Saturation voltage	$V_{DSAT} = V_G - V_{PO}$ or $V_{DSAT} = V_G - V_T$
Geometric-based	W (width), L (length), h (channel thickness), C_G (gate insulator capacitance density)
Channel-based	p_{vo} (hole concentration in the valence band at zero bias), p_{to} (empty trap density at zero bias), $\mu_{interface}$ (interface mobility), μ_{bulk} (bulk mobility), C_S (channel layer capacitance density)

4.3 Conclusions

Cu_3SbS_4 thin films exhibit Hall-effect hole mobility of 14-16 cm^2/V-s and a hole carrier concentration of 10^{17} cm^{-3}. Cu_3SbS_4 TFTs demonstrated p-type, depletion-mode behavior with a small amount of gate-controlled modulation of the channel conductance. The Cu_3SbS_4 TFT assessment demonstrated an incremental mobility of ~ 0.5 $cm^2V^{-1}s^{-1}$, drain current hysteresis of > 7 V, and subthreshold swing of $\sim$ 70 V/dec.

Comprehensive depletion-mode modeling (CDMM) simulation fits to experimental transfer curves were conducted to extract Cu_3SbS_4 TFT carrier concentra-

Table 4.3: Summary of subpinchoff drain current equations and voltage constraints used for depletion-mode p-channel TFT transfer curve simulations [1].

Drain Current Equation	Voltage Constraint
$I_{OFF} = V_D \left(\frac{1}{R_{surface}} + \frac{1}{R_{bulk}}\right) + I_G$	$V_G \geq V_{OFF}$
$I_{D,SUB} = \frac{W}{L}\mu C_G \left(\frac{k_B T}{q}\right)^2 \exp\left[\frac{q(V_G - V_{OFF})}{\left(1+\frac{C_{DOS}}{C_G}\right)k_B T}\right]\left[1 - \exp\left(\frac{-qV_D}{k_B T}\right)\right]$	$V_G \leq V_{OFF}$
$\frac{1}{I_D} = \frac{1}{I_{D,PRESAT}} + \frac{1}{I_{D,SUB}}$, $I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \leq V_{OFF}$, $V_D > V_{DSAT}$
$\frac{1}{I_D} = \frac{1}{I_{D,SAT}} + \frac{1}{I_{D,SUB}}$, $I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \leq V_{OFF}$, $V_D \leq V_{DSAT}$

$R_{surface}$ (surface resistance), R_{bulk} (bulk resitance), I_G (gate leakage current), C_{DOS} (channel layer density of states capacitance density)

tion, and interfacial and bulk mobility. Parameters extracted from CDMM simulation are found to be $\mu_{interface} = 0.04$ cm^{2}V^{-1}s^{-1}, $\mu_{bulk} = 0.45$ cm^{2}V^{-1}s^{-1}, and carrier concentration of 4×10^{-17}cm^{-3}. The parameters extracted from CDMM simulations provided a close fit to Cu_3SbS_4 TFT experimental transfer curves. The CDMM extracted carrier concentration is in close agreement with Hall-effect measurements.

5. SOLUTION-PROCESSED TFTs

Solution-processing of thin film materials promises to be a sustainable and cost-effective method for manufacturing next-generation electronics products. Section 2.3 overviews electronic applications that have been proposed using solution-processing, and the potential cost-savings benefits expected compared to traditional state-of-the-art microelectronics manufacturing. This chapter describes TFTs fabricated using either a solution-processed semiconductor or insulator thin-film layer. The aim here is to contribute to the advancement of solution-processed electronics. The work described in this chapter is divided in three main sections: 1) assessment of TFT performance using a solution-processed IGZO and dual active-layer semiconductor layer with a thermally grown SiO_2 gate insulator, 2) assessment of sputtered IGZO TFT performance with a solution-processed Al_2O_3 or $LaAlO_3$ gate insulator, and 3) Dual active-layer solution-processed TFTs.

5.1 Solution-processed IGZO TFTs

This section describes development of spin-coated IGZO TFTs using a new electrochemical synthesis procedure from IGZO solutions of various compositions. Previous work on IGZO solution-processing by various research groups is presented in Section 2.3.1.1. The electrochemical synthesis procedure employed involves a new IGZO solution chemistry as prepared by Dr. Athavan Natadarajah, a post-doctoral scholar from Prof. Boettcher's Lab at the University of Oregon, working for the Center for Sustainable Material Science (CSMC). The objective of this electrochemical method development effort is to produce highly dense thin films at low temperatures and to accomplish this by avoiding the use of non-functional counterions in the solution chemistry, such as organic ligands that produce porous thin films as they decompose or evaporate upon heating [93]. A simplified description of the solution preparation methodology is provided here, but the primary focus of the work

described herein is to demonstrate TFT performance using electrochemically synthesized IGZO solutions of various compositions.

5.1.1 Methods

5.1.1.1 Electrochemistry synthesis procedure

Figure 5.1 shows a schematic of the custom-built electrolysis equipment utilized to synthesize IGZO solutions. Salt powders of $In(NO_3)_3$, $Ga(NO_3)_3$, and $Zn(NO_3)_2$ are dissolved in water in the two compartments. Three electrodes are utilized: cathode, anode, and reference electrode. A potential of -0.5 V is applied between the cathode and anode. Consequently, nitrates migrate towards the anode, and metal ions towards the cathode. The pH of the solution can be precisely controlled by measuring charge ($Q = It$). The solution produces clusters of 0.8-1 nm which are stable for < 2 hours.

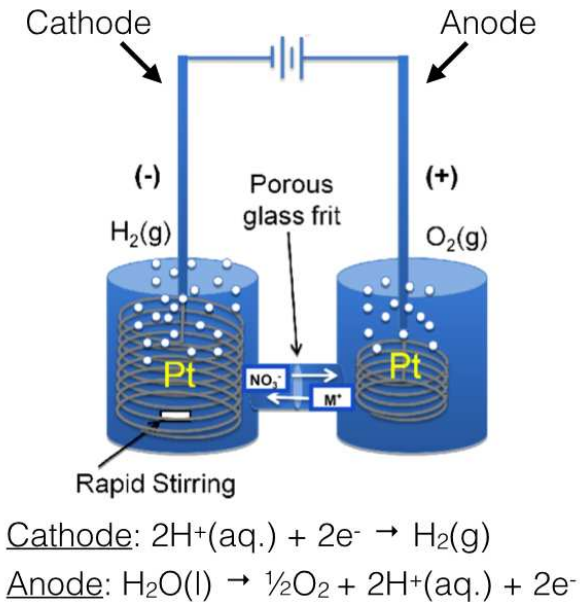

Figure 5.1: Schemematic of electrochemical equipment utilized to produce IGZO solutions [55].

5.1.1.2 TFT Fabrication

Thin films are fabricated on 1" x 1" degenerately-doped p-type Si ($\rho < 1$ $\Omega-$cm) substrates with 100 nm of thermally grown SiO_2 on top and a Au/Ta bottom electrode. Electrochemically prepared solutions of IGZO are spin-coated at 3000 RPM for 30 sec, followed by a hot plate bake for 30 min at 300 °C. The films are later annealed in air at 300-550 °C inside a furnace for 2 hours with a ramp up/down rate of 2 °C/min.

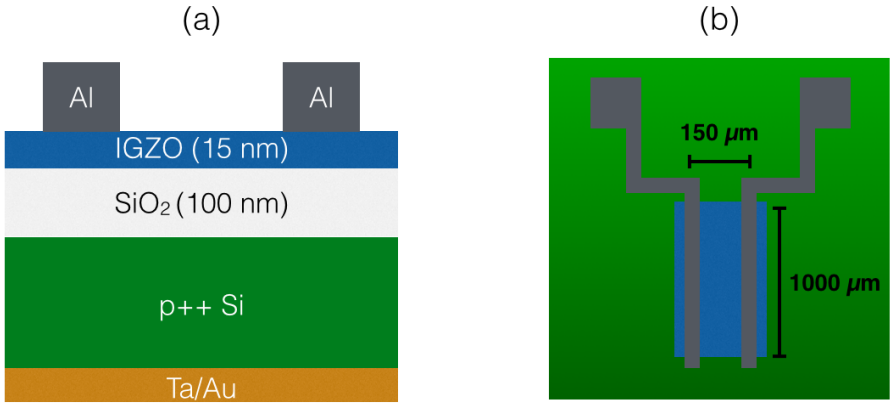

Figure 5.2: Schematic of structural a) cross-sectional and b) top view of a solution-processed IGZO TFT.

Figure 5.2 shows a schematic of the a) cross-sectional and b) top structure of TFTs fabricated. The TFT channel is defined using a photolithographic process. A positive S1818 photoresist is exposed after alignment to a UV light for 12 sec, and developed in 4:1 volume ratio of 351 developer for 2-3 minutes. The TFT channel is patterned by a wet etch process using an HCl (12.1 M) solution for ∼10 sec. The samples are then placed on a hot plate at 300 °C for 10 minutes to remove residues leftover from the lithographic process. This hot plate bake is found to significantly reduce TFT drain current hysteresis (Fig.5.3). Finally, shadow-masked Al source and

drain contacts are deposited by thermal evaporation at a pressure $< 3{\times}10^{-5}$ mbar ($< 2.25 \times 10^{-5}$ Torr).

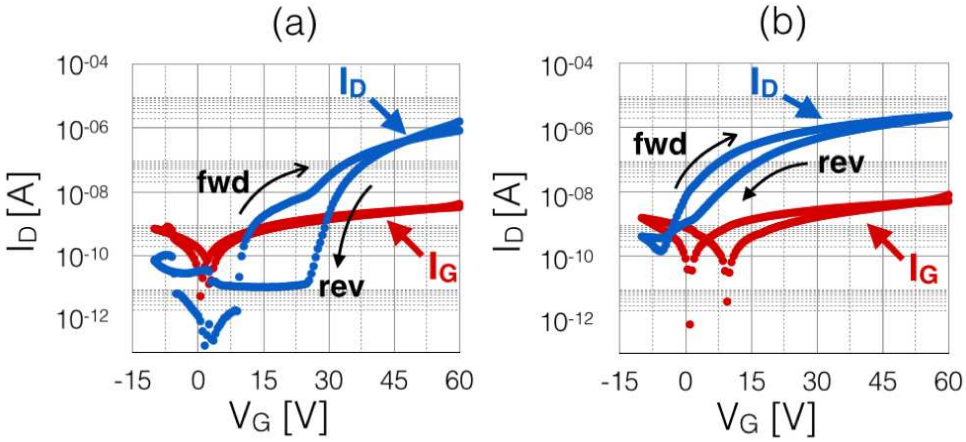

Figure 5.3: Transfer curve hysteresis observed for a photolithographically-defined, solution-processed IGZO TFT a) before and b) after a 10 minute 300 °C hot plate bake. The IGZO (15 nm) is spin-coated using a 2 hour electrolyzed solution with a composition of In:Ga:Zn = 0.33:0.33:0.33, and subsequently annealed at 550 °C in air.

5.1.2 Results

5.1.2.1 Grazing-incidence X-ray diffraction

Figure 5.4 shows the grazing-incidence X-ray diffraction (GI-XRD) patterns of In-rich IGZO thin films spin-coated with a In:Ga:Zn = 0.70:0.15:0.15 solution electrochemically prepared for 1 hour and subsequently annealed at 400-800 °C. The films are deposited on 1" x 1" substrates of degenerately-doped p-type Si with 100 nm SiO_2 on top. The XRD analysis reveals the presence of broad diffraction peaks when samples are annealed below 600 °C. As discussed in Section 3.2.3, broad peaks in a XRD pattern is characteristic of an amorphous micro-structure. The retention

of an amorphous micro-structure is a designed fabrication requirement considered to produce large-area electronics and improve performance (Section 2.3.1). However, solution-processed thin films fabricated in this work benefit from increasing annealing temperature in order to approach towards a film completely free of nitrates and water residual from the the spin-coated solution. Hence, an annealing temperature of 550 °C is explored, a temperature below the 600 °C onset of crystallization observed in Fig. 5.4.

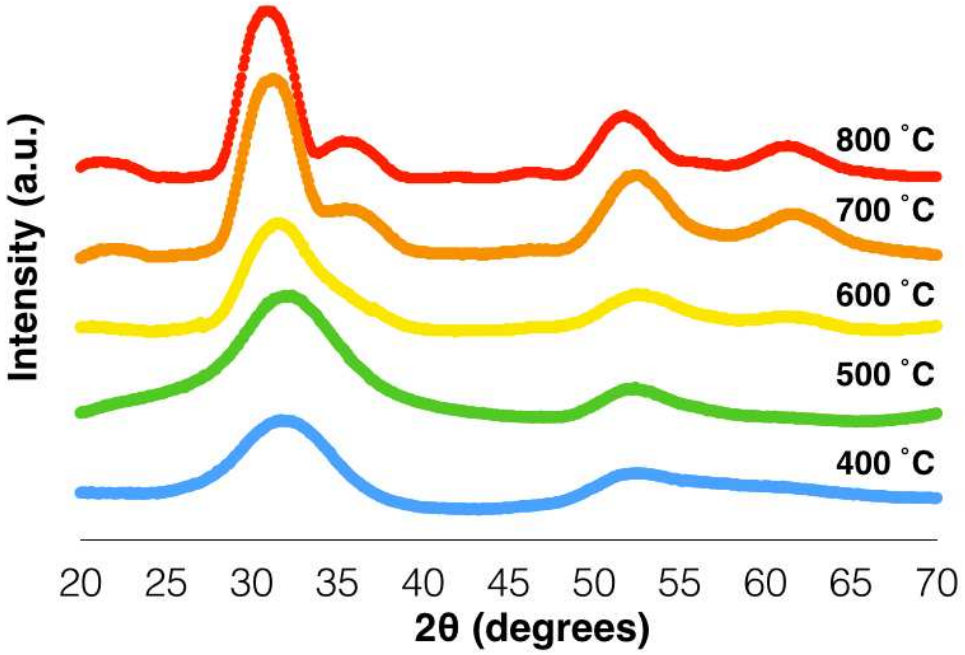

Figure 5.4: The Grazing-incidence X-ray diffraction of spin-coated IGZO (15 nm) thin films using a 1 hour electrochemically synthesized solution with a composition of In:Ga:Zn = 0.7:0.15:0.15. The thin films are fabricated on 1" x 1" substrates of degenerately-doped p-type Si with 100 nm SiO_2 on top. The samples were annealed in air inside a furnace at 400-800 °C.

Figure 5.5 shows the GI-XRD of spin-coated 15 nm IGZO thin films annealed at 550 °C in air with electrochemically prepared solutions with In:Ga:Zn compositions of 0.33:0.33:0.33 (blue), 0.4:0.2:0.2 (green), and 0.7:0.15:0.15 (yellow). All films are deposited on 1" x 1"substrates of degenerately-doped p-type Si with 100 nm on top. The broad diffraction peaks from all the samples of different compositions indicate that the thin films retain an amorphous micro-structure after a 550 °C anneal in air. However, it is important to point out that an XRD pattern is not sufficient to conclude with confidence that the samples measured are strictly amorphous without support data from other film analysis techniques (i.e., AFM[1], TEM[2], PDF[3], etc.).

5.1.2.2 X-ray reflectivity

Figure 5.6 shows the experimental and modeled X-ray reflectivity (XRR) profiles of IGZO thin films spin-coated with a 1 hour electrochemically synthesized In:Ga:Zn = 0.33:0.33:0.33 solution, and subsequently annealed in air at 300-550 °C. XRR analysis is performed to determine thin film thickness, density, and roughness. Modeling of measured XRR data is accomplished using a 3-layer structure: 1) SiO_2 substrate, 2) IGZO bulk, and 3) IGZO "crust" layer; a better modeling fit results when a 3-layer structure is employed.

Table 5.1 shows a summary of the modeling parameters employed to fit the measured XRR data. The thickness is found to be $\sim$ 11–14 nm, where the sample annealed at 550 °C is the thinnest at 11.09 nm. The film roughness increased from 0.70 nm (300 °C anneal) to 0.87 nm (550 °C anneal). The density of the films is compared to an averaged density of 6.208 gm/cm^3, calculated from theoretical density values of In_2O_3, Ga_2O_3, and ZnO bulk crystals. The density is found to increase from 4.91 gm/cm^3 (79.1 %) to 5.12 gm/cm^3 (82.5 %) for samples annealed in air at 300 °C and

[1]Atomic force microscopy
[2]Transmission electron microscopy
[3]Pair distribution function [94]

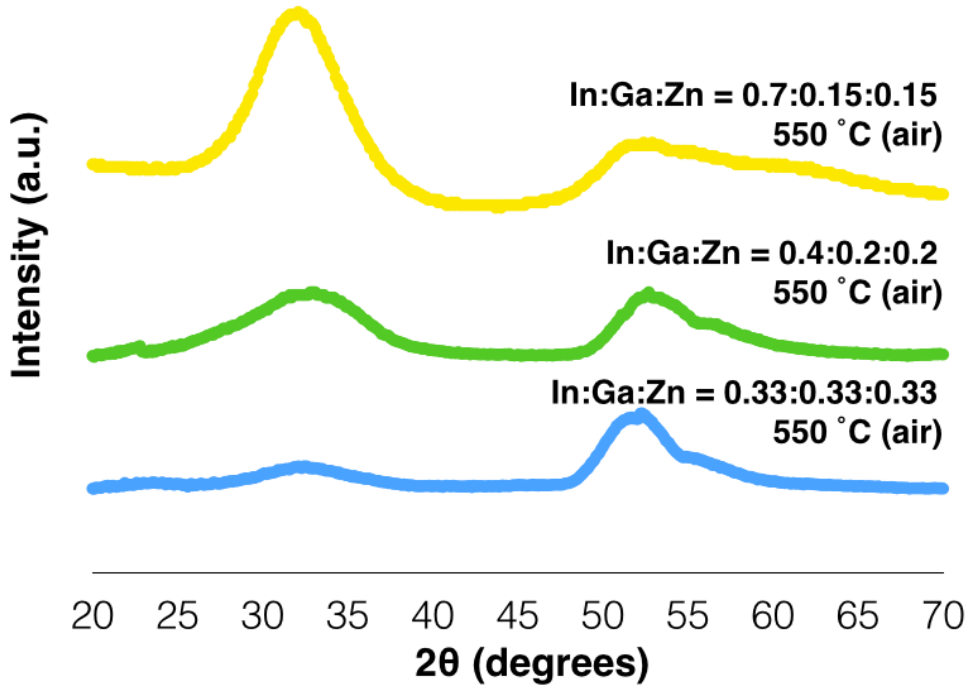

Figure 5.5: The grazing-incidence X-ray diffraction patterns of spin-coated IGZO (15 nm) thin films annealed at 550 °C in air using electrochemically prepared solutions with In:Ga:Zn compositions of 0.33:0.33:0.33 (blue), 0.4:0.2:0.2 (green), and 0.7:0.15:0.15 (yellow) electrolyzed for 1 Hr. The film are fabricated on degenerately-doped p-type Si with 100 nm of SiO_2 on top.

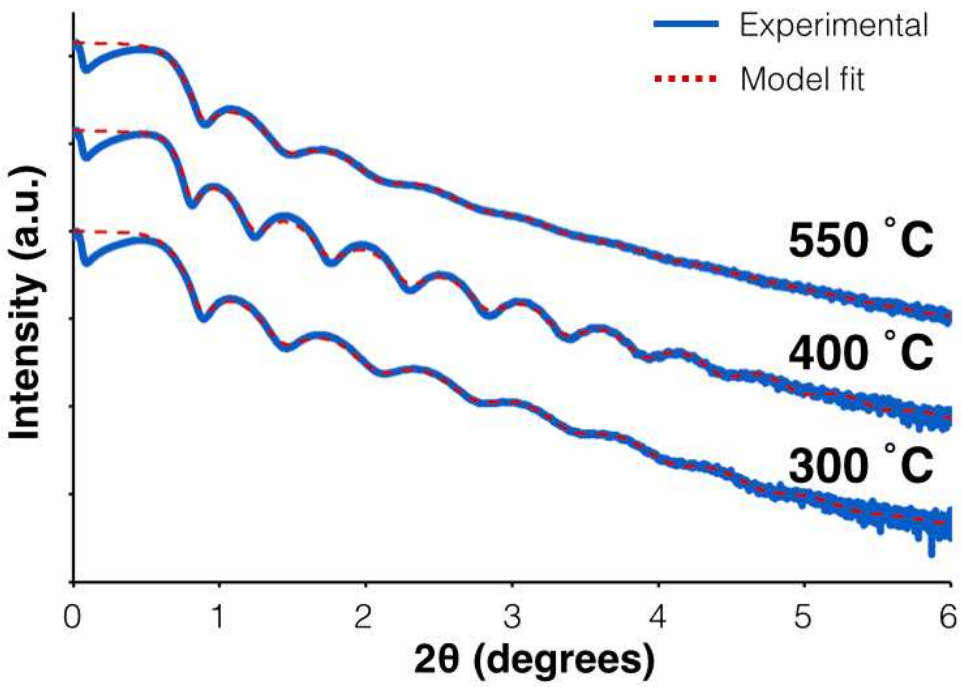

Figure 5.6: X-ray reflectivity experimental (solid lines) and model fit (dash lines) profiles of solution-processed IGZO thin films, spin-coated on p-Si/SiO_2 (100 nm) substrates using an In:Ga:Zn = 0.33:0.33:0.33 electrochemically prepared solution (electrolyzed for 1 hour).

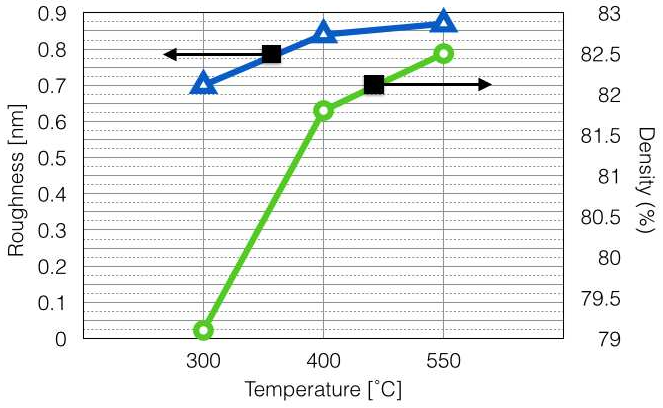

Figure 5.7: X-ray reflectivity density and roughness of solution-processed IGZO thin films, spin-coated on p-Si substrates with 100 nm of thermanlly grown SiO_2 on top, using an In:Ga:Zn = 0.33:0.33:0.33 electrochemically prepared solution (electrolyzed for 1 hour).

Table 5.1: XRR modeling parameters for solution-processed In:Ga:Zn (0.33:0.33:0.33) thin films.

T_A[a]	#	Layer	Thickness [nm]	Density [gm/cm^3]	[%]	Roughness [nm]	R-factor	χ^2
	1	SiO_2	-	2.20	-	0.73		
300 °C	2	IGZO	11.5	4.91	79.1	0.70	0.019	0.007
	3	IGZO	1.70	7.45	120	0.50		
	1	SiO_2	-	2.20	-	0.65		
400 °C	2	IGZO	14.0	5.08	81.8	0.84	0.019	0.007
	3	IGZO	2.04	7.36	119	0.52		
	1	SiO_2	-	2.20	-	0.98		
550 °C	2	IGZO	11.1	5.12	82.5	0.87	0.014	0.003
	3	IGZO	1.99	7.33	118	0.46		

[a]Annealing temperature

550 °C, respectively. Figure 5.7 illustrates a plot of the resulting density and film roughness modeled as a function of annealing temperature.

5.1.2.3 Thin-film transistors I-V characteristics

Figure 5.8 shows the a) transfer curve characteristics and b) average channel mobility of solution-processed IGZO TFTs, spin-coated with electrochemically prepared solutions (electrolysed for 1 hour) of composition 0.33:0.33:0.33 (red), 0.4:0.2:0.2 (blue), and 0.7:0.15:0.15 (green), and subsequently annealed at 550 °C in air for 2 hours. The TFTs with In:Ga:Zn composition of 0.33:0.33:0.33 and 0.4:0.2:0.2 exhibit enhancement-mode behavior with a $V_{ON} \approx 4$ V, and a clockwise drain current hysteresis < 2 V. The In-rich sample (In:Ga:Zn = 0.7:0.15:0.15) exhibits depletion-mode TFT behavior with a $V_{ON} \approx -20$ V, and a clockwise hysteresis $\sim$ 5 V. The highest (lowest) mobility was measured for the IGZO TFT with composition of 0.33:0.33:0.33 (0.4:0.2:0.2). However, the IGZO TFT with composition of 0.7:0.15:0.15 is a depletion-mode TFT. Mobility may be overestimated in a depletion-mode TFT due to an artifact introduced in a channel with excessive carrier concentration (i.e., $> 10^{16}$ cm^{-3}), which creates a high mobility conduction path in the bulk of the channel [1].

Table 5.2: Summary of solution-processed IGZO TFT performance.

Composition In:Ga:Zn	T_A [°C]	Mobility [$cm^2V^{-1}s^{-1}$]	V_{ON} [V]	ΔV [a] [V]	I_D^{ON-OFF}	S [b] [V/Dec]
0.33:0.33:0.33	300	2.75	16	2	5.5×10^3	3.84
	400	5.76	6	1.5	1.2×10^5	2.75
	550	11.9	4	1	3.6×10^5	1.76
0.4:0.2:0.2	550	3.25	4	0.5	1.1×10^5	1.74
0.7:0.15:0.15	550	9.42	-20	3	1.0×10^6	3.32
Sputtered (1:1:1)	400	16.8	5	0.2	1.6×10^6	0.23

[a] Drain current hysteresis
[b] Subthreshold swing

Figure 5.8 shows the a) transfer curve characteristics and b) average channel mobility of solution-processed IGZO TFTs, spin-coated with electrochemically prepared solutions (electrolysed for 1 hour) of composition 0.33:0.33:0.33, and subsequently annealed at 300-550 °C in air. Overall, increasing annealing temperature demonstrated improved TFT mobility from ~ 3 $cm^2V^{-1}s^{-1}$ to ~ 12 $cm^2V^{-1}s^{-1}$, V_{ON} from 16 V to 4 V, drain current hysteresis from 2 V to 1 V, drain current on-to-off ratio from $\sim 10^3$ to $\sim 10^5$, and subthreshold swing from ~ 3.84 V/dec to ~ 1.76 V/dec for samples annealed at 300 °C and 550 °C, respectively. Table 5.2 shows a summary of the performance observed for various solution-processed IGZO TFTs, and a standard sputtered IGZO TFT of similar thickness (i.e., ~ 15 nm).

The improvement in TFT performance observed when annealing temperature is increased may be related to film density (Fig. 5.7). Higher annealing temperatures removes additional residue from the solution precursor (i.e., nitrates and water), and it further densifies the film by quenching remaining pores. Consequently, the fabricated thin films approach optimal levels for carrier concentration and mobility to produce solution-processed TFTs of comparable performance to a sputtered IGZO TFT of similar channel thickness (Fig. 5.9).

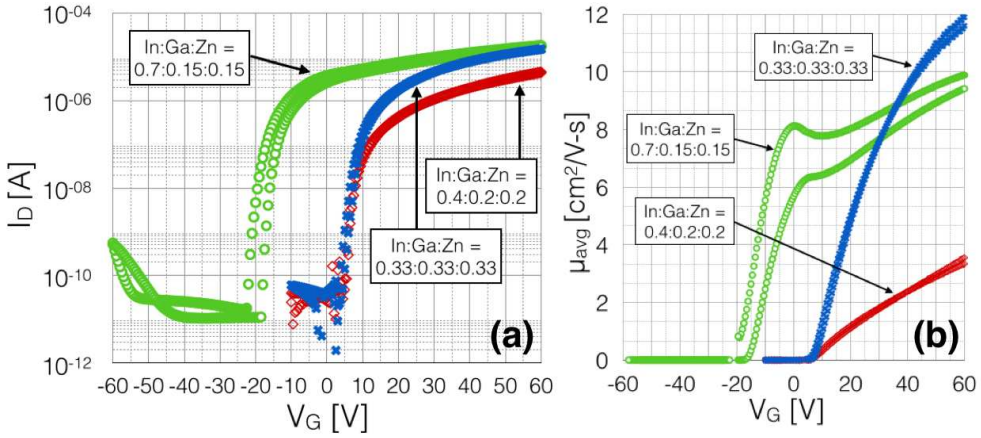

Figure 5.8: Solution-processed IGZO TFT a) transfer curve characteristics and b) average channel mobility, spin-coated with electrochemically prepared solutions (electrolyzed for 1 hour) of composition 0.33:0.33:0.33 (red), 0.4:0.1:0.1 (blue), and 0.7:0.15:0.15 (green), and subsequently annealed at 550 °C in air for 2 hours. Films are fabricated on p-Si($< 1\ \Omega-$cm) with 100 nm thermally grown SiO_2 on top. The TFT channel is 15 nm thick, defined by photolithography with a W/L = 1000 μm/150 μm.

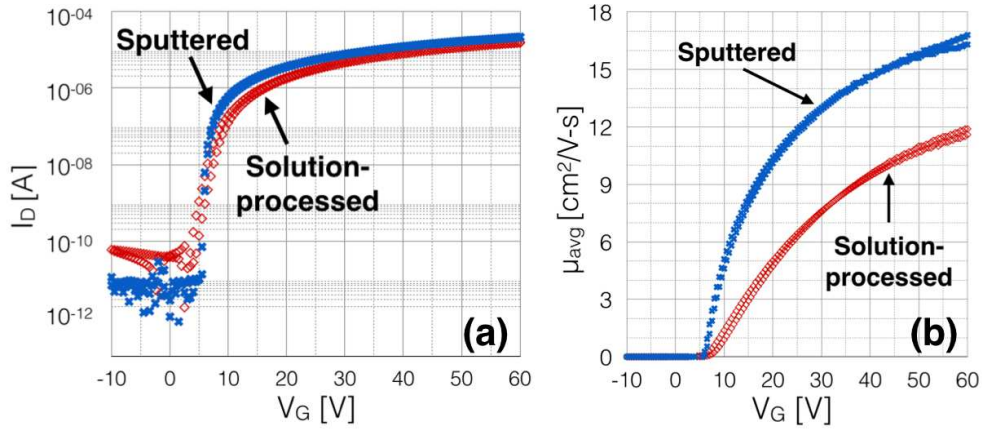

Figure 5.9: Sputtered (blue) and solution-processed (red) comparison of IGZO TFT a) transfer curve characteristics and b) average channel mobility. The sputtered IGZO process parameters are: pressure of 5 mTorr, gas flow of Ar/O_2 = 9/1, RF power of 75 W, and 400 °C anneal in air. The solution-processed IGZO TFT is spin-coated with electrochemically prepared solutions (electrolyzed for 1 hour) of In:Ga:Zn = 0.33:0.33:0.33 composition, and subsequently annealed at 550 °C in air for 2 hours. Both TFTs are fabricated on p-Si($< 1\ \Omega-$cm) with 100 nm thermally grown SiO_2 on top. The TFT channels are 15 nm thick, and a W/L = 1000 μm/150 μm.

5.2 Solution-processed dielectrics

This section describes development of spin-coated Al_2O_3 and $LaAlO_3$ gate dielectrics spin-coated using an aqueous solution precursor, employed in bottom-gate sputtered IGZO TFTs. The solution chemistry uses novel synthesis procedures emergent from the CSMC, prepared in is similar fashion as described in Section 5.1.1.1. Previous work on solution-processed dielectrics developed at Oregon State University is presented in Section 2.3.2.

Table 5.3 shows a summary of the sputtered IGZO TFT performance observed using solution-processed Al_2O_3 and $LaAlO_3$ gate dielectric, compared to a control sample employing a thermally grown SiO_2 gate dielectric.

The initial research development on solution-processed Al_2O_3 was conducted by Dr. Wei Wang as part his Ph.D dissertation, working under Prof. Douglas A. Keszler and funded by the CSMC [55]. The solution-processed Al_2O_3 samples presented in this section were prepared by Sean Smith (Prof. John Conley's Lab, Oregon State University), using solutions prepared by Matt Kast (Prof. Shannon Boettcher's Lab, University of Oregon). The research on solution-processed $LaAlO_3$ and sample preparation is led by Paul Plassmeyer, working under Prof. Cathy Page (University of Oregon) and funded by the CSMC.

5.2.1 Methods

Thin films of Al_2O_3 and $LaAlO_3$ were spin-coated on degenerately-doped p-type Si substrates (0.01-0.02 $\Omega-$cm). The Al_2O_3 thin films are annealed in air at 500 ° C. The $LaAlO_3$ thin films are sequentially annealed at 500-700 °C and 300 °C, in air and in a forming gas environment, respectively. The forming gas is composed of 95 % nitrogen and 5 % hydrogen.

The bottom-gate IGZO TFTs are fabricated by RF sputtering. The TFT structure is similar to Fig. 5.2, where the SiO_2 gate is now replaced by solution-processed Al_2O_3 or $LaAlO_3$. The 5 nm thick channel sputtering deposition conditions

Table 5.3: Summary of bottom-gate TFT performance measured for sputtered IGZO channel with solution-processed Al_2O_3 or $LaAlO_3$ gate insulator.

Insulator			Channel			μ_{AVG}[a]	V_{ON}	ΔV[b]	I_D^{ON-OFF}	S[c]
	T_A[d] [°C]	t[e] [nm]		T_A [°C]	t [nm]	[$cm^2V^{-1}s^{-1}$]	[V]	[V]		[mV/dec]
Al_2O_3	550	10	IGZO	150	5	6.7	-0.1	0	2.0×10^5	91
Al_2O_3	550	10	IGZO	400	35	2.8	0	0.2	1.5×10^3	193
$LaAlO_3$	500	100	IGZO	400	35	3.7	7.5	1.2	1.5×10^5	498
$LaAlO_3$	600	100	IGZO	400	35	4.2	3.8	0	2.4×10^5	335
$LaAlO_3$	700	100	IGZO	400	35	8.4	1.8	0.1	2.7×10^6	272
SiO_2[f]	-	100	IGZO	400	35	16.8	5	0.2	1.0×10^6	230

[a] Average channel mobility
[b] Drain current hysteresis
[c] Subthreshold swing
[d] Annealing temperature
[e] Film thickness
[f] Thermally grow

are: power = 75 W, Ar gas flow = 10 sccm, and pressure = 5 mTorr. The 35 nm thick channel sputtering deposition conditions are: power = 75 W, Ar/O_2 gas flow = 9/1 sccm, and pressure = 5 mTorr. The air post-deposition anneal for 5 nm and 35 nm channel is 150 °C and 400 °C, respectively, for 1 hr with ramp up/down rate of 2 °C/min. Thermally evaporated Al is employed for the gate, source, and drain terminals. The thermal evaporation deposition pressure is $< 3{\times}10^{-5}$ mbar ($< 2.25 \times 10^{-5}$ Torr), producing $\sim$ 500 nm thick Al thin films. The source and drain are defined by shadow mask, yielding TFT dimensions of W/L = 1000 μm/150 μm or W/L = 500μ/150 μm.

5.2.2 Results

Figure 5.10 shows the transfer curves measured for a bottom-gate solution-processed Al_2O_3 (10 nm thick) of a) 5 nm thick IGZO (annealed at 150 °C in air) and b) 35 nm thick IGZO (annealed at 400 °C in air), and c) average mobility. The maximum gate voltage applied is between -1 V to 2 V, due to catastrophic breakdown observed at around V_G = 3.5 V (not shown). The Al_2O_3 gate leakage is about 60 times lower for the 5 nm IGZO compared to the 35 nm IGZO. A 5 nm IGZO TFT annealed at a non-optimal temperature of 400 °C was fabricated showing similar Al_2O_3 gate leakage compared to an optimal 150 °C anneal. This indicates that the higher Al_2O_3 gate leakage observed in 35 nm thick IGZO channel TFTs might be related to sputter damage from a longer deposition time. The TFT performance of solution-processed Al_2O_3 gate with 5 nm (35 nm) thick IGZO channel measured a mobility of 6.7 $cm^2V^{-1}s^{-1}$ (2.8 $cm^2V^{-1}s^{-1}$), turn-on voltage of -0.1 V (0 V), drain current on-to-off ratio of 2.0×10^5 (1.5×10^5), and subthreshold swing of 91 mV/dec (193 mV/dec). The higher performance observed in a 5 nm and 35 nm thick IGZO may be due to improved gate control of channel conductance over the entire thickness of a thin channel, principally at low operating V_G required for a 10 nm solution-processed Al_2O_3 gate insulator.

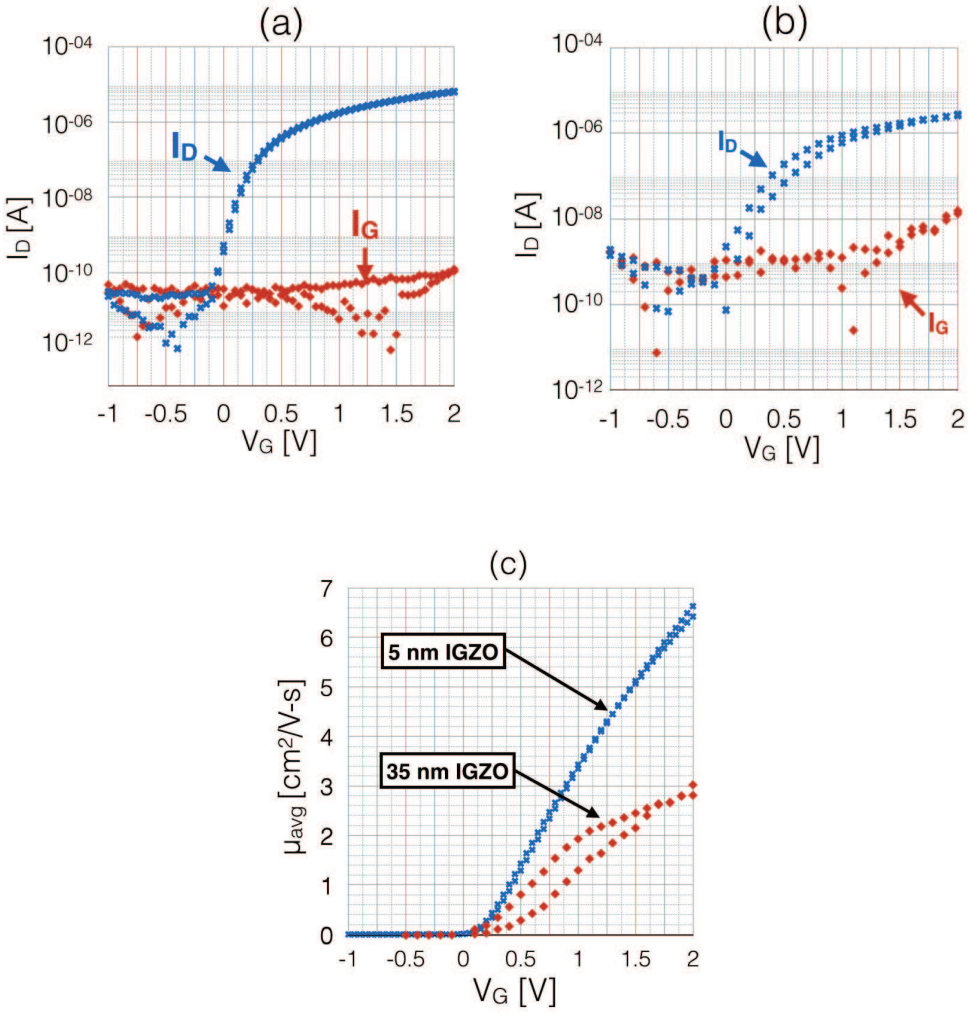

Figure 5.10: Transfer curves measured for a bottom-gate solution-processed Al_2O_3 (10 nm thick) of a) 5 nm thick IGZO annealed at 150 °C in air and b) 35 nm thick IGZO annealed at 400 °C in air, and c) average mobility. The Al_2O_3 thin films are annealed in air at 500 °C in air, and are fabricated on degenerately-doped p-type Si (0.01-0.02 Ω−cm). The RF sputtered IGZO TFTs are defined by shadow mask, and have dimension of W/L = 1000 μm/150 μm. The 5 nm (35 nm) IGZO sputtering deposition variables are: power = 75 W, gas flow Ar = 10 sccm (Ar/O_2 = 9/1 sccm), and pressure = 5 mTorr.

Figure 5.12 shows the transfer curves of sputtered IGZO annealed at 400 °C using solution-processed $LaAlO_3$ gate insulator layer annealed at a) 500 °C, b) 600 °C, and c) a) 700 °C; and d) average mobility. The $LaAlO_3$ thin films are annealed in a forming gas (95 % nitrogen, 5 % hydrogen) environment at 300 °C following the air anneal. The forming gas anneal was shown to produce better TFT performance (Fig. 5.11), presumably due to an improved insulator/channel interface. The TFT performance is observed to improve from a mobility of 3.7 $cm^2V^{-1}s^{-1}$ to 8.4 $cm^2V^{-1}s^{-1}$, turn-on voltage of 7.5 V to 1.8 V, drain current on-to-off ratio of 1.5×10^5 to 1.5×10^6, and subthreshold swing of 436 mV/dec to 238 mV/dec for samples annealed in air at 500 °C and 700 °C, respectively.

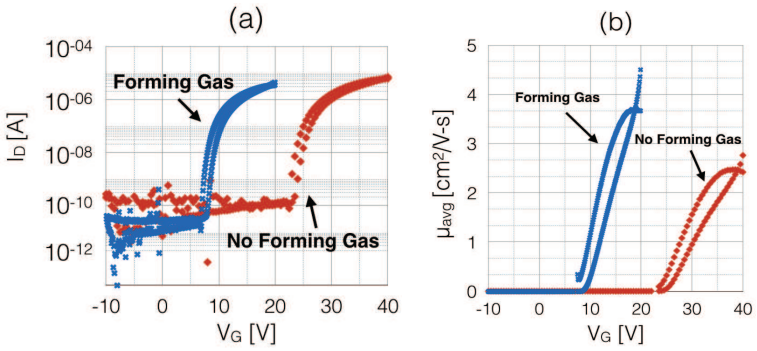

Figure 5.11: Comparison of a) transfer curves measured for sputtered IGZO annealed in air at 400 °C with solution-processed $LaAlO_3$ gate annealed in air at 600 °C with forming gas anneal at 300 °C (blue) and without forming gas anneal (red), and b) average mobility. The $LaAlO_3$ thin films are fabricated on degenerately-doped p-type Si (0.01-0.02 Ω−cm). The RF sputtered IGZO TFTs are defined by shadow mask, and have dimension of W/L = 1000 μm/150 μm. The IGZO fabrication sputtering deposition variables are: power = 75 W, gas flow Ar/O_2 = 9/1 sccm, and pressure = 5 mTorr.

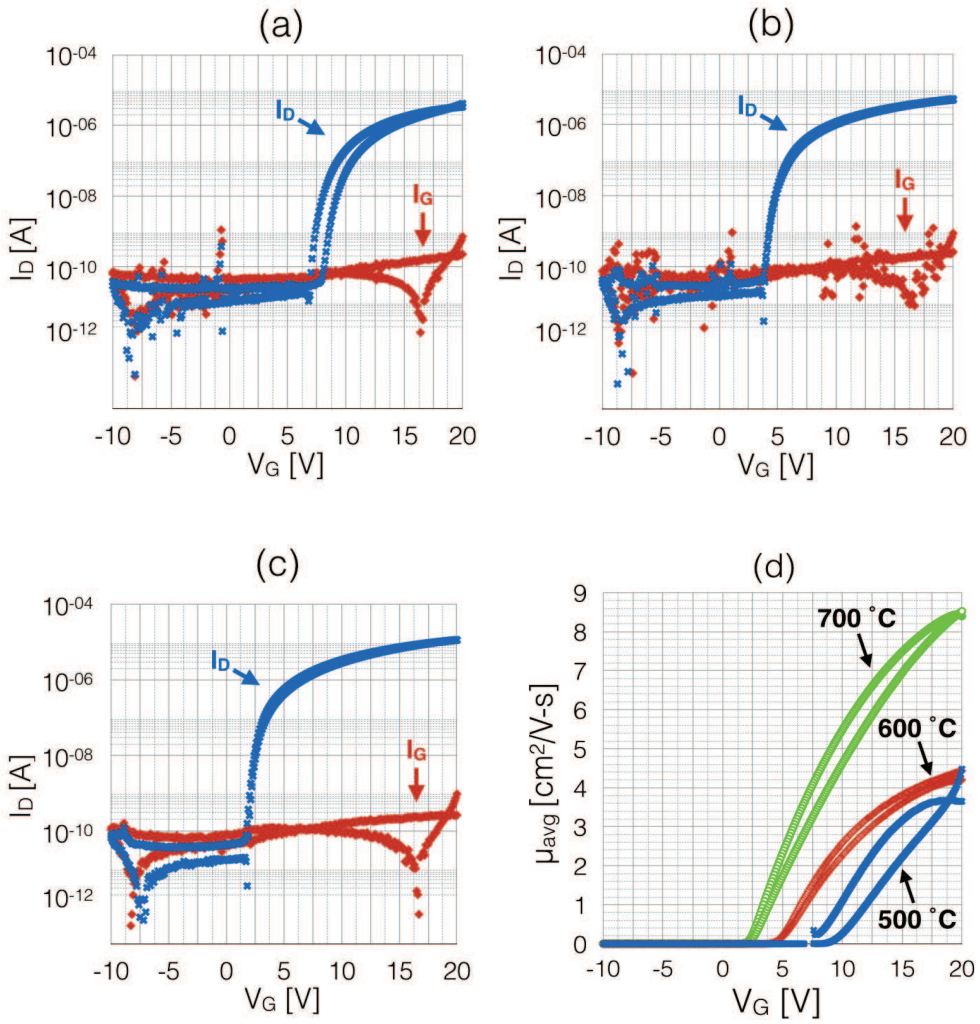

Figure 5.12: Transfer curves measured for sputtered IGZO annealed in air at 400 °C with solution-processed $LaAlO_3$ gate annealed in air at a) 500 °C, b) 600 °C, and c) 700 °C; and d) average mobility. All samples are annealed in forming gas (95 % nitrogen, 5 % hydrogen) following the air anneals. The $LaAlO_3$ thin films are fabricated on degenerately-doped p-type Si (0.01-0.02 $\Omega-$cm). The RF sputtered IGZO TFTs are defined by shadow mask, and have dimension of W/L = 500 μm/150 μm. The IGZO fabrication sputtering deposition variables are: power = 75 W, gas flow Ar/O_2 = 9/1 sccm, and pressure = 5 mTorr.

5.3 Dual active-layer solution-processed TFTs

This section presents results of solution-processed dual active-layer (DAL) TFT performance, spin-coated using electrochemically synthesized precursors. Recently, work by Jeong et al. and Rim et al. suggests that the DAL TFT structure improves mobility [95, 96]. DAT TFTs are fabricated with the objective to further improve performance of dense, solution-processed thin films spin-coated with electrochemically prepared solutions. Figure 5.13(a) shows an schematic of the cross-sectional view of the DAL TFT structure used in this study, and Fig. 5.13(b) shows a top view the fabricated DAL TFT.

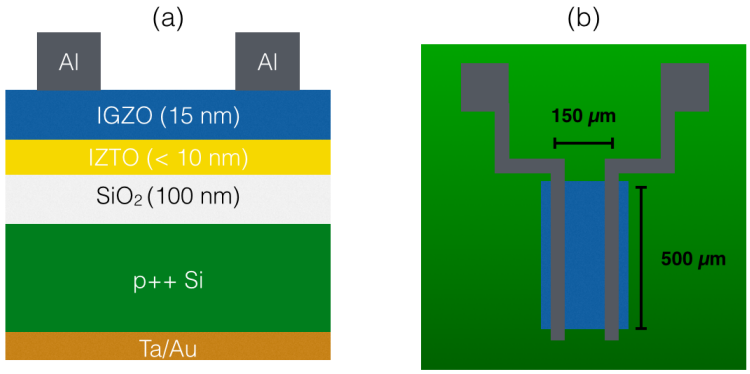

Figure 5.13: Schematic of a) cross-sectional and b) top view of a dual active-layer TFT structure used in this study.

5.3.1 Methods

Solutions prepared by electrochemistry using the procedure described in Section 5.1.1.1 are spin-coated on degenerately-doped p-type Si ($\rho < 1\ \Omega{-}$cm) with 100 nm thick thermally grown SiO_2 on top. Two thin film layers < 5 nm thick of In-Zn-Sn-O (IZTO) are spin-coated on the surface of the SiO_2 gate insulator, employing an electrochemically synthesized solution of 0.03 molar (electrolyzed for 1 hour) with a

composition of In:Zn:Sn = 9:1:1. Each layer is individually soft-baked on a hot plate at 300 °C for 30 minutes. Additionally, a 15 nm thick IGZO thin film is spin-coated above the IZTO layers, using an electrochemically prepared solution of 0.5 molar (electrolyzed for 1 hour) with a composition of In:Ga:Zn = 0.33:0.33:0.33, followed by a soft-baked on a hot plate at 300 °C for 30 minutes. The spin-coated thin films are then annealed in air at 550 ∘C for further dehydration and denitration, and to improve film density. The TFT channels are pattered by photolithography using the procedure described in Section 5.1.1.2. The source and drain electrodes are defined by shadow mask, using thermally evaporated Al. The final TFT dimension is W/L = 500 μm /150 μm.

5.3.2 Results

Figure 5.14 shows the measured DAL TFT a) transfer curve characteristics, and b) incremental and average mobility. The DAL solution-processed TFT exhibits enhancement-mode behavior with an incremental and average mobility of ~ 32 $cm^2V^{-1}s^{-1}$ and ~ 44 $cm^2V^{-1}s^{-1}$, respectively. The turn-on voltage of the DAL TFT in Fig. 5.14 is -3 V, with a drain current hysteresis of 2 V, drain current on-to-off ratio of 6.6×10^5, and subthreshold swing of 1.5 V/dec.

The observed high mobility, compared to employing a single solution-processed IGZO active-layer is partly due the enhancement-mode operation of DAL TFTs [1]. However, a single-layer In-rich enhancement-mode behavior with a turn-on voltage of -20 V does not seem to demonstrate a mobility as high as DAL TFTs (shown in Table 5.2). Figure 5.15 shows an ideal energy band diagram of a DAL TFT, where the electron energy barrier of ~ 0.15 eV between the highly conductive IZTO interface layer and the IGZO layer prevents a flow of electrons between the source and drain terminals [96]. Hence, solution-processed DAL TFT shows improved average mobility, originating from the highly conductive IZTO layer. Moreover, the IZTO-

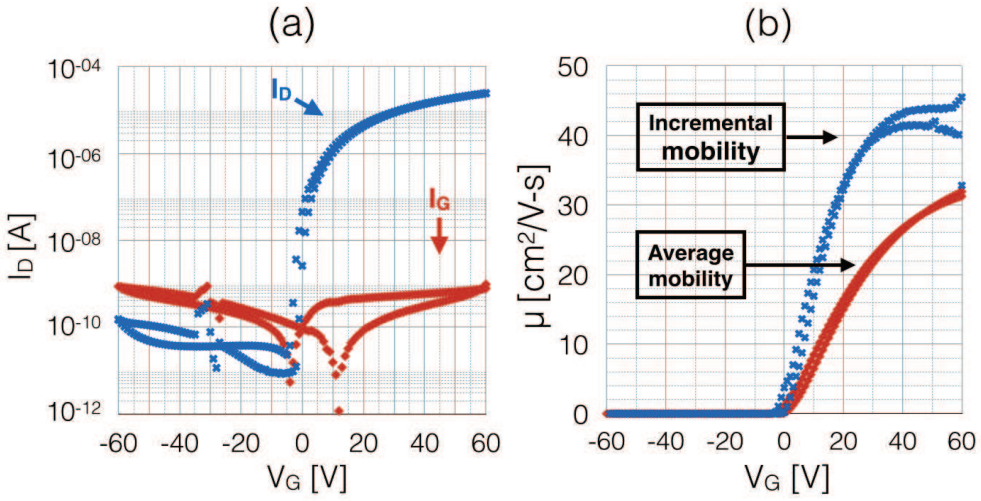

Figure 5.14: Solution-processed, dual active-layer TFT a) transfer curve characteristics, and b) incremental and average mobility assessed for thin films spin-coated with two coats of < 5 nm thick IZTO and one coat of ~ 15 nm, and subsequently anneal at 550 °C in air. The DAL TFT shows a turn-on voltage of -4 V, and substhreshold swing of 1.5 V/dec. The TFTs are fabricated on degenerately-doped p-type Si ($\rho <$ 1 $\Omega-$cm) with a dimension of W/L = 500 μm/150 μm.

IGZO energy barrier contains the drain current, generating an appropriate on-to-off drain current ratio and turn-on voltage.

5.4 Conclusions

This chapter describes the performance of TFTs employing solution-processed thin films, spin-coated with electrochemically synthesized solutions of aqueous metal-nitrate precursors. The fabricated thin films have a density > 80 % and begin to crystallized at 600 °C, as determined from X-ray reflectivity and grazing-incidence X-ray diffraction. The TFT performance of spin-coated solutions with In:Ga:Zn composition of 0.7:0.15:0.15, 0.4:0.2:0.2, and 0.33:0.33:0.33 were studied. The highest average TFT mobility of ~ 12 cm^{2}V^{-1}s^{-1} was observed with an In:Ga:Zn composition of 0.33:0.33:0.33.

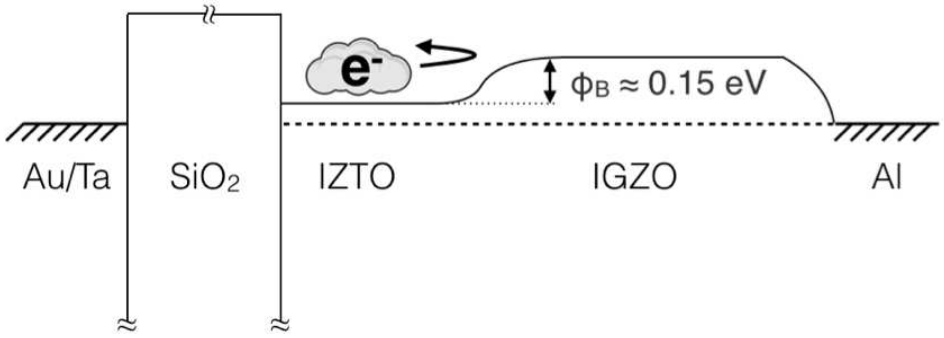

Figure 5.15: Energy band diagram of a dual active-layer TFT [96].

Sputtered IGZO TFTs are studied using solution-processed Al_2O_3 and $LaAlO_3$ as an alternative to a thermally grown SiO_2 gate insulator. The IGZO substhreshold swing employing an Al_2O_3 gate shows improvement from 230 mV/dec to 90 mV/dec compared to a SiO_2 gate insulator. The sputtered IGZO TFTs with a forming gas annealed, solution-processed $LaAlO_3$ gate insulator shows improved performance compared to annealing in air. It appears that a forming gas anneal of $LaAlO_3$ plays a key role to improve TFT performance.

Additionally, a dual active-layer (DAL) TFT structure is utilized to fabricate improve solution-processed TFTs employing electrochemically synthesized solutions. The DAL TFT with solution-processed IZTO-IGZO active layers produced enhancement-mode TFTs with an average mobility > 30 $cm^2V^{-1}s^{-1}$, exceeding that of sputtered IGZO control samples. The results indicate that a DAL structure is an effective method to improve the TFT performance of solution-processed TFTs.

6. CONCLUSIONS AND FUTURE RECOMMENDATIONS

Materials were developed for thin-film transistor (TFT) applications. The materials development presented were explored from two distinct paradigms: 1) p-channel TFTs based on Cu_3SbS_4, and 2) solution-processed TFTs.

6.1 p-Channel Cu_3SbS_4 TFTs

The Cu_3SbS_4 thin films measured Hall-effect mobility of 14-16 cm^2/V-s and hole carrier concentration of $\sim 10^{17}$ cm^{-3}. The Cu_3SbS_4 TFTs showed p-type, depletion-mode behavior with a small amount of gate-controlled modulation of the channel conductance. The Cu_3SbS_4 TFT assessment demonstrated an incremental mobility of ~ 0.5 $cm^2V^{-1}s^{-1}$, drain current hysteresis of > 7 V, and subthreshold swing of $\sim$ 70 V/dec.

The comprehensive depletion-mode model (CDMM) was employed to gain insight of Cu_3SbS_4 TFT carrier concentration, along with interface and bulk mobility. The bulk mobility, interface mobility, and carrier concentration extracted from transfer curve CDMM simulation fits of Cu_3SbS_4 TFTs experimental data is found to be 0.04 $cm^2V^{-1}s^{-1}$, $\mu_{bulk} = 0.45$ $cm^2V^{-1}s^{-1}$, and 4×10^{18} cm^{-3}, respectively. The CDMM extracted carrier concentration is in close agreement with Hall-effect measurements. The close match provided by fitting CDMM to experimental data of Cu_3SbS_4 TFTs indicate the potential of the CDMM to assess TFT performance and carrier concentration. However, the validity of the CDMM must be confirmed with more simulations fits of experimental data.

The key to producing functional Cu_3SbS_4 TFT is reducing carrier concentration. Further studies must be conducted to find effective methods to reduce the carrier concentration of Cu_3SbS_4 thin films.

6.2 Solution-processed TFTs

Solution-processed TFTs of indium-gallium-zinc-oxide (IGZO) were spin-coated utilizing electrochemically prepared solutions with In:Ga:Zn compositions of 0.33:0.33:0.33, 0.4:0.2:0.2, and 0.7:0.15:0.15. The GI-XRD studies indicated that the onset of crystallization temperature is 600 °C. The films were analyzed by XRR, and the density was found to be > 80 % for thin films anneal at 550 °C. The spin-coated solutions with composition of In:Ga:Zn = 0.33:0.33:0.33 demonstrated the highest TFT performance, with a measured average mobility of ~ 12 $cm^2V^{-1}s^{-1}$, drain current on-to-off ratio of 10^5, and subthreshold swing of ~ 1.7 V/dec.

Sputtered IGZO TFTs were fabricated utilizing spin-coated Al_2O_3 or $LaAlO_3$ from solutions prepared by electrochemistry, instead of a thermally grown SiO_2 gate insulator. TFTs with ~ 5 nm thick IGZO channel annealed at 150 °C, utilizing solution-processed Al_2O_3 annealed in air at 500 °C demonstrated average mobility of ~ 7 $cm^2V^{-1}s^{-1}$, drain current on-to-off current ratio of $\sim 10^5$, and outstanding subthreshold swing of ~ 90 mV/dec. Sputtered IGZO TFTs of 35 nm thick with solution-processed $LaAlO_3$ annealed in air at 700 °C, followed by an anneal in forming gas, demonstrated average mobility of ~ 8 $cm^2V^{-1}s^{-1}$, drain current on-to-off ratio $\sim 10^6$, and substhreshold swing of ~ 270 mV/dec.

Solution-processed dual active-layer (DAL) TFTs were fabricated, which showed significant improvement in average mobility compared to a single-layer solution processed TFT. The IZTO-IGZO solution-processed DAL TFT performance was shown to have enhancement-mode behavior (turn-on voltage of -4 V) with an incremental and average mobility of ~ 30 $cm^2V^{-1}s^{-1}$ and ~ 40 $cm^2V^{-1}s^{-1}$, respectively, drain current on-to-off ratio of $\sim 10^6$, and subthreshold swing of ~ 1.5 V/dec. Solution-processed DAL TFTs showed improved performance. However, it will be interesting to study DAL TFTs using vacuum thin film deposition techniques to explore the limits of this technology.

Solution-processed TFTs employing electrochemically prepared aqueous solutions have low porosity and demonstrated respectable performance. While this study demonstrates the advantages electrochemically synthesized solutions, an inherent drawback in the stability of the solution limits TFT reproducibility. Improving the stability of solution is key to increase the possibility of solution-processed TFT commercialization.

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