AN ABSTRACT OF THE THESIS OF

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Abstract approved: _____   _____

David J. Allstot

Multi-level decision feedback equalization (MDFE) is an effective sampled signal processing technique to remove inter-symbol interference (ISI) from disk read-back signals. Parallelism which doubles the symbol rate can be realized by utilizing the characteristic of channel response and decision feedback equalization algorithm.

A mixed-signal IC implementation has been chosen for the parallel MDFE. The differential current signals from the feedback equalizer are subtracted from the forward equalizer output at the summing node to cancel the non-causal ISI. A high-speed comparator with 6 bit resolution is used after the cancellation to detect the signal which contains no ISI.

In this thesis, a description of the parallel MDFE structure and decision feedback equalization algorithm are presented. The design of a high-speed summing circuitry and a high-speed comparator are discussed. The same comparator design is used for the flash analog-to-digital converter (ADC) which generates error signals for adaptation. The circuits design and layout were carried out in an HP 1.2-μm n-well CMOS process.

Design of High-Speed Summing Circuitry and Comparator for Adaptive Parallel

Multi-level Decision Feedback Equalization

by

Hairong Gao

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ACKNOWLEDGMENT

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Chapter 1.   Introduction

This thesis presents the design of a summing circuit and a comparator used in the implementation of an adaptive parallel multi-level decision feedback equalization (MDFE) hard-disk-drive (HDD) read channel. Speed requirements for the summing circuitry and the decision slicer circuitry in DFE were determined by system simulation and the interfaces with adjacent circuit blocks. Circuit design procedures and operation are discussed in detail. Designs were verified with HSPICE simulations. Layout has been completed in a CMOS 1.2-μm n-well process.

1.1 Background

The read channel in modern hard-disk-drive systems is a highly integrated mixed-signal IC which processes the analog read-back waveform from the read head and detects the original stored digital information [1]. The read operation starts when the read head passes over the disk and senses the magnetic transitions on the disk surface between the areas which have positive and negative magnetizations. Figure 1.1 shows the typical write and read waveforms in a hard-disk drive. Due to the non-ideal characteristic of the communication channel, amplitude and phase dispersion will occur in the read-back signal data pulses. Together with high bit density, this will cause inter-symbol interference (ISI). ISI is a major source of errors in data transmission which also limits recording density on the read channel. As massive magnetic data storage systems are more and more desired, bit densities on hard disks increase constantly. The sampling

bit sequence   0   0   1   1   1   0   1   1 ....

write current

magnetization

read voltage

read-back signal   0   +1   0   0   -1   +1   0   0
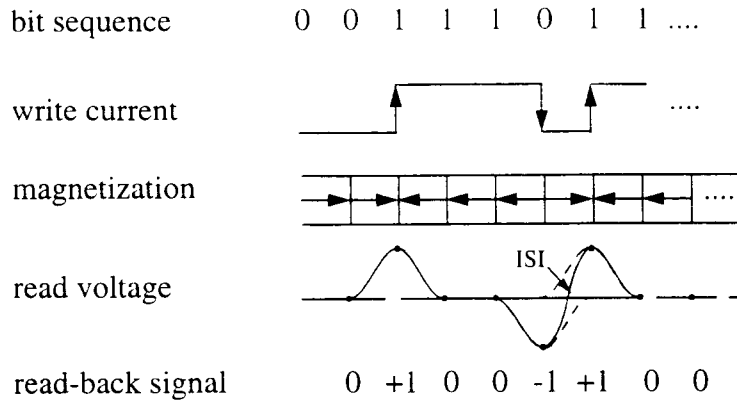
Figure 1.1 Write and read waveforms in a hard-disk-drive

detectors operating on signals which have been processed using signal processing techniques such as partial-response maximum likelihood (PRML) detectors or decision feedback equalization (DFE) have better performance than the standard peak detection scheme both in the signal-to-noise ratio (SNR) and signal density [2]. The key advantage of DFE over PRML (which uses a Viterbi detector) [3], is the simplicity of the circuit implementation.

A basic DFE detection structure with signals at the various stages is shown in Figure 1.2. In the read-back signal sequence, a +1/-1 is detected whenever the polarity of the magnetization of the recording medium changes. The ISI in the read-back signal can be visualized as the superposition of adjacent positive and negative pulses caused by consecutive 1's of alternate polarity. Probability of detection error increases as the bit density increases since more ISI is added to the read-back signal. A forward equalizer filter reduces precursor (non-causal) ISI and a DFE detector eliminates most postcursor (causal) ISI. The read-back signal after these operations is ideally free of ISI so that a simple slicer (i.e., comparator) can make a binary decision during each bit period [4].
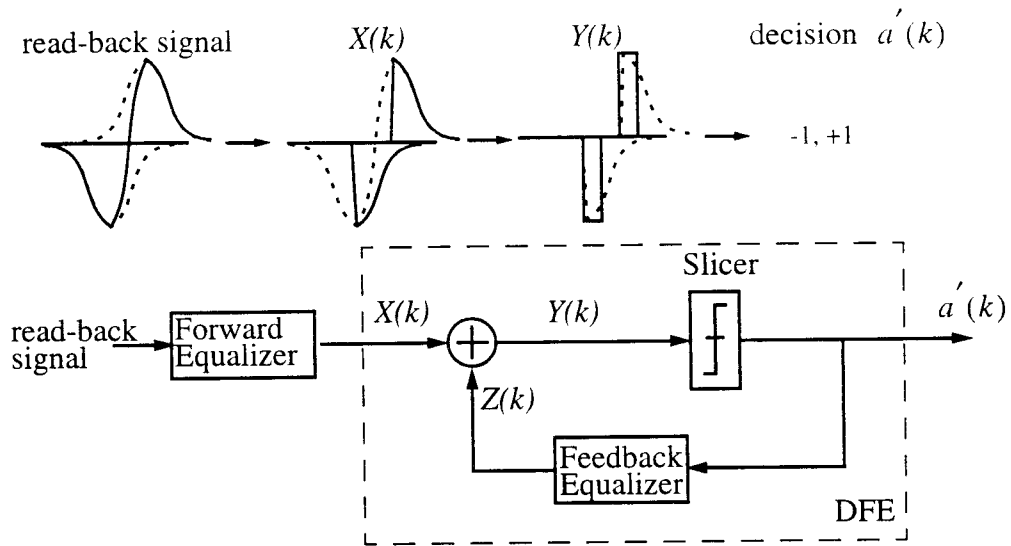
Figure 1.2 A basic structure for DFE detection

Multi-level decision feedback equalization (MDFE) [5][6] is based on fixed delay tree search with decision feedback (FDTS/DF) equalization. In the FDTS/DF algorithm, all but the first two terms of causal ISI are cancelled by decision feedback and the entire tree search rule can be implemented by a 2-tap FIR filter followed by a comparator/slicer. By substituting this filter with a replica in the forward and feedback paths, a detection structure results that is exactly the same as DFE. The major difference between MDFE and DFE is the input to the slicer of MDFE is a multi-level signal. The parallel MDFE structure doubles the operating speed of the system so that DFE detectors are working under half of the input symbol rate [7]. The algorithm and structure for parallel MDFE are discussed in detail in chapter 2.

1.2 Thesis Outline

Each detector in the parallel MDFE structure requires a summing circuit to linearly add/subtract the weighted sum of previous detector decisions from the forward equalizer filter output signal to cancel postcursor ISI. After summation/subtraction, the signal goes through a comparator (decision-slicer) and the decision is made for the feedback equalization filter to convolve with a model of the post-cursor ISI. The operating frequency of the entire read-channel is 100MHz. Taking advantage of the parallelism, each detector operates at 50MHz in the parallel MDFE. In chapter 2, the structure and signal processing on the read-back signal are described. Chapter 3 discusses the design of the high-speed summing circuitry with 6 bit linearity. Chapter 4 focuses on the design of the high-speed comparator with 6 bit resolution. Some suggestions about the direction of the future work are presented in chapter 5 and the IC layouts are included in the appendix.

Chapter 2. Parallel MDFE

This chapter describes the algorithm and structure of the parallel MDFE. By utilizing parallelism, the circuit operating speed is halved from the original symbol rate. Some specifications for different circuit blocks are also developed from the system level simulation results.

2.1 Parallel MDFE

The RLL (run length limited) code $R(d,k)$ in MDFE is 2/3(1, 7) code. 'R' is the code rate which specifies the ratio of the input word length to the output word length. 'd' and 'k' individually define the minimum and the maximum number of 0's that can occur between two consecutive 1's. Thus, the sequences such as '+1 -1 +1' and '-1 +1 -1' are not permitted in the incoming data in 2/3(1, 7) code [8]. The significant drawback of the 2/3(1,7) RLL code is the code rate of 2/3, which means that the disk drive electronics have to operate 3/2 times faster for a given output information rate. Figure 2.1 shows the block diagram of the parallel MDFE in which each decision feedback detector (DFD) is very similar to that in DFE. Two DFDs are the feedback equalization detectors which cancel the ISI due to past data symbols referred to as 'post-cursor ISI'. $G_C(s) \cdot F_C(s)$ models the forward equalizer as a continuous-time first-order all-pass filter followed by a continuous-time first-order low-pass filter. It makes the time domain impulse response causal by eliminating the ISI due to future data symbols referred to as 'precursor ISI'. The forward-equalized read-back signal has a dibit response as shown in Figure 2.2 (its
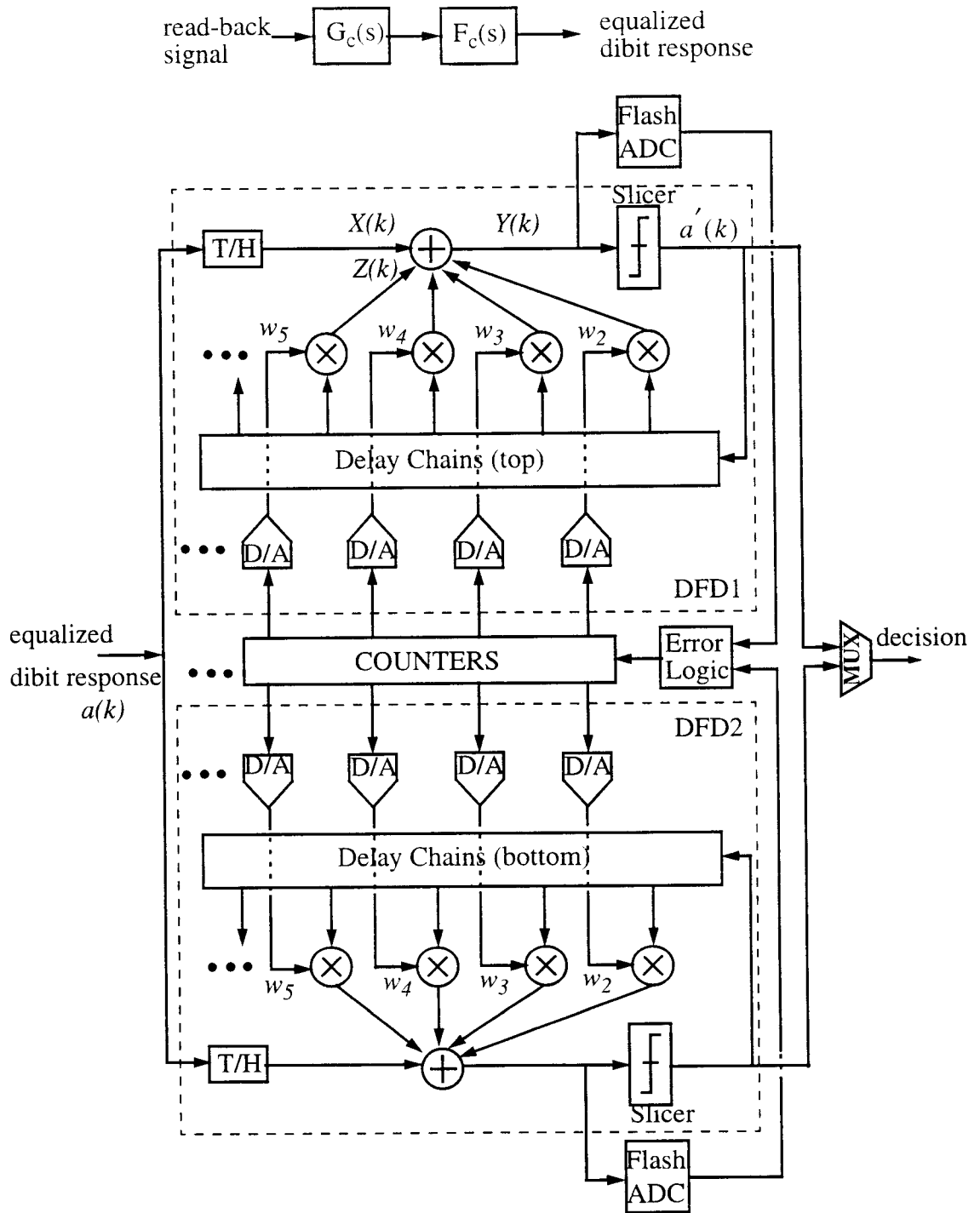
Figure 2.1 Block diagram of MDFE

sampling phase is shifted by $T/5$). The signal at the output of the forward equalizer can
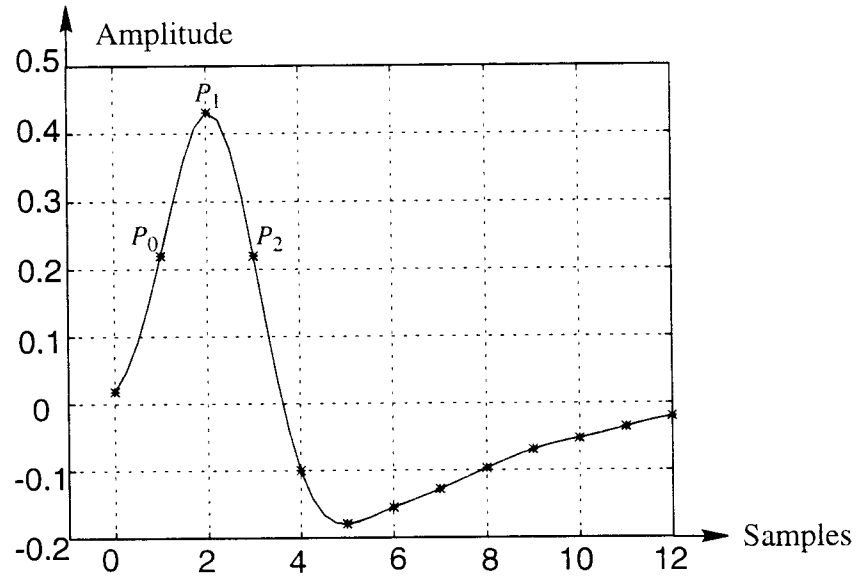
Figure 2.2 Equalized dibit response in MDFE with sampling
phase shift by $T/5$ (Symbol density = 3.75PW50)
(Courtesy of Dan Onu)

be modeled as:

$$X(k) = a(k) \cdot P_0 + a(k-1) \cdot P_1 + a(k-2) \cdot P_2 + \dots$$

The ISI term P_0 before the current decision P_1 has the same amplitude as the ISI

term P_2 after the current decision. The signal at the output of the DFD is:

$$Z(k) = a'(k-2) \cdot w_1 + a'(k-3) \cdot w_2 + a'(k-4) \cdot w_3 + a'(k-5) \cdot w_4 + \dots$$

where w's are the coefficients of the feedback equalizer. By choosing

$w_1 = P_0 - P_2 = 0$ and $w_n = -P_{n+1}$, the input and output signals of the summing node

become:

$$X(k) = a(k) \cdot P_0 + a(k-1) \cdot P_1 + a(k-2) \cdot P_2 + \dots$$

$$Z(k) = a'(k-3) \cdot w_2 + a'(k-4) \cdot w_3 + a'(k-5) \cdot w_4 + \ldots$$

$$Y(k) = (a(k) + a(k-2)) \cdot P_0 + a(k-1) \cdot P_1$$

$Y(k)$ is achieved by assuming decisions are correct so that $a'(k) = a(k)$. The possible incoming data combinations in a RLL 2/3(1,7) code and the corresponding slicer input $Y(k)$'s are listed in Table 2.1.

Table 2 .1 MDFE slicer input levels

$a(k-2)$	$a(k-1)$	$a(k)$	$Y(k)$	Decisions
+1	+1	+1	$2P_0 + P_1$	+1
+1	+1	-1	P_1	+1
-1	+1	+1	P_1	+1
+1	-1	-1	$-P_1$	-1
-1	-1	+1	$-P_1$	-1
-1	-1	-1	$-2P_0 - P_1$	-1

From Table 2.1 it is clear that only four levels are allowed for the summing node output, which means that there are only two inner levels ($P_1, -P_1$) and two outer levels ($-2P_0 - P_1, 2P_0 + P_1$) which are valid for the slicer input. More importantly, the decision has the same sign as the input to the slicer ($Y(k)$). This indicates that the threshold of the slicer can be set to '0' for the detection. The two terms of ISI (P_0 and P_2) in the outer levels are left to provide excess amplitude for the slicer to make a decision. Since the outer levels have much higher signal energy than the inner levels and are less possible to occur (only occur 1/3 of the time), they are more robust to timing, gain and

adaptation errors. Therefore, these errors are only computed by the flash ADC and timing recovery loop on two inner levels.

2.2 Decision Feedback Detector (DFD)

System level simulations show that the feedback filter can be implemented in discrete-time as a 10-tap FIR filter. The first tap of the feedback filter w_1 is zero so that an extra clock cycle is available to split the feedback section into two parallel detectors that both work at half of the original speed [8]. In Figure 2.1, the simplified structure of two detectors (DFD1 and DFD2) are also shown. These two detectors operate in a interleave fashion made possible by the parallel structure of MDFE. In both DFDs, the coefficients of the feedback equalizer are adapted to match the post-cursor ISI.

There are a total of ten counters in the MDFE system. Each detector utilizes a single counter to generate the coefficient for the DC tap. It cancels the DC offsets caused by the device mismatch in the analog circuits of the two DFDs. The other counters are divided equally between DFD1 and DFD2 to adapt the coefficients of the feedback filter. There are two delay chains in each detector. One main delay chain stores the previous decisions made by the same detector. The other delay chain is used to store the previous decisions made by the other detector [9]. In each detector, nine DACs convert the digital coefficients from counters into differential currents. These currents are multiplied by the previous decisions and then added to the equalized dibit response at the summing node. The slicer starts to make a decision after the output of the summing node settles. Concurrently, the flash ADC generates the error signal for adaptation. Inner levels are found when $a'(k-2) = a'(k)$.

2.3 Critical Timing Path in MDFE

The critical timing path in a single decision feedback detector can be analyzed using the block diagram shown in Figure 2.3. By the time the current sample $a(k)$ reaches
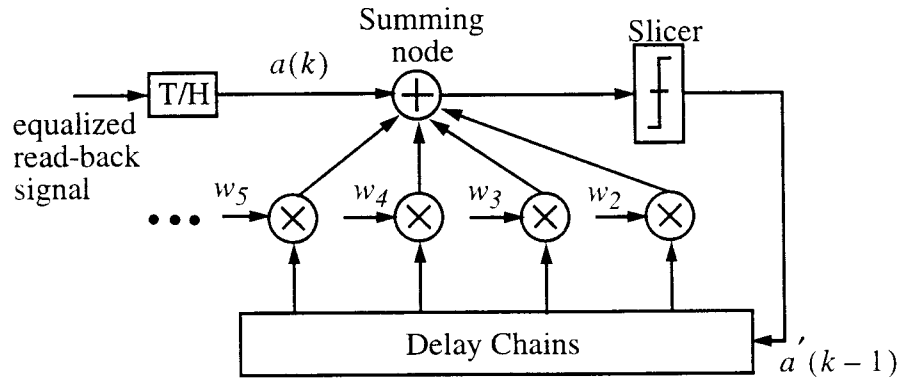
Figure 2.3 Critical timing path in a single DFD

the input of the summing node, the weighted current from previous decision $a'(k-1)$ should also be available. Therefore, the total time period for this feedback loop is 2 symbol periods, which is 20 ns. During these 20 ns, 6 ns are taken by the feedback filter [9], 14 ns are assigned to the summing node plus the comparator. It is also required that all the output signals settle to 6 bit accuracy before the next circuit starts valid operation.

Chapter 3.   High-speed Summing Circuit with 6-bit Linearity

The design of a high-speed summing circuit with 6 bit linearity is discussed in this chapter. The specifications of the summing node were determined by the system level simulations in MATLAB. Design is verified by HSPICE simulation with three different CMOS transistor models, a best-case model, a nominal-case model and a worst-case model.

3.1 Specifications from System Simulation

As discussed in Chapter 2, a summing circuitry is required in the DFE detection between the feed-forward (FF) and feedback (FB) path. The summing node output voltage must settle to 6 bit precision within 10 ns so that post-cursor ISI cancellation can be performed. The output of the forward filter is a continuous-valued differential voltage signal. This signal, which has 1.2V swing with 2.5V common-mode voltage, is sampled and held before being converted to a discrete-valued differential current signal by a voltage-to-current converter (V-to-I).

System level simulations for post-cursor ISI cancellation is done in MATLAB and the results are shown in Figure 3.1. The sampled data D_V from the forward equalizer filter has values of [-1.8, -5.3, -3.5, 1.8, 5.3, 3.5], whose amplitudes include all ISI effects from signal bits before the sampling instants [8]. The corresponding data D_I from feedback equalizer filter are [0.2, -0.9, -1.2, -0.2, 0.9, 1.2], whose amplitudes refer to the total post-cursor ISI that need cancellation. Subtraction of D_I from D_V gives the data sequence D_{SUM} as [-2.0, -4.4, -2.3, 2.0, 4.4, 2.3], which is an ISI-free signal input to the decision slicer. As can be seen from D_{SUM}, the slicer input signal has 4 levels. After
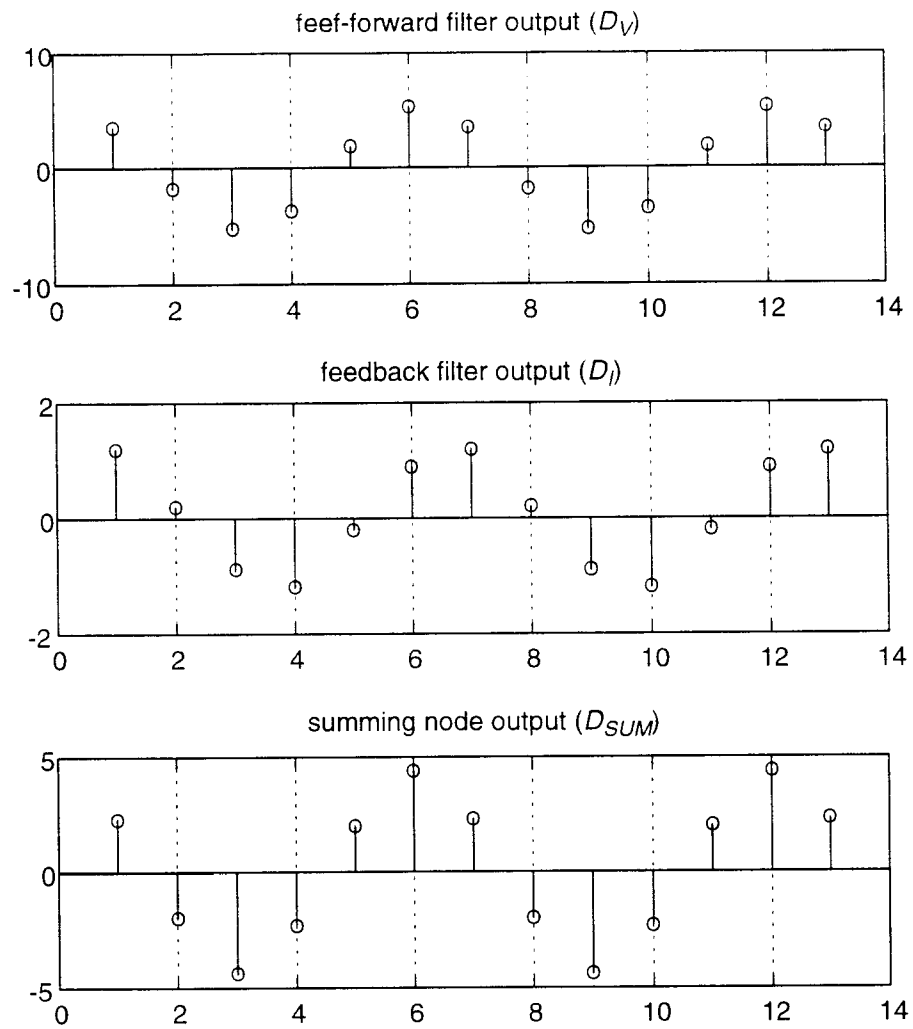
Figure 3.1 Post-cursor ISI cancellation simulated in MATLAB

scaling down D_{SUM} by 4.4 (the absolute value of the maximum digit), the inner levels approximately ± 0.5 and the outer level is ± 1. These data are mapped to the real voltage or current signals in Table 3.1 with the V-to-I to I-to-V gain set at '1'. The relations between data sequences from system level simulation and the real signal for the summing block are

Table 3 .1 Signal values in the summing block

Sample Instants (i)	Data from MATLAB for FF filter (D_V)	Voltage signals from FF filter (V_{FF})	Data from MATLAB for FB filter (D_I)	Voltage caused by FB filter (V_{FB})	Current from FB filter (I_{FB})	Data from MATLAB for summing node output (D_{SUM})	Output voltage from summing node (V_{SUM})
1	-1.8	-0.41V	0.2	45.6mV	36.5µA	-2.0	-0.453V
2	-5.3	-1.2V	-0.9	-203.8mV	-163.04µA	-4.4	-0.996V
3	-3.5	-0.79V	-1.2	-270.9mV	-216.72µA	-2.3	-0.521V
4	1.8	0.41V	-0.2	-45.6mV	-36.5µA	2.0	0.453V
5	5.3	1.2V	0.9	203.8mV	163.04µA	4.4	0.996V
6	3.5	0.79V	1.2	270.9mV	216.72µA	2.3	0.521V

$$\frac{D_V(2)}{V_{FF}(2)} = \frac{D_I(i)}{V_{FB}(i)} \quad \text{and} \quad I_{FB}(i) = \frac{V_{FB}(i)}{R} \quad ;$$

$$\frac{D_V(2)}{V_{FF}(2)} = \frac{D_{SUM}(i)}{V_{SUM}(i)} \quad ;$$

R was chosen as $1.25 K\Omega$ to convert the summed current to a voltage signal. The method

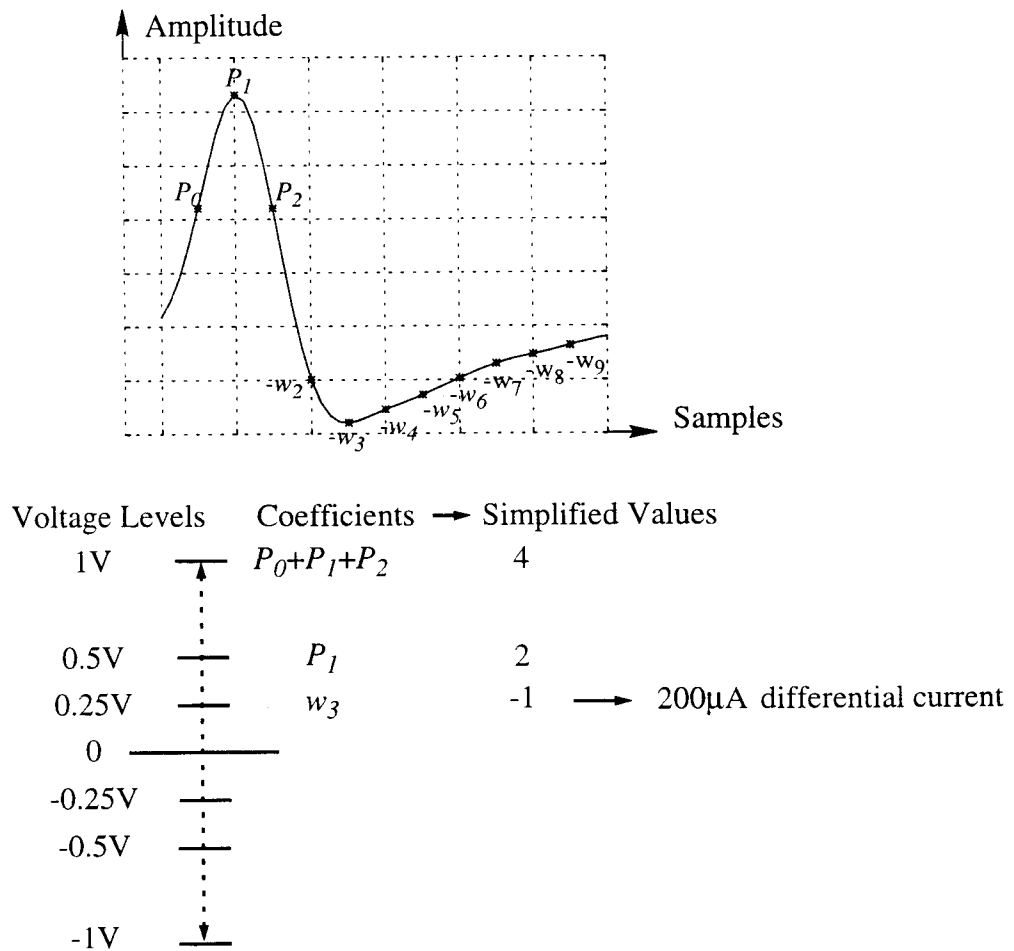used to arrive at this value is analyzed below.

Figure 3.2 Input signal levels for the decision slicer

System level simulation shows that with the main impulse (current decision) scaled to 2.0, the ideal impulse response of the read channel has sampled values of [1.0863, 2.0000, 1.1161, -0.2774, -0.8367, -0.8032, -0.6616, -0.5103, -0.3594, -0.2432, -0.1662]. The feedback equalizer filter should have 8 taps whose coefficients equal the negative values of the last eight impulses. The sum of the first 3 samples corresponds to the peak-to-peak differential input voltage to the decision slicer (after the summing node), which is 0.996V in table 3.1. If the coefficient of the third tap of the feedback equalizer filter is defined as a 6 bit full-scale current which is 200μA [9], then the maximum differential current from the filter becomes 960.66μA with all coefficients add up together. For design simplicity, the specifications are chosen according to the modified coefficients as shown in Figure 3.2. Since 200μA differential current should be converted to a 0.25V differential voltage at the output of the summing node, the resistor R used to do the converting should have a value of $1.25K\Omega$.

3.2 Circuit Design and Operation Analysis

The simplest tunable V-to-I converter is the NMOS-pair transconductor as shown in Figure 3.3.(a). M_3 works in triode region as a linear resistor whose resistance is controlled by the gate voltage V_C. By applying the source degeneration technique, the input signal range is increased while a good circuit linearity is maintained [10]. However, all the backgates of NMOS transistors are connected to the most negative voltage in our n-well CMOS technology. Since input NMOS transistors are source followers, the source to substrate voltage V_{SB} of M_1 and M_2 are about the same values as the input voltages. If channel-length modulation is neglected, the drain current and threshold
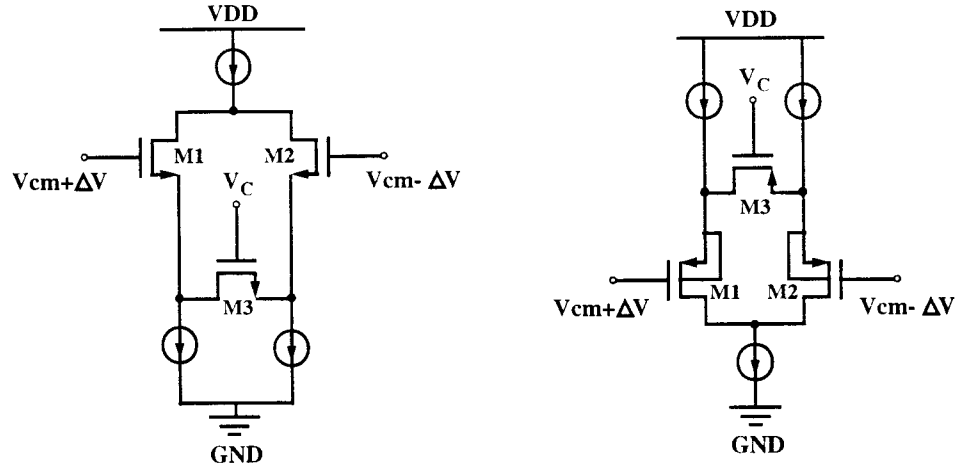
Figure 3.3 (a) NMOS transconductor   (b) PMOS transconductor

voltage characteristic of the transistors follow the equations $I_d = \frac{K}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2$

and $V_t = V_{t0} + \Upsilon(\sqrt{V_{SB} + 2 \cdot \phi_F} - \sqrt{2 \cdot \phi_F})$ (For the devices in saturation region).

Due to the nonlinear dependence that V_t has on V_{SB}, these non-zero V_{SB}'s will cause

a nonlinear relationship between the input signal voltage and the drain current of the

input pair. A PMOS-pair transconductor shown in Figure 3.3(b) is chosen in this design

(rather than an NMOS-pair) to eliminate backgate effect, thus reducing the harmonic

distortion. The gain of the V-to-I converter is $Gm = -\dfrac{g_m}{1 + \dfrac{g_m}{2g}} \approx -2g$, where g is the

effective impedance of the source degeneration part controlled by V_C.

The output of the feedback equalization (FE) filter is a differential DC current

whose value changes every clock cycle. The maximum possible amplitude for this

current is about 960μA (Section 3.1). A low-voltage high-swing cascode current mirror

(Figure 3.4) is used in the design for injecting the signal current to the summing node.

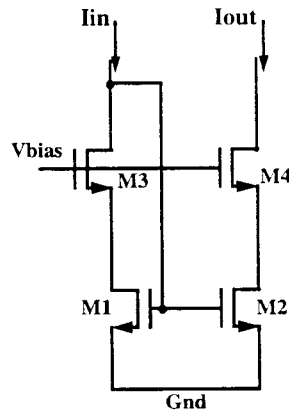Figure 3.4 A low-voltage high-swing cascode current mirror

The cascode device has a high output impedance $\left(\dfrac{g_m}{g_{ds}^2}\right)$ so that it approximates an ideal current source well. This is important because the current mirror is directly connected to the output node of the summing circuit, which has a voltage swing of 1V. V_{bias} and
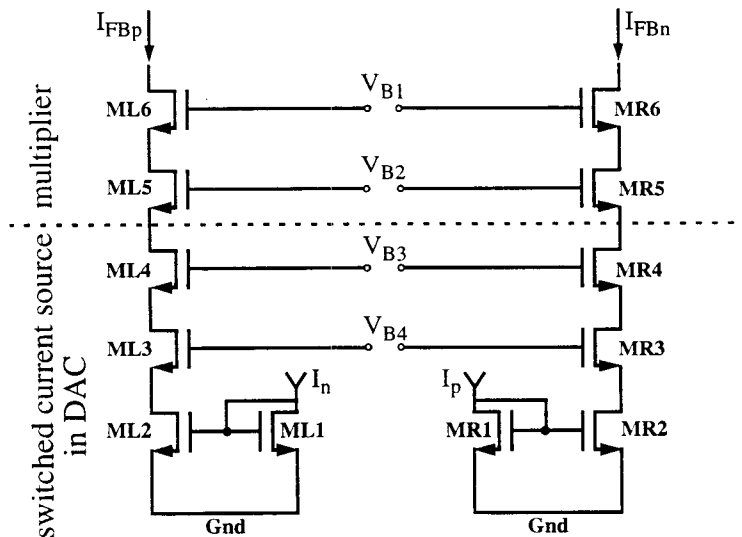
Figure 3.5 Interface in the FE filter with the summing node

devices sizes are chosen in such a way that the input node voltage does not drop below 3.6V. This constraint is set by the DACs and multipliers in the FE filter. Their interface with the summing node is shown in Figure 3.5.

The schematic for the proposed summing circuit is shown in Figure 3.6.
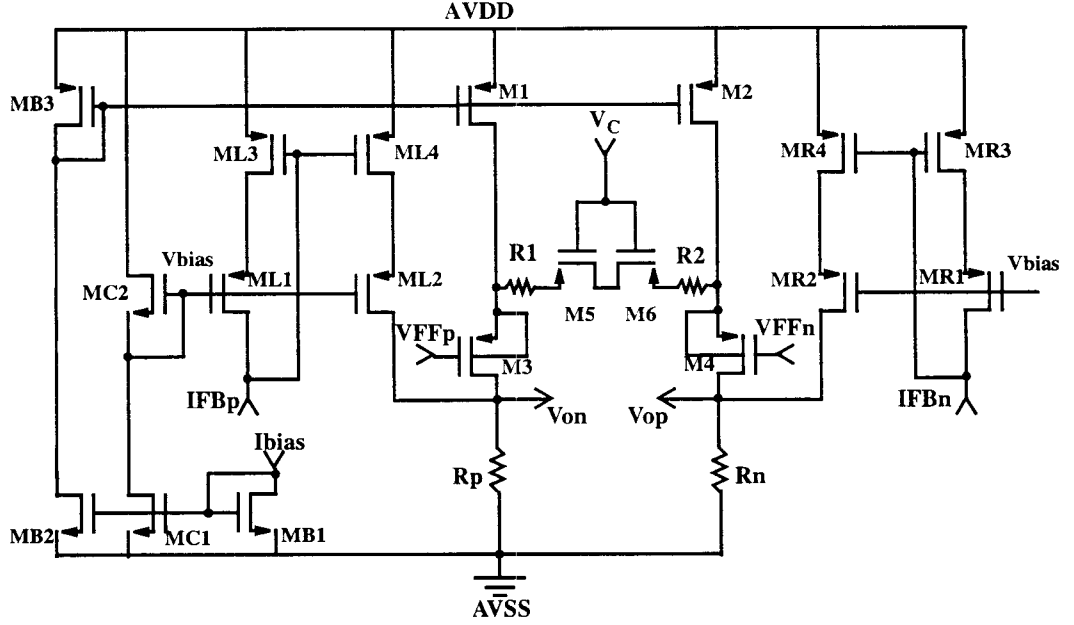
Figure 3.6 Schematic of the summing circuit

Transistors (M_5, M_6) in series with resistors (R_1, R_2) function as source degeneration of the V-to-I block. Biasing current is 100μA available on chip. V_C is the gain control voltage for the V-to-I converter and it is generated by the error detection and gain/phase recovery block in DFE detector. During gain recovery, V_C is adapted to the value that makes the V-to-I to I-to-V gain equal to '1'. Two resistors (R_p, R_n) convert the summed current into a differential voltage which in turn is sampled and compared by the comparator.

3.3 Simulation Results

The summing circuitry is simulated in HSPICE with 0.6pF load capacitance which are the parasitic gate capacitances of the flash ADC plus the decision slicer.

The V-to-I to I-to-V gain is simulated by choosing the input voltage signal from forward filter as values in Table 3.1 and zero differential current signal from FB filter. The simulation result is shown in Figure 3.7. The output voltage follows the input voltage with the V-to-I to I-to-V gain set to '1'. Simulations were done with three different transistor models as mentioned before. The main difference among these models is the threshold voltage of MOSFET devices. The best-case model has the least V_{t0} and the worst-case model has the highest V_{t0}. Since the transistor's drain current relates with threshold voltage as $I_{ds} \propto (V_{gs} - V_t)^2$ in the saturation region, the best-case model has the highest current gain. A total gain from the V-to-I to the I-to-V versus V_C for the summing circuit is shown in Figure 3.8. The solid line is the linearized relation between the total gain and the gain-control voltage V_C from the simulation results for all the three models.

The simulation results for the summing operation are shown in Figure 3.9. The output voltage signal values in the result got from the nominal-case model follows the values in the last column closely. The output voltages settle to 1% (6-bit) of the final value within 5.5 ns.

3.4 Consideration on the Accuracy of the Summing Circuit

The linearity of the summing operation is determined by the linearity of the voltage-to-current converter. In the saturation region, the transistor drain current is given
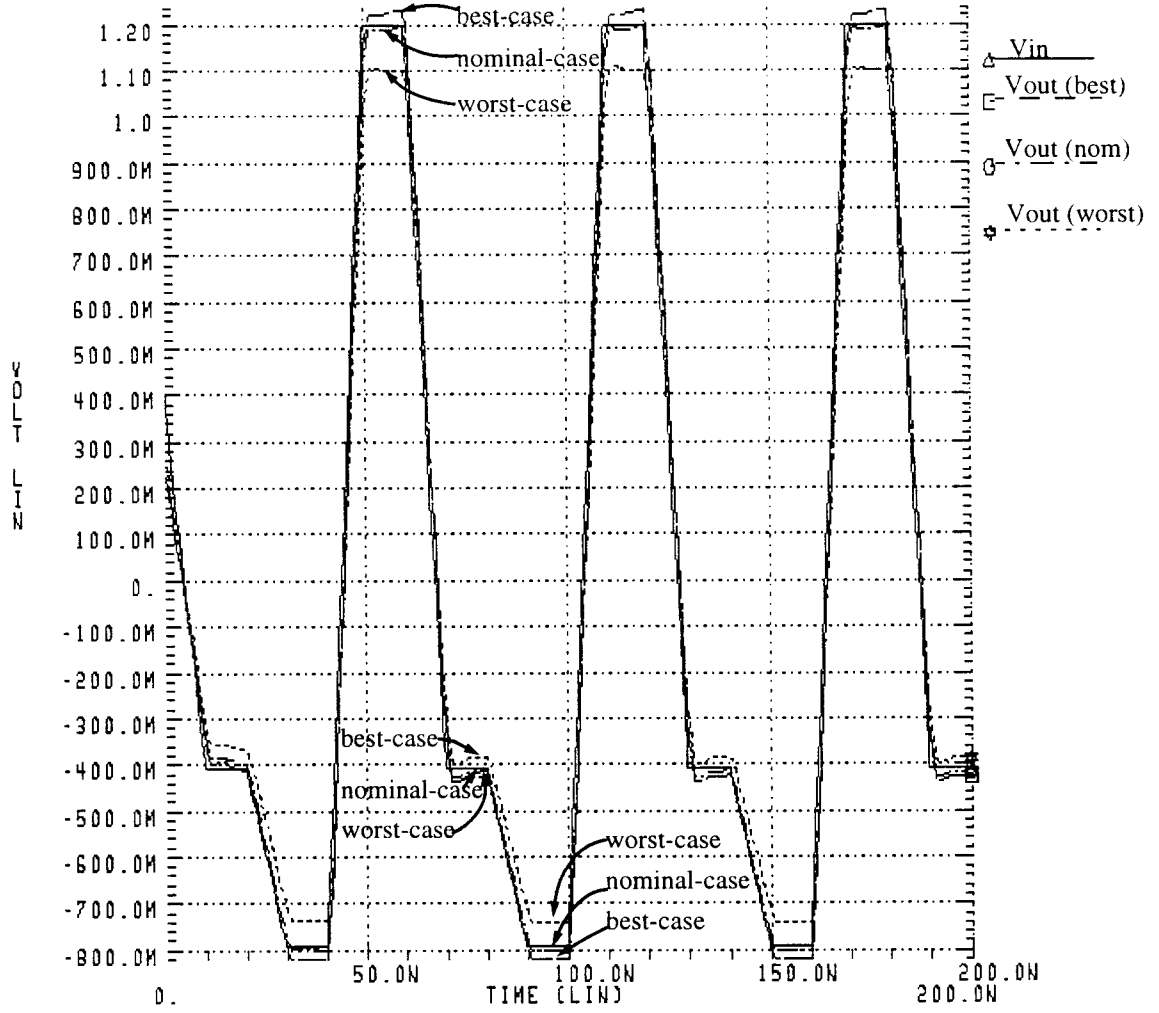
Figure 3.7 Simulation result for V-to-I to I-to-V gain=1.

by $\qquad I_{ds} = \dfrac{K'}{2} \cdot \dfrac{W}{L} \cdot (V_{gs} - V_t)^2 \qquad$ where $\qquad K' = \mu_n C_{ox} \qquad$ and

$$V_t = V_{t0} + \Upsilon(\sqrt{V_{SB} + 2 \cdot \phi_F} - \sqrt{2 \cdot \phi_F}).$$

If we assume that all the mismatch factors are independent variables [11], the

variance in the drain current can be written as $\dfrac{\sigma_I^2}{\bar{I}^2} = \dfrac{\sigma_{K'}^2}{\overline{K'}^2} + \dfrac{\sigma_W^2}{\overline{W}^2} + \dfrac{\sigma_L^2}{\overline{L}^2} + 4\dfrac{\sigma_{V_t}^2}{(V_{gs} - \overline{V_t})^2}.$
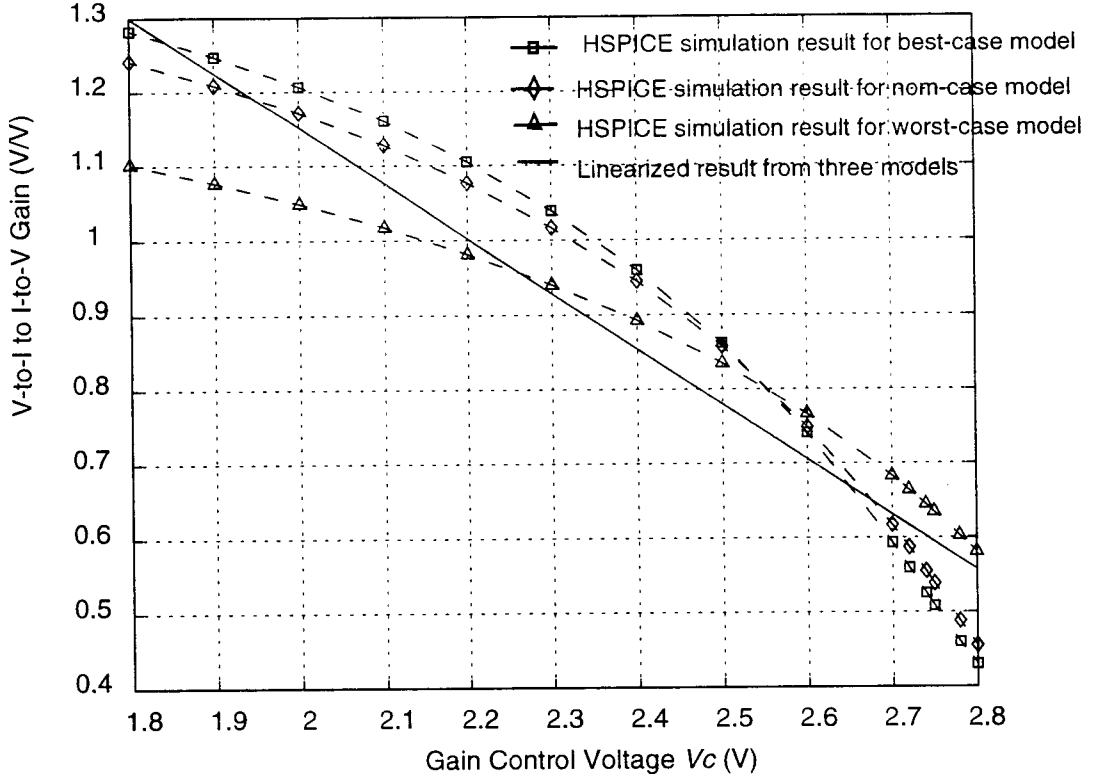
Figure 3.8 The dependence of V-to-I to I-to-V gain on V_C

The mismatch generated by the first term which consists of gate oxide and the mobility is negligible. For large dimension devices, the variations in W and L from edge roughness are also negligible. This leaves the threshold voltage mismatch as the main contribution to the mismatch in the drain current. From a statistical study of MOSFET matching by Pelgrom, et al. [11], the standard deviation in $V_{t0} = V_{FB} + 2\phi_F + \Upsilon\sqrt{2\phi_F}$ is

$\sigma^2(V_{t0}) = \dfrac{A^2_{V_{t0}}}{WL} + S^2_{V_{t0}}D^2$. The matching constants for a 50nm gate oxide, 2.5-μm process are shown in Table 3.2. The mismatch in the input PMOS pair has the most

Figure 3.9 Signals at the summing node

important effect and is estimated by using this formula. A mismatch source with

Table 3 .2 Matching constants for the threshold voltage [11]

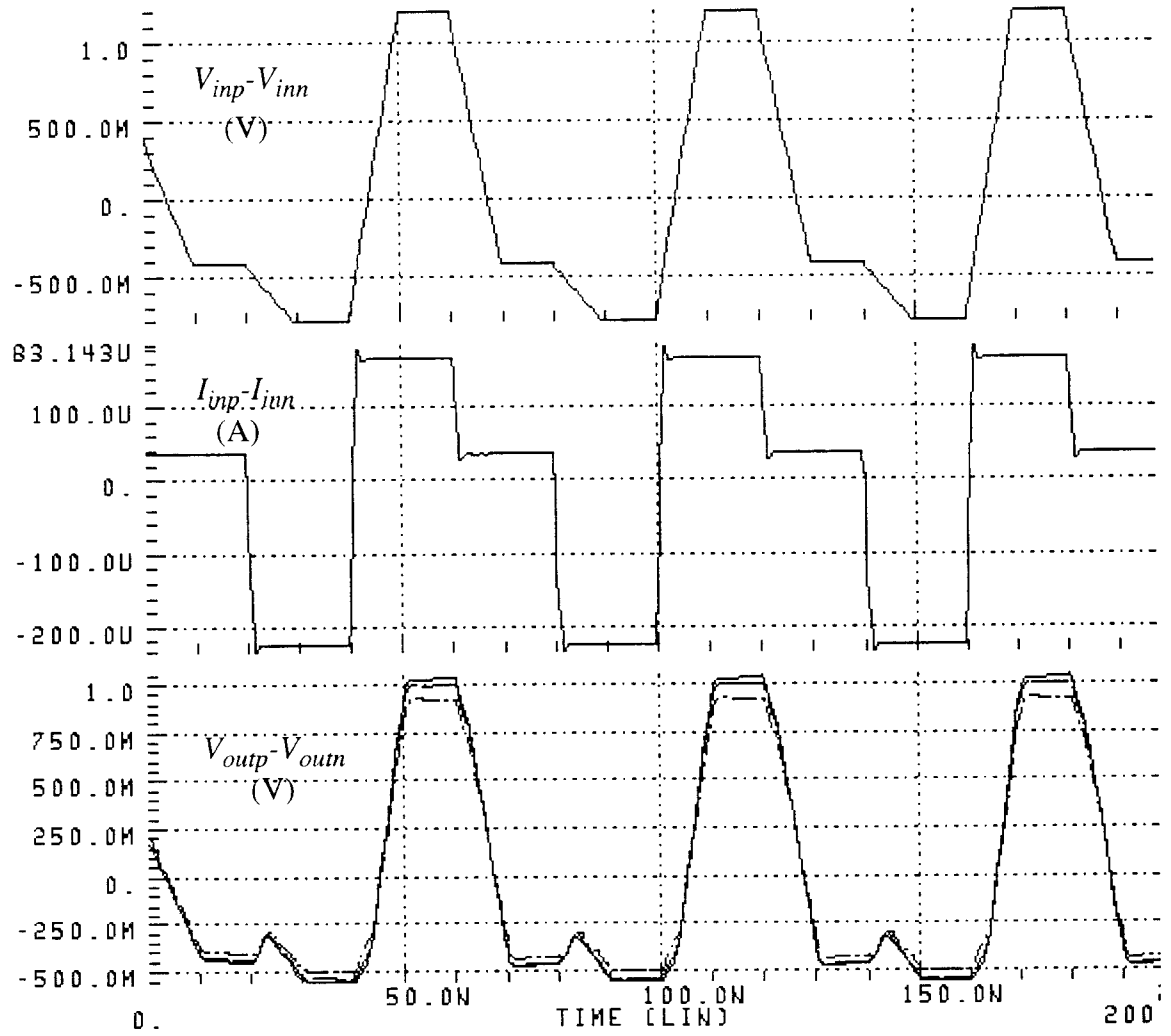| MOSFET	$A_{V_{t0}}(mV\mu m)$	$S_{V_{t0}}\left(\dfrac{\mu V}{\mu m}\right)$
NMOS	30	4
PMOS	35	4

corresponding mismatch voltage is added to the gate of one of the transistor to imitate the effect of the threshold mismatch. The HSPICE simulation results show that the even order harmonic distortion of the current gain introduced by the device mismatch is less than 0.1%.

The even-order harmonic distortion is of slight concern in this summing circuit due to the fully differential scheme. Another issue in the V-to-I converter is the gain compression/expansion caused by the odd-order harmonic distortions. If we take the input voltage signal to the V-to-I converter as $V_{inp} = V_1 \cdot \cos \omega t$

and $V_{inn} = -V_1 \cdot \cos \omega t$, then the output signal can be expressed as

$$V_{outp} = a_1 \cdot V_{inp} + a_2 \cdot V_{inp}^2 + a_3 \cdot V_{inp}^3 + \dots$$

$$V_{outn} = a_1 \cdot V_{inn} + a_2 \cdot V_{inn}^2 + a_3 \cdot V_{inn}^3 + \dots$$

Substitute the input signals into the equations and the output signal can be expressed as the difference between V_{outp} and V_{outn} :

$$V_{out} = 2a_1(V_1 \cos \omega t) + 2a_3(V_1 \cos \omega t)^3 + \dots$$

$$= \left(a_1 V_1 + \frac{3}{4}a_3 V_1^3\right)\cos \omega t + \frac{1}{4}a_3 V_1^3 \cos 3\omega t + \dots$$

The second term in the right hand of equation introduces harmonic distortion. If

$$HD_3 = \frac{1}{4} \cdot \frac{a_3}{a_1} \cdot V_1^2 \le \frac{1}{26}$$ ($a_1 = 1$ in this design), then the gain compression/expansion

will be less than 2.8% with input signal range of 1.2V. Simulation results show that the

gain compression is about 2% in the proposed V-to-I converter.

Chapter 4.   High-speed Comparator with 6-bit Resolution

This chapter presents the design of the comparator which is used as the decision element in the read channel. Its input signal is the ISI free signal and its output is either a '1' or a '0'. This bit stream is then decoded to recover the data bits. For this channel, the comparator requires 6 bit precision and should work at a 50MHz sampling rate. The comparator is part of the critical-timing path in the read-channel and therefore its settling time is critical. The input signal levels to the comparator are determined by the summing circuit. The same circuit topology was used for the flash ADC used in the error-correction circuitry. Design is verified with HSPICE simulations.

4.1 Operation Analysis of the Comparator

From the discussion in Section 3.1, it can be seen that in order to recover the data in a multi-level DFE channel, the threshold of the comparator can be set to zero. Thus, a single comparator can be used as the slicer. The decisions should have at least 6 bit accuracy which is required by the DFE detector. The proposed comparator circuit is depicted in Fig 4.1, [12] which is composed of three separate stages: a differential voltage signal input pair, a CMOS regenerative latch and a R-S latch. The advantage of this design is low input-referred offset with symmetrical layout needs no offset cancellation.

Two non-overlapping clocks are required by the comparator labelled as *phi1* and *phi2* in Figure 4.1. The dynamic operation includes reset and regeneration time periods. The voltages of nodes *a* and *b* are very important for both the reset and regeneration mode of operation since comparison starts with a voltage imbalance at these two nodes. The simplified small signal model for the circuit between these two nodes is shown in
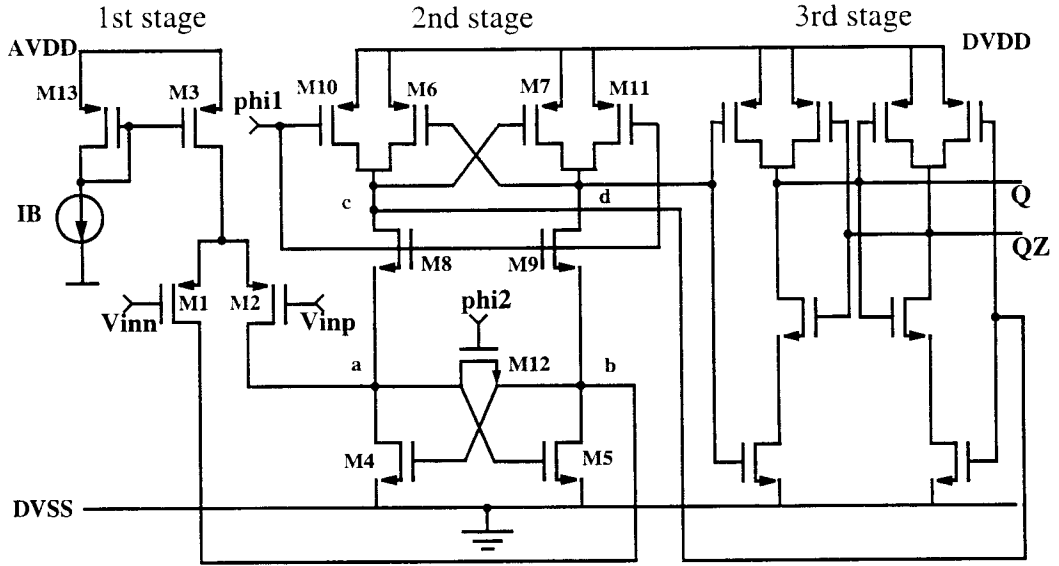
Figure 4.1 Schematic of the comparator

Figure 4.2. This model is valid for the second reset step and the first regeneration step
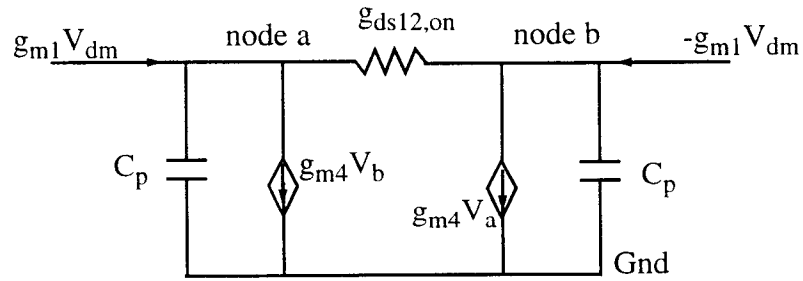

Figure 4.2 Small signal model in the comparator, $V_{dm} = \frac{1}{2}(V_{inp} - V_{inn})$.

when both M_4 and M_5 are turned on. C_p is the total parasitic capacitance at node a or node b. Solving the small signal model above gives

$$v_a - v_b = \frac{g_{m1} \cdot V_{dm}}{2 \cdot g_{ds12} - g_{m4}} + A \cdot e^{t/\tau} \quad \text{where} \quad \tau = \frac{C_P}{g_{m4} - 2g_{ds12}}$$

The reset operation starts when *phi2* goes high and M_{12} turns on. Also $g_{m4} < 2g_{ds12}$ is required according to the equation above. As a result, the voltages at node a and node b are forced to be equal after a very short time interval. However, the differential currents generated by the input PMOS pair ($g_{m1}V_{dm}$ and $-g_{m1}V_{dm}$) are fed into these two nodes, resulting in a differential voltage of $\dfrac{g_{m1} \cdot V_{dm}}{2 \cdot g_{ds12} - g_{m4}}$ to appear across nodes a and b after this signal settles. In the reset mode, nodes c and d associated with the second-stage p-channel flip-flops are charged to the positive power supply voltage, which is 5V in this design. Regeneration starts once *phi2* goes low and M_{12} turns off. Due to the clock feedthrough at nodes a and b, the voltages at these two nodes will tend to drop. However, the current from the input differential pair will charge nodes a and b and try to maintain the voltage at these nodes. Since two non-overlapping clocks are used here, there is a short time period during which both *phi1* and *phi2* are low. During this time, both the strobing devices (M_8, M_9) and the switching device (M_{12}) are off. Therefore there is no conducting paths between either nodes a and c, or nodes b and d. As g_{ds12} drops to less than half of g_{m4}, the positive feedback loop in the n-channel flip-flop rapidly amplifies the initial imbalance at nodes a and b to a voltage difference close to the power supply voltage. The time constant for the regeneration becomes $\tau = \dfrac{C_P}{g_{m4}}$ after M_{12} is fully off (g_{ds12}=0). When *phi1* starts to rise and the n-channel strobing devices turn on, the positive feedback loop in the top p-channel flip-flop is connected to the bottom n-channel flip-flop and the voltage levels at node a and b are replicated at nodes c and d. The voltage at these nodes is the input to the third stage, which is an R-S latch. During the

second regenerative phase, the outputs of the R-S latch are driven to the full complementary digital signal levels. These digital '1' and '0' outputs do not change when the second stage resets since nodes c and d are reset to a digital '1'.

4.2 Design Considerations and Simulation Results

To achieve a high comparison speed, the 100uA reference current is mirrored to a 600uA tail current for the input differential pair by a simple PMOS current mirror. Sizes of transistors in the current mirror are carefully chosen so that V_{dsat3} is less than 0.4V with the desired tail current. Therefore, this comparator has a common-mode-range of 0.2V-3.5V. In order to achieve high speed, the minimum channel length is used for all transistors except the ones in current mirror. M_{10}, M_{11} in the second stage function as pull-up transistors to precharge nodes c and d to both positive power supply voltage. The pull-up speed is not a big concern here since the change of states to both high at nodes c and d do not affect the output logic state. Thus a small sized device can be used to achieve smaller total gate area.

The reset speed is optimized when $W_{12} \geq \frac{1}{4} W_4$. This constraint can be proved from the following example referring to Figure 4.3. Before reset, V_a is high and V_b is low so that M_5 is on and M_4 is off. Reset starts as clock $phi2$ rises and M_{12} turns on. At the beginning of the reset operation, the voltage difference between nodes a and b drops rapidly. M_4 reaches the edge of conducting when V_b increases to one V_{Tn} ($V_{T0n} = 0.74V$ in our process) above V_{SS}. However, the turning on of transistor M_4 will cause less current to flow through M_{12} as well as M_5, which might cause V_b to drop to below V_{Tn4} again. This will affect the reset speed and should be avoided in the high speed
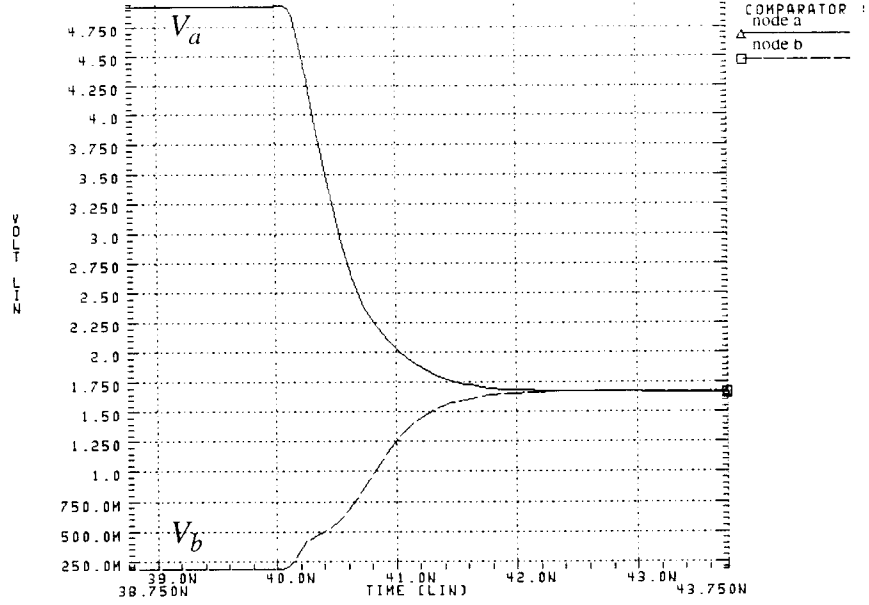
Figure 4.3 Reset operation at nodes a and b

operation. Therefore, the current through M_{12} as V_b reaches V_{Tn4} should have a value bigger than what M_5 needs for getting V_b equal to V_{Tn4}. This relationship can be expressed as

$$K_{pn}\left(\frac{W}{L}\right)_{12}\left[(V_{dd} - V_b - V_{Tn12})(V_a - V_b) - \frac{1}{2}(V_a - V_b)^2\right]$$

$$> K_{pn}\left(\frac{W}{L}\right)_5\left[(V_a - V_{ss} - V_{Tn5})(V_b - V_{ss}) - \frac{1}{2}(V_b - V_{ss})^2\right]$$

Where node voltage V_a is about 2.5V when node voltage V_b just equals to V_{Tn4}. Solving the relation above gives an approximate expression $W_{12} \geq \frac{1}{4}W_4$. With these sizes of M_4 and M_{12}, the time constant constraint $g_{m4} < 2g_{ds12}$ is also satisfied for the reset operation.

As discussed in Section 4.1, the reset and regeneration time constants are both directly proportional to the total capacitance at node a or b. Therefore, the widths of M_2 (M_1), M_4 (M_5), M_8 (M_9), and M_{12} should be chosen accordingly to achieve minimum total parasitic capacitance at these nodes. The total capacitance at node a or b is about 130fF in the proposed comparator design. The reset time is 0.5 ns and regenerate time is 1.7 ns from HSPICE simulations.

Figure 4.4(a) and (b) show the output waveforms for the input differential voltage which changes from 1V to ±4 mV ($\pm0.5 LSB$).

HSPICE simulation result shows that with a 0.15pF load capacitance which is mainly the input parasitic capacitance of the FB filter, the comparator output waveform has a rise time of 1.5 ns and the fall time of 1.1 ns with nominal V_{T0} under room temperature. In the worst case (higher V_{T0} and test temperature is $80^o C$), the rise time and fall time are respectively 2.1 ns and 1.5 ns.

The only quiescent power dissipation is from the current mirror through the input differential pair and the n-channel flip-flop. This is theoretically 3mW. HSPICE simulation result gives 3.11mW (nominal case) with 50MHz sampling frequency. The difference is due to the switching power of the regenerative latch and the R-S latch. If the sampling frequency is set to 100MHz, the switching power increases by 19%.

The devices that have the most contribution to offset are the input differential pair (M_1, M_2) and the positive feedback transistors (M_4, M_5) in the n-channel flip-flop. The input-referred offset voltage of the comparator is estimated as 22mV [13] using the same method discussed in Section 3.3. A negligible error can be realized if the comparator is laid out symmetrically.

The voltages at nodes a and b are have high swings when the clocks switch. This voltage swing will couple directly to the input through the gate-drain capacitance of the PMOS input pair. Therefore the kickback effect is a significant component for this
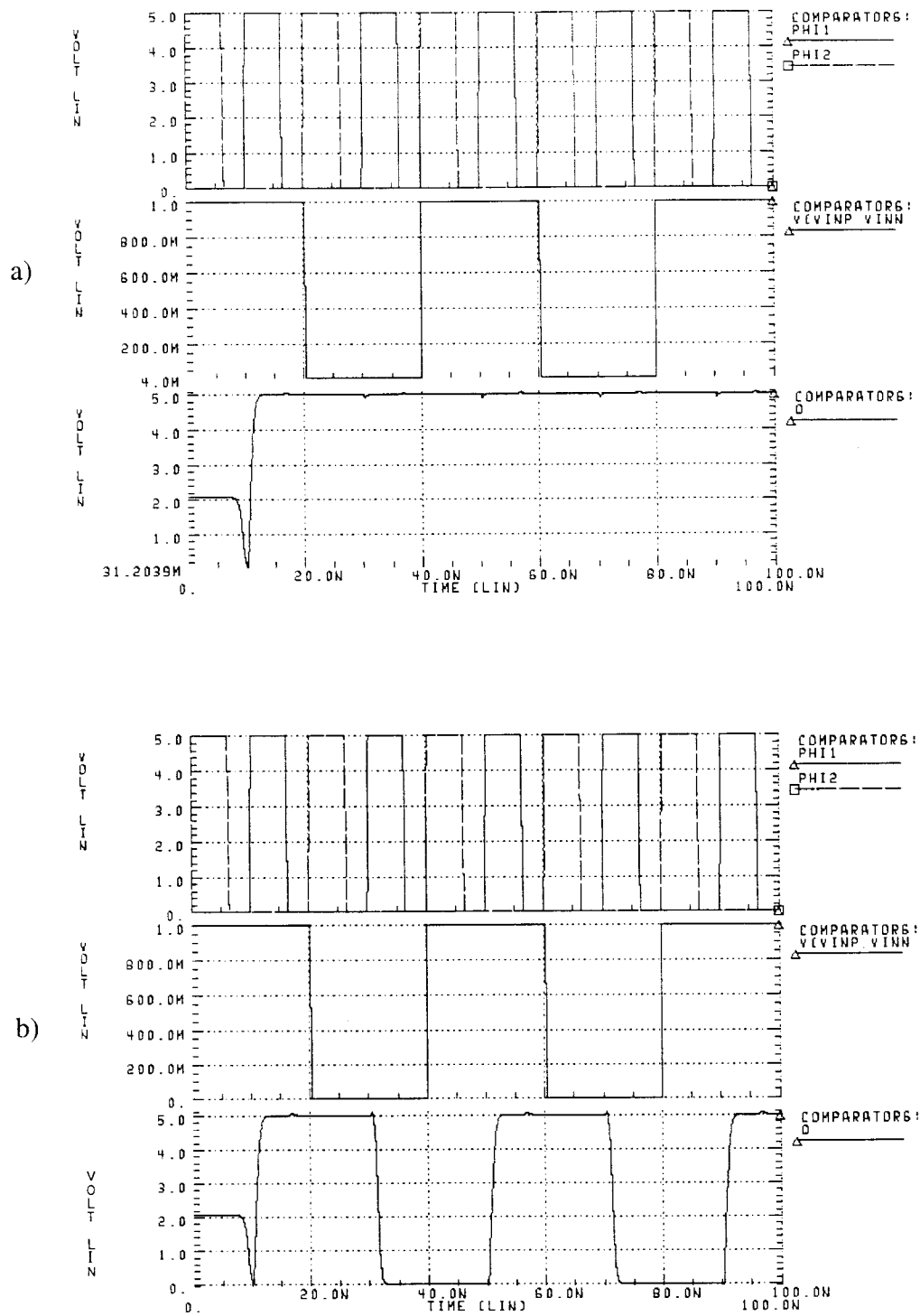
Figure 4.4 Output waveforms for different input signals: (a) the input difference changes from 1V to 4mV; (b) the input difference changes from 1V to -4mV

comparator. Kickback is a function of the output impedance of the preceding stage, which is less than 1.25KΩ from the summing node. The simulations results for kickback with different impedance values are shown in Figure 4.5. Table 4.1 shows the magnitude
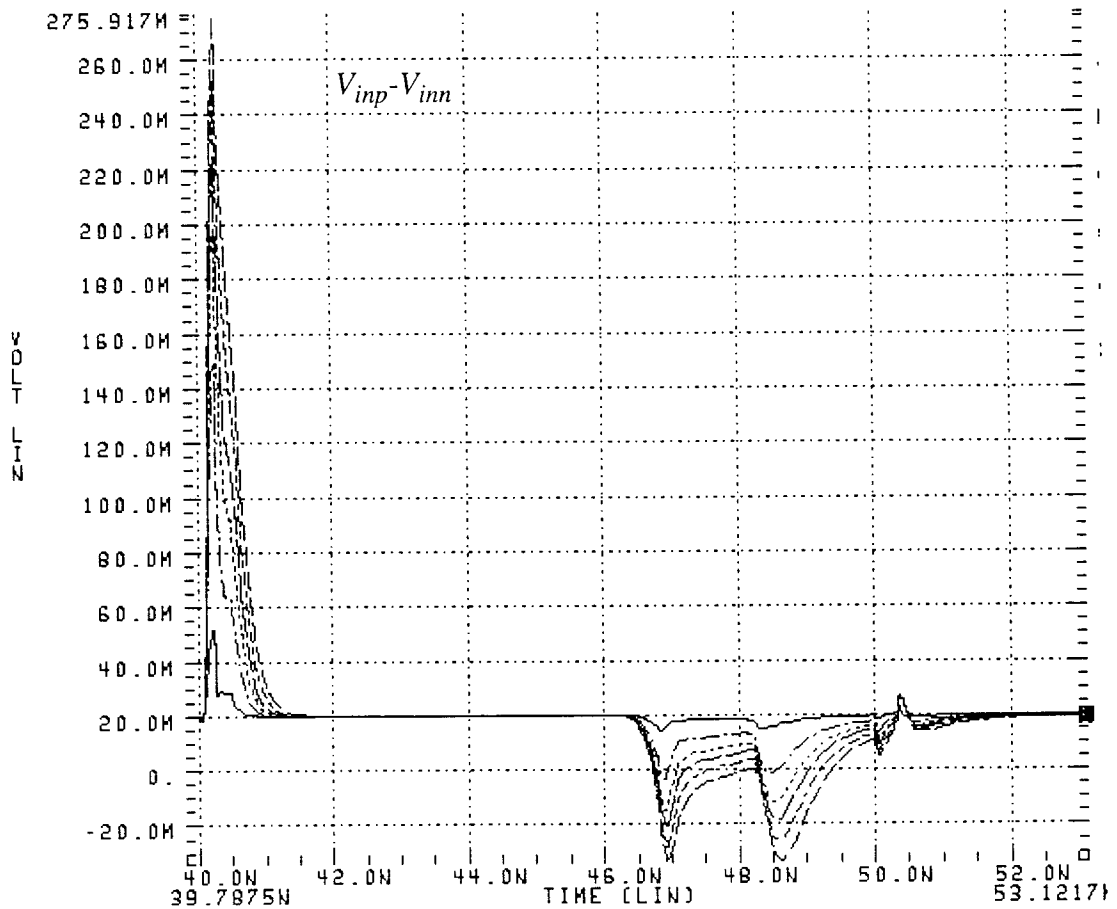

Figure 4.5 Kickback effects on the input voltage in the comparator

of the kickback spike above an input signal of 20mV, and the time for settling from the clock edge to within 4mV of the input level with corresponding output impedance of the preceding stage. Since the regenerative voltage swings more gradually than reset, the spikes appearing at the input have longer duration but smaller amplitude. This will not

Table 4 .1 Kickback spikes on the input signal

Impedance (Ω)	Reset Clock Edge		Regenerative Clock Edge	
	Mag. (mV)	Duration (ns)	Mag. (mV)	Duration (ns)
100	30	0.6	6	4.4
500	128	0.8	23	4.4
800	180	0.9	35	4.5
1000	200	1.0	40	4.6
1250	230	1.0	45	4.8
1500	256	1.2	54	4.9

cause decision errors as long as the direction of initial imbalance is not affected. The positive feedback takes over the regenerative operation afterwards and a decision is made accordingly. The kickback at the reset edge is more important because it has a dramatic change in a very short time period. While this is coupled to the input, it might cause the comparator to reset incorrectly or to have a longer reset time. Simulation result shows that with $1.25K\Omega$ preceding output impedance, the kickback spikes on the input drop to within 4mV before the voltage imbalance is start to be established as node a and b. Thus no decision error occurs to the output.

Chapter 5. Conclusions and Future Work

Simulations of the summing node connected with the comparator are done in HSPICE. IC layout of the summing circuit and comparator has been completed using the 1.2-μm n-well CMOS process. The post-layout simulation results show that the speed of the circuits with inter-connect and other parasitic capacitances still meets the design specifications.

5.1 Simulation Result

The HSPICE simulation result for the summing node when it is connected with the comparator is shown in Fig. 5.1. The clock switching in the comparator cause voltages at node a and b change instantaneously. This voltage variance is coupled back to the input of the comparator, which is the output of the summing node, and causes spikes on the summing node output. This kickback effect does not cause error decision in the operation of this comparator for the reason discussed in Section 4.2.

5.2 Layout and Post-layout Simulation

The summing circuit and the comparator have been laid out in a 1.2-μm n-well CMOS process. Fully symmetrical layout is used for both circuits to improve device matching performance and reduce offset. A n^+ guard ring around the digital block in the comparator is used to reduce noise coupling from the digital section to the analog circuits through the common substrate. The layout size is about $278\mu m \times 267\mu m$ for the summing circuit and about $116\mu m \times 229\mu m$ for the comparator. The layouts are shown
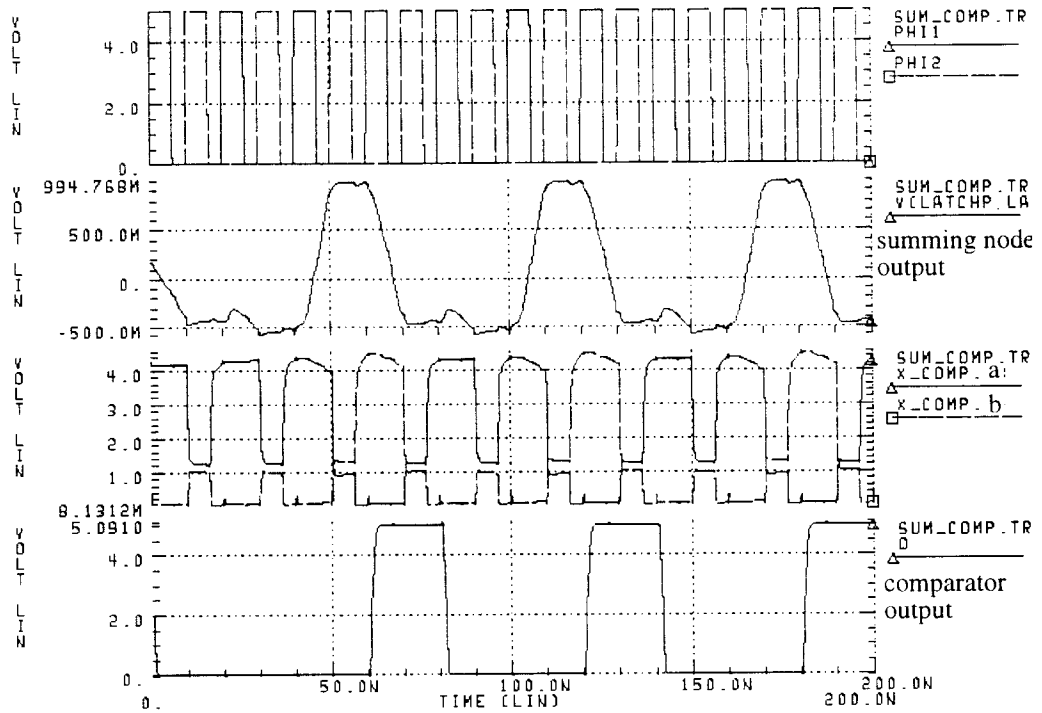
Figure 5.1 Simulation result of the summing node with the comparator

in appendix. Post-layout simulation results of the summing circuit and comparator in Figure 5.2 show that even the wiring and other parasitic capacitances cause some speed degradation, the design can still achieve the desired speed. The comparator has a rise time of 2.8 ns (3.9 ns for the worst case) and a fall time of 2.2 ns (2.8 ns for the worst case) while the summing node output settles to 6 bit accuracy within 8.4 ns (9.5 ns for the worst case).
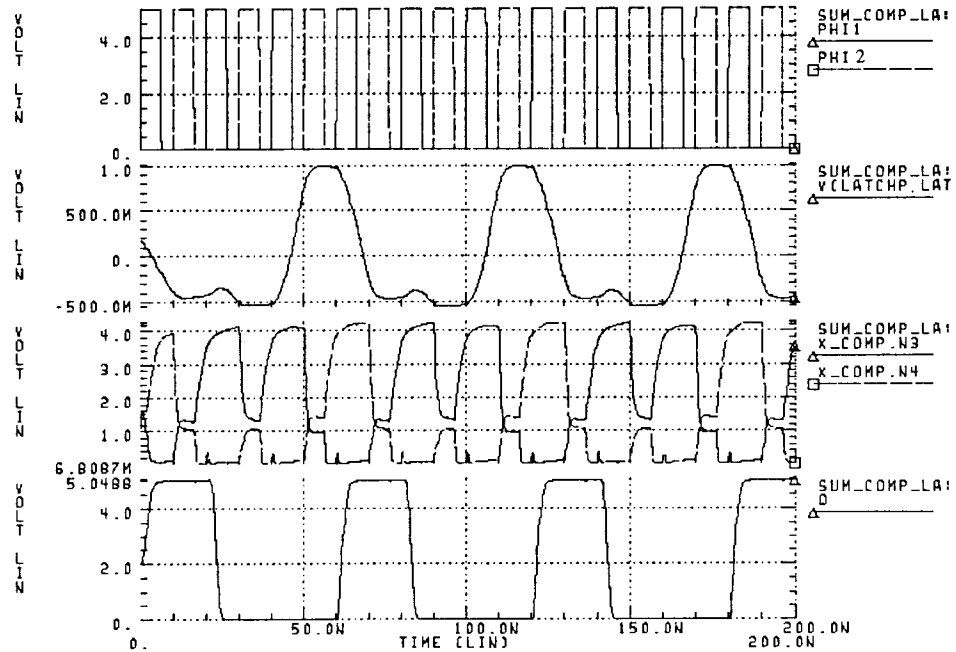
Figure 5.2 Post-layout simulation result of the summing node with the comparator.

5.3 Future Work

The comparator designed in chapter 4 can also be used in the flash analog-to-digital converter (ADC) which generates error signals for adaptation in MDFE. The input stage of the comparator is then modified as shown in Figure 5.3. The reference signals (V_{refp} and V_{refn}) are generated using resistor strings. The required comparison precision is 3 bit for the error correction.

In the proposed comparator circuit, the kickback becomes significant enough to cause errors with minimum level voltage input difference when the output impedance is bigger than 2kΩ from the previous stage. To improve this, two PMOS transistors can be added between the PMOS input pair and the n-channel flip-flop to reduce the voltage variance at the drain of the input pair. The comparator can also be designed for higher
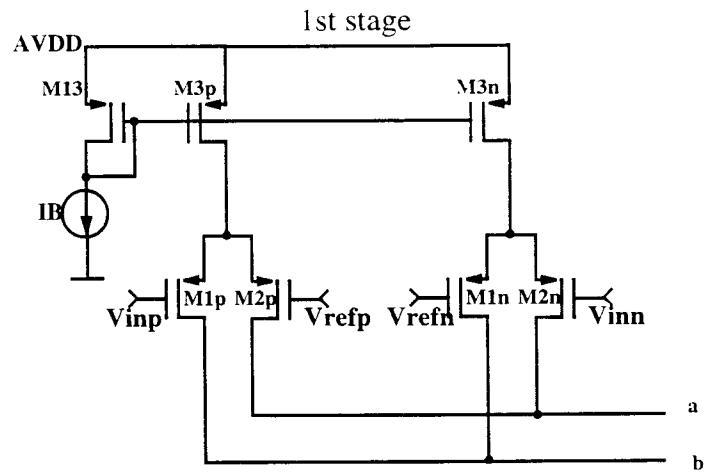
Figure 5.3 Input stage for the flash ADC in MDFE

speed by applying this cascode scheme since the duration of kickback voltage spikes appear on the input signal will also be reduced.
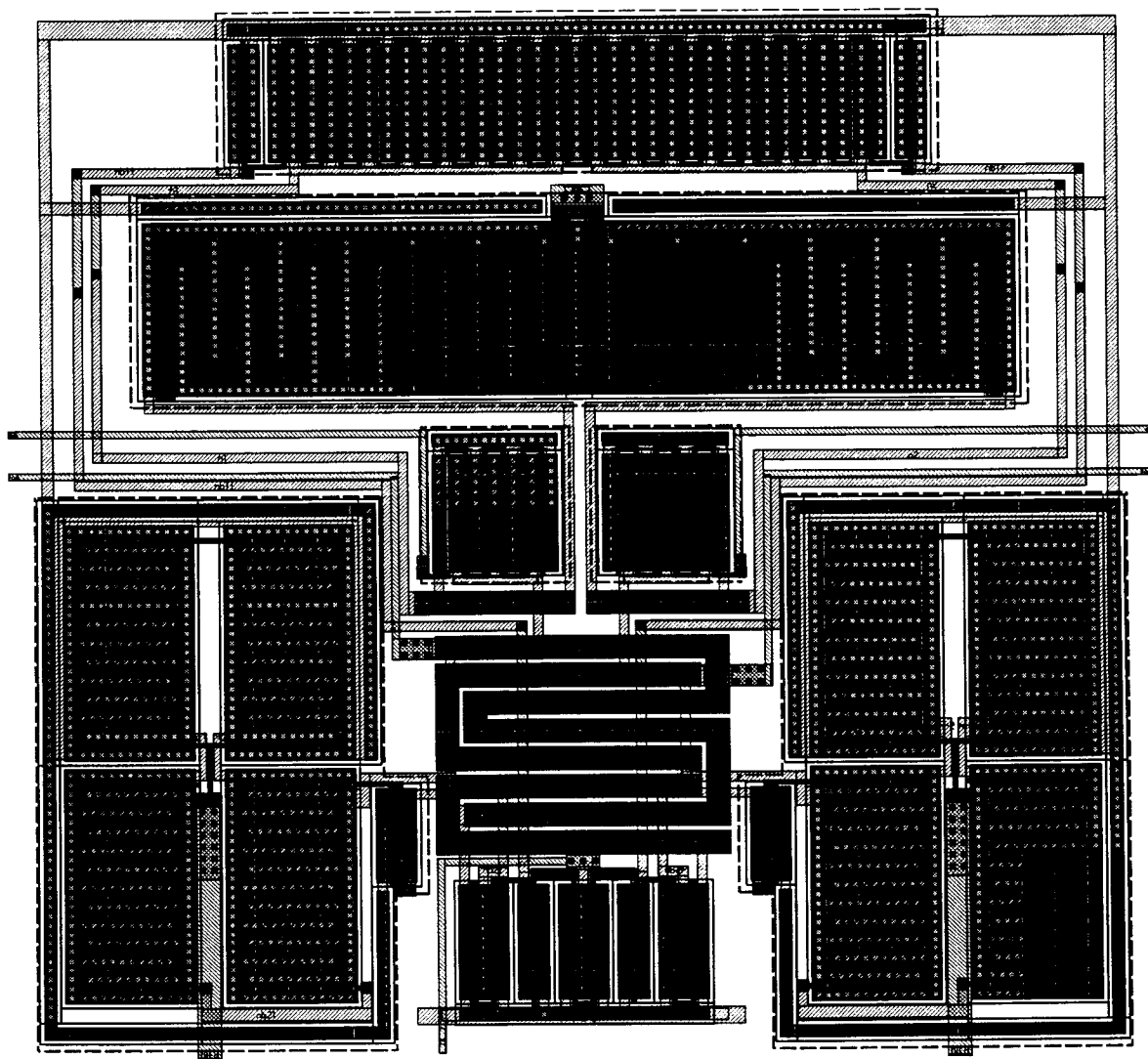
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Appendix: Layouts

Layout of the summing circuit

Layout of the comparator