Andrew Ferrara MS Project – AWG Analog/ Mixed-Signal Output Stage

Project Background:

This project is a custom output stage for a two-channel signal source design project at Oregon State. Starting in January, I began leading a team tasked with the development of an arbitrary waveform generator via the CreateIT Collaboratory at OSU. Undergraduate students interview into the CreateIT Collaboratory and are assigned industry sponsored projects to work on. The Collaboratory is intended to provide engineering work experience with faculty oversight, leading to on-site internship opportunities; giving the students the work experience of a co-op without interrupting academics. I was brought in to lead the group, freeing up some of the faculty oversight, while providing the necessary analog design experience to assure success for the project.

For this arbitrary signal source, a high-speed high-quality DAC is used for Signal Generation. An Analog Devices AD978x series is used, it is a two channel DAC with the following independent adjustments:

- Numerical up-conversion for IF options
- Phase-offset control
- DAC output level
- DC Auxiliary DACs
- Built in Digital Filters

The DAC will be driven by an FPGA, this digital "back-end" is handled by the undergraduate team, supporting data rates up through 800MSPS. I am a technical resource for the undergraduate team, as well as a delegator for tasks that lead to the integration of the digital blocks.

MS Project Details:

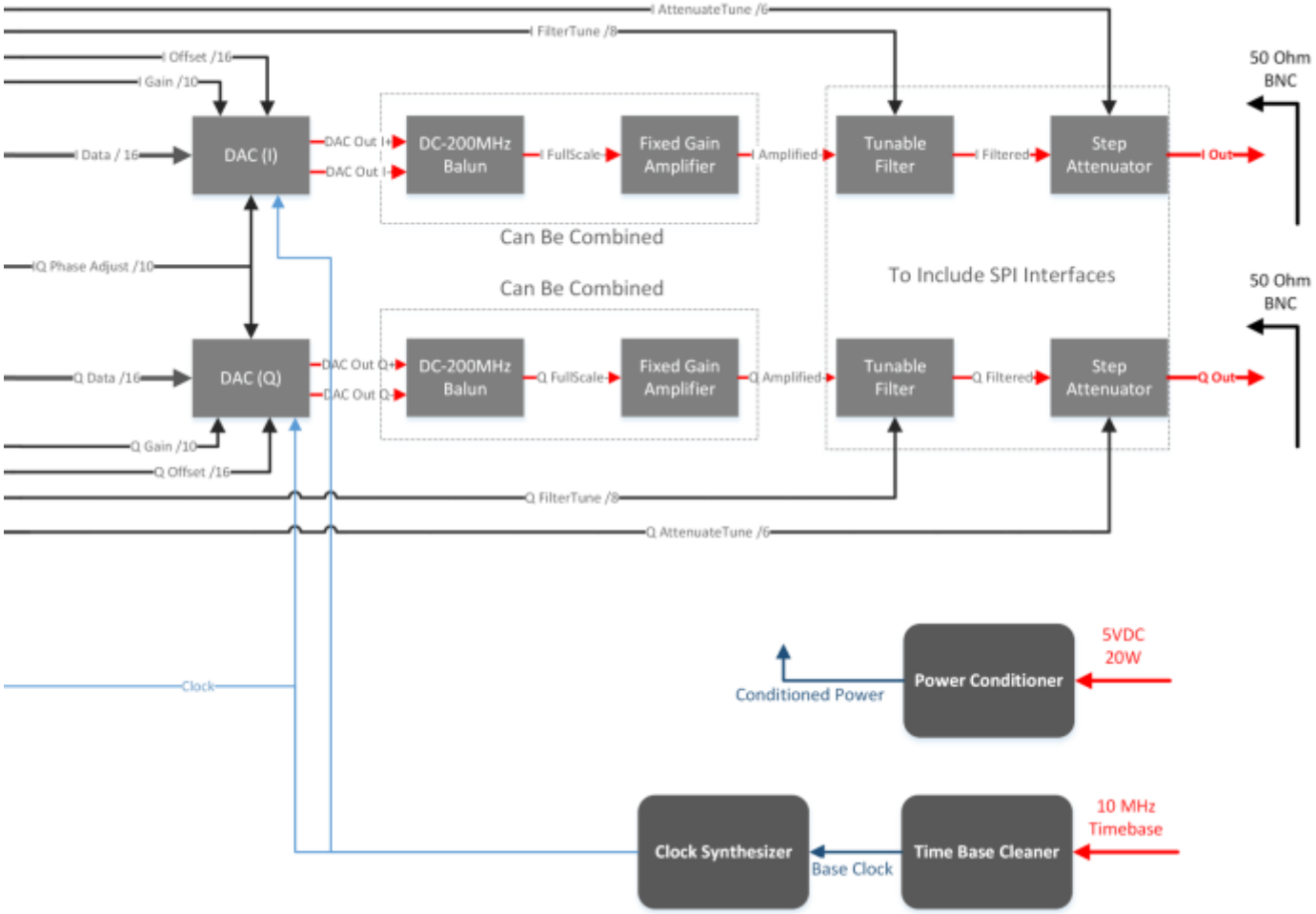
The project is primarily an Analog Output Stage for the DAC, which is a differential, current output DAC. The output of the AWG is single-ended with a 50-Ohm source impedance, supporting amplitude and DC-offset control. The addition of tunable filters to remove data clock spurs and harmonic distortion from the primary signal is also necessary. The first design was board level with each tunable parameter addressed with individual blocks built from off-the-shelf parts: high-speed op-amps, RF switches for switching in step attenuators and filter banks, etc. A custom, discrete transistor level transimpedance balun was designed to be directly driven by the DAC.

The newest version being designed implements the functions of each gain, attenuator, filter, and DC-offset blocks into the discrete transistor balun block. Complementary BJTs from NXP and GaAs FETs from Avago are being used for gain control; mirrors and the auxiliary DACs are used for DC offset control. Discrete capacitor banks limit the bandwidth of the balun, helping to remove the data clock spurs and out of band distortion. The goal is to make the differential part of the balun electrically and physically symmetric; a linear phase response in the pass band also helps to minimize distortion.

The front-end is baseband with a bandwidth of 200MHz per channel. Phase coherence between the channels is maintained so that this signal source may serve as quadrature modulation source.

The above details are primarily analog, my additional responsibilities included:

- Internal/External 10MHz Reference Circuit design and layout
- Data Clock Generator layout and programming
- Circuit design and layout to support automated, internal calibration of the signal chain
- General programming, SPI, to control tunable parameters


I AttenuateTune /6
I FilterTune /8
I Offset /16
I Gain /10
I Data / 16
DAC (I)
DAC Out I+
DAC Out I-
DC-200MHz Balun
I FullScale
Fixed Gain Amplifier
I Amplified
Tunable Filter
I Filtered
Step Attenuator
I Out
50 Ohm BNC
Can Be Combined
To Include SPI Interfaces
IQ Phase Adjust /10
Can Be Combined
50 Ohm BNC
Q Data /16
DAC (Q)
DAC Out Q+
DAC Out Q-
DC-200MHz Balun
Q FullScale
Fixed Gain Amplifier
Q Amplified
Tunable Filter
Q Filtered
Step Attenuator
Q Out
Q Gain /10
Q Offset /16
Q FilterTune /8
Q AttenuateTune /6
Clock
Conditioned Power
Power Conditioner
5VDC 20W
Clock Synthesizer
Base Clock
Time Base Cleaner
10 MHz Timebase