AN ABSTRACT OF THE DISSERTATION OF

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Title: Design Techniques For Delta Sigma Modulators Using VCO Based ADCs

Abstract approved: _____

Pavan Kumar Hanumolu

VCO-based ADCs have recently emerged as attractive alternative to conventional Delta Sigma ($\Delta\Sigma$) modulator architectures. Few salient features of a VCO-based ADC are: 1) the quantization noise is 1^{st} order noise shaped, 2) it is an open loop architecture, and, 3) its implementation is mostly digital in nature. Hence, they are ideally suited for oversampled data converter techniques with the capability to operate at near GHz frequencies. However, their performance is severely limited by the non-linearity of the voltage to frequency transfer curve. Also, when operating at GHz frequencies, the excess loop delay (ELD) of a continuous-time $\Delta\Sigma$ modulator can be a large fraction of the sampling period, thereby affecting the of stability of the modulator. In this work, two new architectures are proposed to overcome the above mentioned drawbacks.

In the first approach, a continuous-time Delta Sigma modulator incorporates a

non-linear VCO as the second stage in a 2-stage residue canceling quantizer (RCQ) and mitigates the impact of its non-linearity by spanning only a small region of the VCOs tuning curve.

In the second approach, both phase and frequency domain information are extracted from the VCO and fedback, which provides an extra clock cycle delay in the feeback path. This relaxes the timing constraints for the modulator, allowing it to be clocked at GHz frequencies.

Design Techniques For Delta Sigma Modulators Using VCO Based ADCs

by

Karthikeyan Reddy

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Karthikeyan Reddy, Author

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CHAPTER 1

INTRODUCTION

Analog to Digital Converters (ADC) are indispensable building blocks of modern day electronic systems. They are found in RF receivers, sensor circuits, audio and video systems, medical instrumentation and industrial solutions. A typical electronic system consists of an analog frontend circuit followed by an ADC, a digital signal processor (DSP) and an output interface circuit as shown in Figure 1.1. Depending on the application, the front end performs one or more combinations of amplification, filtering and frequency modulation on the input signal. The ADC then converts the frontend output into digital data bits. Further digital processing techniques are applied on the digital bits in the DSP and the output is presented back to the real world through the interface circuit.

With finer CMOS processes, DSPs could process more complex algorithms, delivering better performance at faster rates and reduced power and area. This would mean that ADCs also have to work at higher sampling frequencies with better resolution. With a number of mobile applications on the rise, power is

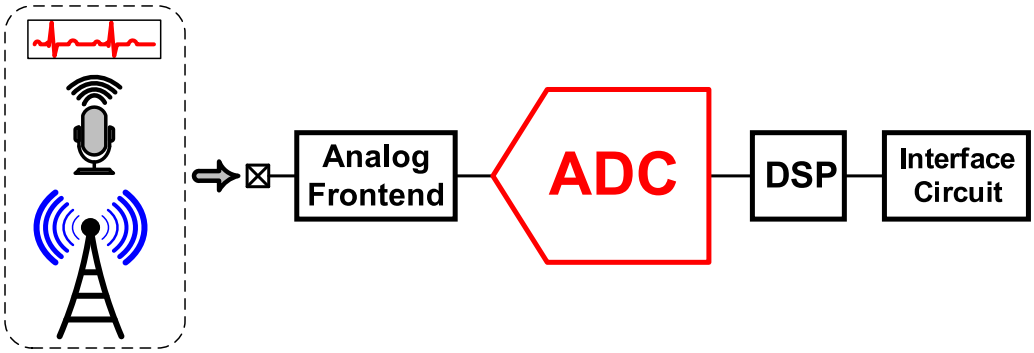

Figure 1.1: Analog to Digital Converter embedded in an electronic system

also a critical component of today's designs and hence the ADC has to be power efficient.

1.1 Scope of this work

Continuous-time (CT) $\Delta\Sigma$ modulators are fast becoming the favoured means of implementing ADCs in wireless applications due to their inherent anti-alias filtering characteristics. Figure 1.2 plots the Figure of Merit (FoM) and Effective number of bits (ENOB) of all the CT $\Delta\Sigma$ modulators published in the International Solid State Circuits Conference between 1997 and 2013 [2]. Over the years, they are shown to have excellent power efficiency (as is evident in Figure 1.2(a)) while achieving better than 12 bit resolution and several MHz signal bandwidth. As the maximum sampling frequency is limited by technology, conventional $\Delta\Sigma$ ADCs combine multi-bit quantization with a higher order loop filter to extend the signal bandwidth. However, additional amplifiers needed to increase the order of the loop filter incur a large power penalty and designing precise analog comparators in deep

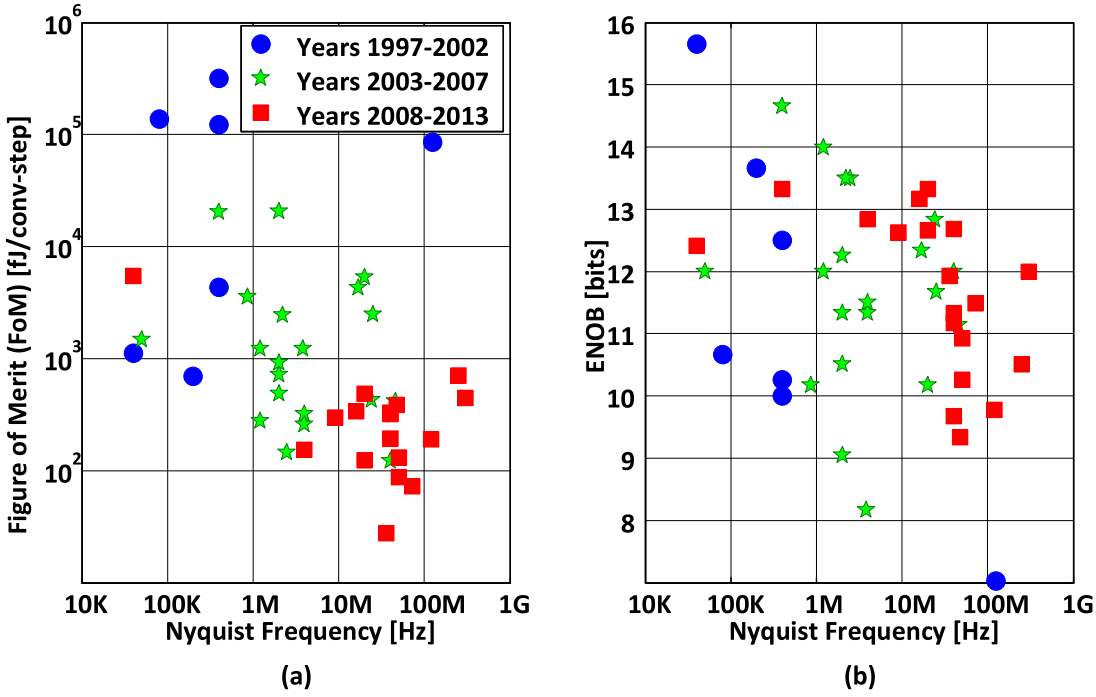

Figure 1.2: Survey of CT $\Delta\Sigma$ Modulators from 1997 to 2013.

sub-micron processes is a challenging design task.

VCO-based ADCs have recently emerged as an attractive alternative to conventional delta sigma architectures [3], [4], [5], [6], [7]. VCO based ADCs achieve first order noise shaping in an open loop manner. Because VCO-based ADCs are implemented using mostly digital circuits such as CMOS inverters and flip flops, they benefit from technology scaling and are capable of operating with GHz sampling clock frequencies. However, the performance of VCO based ADCs is severely limited by the non-linearity of the VCO's voltage-to-frequency (V-to-F) transfer characteristic. Because increasing the signal power mandates exercising the entire non-linear tuning range, VCO-based ADC's performance is severely distortion

limited. Due to their noise shaping abilities, VCO based ADCs are also used as internal quantizers in CT $\Delta\Sigma$ modulators. The ability to still operate at GHz frequencies is severely hindered by large excess loop delay (ELD) at such low sampling periods. This work presents two techniques to overcome the detrimental impact of VCO non-linearity and the stability issue due to ELD.

1.2 Organization

The rest of the thesis is organized as follows. Chapter 2 provides a brief overview of VCO-based ADCs. Some of the advantages and disadvantages of recent architectures in VCO based ADCs are also presented in this chapter. The residue cancelling quantizer, a technique to mitigate VCO non-linearity, is presented in chapter 3. In chapter 4, a dual feedback architecture has been proposed to overcome the stability issue due to excess loop delay. Chapter 5 provides a summary of this work and concludes this dissertation.

CHAPTER 2

VOLTAGE CONTROLLED OSCILLATOR BASED ADCs

The conceptual block diagram of a VCO-based ADC is shown in Fig. 2.1. A voltage controlled oscillator (VCO) converts analog input voltage, V_{IN}, into an output frequency, F_{OUT}. The digital output is generated by measuring F_{OUT} using a frequency-to-digital converter (FDC).

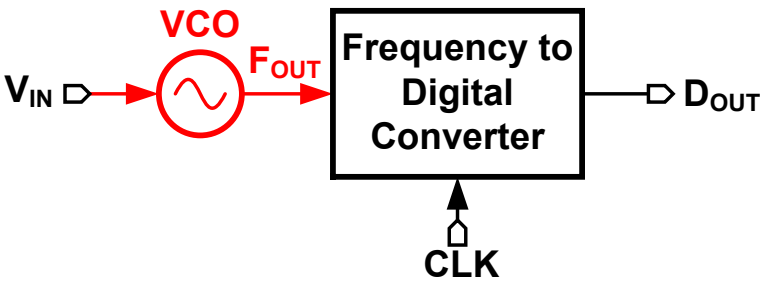

Figure 2.1: Conceptual block diagram of a VCO-based ADC.

While there are several ways to implement the FDC, the most efficient method amenable for high sampling rates is to sample the phase of the VCO as depicted

in Fig. 2.2(a). The sampled oscillator output phase is quantized using a phase to digital converter and digitally differentiated to generate the quantized frequency output. To understand the noise shaping property of the VCO-based ADC, consider its frequency domain model shown in Fig. 2.2(b). The VCO is modeled as an voltage-to-phase integrator, phase sampler as a scale factor, phase-to-digital converter as a summing node that adds the phase quantization error, and digital differentiator by the first order difference block. Using this model, it can be shown that signal transfer function (STF) of the VCO-based ADC is [8]:

$$\mathrm{STF(f)} = \mathrm{K_{VCO}} e^{-j\pi \mathrm{T_s f}} \frac{\sin(\pi \mathrm{T_s f})}{\pi \mathrm{f}} \tag{2.1}$$

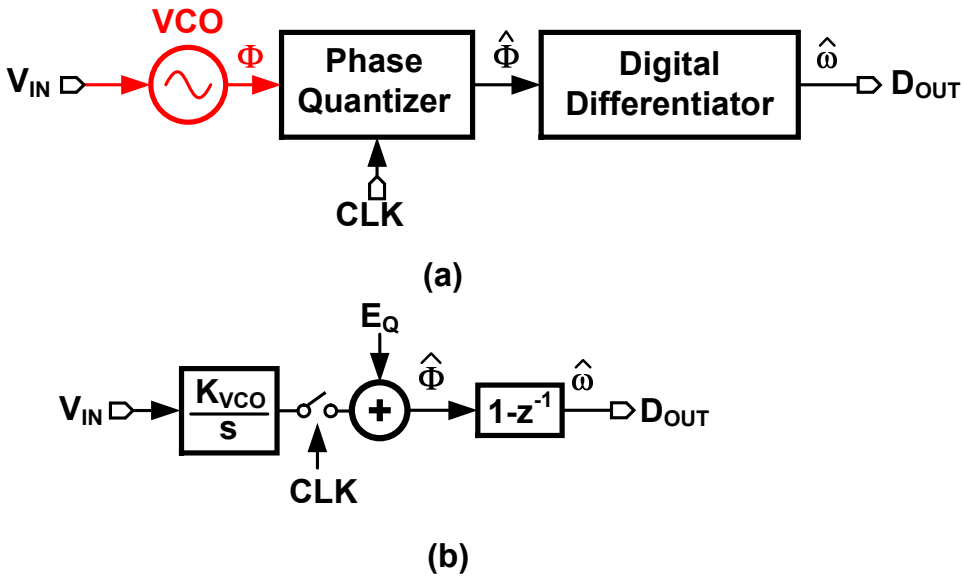

Figure 2.2: (a) Block diagram of a noise shaping VCO-based ADC, and (b) Frequency domain model.

The low pass magnitude response of the STF provides implicit anti-alias filtering similar to that of a conventional continuous-time ΣΔ ADC. Because the output of the phase-to-digital converter is digitally differentiated, quantization error, E_Q, is first order noise shaped by the filter, $1 - z^{-1}$. In other words, the noise transfer function , NTF of the VCO-based ADC is:

$$\mathrm{NTF}(z) = 1 - z^{-1} \tag{2.2}$$

A practical implementation of a VCO-based ADC is shown in Fig. 2.3. The VCO is implemented using a N-stage oscillator (N = 5 in the figure for illustration) whose frequency of oscillation, F_{osc} is controlled by the input voltage V_{IN} such that,

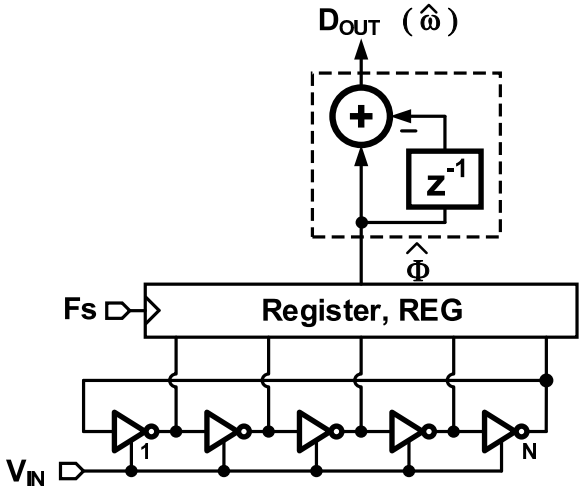

Figure 2.3: A practical implementation of a VCO-based ADC.

$$F_{osc} = F_{fr} + K_{VCO} V_{IN} \tag{2.3}$$

where F_{fr} is the free running frequency of the oscillator and K_{VCO} is the voltage-to-frequency gain. The oscillator phase is sampled by a set of flip-flops and mapped to a digital output to produce the quantized phase. This operation is further illustrated using the phasor diagram shown in Fig. 2.4. The N-bit word captured by phase samplers can have 2N unique values (also called as states), which correspond to the 2N quantized levels of the phase. The number of state transitions within one clock period is proportional to the oscillating frequency and hence the difference between successive sampled phase values gives the quantized output, D_{OUT}.

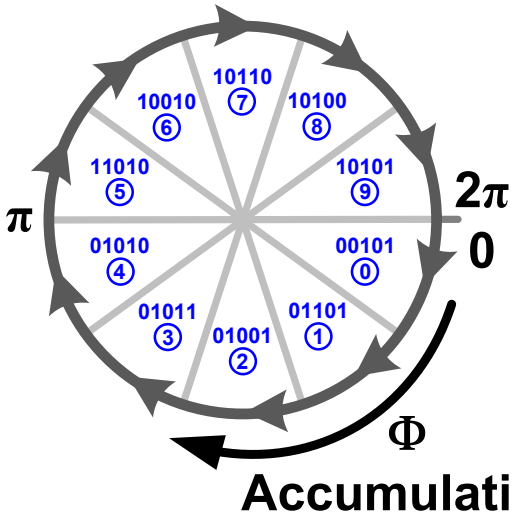

Figure 2.4: Phasor diagram of VCO output.

If the number of transitions of each inverter is restricted to one within the sample period, a setup with a DFF and XOR gate could be used to capture the transitions as shown in 2.5. The XOR outputs a one if there is a transition, and zero otherwise. The output of the XOR gates is a thermometer code and their count is the number of transitions within a sample period. Since the transitions

in the ring oscillator traverse in a cyclic fashion, the thermometer code is data weighed averaged sequence in nature.

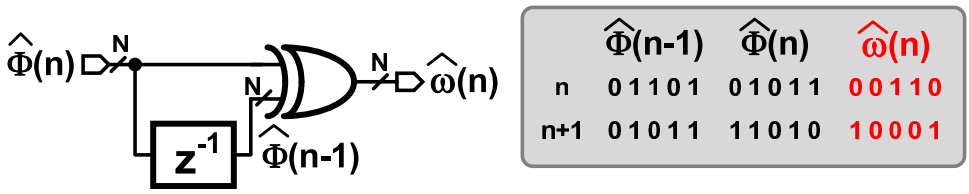

Figure 2.5: Implementation of the differentiation logic using XOR gates.

In the discussion thus far, we assumed that the VCO frequency is a linear function of the input voltage, leading to a constant gain K_{VCO}. However, in most practical VCO implementations, the delay of each stage in the ring oscillator scales linearly with the input voltage rendering an inherent non-linearity to the voltage-to-frequency (V-to-F) transfer curve [8]. Additional circuit non-idealities only further exacerbate this issue. While it appears that VCO non-linearity can be mitigated by tuning the delay as a function of the reciprocal of the input voltage, it is very challenging to implement such a tuning scheme. Consequently, in practice, the V-to-F nonlinearity causes the VCO-based ADC performance to be severely distortion limited. Transistor-level simulations indicate a dynamic range of about 35dB can be achieved at best. Figure 2.6 shows PSD of a ring oscillator based ADC. Each delay cell in the ring oscillator was implemented as a current starved inverter. While a SQNR of 62dB could be attained for an OSR of 32, the performance is limited due to the 35dB third harmonic distortion.

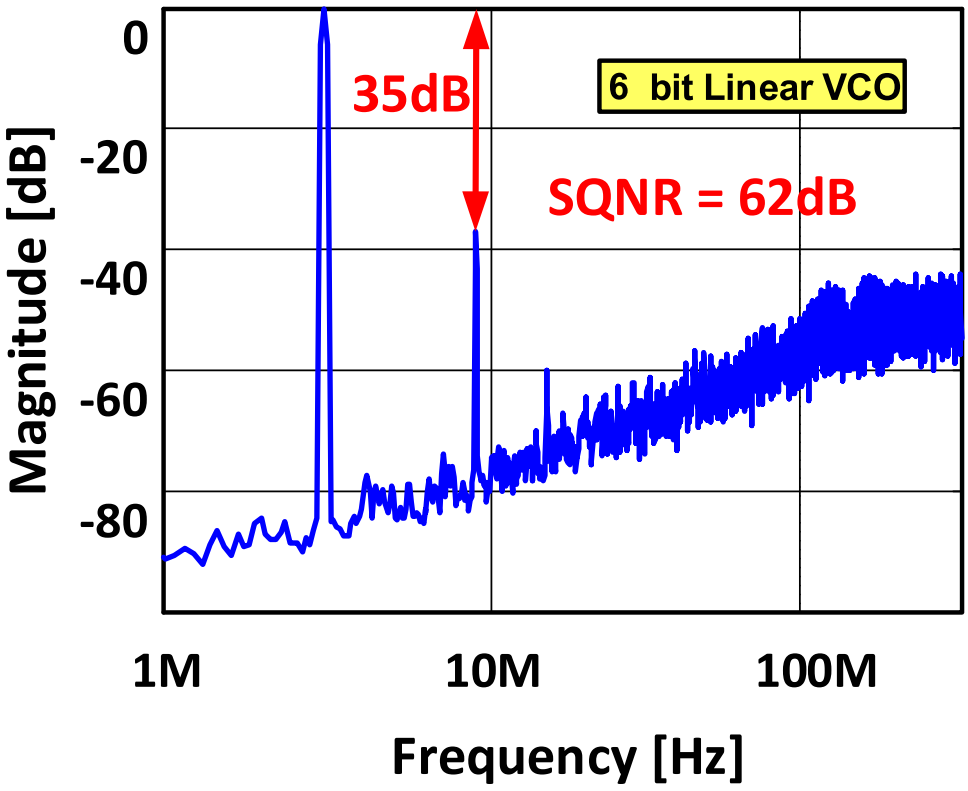

Figure 2.6: Simulated output spectrum of a VCO based ADC.

2.1 Prior Solutions

Several techniques to mitigate distortion caused by the VCO's non-linear tuning curve have been proposed in recent years some of which are briefly discussed in this section.

2.1.1 Digital Background Calibration

A digital background calibration technique is shown in Figure 2.7 [9]. The linearizer is a look-up table (LUT) which implements the inverse V-to-F transfer function. It maps the digital output code of the quantizer, D_{VCO}, to an accurate D_{OUT} which is obtained from the calibration unit.

The calibration unit consists of a frequency locked loop (FLL), with the quantized frequency information provided by the up down counter. By employing a replica VCO in the feedback path, the FLL realizes the inverse V-to-F transfer characteristics at the accumulator output, which provides the high resolution digital code for the LUT.

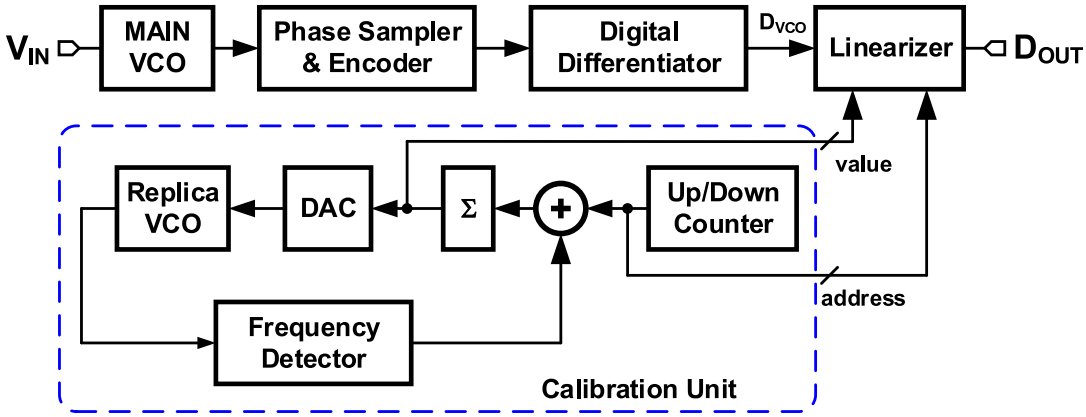

Figure 2.7: Prior art: FLL based Digital background calibration technique.

Another digital background calibration technique, illustrated in Fig. 2.8, employs a calibration unit to cancel the 2^{nd} and 3^{rd} order distortion terms caused by the VCO non-linearity [8]. Operating in background, the calibration unit uses a replica VCO to measure the non-linearity of the main VCO. The estimated

nonlinear coefficient is used to correct the VCO-based ADC output. While this work demonstrated excellent linearity, it suffers from three drawbacks. First, because open loop VCO-based ADCs are limited to first order noise shaping they require sampling clocks in the multi-GHz range to achieve high resolution. Second, matching between the replica and the main VCO needed for good cancelation of the non-linearity is difficult to ensure in deep sub-micron CMOS processes with large variability. Finally, the calibration algorithm is complex and takes very long to converge.

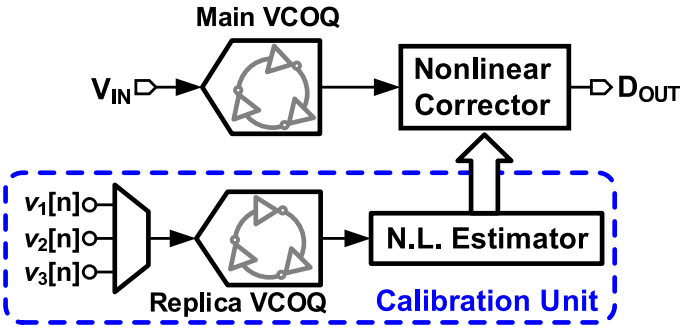

Figure 2.8: Prior art: Coefficient estimation based Digital background calibration technique.

2.1.2 Two level Modulation of VCO input

A calibration-free architecture that seeks to improve the linearity by operating the VCO at only two output frequencies was proposed in [10]. A pulse width modulator converts the analog input voltage to a 2-level signal and drives the VCO to operate it only at either of the two frequencies, F_{HIGH} or F_{LOW}. Since only two operating points on the V-to-F tuning curve are used, the detrimental

impact of VCO nonlinearity on the ADC performance is eliminated. Even though a naturally sampled PWM does not ideally produce any distortion tones within the signal band, it creates many tones around the PWM carrier frequency, F_C, as shown in the representative output spectrum in Fig. 2.9 [11]. Increasing F_C to push these tones to higher frequencies increases power dissipation in the PWM generation circuitry. Furthermore, the quantization error suppression is also limited by first order noise shaping.

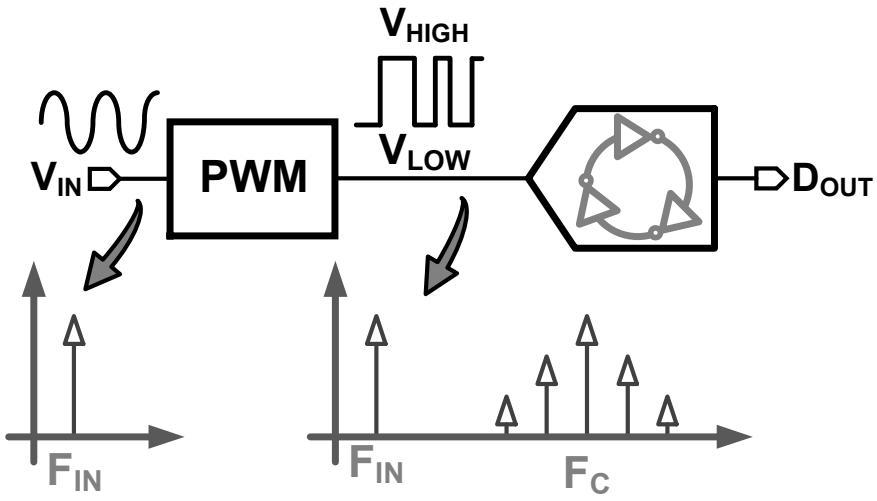

Figure 2.9: Prior art: PWM front end for a VCO based ADC.

2.1.3 $\Delta\Sigma$ Modulator utilizing a VCO based ADC

To circumvent the VCO non-linearity and increase the order of noise shaping simultaneously, the VCO-based ADC was used as a quantizer in a $\Delta\Sigma$ feedback loop as illustrated in Fig. 2.10 [12]. Loop filter, L(s), suppresses the VCO non-linearity to the extent of its gain in the signal bandwidth. Higher order noise shaping can be

achieved by increasing the order of the loop filter. However, the effectiveness of this technique greatly depends on the gain of the loop filter. Because VCO quantizer input spans the entire signal range, it exercises the entire non-linear tuning curve of the VCO. As a result, a very high gain loop filter is needed to suppress the large amount of distortion introduced by the VCO which causes the ADC performance to be always limited by the VCO non-linearity.

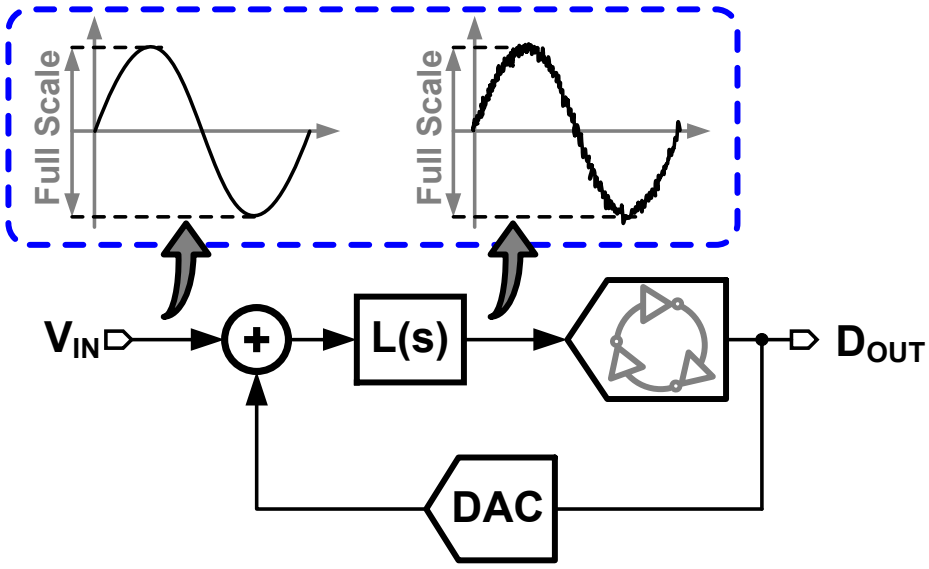

Figure 2.10: Prior art: $\Delta\Sigma$ ADC with VCO quantizer.

To quantify this limitation, the $\Delta\Sigma$ modulator was simulated with different orders of the loop filter for a fixed OSR of 32 and the results are summarized in Table 2.1.

An order of 0 corresponds to just an open loop non-linear VCO quantizer. With a 6-bit linear VCO, the signal-to-quantization noise ratio (SQNR) is 62dB but, as expected, the spurious-free dynamic range (SFDR) is only 35dB. A first

Table 2.1: SNDR and SFDR of a $\Delta\Sigma$ ADC with VCO quantizer for different orders of L(s).

Order	**SNDR (dB)**	**SFDR(dB)**
0	62	35
1	86	58
2	103	73
3	120	88

order loop filter suppresses both the quantization error and the VCO non-linearity by approximately 24dB resulting in an SQNR of 86dB and an SFDR of 58dB. This table shows that at least a third order loop filter is needed to achieve an SFDR of 88dB. Such high order loop-filters are not only difficult to design but also degrade loop stability and increase power dissipation. In view of these drawbacks, we propose a new architecture that seeks to suppress VCO non-linearity without increasing the order of the loop filter.

CHAPTER 3

CONTINUOUS TIME $\Delta\Sigma$ MODULATOR USING A RESIDUE CANCELLING QUANTIZER

3.1 Proposed Architecture

The inability of the $\Delta\Sigma$ loop, discussed in the previous chapter, to completely suppress the VCO nonlinearity is attributed to the large voltage swing at its input. The proposed architecture is based on a simple observation that the impact of VCO non-linearity on the ADC performance can be suppressed by not exercising the non-linear region of the VCO's V-to-F transfer curve. To this end, the proposed VCO-based residue canceling quantizer (RCQ) shown in Fig. 3.1 seeks to minimize the voltage swing at the input of the VCO [13]. Analogous to a classical two step ADC, the proposed RCQ is composed of a cascade of two stages. The first stage, implemented using a combination of flash ADC (ADC_F) and a digital-to-analog converter (DAC_F), determines a coarse estimate of the input voltage, $\hat{V}_{IN}$. The

estimation error, commonly referred to as a residue, is obtained by subtracting $\hat{V}_{IN}$ from input voltage V_{IN}. The residue voltage, which is nominally equal to the quantization error of ADC_F, E_{Q1}, is subsequently digitized by the second stage, implemented using a VCO-based ADC. When the outputs of the two stages are added to generate RCQ output, D_{OUT}, the residue is canceled and it contains only first order noise shaped quantization error from the second stage. Mathematically,

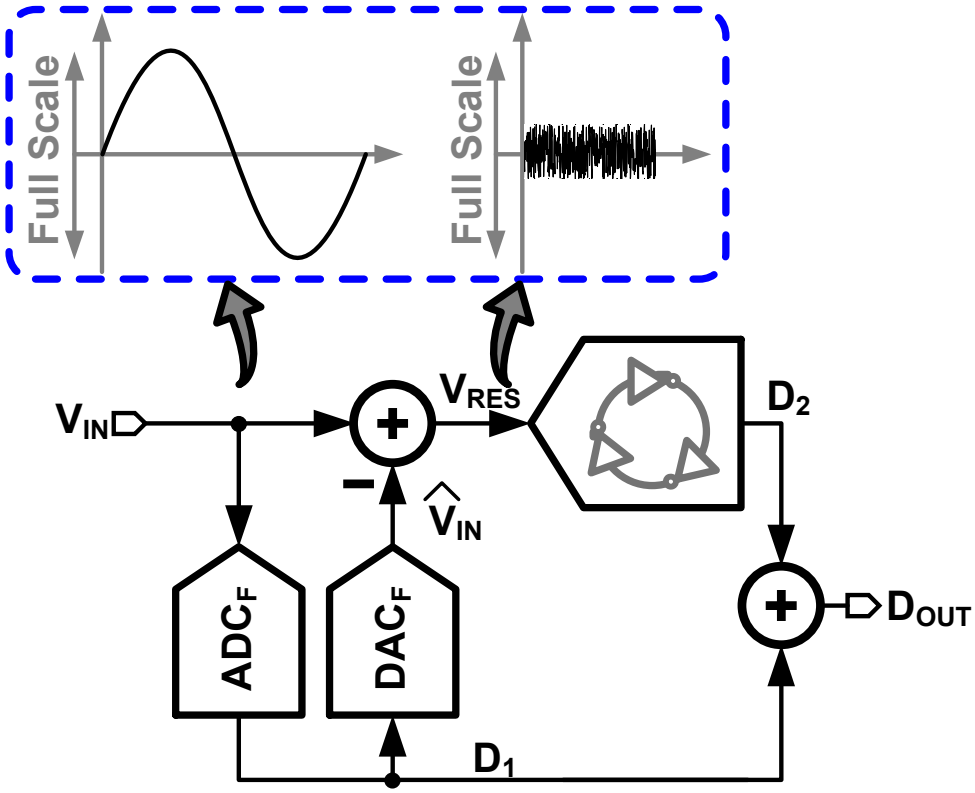

Figure 3.1: Block diagram of the proposed VCO-based residue canceling quantizer.

$$\hat{V}_{IN} = V_{IN} + E_{Q1} \tag{3.1}$$

$$V_{RES} = -E_{Q1} \tag{3.2}$$

$$D_1 = V_{IN} + E_{Q1} \tag{3.3}$$

$$D_2 = -E_{Q1} + E_{Q2}(1 - z^{-1}) \tag{3.4}$$

$$D_{OUT} = D_1 + D_2 = V_{IN} + E_{Q2}(1 - z^{-1}) \tag{3.5}$$

Because VCO process only a small residue voltage, its non-linear tuning characteristic is not exercised, thus suppressing its detrimental impact on the performance of the ADC. In this regard, the proposed RCQ bears some similarity to the ADCs proposed in [14], [15]. While all the residue cancelling approaches are, in principle, effective in suppressing the distortion due to VCO nonlinearity, circuit non-idealities in ADC_F, DAC_F, and the VCO limit their performance in practice, as discussed next.

3.1.1 Limitations of Residue Canceling Quantizer

An error model of the residue canceling quantizer that includes offset and gain errors of ADC_F, DAC_F, and the VCO is shown in Fig. 3.2. The conversion gain and offset of ADC_F are denoted by α_F and E_{OFF}, respectively. Mismatch errors in DAC_F are captured by the additive function $G(D_1)$, and α_D and α_V models DAC_F and VCO conversion gains, respectively. Using this model, the expression for the first stage output D_1, residue voltage V_{RES}, the second stage output D_2, and RCQ output D_{OUT} can be calculated as:

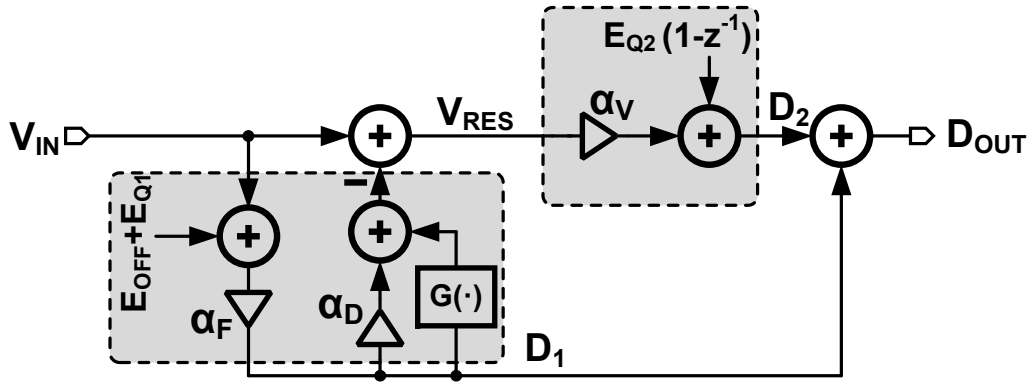

Figure 3.2: Error model of the residue canceling VCO quantizer.

$$\mathrm{D_1} = \alpha_\mathrm{F}(\mathrm{V_{IN}} + \mathrm{E_{Q1}} + \mathrm{E_{OFF}}) \tag{3.6}$$

$$\mathrm{V_{RES}} = -\alpha_\mathrm{FD}(\mathrm{E_{Q1}} + \mathrm{E_{OFF}}) + (1 - \alpha_\mathrm{FD})\ \mathrm{V_{IN}} - \mathrm{G(V_{D1})} \tag{3.7}$$

$$\mathrm{D_2} = (1 - \mathrm{z^{-1}})\mathrm{E_{Q2}} - \alpha_\mathrm{FDV}(\mathrm{E_{Q1}} + \mathrm{E_{OFF}}) + \alpha_\mathrm{V}(1 - \alpha_\mathrm{FD})\ \mathrm{V_{IN}} - \alpha_\mathrm{V}\ \mathrm{G(V_{D1})} \tag{3.8}$$

$$\mathrm{D_{OUT}} \approx \alpha_\mathrm{F}\mathrm{V_{IN}} + (1 - \mathrm{z^{-1}})\mathrm{E_{Q2}} + (1 - \alpha_\mathrm{DV})[\alpha_\mathrm{F}(\mathrm{E_{Q1}} + \mathrm{E_{OFF}})] - \alpha_\mathrm{V}\ \mathrm{G(V_{D1})} \tag{3.9}$$

Ideally, the product of $\mathrm{ADC_F}$ and $\mathrm{DAC_F}$ conversion gains must be equal to 1 ($\alpha_\mathrm{FD} = \alpha_\mathrm{F}\ \cdot\ \alpha_\mathrm{D}\ =\ 1$) and similarly the product of $\mathrm{DAC_F}$ and VCOQ conversion gains must also be equal to 1 ($\alpha_\mathrm{DV} = \alpha_\mathrm{D} \cdot \alpha_\mathrm{V} = 1$). Under this condition, $\mathrm{E_{Q1}}$ and $\mathrm{E_{OFF}}$ are perfectly canceled at the output. The only detrimental impact of $\mathrm{E_{OFF}}$ is that it increases the residue voltage, which makes RCQ susceptible to VCO non-linearity (see Eq. 3.7).

In practice, it is difficult to ensure $\alpha_\mathrm{FD} = 1$ as α_F depends on $\mathrm{ADC_F}$ reference voltages and α_D depends on $\mathrm{DAC_F}$ bias currents, both of which are sensitive to

process, voltage, and temperature (PVT) variations. Therefore, if $\alpha_{FD} \neq 1$, Eq. 3.7 reveals that a small portion of V_{IN}, equal to $(1 - \alpha_{FD})V_{IN}$, leaks to the residue voltage. Assuming the conversion gains can be coarsely tuned such that α_{FD} is within $\pm 10\%$ error, the VCO only processes about 10% of full scale input, which causes minimal distortion degradation. Behavioral simulations indicate, with an error as large as 10%, there is no visible degradation in the performance of the ADC.

Mismatch in DAC_F unit elements results in an error which appears directly at the output of RCQ. Hence, DAC_F should be as linear as the overall RCQ. Since realizing highly linear DAC for higher order, high resolution conventional $\Delta\Sigma$ modulator is a common practice in deep sub-mircron CMOS process, realizing DAC_F to meet linearity requirements in a first order noise shaping ADC is not a concern [16] [17].

The conversion gain of the VCO quantizer, α_V is equal to:

$$\alpha_V = \frac{2NK_{VCO}}{F_S} \tag{3.10}$$

where, K_{VCO} denotes the V-to-F gain of the VCO, N is the number of VCO phases, and F_S is the sampling frequency. Because K_{VCO} is very sensitive to PVT variations, it is difficult to ensure $\alpha_{DV} = 1$ in practice. If $\alpha_{DV} \neq 1$, E_{Q1} is not perfectly canceled and appears in the final output as indicated by Eq. 3.9. The SNR degradation due to the leakage of E_{Q1} depends on the relative magnitudes of shaped second stage quantization error and the leaked E_{Q1}. For example, a 15-level ideal

RCQ achieves an SQNR of 62dB and 71dB for an OSR of 32 and 64, respectively. With a 4 bit ADC_F, the gain error that can be tolerated to cause a 3dB degradation in SQNR is roughly 8% (OSR = 32) and 4% (OSR = 64). Hence, the sensitivity to gain error in the second stage increases for large OSRs, and should be tightly controlled to minimize E_{Q1} leakage.

In summary, the proposed RCQ greatly reduces the performance degradation due to VCO non-linearity but suffers from two drawbacks that limit its viability for high resolution applications. First, RCQ achieves only first-order noise shaping and therefore requires a very high sampling clock frequency to achieve high SQNR. For instance with a 4-bit ADC_F and 15-level VCOQ, the sampling clock frequency must be greater than 5GHz to achieve an SQNR of 90dB in a 10MHz bandwidth. Second, the gain errors limit its performance particularly for high resolution applications. While it may be possible to accurately calibrate the gain errors, RCQ would still be quantization-error limited due to its first-order noise shaping.

3.1.2 Mitigation of RCQ Errors Using $\Delta\Sigma$ Feedback

To overcome the performance degradation caused by gain errors and also achieve higher order noise shaping, we propose to use RCQ as an internal quantizer in a $\Delta\Sigma$ loop as shown in Fig. 3.3 [13]. A high gain loop filter L(s), suppresses the RCQ quantization error and helps achieve high SQNR without increasing the sampling clock frequency into multi-GHz range. For example, with a first order loop filter and 15-level RCQ quantizer, an SQNR of 90dB can be achieved in a 10MHz bandwidth with a sampling clock frequency of 600MHz.

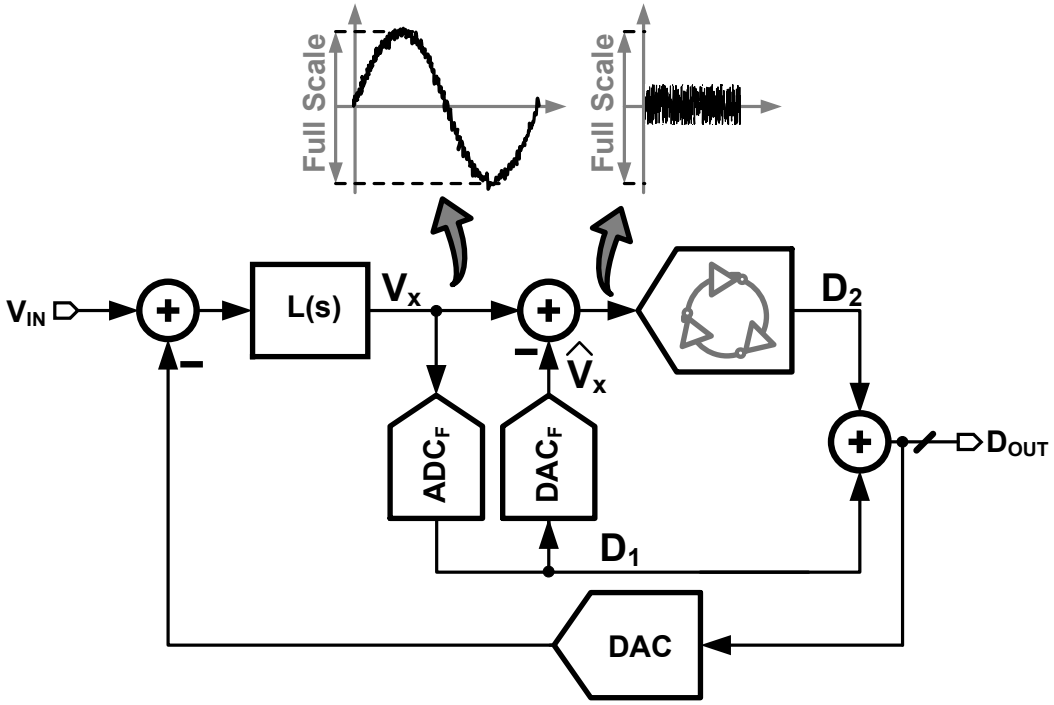

Figure 3.3: Block diagram of the proposed $\Delta\Sigma$ modulator using residue canceling quantizer.

Behavioral simulations were performed to quantify the effectiveness of $\Delta\Sigma$ loop in overcoming the limitations of RCQ quantizer discussed earlier and the results are summarized in Fig. 3.4. A first order loop filter, 4-bit $\mathrm{ADC_F}$ and a 15-level 6-bit linear VCO quantizer is used in these simulations. The simulated signal-to-noise plus distortion ratio (SNDR) is plotted as function of comparator offsets in $\mathrm{ADC_F}$ for hundred samples of the $\Delta\Sigma$ ADC in Fig. 3.4(a). As expected, even with a 0.5LSB 1-σ offset, SNDR degradation is less than 1dB. A plot of the SNDR versus $\mathrm{DAC_F}$ mismatch shown in Fig. 3.4(b) reveals that 9.5-bit 1-σ matching is needed to achieve 3σ SNDR of greater than 83dB. Figures 3.4(c) and (d) plot

SNDR as a function of gain errors in the first and second stages of RCQ. The $\Delta\Sigma$ loop minimizes SNDR degradation to less than 1dB and 6dB due to gain error of 10% in the first and second stages, respectively.

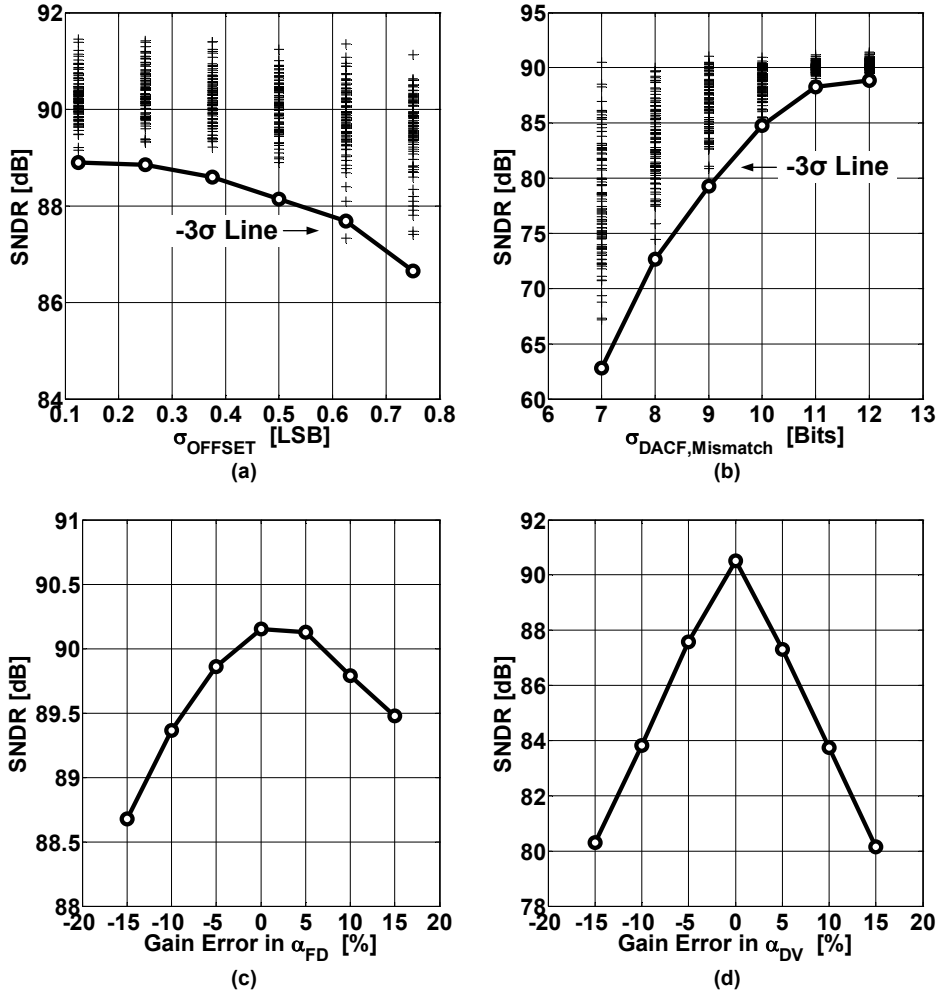

Figure 3.4: SNDR of the $\Delta\Sigma$ AD plotted as function of: (a) standard deviation of comparator offset (100 iterations for each offset) showing the -3σ boundary line, (b) standard deviation of $\mathrm{DAC_F}$ mismatch (100 iterations for each mismatch), (c) gain error in α_{FD}, and (d) gain error in α_{DV}.

The simulated power spectral density of the $\Delta\Sigma$ ADC output is depicted in Fig. 3.5. With a gain error of 5% in the first and second stages of RCQ, comparator offset of 1/4 LSB and DAC_F with 9.5bit matching, the distortion terms are 85dB below the full scale input.

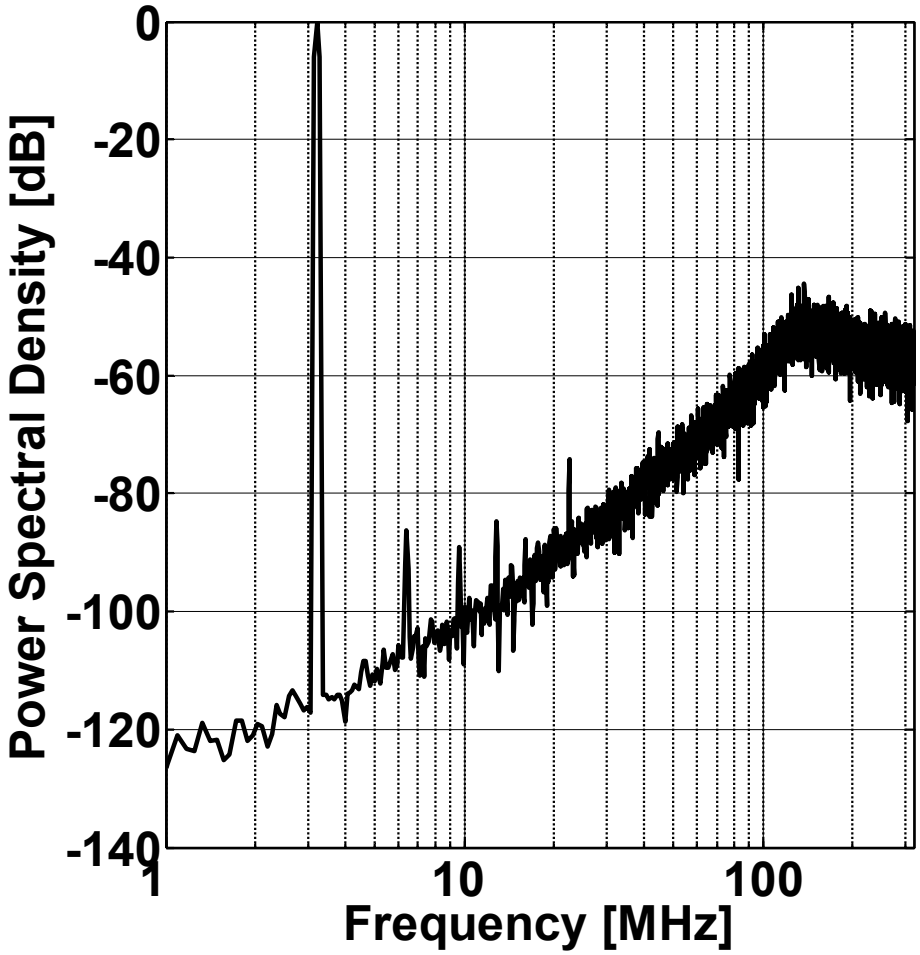

Figure 3.5: Simulated output PSD of the $\Delta\Sigma$ modulator.

3.2 Prototype Continuous-time $\Delta\Sigma$ Modulator

The block diagram of the proposed continuous-time $\Delta\Sigma$ modulator is shown in Fig. 3.6 [13]. It incorporates a first order active loop filter implemented using an opamp-RC integrator, a residue canceling quantizer that uses a 4-bit flash ADC_F in the first stage and a 15-stage pseudo-differential VCO in the second stage to achieve second-order noise shaping of the quantization error. The voltage generated across R_F by the DAC current I_{DACF} is subtracted from the integrator output to produce the residue, V_P. Transistor level simulations indicated that a 4-bit ADC_F was adequate to ensure that the residue voltage is restricted to within $\pm$100mV and the VCO non-linearity is sufficiently suppressed. Behavioral simulations of the modulator with these parameters indicate that an SQNR of greater than 80dB in a 10MHz bandwidth at 600MHz sampling rate can be achieved.

To allow sufficient regeneration time for the comparators in ADC_F, a quarter clock period delay (denoted by $z^{-1/4}$ block in Fig. 3.6) is introduced between ADC_F and DAC_F clocks. For a similar reason, the same delay was also added between the clocks of VCOQ and the main feedback DAC. In the presence of these delays, the discrete time transfer function from the node D_1 to D_2 can be calculated from the model shown in Fig. 3.7. Using impulse invariance technique, the transfer function of this path is evaluated to be $\frac{z^{-1}+z^{-2}}{2}$. To effectively cancel the quantization noise of ADC_F at the output of RCQ, D_1 is fed to an identical digital filter, $H_M(z)$ which is implemented as a two tap FIR structure with coefficients equal to 0.5.

The main feedback DAC should be driven by D_{OUT}, obtained by adding four

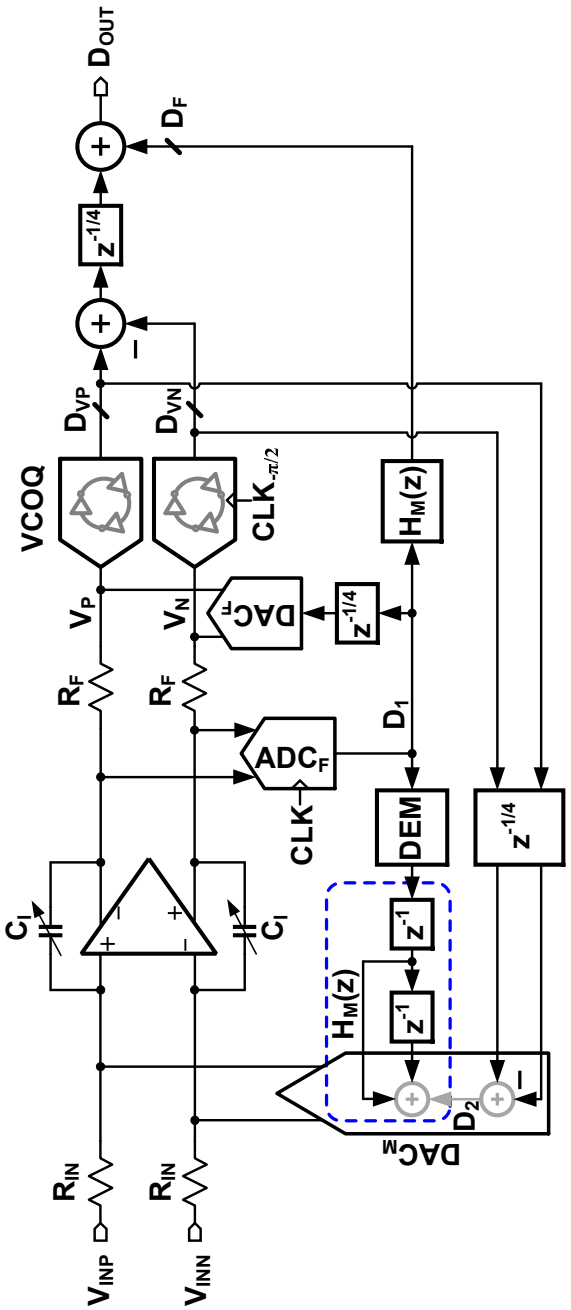

Figure 3.6: Block diagram of the proposed $\Delta\Sigma$ modulator.

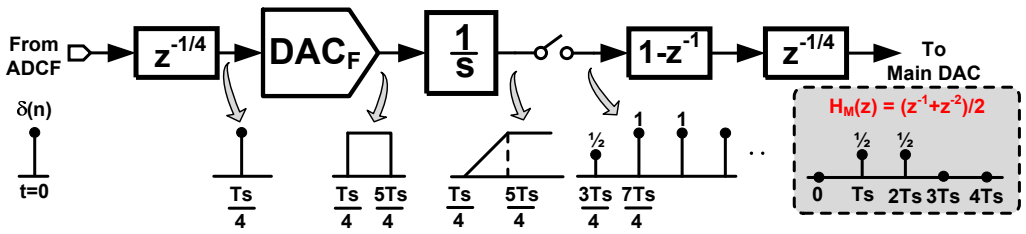

Figure 3.7: Impulse invariance transformation of the DAC_F and the VCO quantizer.

sets of digital codes: two tap outputs of the FIR filter and the two pseudo differential codes of VCOQ. At 600MHz, digital adders consume large power to keep the excess loop delay below acceptable levels. Hence, data bits are fed to four current steering DACs and the addition is performed in current domain. Because the main feedback DAC needs to be as linear as the entire ADC, its mismatch is noise shaped using dynamic element matching (DEM). Explicit DEM was not needed for D_2 because VCOQ provides implicit barrel shifting of its codes [12].

3.3 NTF of the modulator

Figure 3.8 shows the frequency domain model of the proposed 1^{st} order prototype modulator. ADC_F is replaced by a sampling switch and additive quantization noise E_1. DAC_F is replaced by its delay $z^{-\frac{1}{4}}$. The VCO is replaced by the integrator followed by sampling and discrete time differentiation. The delay $z^{-\frac{1}{4}}$ in the VCO path is the clocking delay between the VCO and the feedback DAC. The feedback DAC is represented by a zero order hold (ZOH) block. From previous discussions on RCQ, it has been established that path 1 and path 2 have the same transfer

function, which cancel each other. Hence only path 3 contributes to the noise transfer function which is show in the simplified model in Figure 3.9. The shaded

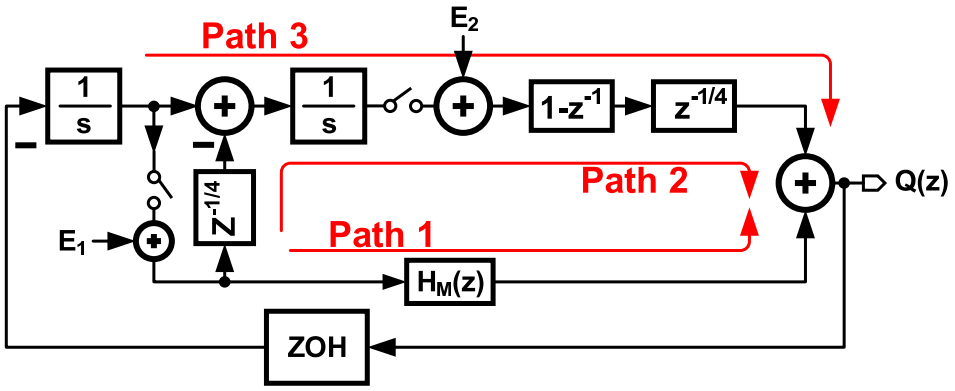

Figure 3.8: Frequency domain model of the modulator.

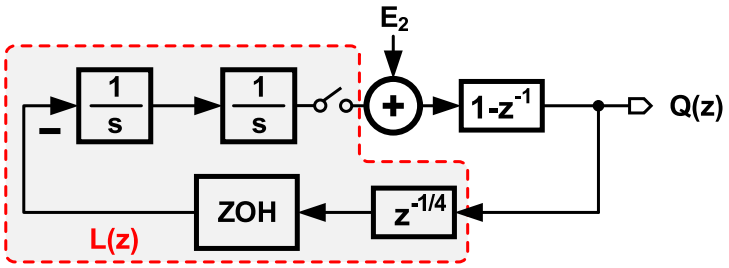

Figure 3.9: Simplified frequency domain model to compute the noise transfer function.

region within the red block shows the continuous time loopfilter, whose discrete time equivalent is determined by the impulse invariance transform of L(s) and is given by:

$$L(z) = \frac{0.28125z^{-1} + 0.6875z^{-2} + 0.03125z^{-3}}{1 - 2z^{-1} + z^{-2}} \tag{3.11}$$

The NTF is then given by:

$$
\begin{aligned}
NTF(z) &= \frac{Q(z)}{E_2(z)} \\
&= \frac{1 - z^{-1}}{1 + \dfrac{(1 - z^{-1})(0.28125z^{-1} + 0.6875z^{-2} + 0.03125z^{-3})}{1 - 2z^{-1} + z^{-2}}} \\
&= \frac{(1 - z^{-1})^2}{1 - 0.71875z^{-1} + 0.6875z^{-2} + 0.03125z^{-3}}
\end{aligned}
\tag{3.12}
$$

Figure 3.10(a) shows the pole zero plot of the noise transfer function(NTF) and Figure 3.10(b) plots the magnitude and phase response of the NTF. The peaking in in the transistion region of the NTF is a desired characteristic as they are less sensitive to clock jitter [18].

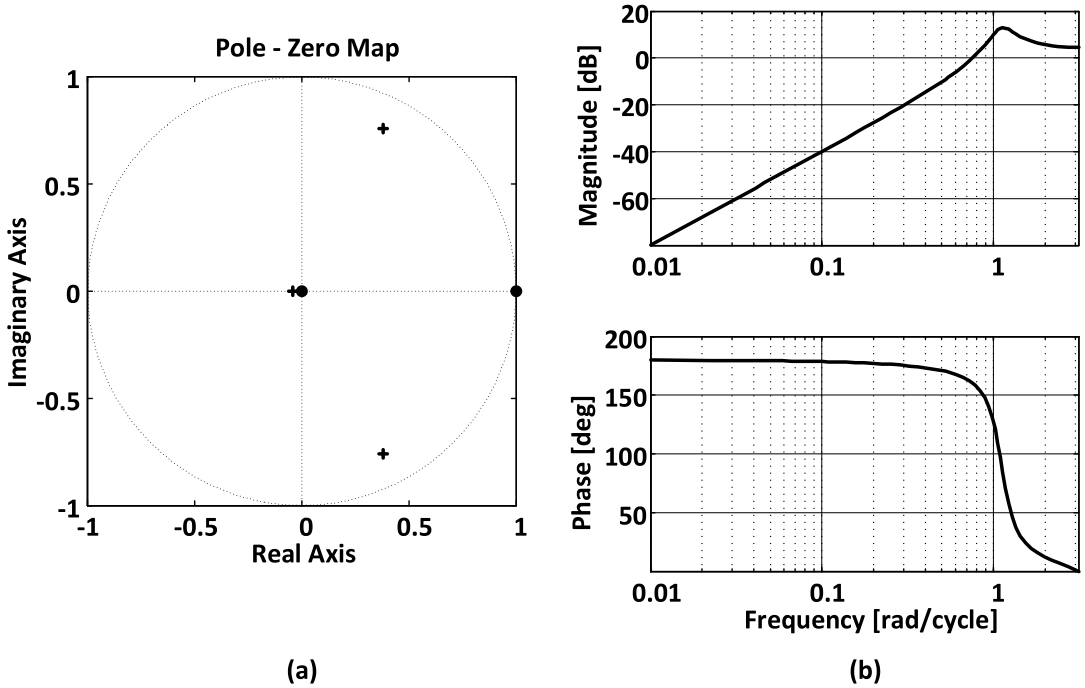

Figure 3.10: (a) Pole zero map of the NTF (b) Bode plot of the NTF

3.4 Schematic Design

The circuit design details of the key building blocks in the modulator are described next.

3.4.1 VCO Quantizer

The schematic of the VCO quantizer is shown in Fig. 3.11. The input signals to the quantizer, V_P and V_N, are separately processed by the positive and negative half circuits in a pseudo-differential manner. Each half circuit consists of a 15-stage voltage controlled ring oscillator, an array of sense amplifier flip flops, and a digital differentiator that produces the digital output. Each stage in the VCO is implemented using two coupled CMOS inverters. Transistor M_0 converts the input voltage to current and tunes the oscillator frequency. VCO gain is digitally tuned by varying the size of M_0 using the control word, D_{KVCO}. Phase sampling and quantization is performed by an array of sense-amplifier flip-flops and first-order digital differentiation is implemented using an array of true-single-phase clock (TSPC) flip-flops and static XOR gates. To prevent overloading of the phase samplers, maximum VCO frequency is restricted to be less than half the sampling frequency.

The V-to-F transfer characteristic of the VCO ideally has infinite bandwidth. However, in practice, a parasitic pole is always present at the control node of the oscillator, X_P which adds undesirable phase shift and alters the modulator loop transfer function. Denoting the impedance looking into the oscillator as R_{VCO},

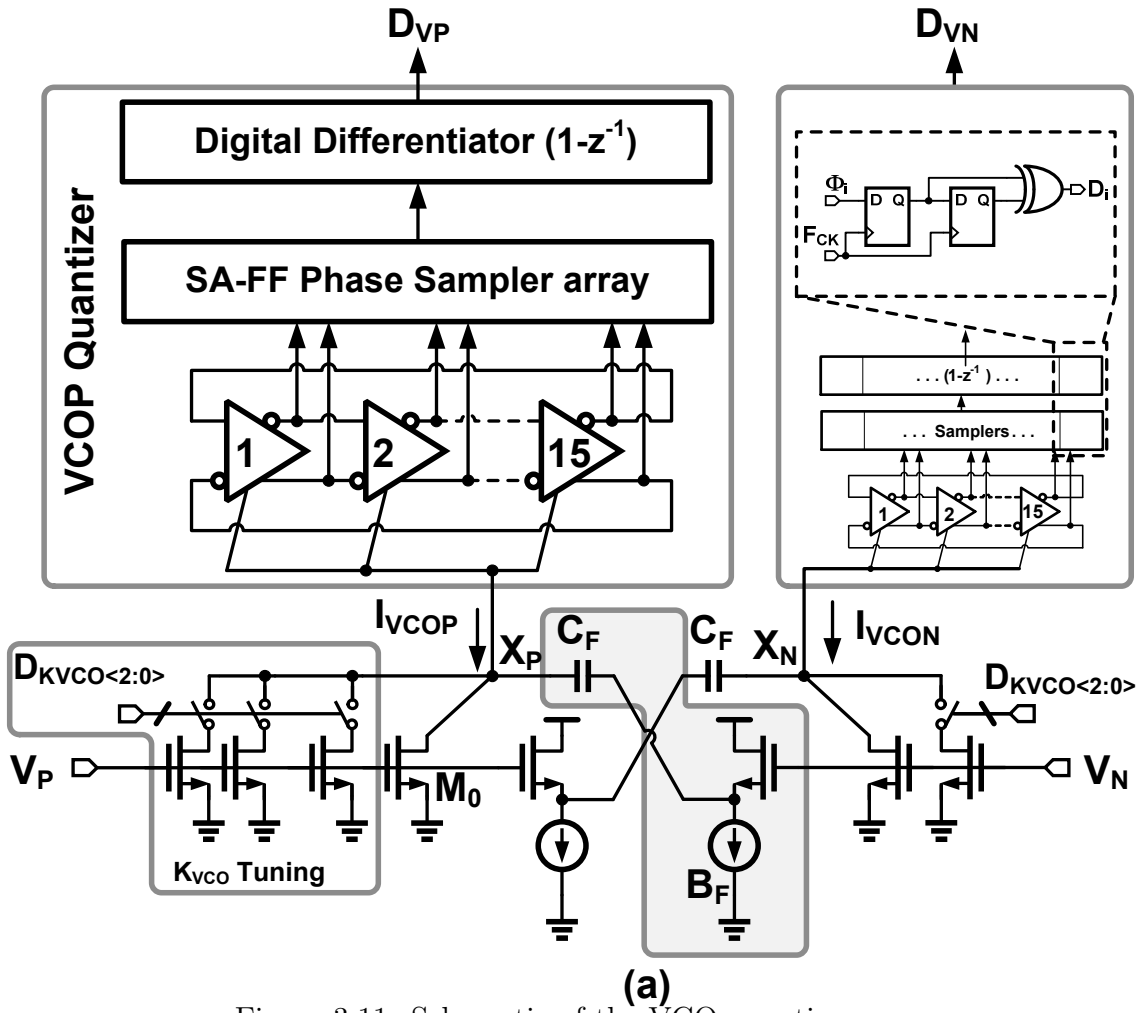

Figure 3.11: Schematic of the VCO quantizer.

parasitic capacitor by C_{VCO}, a pole is introduced at $\omega_p = 1/(R_{VCO}C_{VCO})$. The phase shift added by this pole can be compensated by adding a faster loop around the quantizer at the cost of increased power dissipation. In this work, we propose to extend the V-to-F bandwidth of the VCO and obviate the need for any additional loop delay compensation circuitry. The proposed bandwidth enhancement technique is shown in the shaded region in Fig. 3.11 . A buffer B_F and capacitor

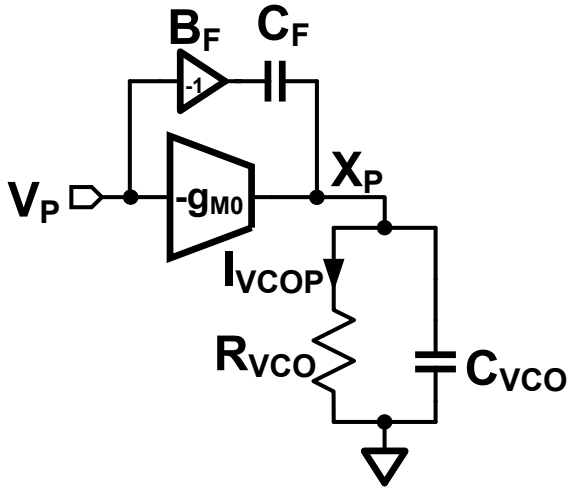

Figure 3.12: Small signal model of the compensation scheme in the VCO.

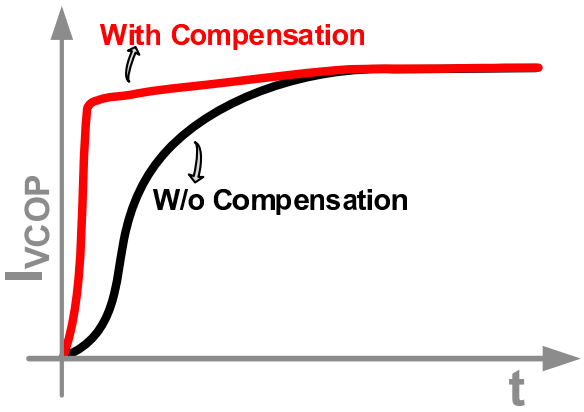

Figure 3.13: VCO step response with and without the compensation.

C_F couple the negative input of the VCO to node X_P and introduces a zero, ω_z, in the VCO transfer function. Analysis of this compensation scheme using the small-signal model in Fig. 3.12 reveals that $\omega_z = g_{M0}/C_F$. By nominally matching ω_z and ω_p, VCO bandwidth is greatly extended. Transistor-level simulation of the VCO indicates that the effective time constant is reduced to less than 200ps

after compensation from an otherwise uncompensated time constant of 700ps (see Figure 3.13). Simulations of the modulator indicate that this method of bandwidth enhancement is adequate to obviate the need for explicit excess loop delay compensation under all process corner conditions.

3.4.2 Loop filter

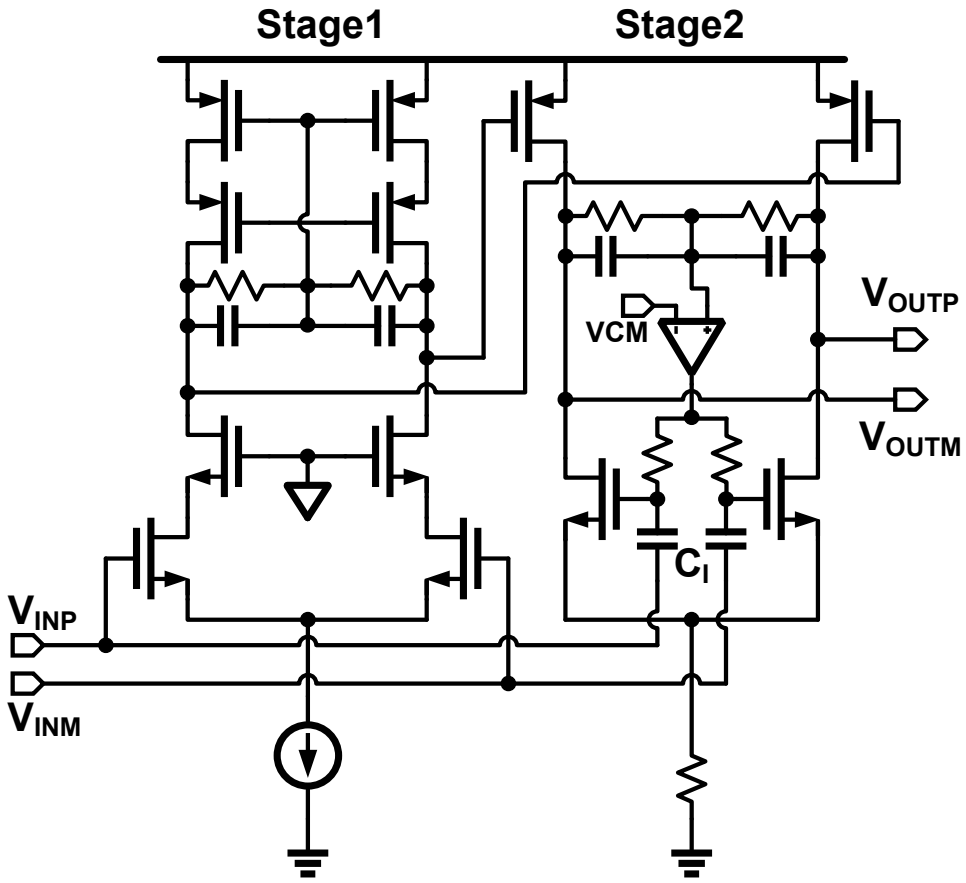

Figure 3.14: Opamp used in the loop filter integrator.

The first-order loop filter is realized using an active-RC integrator because it is

more linear compared to a $G_M - C$ topology and it provides a clean virtual ground, which eases the design of the feedback DAC. The amplifier in the integrator is implemented using 2-stage fully-differential amplifier shown in Fig. 3.14. Feed-forward compensation conserves the gain bandwidth product of the opamp and minimizes the excess loop delay caused by the integrator [19]. Because the input common-mode voltage is constant, a telescopic cascode amplifier is used in the first stage and the second stage is implemented with a common source amplifier. Two separate common feedback circuits are used to establish the output common mode voltage of the both the stages independently. A self biased common mode feedback circuit is used in the first stage and an explicit common-mode amplifier is used in the second stage. The feed-forward path from the input to the second stage is implemented by the AC coupling capacitor C_I. The simulated magnitude and phase response of the opamp is shown in Fig. 3.15. The amplifier consumes 2mA current and achieves a DC gain and an unity gain bandwidth of 58dB and 2GHz, respectively.

3.4.3 Four-bit Flash Quantizer (ADC_F)

The schematic of the 4-bit flash quantizer (ADC_F) used in the first stage of the residue canceling quantizer is shown in Fig. 3.16. It consists of 16 comparators whose reference voltages are provided by the resistor ladder. The comparator is implemented using a cascade of a pre-amplifier and a sense amplifier flip flop [20]. The pre-amplifier incorporates a double differential input stage to subtract the reference voltage from the differential input voltage and a low impedance diode

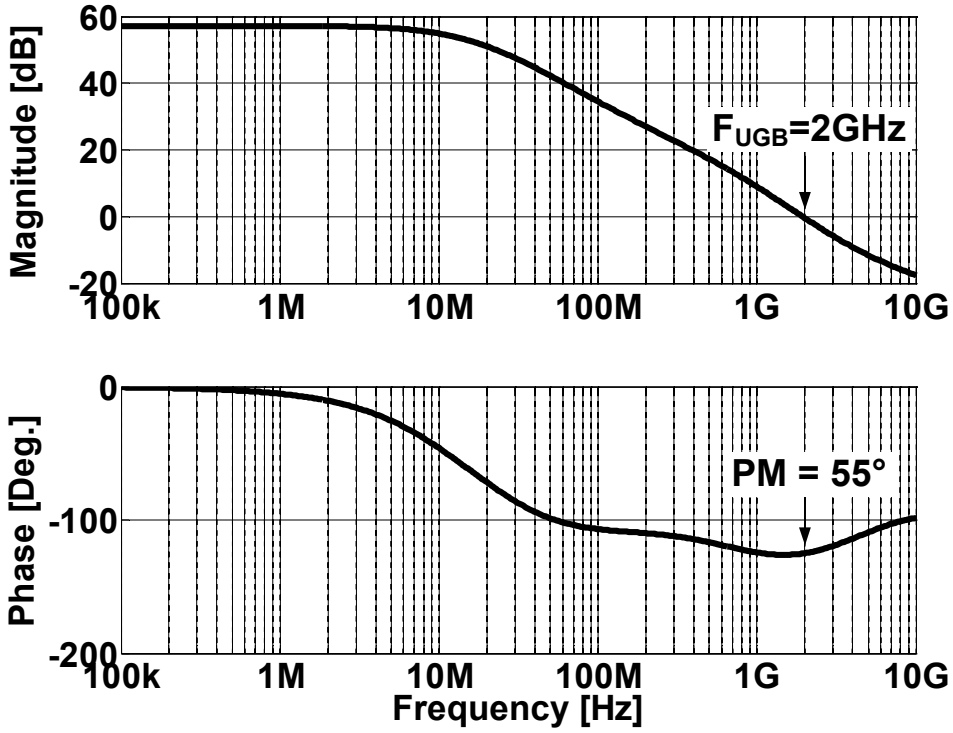

Figure 3.15: Simulated magnitude and phase response of the opamp.

load to isolate the quantizer input from kick back of the sense amplifier flip-flop.

3.4.4 Digital to Analog Converters (DAC_M and DAC_F)

The two DACs in the modulator, DAC_M in the main feedback path and DAC_F in the first stage of the residue canceling quantizer, are implemented using a non-return-to-zero (NRZ) topology. As opposed to a return-to-zero topology, an NRZ DAC is less sensitive to clock jitter but is more susceptible to inter-symbol interference (ISI). Current steering architecture is used to achieve fast switching and reduce the distortion caused by ISI.

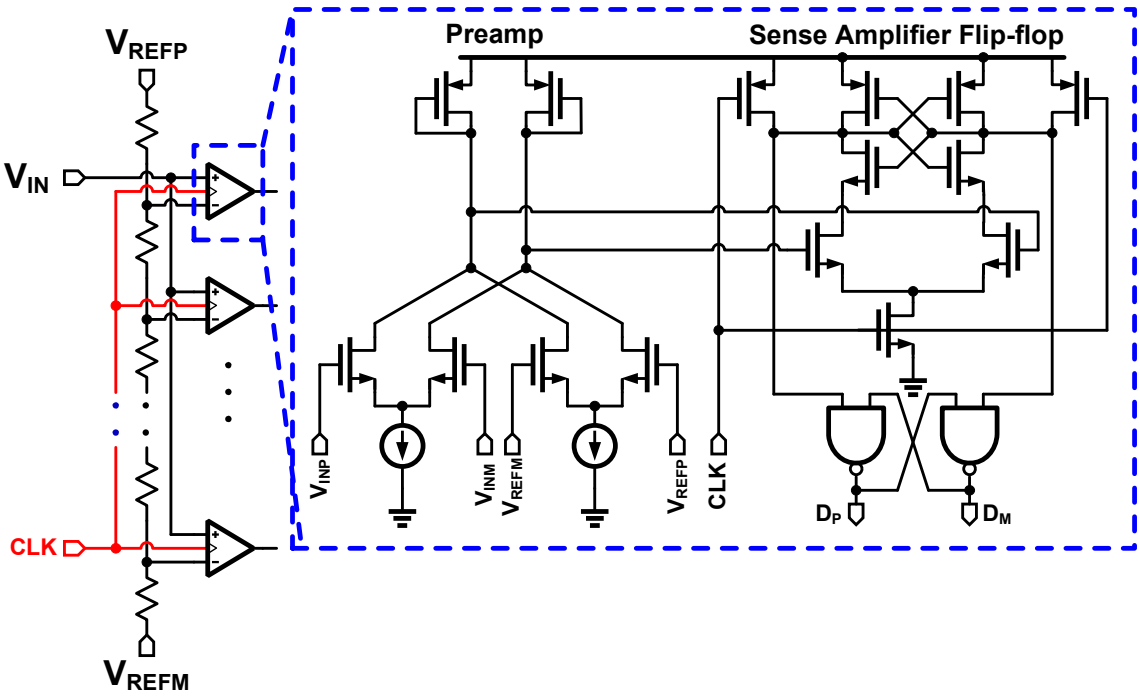

Figure 3.16: 16-level flash ADC_F.

Both DAC_M and DAC_F are thermometer coded. DAC_M has 62 unit elements, of which 30 cells are controlled by the VCO quantizer outputs. The rest are controlled by the $H_M(z)$ filter. The schematic of the unit cell used in DAC_M is shown in Fig. 3.17. The nMOS current is steered into the virtual ground node of the loopfilter integrator using switches, M_S. The current source was cascoded to increase output impedance and isolate it from glitches at the virtual node. Further, voltage glitch at the drain of the cascode transistor is minimized by using digital input signals with high cross over point. Cross coupled NOR gate latches followed by inverters are used to generate the high cross over point signals. To minimize the noise contribution, the DAC_M current sources were designed with a

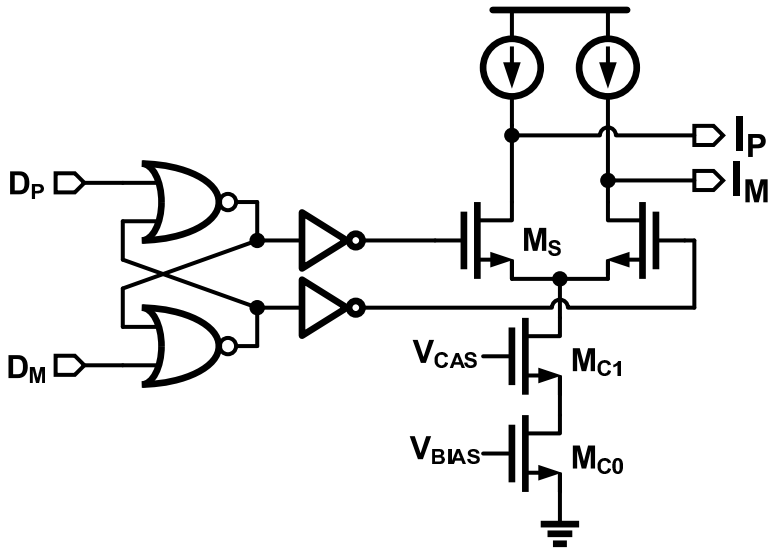

Figure 3.17: Unit current cell of DAC_M.

large overdrive voltage. Large dimension transistors were used to achieve better than 9-bit matching in the DAC. Cascoded pMOS current sources maintain the common mode current of the DAC to be equal to zero. The DAC_F has 16 unit elements and the schematic of one unit cell is shown in Fig. 3.18. Due to the first order noise shaping of the DAC_F errors by the loop filter, its requirements are relaxed when compared to DAC_M. Hence, simple level-triggered sampling using pass transistors was implemented to minimize power consumption. Both NMOS and PMOS current sources were switched to reduce power dissipation.

3.5 Measurement results

The prototype IC was fabricated in a 90 nm CMOS process and occupies an active area of $0.36mm^2$. The die microphotograph of the chip is shown in Fig. 3.19. The

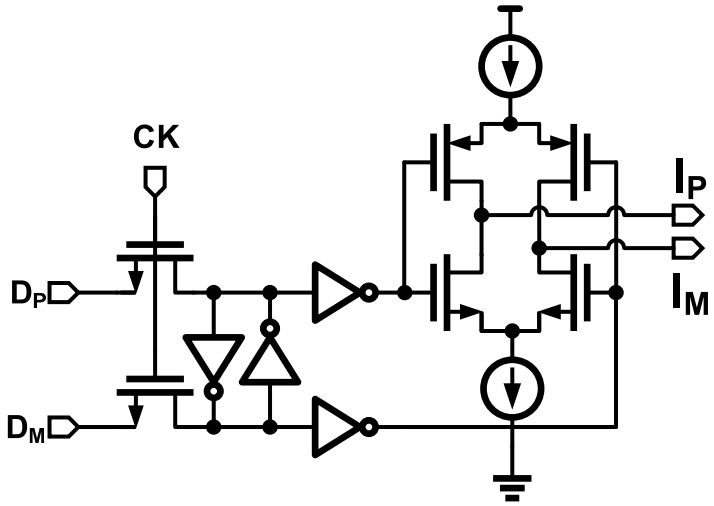

Figure 3.18: Unit current cell of DAC_F.

die was packaged in a 56-pin QFN package. At 600 MHz sampling rate, modulator consumes 16 mW of which 6.5 mW is consumed by the analog blocks and 9.5 mW by the digital blocks. Though the power consumption of individual blocks could not be measured, simulations have shown that the loop-filter opamp consumes about 2.8 mW and the two DACs consume 3.2 mW. Among the digital blocks, the flash ADC and the VCO consume 1.3 mW and 1 mW, respectively. The analog and digital blocks operate with a 1.4 V and 1 V supply voltages, respectively The full scale range of the ADC is 1.4 V_{p-p} and a common mode voltage of 0.6 V was used.

Figure 3.20 shows the measured ADC output spectrum for an -2 dBFS input tone at 500 kHz at a sampling frequency of 600 MHz. It illustrates that the modulator achieves second order noise shaping using only a first order loop filter. The measured SNDR over a 10 MHz bandwidth is 78.3 dB. An excellent SFDR

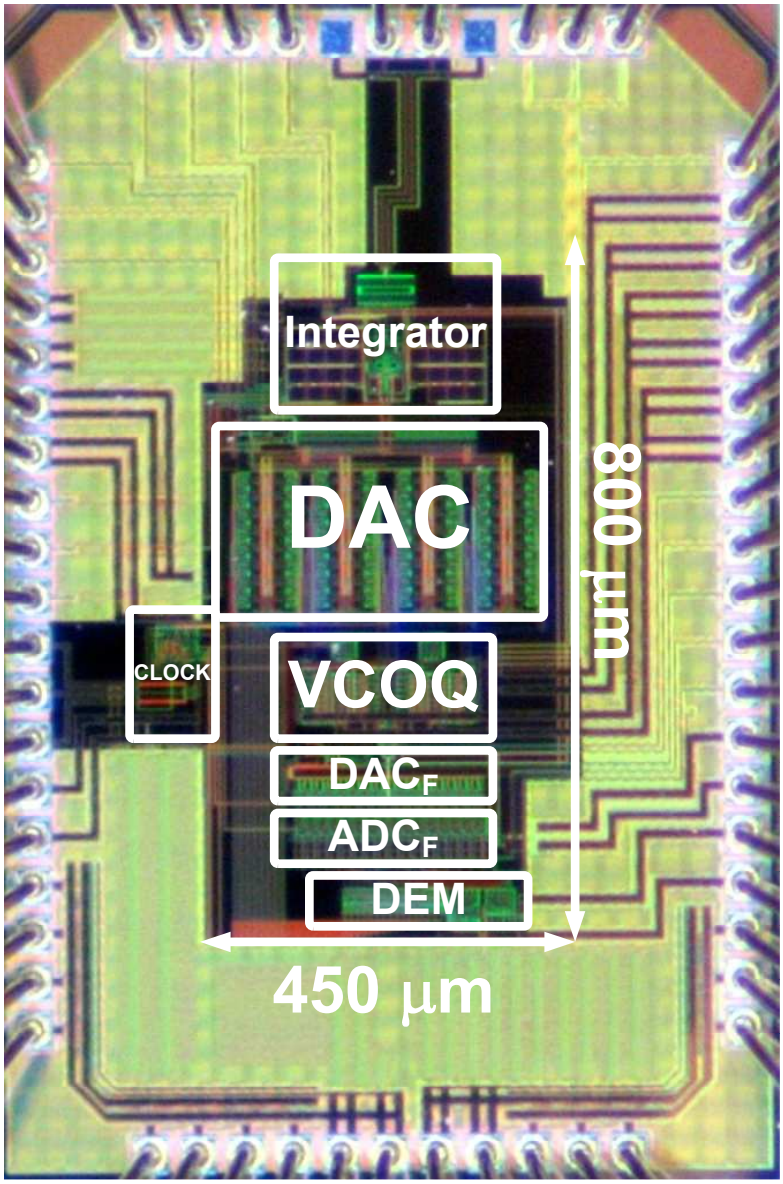

Figure 3.19: Die microphotograph of the prototype.

of 88.5 dB validates the claim that the proposed architecture is robust to VCO non-linearity. The spectrum of the ADC_F and VCO quantizer outputs are plotted in Fig. 3.21. It shows that the VCO quantizer processes mostly the quantization

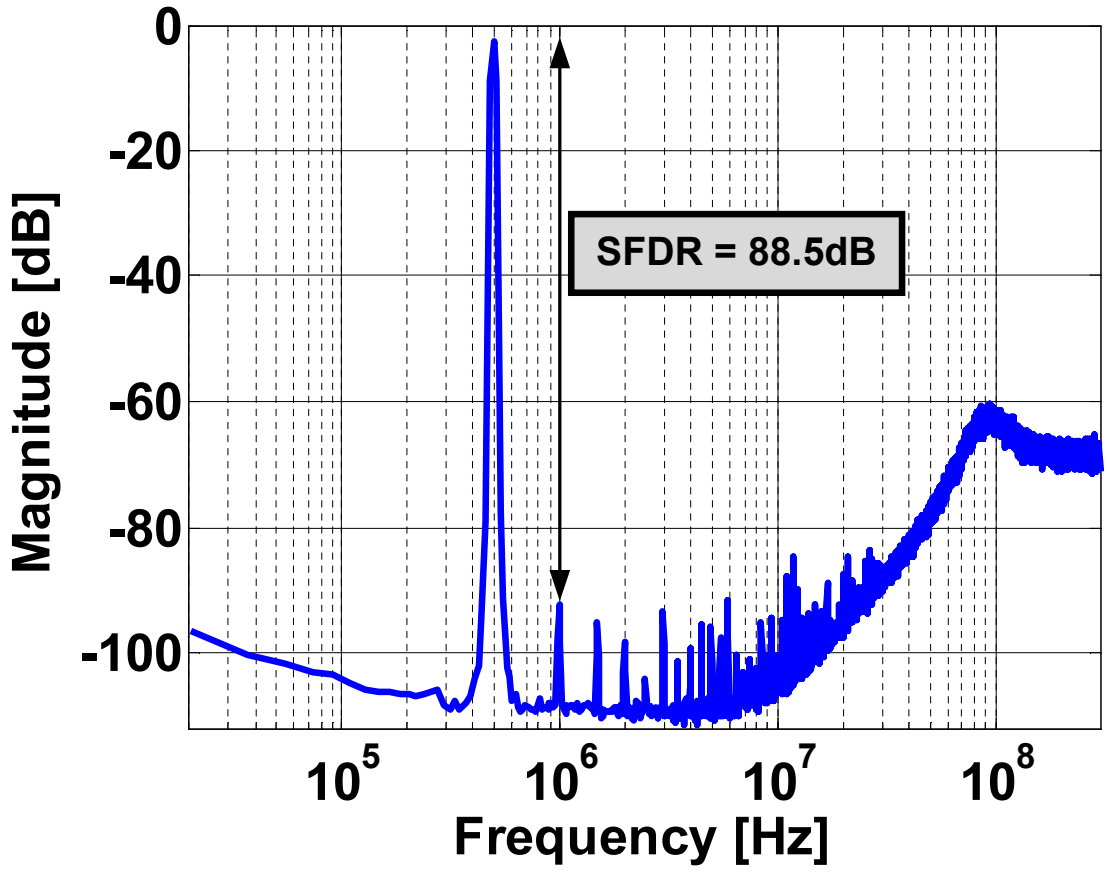

Figure 3.20: Measured modulator output spectrum (16 times averaged, 32768 FFT).

noise from ADC_F which contains very little input signal. Inband two tone test was also performed, and the intermodulation tones were measured to be greater than 80 dB. Figure 3.22 plots the spectrum of a two tone test for inputs of 500 KHz and 2 MHz. The measured SNR and SNDR are plotted for various input amplitudes in Fig 3.23(a) for a 100 kHz input tone. The peak SNR is 83 dB and the modulator achieves a dynamic range of 83.5 dB. The SNDR curves for various input

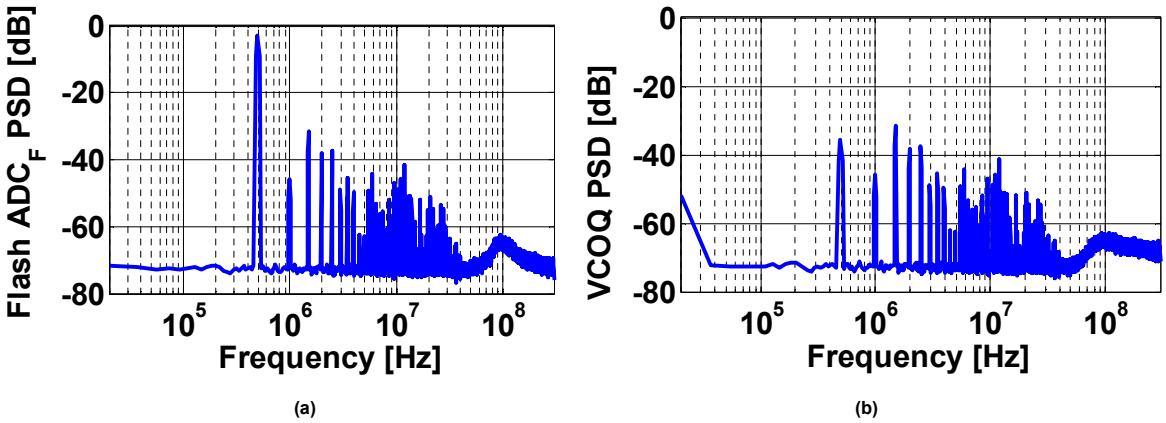

Figure 3.21: Measured spectrum of (a) ADC_F and (b) VCOQ.

frequencies near the full scale amplitude are plotted in Fig. 3.23(b).

The performance of the ADC is summarized in Table 3.1. The proposed ADC achieves a figure of merit (FoM) of 120 fJ/conversion-step for a 100 kHz input tone and 145 fJ/conversion-step for 1 MHz tone, which is an improvement of nearly a factor of 2 over the state of the art VCO based ADCs [12], [8], [21].

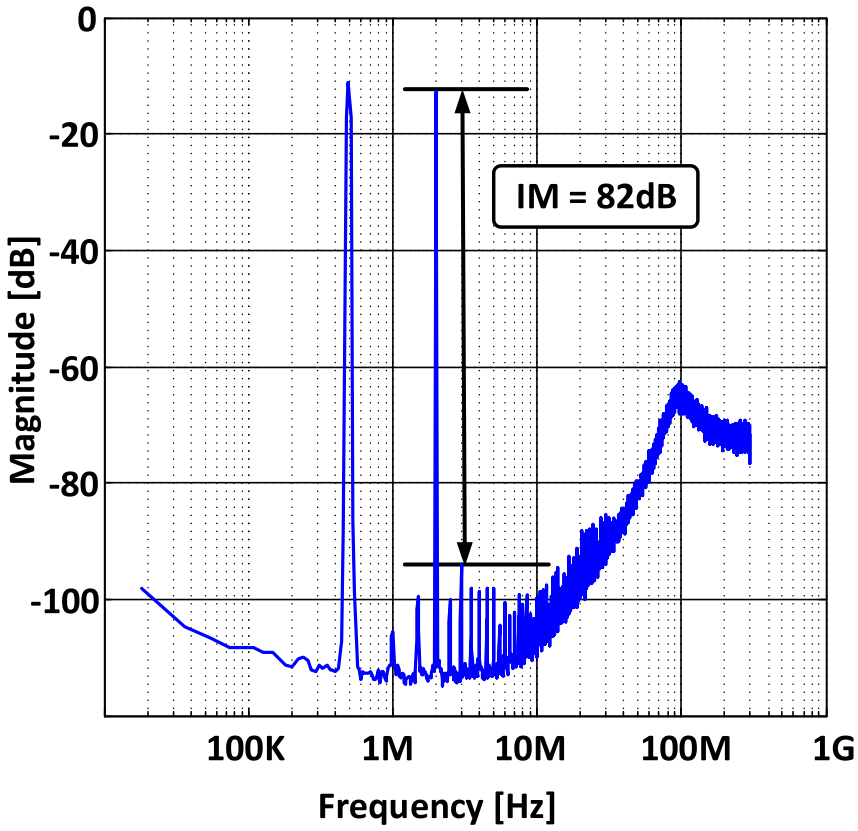

Figure 3.22: Two tone test on the modulator.

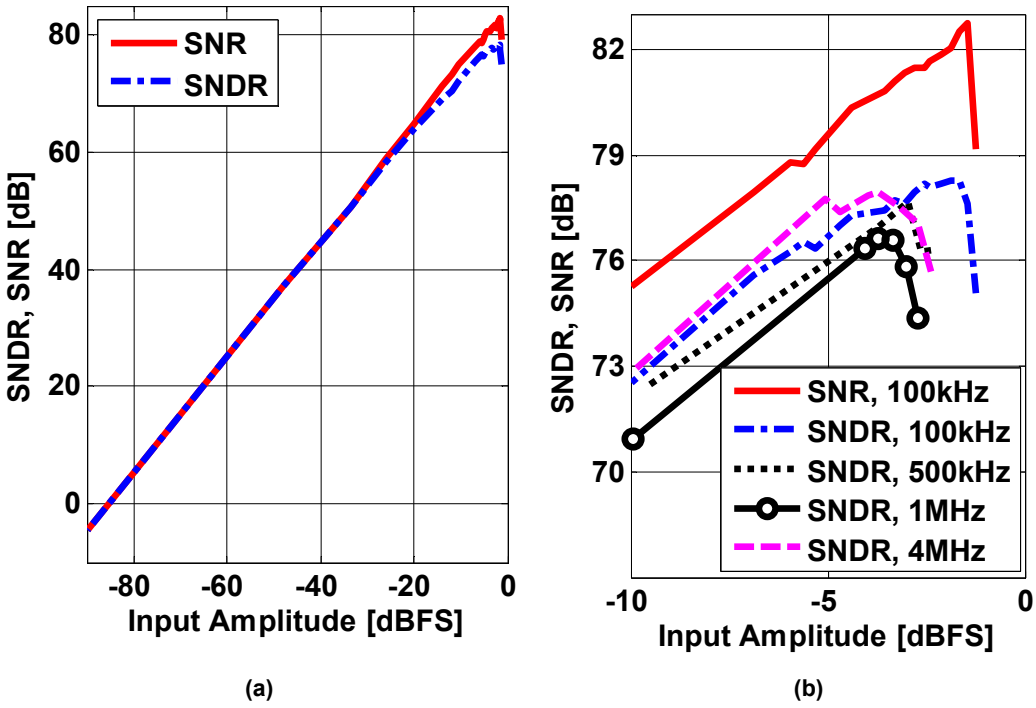

Figure 3.23: (a) SNR vs input amplitude for a 100 kHz sinusoidal tone, and (b) SNDR curves for 100 KHz, 500 KHz, 1 MHz and 4 MHz sinusoidal tones near fullscale amplitude.

Table 3.1: Performance summary and comparison with prior works.

	This Work			[8]	[12]	[21]	[16]	[17]
Technology	90nm			65nm	0.13μm	0.13μm	0.13μm	0.18μm
Area (mm^2)	0.36			0.07	0.42	0.45	0.15	0.7
Fs (MHz)	600			1152	950	900	640	640
Power (mW)	16			17	40	87	20	100
BW (MHz)	10			9	10	20	20	10
F_{IN} (MHz)	0.1	1	4	1	1	2	2.4	2.4
SNR (dB)	83	80.5	79.1	76	86	81.2	76	84
SNDR (dB)	78.3	76.6	78	73	72.4	78.1	74	82
ENOB (bits)	12.7	12.4	12.6	11.8	11.7	12.7	12	13.2
FOM (fJ/conv-step)	120	145	125	258	587	331	122	485

CHAPTER 4

CONTINUOUS-TIME $\Delta\Sigma$ MODULATOR USING PHASE-FREQUENCY FEEDBACK TECHNIQUE

With the advent of mobile technology standards such as 4G, LTE and LTE-A, there is an imminent need for ADCs with signal bandwidth of 20MHz and above. Designing a $\Delta\Sigma$ modulator with an RCQ quantizer at such frequencies might be challenging. Firstly, the loopfilter should be second order or more, and would require excess loop delay compensation circuit. Secondly, implementing residue cancelling operation in the multiple feedback DACs, required for higher order loop-filter and for compensation, would result in large area and power penalty and also complex digital routing. This chapter presents a new architecture which proposes to use both phase and frequency information of the VCO to target high sampling frequencies, for achieving high resolution and bandwidths.

4.1 VCO as a Phase quantizer

The frequency model of the VCO quantizer is again shown in Figure 4.1. It could

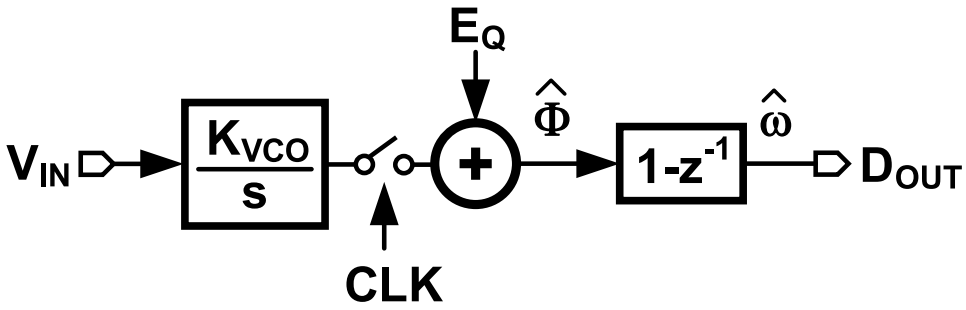

Figure 4.1: Frequency domain model of a VCO quantizer.

be observed that while the desired output is the quantized frequency variable, phase information is also available in the digital domain. All the prior architectures discussed until now have used the frequency domain variable as the desired output, as it is proportional to the input voltage. It was shown in [21] that it is also possible to use the quantized phase variable as the desired output. Since the VCO integrator has very high gain in the signal bandwidth (assuming K_{VCO} is large enough), meaningful extraction of phase information is possible by feeding back the phase to the input of the VCO using a DAC as shown in Figure 4.2. Here, the VCO acts as the loopfilter providing first order noise shaping for the quantization error. Moreover, the high gain of the VCO restricts its input voltage swing to a small fraction of input signal range, thus overcoming the nonlinearity issue of the VCO.

To this end, a prototype modulator was demonstrated to achieve 13 bit ENOB

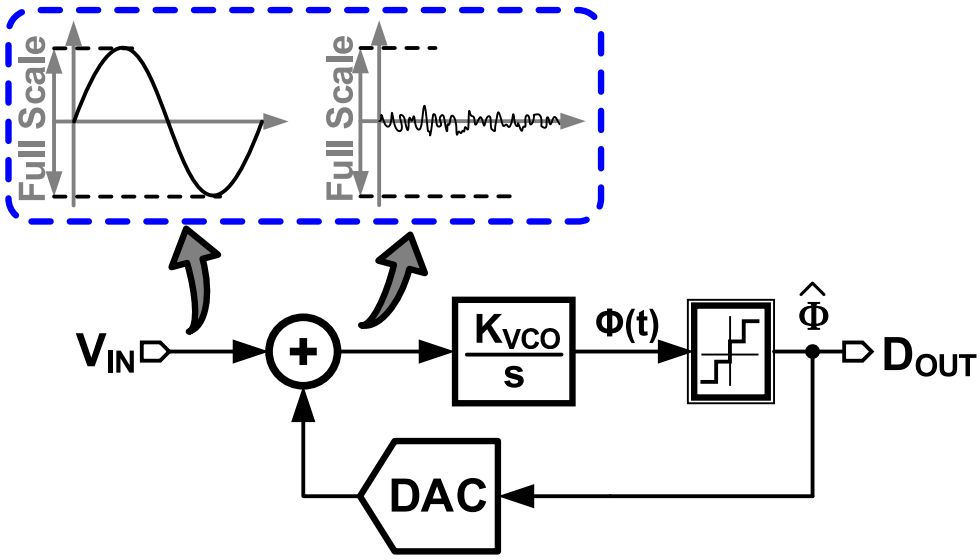

Figure 4.2: VCO as a phase quantizer.

at 20MHz signal bandwidth, and is shown in Figure 4.3. To provide high resolution, a third order loopfilter precedes the VCO and provides additional noise shaping. Due to the inaccessibility of the analog phase variable, $\phi(t)$, the modulator is realised using cascade of integrators with a feedforward and feedback loopfilter (CIFF-FB). The direct feedback path around the quantizer, required to compensate for excess loop delay, is accomplished by differentiating the output before feeding to the VCO. A return-to-zero DAC is used to restrict the impulse response of the path to one clock period.

Mismatch among the DAC unit cells will degrade the performance of the modulator and hence an explicit dynamic element matching (DEM) circuit is required in the phase feedback path to noise shape the mismatch. The differentiation in the compensation path is implemented using XOR gates. It is known that this

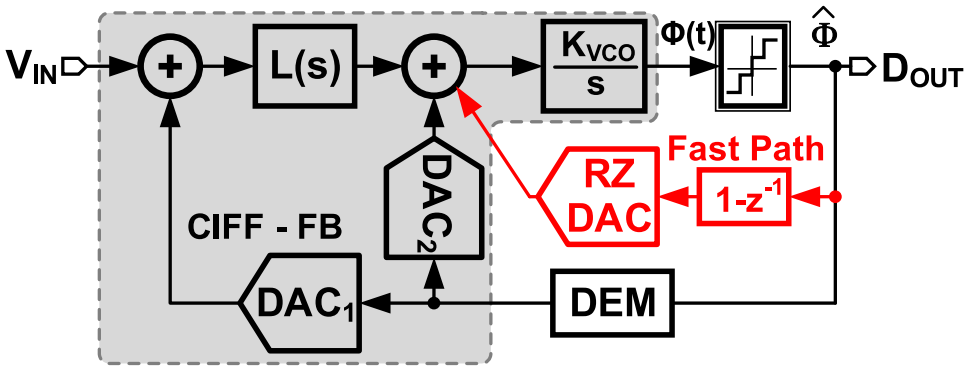

Figure 4.3: Prototype ΔΣ modulator with VCO as internal phase quantizer.

operation results in a thermometer code which is first order data weighed averaged in nature [12], hence there is no need for an explicit DEM in that path.

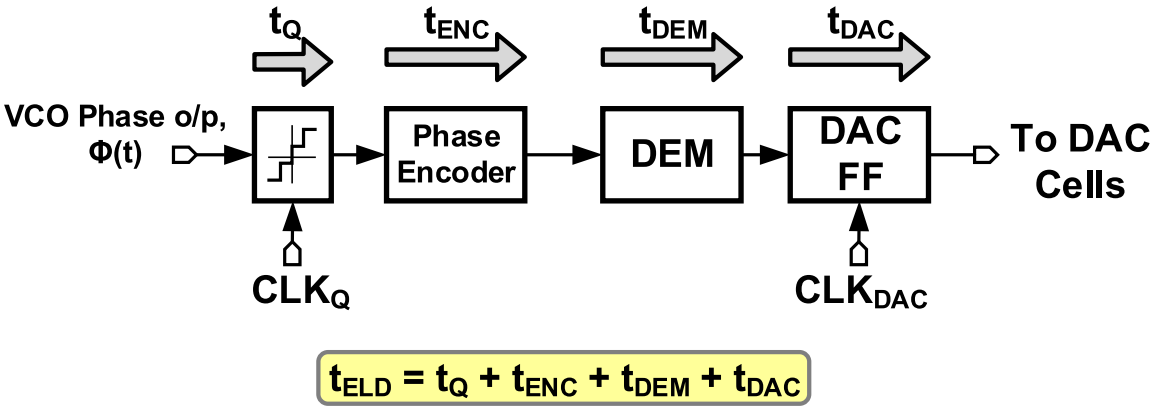

Figure 4.4: Blocks contibuting Excess loop delay in continous time ΔΣ Modulators with VCO based phase quantizer.

While the modulator was able to demonstrate a remarkable performance, the excess loop delay in the feedback path acts as a stumbling block for high sampling frequencies. Figure 4.4 shows the blocks in the path that contributes to the excess loop delay. It consists of the phase sampler, the phase encoder, DEM circuit and

the retiming flip-flops in the DAC. Typically, a sense amplifier based flip-flop is used as a phase sampler. The time taken for the output of the flip-flop to resolve into binary bits is called as the clock-to-q propagation delay (t_Q). The phase encoder seperates the signal dependent phase content from the free running phase of the VCO and encodes it to thermometer code. It consists of one or more levels of combination logic gate and their delay is denoted by t_{ENC}. The most common architecture for the DEM circuit is the log shifter, which consists of $\log_2(N)$ gate levels for N level input thermometer code. The propagation delay through the DEM, t_{DEM}, is a significant fraction of excess loop delay. The delay through the DAC flip-flop is a combination of setup time and the clock-to-q propagation delay, (t_{DAC}). The excess loop delay is then given by:

$$t_{ELD} = t_q + t_{ENC} + t_{DEM} + t_{DAC} \tag{4.1}$$

The next section investigates the impact of excess loop delay and how it determines the maximum sampling frequency for a Continuous-time $\Delta\Sigma$ modulator.

4.2 Impact of Excess Loop Delay on the stability of the Modulator

Ideally, CT $\Delta\Sigma$ modulators can be compensated for excess loop delays upto one clock period by having a fast loop DAC around the quantizer [22], [23],[24]. It is worth mentioning at this point that a method for compensating delays greater

than one clock period has been proposed in [25]. However, it comes at the cost of reduced SQNR. Hence, the focus of this discussion will be limited to excess loop delays less than one clock period. In practice, the ability to compensate for delays upto the entire range of one clock period does not hold true when the analog intensive circuits have parasitic poles comparable to Fs. The following analysis lends support to this argument.

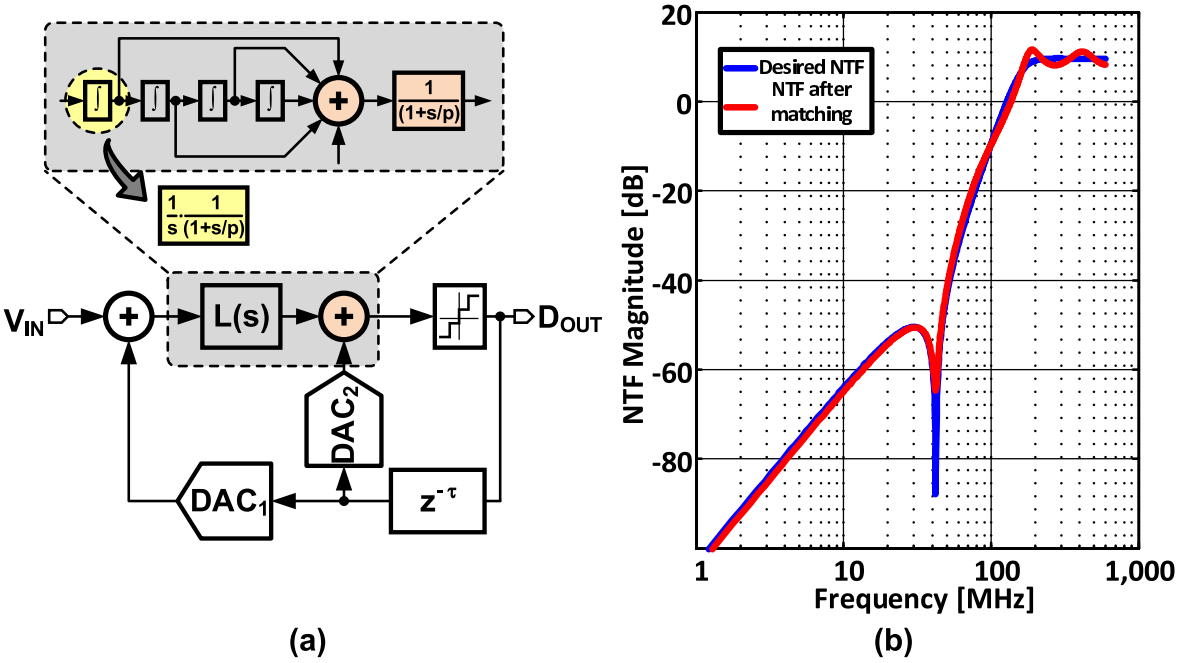

Figure 4.5: (a) Conventional $\Delta\Sigma$ modulator with parasitic poles in the analog circuits, (b) Desired NTF and NTF of the real modulator after matching for p=F_s and $\tau = 0.5$

Figure 4.5(a) shows a block diagram of a conventional 4^{th} order modulator with a FLASH quantizer, and the loopfilter is a cascade of integrators with feedforward (CIFF) structure. The transfer function of the integrators in the loopfilter is given

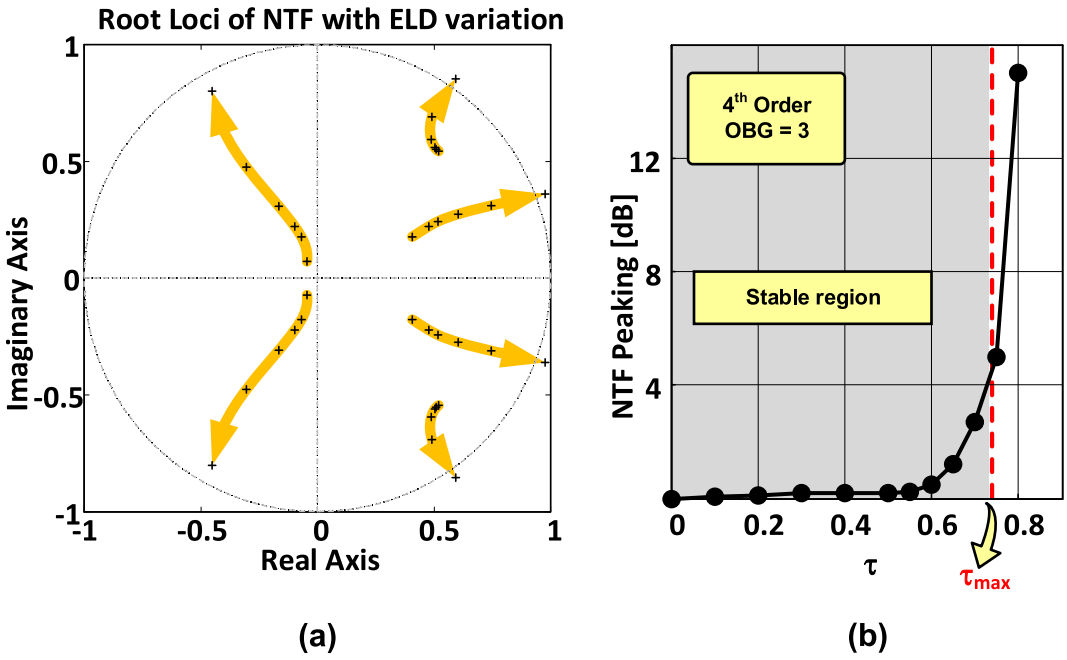

Figure 4.6: (a) Root Loci of the NTF with varying τ, (b) Peaking in the NTF of the modulator plotted as a function of τ

by $\frac{1}{s}\frac{1}{(1+\frac{s}{p})}$, where p is the parasitic pole due to the finite bandwidth of the opamp (assuming that active opamp-RC integrators are used). For simplicity, in this analaysis, the same parasitic pole is considered for the summing amplifier too. DAC_2 is a NRZ DAC which compensates for excess loop delay and the digital backend is modeled as a delay block, and τ is the ratio of the excess loop delay, (t_{DEM}), to the sampling period, T_s. The sampling frequency could be assumed to be 1 without any loss of generality.

Using the design centering technique of [26], the gain coefficients of each integrator and the DAC_2 are found by matching its impulse response with that of an ideal loopfilter using the LMS algorithm. It has been observed that the extent to

which the real NTF could match the ideal NTF reduces with increase in τ, and this can be quantified by the peaking in the NTF. A value of 3 has been chosen for the out of band gain for the ideal NTF as it optimizes inband noise in presence of clock jitter [27]. Figure 4.5(b) shows one such instance where p=F_s and τ of 0.5. Figure 4.6(a) plots the root loci of the NTF for various values of τ and the modulator becomes unstable when the poles cross the unit circle. Figure 4.6(b) plots the peaking as a function of the τ. From the above analysis, it is evident that it is not possible to compensate for delays of upto entire range of one clock period.

The above analysis could also be performed for modulators employing VCO based ADCs. As shown in Figure 4.3, the architecture has a combination of cascade of feedfoward and feedback (CIFF-FB) loopfilter, with the VCO phase integrator acting as the farthest integrator in the loopfilter. Since the compensating DAC feeds to the input of the VCO, it is preceded by a digital differentiation and is implemented as a return-to-zero(RZ) DAC. The peaking in the NTF was again determined for various values of τ and is plotted in Figure 4.7.

4.2.1 Upper limit on the sampling frequency

Two observations could be made from the plots of Figure 4.5(b) and 4.7. Firstly, as the excess loop delay (ELD) increases, the peaking in the NTF also increases, and the stability of the NTF deteriorates at high ELD; and two, the stability worsens at a faster rate for larger values of ELD. Intuitively, it can be explained that the parasitic poles add additional phase shift in the loop, which can be approximated

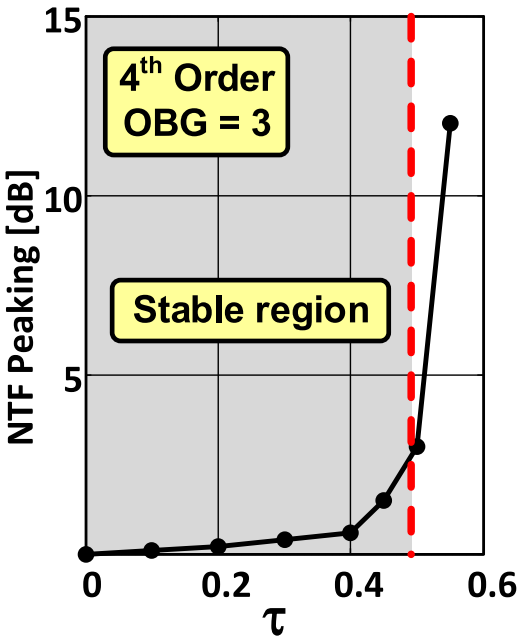

Figure 4.7: Peaking in the NTF of the modulator with VCO based ADC, plotted as a function of τ

as additional delays in the signal chain. This results in the *effective* loop delay to approach one, even though the actual digital loop delay is still less than one clock period.

Consequently, from the plots of Figure 4.5(a) and 4.7, for a given excess loop delay, t_{ELD}, there is a maximum sampling frequency at which the NTF is reasonably stable and is also less sensitive to the variations in ELD. The maximum permissable sampling frequency, $F_{s,max}$ is then given by

$$F_{s,max} = \frac{\tau_{max}}{t_{ELD}} \tag{4.2}$$

where, τ_{max} is value of ELD at which the NTF peaking reaches a threshold, say

3 dB. From the above equation, it is evident that the means to increase the sampling frequency is to either tolerate larger peaking in the NTF or to decrease the excess loop delay in the system. The first choice is not preferred as it inadvertently affects the stability of the system. The next section addresses excess loop delay and proposes a new architecture which introduces a faster parallel path that circumvents the existing phase feedback feepath, and allows the modulator to be clocked at more than one GHz sampling frequency.

4.3 Proposed Phase-Frequency architecture

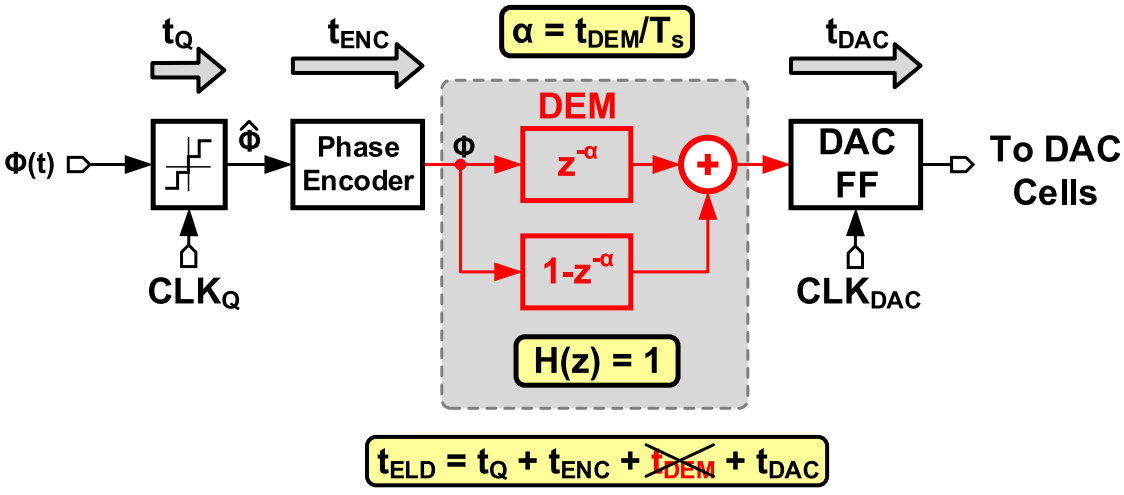

Figure 4.8: Proposed modification to the feedback path to reduce dependence of excess loop delay on the DEM.

Figure 4.8 shows the proposed phase-frequency feedback path. A second path is introduced parallel to the DEM with the intention of removing the dependence of the excess loop delay on the propagation delay of the DEM, t_{DEM}. Ideally, if

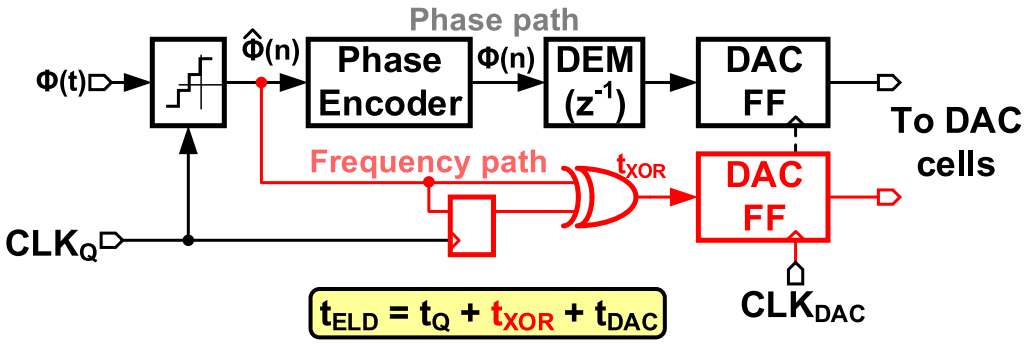

Figure 4.9: Practical implementation of the Phase-Frequency feedback.

the second path has a transfer function of $\left(1 - z^{-\left[\frac{t_{DEM}}{T_s}\right]}\right)$, then the delay from the output of the phase encoder to the input of the DAC is zero (for the moment, the second path is assumed to be delay free). The excess loop delay is now given by,

$$t_{ELD} = t_Q + t_{ENC} + t_{DAC} \tag{4.3}$$

If a delay of one clock period is allocated to the DEM circuit, the second path performs a simple first order differentiation, $(1 - z^{-1})$ on the phase input to give a frequency output, henceforth, this path will be referred to as frequency path. A practical implementation of this phase-frequency feedback path is shown in Figure 4.9. If the oscillating frequency of the VCO is restricted to $F_s/2$, the frequency encoder could be implemented with a register and an XOR gate. This implementation is known to produce an implicit data weighed averaged thermometer code. To avoid delays caused due to the adders, the codes from both the paths are added in the current domain.

In summary, the signal in the feedback path is split into phase and frequency

information, wherein the frequency path permits an additional delay of upto one clock period in the phase path for it to perform its encoding and the DEM operation. The excess loop delay of this implementation is

$$t_{ELD} = t_Q + t_{XOR} + t_{DAC} \tag{4.4}$$

where t_{XOR} is the delay of the XOR in the frequency encoder. When compared to the delay expression of Equation (4.1), the proposed technique reduces the excess loop delay by almost t_{DEM} (assuming that t_{ENC} and t_{XOR} are of similar order). The new sampling rate of the modulator, $F_{s,\phi-f}$ can be shown to be,

$$F_{s,\phi-f} \approx F_s\Big(1 + \frac{t_{DEM}}{t_Q + t_{XOR} + t_{DAC}}\Big) \tag{4.5}$$

where F_s is the sampling frequency of the conventional modulator. For a 65nm CMOS process and four bit quantizer, transistor level simulations have shown that the multiplication factor in the above equation is close to 1.3. The next few sections discusses the implementation of a prototype modulator utilizing the phase-frequency feedback technique.

4.4 Prototype $\Delta\Sigma$ Modulator

Figure 4.10 shows the block diagram of the CT $\Delta\Sigma$ modulator with the proposed phase-frequency feedback technique. The modulator was targeted to achieve more than 12 bit ENOB at 50MHz signal bandwidth. The oversampling ratio (OSR),

order and the number of bits was determined from behavioral simulation and is tabulated in Table 4.1. To optimize the inband quantization noise, the null in the NTF was placed at 42MHz. The NTF of the modulator is plotted in Figure 4.11. The values of the gain coefficients obtained after design centering are tabulated in Table 4.2. The excess loop delay was set as to half clock delay for the outer DAC and DAC_2. The return-to-zero DAC was clocked with a quarter clock delay.

Table 4.1: Specification for the Modulator

NTF Specs	Value
OSR	12
Order	4
OBG	3
Quantizer bits	4
F_s	1.2 GHz

Table 4.2: Gain Coefficients of the Loopfilter

Coefficient	Value
k_0	3.1
k_1	2.8
k_2	1.6
k_3	0.7
k_4	0.125
g	0.05

The schematic diagram of the modulator is shown in Figure 4.12. The loopfilter is implemented using opamp RC integrators. The capacitors are digitally trimmable with 3 bit binary word. The weighted summation of the outputs of the

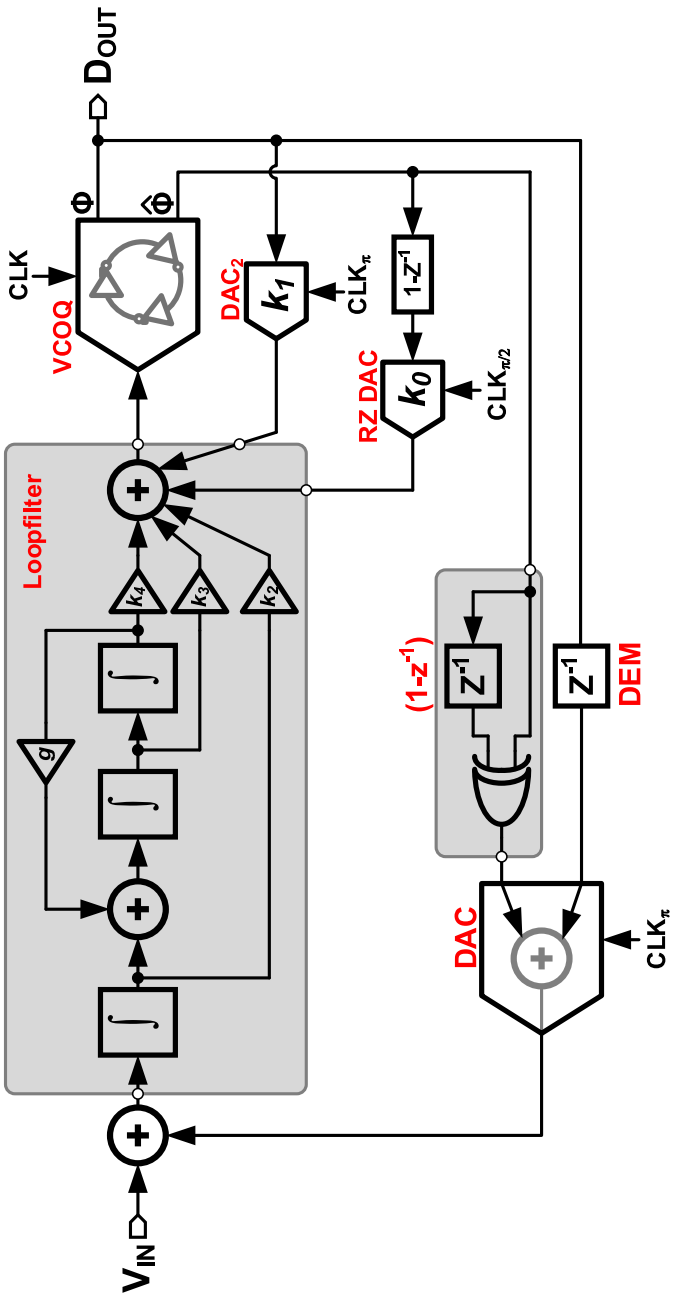

Figure 4.10: Proposed $\Delta\Sigma$ Modulator with Phase-Feedback mechanism.

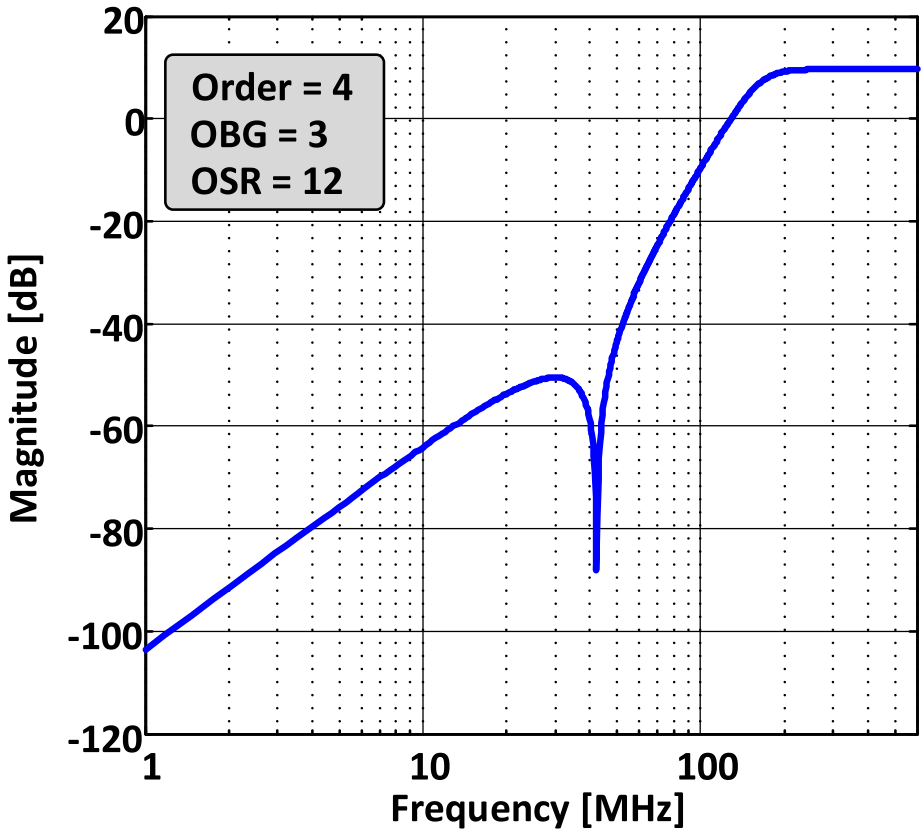

Figure 4.11: Noise transfer function of the modulator

integrators and the innerloop DAC currents is implemented with a resistor feedback amplifier. The feedback resistor is also programmable with three bit binary word to adjust for variations in the VCO's gain. The voltage controlled oscillator is implemented with a 16 stage delay cells. The differential outputs of the adder controls the VCO's frequency, with the positive and negative outputs of the adder controling the supply and ground of the VCO respectively.

The output phase of the VCO is sampled using a sense amplifier flip-flop (SA-FF). The SA-FF outputs are fed to the frequency and the phase encoder. The

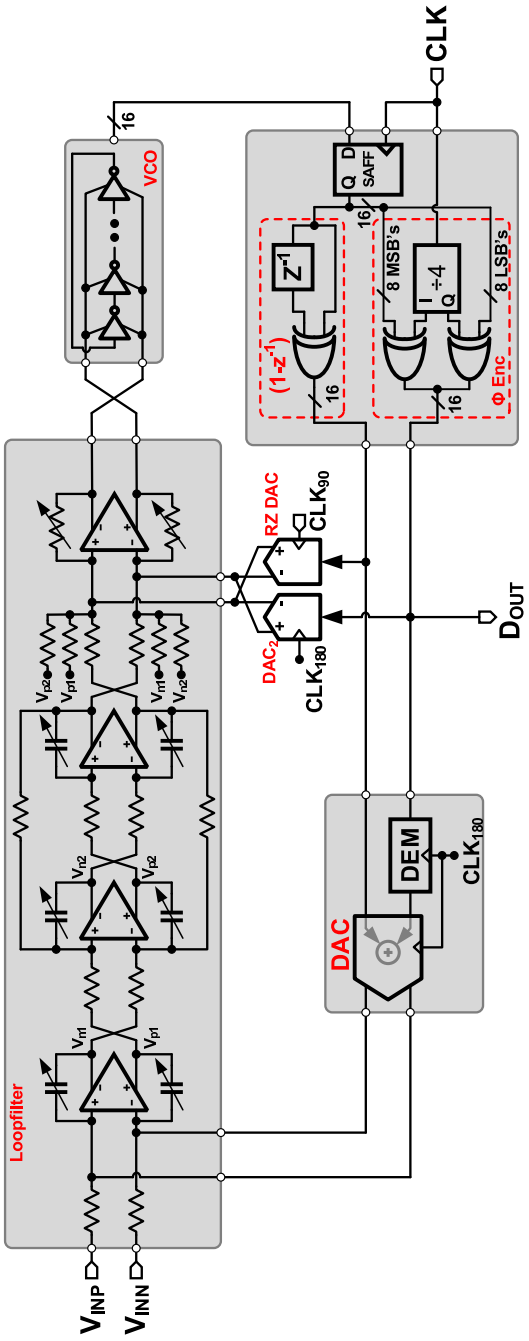

Figure 4.12: Schematic diagram of the Modulator.

frequency encoder implements the first order difference equation using a register and an XOR gate. The output code is a 16 bit DWA code. The VCO's free running frequency is chosen to be $F_s/4$, so that the oscillating frequency range is within Fs/2.The sampling frequency is divided by four in the phase encoder and is used to subtract the free running phase using the XOR gate. The output code resembles a thermometer code, which is fed to a four stage log shifter in the DEM block. The DEM is clocked with a half clock period delay to accomodate the delays in the SA-FF and the phase encoder.

An ELD of 0.5 is selected and hence the outer loop DAC and inner loop DAC, DAC_2 are also clocked at half clock delay. This provides one clock period for the DEM alone, relaxing its delay constraints. The return-to-zero DAC is clocked at quarter clock delay to offer a faster compensating loop.

4.5 Schematic Design

This section presents some of the circuit design details of the key building blocks.

4.5.1 Adder and VCO

Previous implementations of a VCO involved a transconductance stage controlling the current in a inverter based ring oscillator (Figure 3.11, [12], [28]). One side effect of this implementation is that, a parasitic pole is formed at the control node and the location of this pole is very close to the oscillating frequency. In this case, since the oscillating frequency is $F_s/4$, stabilizing the loop for such low

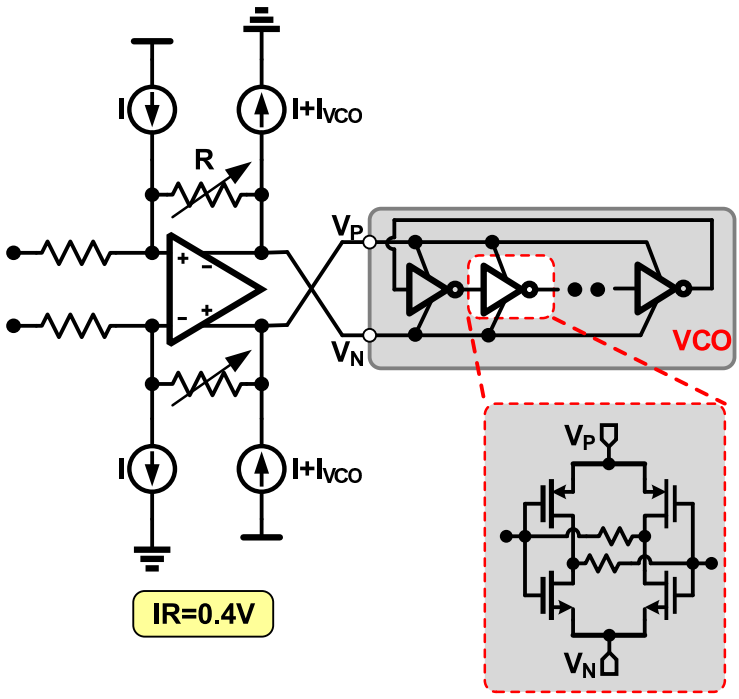

Figure 4.13: Schematic of the Adder and VCO

parasitic pole is very challenging. Though methods for compensating the control node pole have been suggested by the same author [13], it has been found to be still inadequate at such high sampling frequencies.

Figure 4.13 shows the implementation of the VCO and the adder in the loop-filter. The VCO acts as the load for the adder, thereby, the opamp in the adder absorbs the control node pole of the VCO as part of its intrinsic parasitic pole. The positive and negative outputs of the adder controls the supply and the ground of the VCO. The VCO is implemented with pseudo differential inverter cells which are resistively coupled to ensure phase alignment [29]. Under dc operating conditions, the positive and the negative outputs of the adder are 1.25 and 0.45 respectively

for the VCO to oscillate at $F_s/4$. These voltages are derived by pumping a current through the feedback resistor. The VCO's nominal current, I_{VCO} is also provided by current sources connected at the output of the adder.

Opamps

The schematic of the opamp used in the integrator and the adder is shown in Figure 4.14(a) and (b) respectively. A two stage amplifier with feedforward compensation, similar to the opamp in the earlier RCQ modulator was implemented for the integrator opamps. An additional modified miller compensation scheme was implemented for the adder opamp to compensate for the excess phase shift caused by the feedback resistor and the input capacitance of the adder. The voltage supply for the integrator and the adder opamps are 1.5V and 1.8V, respectively.

4.5.2 DAC

Nonreturn-to-zero(NRZ) DACs suffer from distortion due to mismatch induced signal dependent intersymbol interference (ISI) [1]. This is more pronounced when they are controlled by DEM circuits. Figure 4.15(a) shows the schematic of a unit cell of the NRZ DAC. Capacitor, C_0, is the parasitic capacitor at the drain node, V_C of the cascode transistor. Any mismatch between the input pair transistors in the first integrator opamp would result in an voltage offset, ΔV, at the DAC output. When the DAC cell switches the current from one output to the other, the drain node voltage swing is proportional to the offset voltage. During this process, the capacitor dumps a charge, Q_0 proportional to the voltage swing in the form of

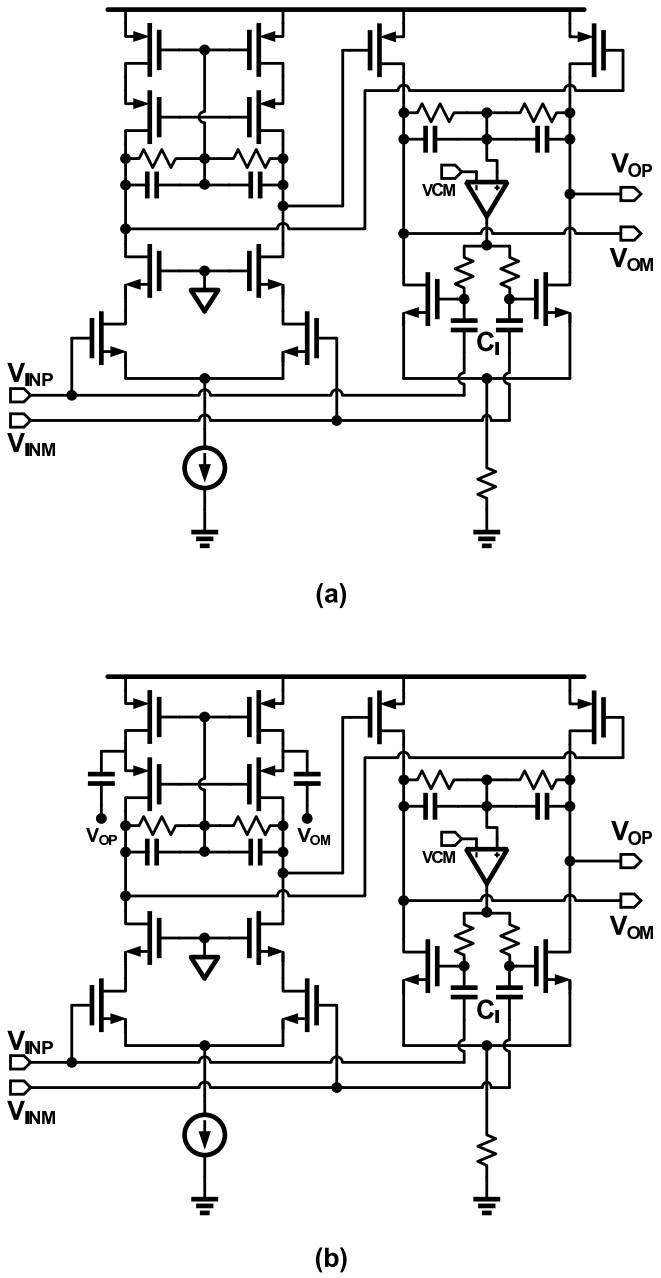

Figure 4.14: (a) Opamps used in the integrators, and (b) Opamp used in the adder.

an impulsive current as shown in Figure 4.15(b). Similarly, V_{th} mismatch between the transistor M_0 and M_1 would also cause identical impulsive current.

Since each DAC cell injects this current into the system only when the input bit flips, the total impulsive current from the DAC is proportional to the transition density of DAC input. For a DWA pattern, this transition density is a nonlinear function of its input signal as shown in Figure 4.15(c) [30]. For inputs code upto half scale, the transition density increases linearly. Beyond that, they decrease linearly with the input, making it an overall nonlinear function. This causes distortion in the DAC and affects the overall performance of the $\Delta\Sigma$ modulator. Simulation results for an offset of 10 mV and V_{th} variation of 10 mV is shown in Figure 4.19. A stand alone NRZ DAC is fed by a DWA output of an ideal modulator. The DAC output is filtered before taking the FFT to capture all the transient characteristics. The NRZ DAC is found to have an SFDR of 76dB, whereas an ideal DAC has a noise floor well below 100dB.

The solution to the problem lies in making the transition density to be independent of the input signal. This makes Return-to-zero DAC (RZ DAC) an ideal candidate as all the DAC current units in a RZ DAC transit at every clock edge, and hence have a constant transition density. This means all the DAC cells transfer charge to the system at every clock edge. But return-to-zero DAC are very sensitive to clock jitter, and hence a dual return-to-zero DAC (DRZ) structure acts a compromise between performance and power dissipation.

A power efficient dual return-to-zero (DRZ-I) structure discussed in [1] is shown in Figure 4.16. Here two RZ DACs are clocked at with a half clock delay and

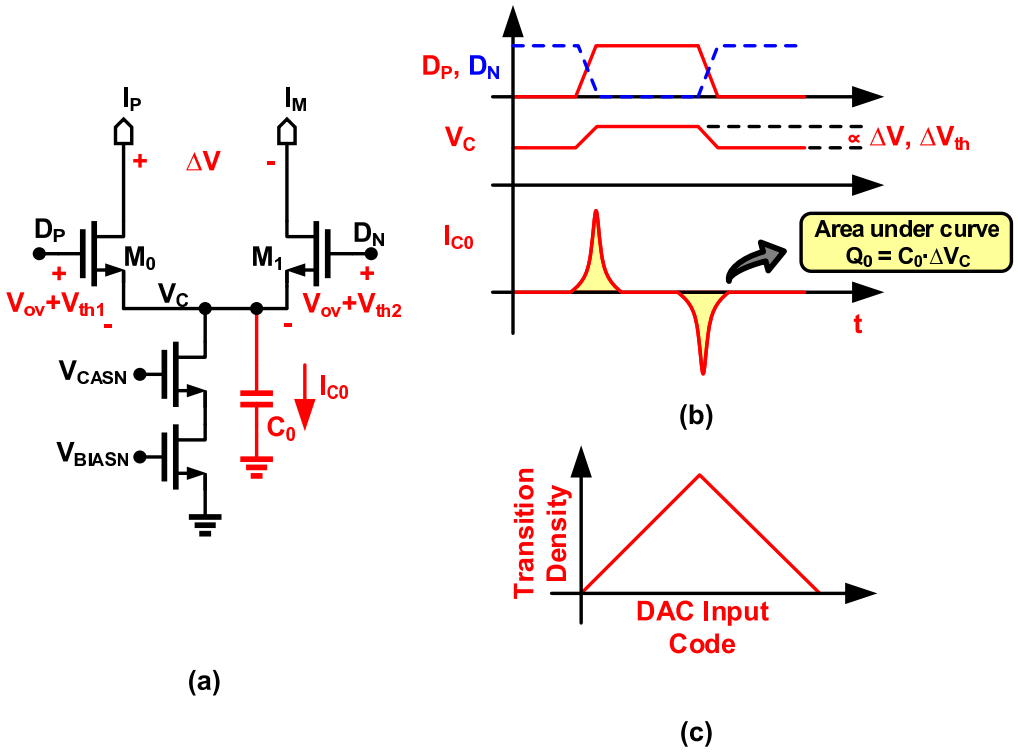

Figure 4.15: (a) Nonreturn-to-Zero DAC current cell, (b) Impulsive current through the capacitor during switching in presence of mismatches in the system, and (c) Transition density of a NRZ DAC with DEM bit codes.

the output current resembles a NRZ DAC pulse (see Figure 4.17). $D_{P1,N1}$ are active when clock is high and $D_{P2,N2}$ are active when clock is low. This structure helps to solve the distortion problem due to transient rise and fall time mismatches [1]. Unfortunately, it does not eliminate the distortion arising due to the above mentioned nonidealities such as offset and the switching transistor V_{th} mismatches. Since the node V_C is common for both the RZ pulses, in the presence of ΔV offset, V_C swings only when the bits flip. Hence this scenario is similar to the NRZ DAC. But, it does lowers the distortion due to the V_{th} mismatches of the switching

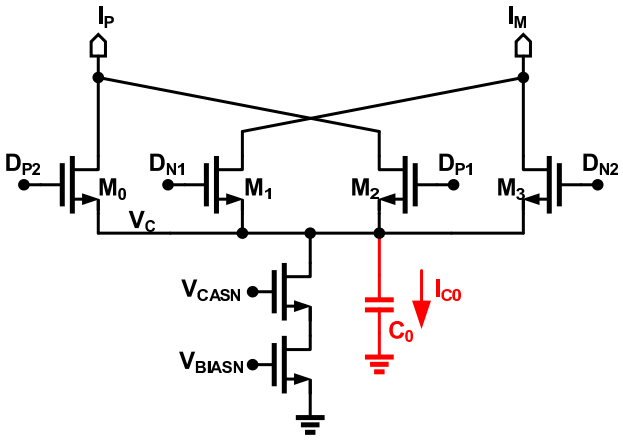

Figure 4.16: Unit cell of DRZ-I DAC analyzed in [1].

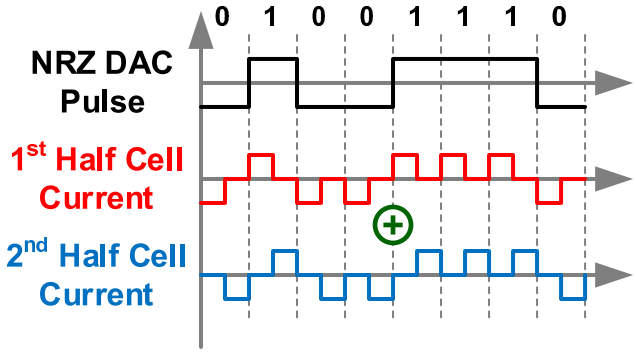

Figure 4.17: Dual return-to-zero DAC pulse.

transistor. When input bit is high, the two transistors M_2 and M_0 are used in the first and second half of the clock period respectively. It *effectively* averages the mismatches fo those two transistors and hence reduces the mismatch variation by a factor of 2. The simulations results under same conditions of offset and V_{th} mismatches as that of the NRZ DAC yields an SFDR of 83dB as expected.

A dual return-to-zero DAC (DRZ-II) cell proposed in [31] overcomes this problem and has been used in the outer loop DAC. The DAC cell is shown in Figure 4.18.

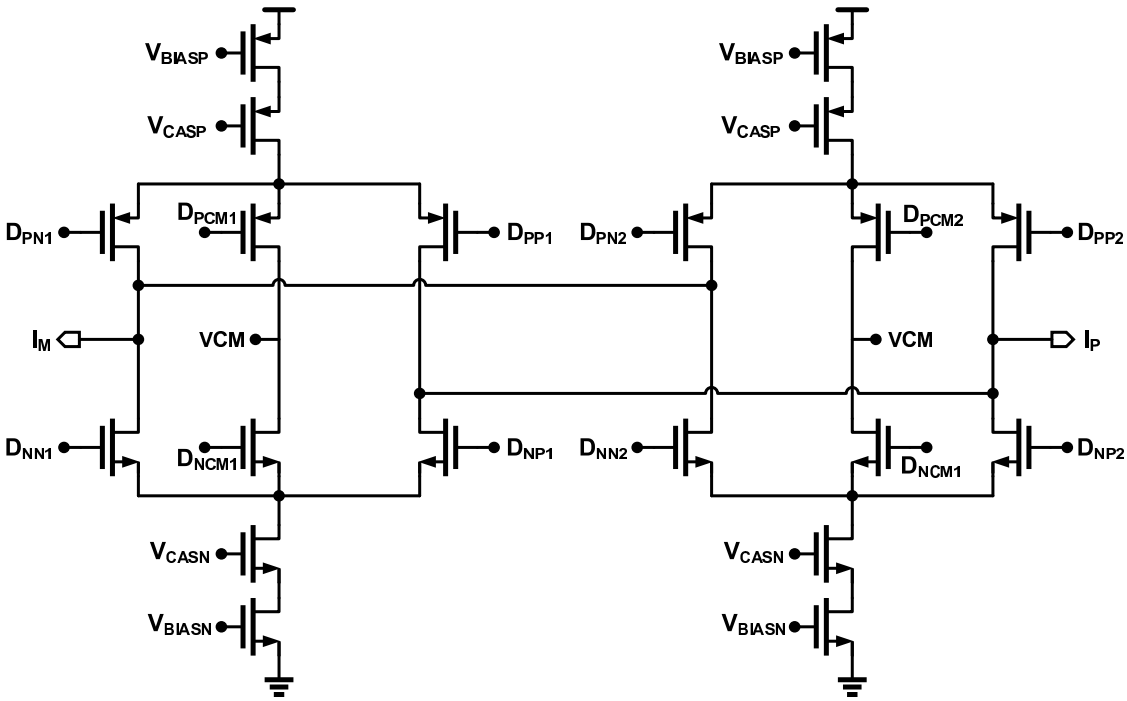

Figure 4.18: Unit cell of the Dual Return-to-Zero DAC (DRZ-II) implemented in the prototype.

It is has two physically seperated current sources which are switched at half clock period intervals and the outputs currents are then summed. In that sense, it is a fully time interleaved implementation of a return-to-zero DAC. With V_C being isolated between the two RZ DAC structures, it exactly mimicks the transient performance of a RZ DAC and also maintains the clock jitter properties of a NRZ DAC. Simulations show that it can achieve an SFDR of 92dB. Both the nMOS and pMOS current sources are switched to improve the power efficiency of the DAC and to lower the DAC noise.

Figure 4.19 shows the simulation results of the the stand-alone DACs whose

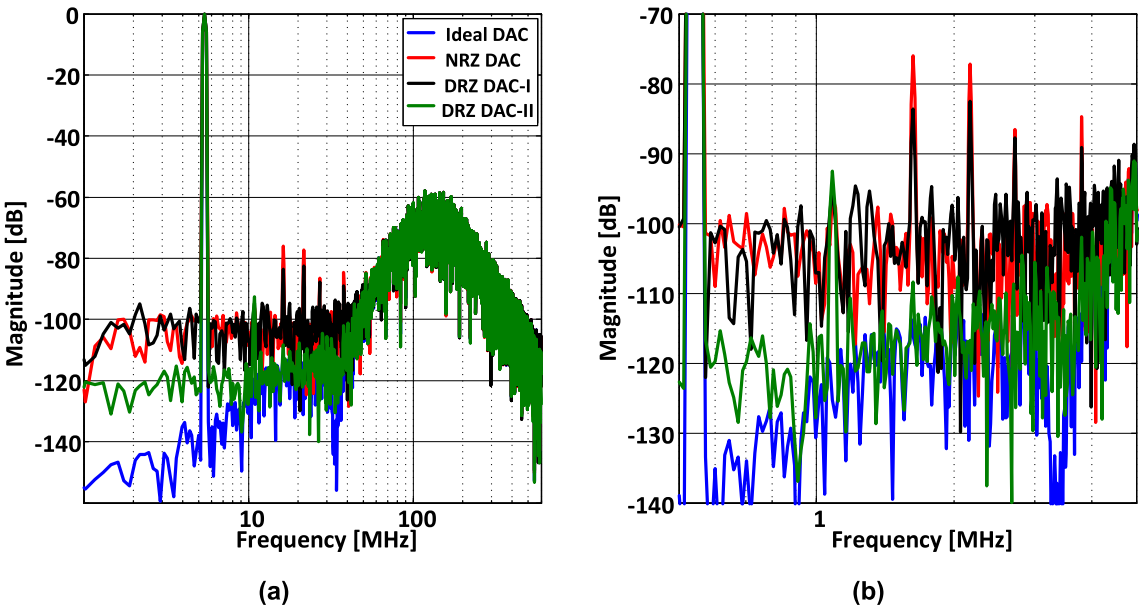

Figure 4.19: Simulated spectrum of an ideal DAC, NRZ DAC, DRZ DAC-I and DRZ-II DAC , and (b) Zoomed in plot of the spectrum.

input is a DWA bit pattern of an ideal $\Delta\Sigma$ modulator. The distortion of the three DACs, the NRZ, DRZ-I and the DRZ-II DACs are tabulated in Table 4.3.

Table 4.3: Comparison of distortion in various DAC architectures due to offset at the DAC output and V_{th} mismatch of the switching transistors

DAC Architecture	SFDR (dB)
Nonreturn-to-Zero DAC	76
Dual Return-to-Zero-I DAC	83
Dual Return-to-Zero-II DAC	92

The inner loop DAC_2 current cell was implemented similar to the schematic shown in Figure 3.18. The schematic of the compensating return-to-zero DAC is shown in Figure 4.20.

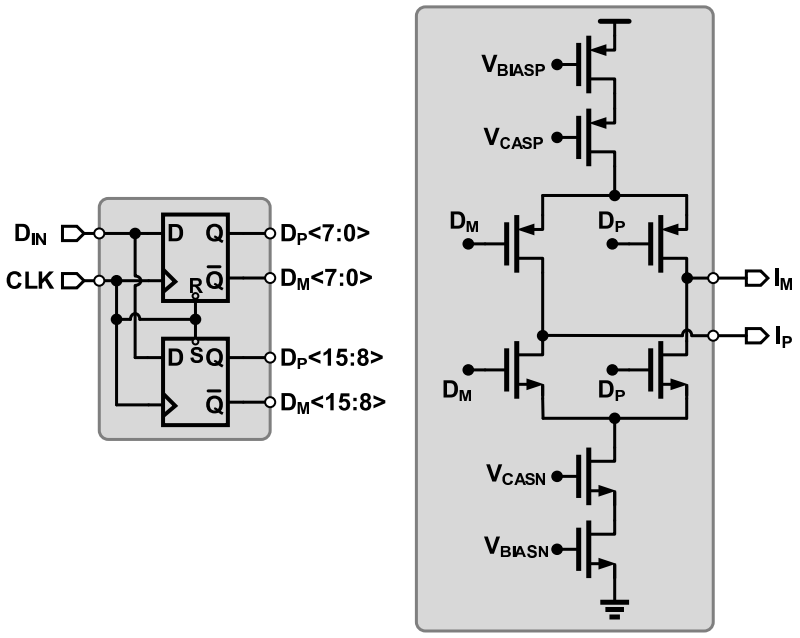

Figure 4.20: Unit cell of the Compensating Return-to-zero DAC current cell and the digital logic for all the 16 cells.

4.6 Simulation Results

A snapshot of the layout of the prototype modulator is shown in Figure 4.21. The prototype chip was designed in TSMC 65 nm CMOS process and will be fabricated shortly. The active area of the chip is 0.5 mm^2. The modulator is clocked at 1.2GHz and consumes 50 mW power. Of this, 28 mW is consumed by analog blocks and the rest by digital blocks. The power consumption of the loopfilter includes that of the VCO. The analog blocks operate at 1.5 V, except the adder opamp whcih operates at 1.8 V to support the voltage swing of the VCO. The digital supply is 1 V.

Figure 4.22 shows the 2 times averaged, 4096 point simulated result of the C+CC extracted modulator. A -3 dBFS sinusoidal signal at 3.5 MHz was the input and the measured SNDR in the signal bandwidth of 50 MHz was 76.7 dB, and the THD was observed to be more than 84dB. The simulation results are tabulated in Table 4.4. The modulator achieves a figure of merit (FoM) of 90 fJ/conv-step. For signal bandwidths of more than 20 MHz, this performance is at par with many conventional CT $\Delta\Sigma$ modulators.

Table 4.4: Performance summary.

Technology	65nm
Area (mm^2)	0.5
Fs (GHz)	1.2
Power (mW)	50
BW (MHz)	50
F_{IN} (MHz)	3
SNDR (dB)	76.7
ENOB (bits)	12.5
FOM (fJ/conv-step)	90

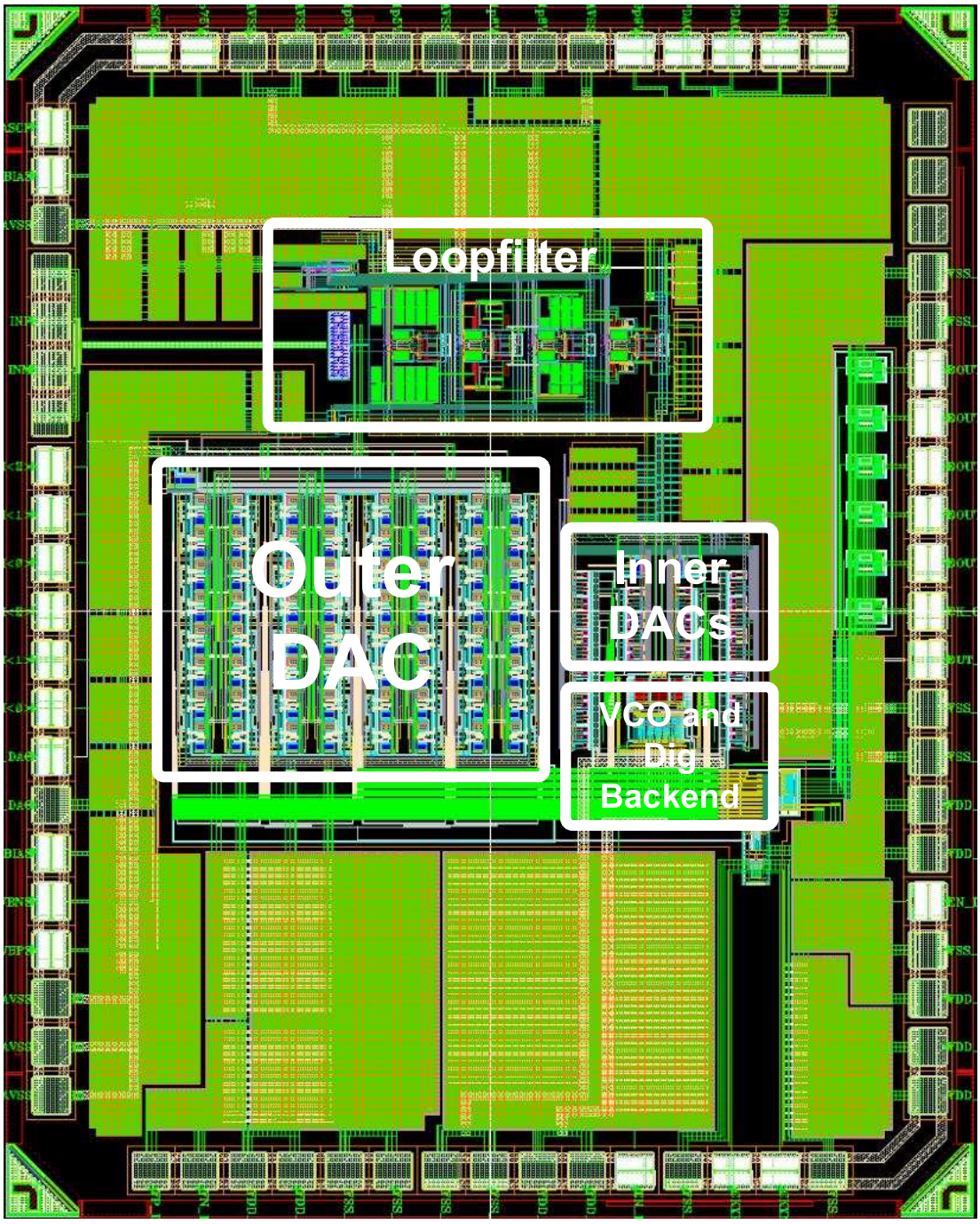

Figure 4.21: Snapshot of the layout.

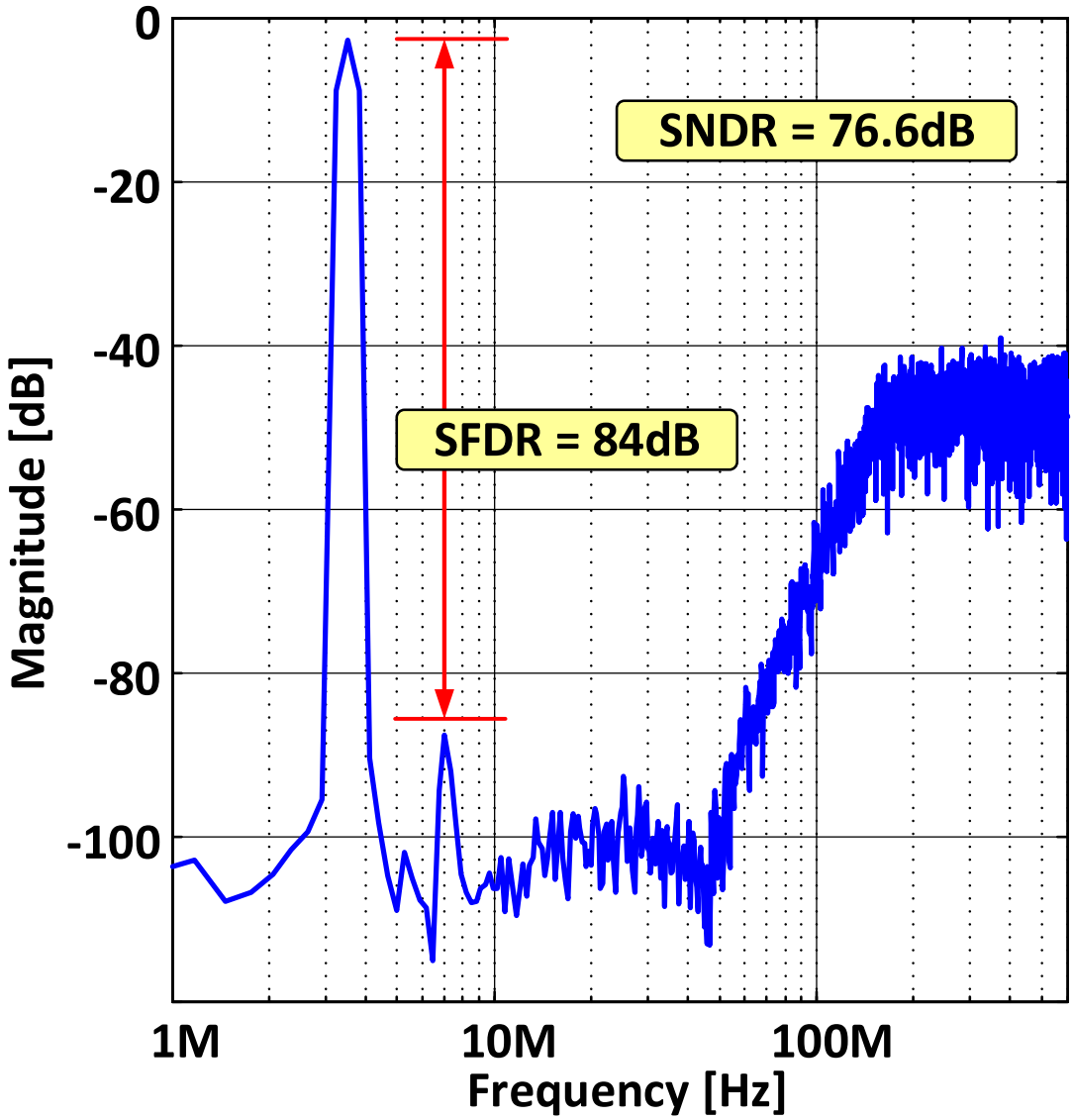

Figure 4.22: Simulated Output spectrum with a 3.5MHz input at -3dBFS (4096-point 2-time averaged with Hann window).

CHAPTER 5

CONCLUSION

VCO-based ADCs have many attractive features: (1) They achieve first order noise shaping in an open loop manner and so do not require analog integrators or a highly accurate feedback digital-to-analog converter (DAC) and (2) Because VCO-based ADCs are implemented using mostly digital circuits such as CMOS inverters and flip flops, they benefit from technology scaling. However their performance is severely limited by the non-linearity of the VCO's voltage-to-frequency tuning characteristic.

In the first part of this work, a continuous-time (CT) $\Sigma\Delta$ modulator using a VCO-based internal quantizer is presented. By incorporating the non-linear VCO as the second stage in a 2-stage residue canceling quantizer (RCQ), the input to the VCO spans only a small portion of the non-linear tuning curve, thus mitigating the impact of its non-linearity on the ADC performance. The order of noise shaping is increased by placing the RCQ in a continuous-time (CT) $\Sigma\Delta$ loop. Using only a first order loop filter, the proposed $\Delta\Sigma$ modulator achieves second order noise

shaping. Fabricated in a 90nm CMOS process, the prototype modulator occupies an active area of 0.36 mm^2 and consumes 16 mW power. It achieves a peak SNDR of 78.3 dB in 10 MHz bandwidth and an SFDR of better than 85 dB when clocked at 600 MHz. The figure of merit (FoM) of the modulator is 120 fJ/conv-step.

Continuous Time $\Delta\Sigma$ modulators with VCO based ADC as a phase quantizer suffer from their operating frequencies being limited due to excess loop delay. The excess loop delay appears to be further magnified in the presence of DEM circuits that might be required to noise shape the mismatches in the DAC current cells. The second part of this work presents an architecture which utilises both the phase and frequency information to overcome this issue. By feeding back, the frequency information along with phase information, the excess loop delay could be relaxed by one extra clock cycle period in the phase path. Transistor level simulations show that a prototype fourth order modulator could be operated at 1.2 GHz and achieve 76.7 dB SNDR in 50 MHz while consuming just 50 mW of power.

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