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Title OSCILLOSCOPE SAMPLING CONVERTER FOR OBSERVING NANOSECOND WAVEFORMS

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The sampling technique, as applied to oscillography, has made possible the displaying of very fast risetime repetitive electrical waveforms on a cathode ray tube face, with a minimum of associated high speed amplifying and display circuitry. The performance of a sampling mode instrument, with respect to minimum rise or fall time which may be displayed, is dependent mainly on the minimum width of a strobe pulse which opens a sampling gate and the speed of the sampling gate itself. The time width of the strobe or sampling pulse is effectively equal to the minimum signal rise time viewable, and the avalanche switching mode of an ordinary junction transistor provides a solid state source of nanosecond or even subnanosecond voltage steps which may be differentiated to form this narrow sampling pulse.

This thesis is the culmination of a project to

design and build a unit to convert an ordinary one megacycle oscilloscope to the sampling mode of operation using solid state elements only. Wherever possible, the circuitry and controls available on a conventional oscilloscope were used in an effort to make an inexpensive, yet effective instrument capable of monitering the nanosecond waveforms so prevalent in today's electronic laboratories.

OSCILLOSCOPE SAMPLING CONVERTER FOR OBSERVING NANOSECOND WAVEFORMS

by

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INTRODUCTION

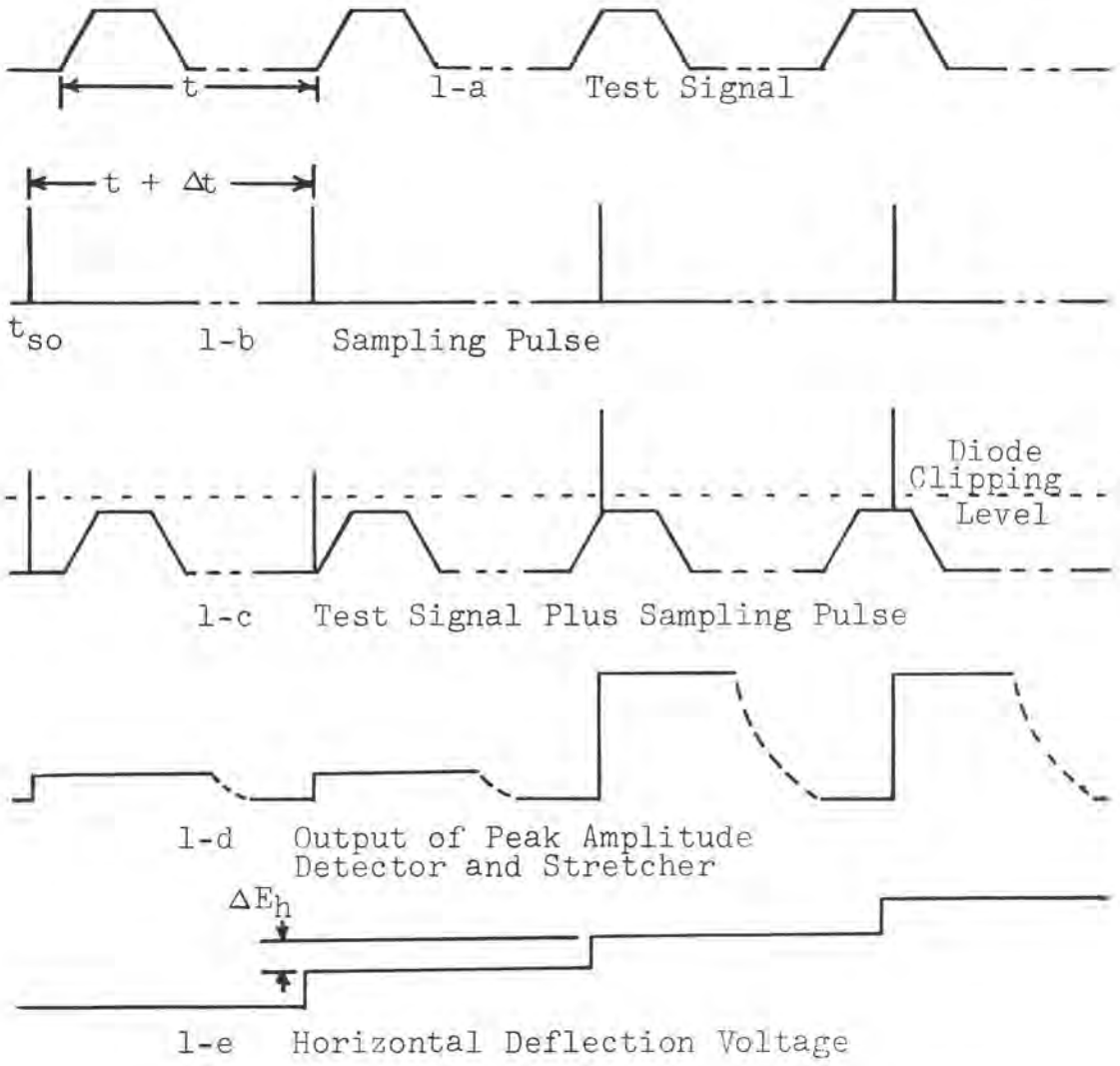
With the continued extension of the high frequency limits and the lowering of the rise times of electronic devices has come the need for laboratory oscilloscopes capable of evaluating the performance and characteristics of these devices and circuits using them. The high frequency applications of conventional oscilloscopes have been limited in several ways. These include basic cathode ray tube limitations, such as deflection sensitivity and the writing rate of phosphors, and bandwidth and speed requirements of the associated amplifying, sweep, and trigger circuits. These problems have been attacked from a variety of viewpoints (6, p. 218). They include increasing the speed of the display circuitry which is expensive and still limited in frequency, and new ideas and designs of the CRT itself, such as traveling wave types of deflection plates, which are severely limited in deflection sensitivity and also expensive. Another technique is frequency conversion via sampling methods and then displaying, at a lower frequency, a replica of the original waveform, thereby alleviating many of the speed requirements of the CRT and its display circuits (4, p. 815).

The use of the sampling method of increasing oscilloscope bandwidth is the topic of this thesis. Emphasis is placed on simplicity of operation and circuitry, and on building an inexpensive, effective attachment for converting a low frequency oscilloscope to the sampling mode of operation, thereby increasing its effective bandwidth by orders of magnitude. Perhaps the most stringent limitation of the sampling method is that it requires a repetitive waveform. The waveform is sampled but once each repetition and many samples are required to reconstruct the original waveform. Even with this limitation, the method has many applications since most waveforms encountered in laboratory test work are, or can be made to be repetitive.

THE CONCEPT OF SAMPLING OSCILLOGRAPHY

The sampling principle makes use of the repetitive nature of the majority of electrical signals found in a laboratory by extracting a small amount of information from each successive waveform and displaying this information in the proper position on the CRT face. In this manner, repeated sampling of a waveform may be used to reconstruct a replica of the original waveform. Basically, this method is a frequency division, or time stretching, of fast signals in order that they may be displayed on oscilloscope equipment which otherwise would be incapable of handling these fast signals. This effectively increases the instrument's bandwidth at the expense of efficiency in gathering information about the signals, since many repetitions are required to have enough data to reconstruct the waveform. The diagrams of Figure 1 indicate how this sampling procedure is accomplished.

In practice the sampling pulse, Figure 1-a, and the signal, Figure 1-b, may be summed as per Figure 1-c. The peak amplitude or sample, of the combination is detected, stretched, amplified, and applied to the vertical deflection plates of the CRT, thus giving a vertical deflection proportional to the magnitude of



1-f CRT Plot of Sample

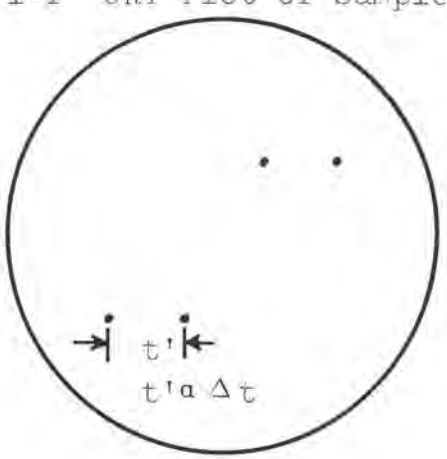


Figure 1. Waveforms In a Sampling Process

the input signal at the time it was sampled (3, p. 6). Then the next input waveform is sampled at some time Δt later from t_{so} and the CRT horizontal deflection voltage, E_h, increased by ΔE_h. This sample is proportional to the signal at $t_{so} + \Delta t$ and will be displayed at a later timewise position on the CRT face by (ΔE_h) x (oscilloscope horizontal deflection sensitivity, S_h). On the next signal input, the sampling pulse is delayed by 2 Δt from t_{so} and E_h is again increased by ΔE_h, thus displaying another sample at $(E_h)(S_h) = (E_{ho}+2\ \Delta E_h)(S_h)$. This process continues until $(t_{so} + n\ \Delta t)$ and $(E_{ho} + n\ \Delta E_h)$ reaches some specified value. Then the sample pulse delay and the horizontal deflection voltage return to zero and the process repeats itself, thereby giving an effective time stretching of the signal and a sampled display on the CRT face which is a low frequency replica of the signal. Only four samples are shown in Figure 1 for graphical clarity, but for the actual display, as many as a hundred or more samples per scan, or display, of the signal may be used by decreasing Δt and ΔE_h. This brings up the interesting point that for many samples per scan, the stairstep waveform of Figure 1-d becomes essentially a linear ramp. This property is used in the final design of the thesis instrument. Also, in Figure 1 the time

between the waveform repetitions is shown as the same order of magnitude as the pulse width for ease of graphical representation. This spacing is, in practice, the repetition time of the waveform, which may be one millisecond for a one kilocycle repetition rate or ten microseconds for a 100 kilocycle repetition rate, etc. Now it can be seen that the vertical deflection voltage for each sample may be many times the duration of the signal waveform itself, yet represent only a small fraction of the signal timewise. In this manner the time stretching or frequency division is accomplished and the circuits from this point on in the instrument's signal path need not be high speed.

THE SAMPLING SYSTEM

The block diagrams of Figure 2 and Figure 3 represent two possible systems for an oscilloscope sampling converter. The former depicts an internally triggered system, i.e., the converter operates in the free running mode and triggers the test circuit at the appropriate time in the converter cycle. The latter, Figure 3, indicates an externally triggered system where the signal to be monitered triggers the sampling system. Obviously, the possibility of both modes of operation would be useful in a laboratory instrument and the system described in this thesis will operate conveniently in either mode. For the sake of clarity, the two modes of operation are discussed separately.

The operation of the internally triggered system of Figure 2 is as follows: The clock pulse generator is operating in the free running mode and has a positive pulse output of about 20 volts magnitude and one microsecond duration with a repetition rate of 50 kc. For this discussion consider the start of each pulse of the clock as t_o of the cycle. The leading edge of this pulse initiates the trigger output pulse generator. The sole function of this pulse generator is to provide a pulse output from the system to trigger the test circuit,

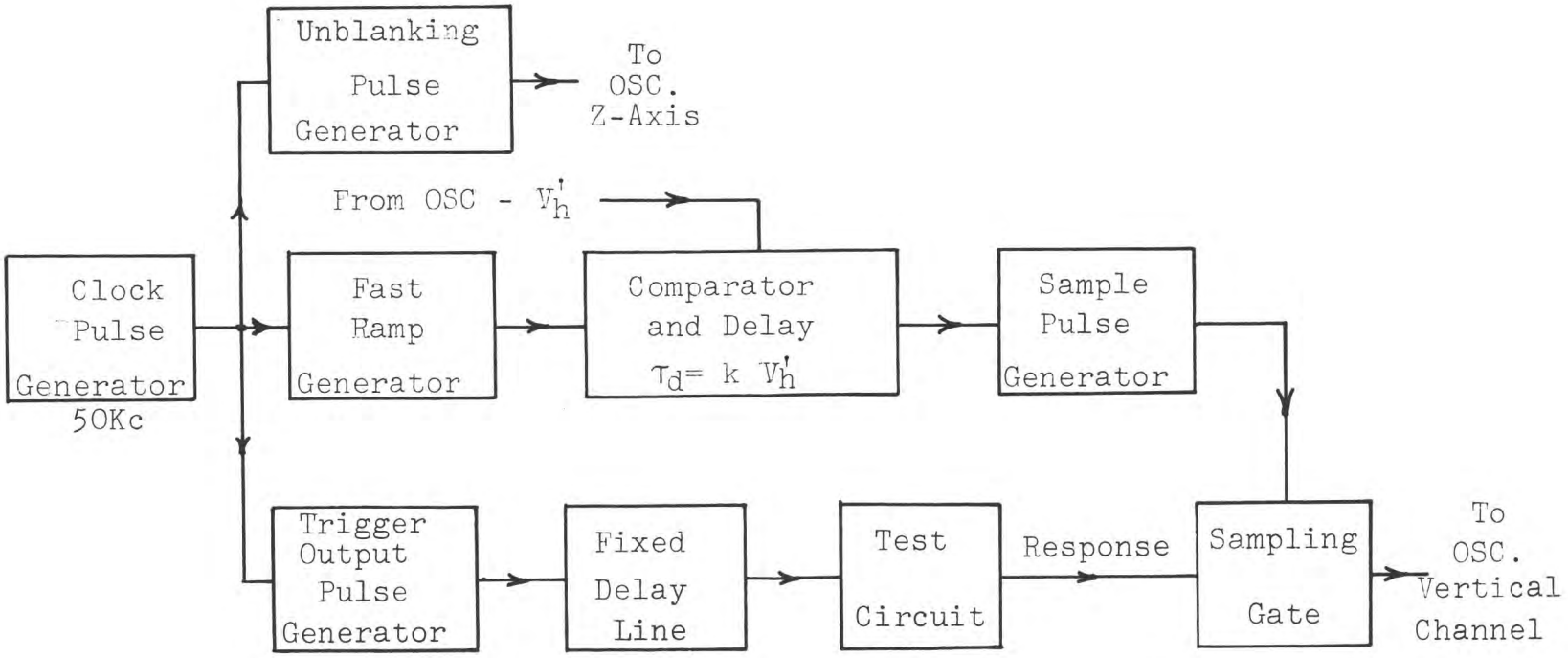


Figure 2. Block Diagram of Internally Triggered Sampling System

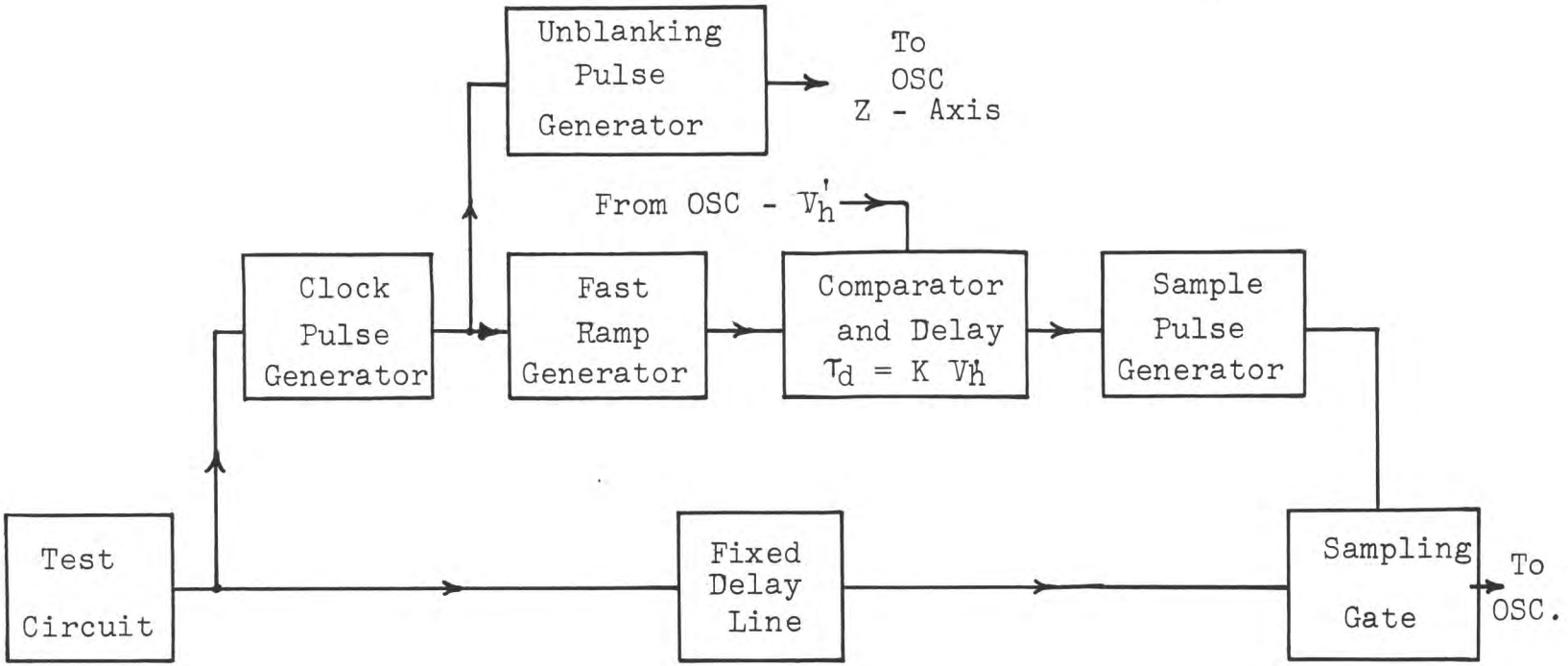


Figure 3. Block Diagram of Externally Triggered Sampling System

hence the time of this trigger action is always fixed with respect to t_o of the converter cycle. The output trigger pulse is delayed by propagation through an electronic delay line, such as a length of coaxial cable, before being applied as a trigger to the test circuit. The reason for this required delay will become clear as the system is further explained.

The leading edge of the clock pulse also initiates a fast linear voltage ramp of $\frac{dV_{fr}}{dt} = \frac{1}{k}$, which from circuit considerations is limited in time duration to the duration of the clock pulse and limited in peak amplitude to the amplitude of the clock pulse. This fast ramp voltage, V_{fr}, is fed into the voltage comparator circuit which compares the V_{fr} magnitude to the magnitude of a voltage proportional to the oscilloscope sweep which is slow enough to be considered dc compared to the fast ramp. When V_{fr} increases to some small constant, ΔE_t above the slow ramp, an output trigger pulse appears which will initiate the sampling pulse generator. The delay, τ_d, of the trigger output of the comparator with respect to t_o is then proportional to the magnitude of the slow ramp. This in turn is directly proportional to the horizontal deflection voltage, V_h, and the horizontal spot position of the CRT beam. The trigger delay equals $[k(V_h) + \tau_{min}]$ and is proportional to the horizontal

position of the CRT beam. Here k equals $1/\frac{dV_{fr}}{dt}$, and τ_{min} is a fixed, minimum possible delay. Now it can be seen that the output pulse from the sampling pulse generator appears at a small Δt later than the previous sample time position, with respect to t_o, for each successive cycle of the system until V_h reaches its maximum. Then V_h goes to zero, V_{ho}, and the process repeats itself, starting the sampling pulse at $t_o + \tau_{min}$. Linearly increasing the delay effectively sweeps the sample position across the signal repetitively. The minimum time after t_o at which the sample pulse may be generated results from the fixed minimum delay times to start the fast ramp, to then obtain a trigger output from the comparator, and for this trigger to operate the sampling pulse generator. The sum of these minimum delay times, τ_{min}, is then the minimum time at which the start of the test signal can be made available at the gate circuit to be sampled so that the sampling will include its initial rise or fall. Hence the reason for the delay of the trigger pulse to the test circuit; so the test signal will start at the sampling gate at some time later than τ_{min} with respect to t_o, and be sampled in its entirety.

As shown in Figure 1-c, the sample pulse and the test signal may be summed and the combination voltage

applied to a gate, Figure 2, which is set to open only when the sampling pulse is present. This charges a small capacitor to a voltage level proportional to the combination voltage during this sampling time. This sample voltage level then may be stretched, amplified, and applied to the vertical deflection plates of the CRT. An illustration of this is a gate consisting of merely a diode clipping circuit feeding into a capacitor with the capacitor output being applied to a high input impedance amplifier. With a clipping level set as per Figure 1-c, the capacitor will charge up to the peak amplitude of the sample while the gate is opened, then slowly discharge through the reverse biased diode and the high impedance amplifier. This simple stretcher circuit may be utilized only if a small enough portion of the stretched sample is utilized so that the RC discharge tilt of the capacitor voltage is not displayed. One technique of doing this is to have the CRT beam normally blanked off and then unblank it for a short time during a nearly constant voltage portion of the RC discharge of the sample storage capacitor. An unblanking pulse which is initiated by the trailing edge of the clock pulse and has a duration of a few microseconds is adequate for this. Thus, internally triggered sampling is accomplished, and may be shortly summarized as follows:

The voltage level of a small timewise portion of the signal is sampled and displayed on a CRT in a position proportional to the amplitude and time position of the sample at time $(t_o + \tau_d)$. Then τ_d is increased and another sample is taken from the next test signal and appropriately displayed. This process continues, repeatedly sampling the signal until it is displayed in its entirety. If the scanning rate, the rate at which a signal is entirely sampled along its time width, is high enough (approximately 20/second), the displayed replica of the signal will appear without flicker because of the retentivity of the CRT phosphors and the human eye. Note that this 20/second scanning rate corresponds to 50,000/20 = 2500 samples per scan or per ten centimeters. Therefore the display's individual samples will not be discernable. Also note that the number of samples per display may be changed by changing the speed of the sweep generator in the oscilloscope; number of samples per scan = $\frac{\text{free running rate of clock generator}}{1/(\text{time of ten cm. horizontal sweep})}$.

One other main consideration in this system is that the equivalent sweep time of the display is independent of the actual sweep of the oscilloscope. It is governed completely by the magnitude of the difference of $(V_{h_{max}} - V_{h_{min}}) = (\Delta V_h)_{max}$ as shown on page 10 where

$$(\Delta \tau_d)_{max} = \text{equivalent time of one sampling scan}$$

$$= k(\Delta V_h)_{max}.$$

This relationship then shows the simple way in which the equivalent sweep time may be changed; simply by changing $(\Delta V_h)_{max}$. This may be accomplished by a simple resistive voltage divider operating on the V_h sweep from the oscilloscope.

In summary then, the systems samples per scan rate may be changed by changing the oscilloscope sweep rate, the equivalent time calibration may be changed by changing the ratio in a resistive voltage divider, the high input impedance amplifier may be the oscilloscope vertical amplifier ($\sim$ 1 megohm for most oscilloscopes) and the vertical amplifier voltage calibration may be used as one of the controls.

In describing the externally triggered system of Figure 3, the differences between it and Figure 2 will suffice. The only differences are: (1) the clock pulse generator is made to operate in a triggered mode, to be triggered from the test signal at the test circuit output, and, (2) the required delay of the test signal before application to the sampling gate is accomplished by introducing a delay cable between the test circuit output and the sampling gate. In every other aspect the

operation is identical to the description of the first system except that now the samples per display rate is

$$\frac{\text{test circuit repetition rate}}{1/(\text{time for ten cm horizontal sweep})} = \text{samples per scan.}$$

The unit constructed and tested for this thesis operates in accordance with both of these system discussions. The details of how each specific part of the operation is obtained are discussed in the circuit descriptions section.

PERFORMANCE LIMITATIONS OF THE SAMPLING SYSTEM

The performance of the sampling system may be roughly divided into four categories: (1) response to a step input of voltage, or minimum rise time, (2) time jitter in the sampling pulse position, (3) linearity of the equivalent time base, and (4) the minimum viewable signal voltage level, which is dependent mainly on the ambient noise level of the sampling process.

In the first performance category, the minimum rise time which may be represented on the CRT can be shown to be approximately equal to the base width of the sampling pulse, if that pulse is assumed to be triangular in shape (3, p. 3). As will be shown in the circuit description section, this is a reasonable approximation. With this consideration, any attempt to increase the bandwidth of the instrument must first be aimed at decreasing the width of the sampling pulse itself.

Any decrease in the sampling pulse width to decrease the risetime of the system must be compatable with the time jitter in the positioning of the sampling pulse with respect to t_o, i.e., each equivalent sample of successive scans must occur at the same timewise position of the test signal. It is obvious that a sampling pulse capable of resolving a one nanosecond risetime is not

compatable with a positioning control with a one nanosecond order of magnitude time jitter. The experimental sample pulse generator has approximately a five millivolt randomness in its trigger level (2, p. 813) and is being triggered from a fast ramp of 40×10^6 V/sec. rate of rise, giving a time jitter of $(5 \times 10^{-3})/(40 \times 10^6) \cong$ 0.12ns, which would be compatable with a one nanosecond sampling pulse width.

The linearity of the equivalent sweep, or the linearity of τ_d, is dependent on the linearity of the fast ramp described in the previous section, if the slow ramp oscilloscope sweep is assumed linear. This is a good assumption for most oscilloscopes operating below their maximum sweep rate. The experimental fast ramp is derived from the first 20 volts of a 150 volt RC charge curve so the nonlinearity is

$$\text{N.L.} \cong 12.5\% \ln \frac{E_{bb}-E_I}{E_{bb}-E_f} \quad \text{(9, p. 156)}$$

$$= 12.5\% \ln \frac{150}{130} \cong 1.2\%$$

which is certainly adequate for most laboratory work.

The minimum signal level which may be displayed depends on the system mode of operation. For the externally triggered mode, the minimum is usually the minimum signal level which will trigger the system into operation. The

internally triggered low signal level limit is the ambient noise level of the system at the output of the converter referred to the input. These two limitations will be discussed further in the circuit descriptions, and are approximately one volt and 20 millivolts respectively.

EXPERIMENTAL CIRCUIT DESCRIPTION

Included in this section are descriptions and analyses of the component circuits which fit together to give the desired system action as described in the previous three sections. The circuits are not presented in the order of operation in the circuit, but rather in a manner in which the description of operation of a circuit may use ideas and concepts developed in the prior discussion of a simpler circuit whose operation is easier to perceive. Then the interaction of the separate circuits in the system scheme will be discussed and expanded upon, to give a complete picture of the operation of the sampling converter unit, with descriptive equations presented to define its operation and characteristics.

Trigger Output Generator

The circuit utilized to give a trigger pulse out of the system to initiate a test circuit cycle is a basic avalanche mode transistor pulse generator as shown in Figure 4. Typical collector characteristics of a transistor with $I_b = 0$ are shown in Figure 5, indicating the switching characteristics of the device. In the circuit of Figure 4, the transistor is biased near its avalanche breakdown region as shown by the dc load line. When a

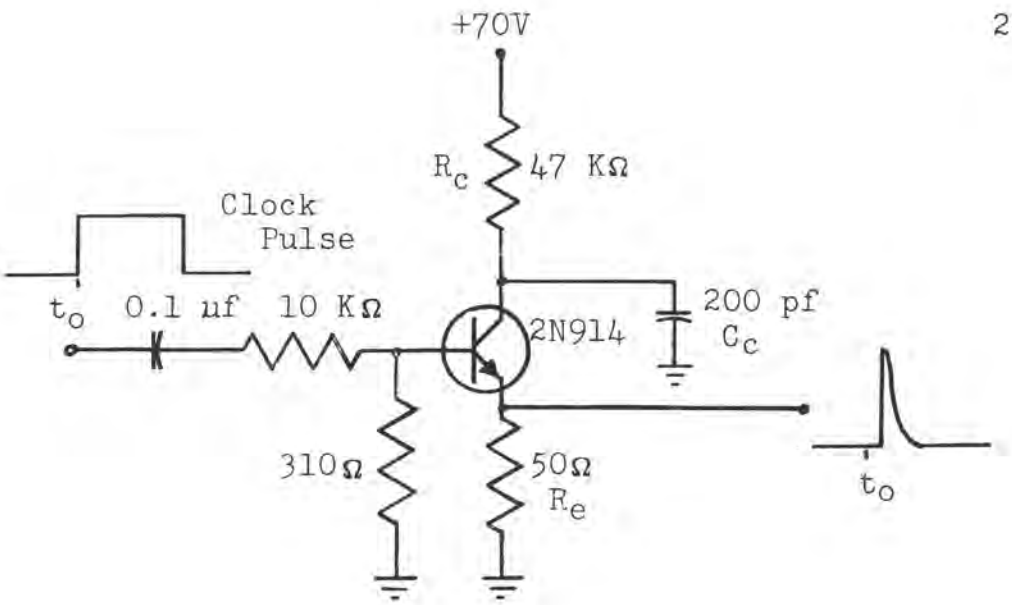


Figure 4. Trigger Output Pulse Generator

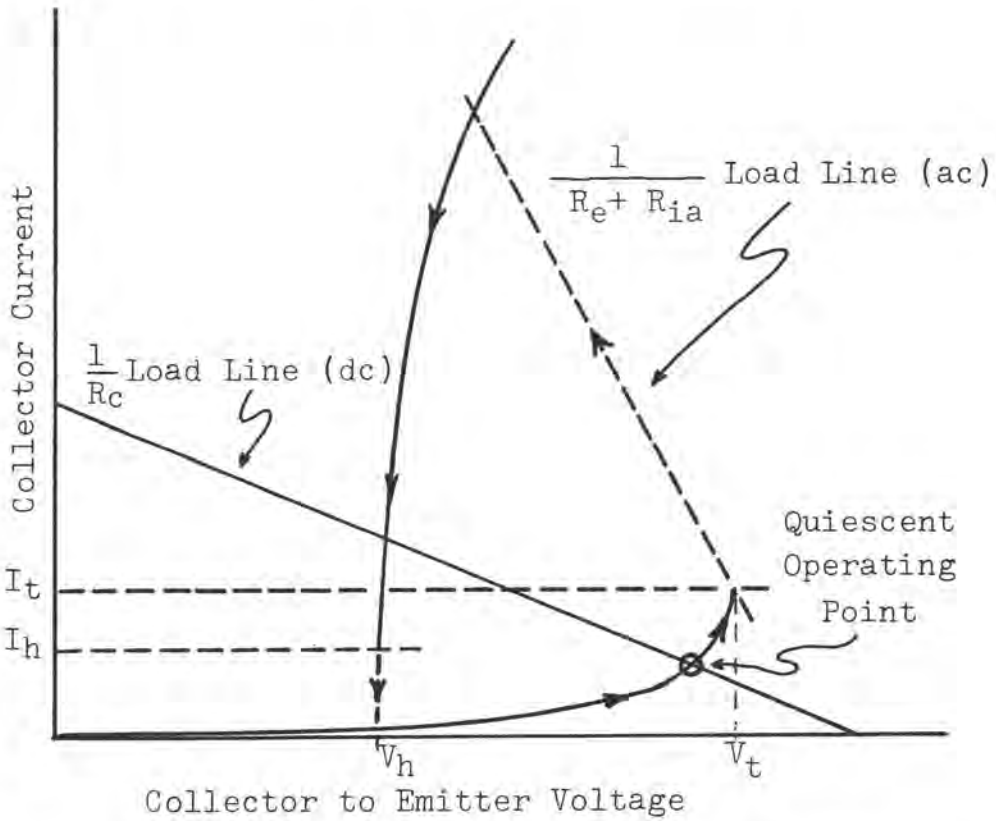


Figure 5. Collector Volt-Ampere Characteristics of An Avalanche Mode Transistor (7, p. 15)

positive pulse of base current is introduced, the collector current will increase to above the trigger current, I_t, of the transistor and it will enter the avalanche breakdown condition. Then the transistor has an internal avalanche resistance, R_{ia}, of about 40 ohms from collector to emitter (7, p. 22). Then the R_c is large enough to be considered an open circuit, and the rest of the circuit consists of the collector capacitor, C_c, as a voltage source to the series R_{ia} and R_e. The capacitor provides current through the transistor and R_e until it has discharged to below the holding current, I_h, of the transistor. Then the transistor switches out of the avalanche mode and back to its normal,high collector to emitter impedance state and the capacitor discharge stops. This gives, then, a voltage output pulse across R_e as long as the capacitor is discharging. The pulse width is governed by the RC time constant of $(R_e+R_{ia})\ C_c$, which is approximately 20 nanoseconds, and the breakdown and holding voltages of the transistor. The avalanche breakdown or ionization process is extremely rapid giving collector voltage fall times or emitter resistor voltage rise times of the order of a very few nanoseconds. The width of the pulse is then mainly determined by the $(R_e+R_{ia})\ C_c$ time constant, and the circuit gives a narrow, fast risetime pulse output of

approximately 35 volts amplitude which is very suitable for use as a trigger pulse. Immediately after the pulse output the capacitor C_c voltage is at about the holding voltage of the transistor and must charge through the 47 kΩ collector resistor to near the breakdown voltage of the transistor before the circuit can be triggered again. This gives an automatic holdoff action to keep the pulse generator from being retriggered during the active one microsecond portion of the converter cycle since $R_cC_c \cong$ 5 microseconds. As shown in Figure 4, this pulse generator is triggered by the positive going portion of the clock pulse, so the output trigger pulse is always at t_o plus the delay time of the avalanche process which is about ten nanoseconds for a typical transistor of the type used, i.e., 2N914.

Unblanking Pulse Generator

Data from a Tektronix type 545 oscilloscope indicated that with the intensity control decreased until the electron beam spot on the CRT face was not visible, a 40 volt, negative going, two microsecond pulse applied to the z-axis terminal, i.e., CRT grid, was sufficient to unblank the beam for good viewing. Subsequent data on various models of Tektronix and Hewlett-Packard oscilloscopes indicated that this is a typical value for good results.

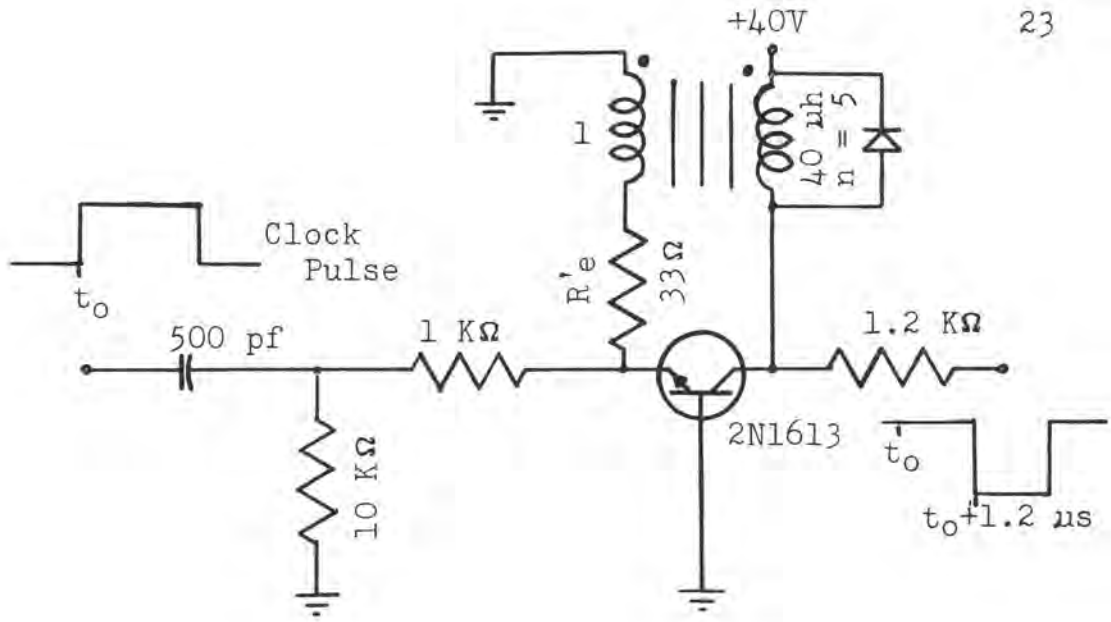


Figure 6. Unblanking Pulse Generator

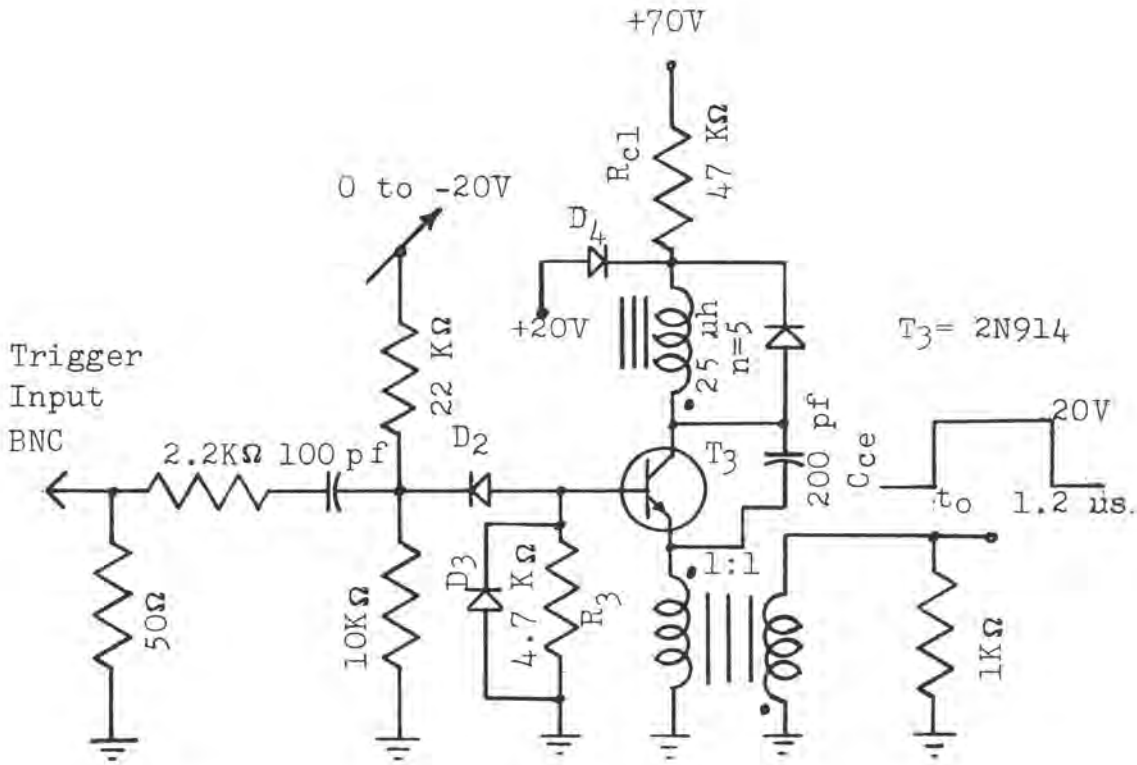


Figure 7. Clock Pulse Generator

The circuit chosen to obtain the required unblanking pulse was the emitter controlled blocking oscillator as shown in Figure 6. The blocking oscillator offers a simple circuit, which is easily triggered, and which meets the requirements as stated above. The emitter controlled configuration was used mainly because the output pulse width is somewhat independent of transistor parameter variations as shown in Equation 2, where

$$PW = \frac{L}{nR_e'}\left[\alpha - \frac{1}{n}\right] \qquad \text{Equation 2 (5, p. 246)}$$

L is the primary inductance of the transformer, n is the turns ratio and α is the transistor collector-emitter current ratio. The circuit in Figure 6 requires a negative going trigger pulse and is timed to occur after the sampling process has occurred, thus the simple RC differentiating circuit acting on the clock pulse gives the required negative trigger from the trailing edge of the clock pulse, which is at the appropriate time in the converter cycle. No circuit isolation is required since the sampling portion of the converter cycle is completed when the unblanking pulse generator is active, and the sample storage element is not influenced by this unblanking pulse generator.

Clock Pulse Generator

The clock pulse generator requirements from the system discussion were perhaps the most stringent in the

whole system. The output needed to be a very fast rise voltage pulse of about 20 volts magnitude and one microsecond duration with the pulse generator capable of free-running or triggered operation. For the free-running mode, the repetition rate was to be approximately 50 kc, and the triggered mode was to trigger on a low level, narrow pulse with a very small, but constant, amount of delay time. The square pulse requirement suggests the use of a blocking oscillator circuit, however, rise times and trigger delay times are not in the low nanosecond range as would be desirable. These latter requirements make an avalanche pulse generator seem attractive, especially so since it may be made to operate free-running or triggered simply by changing a supply voltage level, usually the collector supply. Also, a continuously variable supply allows adjustment of repetition rate, or trigger sensitivity, depending on which operating mode it is in. However, the avalanche generator, in its simple form, requires a bulky, and perhaps expensive, delay cable or simulated delay line in order to generate a flat topped pulse (7, p. 37). Thus the circuit of Figure 7, which combines the avalanche and blocking oscillator operation into the same circuit, is used. It is a blocking oscillator with the transistor operating in the avalanche mode.

Consider only the part of the circuit of Figure 7 to the right of diode D_2, which excludes the triggering portion of the circuitry. The collector bias of 70 volts is sufficient to free run the type of avalanche transistor used, the 2N914. Starting at the portion of the cycle when the 200 pfd capacitor has just charged to the firing potential of the transistor, the transistor enters the avalanche mode of breakdown and the collector voltage goes towards zero volts with a fall time of low nanosecond order of magnitude. But when the cathode of D_4 becomes less than 20 volts, D_4 becomes forward biased and the circuit is then exactly equivalent to the blocking oscillator described in the previous section since also during this time the transformer winding in the transistor emitter circuit has coupled a negative pulse to the emitter circuit which would tend to forward bias the base emitter junction of T_3 and the diode D_3. This is equivalent to having grounded base operation. Then the pulse width is determined mainly by the transformer primary inductance and the pulse magnitude is the 20 volts of the power supply times the output transformer ratio, which in this case is 1:1. Using the third winding on the transformer gives some choice in the output as to polarity and magnitude, and for this application gives a needed low resistance dc bias path as will be described

in the next section. The collector-emitter capacitor completely discharges during the blocking oscillator portion of the cycle when T_3 is saturated and the repetition rate is then determined by the charge time, from zero volts to the breakdown voltage of the transistor, of the 200 pf C_{ce} through the 47 kΩ R_{c1}, with $R_{c1}C_{ce} \cong 9$ microseconds.

The triggering method is similar to that used by R. B. Seeds (8, p. 53), in that the transistor collector is biased at a high enough voltage so the transistor is in the avalanche multiplication region, but that the avalanche current is allowed to flow out of the base, in this case by virtue of the negative 20 volt supply, $-V_1$, and diode D_2, so that the transistor does not enter an active avalanche breakdown state. A positive voltage pulse applied to D_2 will turn it off, and the base reverse bias avalanche current must then flow in the emitter circuit, i.e., electrons are emitted into the base, and then avalanche breakdown will occur and the clock pulse generator cycle will start. Note here that by decreasing the magnitude of $-V_1$, the diode D_2 may be dc biased off and the blocking oscillator will then be in the free running mode of operation, or by increasing the magnitude of $-V_1$ the diode D_2 is forward biased and

the trigger sensitivity may be controlled by $-V_1$, i.e., the greater $-V_1$, the less the trigger sensitivity, or the greater the pulse voltage required to back bias D_2 is. Thus a simple potentiometer variable supply voltage is sufficient to control the mode of operation, free-running or triggered, and the trigger sensitivity of this clock pulse generator. In this circuit, similar to the trigger output circuit, there is a hold-off action due to the fact that C_{ce} must be recharged for a trigger pulse to have any effect, thus in effect the clock generator counts down high repetition rate trigger signals to about the 50 kc free-running repetition rate. Also, the diodes D_2 and D_3 are biased such that during the active portion of the cycle, no feed through into the trigger circuit is experienced, and thus no buffer trigger amplifier is required.

Ramp Generator

The ramp generator output needed to be a very linear ramp with a peak magnitude of approximately 20 volts at one microsecond from its initiation. As shown in Figure 8, the diode D_5 is normally forward biased and point 2 is at approximately +0.3 volts. Upon application of the clock pulse, D_5 is back biased and C_r begins charging to 150 volts through R_r. Here lies the requirement for

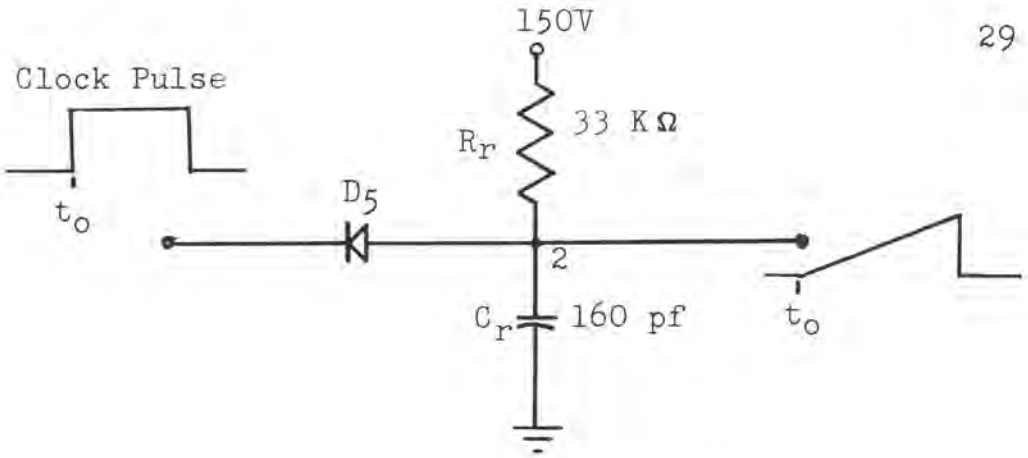


Figure 8. Fast Ramp Generator

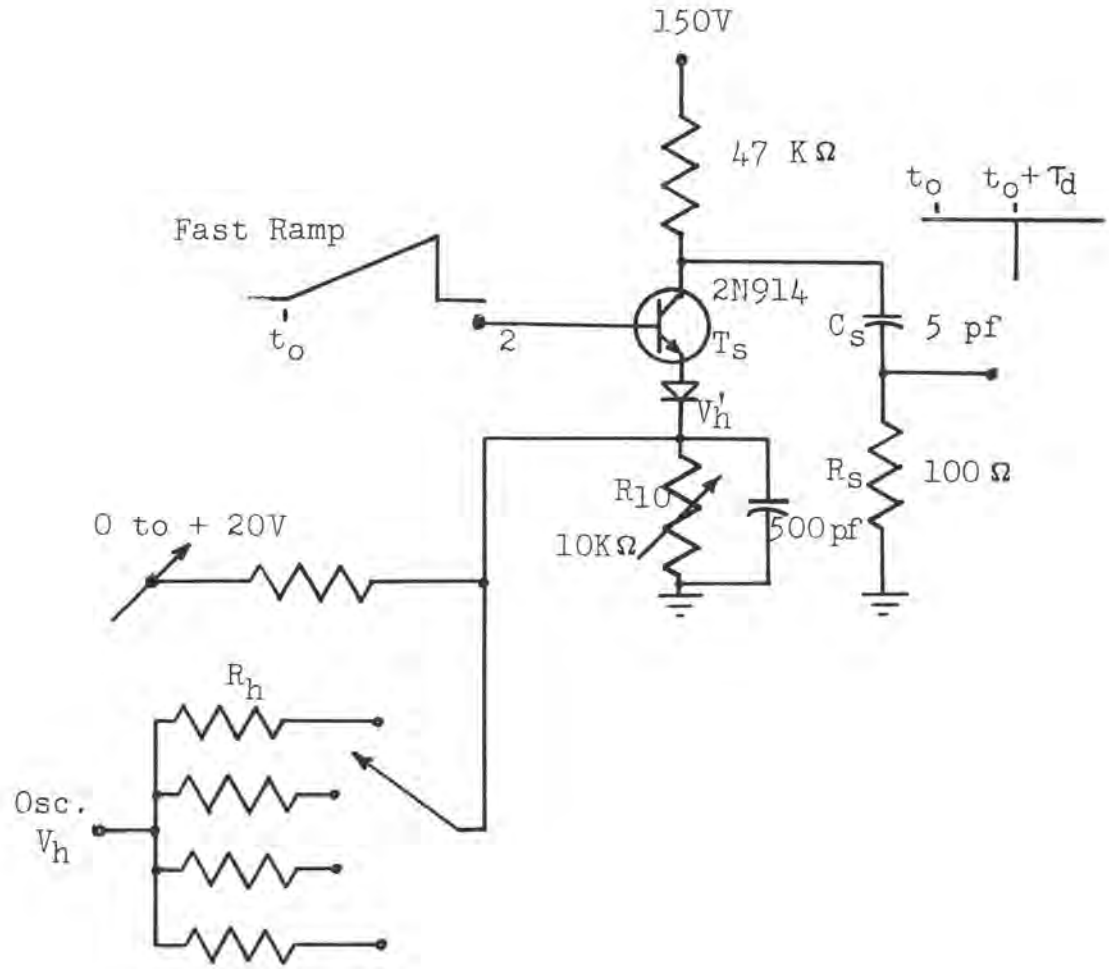


Figure 9. Comparator and Sample Pulse Generator

the magnitude of the clock pulse since the point 1 voltage must not exceed the clock pulse voltage during the active portion of the converter cycle. Twenty volts and one microsecond were chosen giving a fast ramp, $\frac{dV_{fr}}{dt}$ = 20 Mv/second, a linear portion of the RC charge curve, N.L. $\cong$ 1.2% and the ability to observe a one microsecond range of real time in the final display. At the end of the clock pulse, D_5 becomes forward biased and C_r discharges quickly through the diode forward resistance and is ready for the next cycle in the sampling operation.

Sample Pulse Generator

The circuit shown in Figure 9 combines three operations; generating the sampling gate pulse, providing the change of sample position, timewise, and providing a dc control for time or horizontal positioning. The pulse generator portion of the circuit is, in essence, the same as the trigger output circuit, except that here the collector capacitor C_s is so small that the R_s and C_s have the effect of severely differentiating the avalanche breakdown step voltage of the transistor, giving the narrow two or three nanosecond pulse as required. Since the avalanche step magnitude is of the order of 40V, the loss of magnitude in the R-C differentiator

is of no great consequence. As seen from Figure 9, the triggering of the circuit occurs when the voltage V_2 increases to some specified value V_t above the voltage V_h'. The value of V_t was found to vary somewhat from transistor to transistor but was a constant, as required, for each unit (1, p. 99). Since V_h' is slowly increasing, each sample pulse will occur at some time later, with respect to t_o, than the previous pulse as described by the following equations:

$$t_{sp} = t_o + K(V_h' + V_t - 0.3) \qquad \text{Equation 2}$$

$$\text{where } V_h' = \frac{V_R R_{10}}{R_{10}+R_h} + V_{dc} \qquad \text{Equation 3}$$

As can be seen from these equations the sample occurs at a real time, with respect to t_o, which is proportional to the horizontal sweep voltage, V_h, which is in turn proportional to the horizontal position of the CRT beam as described in the system discussion. Thus the sample position and the CRT beam display position are timewise equivalent. Also, the equivalent time calibration may be changed simply by changing R_h, a method used as a front panel rotary switch on the experimental model. In the experimental system there is a front panel provision for changing the dc bias contribution to V_h', V_{dc}, which is a method of horizontal positioning of the "viewing window" with respect to t_o. The

diode D_6 is included so that when V_h' is large with respect to V_2 the base-emitter junction of T_s will not experience reverse breakdown.

Sampling Gate

The final portion of the converter circuit is shown in Figure 10, the sample gate itself. A Laplace analysis of this circuit shows that the voltage appearing at point 3 is the average of the sample pulse generator voltage and the incoming test signal, V_s, or

$$V_3 = \frac{V_{pg}+V_s}{2} = \frac{V_{pg}}{2} + \frac{V_s}{2}. \quad \text{Equation 4}$$

Considering only the time in the cycle when $|V_{pg}|$ is a maximum, the variations in the voltage level V_{3max} are due only to test level signal variations since $|V_{pg}|_{max}$ is a constant. At the occurrence of a sampling pulse maximum, the diode D_7 is forward biased and $[C_5+C_{input}]= C_i$ is charged through$(r_{D_7}+ 50\Omega)$ to a value which will be proportional to the value of V_s. At the end of the sampling pulse, D_7 is again reverse biased and C_s must discharge through$(r_{D_7} \| 5\ M\Omega) \cong 5\ M\Omega$. This long time constant allows C_i to stay charged long enough so that the one microsecond unblanking pulse, which allows this voltage to be displayed, is not long enough so the voltage tilt is noticable in the display. However, the

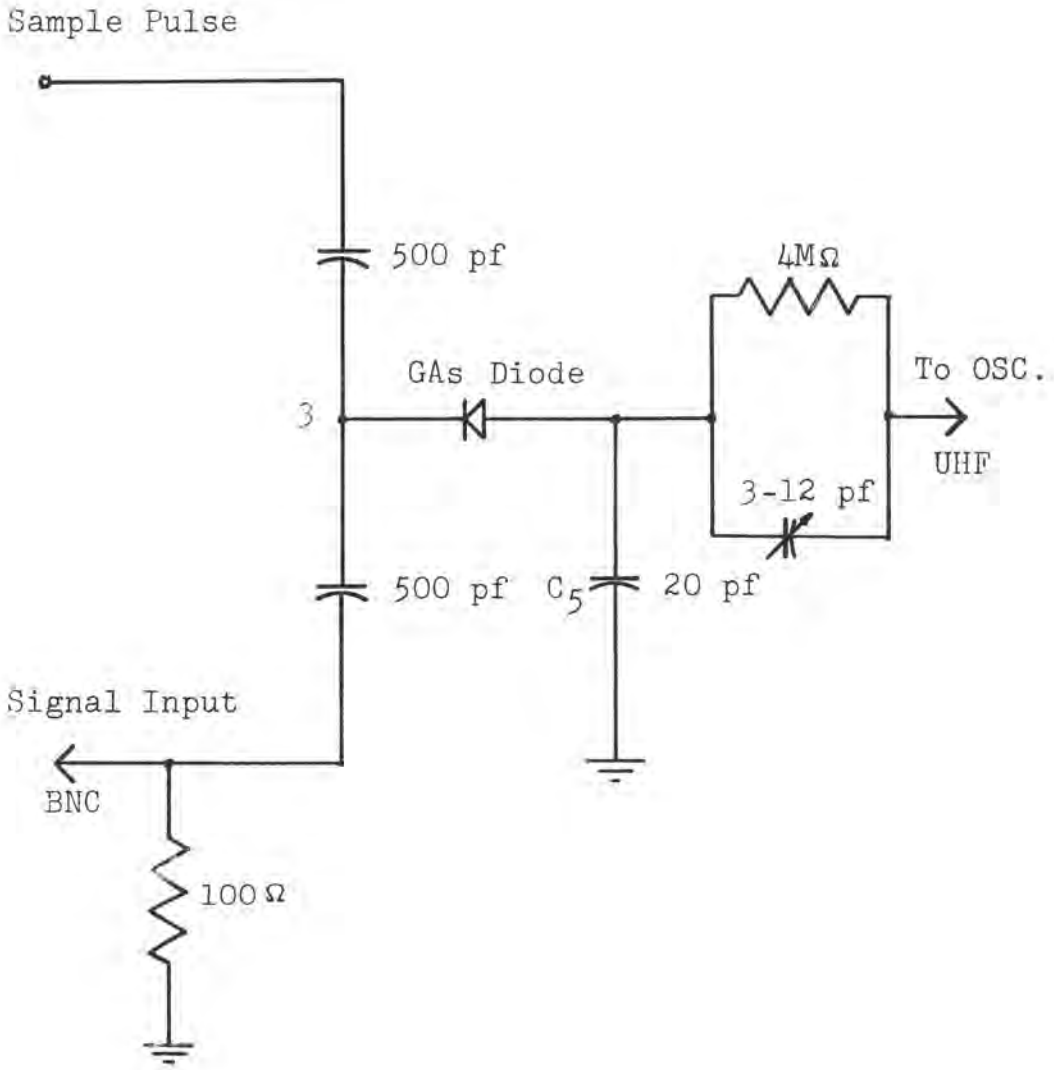


Figure 10. Sampling Gate

discharge is fast enough so C_i is completely discharged by the time the next sample occurs. As can be seen from the above discussion, the input signal level must not exceed the $|V_{pg}|$ max $\cong$ 2 Volts for the sampling gate to function properly. Also, in this circuit there is considerable attenuation between the signal and the sample voltage, first due to the averaging property of the input capacitors, then because the charge time constant of C_s is long enough so that C_s does not become fully charged during the sample duration (sampling efficiency) and finally the 5:1 attenuation of the input circuit to the oscilloscope. However, recognize the fact that at the output of this converter, the signal is not of exceptionally high frequency content and the conventional amplifiers of an oscilloscope may be used to amplify the samples to sufficient magnitude for a vertical display of the sample. The speed requirement placed on the display oscilloscope is that its vertical amplifier must have a risetime equal to or less than the minimum possible time between a sample and the unblanking of the CRT beam. This minimum time occurs when τ_d is maximum and is the clock generator output pulse width plus the unblanking pulse generator risetime minus $\tau_{d_{max}}$. For the experimental model this is

(1.2+0.2-1) microsecond = 400 nanoseconds

which corresponds to about a one megacycle bandwidth requirement for the oscilloscope's vertical amplifier. This minimum risetime may be increased by increasing the clock generator pulse width, but the sample capacitance discharge curve must have a long enough time constant so the sample voltage is very near its maximum value during the unblanking pulse for all values of T_d, or sample position, to avoid waveform distortion.

System Circuit Operation

From the discussion of the separate circuits comprising the sampling system, the operation of the system becomes more obvious. This section is presented with the idea of further clarifying the operation and presenting equations to describe it.

The need for a method of electronically delaying the signal can now be seen in that the clock pulse generator, the ramp generator, and the sample pulse generator each have some inherent minimum delay. The minimum delay real time position of the sample pulse must occur before the beginning of the test signal pulse at the input of the sample gate, in order for the initial portion of the test signal to be sampled and displayed. A delay line consisting of coaxial cable with 50 ns

delay proved satisfactory.

From circuit discussions it can now be seen that the sweep rate, f_s, of the oscilloscope has nothing to do with the apparent sweep speed but that it controls the number of samples per display, S_d, as follows:

$$S_d = \frac{\text{(Test Signal Repetition Rate)}}{\text{(Oscilloscope Sweep Rate)}} \quad \text{Equation 5}$$

Thus the samples may be made to appear spaced apart or to be a continuous line merely by increasing or decreasing the f_s of the oscilloscope, for any repetition rate of the signal. Since the sample is always taken and displayed at a time and position which is proportional to the oscilloscope sweep voltage, the test signal repetition rate may be variable.

The apparent sweep speed may be changed by switching in different values of R_h as shown in Figure 9. The following are equations for calibration of the apparent sweep speed in terms of R_h, $\frac{1}{k} = \frac{dV_{fr}}{dt}$ of the fast ramp, and V_{hm} which is the value of the voltage of the slow ramp of the horizontal sweep which corresponds to 10cm of deflection.

$$T = \text{apparent time/cm} = (k)\left[\frac{V_{hm}}{10}\right]\left[\frac{R_{10}}{R_{10}+R_h}\right]$$

$$\text{or } R_h = \left[\frac{k\,\frac{V_{hm}}{10}\,(R_{10})}{T}\right] - R_{10}$$

or for the experimental circuit

$$R_h = (20 \times 10^{-9})\left[\frac{V_{hm}}{T}\right] - 10k\Omega$$

In the circuit, R_{10} is a potentiometer to provide internal calibration of the apparent sweep speed to a standard.

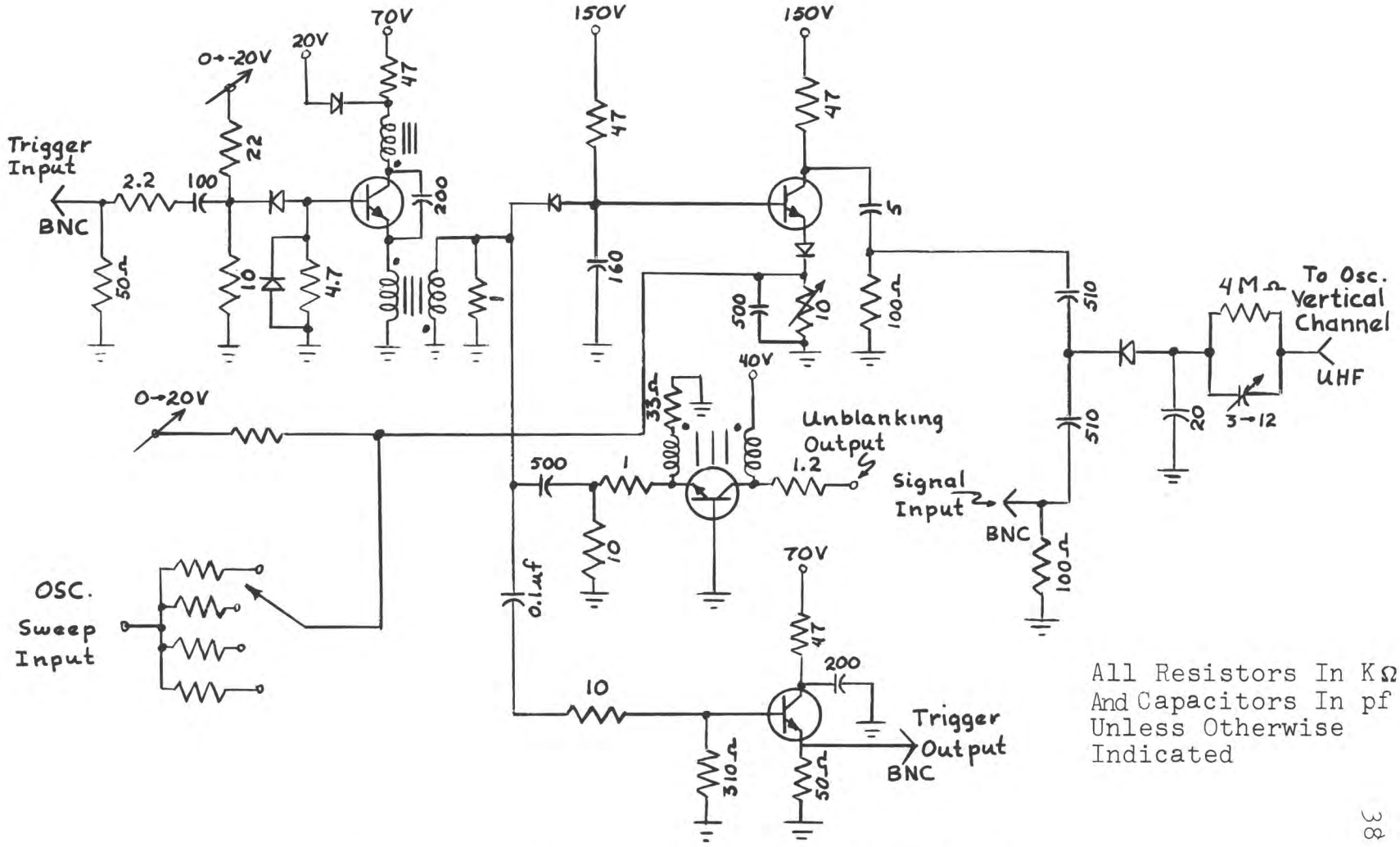


Figure 11. Converter Unit Circuit Schematic

EXPERIMENTAL RESULTS AND EVALUATION OF PERFORMANCE

The circuit of Figure 11 shows the final circuit with the exception of the dc power supply and dc voltage dividers. The experimental unit constructed, see Figure 12, required external dc power supplies of +150V @ 30ma and - 20 V @ 5ma with the various values of dc voltage required internal to the unit provided by simple resistive voltage dividers and capacitor filters. Since the duty cycle of the various component circuits of the converter is small, less than two percent, the filtering requirements are not excessive. The specifications of the unit used in conjunction with a one megacycle bandwidth oscilloscope are summarized in Table I below.

Table I

Sampling Converter Specifications

Oscilloscope Used in Test -	Tektronix 545 Model Oscilloscope with Type D plug-in set at one megacycle bandwidth.
Free Running Operation	

Trigger Output Amplitude	- 30 V
Trigger Output Risetime	- 1 nanosecond
Trigger Output Pulse Width	- 35 nanoseconds (50% Point)
Repetition Rate	- 48 kc
Apparent Minimum Risetime	- 2 nanoseconds
Input Sensitivity	- factor of 0.1 between input and output signal levels
Noise Level	- 20 millivolts referred to input
Maximum Pulse Width Which May be Displayed	- 1000 nanoseconds
Input Overload Voltage Level	- 2 Volts
Minimum Delay of Test Signal Input	- 50 nanoseconds from trigger output time in cycle
Sweep Nonlinearity	- None Observed (calculated 1.2%)
Waveform Distortion	- None Observed

Triggered Operation

Trigger Input Requirements	- 1V, 5 nanoseconds minimum 0.5V, 20 nanoseconds minimum
Trigger Input Repetition Rate	- Maximum Converter Repetition Rate, 52 kc. Counts down higher trigger rates to approximately 50 kc.

Apparent Minimum Risetime	- 2 nanoseconds
Input Sensitivity	- Factor of 0.05 between input and output signal level.
Noise Level	- 20 millivolts referred to input
Maximum Pulse Width Which May be Displayed	- 1000 nanoseconds
Signal Input Overload Voltage Level	- 2 Volts
Must Delay Test Signal Input	- 50 nanoseconds between trigger input and signal input

Sweep Nonlinearity and Waveform Distortion - N.O.

Figures 13 and 14 show oscillograms obtained from the experimental unit used as described in Table I, with triggered operation. The oscillograms of Figure 13 are obtained using a 60 cps pulse generator with rise and fall times less than one nanosecond, so the apparent risetime of two nanoseconds, which corresponds to a bandwidth of approximately 200 megacycles, is then the minimum risetime of the converter unit. Figure 14 was obtained using a 100 Kc pulse generator and shows that a wide pulse width may be observed with the converter. The four oscillograms indicate the wide range of repetition rates with which the converter is useful and also that a reasonably long pulse may be observed. The combination then, of a one megacycle oscilloscope used conventionally or with

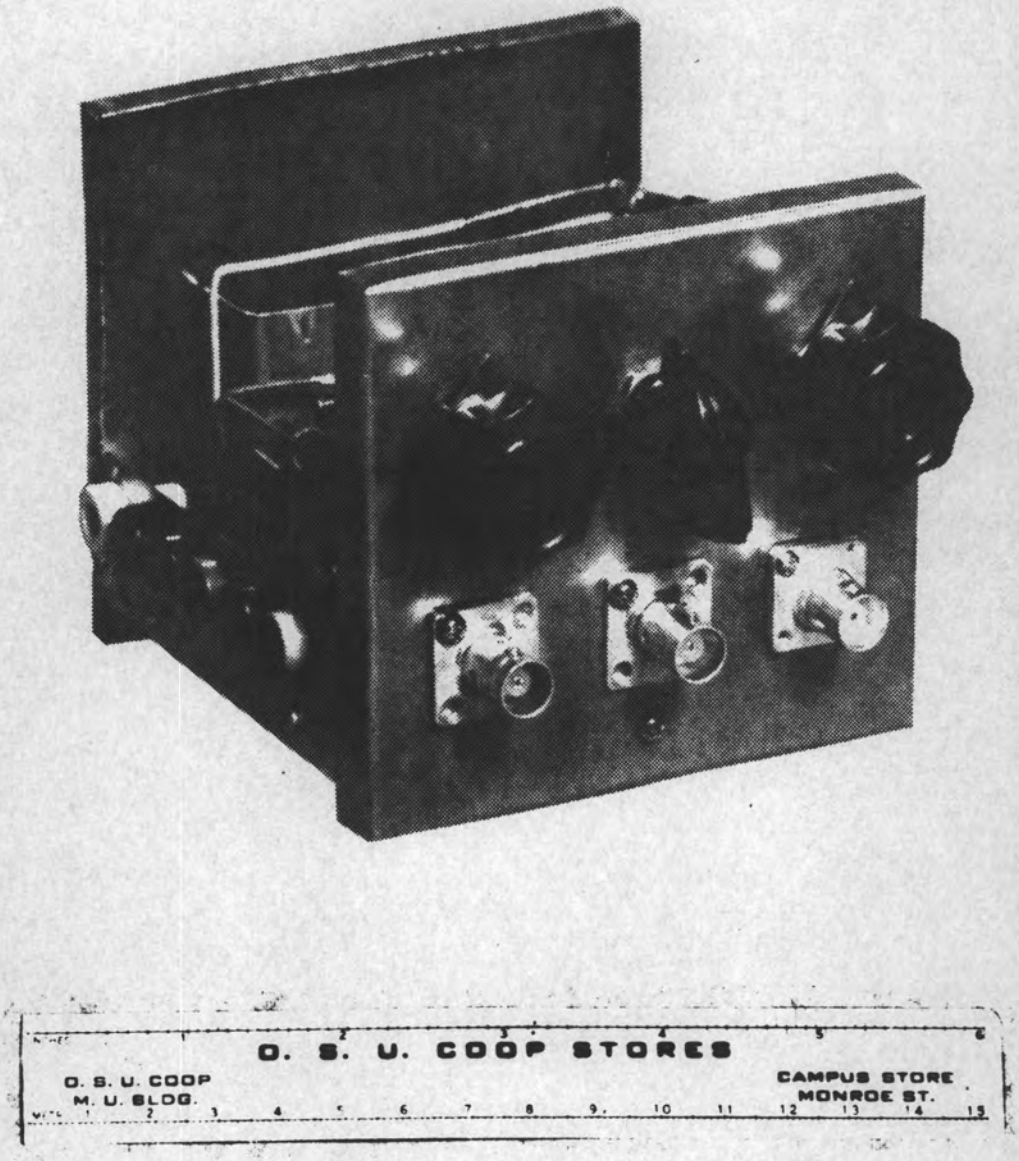


Figure 12 Experimental Converter Unit

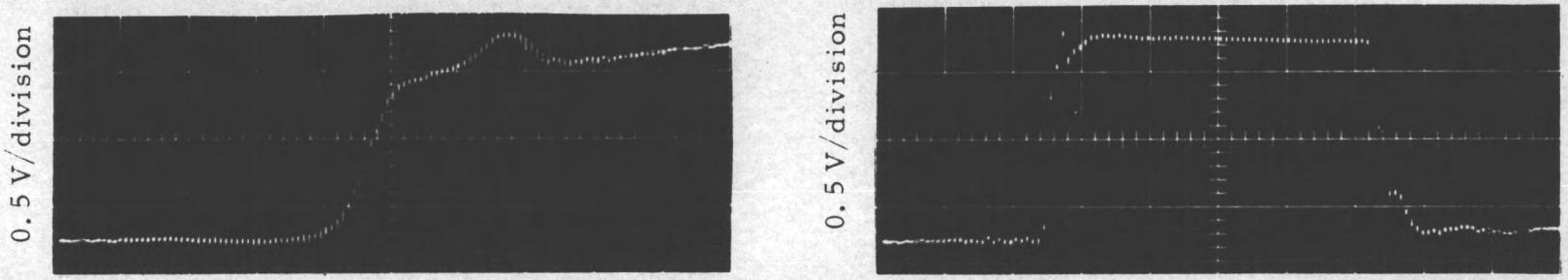


Figure 13 Experimental Oscillograms Obtained Using The Converter In Conjunction With A One Megacycle BW Oscilloscope. Pulse Source--Epic Model 200 PG ($RT < 0.6$ ns)

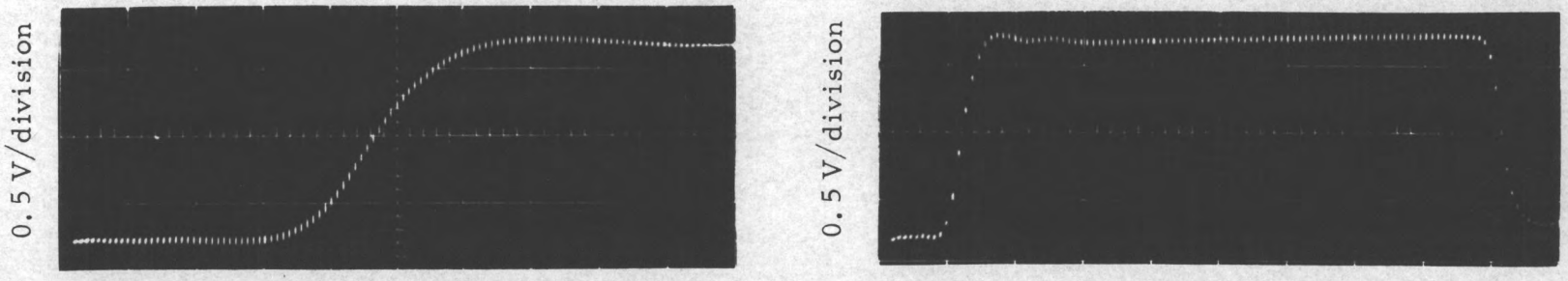


Figure 14 Experimental Oscillograms Obtained Using The Converter In Conjunction With A One Megacycle BW Oscilloscope. Pulse Source--Dumont Model 404 PG ($RT \cong 25$ ns)

the experimental converter unit, gives coverage from dc to 200 megacycles bandwidth with relatively little expense.

In the experimental unit, with three fast switching avalanche transistors, there was a problem of electrostatic coupling to the sampling gate which showed up as noise on the display. This was relatively easy to overcome by simple electrostatic shielding around the sampling gate circuitry. The resulting noise level of the unit can be attributed to the slight random variation of the sampling pulse peak magnitude which was approximately ten millivolts, or 20 millivolts as referred to the input.

SUMMARY

This thesis has presented a simple, yet effective, system circuit concept which allows a relatively low frequency oscilloscope to be used in the sampling mode to observe experimental voltage waveforms with rise and fall times in the order of two nanoseconds. The circuits of this system are exclusively solid state and use extensively the avalanche mode of operation of a transistor and the inherent triggering stability, low trigger delay times, large voltage swings, and nanosecond switching abilities of this mode.

The greatest advantage of this system is obtained by recognizing the fact that certain functions common to every oscilloscope may be used to perform functions which are required in a sampling system. By recognizing this fact, it was possible to use the horizontal sweep of an oscilloscope to position not only the electron beam of the CRT but to provide a signal which determined the time position of a sampling pulse with respect to a test signal. In this manner horizontal sweep circuits and part of the sampling pulse delay circuit were eliminated from the sampling converter. Another consequence of this line of reasoning is that the sampling process is essentially a frequency converting device, and the output of

the sampling circuit itself, although low level, is of low frequency content and any amplification which may need to be done at this point in the circuit to provide vertical CRT beam deflection may be adequately handled by a relatively low frequency amplifier, one megacycle in the experimental converter, as available in the vertical channel of an oscilloscope. Thus the need for amplifying circuits in the converter is virtually eliminated. By avoiding redundancy of effort in the above manner, the final converter circuit contained a total of only four transistors, three of the avalanche variety, of which adequate performance could be obtained by selecting particular units from commercially inexpensive transistor types.

The final circuit was designed with simplicity and ease of laboratory use being a prime consideration along with speed requirements which would rival the best conventional high speed oscilloscope. The result is a system whose bandwidth is from dc to approximately 200 megacycles which is capable of operating in either a signal triggered or trigger the signal mode. The main disadvantages of the experimental system are a 20 millivolt input noise level, 50 ohm level signal input connection and the requirement that the test signal be repetitive in nature. Even with these limitations, the

potential low cost, the performance available, and the ease of operation make this converter unit a useful laboratory instrument.

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APPENDIX

OPERATING INSTRUCTIONS FOR EXPERIMENTAL SAMPLING CONVERTER

1. Attach the unit to input of an oscilloscope using UHF connector.
2. Connect the unblanking output terminal to the z-axis of CRT grid of the oscilloscope.
3. Connect the ramp input terminal to the sweep output of the oscilliscope.
4. Connect the +150, Ground, and -20 V dc power supplies to the appropriate terminals of the converter.
5. Set the oscilloscope trigger to free running.
6. Set the converter trigger level control to free running.
7. Adjust oscilloscope sweep speed so that individual sample positions (bright spots in CRT trace) are discernable. (Approximately 0.5 millisecond/sweep.)
8. Decrease beam intensity until only the sample positions are shown in the sweep.
9. Calibrate the vertical and horizontal channels if necessary, (see calibration instructions), and/or set converter time base control as desired.
10. Apply test signal to signal input BNC connector.
    a. Free Running Case: Apply converter trigger output, properly attenuated and of correct polarity,

to test circuit. Note: The converter trigger output is a 30V positive pulse. Insert 50 nanosecond delay cable between test circuit output and converter signal input connectors, or between the converter trigger output and the test circuit.

b. Trigger Case: Connect test circuit output to the trigger input of the converter, using pulse transformer if necessary to give positive trigger voltage. Connect test circuit output to converter signal input connecter through a 50 nanosecond delay cable. Then turn the trigger sensitivity control until the converter is operating in the triggered mode (usually indicated by a change in number of sample positions) and then set for maximum level at which triggering will occur without the converter free running.

11. Vary oscilloscope sweep until number of samples is adequate to display a waveshape. (Decrease sweep speed to increase number of samples.)

12. Use converter controls for changing apparent sweep speed and horizontal position and use the oscilloscope's vertical amplifier sensitivity controls for varying the vertical position and sensitivity.

Calibration Procedure

A square wave generator may be used in calibrating both the horizontal and the vertical channels of the converter system. Follow the operating instructions to Step 9 and then proceed as shown below: (Note: Square wave repetition may be any value.)

1. Apparent Sweep Calibration -- apply a square wave of amplitude $\frac{V_{sweep\ max}}{n}$ ($\frac{150\ V}{n}$ for most Tektronix oscilloscopes) to the ramp terminals in place of the oscilloscope ramp signal. Then, using the horizontal input to the oscilloscope with the sweep disabled, measure the voltage across the calibrating resistor R_{10}. The time represented by the horizontal deflection, V_{hd}, is then $t = nkV_{hd}$ where $\frac{1}{k}$ equals the rate of rise of the fast ramp generator output. $\frac{1}{k} = \frac{dV_{fr}}{dt}$. Adjust R_{10} to the desired calibration.
2. Amplitude Calibration -- apply a square wave of known amplitude, less than 2V, to the signal input through cable connections as per Step 10 of operating proceedure, and adjust oscilloscope vertical channel calibration control as desired. The CRT display will consist of two horizontal lines of samples with

the vertical distance between them representing the square wave peak to peak amplitude.

Transistor Selection

The transistors selected for the avalanche circuits in the converter were commercial silicon 2N914 npn units. From a batch of 40 units tested, all showed the characteristic negative resistance avalanche region when the volt-ampere characteristics of the transistors with the base lead floating were displayed on a Tektronix transistor curve tracer, as per Figure 5. The units were then tested in a circuit similar to the trigger pulse generator of Figure 4 to determine the avalanche switching time using a Tektronix type N sampling plug-in unit. Twenty-one of the tested transistors had a switching time of two nanoseconds or less with the faster of these being less than one nanosecond on the 0.6 nanosecond risetime test oscilloscope. Subsequent testing indicated that most high frequency silicon transistors and a few low frequency units display the avalanche characteristic with switching times varying from less than one nanosecond to greater than 40 nanoseconds. These tests indicate that individual selection of the avalanche transistors is necessary, but that satisfactory units are readily available from commercial batches of transistors.

The transistor used in the blocking oscillator unblanking pulse generator does not need to be specially selected since the pulse width is relatively independent of the transistor's beta. The main requirements here are a switching time less than 0.2 microseconds and a collector breakdown voltage greater than 40 Volts.