AN ABSTRACT OF THE DISSERTATION OF

Zhenyong Zhang for the Degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 27, 2006.

Title: A Dual-Path 2-0 MASH ADC with Dual Digital Error Correction

Abstract approved:

_____

Gabor C. Temes

This dissertation presents a dual-path 2-0 MASH (Multi-stAge-noise - SHaping) ADC with two verified digital corrections of DAC mismatch error and quantization noise leakage. By using these two techniques, the requirements for the analog circuits are greatly relaxed. The dual-path structure generates two outputs, one only composed of conversion errors, the other input signal plus conversion errors. For the above two correlation algorithms, the input signal is the largest interference. Hence, the first output is suitable for a correlation operation, greatly speeding up the correlation based techniques, while the second serves as the final output after removal of the DAC error and quantization noise leakage.

The dissertation also proposes a new Dynamic Element Matching (DEM) technique, namely Segmented Data Weighted Averaging (SeDWA), for application

in a multi-bit Delta-Sigma Modulator (DSM). In SeDWA, the DAC elements are divided into several subsets with Data Weighted Averaging (DWA) applied in each set. This allows a simpler and faster implementation, and the selecting sequences for the DAC elements are more randomized than in conventional DWA. It reduces pattern tones, but still provides mismatch error shaping. In the simulated Power Spectra Density (PSD), no in-band pattern tones were observed, and only a moderate rise of the noise floor. Therefore, higher Spurious-Free Dynamic Range (SFDR) was achieved. The implementation of SeDWA can be simpler and faster than that of conventional DWA, making it suitable for high-speed applications.

To verify the first technique, an experimental dual-path 2-0 MASH DSM was built. The split structure allows fast convergence and improved accuracy for the correction. Using a 20 MHz clock, the prototype chip achieved an 84 dB dynamic range in a 1.25 MHz signal band, when fabricated in CMOS 0.18um process.

A Dual-Path 2-0 MASH ADC with Dual Digital Error Correction

by

Zhenyong Zhang

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of

the requirement for the

degree of

Doctor of Philosophy

Presented November 27, 2006

Commencement June 2007

Doctor of Philosophy dissertation of Zhenyong Zhang

presented on November 27, 2006

APPROVED:

_____

Major Professor, representing Electrical and Computer Engineering

_____

Director of School of Electrical Engineering and Computer Sciences

_____

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes of release of my dissertation to any reader upon request.

_____

Zhenyong Zhang, Author

ACKNOWLEDGEMENTS

Firstly I would like to express my sincere appreciation to Dr. Gabor C. Temes, my advisor. It is my honor and privilege to work under his supervision. I benefits so much from his advice both on the research and personal matters. He creates a comfortable research environment and lets me focus on the research I am interested in.

Also I would like to thank Prof. Un-Ku Moon, Prof. Huaping Liu, Prof. Albrecht Jander and Prof. Michael H. Scott for serving in my committee and giving lots of helpful advice on my Ph.D study.

I am grateful to Xuesheng Wang, Jose Silva, who helped me take a first stride in the research field of delta sigma modulators. I gained a lot from each conversation between them. They keep encouraging me even after their graduation.

I appreciate all my colleagues in analog group for the helpful discussion on the research and the happy time we spent together. They are Chris, Dave, Gil-cho, Jie, Jim, Jose Ceballos, Jose Silva, Josh, Kye-hyung, Merrick, Minfang, MinGyu, Pavan, Peter, Qingdong, Ruopeng, Sunwoo Sasidhar, Tawfig, Ting, Vova, Weilun, Wenhuan, Wonseok, Xuefeng , Xuesheng, Yan , Yoshio, Younjae, Yuhan, Zhimin, Zhiqing.

My early time in Corvallis would have been much tougher without help from Jipeng Li, Xuesheng Wang, Yuhua Guo and Ying Xiao. They helped me quickly settle down and adapt to the new life here.

I am indebted to the NS Lab from National Semiconductor, which offered the free fabrication of my chip. Dr. Jian-yi Wu, Massod Yousefi and Raj Subramoniam from National Lab reviewed my design and gave me lots of good comments on how to make chip work properly.

Finally, nothing can express my appreciation and love to my families, my parents Zhongqi Tang and Fengying Zhang, my younger brother Zhenqing Tang, and my girlfriend Jinjin He. They cared, supported and loved me unconditionally, encouraging me to go through hardship and enjoy the brightness of life.

TABLE OF CONTENTS

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES(Continued)

LIST OF FIGURES(Continued)

LIST OF TABLES

A Dual-Path 2-0 MASH ADC with Dual Digital Error Correction

Chapter 1 Introduction

1.1 Basics of Delta-Sigma ADC

ADCs (Analog-to-Digital-Converters) are the only bridges from the analog world to digital one, converting analog signal into digital one as shown in Fig.1-1. Here *err* defines the conversion errors, quantization error and devices noise, etc. Essentially, ADCs are divided between over-sampling and Nyquist-rate ADCs. Nyquist-rate ADCs are memoryless systems, converting the analog signal sample by sample. For over-sampling ADCs, delta-sigma and incremental ADC, their outputs depend on all previous input signals. The accuracy of Nyquist-rate ADC are more limited to the circuits performance, since all the error power caused by circuits imperfections falls into the signal band. But for over-sampling ADC, things get much better, usually the over-sampling nature makes only small part of the power of these errors fall into the signal band.

As shown in Fig.1-2 and Fig.1-3 respectively, if the conversion error is assumed to be additive white noise, for the PSD of Nyquist-rate ADC output, power of all conversion errors are evenly distributed in the signal band, while for the counterpart, only a small part.

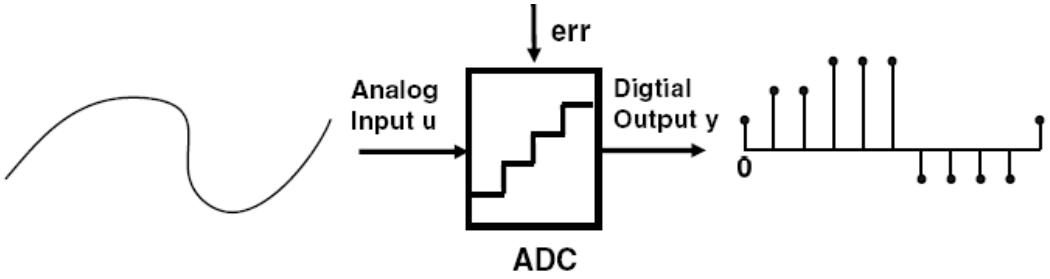

Fig.1-1 General principle of ADC

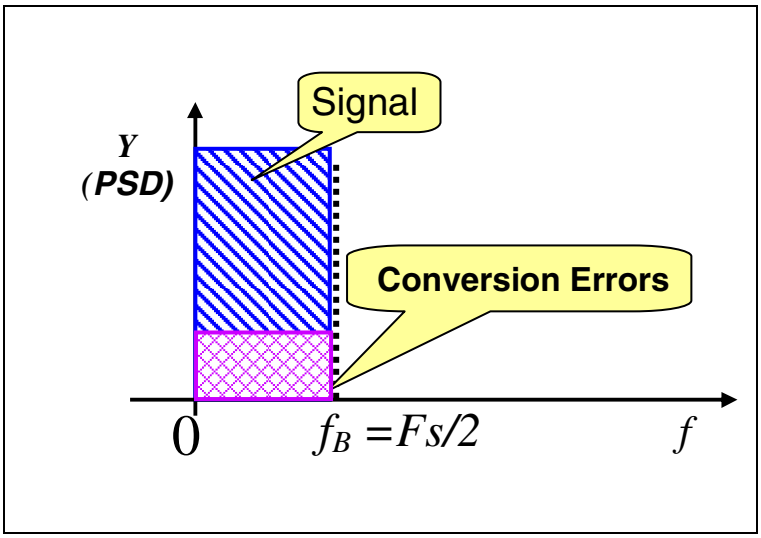

Fig.1-2 PSD of Nyquist-rate ADC

To remove the out-of-band conversion errors, post signal processing is needed in over-sampling ADC. To further reduce the power of conversion errors in the signal band , it is not difficult for researchers to think of noise shaping, filtering most power of evenly distributed conversion errors out of the signal band, as shown in Fig.1-4. The efficiency of noise shaping depends on the over- sampling

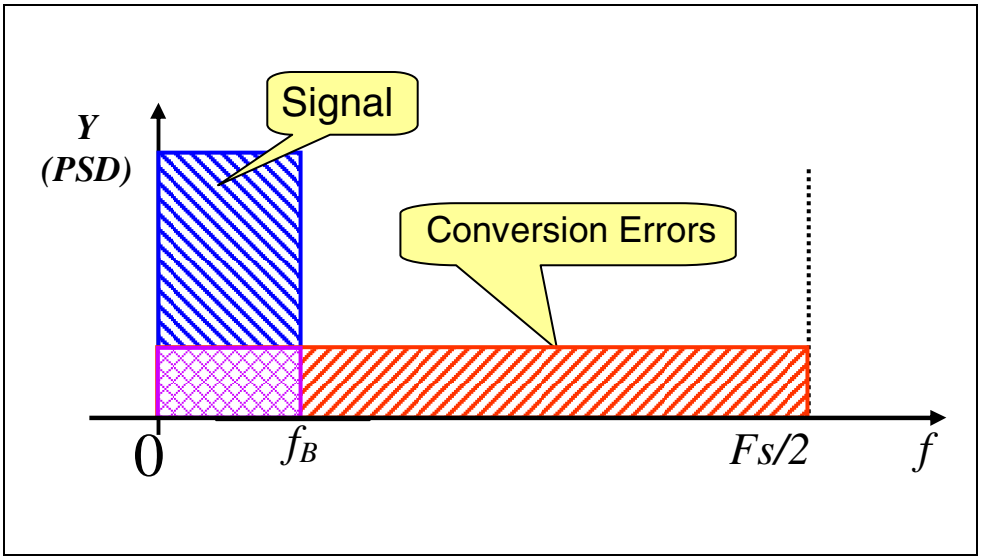

Fig.1-3 PSD of over-sampling ADC

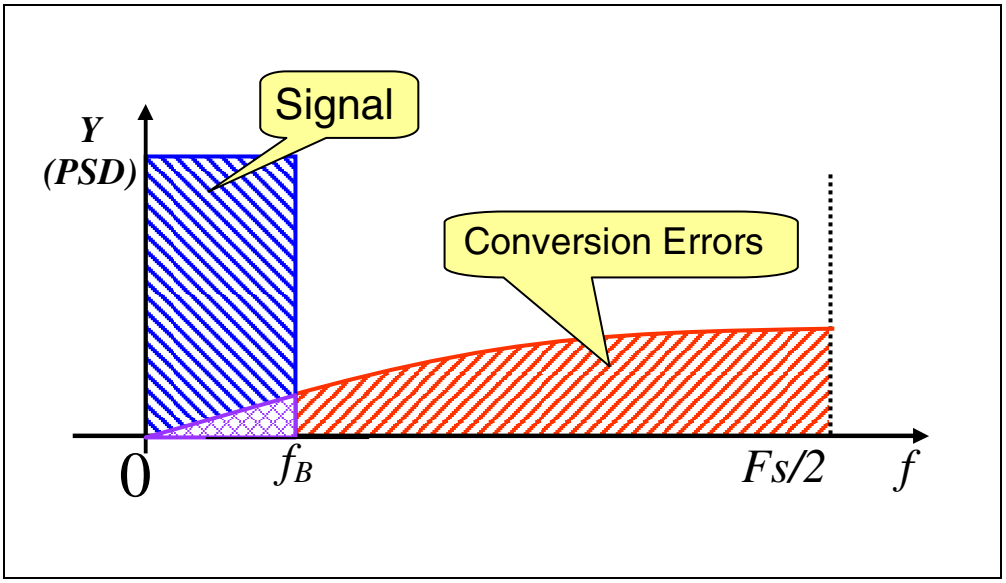

Fig.1-4 PSD of over-sampling ADC with noise shaping

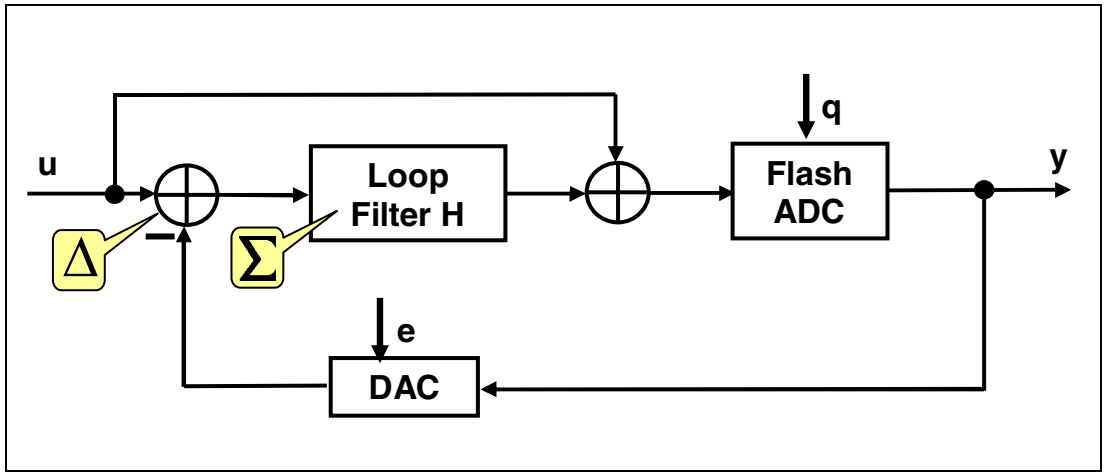

Fig.1-5 DSM in feed-forward structure

ratio (OSR) and shaping order. Since there are lots of error sources in the converters, it is impossible to design a converter with all noise sources high-pass filtered. Usually quantization error introduced by quantizer is the biggest one. It is desirable to find an over-sampling converter structure with a high-pass Noise Transfer Function (NTF) for quantization noise. Here comes the $\Delta\sum$ ADC. Fig.1-5 shows a DSM in a feed-forward structure. *u* represents the input signal, *q* quantization error, *e* DAC mismatch error if multi-bit DAC is used, as shown in Fig.1-6. If the loop filter is composed of one or more integrators with high gain at low frequency, it can be shown that the quantization noise is greatly attenuated by the gain of loop filter at low frequency. However, the input signal and DAC error aren't attenuated at low frequency. Hence, the NTF shows the character of high-pass, while Error Transfer Function (ETF) and Signal Transfer Function (STF) low-pass or all pass. Then the output of DSM can be written as:

$$Y = U \cdot STF + Q \cdot NTF + E \cdot ETF \tag{1-1}$$

NTF, ETF and STF are given by Eq.1-2—1-4 respectively:

$$NTF = 1/(1+H) \tag{1-2}$$

$$ETF = H/(1+H) \tag{1-3}$$

$$STF = (1+H)/(1+H) = 1 \tag{1-4}$$

1.2 Motivation

Wide-band high-accuracy ADCs have many applications in wireless and wireline communications systems. $\Delta\sum$ ADCs are very useful for such applications if they can provide at least 12-bit performance at OSR of 8 or less [1-1]--[1-3]. Because of low OSR, noise-shaping techniques become less effective. MASH structures with internal multi-bit quantization are typically used to suppress the quantization noise to the required level. MASH structures, however, are prone to quantization noise leakage. Nonlinear errors of DAC are also introduced if multi-bit quantization is applied. This nonlinear error is caused by the mismatch of different unit elements in the feedback DAC and it can't be attenuated by the loop filter, as shown in Eq.(1-3).

Techniques, such as trimming, DEM, digital correction, etc., are used to handle the problem of DAC error. Among them DEM techniques, DWA[1-4], BiDWA[1-3], ILA[1-5], etc., are most popular, shaping most power of DAC mismatch error out of signal band. Like the shaping of quantization noise, DEM becomes less effective in the low-OSR DSM. In [1-6], a digital technique was proposed and verified for the digital correction of DAC error, and its efficiency is independent of OSR, hence suitable for low-OSR (wide-band) DSMs.

The quantization noise leakage in MASH ADCs also can be compensated through a similar digital correction technique [1-7]. Therefore the digital correction technique is suitable for the low-OSR wide-band DSM.

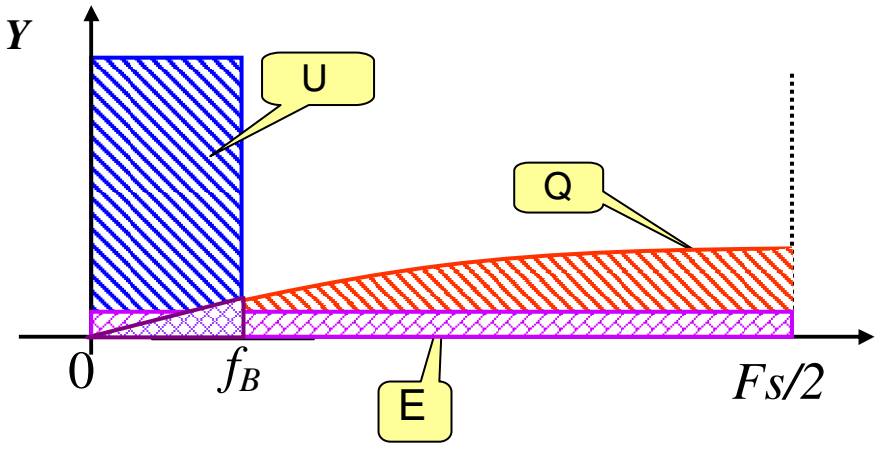

Fig.1-6 PSD of $\Delta\sum$ ADC with DAC mismatch error

1.3 Contribution of this work

This thesis proposes a new family of dual-path DSMs [1-8], suitable for digital DAC error correction presented in [1-6]. A dual-path switched-capacitor (SC) 2-0 MASH DSM with the similar structure in [1-9] was finally implemented to improve the efficiency of two digital correction techniques, digital corrections of DAC error [1-6] and quantization noise leakage [1-7]. The basic idea is to build two DSMs, combine their outputs into such a way, one used for speeding up digital correction, the other for the final output after removing quantization noise leakage and DAC nonlinear errors. A prototype chip was designed to prove the efficiency of this structure. It was fabricated in National 0.18um CMOS process. After turning on the digital correction, around 10dB improvement of Signal-to-Noise-and-Distortion Ratio (SNDR) can be reached. 14 bit dynamic range was achieved in a 1.25MHz signal band with OSR of 8.

A modified DWA technique, SeDWA is also proposed. It solves the problem of pattern tones generated in the output of DSM with DWA technique. By using SeDWA, DAC selecting sequences are more randomized, therefore pattern tones are broken into noise. However, it still keeps the benefit of error shaping. The implementation of SeDWA is also discussed. It can be simpler than that of DWA, hence faster operation is possible, making it suitable for the high-speed DSM.

1.4 Structure of thesis

Chapter 2 gives the background of these two correlation-based digital correction techniques. The algorithms are described. The factors affecting the convergence speed and accuracy of the correction algorithms are analyzed.

Chapter 3 introduces dual-path DSM. It is suitable for correlation based digital correction. One of them is especially efficient for digital DAC error correction. The possible implementations are also discussed.

Chapter 4 presents the system level design of a dual-path 2-0 MASH DSM. Most emphasis is laid on the noise budget and dynamic scaling.

Chapter 5 goes deep into discussion about each analog block in the prototype chip.

Chapter 6 proposes a Segmented DWA technique. The algorithm is presented. Its advantage over conventional DWA and implementation are discussed.

Chapter 7 summarizes the whole thesis.

Chapter 2 Correlation – based digital correction techniques for DSM

Correlation-based digital correction techniques have been used in pipelined , algorithmic/cyclic or $\Delta\sum$ ADC for the calibration of circuits non-idealities, such as device mismatch and finite opamp DC gain, [2-1], [1-9],[1-6]. These techniques can be run in the background, hence will not interrupt the normal ADCs' operation. Because of the calibration, high performance can be achieved with relaxed requirements of analog circuits. The basic idea is as follows: small errors caused by mismatch or finite opamp DC gain are modulated on some pseudo-random sequences, then processed in the analog circuits, finally converted to digital outputs along with the input signal. These peudo-random sequences are only correlated with the modulated error sequences, uncorrelated with other components in the digital output, therefore static or slow-varying small errors can be detected by taking correlation calculation between these random sequences and digital outputs. To improve the accuracy of correlation, these random sequences are filtered by a digital filter emulating the signal path of error sequences processed in the analog circuits.

In this chapter, two correlation-based digital correction techniques will be discussed, digital corrections of DAC error and quantization noise leakage in MASH DSM.

2.1 Digital DAC error correction

2.1.1 Overview of solutions to DAC mismatch error

In a multi-bit DSM, because of mismatch of DAC unit elements, the analog output of each digital code deviates from the ideal one. As shown in Fig.(2-1), here the most positive and negative analog output level define the Full Scale (FS) of DAC output. The analog output level corresponding to digital code "0" is defined as offset. After removing the offset error, the slope of the straight line connecting the two full-scale points, defined as the gain of DAC, ideally should be "1". In practical circuits, any slope deviation from "1" is defined as gain error. The gain and offset errors usually don't cause big problems in the system using DSM. After removing the offset and gain error, in the ideal case, all the analog output levels should fall on the straight line connecting the two full-scale points. The deviation of any analog output level from this line is defined as DAC error. For single-bit DAC, since there are only two analog output levels, it is always linear. But for the multi-bit DAC, because of mismatch between each unit element, except for the

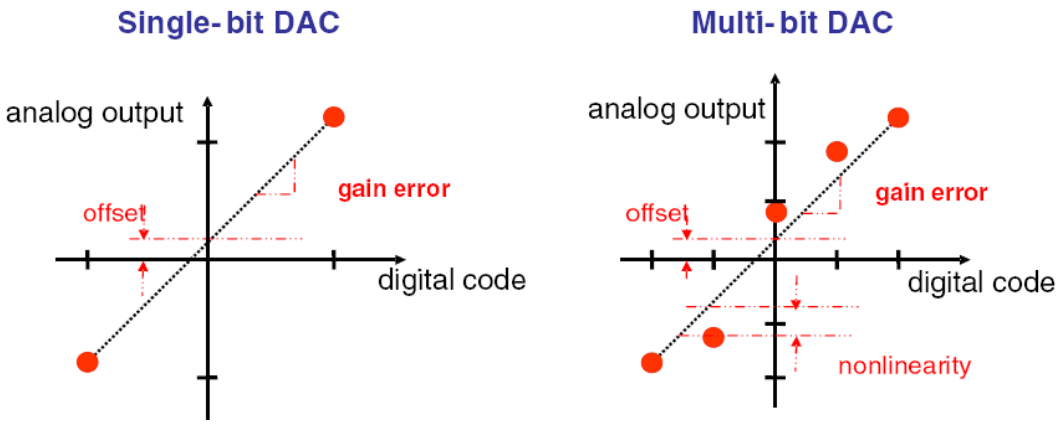

Fig.2-1 DAC error definition

most positive and negative analog output, all the others are error contaminated. In the DSM, DAC mismatch errors can't be attenuated by loop filter, Eq.(1-3). If DAC selecting sequences are not scrambled before applied on the DAC units, the DAC errors are modulated on the signal dependent selecting sequences, generating harmonics, greatly reducing the linear performance. There are several solutions to this problem.

A. Trimming or analog calibrating the unit elements to improve the matching accuracy. It increases the fabrication cost or circuit complexity.

B. Dynamic element matching (DEM)

It is a very efficient way in high OSR DSM. If simple randomization is used, DAC errors are modulated on randomized selecting sequences, the signal dependent tones are broken into noise. Furthermore, if the selecting sequences are randomized and high-pass filtered, using DWA [1-4], BiDWA[1-3], ILA[1-5], SDWA[2-2], FPDWA [2-3], etc., then the DAC error power is filtered out of the signal band, Fig.2-2. Like quantization noise shaping, its efficiency depends on the OSR and shaping order. In the low OSR case, these techniques become less effective. In some simple DEM algorithm, such as DWA, pattern tones are generated, limiting the linear performance of DSM.

C. Digital error correction

It extracts the static error of each unit element through a correlation-based technique, then removes them from the final output. The correction performance depends on the algorithm, how accurately the estimated errors can be achieved. Its efficiency is independent of OSR, thus suitable for the low-OSR (wide-band) and high-accuracy DSM.

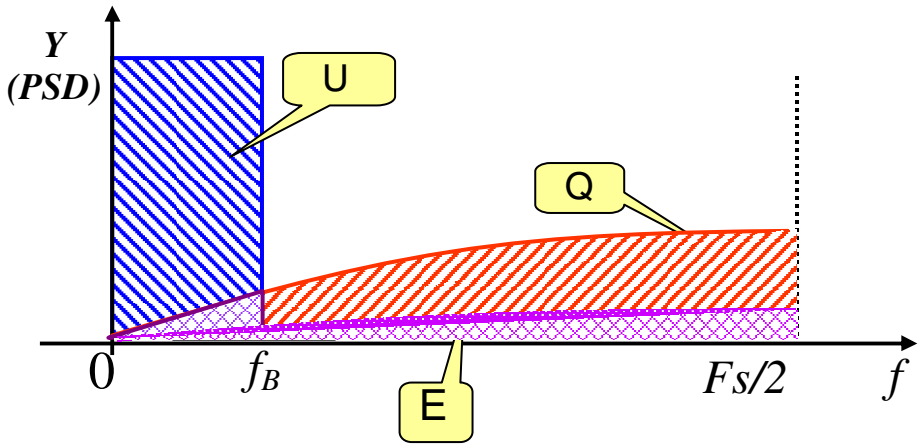

Fig.2-2 PSD of DSM with DAC error shaping

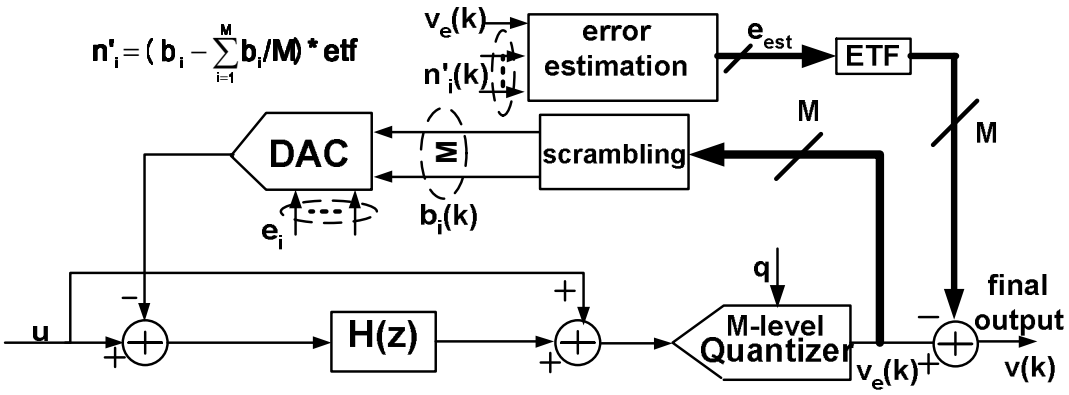

Fig.2-3 Digital DAC error correction

2.1.2 Algorithm of digital DAC error correction

In thermometer-coded DAC, its error is composed of the summation of the unit element errors modulated by their selecting sequences, whose values can be zero or one. Fig.2-3 shows the digital DAC correction technique [2-4] applied to a feed-forward DSM. Here M is the number of unit elements in the DAC, e_i defines the error of ith DAC unit, e_{est} are the estimated error of each DAC unit, $v_e(k)$ is the DSM output, composed of filtered version of signal u, quantization noise q and summation of DAC unit error e_i, Eq.2-1. Here asterisk "*" defines the convolution operation.

$$v_e(k) = u * stf + q * ntf + \sum_{i=1}^{M} b_i e_i * etf \qquad (2\text{-}1)$$

By randomizing the connections between M quantizer outputs and DAC inputs, the selecting sequence of i th unit element $b_i(k)$ is less correlated with input signal u and quantization noise q. To further weaken the correlation between each DAC selecting sequence and quanizer output, we remove the parts in $b_i(k)$ which is correlated with quantizer output. Because the summation of all DAC selecting codes $b_i(k)$ is same as summation of all quanitizer output bits. In Eq. 2-2, Δ is the ideal analog interval between adjacent DAC output levels. For simplification, Δ is assumed to be "1".

$$\sum_{i=1}^{M} b_i(k) = v_e(k)/\Delta + M/2 \tag{2-2}$$

After the randomization of DAC selecting sequences, the correlation between selecting sequence of each DAC unit and quantizer output should be same, 1/M. Hence, $b_i(k)$ is modified to $n_i(k)$:

$$n_i(k) = b_i(k) - \sum_{i=1}^{M} b_i(k)/M \tag{2-3}$$

$n_i(k)$ is uncorrelated with quantizer output, input signal and quantization error, but correlated with the DAC error sequences. Based on Eq.2-3, the summation of DAC unit error at time instant of k can be rewritten as:

$$\sum_{i=1}^{M} b_i(k)e_i = \sum_{i=1}^{M} n_i(k)e_i + \frac{\sum_{i=1}^{M} b_i(k)}{M} \sum_{i=1}^{M} e_i \tag{2-4}$$

Given in Fig.2-1, full-scale analog outputs are assumed to be error free. The summation of total units error is zero:

$$\sum_{i=1}^{M} e_i = 0 \tag{2-5}$$

Eq.2-4 can be simplified as:

$$\sum_{i=1}^{M} b_i(k)e_i = \sum_{i=1}^{M} n_i(k)e_i \tag{2-6}$$

Since the DAC selecting sequences $b_i(k)$ are filtered by ETF in the analog domain, the pre-known sequence $n_i(k)$ should also be filtered by ETF in the digital domain, emulating the analog path of the DAC error sequences in the DSM, before being correlated with the final digital outputs $v_e(k)$. Hence $n_i(k)$ is modified to $n'_i(k)$:

$$n'_i(k) = n_i(k) * etf \tag{2-7}$$

The operation of correlation is defined as:

$$Corr(v_e(k), n'_i(k)) = \frac{\sum_{k=0}^{N-1} v_e(k) \cdot n'_i(k)}{\sum_{k=0}^{N-1} n'^2_i(k)} \tag{2-8}$$

N is the data length for the correlation operation. If no device noises are included, the correlation between $n'_i(k)$ and $v_e(k)$ can be written as:

$$Corr(v_e(k), n'_i(k)) = Corr(u * stf + q * ntf + \sum_{i=1}^{M} b_i e_i * etf, n_i(k) * etf) \quad (2\text{-}9)$$

Since the correlations between the $n'_i(k)$ and filtered versions of input signal u and quantization noise q are both equal to zero, Eq.2-9 is simplified as:

$$Corr(v_e(k), n'_i(k)) = Corr(\sum_{i=1}^{M} b_i e_i * etf, n_i(k) * etf) \quad (2\text{-}10)$$

If we combine Eq.(2-6), (2-7) and (2-10), we get

$$Corr(v_e(k), n'_i(k)) = Corr(\sum_{i=1}^{M} n'_i e_i, n'_i(k)) \quad (2\text{-}11)$$

$$Corr(v_e(k), n'_i(k)) = Corr(\sum_{j \neq i}^{M} n'_j e_j, n'_i(k)) + Corr(n'_i(k) e_i, n'_i(k)) \quad (2\text{-}12)$$

From Eq.2-3, we derive

$$\sum_{i=1}^{M} n_i(k) = \sum_{i=1}^{M} (b_i(k) - \sum_{i=1}^{M} b_i(k)/M) = 0 \quad (2\text{-}13)$$

$$n_i(k) = -\sum_{j \neq i}^{M} n_j(k) \tag{2-14a}$$

$$n'_i(k) = -\sum_{j \neq i}^{M} n'_j(k) \tag{2-14b}$$

Thanks to the randomization of selecting sequence, the correlation between $n'_i(k)$ and any other $n'_j(k), _{j \neq i}$ should be the same:

$$Corr(n'_{j, j \neq i}(k), n'_i(k)) = -\frac{1}{M-1} \tag{2-15}$$

Substituting Eq.2-15 into Eq.2-12, we get:

$$Corr(v_e(k), n'_i(k)) = -\frac{1}{M-1}\sum_{j \neq i}^{M} e_j + e_i \tag{2-16}$$

From Eq.9, we know:

$$\sum_{j \neq i}^{M} e_j = -e_i \tag{2-17}$$

The final correlation results can be obtained:

$$Corr(v_e(k), n'_i(k)) = \frac{M}{M-1} e_i \tag{2-18a}$$

$$e_i = \frac{M-1}{M} Corr(v_e(k), n'_i(k)) \tag{2-18b}$$

For the correlation process, the DAC error sequences are the signals of interest, all the others are interferences .Among them, input signal u is the biggest one, reducing the speed of convergence and accuracy of final correlation results. It should be filtered out or removed to improve the efficiency of correlation.

2.2 Digital correction of quantization noise leakage in MASH

MASH structures with multi-bit internal quantizer are often used in the design of wideband and high-accuracy DSM, because it is free of instability if the order of loop filter is less than 2 in each stage. In the low OSR DSM, less improvement of Signal to Quantization Noise Ratio (SQNR) is obtained by increasing the order of noise shaping. Quantizer with high internal resolution should be used for lower quanization noise power. Limited by the circuit complexity and power consumption, the internal quantizer in DSM is always limited to 6 bit. But in a 2-0 MASH, a pipeline ADC can be used at the second stage. A 10-bit accuracy pipeline ADC is not a very challenging design using

current technology. Hence high-accuracy can still be achieved even with OSR less than 8 in MASH structure.

However, there is a predominant problem limiting the performance of MASH: quantization noise leakage. In MASH, the quanization noise except the one in the final stage is processed in two signal paths, one is mostly in the analog domain, the other is mostly digital. Ideally, the quanization noise processed in these two paths are cancelled at the final output. (in Fig.2-4, q1 is filtered by Analog NTF (ANTF) in the first stage and Digital NTF (DNTF) at the second stage , ideally they should be same. If these two paths don't match well, leakage of quantization noise occurs at the final output with great decrease of SQNR.

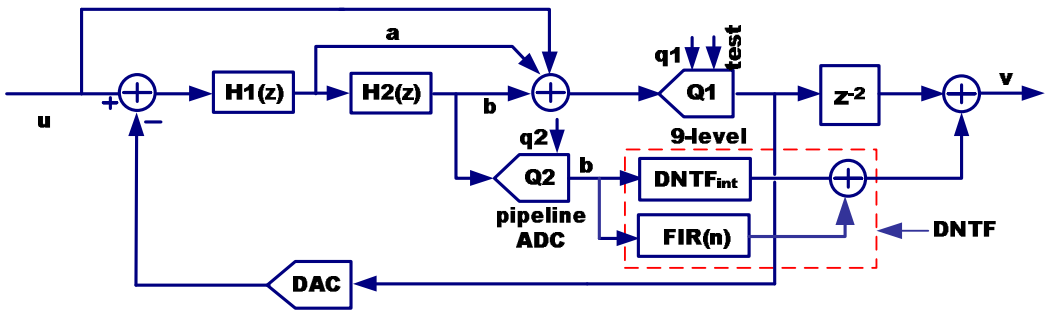

Fig.2-4 2-0 MASH structure

There are two ways to handle the problem. One is to use high performance analog circuits, such as opamps with high DC gain, making the ANTF exactly same as the initial NTF we want to design. The other is to tolerate the deviation of ANTF from the initial DNTF, but tuning the DNTF to be exactly same as ANTF.

Obviously, the second solution can be much cheaper, since it is realized in the digital domain.

A feed-forward 2-0 MASH DSM is shown in Fig.2-4. The first stage is a 2nd order DSM, while the second stage is a pipelined ADC. To simplify analysis, the pipeline ADC is modeled as a quantizer with zero delay. Silva structure [2-5] is used in 1st stage, which relaxes the linearity requirement of the integrators. Because only the conversion errors are processed by the integrators, the nonlinearity of integrators only causes the increase of noise floor instead of the distortion of input signal u. Here $H_1(z), H_2(z)$ represent the models of 1st and 2nd non-inverting delaying integrators, Fig.2-5. In the ideal case, proper selection of *a*, *b* and integrator gains can make NTF exactly same as Eq.2-19. Considering the effects of finite DC gain and integrator gain mismatch, the model of a non-inverting delaying SC integrator can be written as Eq.2-20, [2-6]:

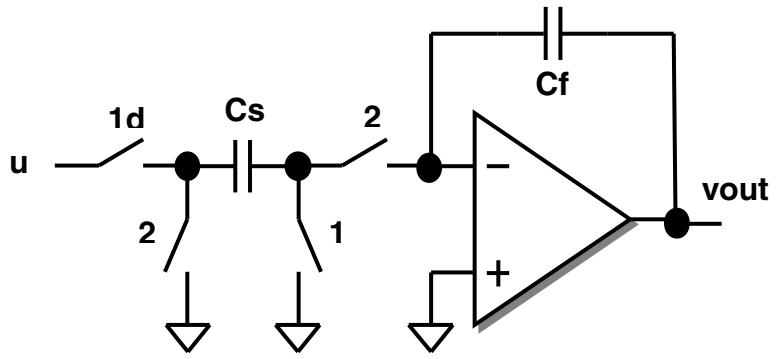

Fig.2-5 Non-inverting delaying SC integrator

$$DNTF_{int} = (1 - z^{-1})^2 \tag{2-19}$$

$$H(z) = \frac{c(1-\alpha)z^{-1}}{1-(1-\beta)z^{-1}} \tag{2-20}$$

c is the integrator gain (C_s / C_f), and A is the DC gain of the opamp. The gain error α and the pole displacement β are expressed as:

$$\alpha = (1 + c) / A \tag{2-21a}$$

$$\beta = c / A \tag{2-21b}$$

Based on the linear models in Fig.2-6, [2-5] gives the detailed analysis for the adaptive filtering algorithm. To cancel the quantization noise *q1* at the final output *v*, the DNTF should be same as ANTF:

$$ANTF = \frac{[1-(2-\beta_1-\beta_2)z^{-1}+(1-\beta_1)(1-\beta_2)z^{-2}]}{[bc_1c_2(1-\alpha_1)(1-\alpha_2)]} \tag{2-22}$$

Eq.2-22 can be written in a more general form:

$$ANTF = (1+l_0) - (2+l_1)z^{-1} + (1+l_2)z^{-2} \tag{2-23a}$$

The initial setup of $DNTF_{int}$ is :

$$DNTF_{int} = (1 - z^{-1})^2 \tag{2-23b}$$

$$ANTF - DNTF_{int} = l_0 - l_1 z^{-1} + l_2 z^{-2} \tag{2-23c}$$

Eq.2-23c indicates the deviation of initial setup of DNTF from the real ANTF, which causes leakage of noise. To compensate it, an adaptive FIR should be used:

$$FIR(n) = ANTF - DNTF_{int} \tag{2-24a}$$

FIR (n) is a 2nd order filter:

$$FIR(n) = l_0(n) - l_1(n) z^{-1} + l_2(n) z^{-2} \tag{2-24b}$$

Taking the quantization noise leakage into account, NTF of *q1* in Fig.2-4 should be a IIR, which can be approximated as a FIR in terms of Taylor series:

$$NTF_{leak} = \sum_{i=0}^{\infty} l_i z^{-(i+2)} \tag{2-25}$$

Further analysis reveals that if only considering the first-order effect caused by the integrators gain mismatch and opamp finite DC gain, the leakage Transfer Function (TF) of *q1* can be approximated by:

$$NTF_{leak} = l_0(n)z^{-2} - l_1(n)z^{-3} + l_2(n)z^{-4} \tag{2-26}$$

It can be proved that in NTF_{leak}, all the polynomial terms higher than z^{-5} can be neglected. Although only a 2-0 MASH is taken an example here, the above analysis can be applied to any MASH DSM using the Silva structure.

If a pseudo-random "test" sequence is injected at the input of quantizer, Fig.2-4, it will have the same signal path of quantzation noise *q1*. And the cancellation of "test" signal at the final output indicates the cancellation of the quantization noise *q1*. Since the injected pseudo -random "test" signal is uncorrelated with the input signal *u* and conversion errors (quantization noise, DAC errors, device noises), the coefficients of NTF_{leak} can be directly achieved by correlating the "test" signal and final MASH output:

$$l_0(n) + e_1 = Corr(v_i, test_{i-2}) \tag{2-27a}$$

$$-l_1(n) + e_2 = Corr(v_i, test_{i-3}) \tag{2-27b}$$

$$l_2(n) + e_3 = Corr(v_i, test_{i-4}) \tag{2-27c}$$

e_1, e_2, e_3 are the difference between ideal correlation results and practical ones. The first order effect of quantization leakage at instant n can be compensated by adjusting l_0 (n), l_1 (n), l_2 (n) based on the correlation results of Eq.2-27a,b,c. At instant n+1, based on the new correlation results, l_0 (n), l_1 (n), l_2 (n) are updated.

$$l_0(n+1) = l_0(n) + (-l_0(n) + e_1) \tag{2-28a}$$

$$l_1(n+1) = l_1(n) + (-l_1(n) + e_2) \tag{2-28b}$$

$$l_2(n+1) = l_2(n) + (-l_2(n) + e_3) \tag{2-28c}$$

The accuracy and convergence time of the correlation process depends on how many data points collected for correlation operation and the power of interferences, the conversion errors and input signal. Input signal is the biggest interference and its power is much larger than the injected “test” signal. Hence in [1-7], long time is needed for the convergence of correlation-based Sign-Sign-Block-Least-Mean-Square (SSBLMS) algorithm. However, the performance of the correlation process can be greatly improved by removing or filtering out input signal u before correlation operation.

Chapter 3 Dual-path DSM for speeding up correlation-based digital correction

For the correlation-based digital correction, the accuracy and speed of correlation operation are greatly dependent on the power ratio of signal of interest over the interferences. The input signal u is the largest interference. It greatly slows the converging process. In [2-1], DAC Noise Cancellation (DNC) technique was simulated with a large input signal. 2^{25} data points were needed to estimate the DAC noise error as accurate as 14 bit. While in [1-7], after around 2^{30} clock cycles (6000 adaptive steps, each achieved with a correlation block of 2^{16}), the quantization noise leakage was estimated and corrected to a satisfactory extent. Finally the DSM achieved 14 bit accuracy.

To speed up the convergence, several ways can be used. One is power-up calibration. Before the normal operation of DSM, with zero amplitude input signal applied, digital correction is carried out to extract the linear errors caused by the analog non-ideality. Then the errors are stored and removed from the final outputs. The second way is to generate another digital output suitable for the correlation operation. For example, before the correlation, the DSM output is high-pass filtered with most of the in-band input signal u attenuated. The third way is to devise a new DSM structure with two outputs, one is for correlation purpose, the other for DSM final output after removing extracted error.

In this chapter, a third solution will be presented. The dual-path DSM structures, both in configuration of single loop and MASH will be discussed. Some of them are especially suitable for the DAC error correction.

3.1 Dual-path single-loop DSM for fast digital DAC error correction

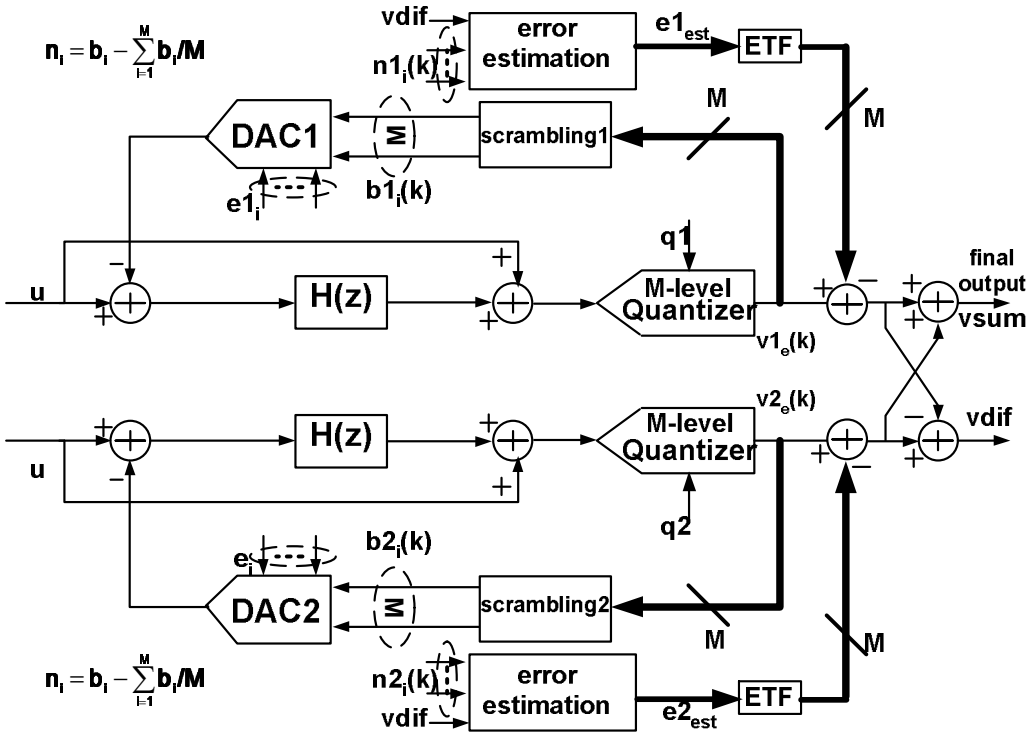

Fig.3-1 Basic dual-path DSM

As discussed above, for the correlation between the DAC selecting sequences and DSM output, if the input signal and quantization noise at the DSM output can be removed, more efficient correction operation can be achieved. In a sense, a DSM topology based on dual-path signal processing is generated in Fig.3-

1. The input signal *u* is entered into two same DSMs, and the two output signals are combined in such a way, one output *vsum* contains the input signal as well as the conversion errors (quantization noise, DAC error), while the other *vdif* only the error signals. The latter ("error output") is suitable for the extraction of the DAC errors using a digital correlation algorithm, since it is not dominated by the input signal. Assuming the two DSMs to be exactly same, before the correction process is turned on, the two outputs vsum , vdif can be expressed as Eq.(3-1) and (3-2) individually:

$$vsum = 2u * stf + (q1 + q2) * ntf + (\sum_{i=1}^{M} b1_i e1_i + \sum_{i=1}^{M} b2_i e2_i) * etf \qquad (3\text{-}1)$$

$$vdif = (q1 - q2) * ntf + (\sum_{i=1}^{M} b1_i e1_i - \sum_{i=1}^{M} b2_i e2_i) * etf \qquad (3\text{-}2)$$

Eq.(3-2) shows the input signal *u* is cancelled at vdif, hence vdif is suitable for the correlation process. It seems that hardware and power consumption is doubled, compared with a basic single path structure. Actually, shown in Eq.(3-1) ,the signal power is four time larger ,while the noise and DAC error power is only doubled. 3dB improvement of Signal-to-Noise Ratio (SNR) can be gained, which can compensate the increased noise floor, if all the capacitor size and opamps are half sized.

However, the two DSMs are not necessarily identical. In dual-path DSMs, what we are seeking is two outputs. One has less interference to correlation

process, the other contains the undistorted signal component with fewest noises and DAC errors. A new structure in Fig.3-2 results,[1-8]. There are two delta-sigma loops in this structure. One is composed of $H1, H2, Q1, DAC11, DAC21,$ $scrambling1, scrambling2$, while the other is composed of $H1, Q2, DAC3$. The former is a high-order DSM, while the latter is a low-order one. $H1, H2$ are different loop filters. Both loops are realized in differential structures. The input signal u and quantization noise *q2* are cancelled at vdif .In the z-domain (capital symbols), *vdif* ,*vsum* ,*d* can be expressed as:

$$Vsum = U - \frac{H1H2}{1+2H1H2}(E1+E2) + \frac{Q1}{1+2H1H2} \tag{3-3}$$

$$Vdif = \frac{H1}{1+2H1}(E2-E1) + \frac{Q2}{1+2H1} - \frac{2H1}{1+2H1}E3 \tag{3-4}$$

$$D = \frac{H1}{1+2H1}(E2-E1) - \frac{2H1}{1+2H1}Q2 - \frac{2H1}{1+2H1}E3 \tag{3-5}$$

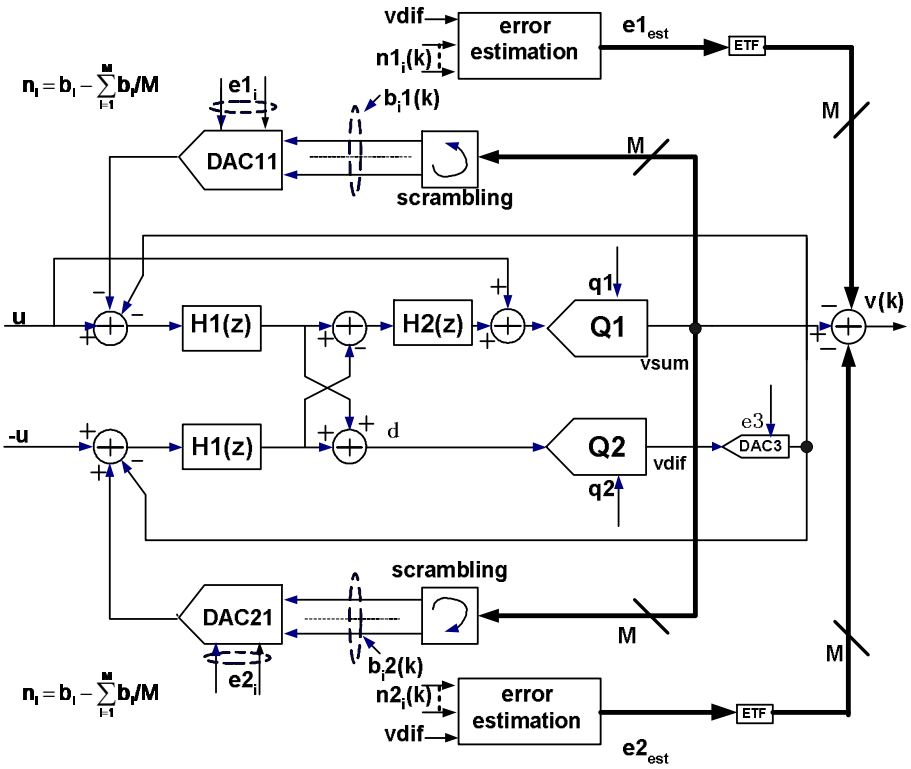

Fig.3-2 Modified dual-path DSM

vsum contains the input signal u, high-order shaped quantization noise *q1*. Compared with conventional single -path DSM structure, the SNDR deterioration will be caused by the inclusion of the DAC error *e2*, however, it will be finally corrected, and hence , is not a serious problem.

Signal *vdif* only contains the DAC error, $e1, e2, e3$ and shaped quantization noise *q2*. The input signal *u* and quantization noise *q1* have been cancelled here. Moreover, the quantizer Q2 only handles the DAC error and its own quantization error, its full scale can be very small, so does its quantization noise *q2*, which is

much smaller than *q1*, therefore, *vdif* is suitable for the correlation-based DAC error correction.

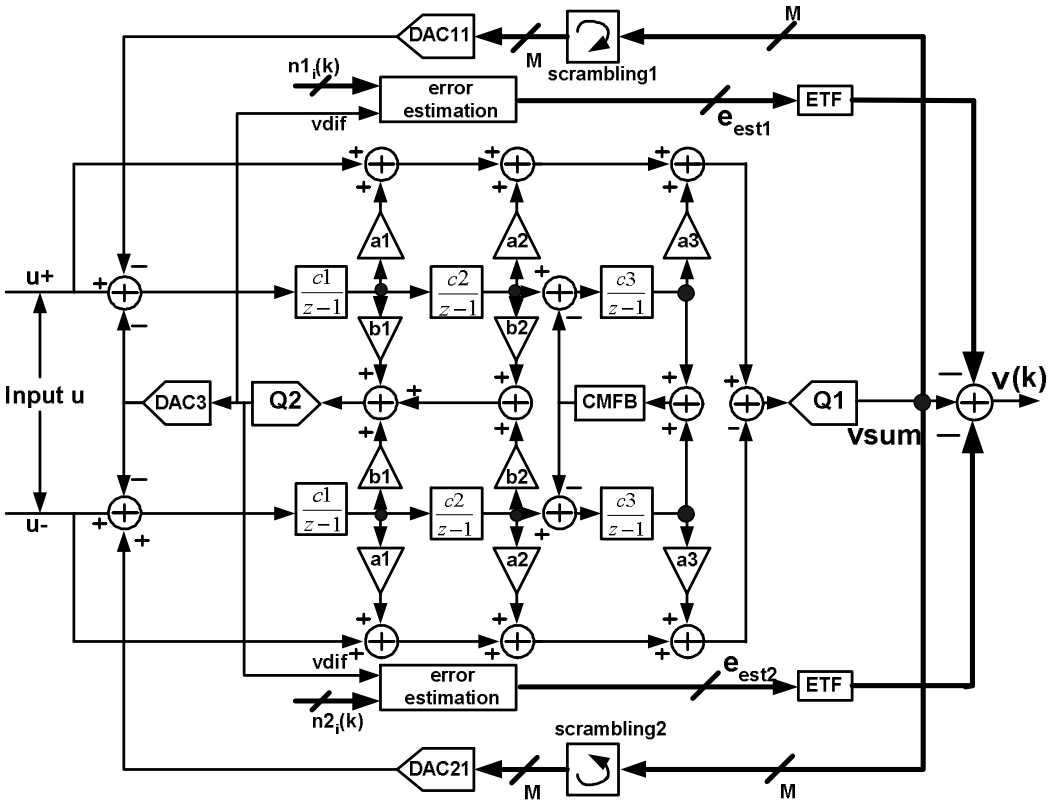

Fig.3-3 Circuit implementation of dual-path DSM

The generic circuit implementation of Fig.3-2 can be much simpler than the diagram if it is realized in a differential structure. The two delta-sigma loop needn't be implemented independently. They can be combined into one DSM structure. An example is shown in Fig.3-3, where the dual-path DSM is composed of one 3rd-order DSM (DSM1) and one 2nd-order DSM (DSM2). Here, $H1$ is

constructed from the first four integrators with coefficients $c1$ and $c2$, while $H2$ is realized by the fifth and sixth ones, with coefficient $c3$. The Common-Mode (CM) outputs of the $H1$ integrators are used to generate vdif, and hence no CM feed-back is used in these stages. The $H2$ integrators use CM feedback and conventional fully-differential circuitry. With different feed-forward coefficients, $b1$, $b2$, the implemented NTF and STF of DSM2 can be independent of those of DSM1. The optimum STF, NTF in DSM2 is designed for the maximum power ratio of DAC errors over quantization noise *q2*. The CM signals (errors of three DACs , $e1$, $e2$, $e3$, quantization noise *q2*) and differential signals (input signal u, errors of DAC11, DAC22, quantization noise *q1*) are both processed in the first two stages, while in third stage, only the differential signals are processed, the CM signal is suppressed by the Common-Mode-FeedBack (CMFB) circuitry. The simulation results are based on the prototype model shown in Fig.3-3. Here the quantizer Q1 has 9 levels, Q2 has 3 levels. Hence DAC11 and DAC21 contain 8 unit elements, while DAC3 has 2 unit elements. Fig.3-4 shows some simulated output spectrum, under the following conditions: for DAC11, DAC21 unit element mismatch error of 0.5%; for DAC3 unit element mismatch error of 1%; OSR = 32; input sine-wave frequency of fs/128, amplitude of -6 dBFS. The correlation was carried out in blocks ("rounds") of 2^{-12} clock periods each. The top curve shows the output spectra without correction, while the bottom ones after 6 rounds of correction. Clearly, 6 rounds of correction is sufficient to reduce the DAC error effects to negligible values, and hence achieve an SDNR close to the ideal value

(here, 87.65 dB).For comparison, a conventional single-path DSM with the same structure was designed and simulated. Under the same simulation conditions, DAC error correction process doesn't converge, even with a high-pass filter applied on the DSM output to reduce the interference from input signal u to correlation operation. The reduction of the residual errors of 8 unit elements in DAC11 during the iteration is illustrated in Fig.3-5.

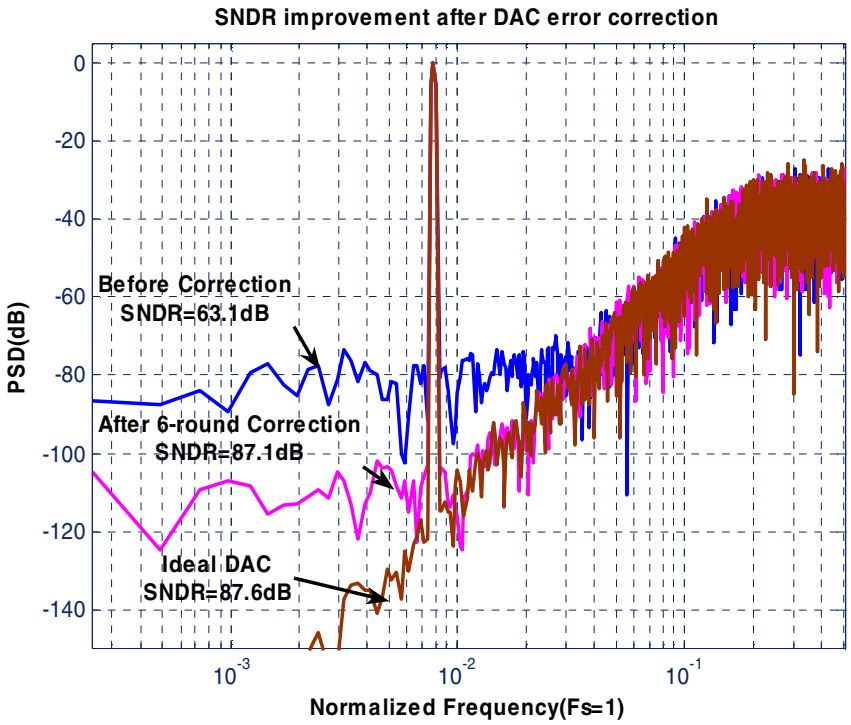

Fig.3-4. SNR improvement after DAC correction

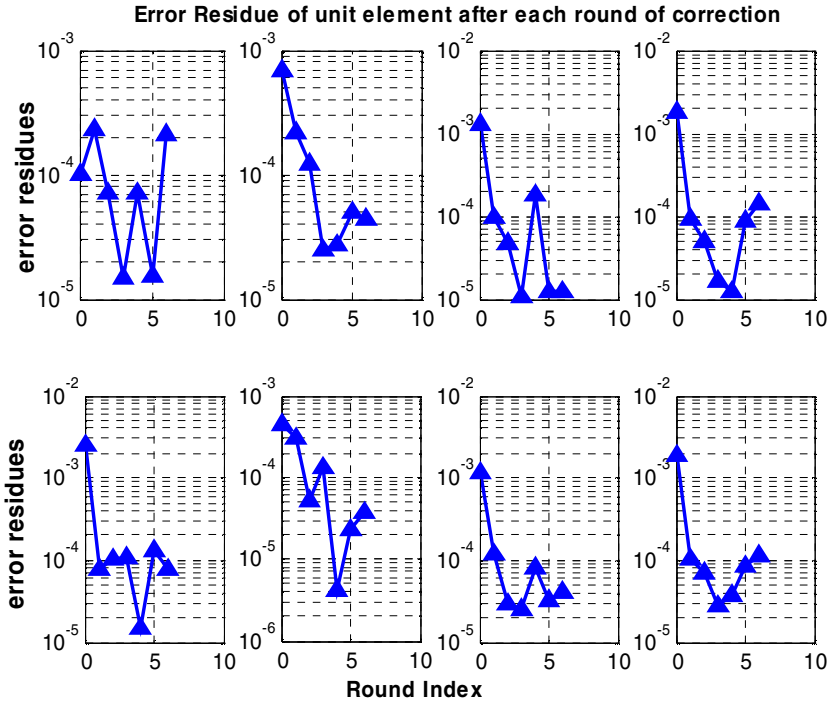

Fig.3-5. Error residues of DAC11 after 6-round correction

3.2 Dual-path MASH DSM for fast digital error corrections

The dual-path single loop structure shown in Fig.3-1 can be easily extended to MASH structure (Fig.3-6), using two identical MASH DSM and combining their outputs in the same way, one is subtracted version (*vdif*) for correlation purpose, the other (*vsum*)for final output. In the ideal case, only the conversion errors exist in *vdif*, including 1st stage quantization noise leakage, 2nd stage quanization noises, devices noises and DAC mismatch errors. Since the input signal is the largest interference for both digital corrections and it is cancelled in *vdif* , the correlation operation is faster. Compared with Fig.3-1, even faster

convergence can be obtained here. In Fig.3-1, after removal of input signal, quantization noise *q1* still exist in vdif. While in Fig.3-6, only the quantization noise leakage of 1st stage and quantization noise of 2nd stage, which is usually much smaller than that in Fig.3-1, thus less interferences for the correlation operation. Because in low OSR MASH, usually high-accuracy quantization is designed in the 2nd stage to compensate less attenuation of quantization noise in the signal band.

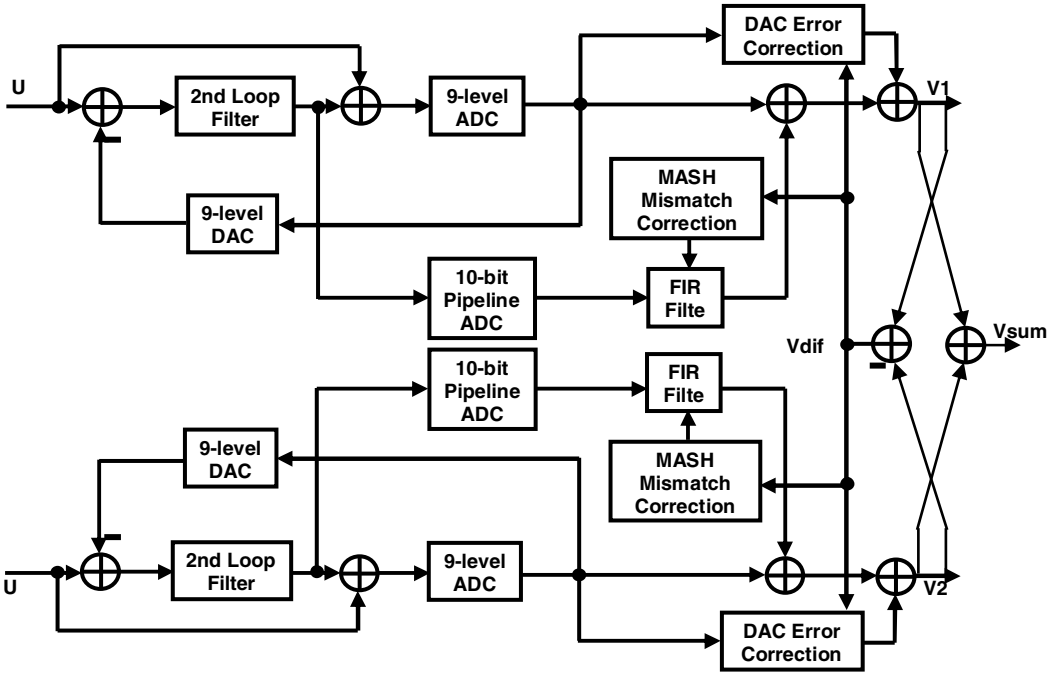

Fig.3-6 Dual-path 2-0 MASH with digital corrections

Chapter 4 Prototype chip design---system level design

To prove the efficiency of the dual-path structure, a design example is given out in this chapter. A dual-path 2-0 MASH structure is presented in Fig.4-1. The first stage is a second-order DSM with 9-level quantization. The second stage is a pipelined ADC. A scrambler is inserted between quantizer output and DAC input to randomize the DAC selecting sequences. The on-chip circuits include the DSMs in the 1st stage, pipelined ADCs and their corresponding digital blocks, clock generators. The digital correction algorithms are implemented off-chip,

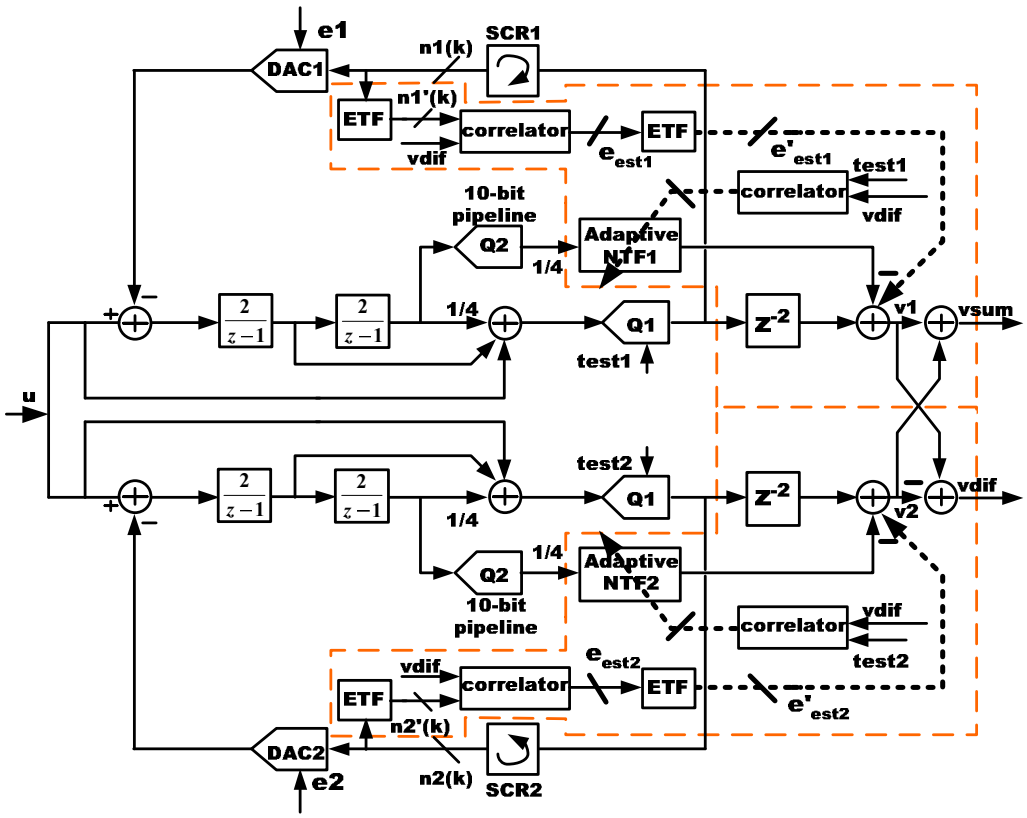

Fig.4-1 Dual-path 2-0 MASH DSM

surrounded by dash rectangular curve in Fig.4-1, including adaptive NTF filter, the quantization Noise Cancellation Logic (NCL), DAC error estimation and cancellation logic. The targeted performance of design is 80dB SNDR with OSR less than 8 and signal bandwidth of larger than 1MHz.

4.1 Structure selection

A low-distortion feed-forward structure [4-1] was adopted for the 1st stage. It offers low power and area consumption. Since only the conversion errors are processed in the integrators, the nonlinearity of integrators just causes the noise folding into the signal band, instead of the input signal distortion. The other benefit is that the quantization noise from 1st stage, serving as the input of second stage, can be directly extracted from the output of 2nd integrators without using any extra circuits. Circuit complexity is greatly reduced.

Under the condition of not saturating integrators, usually the 1st integrator's gain should be as large as possible in order to reduce the input referred noise from the following circuits. In the practical design, the larger integrator gain, the smaller its feedback factors. Hence, faster opamps should be designed to meet the same settling requirement. In this design, the 1st integrator gain is selected as "2" based on the trade-off of above two factors. Also we find if the 2nd integrator gain is "2", the output swings of both opamps are almost same, indicating both opamps' maximum output swing can be made full use of. Since the integrators output swing is proportional to quantization noise, this 2-2 combination of integrators gain is

optimum for all the low distortion structures shown in Fig.4-1. Fig.4-2a, Fig.4-2b, gives the probability of two integrators' outputs with a 9-level quantizer and an input signal of -3dBFS @ $13*2^{-8}$ Fs (in the following system simulation , the signal full scale FS and sampling frequency Fs are normalized to -1--+1 and 1 , respectively).

Since the quantization noise in the 1st stage will be cancelled at the final output, it will not affect the final SNDR. The selection of internal quantization level is only determined by the requirement of maximum input signal amplitude. Larger quantizer interval causes a reduced maximum input signal amplitude. In this design, a 9 level quantization can still allow an input signal amplitude up to -3dBFS without saturating the quantizer. A quantizer with more quantization levels will increase the maximum allowed input signal amplitude, but more power and area consumption are needed for the quantizer design. Fig.4-3a, Fig.4-3b show the probabilities of quanitzer inputs with a input signal of -3dBFS@ $13*2^{-8}$ Fs for 9-level and 33-level quantizer, respectively. The maximum quantizer input in 33-level DSM is around 2dB lower than that in 9-level one, which means 2dB larger maximum input signal is allowed at the cost of 32 quantizers with higher accuracy. Hence, 9-level quantization is used in this case.

Based on the initial simulation results of folded-cascode opamps in a 0.18um CMOS process, 1.08V Peak-To-Peak (P2P) differential output swing with moderate DC gain droop during the output swing range is not hard to design. Since in the system-level simulation, the maximum integrators swing is around 0.73FS ,

thus we decide the full scale of input signal of -0.72V—+0.72V. Actually the opamp swing of active adder is higher than those of integrators. But the nonlinearity generated at the summing node will be mostly cancelled in the MASH DSM. Hence it is not a big problem.

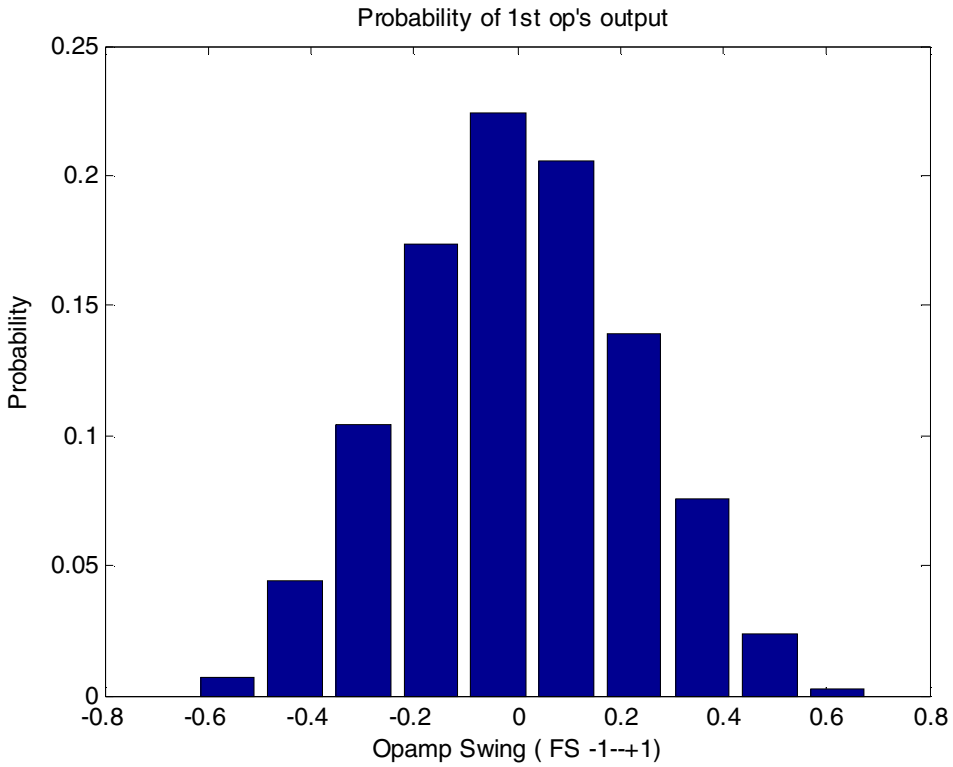

Fig.4-2a Histogram of 1st opamp's output

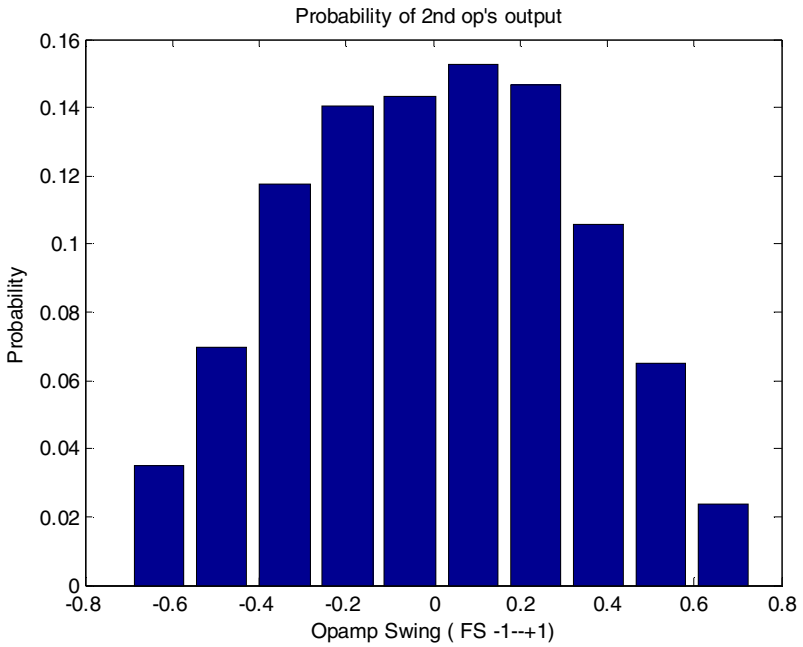

Fig.4-2b Histogram of 2nd opamp's output

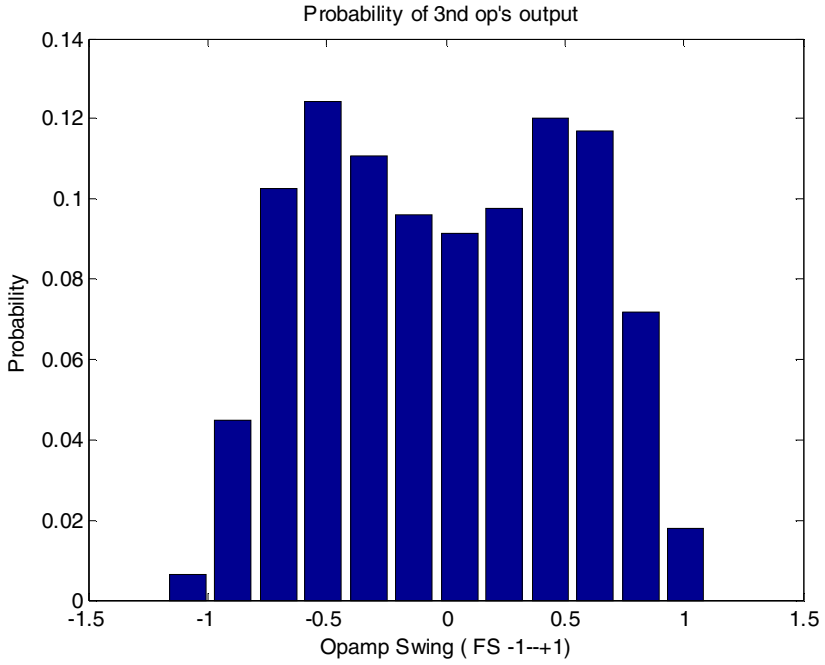

Fig.4-3a Histogram of the 9-level quantizer input

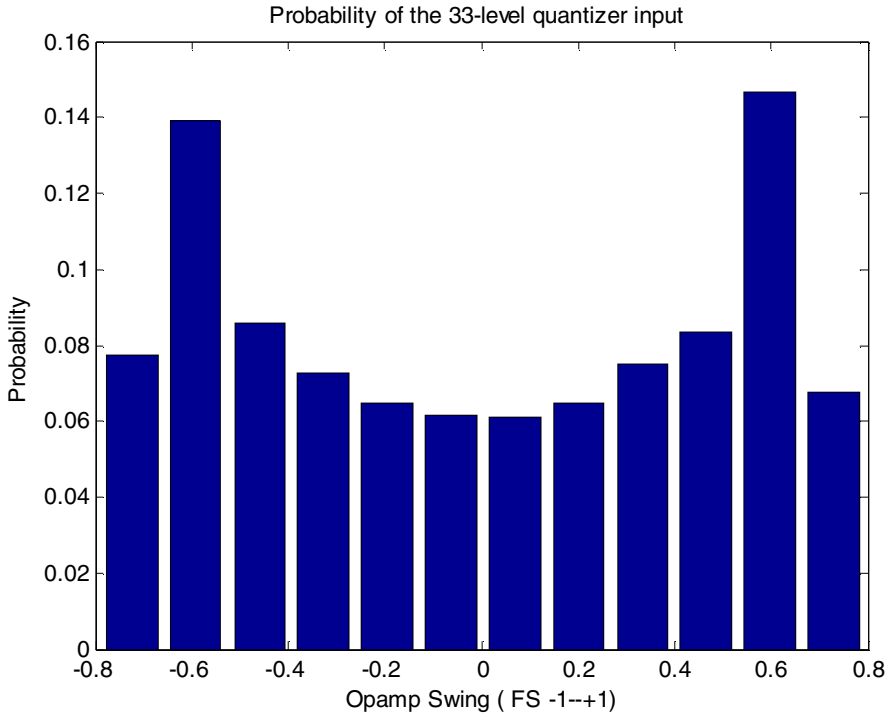

Fig.4-3b Histogram of the 33-level quantizer input

4.2 Noise analysis

In the DSM design, the intrinsic noise sources concerned can be divided into two groups, one device noises, such as thermal noise, 1/f noise, the other non-device noises, such as quantization noise, residue of quantization noise leakage and DAC mismatch error after digital calibration. The devices noise can be reduced at the cost of chip area and power by using larger devices to reduce the mismatch errors and 1/f noise or burn more power to reduce thermal noise. The non-device noises are more dependent on the system level design, such as how aggressive the NTF is designed. Reducing devices noises in DSM is more expensive, Hence they usually dominate the final noise floor in a practical design.

In this thesis, all noise sources are assumed as the white additive noises, just as thermal noise. For a 1MHz signal band, 1/f noise isn't dominant, but not negligible. To simplify the noise analysis, total 1/f noise power is calculated by integrating its PSD in the whole clock-frequency band. Its average PSD is calculated by averaging its noise power in the whole clock-frequency band. Then in the noise analysis, it can be treated as white additive noise. Hence the technique of fast estimation of thermal noise can be used for all the device noise, [4-2]. Certain errors will be introduced in this way, but it will not affect the final noise performance greatly.

All the device noise sources are shown in Fig.4-4. For SC integrators, two noise sources, switch noise and opamp noise, are introduced in two phases, sampling phase (phi1) and integrating phase (phi2). For simplification, here all the noise generated in the integrators are modeled by two equivalent noise sources, one is the integrator Input Referred Noise (IRN) and the other Output Referred Noise (ORN), [4-2]. The IRN includes the switch noise during phi1 plus opamp and switch noise in phi2, which are referred to the noise voltage across the sampling capacitor. Thus these noises have the same TFs as the signal sampled on *Cs*. *Vcon1*, *Vcon2* are IRN of each integrator, Fig.4-4. The output noise is composed of the opamp noise generated in the phi1.*Von1* and *Von2* are ORNs. *Von3* models the switch noise in the feed-forward pathes plus opamp noise from the active adder. *Vpn3* models the noise generated by the pipelined ADC.

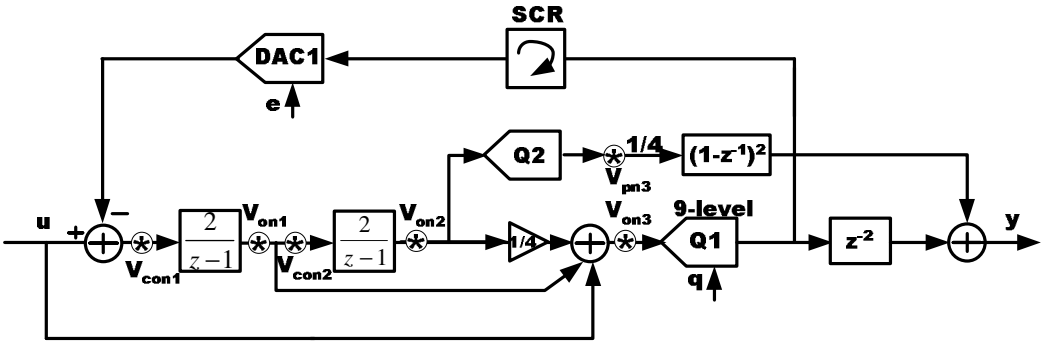

Fig.4-4 The noise sources in 2-0 MASH

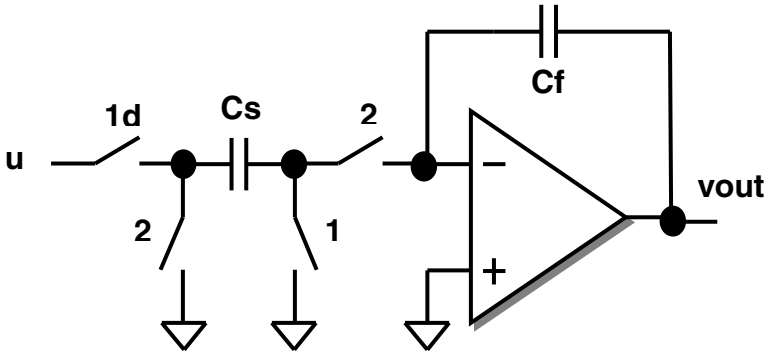

Fig.4-5 Non-inverting delaying integrator

Each noise source has different contribution when referred to the input of DSM. For example, *Von2* is 2nd order shaped, while Vcon1 is never attenuated by the loop gain, therefore *Von1* is much more important that *Von2*. Table.1 gives the Mean Square (MS) power gain for each noise source. Because of over-sampling, only small part of noise falling into signal band, this has been taken into account in the calculation of MS power gain. The noise *Von3* exactly follows the path of quanization noise in the DSM, since the quantization noise leakage will be corrected using the digital correction, all the noises injected before quantizer, "test" signal and *Von3*, are cancelled at the final output. Same does the DAC

mismatch error e, which will be removed through digital DAC correction. In the practical circuits, there are still some residues of quantization noise leakage and DAC mismatch error in the final output, which should be taken into account in the plan of noise budget.

In the system simulation, the peak SNDR occurs at the input signal of -2.5 dBFS. Since the full scale signal of DSM is -0.72V--+0.72V, its equivalent full scale in a dual-path structure is -1.44V--+1.44V.Hence

$$P_{sig} = -2.8dBV^2 \tag{4-1}$$

To achieve 80dB SNR with 1dB design margin,the total in-band noise power must be

$$P_{noise} = -83.8dBV^2 \tag{4-2}$$

Noise Source	TF	MS Power Gain
Vcon1	z^{-2}	1/OSR
Vcon2	$0.5[(z^{-1}-z^{-2})](1-2z^{-1}+2z^{-2})$	0.0296/OSR
Von1	$0.5z^{-2}(1-z^{-1})$	0.05/OSR
Von2	$0.25(1-z^{-1})^{-2}(1-2z^{-1}+2z^{-2})$	0.0024/OSR
Vpn3	$0.25(1-z^{-1})^2$	0.0044/OSR
Von3,q,e	0	0

Table 4-1 Noise sources and corresponding MS power gain

The final noise budget is shown in Table 4-2.

SNDR	kT/C		Opamp		Quantization Noise DAC error & Other	Pipeline ADC
81dB	40%		20%		22%	18%
Integrators	1st	2nd	1st	2nd	noise residues after digital correction	
	85%	15%	84%	16%		

Table 4-2 Noise budget of 2-0 MASH

In the simulation, a 800 level quanitizer is used to model the pipelined ADC. Hence its noise power is: $P_{pipe,noise} = -66dBv^2$ (4-3)

It uses the same reference voltages as 1st stage. Its input signal range is determined by the output of 2nd integrators in the 1st stage, limited to $\pm$0.73FS. Since this pipelined ADC only processes the quantization noise, any distortion in its operation causes the quantization noise folding into the signal band. In the actual design, 60dB SNDR is required. The noise budget of the pipelined ADC is shown in the Table 4-3.

SNDR (dB)	kT/C	Opamp	Quantization Noise plus cap mismatch	Margin
60	23%	22%	45%	10%

Table 4-3 Noise budget of pipelined ADC

Fig.4-6a, Fig.4-6b illustrate the SNDR improvement after turning on both digital error corrections, simulated for -3dBFS input signal of $13*2^{-7}$ Fs and $13*2^{-8}$

Fs, respectively , 0.1% RMS DAC errors , 52-dB opamp DC gains, 1% coefficients mismatch and channel mismatch , and random “test” signal with amplitude of ±1/5 quanitzation interval .Here, device noise was included in the simulation and the effect of limited opamp swing is also taken into consideration. Before correction, SNDR is 57dB and 60.3dB at OSR of 4 and 8, respectively. After correction, SNDR is improved to 80dB and 83.8dB, respectively. The 3dB difference of SNDR in two cases indicates the noise performance is mostly constrained by the kT/C noise and opamp noise in the 1st integrator, where those noise are not shaped but attenuated 3dB by doubling the OSR.

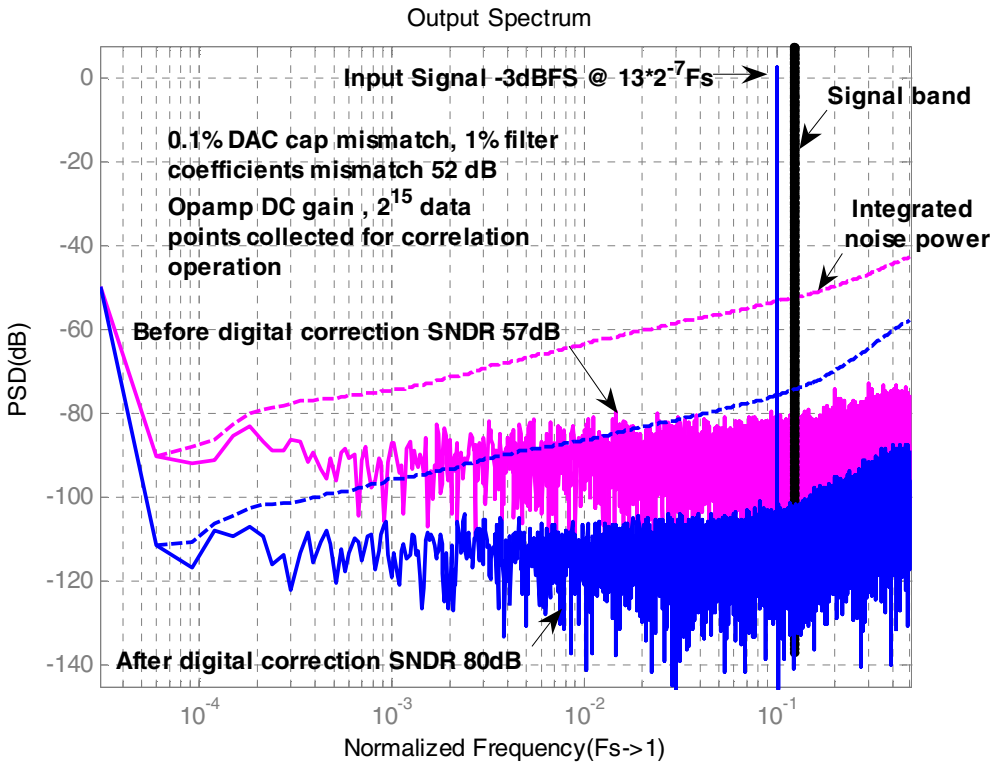

Fig.4-6a SNDR improvement @ OSR=4

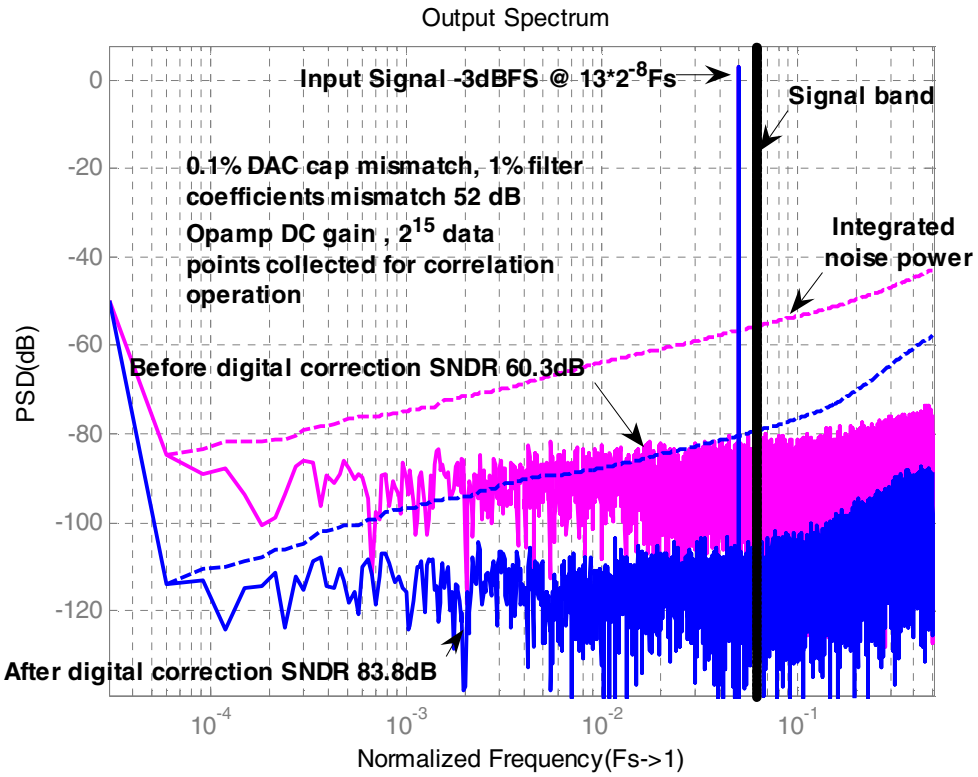

Fig.4-6b SNDR improvement @ OSR=8

Chapter 5 Prototype chip design---circuit and layout design

Based on the noise budget of Table.4-3, the capacitors size is decided. The corresponding SC implementation of 1st stage is presented in Fig.5-1. Only one channel in single-ended implementation is shown. In the actual design, differential circuits were implemented with all capacitors half sized. The sampling capacitors are shared by feedback DAC, which brings up to 3dB improvement of kT/C noise. Since this DSM is run at moderate clock frequency and the targeted SNDR is not very high. The effect of signal dependent loading for the reference voltage may not cause big trouble even without on-chip reference buffer. [5-1]

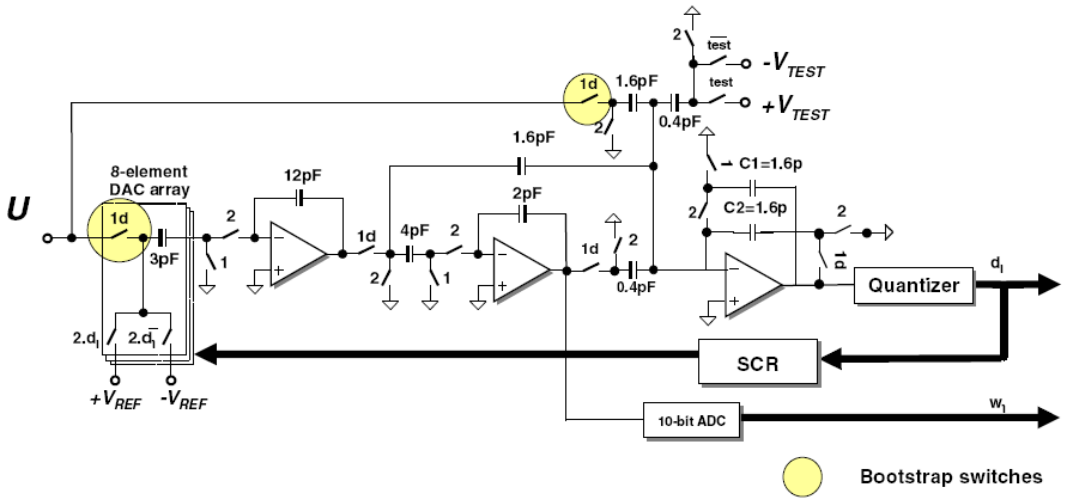

Fig.5-1 SC implementation of 2-0 MASH

5.1 OTAs

In this MASH, all the quantization noise leakage caused by finite opamp DC gain will be corrected using digital correction, thus single stage folded-cascode OTAs [2-5] are used in the 1st stage. All OTAs use the same structure. Based on the different capacitor loading, the power and transistors size are scaled. Here the continuous CMFB is realized by controlling the tail current. MC2, MC3 work in the triode region, serving as feedback network, sensing the CM level of output signal. One important thing for the layout design is to keep the parasitic resistor

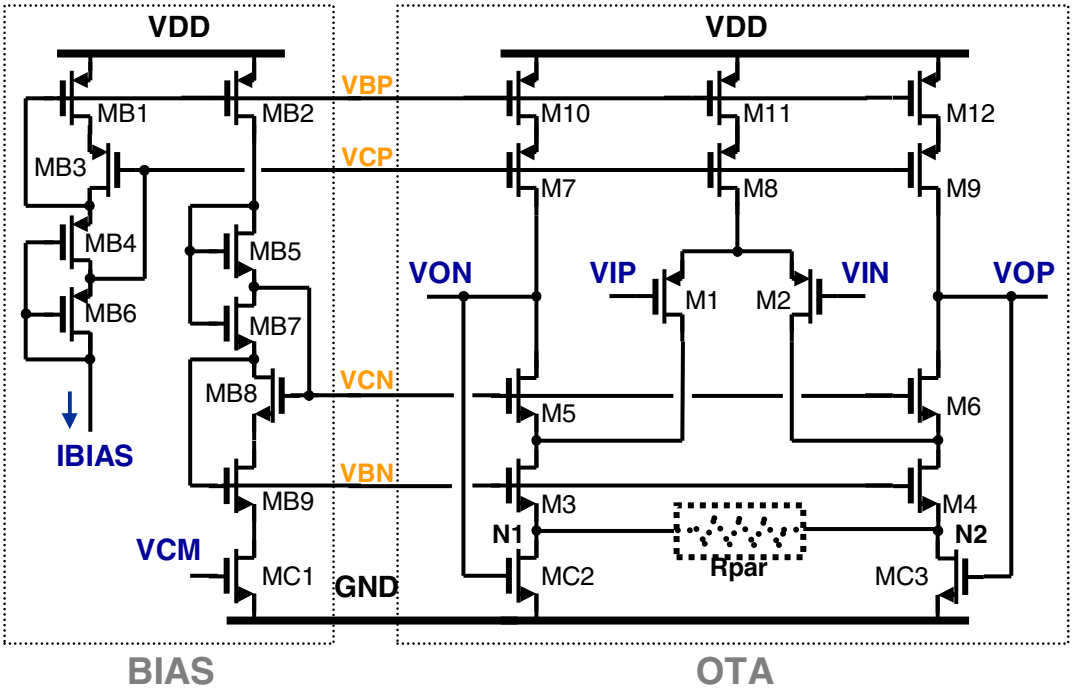

Fig.5-2 Folded-cascode OTA

Rpar as small as possible. In the ideal case, if Rpar=0, nodes N1 and N2 are shorted , serving as the virtual ground of differential signal. The loop gain for differential signal is zero. The CMFB loop only sense and attenuate the output CM signal variation. But if Rpar≠0 , there will be differential signal across the nodes of N1 and N2, the loop gain of differential signal in CMFB is not zero. Hence the OTA's differential AC gain will be attenuated by the differential loop gain of CMFB loop. In the designed OTAs, even 1ohm of Rpar will cause the 20dB drop of DC gain and great deterioration of phase performance.

For OTAs used in the pipelined ADC, since the error voltage caused by finite opamp DC gain is proportional to$1/\alpha\beta$, where α is the opamp DC gain and β is the feedback factor, for a 10bit 1.5 bit/ stage pipelined ADC , the first stage's opamp gain should be at least 60dB [3-2]. The single stage folded-cascade OTA shown in Fig.5-2 , gives less than 60dB DC gain, hence gain boost circuits are used, shown in Fig.5-3. The two supplementary opamps for gain-boost are also in folded cascade structure with scaled sized and bias current. To accommodate the different input CM level, one is with NMOS inputs, the other PMOS inputs.

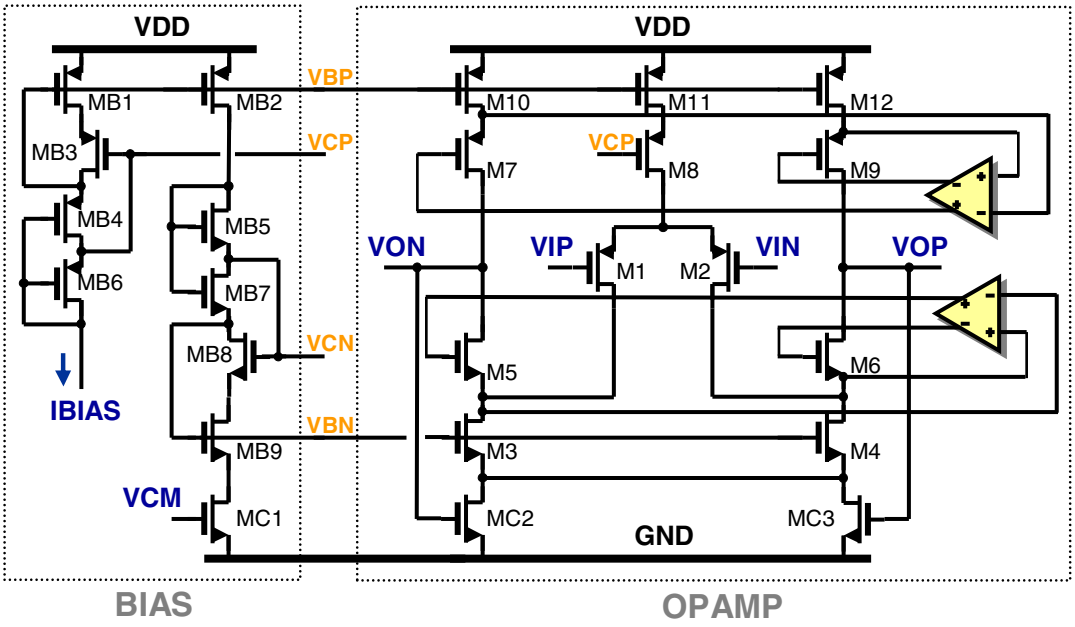

Fig.5-3 Opamp with gain boost circuit

The close loop bandwidth of opamps combined with the switch on resistance and capacitor loading determines the final settling accuracy in each clock phase. In the initial design, 80% time is assigned for the opamp settling and 20% time is assigned for the slewing process in each phase. If only considering the opamp settling, the settling error is limited to 16 bit accuracy. Fig. 5-3 summarize the opamps performance in the initial design. Here phi1 is the sampling phase, phi2 integrating phase. 1^{st} ,2^{nd} ,3^{rd} ,4^{th} Opamps indicated the opamps used in the 1^{st} integrator , 2^{nd} integrator , active adder of 1^{st} stage, and pipelined ADC, respectively.

Opamp	β (dB)	β *UGBW (MHz)	PM	CL (pf)	DC gain (dB)	CMFB DC Gain (dB)	CMFB UGBW (MHz)	CMFB PM
1st (phi2)	-11.5	90	83	4.4	56.9	42	24.9	92
1st (phi1)	-4.9	156	78	5.47	56.9	42	20	91
2nd(phi2)	-12.4	110	83	0.76	57.6	41.5	20	75
2nd (phi1)	-6.65	108	82	1.53	57.6	41.5	14.8	77
3rd (phi2)	-15.2	125	79	0.66	53.8	40	66	108
3rd (phi1)	-14	93	82	1.55	53.8	40	37	105
4th (phi2)	-11	92	81	1.1	99	40	23	85

Opamps output swing:-0.54v-0.54v, DC gain droop: less than 1 dB

Current/OP	1st (DSM)	2nd (DSM)	3rd (DSM)	4th (PIPE)
Current (mA)	4.1	1.1	2.1	0.8

Table.5-1 Opamps performance summary

5.2 Active adder

For the low OSR feed-forward DSM, the summing node before the quantizer (Fig.5-1) becomes important to its linear performance, since signal distortion generated at this point may not be sufficiently attenuated because of low OSR. A passive adder saves power, but the quantizer input capacitors are voltage dependent. And this cause the signal-dependent gain variation of active adder, hence nonlinearity is introduced. Unlike the active adder, this nonlinearity can't be attenuated by the loop gain of opamp. In this design active adder is used [5-3]. In the adding phase (phi1), C2 sampled the output of active adder while in the reset phase (phi2), it holds the output, hence only the charge difference between clocks

need to be transferred in the next adding phase. For the DSM, this is very useful, since the input signal changes slowly compared with the clock frequency. Hence the voltage jump at the opamp output is greatly reduced from phase to phase, which greatly relaxes the required slew rate. On the other hand, since C1 sampled the 1/f noise and offset of opamp at the reset phase, these errors can be cancelled in the next adding phase. In this design, because of low resolution and noise shaping, actually we don't care much about these errors.

5.3 Comparator

There are 9 levels in the quantizer. For the FS of 1.44V, it indicates the offset of comparators should be less than 90mV to avoid the missing code. Illustrated in Fig.5-4, the comparator consists of preamplifier, degenerative latch[5-4], followed by a SR latch and bubble correction circuits (not shown here). The preamplifier is designed for a DC gain of 23dB, 3-dB cutoff frequency of 142MHz and UGBW of 1.75GHz with phase margin of 53^{o}. It means that even though the offset from degenerative latch is larger than 1.26V, still no missing code occurs. In a reasonable design, the latch offset is usually less than 150mV, indicating that the input referred offset is less than 11mV. The UGBW of preamplifier is also determined by the settling accuracy during the reset phase, when the reference voltage generated by the resistor ladder are sampled. The settling accuracy is mainly determined by the preamplifier bandwidth, sampling

capacitor size, ladder resistors and switch on-resistance, which is a complex process. The selection was optimized by simulation results.

To reduce the loading of the active adder, small input device is used for the comparator. The offset caused by the mismatch from small input device is handled by using the technique of Input Offset Storage (IOS) [5-5]. In the reset phase, the preamplifier is in the close loop configuration and its input offset is stored on the input capacitor. At the comparing phase, the comparator is in open loop and its input offset is cancelled. The preamplifier also serves as buffer, relieving the effect of "kickback" on the active adder when the comparator comes into latch phase.

A regenerative latch and an SR latch are following the preamplifier. When Φ_C is high, the regenerative latch is reset. SR latch holds the comparison result of last cycle. The new comparison result is latched at the falling edge of Φ_C.

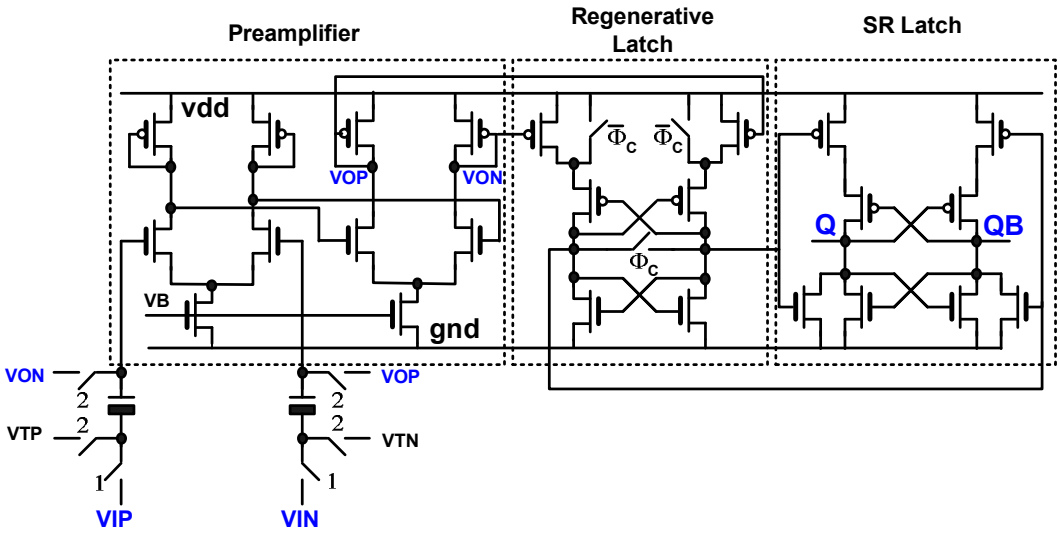

Fig.5-4 Comparator with preamplifier

Because of low frequency and low resolution, not much consideration was put on the effects of metastability and hysteresis [5-6]. Actually the latter is relieved by the reset phase after each latch operation.

5.4 Bootstrapped switch

The basic operation of bootstrapped switches can be described as follows: in the reset phase, the cap C_{Boot} is charged to V_{DD}: at the sampling phase, the input signal V_{IN} is applied to its bottom plane boosting its top plane to $V_{IN}+V_{DD}$. Hence the gate-to-source voltage of switch MSW (Fig.5-5) is kept constant at V_{DD}, which means both the switch on resistance and charge injection of MSW in the sampling phase are signal independent, if the body effect is neglected here. Therefore high linearity sampling operation is achieved. Compared with the circuit in [5-7], the implementation in this design [5-8] is much simpler.

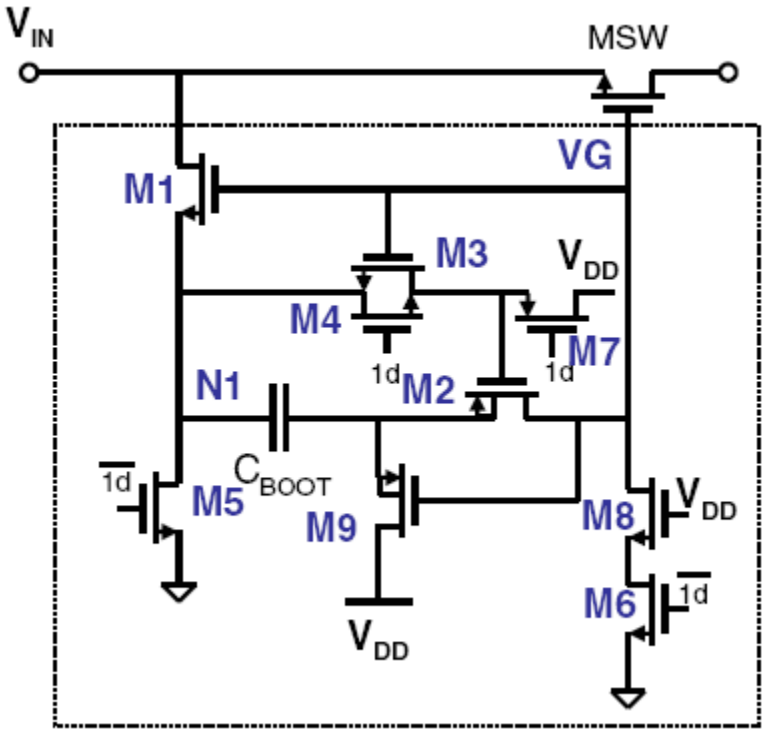

Fig.5-5 Bootstrapped switch

For the DSM shown in Fig.5-1, the nonlinear error generated in the input feed-forward path will be partially cancelled at the final output in the ideal case, since it has same transfer function as that of quantization noise. But the non-linear error generated at the front end of loop filter can't be attenuated by the delta-sigma loop. To achieve the high linearity performance, bootstrapped switches [5-7] should be used for input switches, as shown in Fig.5-1. Also bootstrapped switches are used in the sampling switches in the 1st stage of pipelined ADC .Since pipelined ADC processes the quantization noise from 1st stage, any nonlinear error will cause the quantization noise folding.

5.5 Pipelined ADC

Based on the system level simulation, 10-bit accurate quantization is needed for the second stage of MASH ADC. Here, a 12 bit pipelined ADC with Effective Number Of Bit (ENOB) of 10 was designed. To simplify the circuit design, 1.5 bit / stage was used. The first 10 stages are composed of 1.5-bit Multiplying-Digital-to-Analog Converters (MDAC), while the last stage is a 1.5 bit flash ADC, as illustrated in Fig. 5-6,7. Digital error correction is used to obtain the final 12-bit binary outputs.

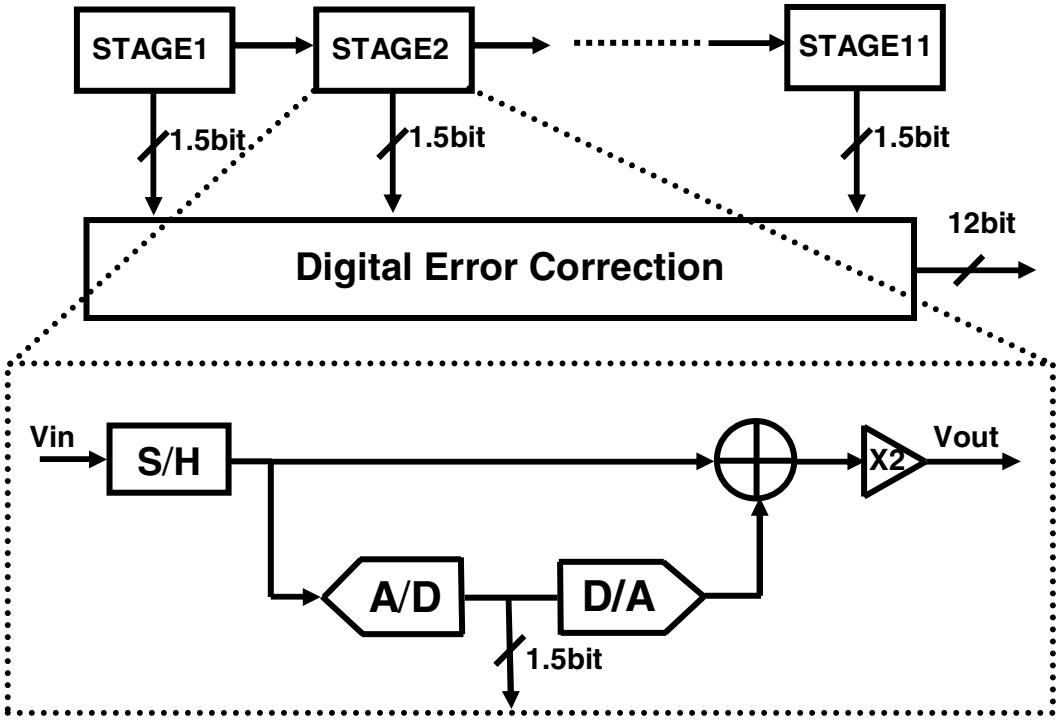

Fig. 5-6 10 bit accuracy pipelined ADC

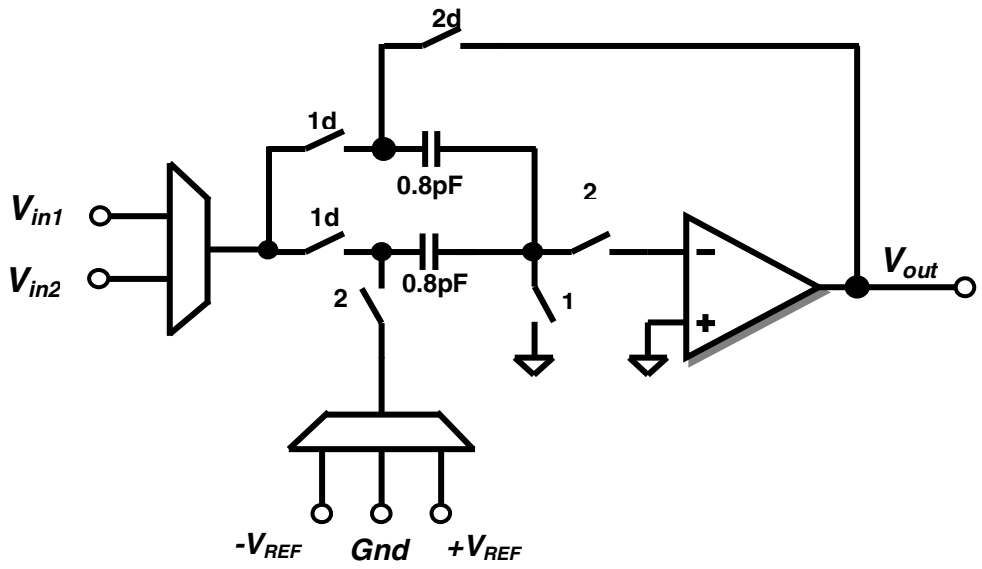

Fig.5-7 MDAC of 1st stage

Fig.5-7 is the 1st stage MDAC with programmable inputs. In the designed 2-0 MASH ADC, the input of pipelined ADC comes from the 1st stage DSM. In order to allow the easy debugging in the test stage, its input is programmable, one is from the 1st stage in the normal operation, the other from an external signal source, which will be applied only if the MASH doesn't work well, and debugging has to be carried out. Bootstrapped switches are used for the sampling operation. The comparators used in the MDAC are the same as those in the 1st DSM.

The following MDACs have the same structure as the first one, except for the programmable inputs. Based on the technology data, 12-bit matching accuracy can be achieved for capacitors used in MDAC. Also, high DC gain was designed

for the opamps in the MDAC. In the simulation, 10-bit accuracy could be achieved without calibration.

5.6 Scrambling block

The butterfly structure [5-8] was used for the scrambling block, randomizing the DAC selecting sequences. It is composed of 8 layers of switch boxes, shown in Fig.5-8. Each layer is controlled by one pseudo-random sequence, indicating two possible connections. In the simulation, 6-layer butterfly structure brings enough randomization of DAC selecting sequence for the DAC digital correction.

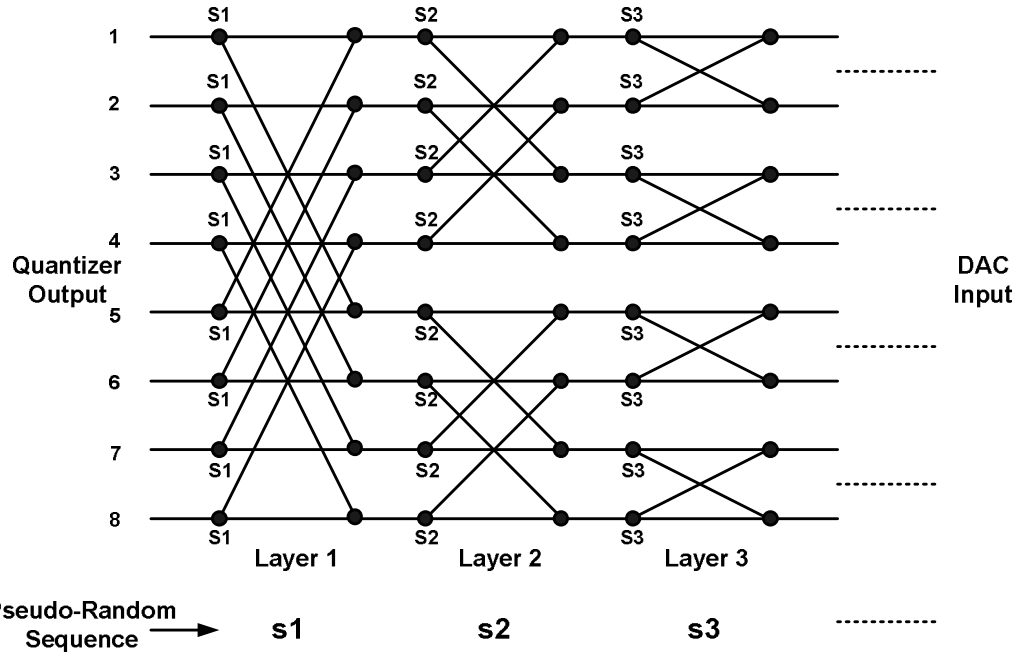

Fig.5-8 Butterfly structure

5.7 Experimental results

The chip was fabricated in a double-poly/6-metal 0.18 um CMOS process. Fig.5-9 gives the test setup of the chip. The left half of the board contains the interface circuits for digital signals, while the right half circuits for analog signals. Figs.5-10 and 11 give the SNDR improvement after turning on the digital correction. Finally, the performance summary is given in Table.5-2. Under the same test condition, the correction technique fails to converge if only one channel output is used for correlation operation.

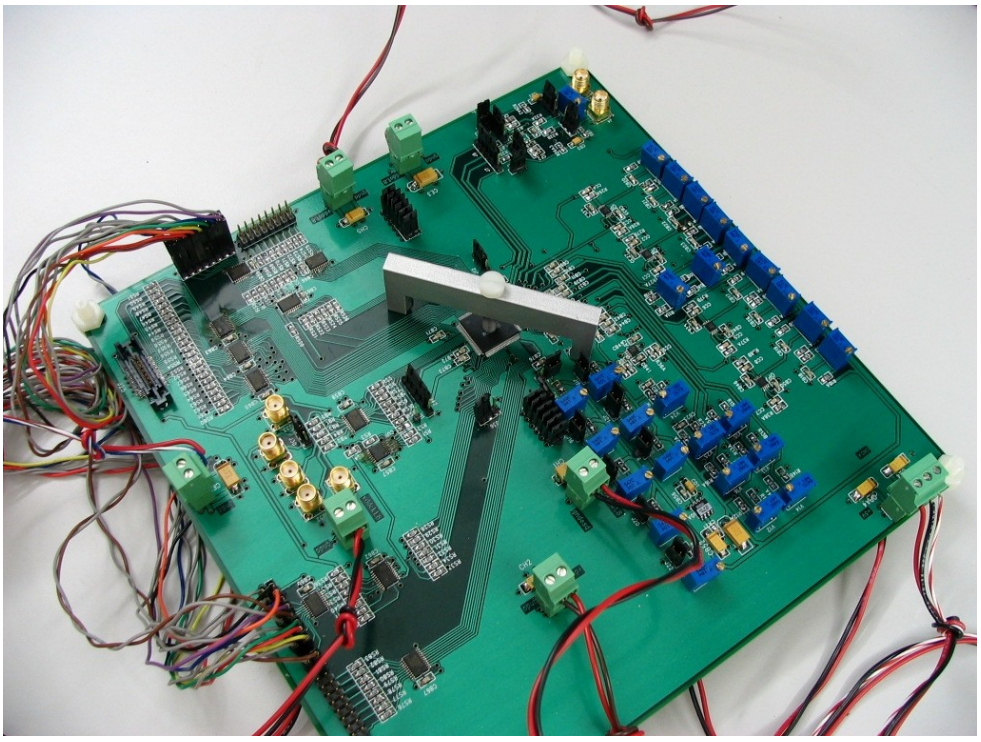

Fig. 5-9 Test setup of the dual-path MASH Chip

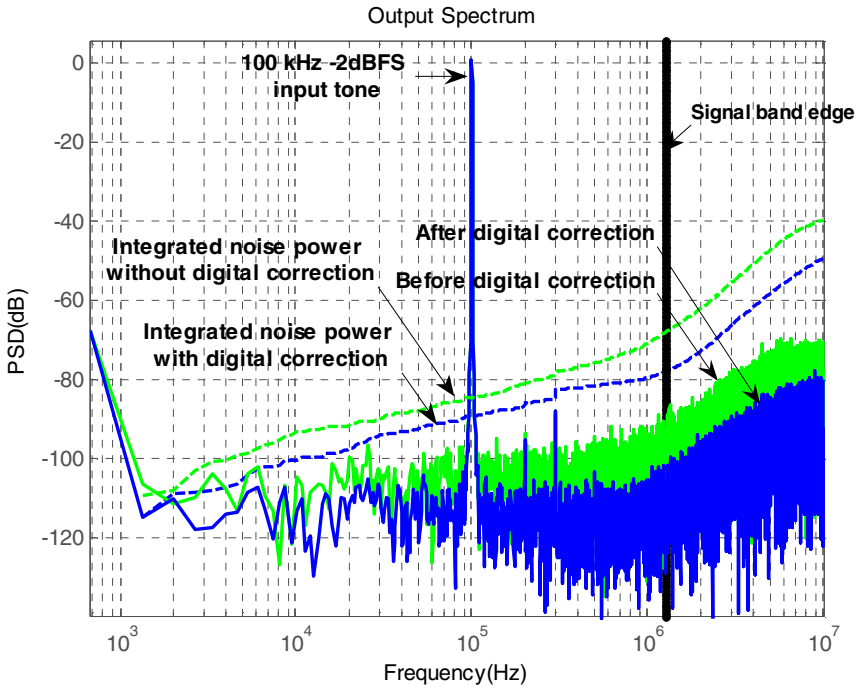

Fig.5-10 SNDR improvement after turning on digital correction

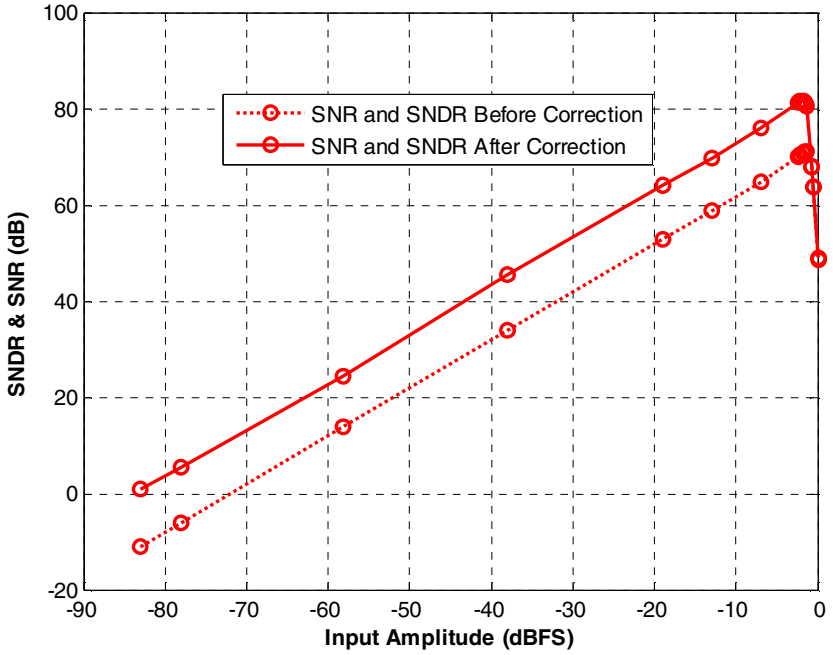

Fig.5-11 SNR and SNDR versus input amplitude with digital correction on and off

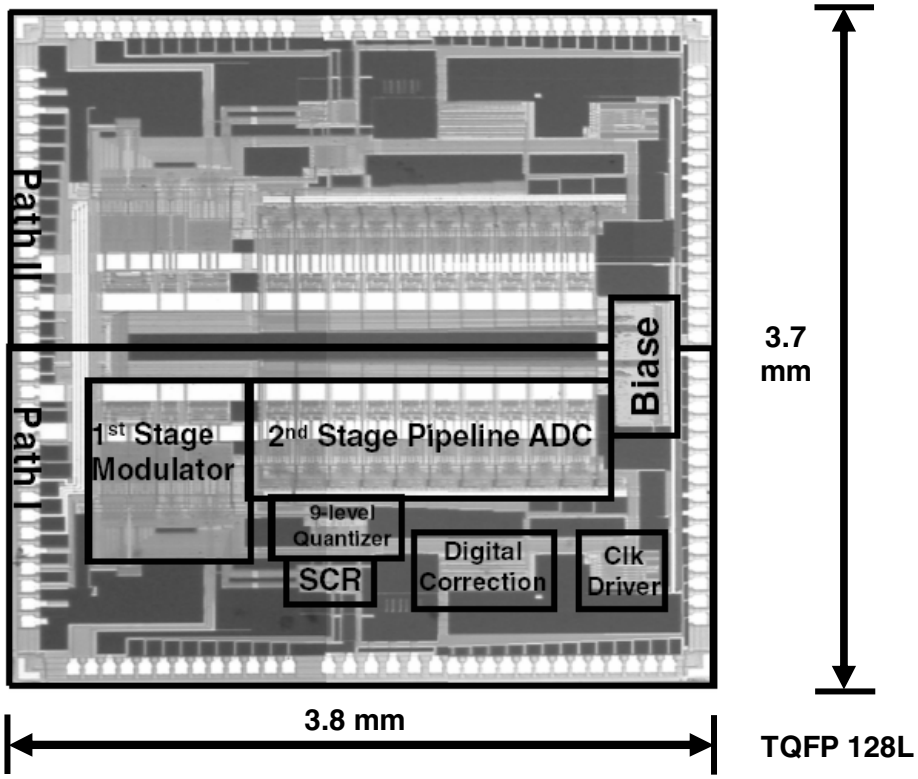

Fig.5-12 Die micrograph of the dual-path 2-0 MASH ADC

Sampling Frequency	20 MHz
Signal Bandwidth	1.25 MHz
Oversampling Ratio	8
Peak SNR, SNDR	82 dB, 81dB(-2 dBFS @ 100 kHz)
Dynamic Range	84 dB
Input Range	1.6 Vpp(Differential)
Power Consumption	46 mW (analog) , 18 mW (digital)
Power Supply	1.8 V
Process	0.18 um CMOS

Table 5-2 Performance summary of the prototype chip

Chapter 6 Segmented data-weighted-averaging technique

6.1 Review of DEM technique

In a DSM with multi-bit quantization, Dynamic Element Matching (DEM) is usually used to filter the DAC mismatch error out of signal band, by using a scrambler to shuffle the thermometer coded quantizer outputs before they are applied on the feedback DAC. Data Weighted Averaging DWA [1-4] is the most popular DEM technique, because of its simple implementation and efficiency. The basic idea of DWA is to use all DAC units equally over the long term. In each clock period, the DWA scrambler rotates the thermometer-coded input bits following a rotation pointer. DAC units not used in the previous clock cycles take priority (Fig.6-1). Here the DAC code sequence determines how many DAC units should be selected during each clock cycle.

The implementation of DWA is very simple [5-1]. A 4-bit DWA circuit is shown in Fig.6-2, containing a counter and a log shifter. The counter generates the rotation pointer indicating where each input bit, q(3)—q(0), should be rotated during the next clock cycle. The log shifter rotates each input bit to the proper position through the binary-weighted control code sh(1)-sh(0). In some DWA implementations, instead of a log shifter, a coder is used to directly map the quantizer output bits to the DAC inputs d(3)—d(0), but this implementation is slower than the shifter-based one. Also, such coder-based DWA system introduces more loop delay in a continuous-time DSM, making it less stable. In an

SC realization, settling errors are introduced in the integrating phase. Hence shifter-based DWA implementation is often preferred.

However, DWA has also several potential problems. Because of its simple operation, it is easy for the DAC error sequences to form fixed patterns. Then

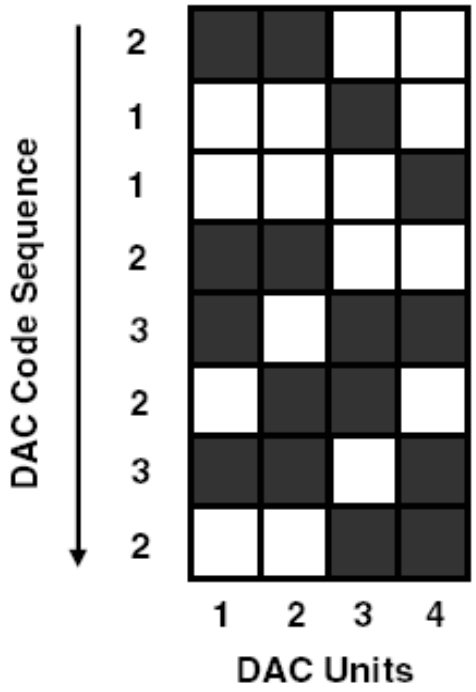

Fig.6-1 Principle of DWA operation

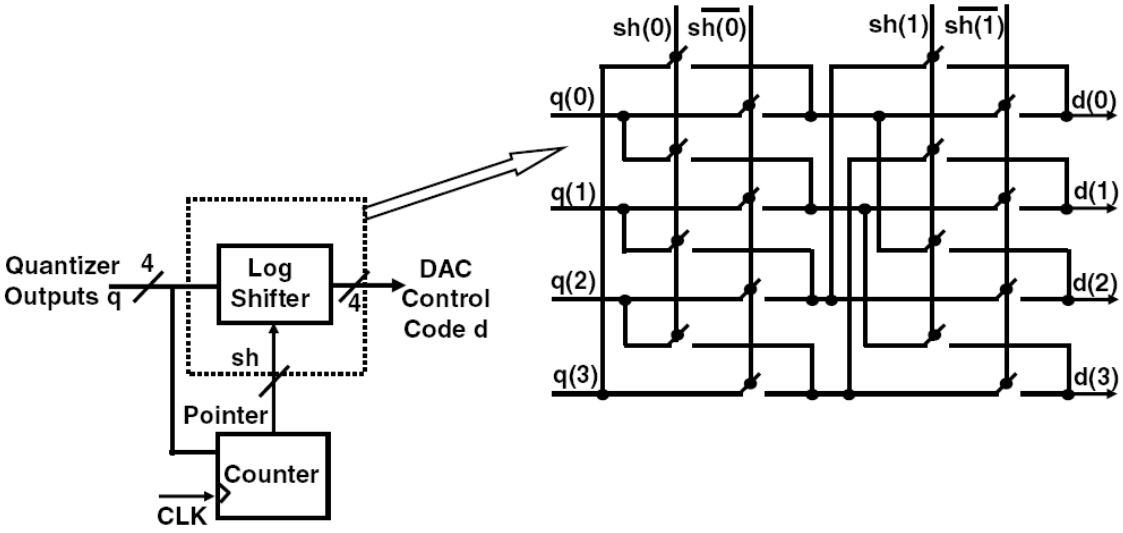

Fig.6-2 Shifter-based DWA implementation

tones are generated. (See Fig.6-3, which shows the simulated output PSD of a 2-0 MASH of Fig.6-4 with and without DWA.) Here, a 13-bit DAC matching accuracy was assumed, and no other device noises and mismatch errors were included. The OSR was 8, and a -2dBFS input signal with a frequency $13*2^{-8}$ fs was applied. The ideal SNDR and Spurious-Free Dynamic Range (SFDR) are 110 dB and 121 dB, respectively. (Only the in-band tones are taken into account when calculating the SFDR.) As shown in Fig.6-3, most of the DAC mismatch error power was filtered out of signal band, leading to a 10 dB improvement of SNDR (broken curves show the integrated noise power.) But the improvement of SFDR is much less, only about 4 dB. This is due to the pattern tones generated by DWA. In some applications, these tones are very harmful, for example in audio systems even tones 10 dB lower than the noise floor can be detected by the human ear. To eliminate tones, more complicated DEM techniques have been used, such as

BiDWA [1-3], ILA [1-5], SDWA[2-2] , which convert the tones into noise. Also, as Fig.2 illustrates, for DWA implementation, each rotation pointer should be generated in one clock cycle. In a high speed DSM, for example with a clock frequency higher than 400 MHz, realized in a 0.18 um or older CMOS technology, 2.5 ns of one clock cycle may not be enough for the generation of the rotation pointer, especially for a DAC with a large number (> 7) of units.

The segmented DWA proposed here offers a solution to both of these problems. It performs the noise shaping of the DAC mismatch error, and also randomizes the selecting sequences of the DAC units, thus suppressing all tones (no in-band tones could be observed in the simulations).In addition, as shown below, its implementation can be faster and simpler.

6.2 The SeDWA algorithm

SeDWA is performed as follows. The DAC units are divided into 2 or more subsets, with equal or unequal number of units (Although equally populous subsets are demonstrated here, unequal subsets are also possible). The subsets are divided into a master set and slave sets. All subsets have their own rotation pointers for DWA operation. In each time period, there is only one master set, and all the other subsets are slave sets. The master set roles are assigned in turn. During each clock cycle, the units in the master set have a priority of usage over

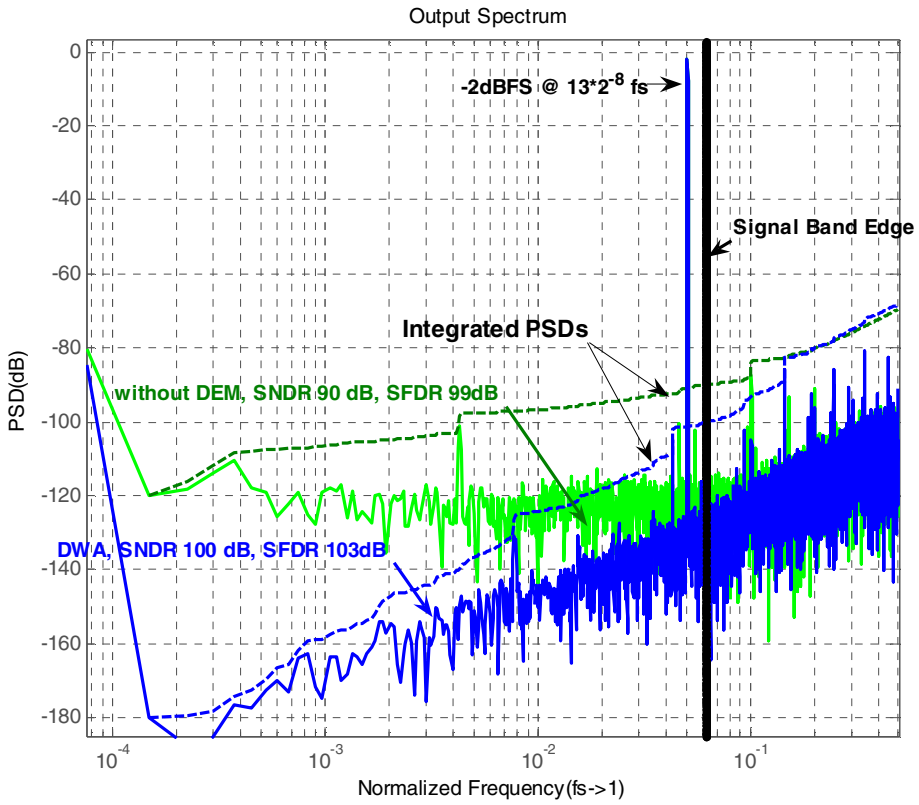

Fig.6-3 The PSD with and without DWA

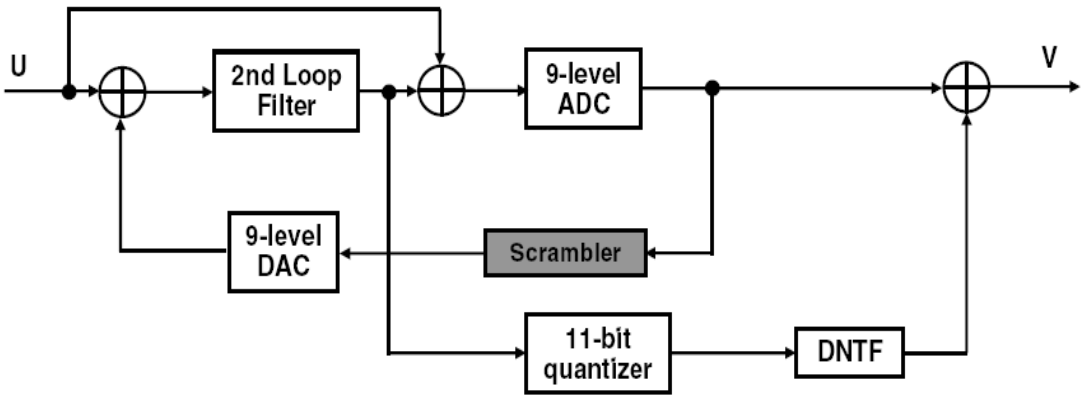

Fig.6-4 2-0 MASH with 9-level internal quantization

those in the slave sets. For a DAC with M units divided into N subsets, if P units ($P \leq M/N$) must be selected in the DAC, then only the units in the master set will

be chosen, using its DWA rotation pointer. If P > M/N, all units in the master set will be first selected, and then the remaining (P-M/N) units are chosen from the slave sets, in an order based on the previous usage of slave sets, with the slave set used least recently taking the highest priority.

In Fig.6-5 the operation of SeDWA with 8 DAC units divided into 2 subsets, set 1 and set 2, is demonstrated. The master and slave set roles are assigned alternatively. For example, at time instant n = (2k+1)T, set 1 is the master set and set 2 is the slave set. If n = 2kT, the roles are reversed.

If less than 4 DAC units should be selected in a cycle, all these units will be chosen from the master set based on its DWA rotation pointer. If more than 4 DAC units are selected, then first all the units in the master set are used, and the rest of units are selected from slave set. In Fig.6-5, at n=1 set 1 is the master set, so the first unit in set 1 is selected, and its rotation pointer is advanced by one. At n =2, set 2 is the master set, hence the first 3 units in set 2 are used, and the rotation pointer of set 2 is advanced by 3. At n=3, set 1 is the master set again. Since the input DAC code is 5, all 4 units in set 1 are selected and its rotation pointer remains unchanged. The remaining unit is selected from slave set 2. Since the rotation pointer for set 2 is at 3, the fourth unit in set 2 is chosen.

6.3 Simulation results

To compare the performance of SeDWA with that of conventional DWA, the output PSDs of DSMs using various DEM algorithms were simulated. Fig.6-6

shows the PSDs for the DSM of Fig.6-4 with two input signal frequencies: a low (2^{-11}fs) and a high ($13*2^{-8}$fs) one. A simple randomization is also illustrated. As the figures show, compared to randomization, SeDWA also performs mismatch shaping, resulting in a 11 dB improvement of SNDR in both cases.

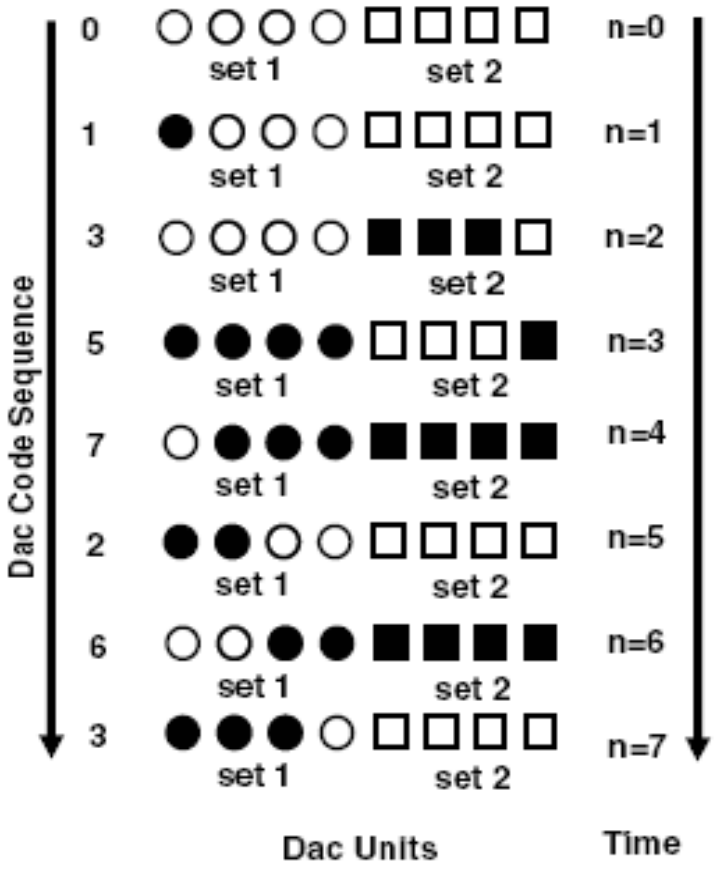

Fig.6-5 The SeDWA algorithm

Furthermore, SeDWA has a better linearity performance than conventional DWA. The SFDR of SeDWA is 2 dB less than that of DWA with low frequency input, and 9 dB better with a high frequency input, because the selecting sequences in SeDWA are more random. The SNDR of SeDWA is 9 dB lower for

the low frequency input, and 6 dB lower for the high frequency one, due to the increased noise floor generated by the randomized tones.

If more subsets are used in SeDWA, its performance deteriorates, because of less uniform usage of units in the different subsets. Fig.6-7 shows the PSD using SeDWA with 4-subset and 2-subset, respectively, simulated under the same above conditions, except that 32 units with 13 bit matching accuracy were used in the DAC. The SNDR and SFDR of 2-subset case are around 6dB, 4dB better than that of 4-subset. But a multi-subset SeDWA can be run at a much faster operation frequency, which can be useful in a high-speed application.

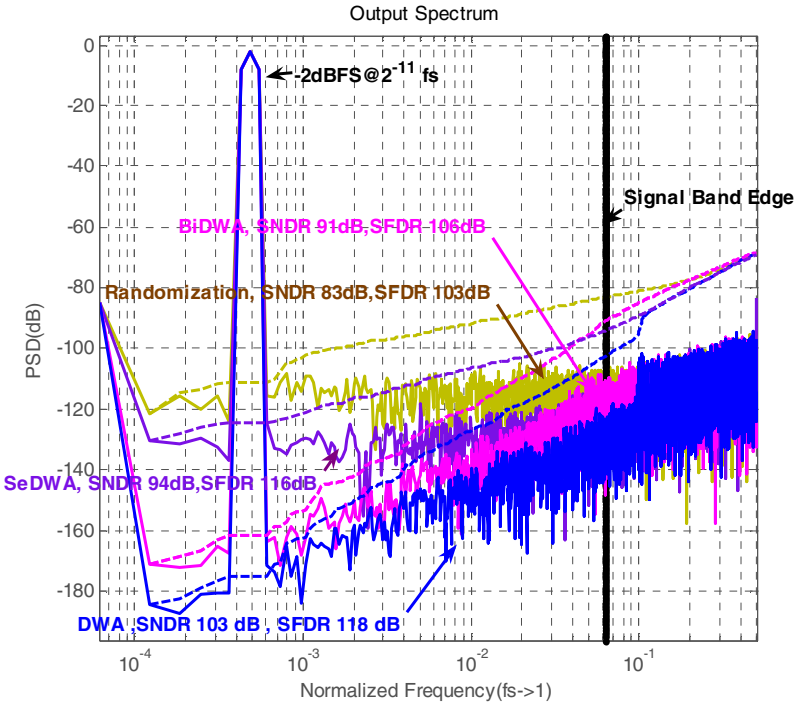

Fig.6-6a Output PSD with randomization, DWA, BiDWA and SeDWA (fin =2^{-11} fs)

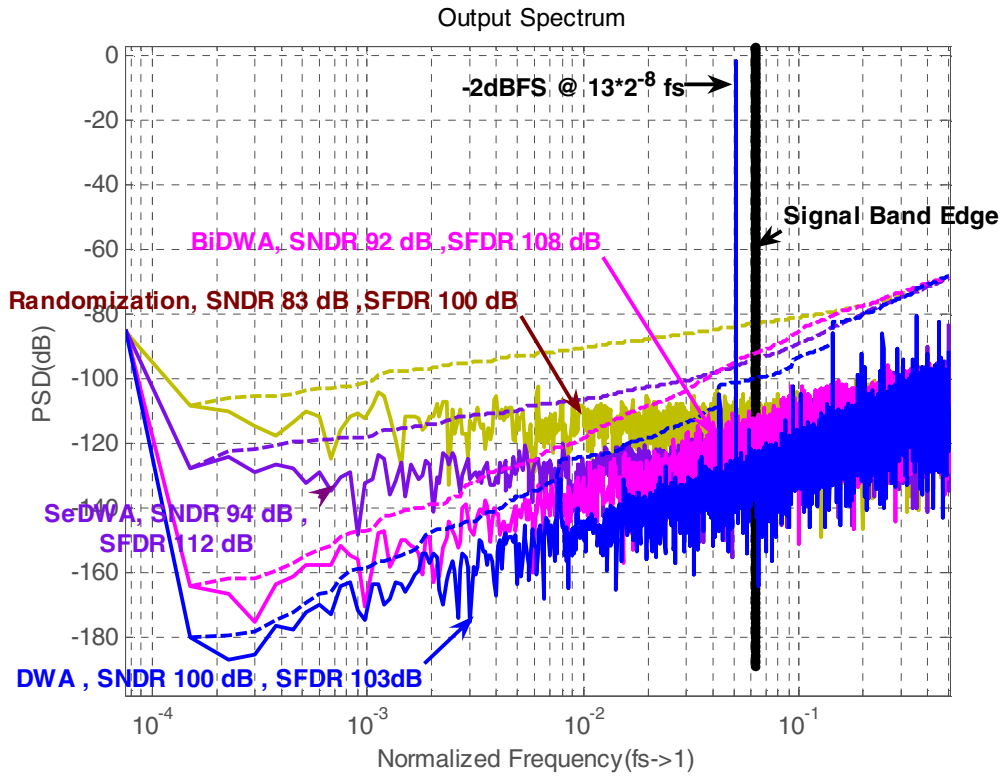

Fig.6-6b Output PSD with randomization, DWA , BiDWA and SeDWA

(fin =13*2^{-8} fs)

6.4 The implementation of SeDWA

Although one or more additional DWA circuits are needed for the subsets in SeDWA than in conventional DWA, faster speed and reduced hardware complexity can be both achieved. Since the input of the scrambler is thermometer coded (Fig.6-8), for the two-subset case the inputs of the DWA circuit in the master set is always at the bottom half of the quantizer output, while the top half is for slave set. This is also true for SeDWAs with more than two subsets. Hence the conventional DWA implementation can be used for each subset with an extra control signal (M/S ctrl) which decides which set is master and which ones are

slaves. Since the DAC units are divided into two or more subsets, the counter and shifter for all subsets are simpler. Hence, the scrambler can be faster, and the delay introduced by the scrambler is reduced.

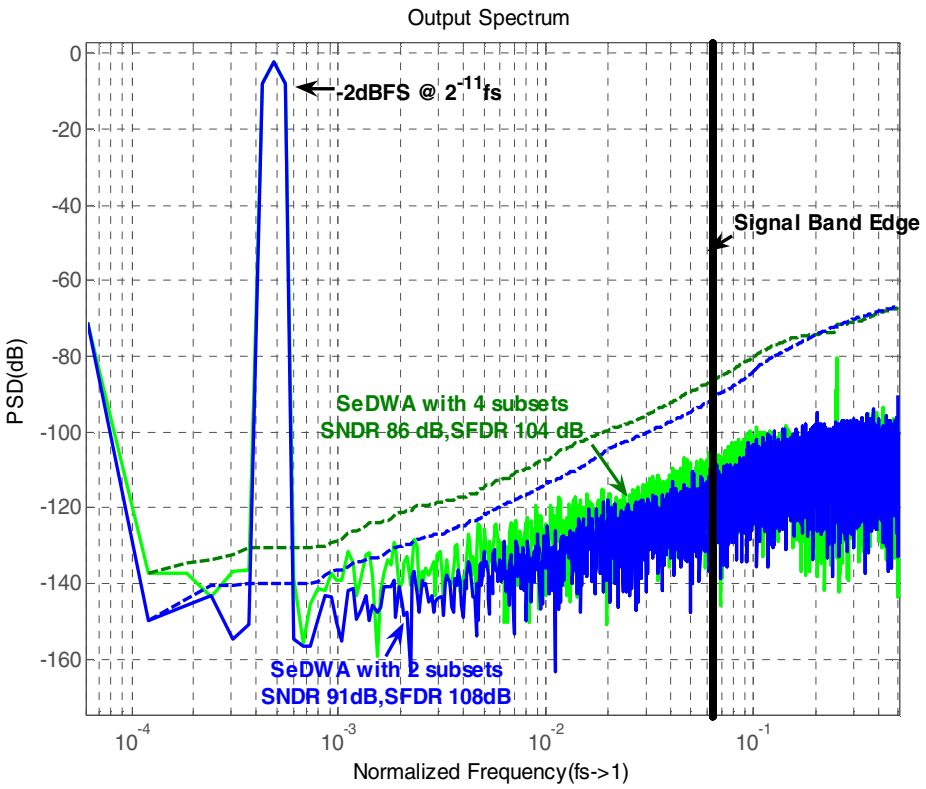

Fig.6-7a SeDWA PSDs with two and four subsets (fin = 2^{-11} fs)

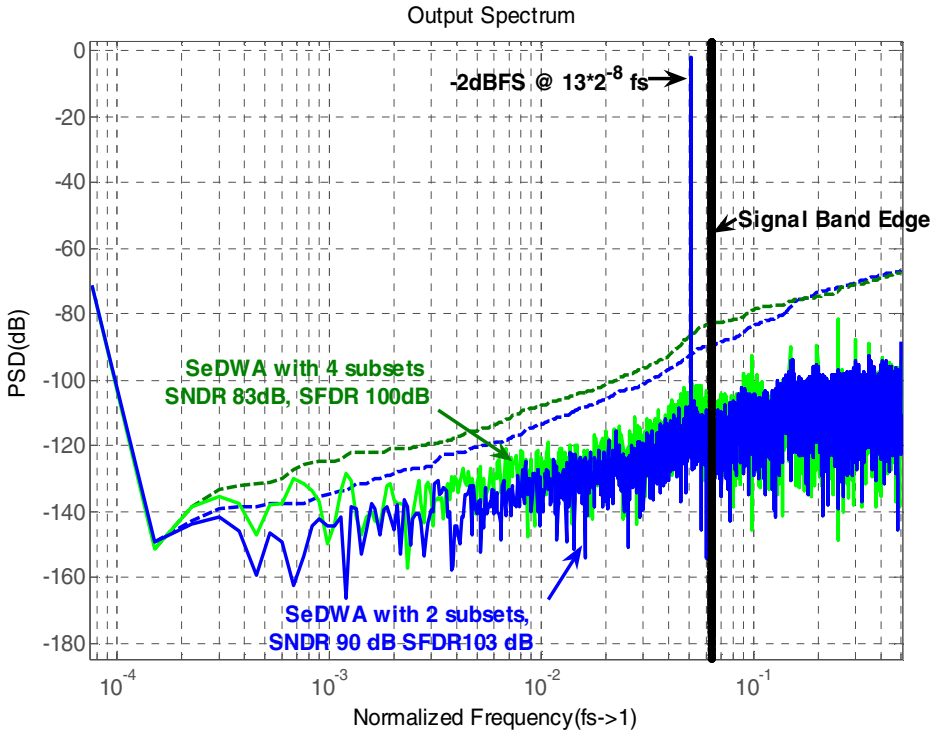

Fig.6-7b SeDWA PSDs with two and four subsets (fin =13*2^{-8} fs)

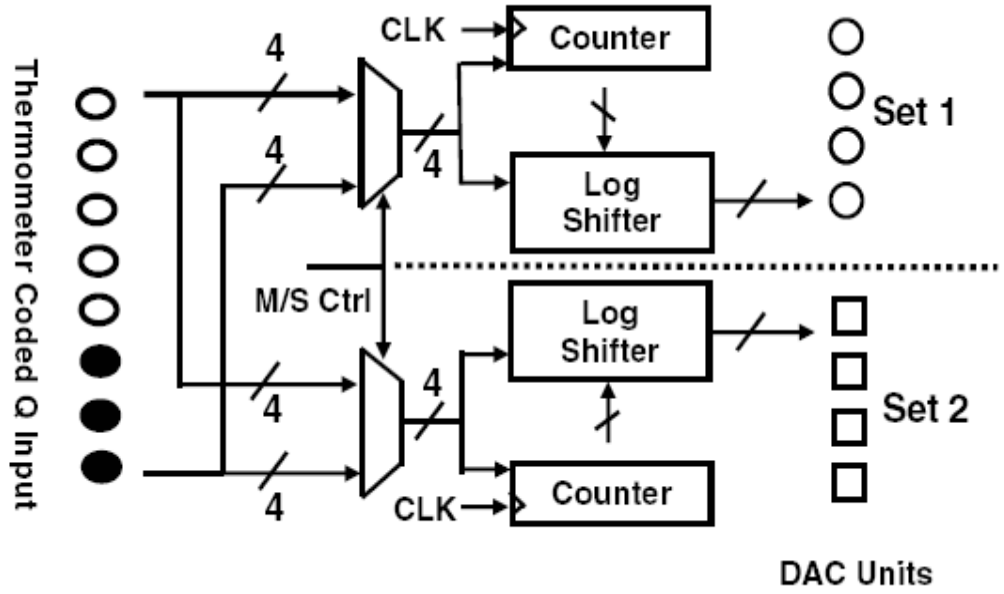

Fig. 6-8 Implementation of SeDWA

Chapter 7 Conclusion

A dual-path MASH DSM was designed and fabricated in 0.18um CMOS process. Two digital correction techniques were applied in this DSM: DAC error correction and quantization noise leakage correction. By using a dual-path structure, the efficiency of correlation based digital error correction technique was greatly improved. 10dB improvement was observed for the measured SNDR. In the future, for a dual-path structure, differential dual signal processing is preferred. Fig.7-1 shows a differential implementation of dual-path structure, a modified version of Fig.3-6. The common-mode signal of two channels, such as common - mode digital noise, can be then better attenuated.

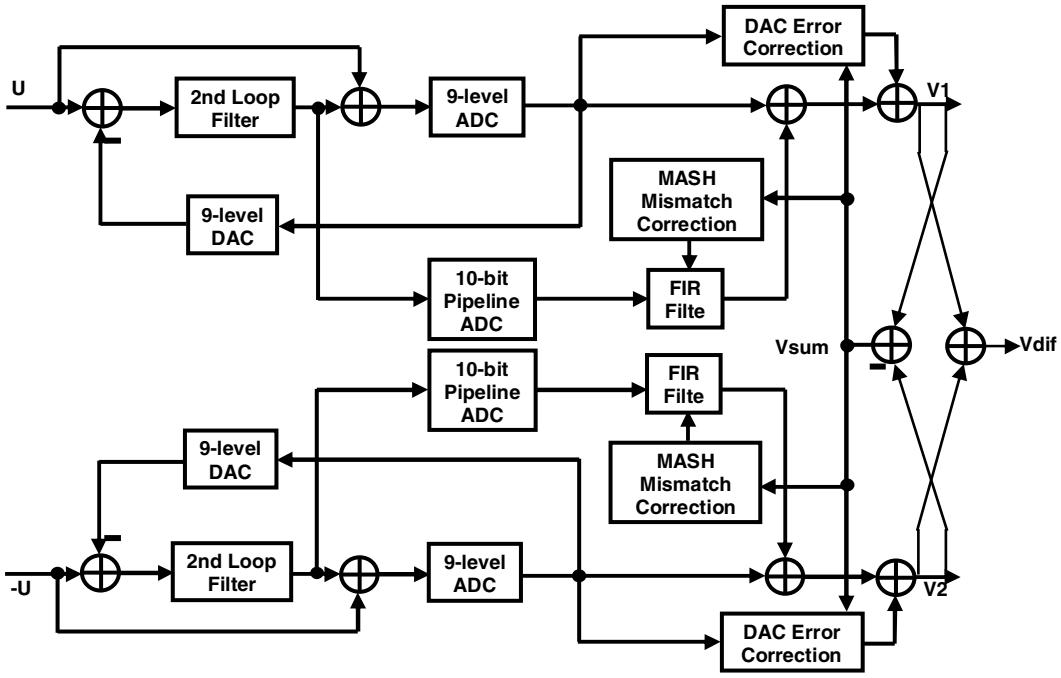

Fig.7-1 Modified dual-path structure

Secondly, a Segmented DWA technique was proposed for the high speed DSM operation. Compared with conventional DWA, it doesn't have problems with pattern tones. In addition, its implementation can be faster and simpler.

Bibliography

[1-1]. P. Balmelli, Q. Huang, "A 25MS/s 14b 200mW ΔΣ modulator in 0.18um CMOS", *ISSCC Dig. Tech. Papers*, pp. 74-75, Feb. 2004

[1-2]. A. Bosi et al., "An 80MHz 4x oversampled cascaded ΔΣ-pipelined ADC with 75dB DR and 87dB SFDR", *ISSCC Dig. Tech. Papers*, pp. 174-175, Feb. 2005

[1-3]. I. Fujimori et al., "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8x oversampling," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820—1828, Dec. 2000

[1-4]. R. T. Baird and T. S. Fiez, "Linearity enhancement of ΔΣ A/D and D/A converters using data weighted averaging", *IEEE Trans. Circuits Syst. II*, vol. 42, no.12 , pp. 753 -762, Dec. 1995

[1-5]. F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453 -460, Aug. 1997

[1-6]. X. Wang, Y. Guo, U. Moon and G.C. Temes, "Experimental verification of a correlation-based correction algorithm for multi-bit delta-sigma ADCs," *IEEE Custom Integrated Circuits Conf.*, Oct 2004

[1-7]. P. Kiss et al., "Adaptive digital correction of analog errors in MASH ADC's – part II: correction using test-signal injection," *IEEE Trans. Circuits Syst. II*, vol. 47, no.7, pp. 629-638 ,July 2000

[1-8] Z. Zhang, J. Steensgaard, G. C. Temes "Dual-path delta-sigma modulators ",*48th Midwest Symposium on Circuits and Systems*, pp. 700-703, Aug. 2005

[1-9]. J. Li, G. Ahn, D. Chang, and U. Moon, " A 0.9V 12mW 5MSPS algorithmic ADC with 77dB SFDR," *IEEE J. Solid-State Circuits*, pp. 960-969, Apr. 2005.

[2-1]. I. Galton, "Digital cancellation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits and Syst. II,*vol. 47, no.3 , pp. 185-196, Mar. 2000.

[2-2]. R. Wang, G. C. Temes, "Split-set data weighted averaging", *IEE Electronics Letters*, vol. 42, no. 4, pp 248-249, Feb. 2006

[2-3]. C. Kuo, T. Hsueh, S. Liu, "Multi-bit delta-sigma modulator using a modified DWA algorithm", *Analog Integrated Circuits and Signal Processing*, vol. 33, pp. 289-300, 2002

[2-4]. X. Wang, *A Fully Digital Technique for the Estimation and Correction of the DAC Error in Multi-bit Delta Sigma ADCs*, Ph.D Thesis, Oregon State University, School of Electrical Engineering and Computer Science, Dec. 2003

[2-5] J. Silva, *High-Performance Delta-Sigma Analog-to-Digital Converters*, Ph.D Thesis, Oregon State University, School of Electrical Engineering and Computer Science, Jul. 2004

[2-6] Ichiro Fujimori, *High resolution CMOS analog-to-digital digital-to-analog converters using delta-sigma modulation, Ph.D Dissertation,*Hiroshima University, June 2003

[3-1] J. Steensgaard, "Self-correcting dual-path delta- sigma modulator", Technique Report, Dec. 2000

[3-2] J. Li, *Accuracy Enhancement Techniques in Low-Voltage High-Speed Pipelined ADC Design*, Ph.D Thesis, Oregon State University, School of Electrical Engineering and Computer Science, Oct. 2003

[4-1] J. Silva, U. Moon, G. C. Temes, "Low-distortion delta-sigma topologies for MASH architectures", in *proceedings of the IEEE International Symposium on Circuits and Systems* , vol. 1, pp. I-1144-7, May 2004

[4-2] R. Schreier et al., "Design-oriented estimation of thermal noise in switched-capacitor circuits ",*IEEE Trans. Circuits and Syst. II,* vol.52, no.11, pp.2358—2368, Nov. 2005

[5-1] Y. Geerts, M. Steyaert, W. Sansen," A high-performance multibit ΔΣ CMOS ADC", *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829—1840, Dec. 2000.

[5-2] T. Choi et al., "High-frequency CMOS switched-capacitor filters for communications application," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 652-664, Dec. 1983.

[5-3] K. Martin et al., " A differential switched-capacitor amplifier ",*IEEE J. Solid-State Circuits,* vol. sc-22, no.1 , pp. 104-106, Feb. 1987

[5-4] I. Mehr and D. Dalton, “A 500-MSamples, 6-bit nyquist-rate ADC for disk-drive read-channel applications," *IEEE J. of Solid-State Circuits*, vol. 34, no. 7, pp. 912--920, July 1999.

[5-5] B. Razavi and B. Wooley, “Design techniques for high-speed, high-resolution comparators," *IEEE J. of Solid-State Circuits*, vol. 27, no. 12, pp. 1916--1926, Dec. 1992

[5-6] David Johns, Ken Martin, *Analog Integrated Circuits Design*, John Wiley & Sons, Inc. ,1997

[5-7] M. Dessouky, A. Kaiser, “Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping,” *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349– 355, March 2001

[5-8] A. M. Abo , P. R. Gray, “A 1.5-V 10-bit 14-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999

[5-9] Robert Adams, Khiem Q. Nguyen, Karl Sweetland; “A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling”, *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1871-1878, December 1998.

Acronyms

ΔΣ	Delta-Sigma
ADC	Analog-to-Digital Converter
ANTF	Analog Noise Transfer Function
BiDWA	Bi-Directional Data Weighted Averaging
dBFS	Decibels Full Scale
DAC	Digital-to-Analog Converter
DC	Direct Current
DEM	Dynamic Element Matching
CM	Common Mode
CMFB	Common-Mode-FeedBack
CMOS	Complementary Metal–Oxide–Semiconductor
DNC	DAC Noise Cancellation
DNTF	Digital Noise Transfer Function
DSM	Delta-Sigma Modulator , (See Fig.1-5)
ENOB	Effective Number Of Bit
ETF	Error Transfer Function
FIR	Finite Impulse Response
FS	Full Scale
FPDWA	Four Pointer Data Weighted Averaging
ILA	Individual Level Averaging
IOS	Input Offset Storage
IRN	Input Referred Noise
MASH	Multi-stAge-noise-SHaping
MDAC	Multiplying-Digital-to-Analog Converter
NCL	Noise Cancellation Logic
NTF	Noise Transfer Function

Opamp	Operational Amplifier
ORN	Output Referred Noise
OSR	Over-Sampling Ratio
OTA	Operation Transconductance Amplifier
PSD	Power Spectra Density
P2P	Peak-To-Peak
RMS	Root Mean Square
SC	Switched-Capacitor
SDWA	Split-set Data Weighted Averaging
SeDWA	Segmented Data Weighted Averaging
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal to Quantization Noise Ratio
SSBLMS	Sign-Sign-Block-Least-Mean-Square
STF	Signal Transfer Function
TF	Transfer Function
UGBW	Unit Gain Bandwidth