AN ABSTRACT OF THE THESIS OF

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in Electrical and Electronics Engineering (Major)

presented on 6-7-72. (Date)

Title: THE MOS TETRODE TRANSISTOR



Abstract approved: James C. Looney

The MOS tetrode transistor is studied in this project. This device is ideally suited for high frequency and switching application. In effect it is the solid state analogy of a multigrid vacuum tube performing a very useful multigrid function. A new structure is developed for p-channel 10 ohm-cm. silicon substrate of (111) crystal orientation. This structure consists of an aluminum control gate $G_1$ buried in the pyrolytic $SiO_2$, or E-gun evaporation $SiO_2$, with thermal oxide for the control gate insulator. An offset gate $G_2$ produces another channel $L_2$ and causes a longer pinchoff region in the device. The drain breakdown can be maximized so as to approach bulk breakdown as the result of the redistribution of the surface field. The Miller feedback capacitance $C_{G1-D}$ is very low, approaching values similar to those of the vacuum pentodes.

This paper describes the design, artwork, pyrolytic $SiO_2$ and E-gun evaporation $SiO_2$ process. The V-I

characteristics, dynamic drain resistance, capacitance, small signal equivalent circuit and large signal limitation, and drain breakdown voltage are also discussed.

# THE MOS TETRODE TRANSISTOR

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1973

APPROVED:

Redacted for Privacy

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in charge of major

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Date thesis is presented 6-7-72.

Typed by Erma McClanathan for Thawee Limvorapun

ACKNOWLEDGMENTS

I wish to express my sincere appreciation to my advisor, Professor James C. Looney, for his continuous guidance and constructive criticism during the course of this research.

Also, gratitude is expressed to Professor Harley A. Perkins for suggestions, and to Mr. Mark L. Nelson and Mrs. Blanche B. Stroup for consultation in preparing the manuscript.

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## INTRODUCTION

The objective is design of transistors suited to high frequency application, having low Miller effect capacitance similar to that of the cascode amplifier. It was found that the metal oxide semiconductor (MOS) tetrode transistors were best suited to the idea of multigrid transistors which bring to the solid-state amplifier high frequency characteristics of the pentode vacuum tube (5). Some high frequency devices, such as the cascode amplifier of the triode vacuum tube, have long been used to reduce the effective feedback capacitance in unneutralized amplifiers, thus improving stability and bandwidth. The MOS tetrode transistor can accomplish similar results. The MOS tetrode transistor overcomes the problem of high Miller feedback capacitance $C_{G1-D}$ between control gate $G_1$ and drain and the regenerative instability in high frequency amplifiers.

MOS tetrode transistors with two stacked gates were constructed. Gate $G_1$ was the control gate, and gate $G_2$ was the offset gate. The gate insulators were in the layers of $SiO_2$: the first layer was thermal oxide, and the second layer was pyrolytic $SiO_2$ or E-gun evaporation $SiO_2$. Either P or N channels for the devices are possible, as shown in Figures 1 and 2. The major change from the regular MOS transistor was the addition of the second gate $G_2$ which was

used to induce an inversion channel $L_2$ from the edge of the first gate $G_1$ to the drain contact. The conductivity of channel $L_2$ can be adjusted by the gate potential $V_{G2}$ to any value up to the point of gate insulation breakdown. According to Dill (5), the drain breakdown can be maximized so as to approach bulk breakdown as the result of the redistribution of the surface field.

This project consists of the design and fabrication of a 10 ohm-cm. n-type silicon wafer, with (111) crystal orientation. The pyrolytic $SiO_2$ process and E-gun evaporation of pure quartz and the methods and associated problems are discussed, together with the drain current, threshold voltage, transconductance, source drain resistance, pinchoff region and C-V characteristics. The small signal equivalent circuit and large signal limitation influence the frequency response of the devices.

Some previous MOSFET transistors have been considered. The MOSFET transistor has the property of extremely high input resistance, as high as $10^4$ ohms, while the input capacitance is rather low, about 5 pF. or less. This gives a time constant of 500 seconds. The amount of charge required on 5 pF. capacitance to reach 120 volts is only $6 \times 10^{-10}$ couloumbs, or the charge obtained by allowing 0.26 nano amp. to flow for one second (11). The high frequency performance of the MOSFET transistors was examined. Some improvement in the device was the result of a decrease in channel length from 5 to 2.5 micrometers. An increase in

maximum available power gain of about 4 db. was observed. This value fell short of the expected increase because critical fields resulting from field dependent mobility were experienced over the major portion of the channel. Although the experimental results were consistent with reduced effective mobility, the parasitic loading element was expected to limit the high frequency performance (2). Stability problems also have arisen with the conducting channel between the edge of the gate electrode and drain contact.

In 1965 the dual gate transistor, which has a single oxide layer, was developed for VHF application. The most important point in favor of this device is that the feedback capacitance is very low. The improved frequency response of the wide band amplifier eliminates a need for neutralization in the tuned amplifier. It also is suited for high frequency application such as r-f and i-f bandpass amplifiers, mixers and demodulators (2, 3). However, the performance of the Dual Gate transistors in cascode form can be seriously degraded by the center point capacitance between gate $G_1$ and gate $G_2$.

Thus the MOS tetrode transistor is promising for the cascode amplifier.

# THEORETICAL ANALYSIS OF MOS TETRODE TRANSISTOR

## Device Fundamentals

Metal-Oxide-Semiconductor tetrode transistors with two stacked gates were studied. Both P and N channel devices can be fabricated (Figures 1 and 2). The additional second gate $G_2$ produces channel $L_2$ and causes a longer pinchoff region LS. The conductivity of channel $L_2$ can be adjusted by the second gate potential $V_{G2}$ to any value up to the point of gate insulation breakdown.

Ignoring the second gate $G_2$ and letting the first gate $G_1$ modulate the entire channel, the MOS tetrode drain V-I characteristic was derived from MOS transistor characteristics ($I_D \cong I_{L1}$). If these characteristics are plotted for a family of gate voltages the results are similar to the typical curves in Figure 3.

There are two modes of operation: the enhancement-mode and depletion mode. The type of channel is determined classically by the type of majority carrier in the channel. The mode of operation is related to the state of the channel at zero gate bias. If the channel must be formed before conduction can occur, it is called the "enhancement-mode." The P-channel enhancement mode MOS tetrode structure is assumed throughout this paper.

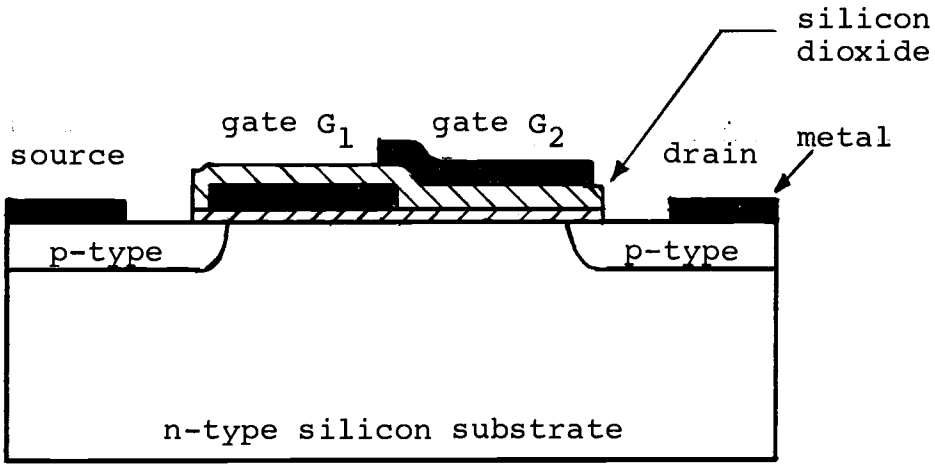



Figure 1. The cross section of a p-channel MOS tetrode transistor.

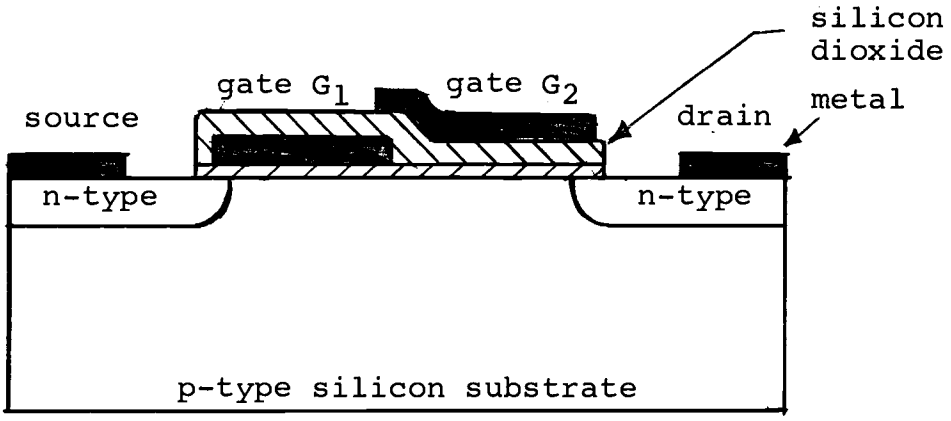



Figure 2. The cross section of an n-channel MOS tetrode transistor.

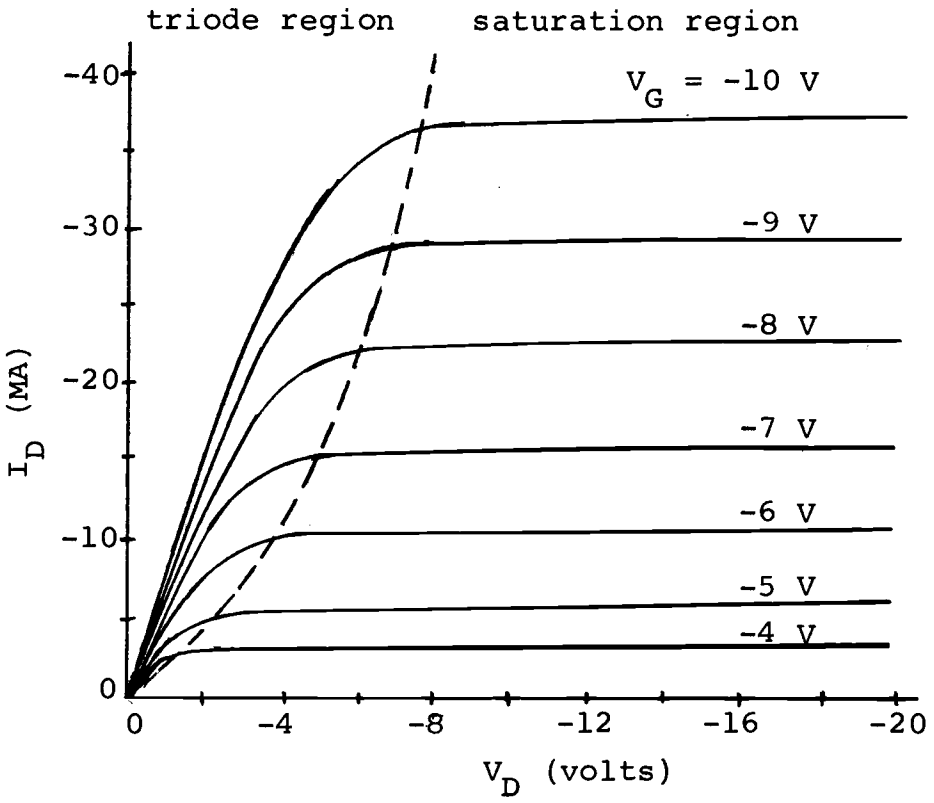



Figure 3. The typical current-voltage characteristics of the MOS p-channel enhancement type transistor.

## The Drain Current

The typical family of curves in Figure 3 shows two active regions concerned with the operation of the device:

1. The triode region (non-saturation region)
2. The saturation region

### The Triode Region

The theoretical drain current has been investigated by J. T. Wallmark, H. Johnson, and S. R. Hofstein (9). In the triode region, it is assumed that drain current depends on the channel currents ($I_D$, $I_{L1}$). It is expressed in the parameter K for convenience

so $$I_{L1} = \frac{\mu\epsilon_o\epsilon_i W}{d_{i1}l_{L1}} V_D \left[ V'_{G1} - \frac{V_D}{2} \right]$$

Let $$K_1 = \frac{\mu\epsilon_o\epsilon_i W}{d_{i1}l_{L1}}$$

$$V'_{G1} = V_{G1} - V_T$$

$$I_{L1} = K_1 V_D \left[ V'_{G_1} - \frac{V_D}{2} \right] \qquad (1)$$

$$V_{G1} \leqslant V_D \text{ (triode region)}$$

The saturation region

$$I_{L1} = \frac{K_1}{2} V'^2_{G_1} \qquad (2)$$

$$V_{G1} \geqslant V_D \text{ (saturation region)}$$

where

$\mu$ is the average surface mobility in the channel

$\epsilon_i$ is the relative dielectric constant of the insulating material

$\epsilon_o$ is the permitivity of free space ($8.85 \times 10^{-14}$ farads/cm.)

$d_{il}$ is the thickness of oxide under the gate $G_1$

W is the width of the channel

$I_{L1}$ is the channel length measured from the source to the edge of pinchoff region

$V_D$ is the voltage from drain to source

$V_{G1}$ is the voltage from gate $G_1$ to the source

$V_T$ is the threshold voltage

## The Threshold Voltage

$V_T$ is the first gate $G_1$ voltage required to neutralize, in effect, the immobile charge above and below the channel region. Any additional gate voltage over and above $V_T$ will produce a gate charge that must be neutralized by an equal amount of mobile channel charge (1). In the following calculations, a typical value of $V_{ss}$ is used. Assume $d_{il} = 1500$ Å of oxide thickness under the gate $G_1$

$$\epsilon_{ox} = \frac{1}{3} \text{ pF/cm.}$$

then

$$V_{ss} = - \frac{d_{il}}{\epsilon_{ox}} Q_{ss}$$

$$= - 2.88 \text{ volts}$$

$$V_T = V_{IT} + V_{ss}$$

or

$$V_T = -K_1 \sqrt{\phi_s + V_{BG}} + V_{ss} \qquad (3)$$

where

$V_{IT}$ is the intrinsic threshold voltage

$V_{ss}$ is the gate voltage through the same constant, C, as is the bulk charge.

$$K_1 = \pm \frac{d_{il}}{\epsilon_{ox}} \sqrt{2q\epsilon_s N}$$

0.62 (n-type 10 ohm-cm., 1500 Å)

$$\phi_s = 2\phi_F = -0.58 \text{ volts}$$

$V_{BG}$ is the reverse-biased voltage of the substrate with respect to the source

$$V_{IT} = -0.63 \sqrt{0.58} = 0.49 \text{ volt}$$

$$V_T = -2.88 - 0.49 = -3.37 \text{ volts}$$

## Transconductance

The gain parameter of the device is the forward transfer-conductance ratio. Normally the parameter of transconductance is determined in the saturation region. Mathematically, this is written as

$$g_m = \frac{\partial I_D}{\partial V_{G1}}\bigg|_{V_D}$$

$$g_{mL1} = K_1 V'_{G1} \qquad (4)$$

Source-Drain Resistance

The triode region is so named because of the strong influence drain voltage has upon drain current in this region. In the MOS tetrode channel $L_1$ and $L_2$ form a continuous current path from source to drain if

$$V_D < V'_{G1} + I_D r_{L2}$$

$$r_D = r_{L1} + r_{L2}$$

H. G. Dill (5) reported that if the channel lengths $L_1$ and $L_2$ are similar and gate $G_2$ is biased for the highest drain breakdown potential $V_{DBM}$, the additional resistance of channel $L_2$ can in most cases be neglected.

In the saturation region

$$V_D \gg V'_{G1} + I_D r_{L2}$$

The source-drain resistance is now dominated by the large dynamic resistance $r_{dL1}$ of channel $L_1$

$$r_{dL1} \gg r_{L1} + r_{L2}$$

The finite dynamic drain resistance expressed by Hofstein and Heiman ( 9 ) is:

$$r_{dL1} = \frac{\Delta V_D}{\Delta I_D} \simeq \frac{\Delta V_D}{\frac{V'_{G1}}{l_1}\,\mu\,\frac{C_{L1-L2}}{l_1}\,\Delta V_D} \qquad (5)$$

where

$\frac{V'_{G1}}{l_1}$ is the average drift field along the channel $L_1$

$\frac{C_{L1-L2}\Delta V_D}{l_1}$ is the channel sheet charge per unit length induced by $\Delta V_D$

$C_{L1-L2}$ is the effective coupling capacitance between channel $L_1$ and drain area

$$C_{L1-L2} \simeq \frac{l_1}{l_1-2l_{LS}} \frac{\epsilon_o \epsilon_s W}{\beta} \tag{6}$$

$\beta$ expresses the shielding effect of the substrate depletion region

$$r_{dL1} \simeq \frac{\beta(l_1^2 + 2l_1 l_{LS})}{\mu W \epsilon_o \epsilon_s} \frac{1}{V'_{G1}} \tag{7}$$

$l_{LS}$ is the pinchoff region, given in (11).

From equation (7), the dynamic drain resistance increases with increasing $V_D$ because the pinchoff region LS is wider. The feedback from drain to channel $L_2$ toward the drain electrode increases with drain potential $V_D$, and may be estimated from the dynamic drain resistance $r_{dL1}$ as shown in Figure 4.

Length of the pinchoff region increases slowly as the drain potential increases from $V_{DP}$ to $V_{DK}(l_{LS} \ll l_2)$. Also, $r_{dL1} = r_{dL1L}$ has the same value for MOS tetrodes and MOS transistors, shown in Figures 5, 6.

When the field voltage is applied at the second $G_2$, the channel $L_1$ builds up as soon as the pinchoff region LS

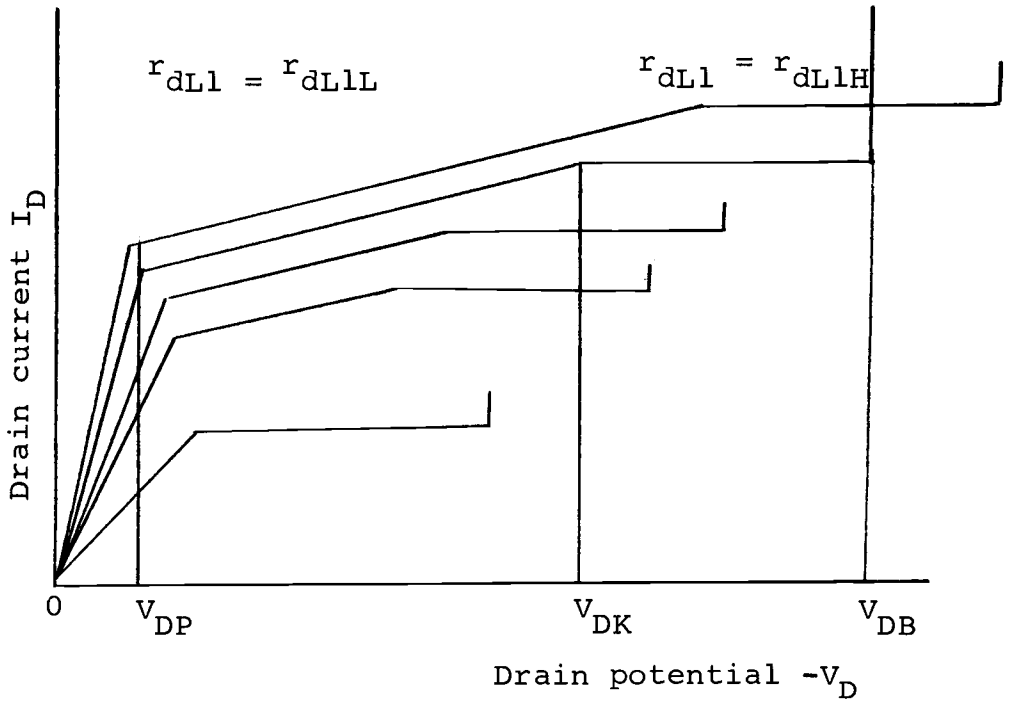



Figure 4. The influence of $V_D$ and $V_{G2}$ on the MOS tetrode transistor saturation drain resistance to define $r_{dL1L}$ and $r_{dL1H}$.

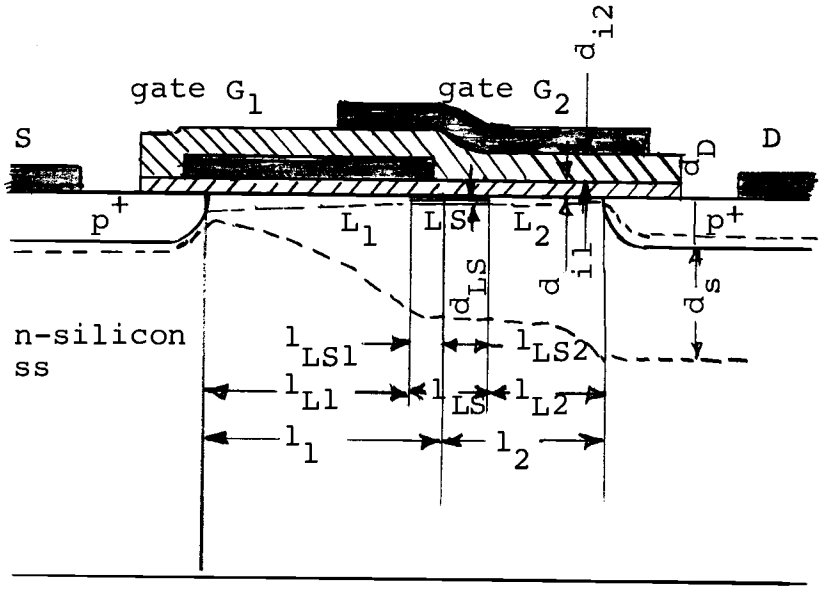



Figure 5. The cross section of a p-channel MOS tetrode with offset channel $L_2$ induced by the field from gate $G_2$.

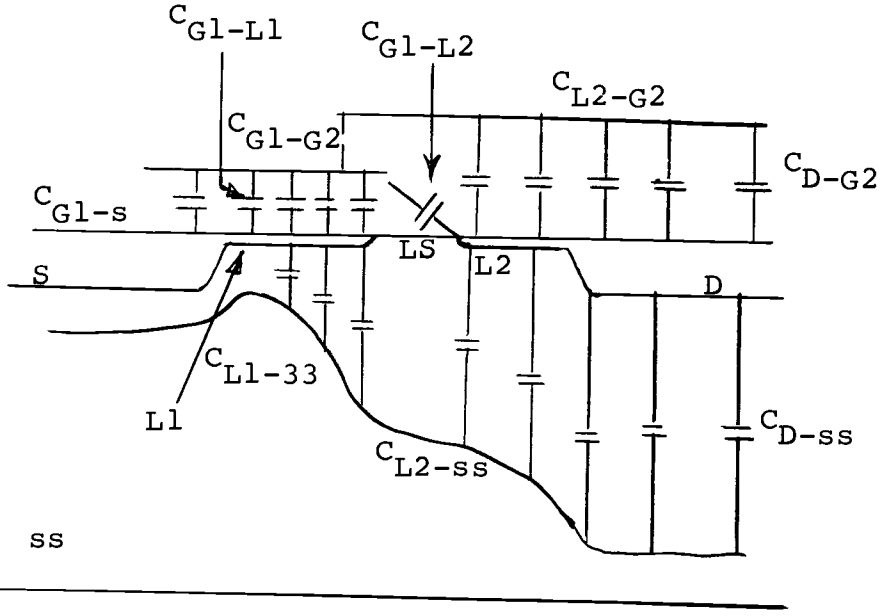



Figure 6. The cross section of the MOS tetrode channel region with resistance and capacitance elements marked.

widens. Establishing this field has two effects on the operation of the MOS tetrode at $-V_D > -V_{DK}$. Firstly, the gate $G_2$ is coupled to the channel $L_1$; secondly, it seems that the field from gate $G_2$ reduces the effective length $l_L$ with increase of $V_{G2}$ (5). This results in higher values of $g_m$ and $I_D$ than in the regular MOS transistor.

## The Pinchoff Region of the MOS Tetrode Transistor

The pinchoff region $l_{LS}$ starts at the drain end of the first gate and spreads with the growing drain potential. It spreads out in both the directions of source and drain, as $l_{LS1}$ and $l_{LS2}$. From Wright's calculation (13), $l_{LS1}$ is small enough to be neglected when compared with $l_{LS2}$.

Thus $l_{LS} = l_{LS2}$.

$l_{LS}$ is a function of design parameters and applied DC bias (5).

$$l_{LS} = \frac{l}{\delta} \frac{1}{\frac{\epsilon_i (V_{G2} - V_D)}{\epsilon_s d_{i2} V_D} - \left[\frac{2Ng}{\epsilon_s \epsilon_o V_D}\right]^{\frac{1}{2}}} \qquad (8)$$

$\delta$ = field correction factor related to LS for the shielding effect of the substrate depletion region. For 10 ohm-cm. silicon $\delta = 2$, N = number of donor or acceptor states in the substrate material. As the first approximation, it is assumed that the entire channel region LS is depleted.

The space charge current $I_{LS}$ is defined for the pinch-off region which is dependent on the drift field and carrier mobility.

Small drift fields and constant carrier mobility can be assumed to correlate with the space charge current (10,12).

$$I_{LS} \propto \frac{V_D}{l_{LS}^3}$$

Large drift fields and the carrier are velocity limited.

$$I_{LS} \propto \frac{V_D}{l_{LS}^2}$$

The drift field in the pinchoff region of the MOS Tetrode is generally above $10^4$ V/cm. (5), indicating that limited carrier velocity can be assumed.

## The $V_D$-$I_D$ Characteristics of the MOS Tetrode

The $V_D$ - $I_D$ characteristic of the MOS tetrode depends upon the magnitude of $I_{Ll}$ and $I_{LS}$. The $V_D$ - $I_D$ curve is shown in Figures 7, 8.

In the case $I_{Ll} \ll I_{LS}$, injection from $L_1$ into LS is limited and $I_D = I_{Ll}$ is dependent on $V_D$, so

$$I_{Ll} = \frac{K_1}{2} V'^2_{Gl}$$

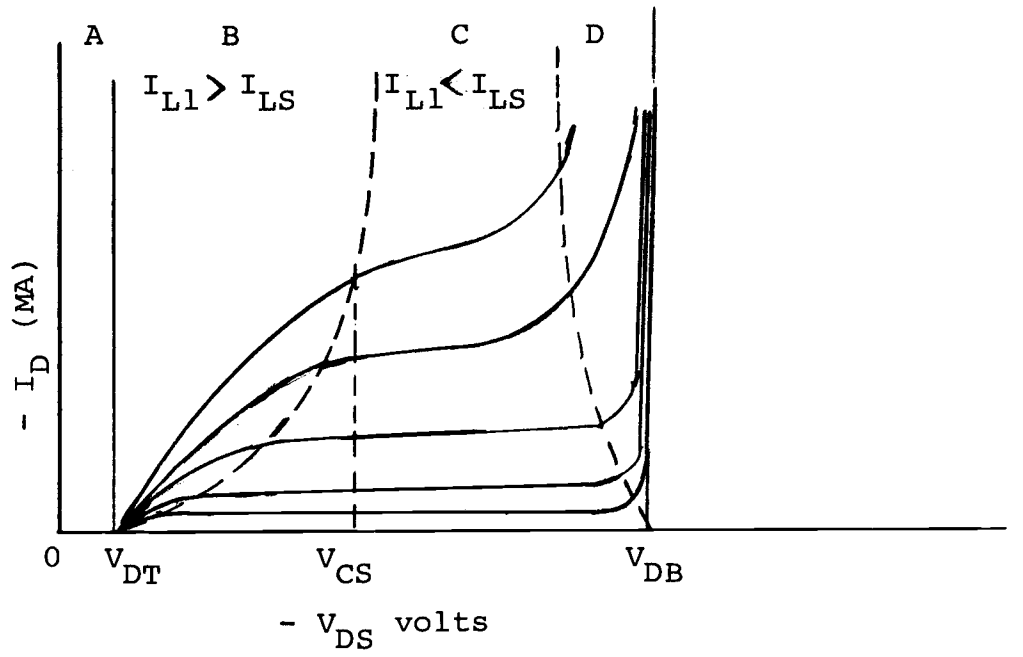



Figure 7. V-I characteristics of a p-channel MOS tetrode with $L_2$ not present.

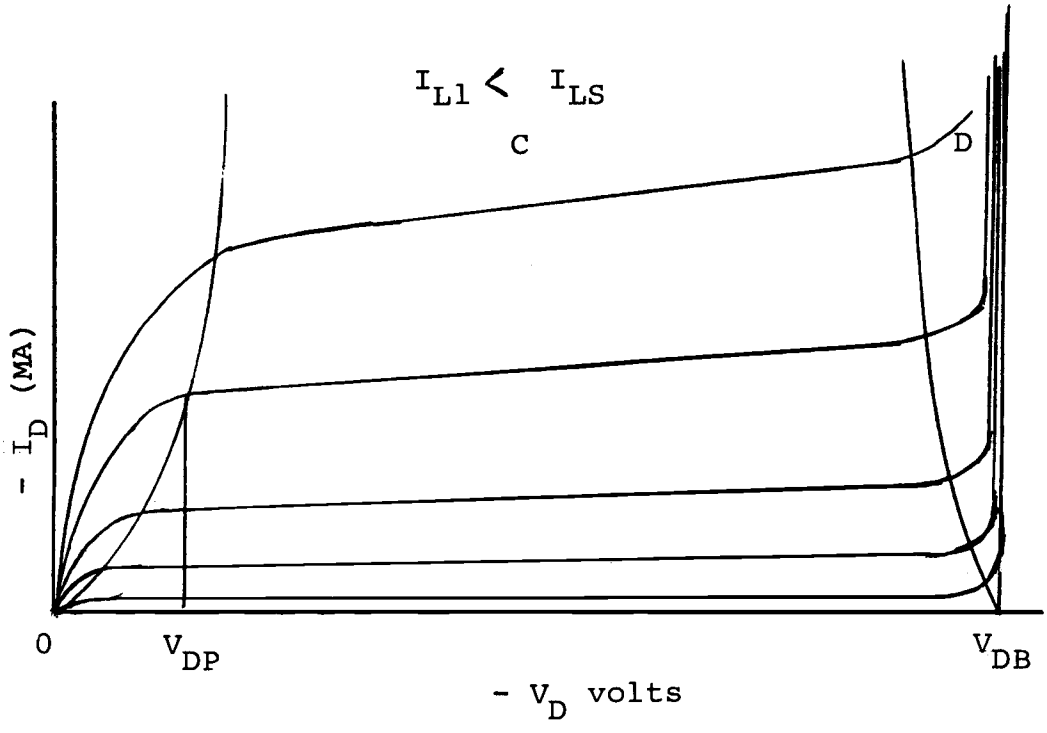



Figure 8. V-I characteristics of a p-channel MOS tetrode with channel $L_2$ present.

where

$$K_1 = \frac{\mu W \epsilon_i \epsilon_o}{d_{i1} l_{L1}}$$

$$V_G' = V_{G1} - V_T$$

In the case $I_{L1} \gg I_{LS}$, unlimited injection from $L_1$ into LS can be assumed, and $I_D = I_{LS}$ is a strong function of $V_D$.

The MOS tetrode transistor is influenced by the width of the inversion channel $L_2$. The discussion by H. G. Dill (5) of the inversion channel is concerned with two cases.

Case 1. No inversion channel present. The voltage supply at gate $G_2 = 0$. The $V_D - I_D$ characteristic can be separated into four regions (Figure 7).

Region A. The drain junction is reverse biased and $I_D$ consists only of a small leakage current from drain to substrate. The depletion region widens steadily for increasing drain potential until the punchthrough of the channel $L_1$ occurs at $V_D = V_{DT}$. The magnitude of $V_{DT}$ depends on the offset distance, the substrate resistivity and the width of a possible enhancement or depletion channel $L_2$.

Region B. The drain current is dominated by the space charge current $I_{LS}$ because $I_{L1} > I_{LS}$. This $V_D - I_D$ characteristic curve follows a square law characteristic (triode region). The modulation of $I_D$ by $V_{G1}$ is a result of the interaction between channel $L_1$ and space-charge region LS.

Region C. The space-charge current $I_{LS}$ has grown to the point where $I_{L1} < I_{LS}$ and the drain $I_D$ is defined by $I_{L1}$ according to $I_{L1} = K_1/2\ V'^2_{G1}$ . The space-charge current is limited to the constant current $I_{L1}$ supplied by channel $L_1$ as soon as $I_{L1} < I_{LS}$ .

Region D. The drain current is multiplied by impact ionization.

Case 2. When the channel $L_2$ is present the length of LS is given by (11). The $V_D$ - $I_D$ characteristic is shown in Figure 8. Region C exists for the whole drain voltage range up to a drain current $I_D = I_{LS}$. Therefore, the effect of the space-charge characteristic can be neglected for a strong inversion channel $L_2$ as far as the $V_D$ - $I_D$ characteristic is concerned. For increasing values of $V_{G2}$, channel $L_2$ appears and, consequently, region C starts to dominate over regions A and B.

## The MOS Tetrode Capacitor

There are several kinds of capacitances associated with the MOS tetrode transistor, shown in Figure 6.

1. The intrinsic capacitance is due to the charge stored on the gate and channel of the device. It is defined as the total value of gate oxide silicon parallel plate capacitance. It depends upon the oxide thickness.

$$C_o = \frac{\epsilon \text{ oxide}}{(t \text{ oxide}) x (\text{Area of gate})}$$

for an oxide thickness of 1200 Å, typically

$$C_o = 0.19 \text{ pF/mil}^2$$

2. The parasitic capacitance falls into the area of the overlap capacitance due to the fact that the gate metal overlaps into the source and drain areas. The junction capacitance is related to the back-bias of the diffused junction of the source and drain. The junction capacitance depends on the amount of reverse bias and is found to be given approximately by the formula

$$C = \frac{0.08}{\sqrt[3]{0.6+V_R}} \quad \text{pF/mil}^2$$

3. The space-charge capacitance arises from the depletion of majority carriers from the layer near the surface of the silicon. The space-charge capacitance per unit area is:

$$C_{SC} = \frac{K_{SC}\epsilon_o}{Xd}$$

where

$K_{SC}$ = relative permitivity of the semiconductor

$\epsilon_o$ = permitivity of free space ($8.86 \times 10^{-14}$ f/cm)

Xd = space-charge layer width

## C-V Characteristics

When the bias on the metal electrode is varied, the majority carrier concentration near the oxide-silicon interface can be accumulated above the concentration in the bulk concentration or inverse. Capacitance-voltage is shown in Figure 9.

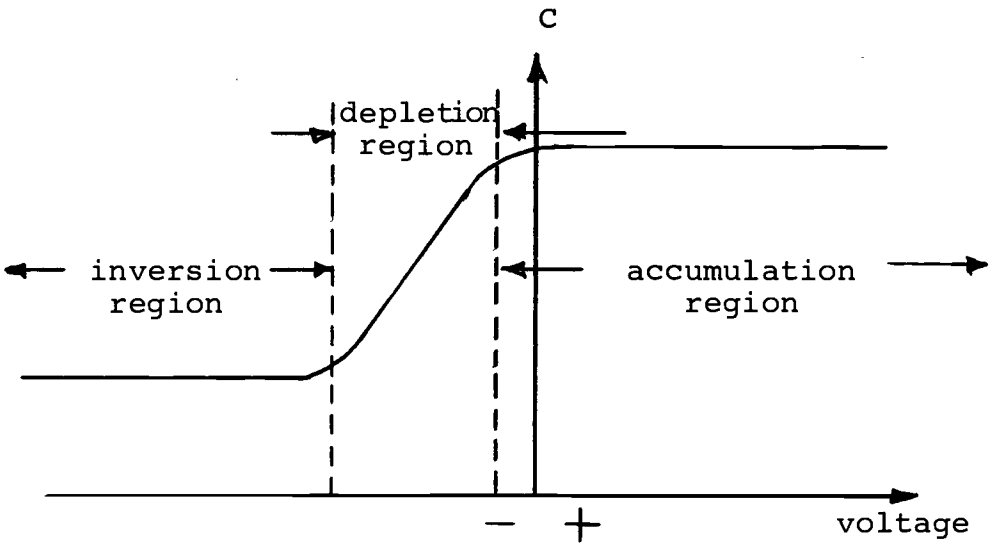



Figure 9. Typical capacitor voltage characteristics of an MOS capacitor n-type silicon substrate.

The bias voltage change from positive voltage to negative voltage creates three regions: accumulation region, depletion region and inversion region, explained by Grove et al. (7).

The additional parasitic capacitances of MOS Tetrode Transistors $C_{G1-S}$, $C_{G1-L2}$, $C_{D-G2}$ and $C_{D-SS}$ are functions of device design and biasing conditions shown in Figure 6.

The most interesting capacitance is $C_{G1-L2}$ (the Miller feedback capacitance).

## Frequency Response

The MOS tetrode transistor consists of two channel regions, $L_1$ and $L_2$, so that the response time depends on the signal amplitudes. For large signal amplitudes, the modulation of channel $L_2$ by the signal may reduce the response time. For small signal amplitudes it can be assumed the length of channel $L_2$ is fixed by the DC bias (11). Frequency response is a function of the time constant of the offset channel region (5). The high frequency equivalent circuit is shown in Figure 10. The two main frequency limiting time constants are $\tau_1 = r_1C_1$ of channel $L_1$ and $\tau_2 = r_2C_2$ of channel $L_2$.

Because of the time constant of $\tau_1$ and $\tau_2$ in the high-frequency region, the "y" parameters are used to solve the problem. The approximation (5, 6) of the parameters for the case where $\tau_2 \gg \tau_1$ and $r_{dL1} = \infty$ is:

$$y_{11} \approx \omega^2 r_1 C_1^2 + j\omega(C_{GS} + C_{GD} + C_1) \tag{9}$$

$$y_{22} = \frac{(\frac{\omega}{\omega_2}^2)(C_{GD} + C_2)}{1 + (\frac{\omega}{\omega_2})^2} + j\omega\left[C_{DS} + \frac{C_{GD} + C_2}{1 + (\frac{\omega}{\omega_2})^2}\right] \tag{10}$$

$$y_{12} = \frac{(\frac{\omega}{\omega_2}^2)\ C_{GD}}{1+(\frac{\omega}{\omega_2})^2} - j\omega\ \frac{C_{GD}}{1+(\frac{\omega}{\omega_2})^2} \tag{11}$$

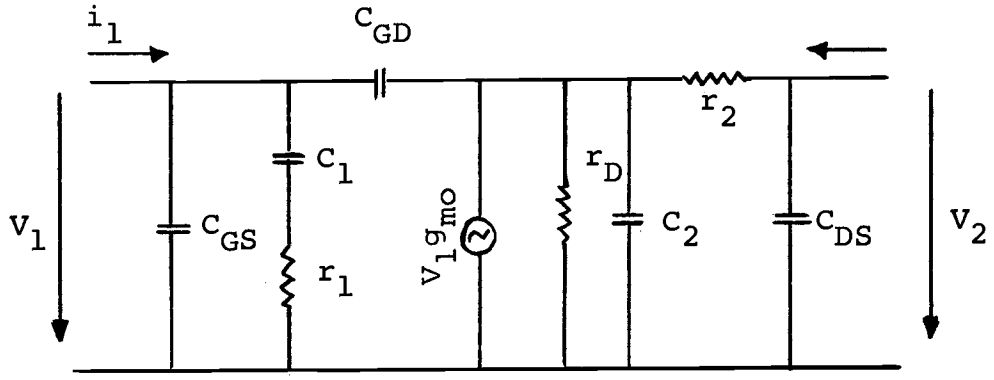



Figure 10. The equivalent circuit of an MOS tetrode transistor at high frequency.

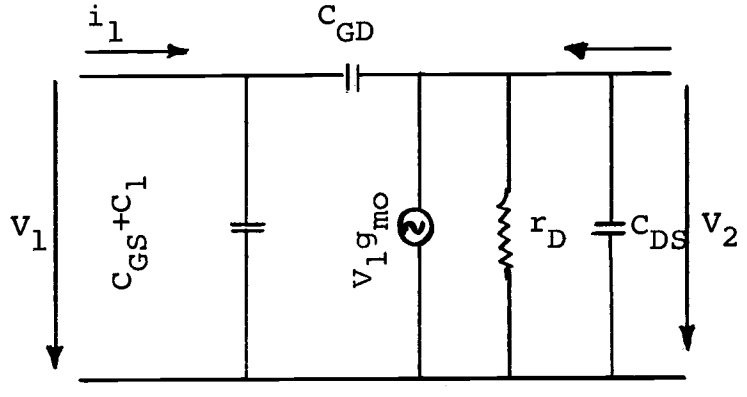



Figure 11. The equivalent circuit of an MOS tetrode transistor at low frequency.

$$y_{21} = \frac{g_{mo} - (\frac{\omega}{\omega_2})^2 C_{GD}}{1 + (\frac{\omega}{\omega_2})^2} - j\omega \frac{C_{GD} + (\frac{g_{mo}}{\omega_2})}{1 + (\frac{\omega}{\omega_2})^2} \quad (12)$$

Where

$$\omega_1 = \frac{1}{\tau_1} \quad (13)$$

if $C_{GD} \ll C_2$ , $\omega_2 = \frac{1}{\tau_1}$ (14)

$g_{mo}$ is the small signal DC transconductance in the frequency range $\omega < \omega_2$ .

The peak amplitude of $y_{21i}$ at $\omega_2$ and the polarity change of $y_{21r}$ become effective at the point where

$$\omega_3 \simeq \sqrt{\frac{g_{mo}}{\tau_2 C_{GD}}} \quad (15)$$

The circuit may be derived from y parameters.

$$C_{GD} = -\frac{y_{12i}}{\omega} \quad \text{for } \omega < \omega_2 \quad (16)$$

$$C_1 = \left[\frac{y_{11i}}{\omega} - C_{GS} - C_{GD}\right] \quad \text{for } \omega_1 > \omega > \omega_2 \quad (17)$$

$$C_2 = \sqrt{\frac{y_{22i}}{\omega^2 r_2}} - C_{GD} \quad \text{for } \omega < \omega_2 \quad (18)$$

$$r_1 = \frac{y_{11r}}{C_1^2 \omega^2} \quad \text{for } \omega_1 > \omega > \omega_2 \quad (19)$$

$$r_2 = \frac{1}{y_{22r}} \quad \text{for } \omega > \omega_2 \quad (20)$$

$$f_2 = \frac{1}{2} \pi \tau_2 \quad (21)$$

For the low-frequency region, if we assume $\tau_1\omega \ll 1$ and $\tau_2 \ll 1$, the basic equivalent circuit shown in Figure 11 is valid.

## The Drain Breakdown Potential

The drain breakdown potential depends upon the redistribution of the surface from the drain junction to gate $G_1$ as a function of gate $G_2$ potential. This phenomenon also agrees with Grove's experiment (7).

The approximate value of the maximum drain breakdown potential $V_{DBM}$ may be calculated if it is assumed that the field constant along the pinchoff region (5) is:

$$V_{DBM} \simeq E_{AV} l_2 \tag{22}$$

The critical avalanche field $E_{AV}$ is about $3\text{x}10^5$ V/cm. for a 10 ohm-cm. n-silicon substrate.

The $V_{DBM}$ is also limited by thickness of the insulator under gate $G_2$. The required minimum gate insulator thickness $d_{i1} + d_{i2}$ for a given value of $V_{DBM}$ is:

$$d_{i1} + d_{i2} \geqslant \frac{V_{DBM}}{2\text{x}10^2} \ \mu\text{m} \tag{23}$$

## CONSIDERATION OF THE DESIGN

The silicon wafers can be of n-type or p-type. Higher resistivity of substrate material increases drain breakdown voltage because the drain-gate field dominates. In this paper a 10 ohm-cm. wafer is used.

Source-drain junction depth depends on diffusion time. Boron deposition occurs in 15 minutes at 1100°C (boron diffusion furnace) in air. Typical source-drain junction depth is approximately 0.13 mil.

The gate dielectric material used was silicon oxide. The first gate $G_1$ oxide layer was grown with phosphorus stabilization (wet oxidation 5.5 minutes, approximately 1500 Å). The second Gate $G_2$ oxide layer was grown with the pyrolytic process and an E-gun evaporation process. These two processes will be discussed under Fabrication of the MOS Tetrode Transistor. These types of silicon oxide are suitable for 5000 Å thickness.

Aluminum was used for forming contacts, interconnecting leads and the gate electrodes.

Different channel lengths and widths are shown in Table I. The fabrication design of the MOS tetrode transistor is similar to that for an MOS transistor. It includes consideration of the V-I characteristic, breakdown potential, dynamic drain resistance, small equivalent circuit and large signal limitation. The frequency response

TABLE I. DEVICE DIMENSIONS

| Device No. | Channel Length $L_1$(mil) | | Channel Length $L_2$(mil) | | Channel Width $W_1$(mil) | | Channel Width $W_2$(mil) | |
|---|---|---|---|---|---|---|---|---|
| | Mask | Actual | Mask | Actual | Mask | Actual | Mask | Actual |
| 1 | 0.35 | 0.30 | 0.45 | 0.4 | 25 | - | 24 | - |
| 2 | 0.35 | 0.30 | 0.25 | 0.2 | 25 | - | 24 | - |

No. 1 Source Area 118.34 $mil^2$
Drain Area 30.25 $mil^2$

No. 2 Source Area 119.44 $mil^2$
Drain Area 30.25 $mil^2$

First silicon oxide layer $d_{11}$ = 1500 Å

Second silicon oxide layer $d_{12}$ = 5000 Å

10 Ω-cm silicon substrate

No. 1 is the left device of the photo mask
No. 2 is the right device of the photo mask

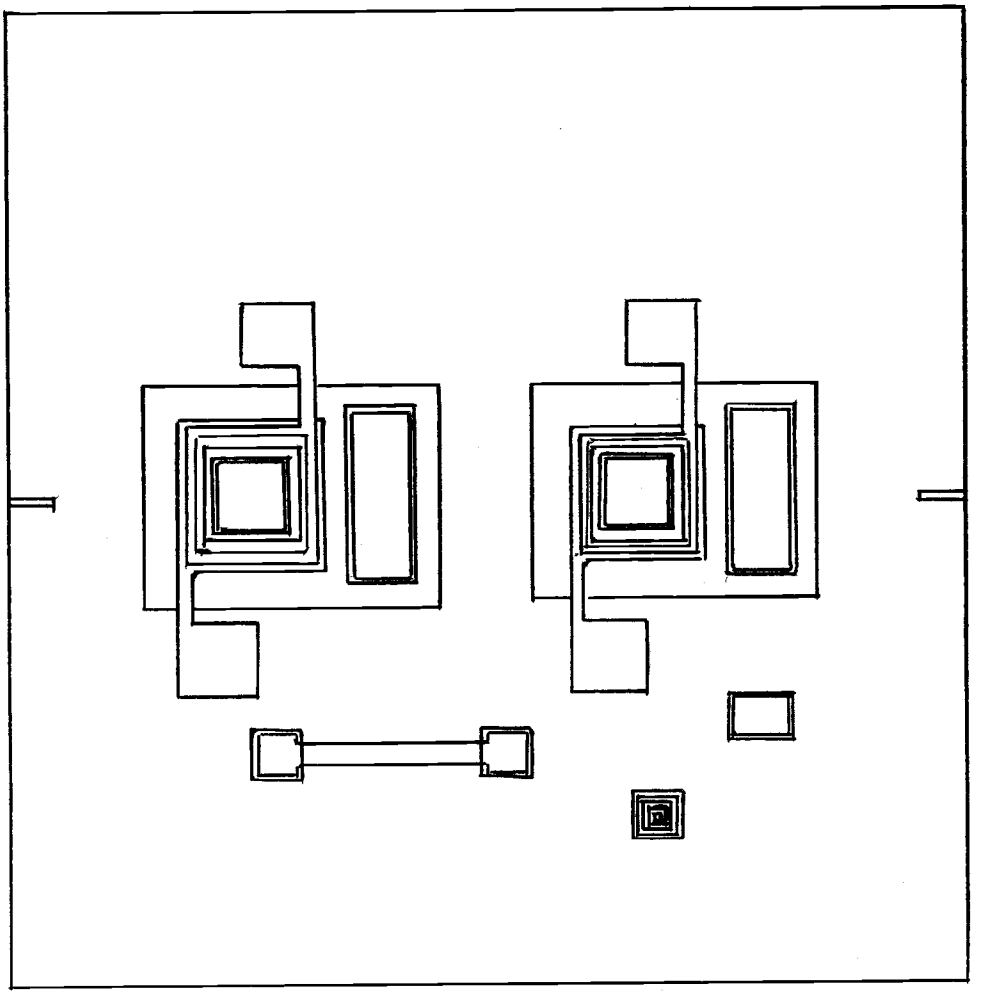
Both device No. 1 and device No. 2 are shown in Figure 12.

Fabrication of the design of the MOS tetrode transistor is more complicated than that of the regular MOS transistor. There are at least five photo masks, such as:

1. Photo mask for source-drain window
2. Photo mask for gate oxide control
3. Photo mask for metal gate one etching
4. Photo mask for open contact
5. Photo mask for metal and second gate etching

and switching application are also discussed in the previous analysis and theory of the MOS tetrode transistor.

The master mask of the MOS tetrode transistor can be drawn from design considerations as shown in Figure 12.



Scale 1 inch : 10 mil.

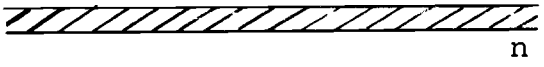
Figure 12. The master mask of an MOS tetrode transistor.

## FABRICATION OF THE MOS TETRODE TRANSISTOR

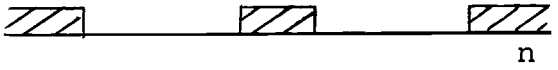
The MOS tetrode transistors were fabricated on a 10 ohm-cm ($N_C = 5x10^{14}$ $cm^{-3}$) n-type silicon wafer with 111 crystal orientation. The processing steps for an MOS tetrode transistor in simplest configuration are shown in Figure 13-a and -b.

The initial cleaning procedure is explained in detail in the Appendix. Initial oxidation to produce a silicon oxide 8500 Å thick required an oxidation time of two hours with wet oxygen 0.4 cfh at 95°C, and 30 minutes with nitrogen at 1.0 cfh, both in the furnace at temperature 1100°C. After oxidation the substrate was removed and allowed to cool. Source-drain openings were made on the silicon oxide layer by the use of the first mask and the photographic process with AZ-1350 photo resist. The etching time in buffered HF 4:1 took 7.5 minutes to maintain the proper channel length. The photo resist was removed by acetone and rubbing with a cotton swab. Then the wafer was placed in the ultrasonic tank with acetone, left for three minutes, and rinsed with DI water.

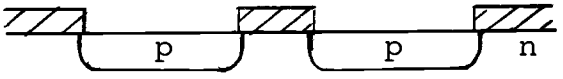
Before the source-drain deposition, the wafer was boiled for ten minutes and rinsed with DI water and blown dry with nitrogen. For the n-type substrate, 2:1 borofilm was used as the source material. The boron deposition required 15 minutes in the furnace at 1100°C in air. After



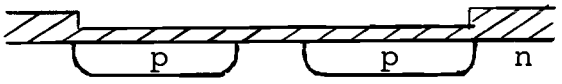

Step 1. Initial oxidation 8500 Å



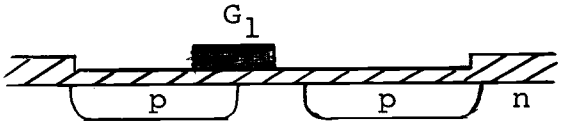

Step 2. Window opening for source-drain diffusion



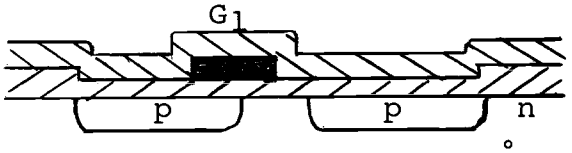

Step 3. Source-drain diffusion




Step 4. Gate oxide regrown 1500 Å

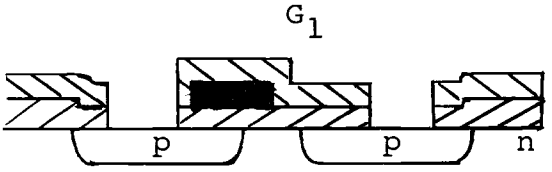



Step 5. Evaporation and metal etching for gate $G_1$

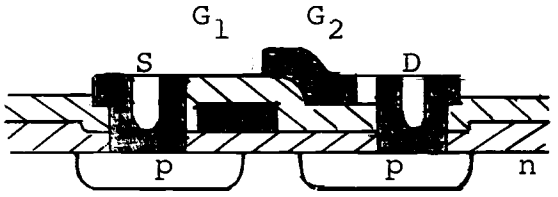



Step 6. Second layer oxide 5000 Å, grown by pyrolytic process or E-gun evaporation

Figure 13a. The processing steps for an MOS tetrode transistor in the simplest configuration.




Step 7. Open contact for source-drain and gate $G_1$




Step 8. Evaporation and metal etching for source-drain contact, gate $G_1$ and gate $G_2$

Figure 13b. The processing steps for an MOS tetrode transistor in the simplest configuration.

deposition the wafer was boiled for 30 minutes in DI water for removal of any possible boron film. Then the wafer was etched in buffered HF 4:1 for half a minute to remove the oxide film grown during the deposition.

A photo mask was applied for gate oxide control. Cleaning before gate mask etching is explained in the Appendix. The photo mask for gate oxide etching was the same as the one previously discussed. The gate oxide etching time was the same as the source-drain etching time. After etching, the sheet resistance was measured and found to be 20 ohm-cm.

Gate oxide regrows with phosphorus compensation. The wafer was put in the oxidation furnace. It took 5.5 minutes to get an oxide thickness of 1500 Å with furnace temperature at 1100°C and oxygen flow of 0.4 cfh through the water at 95°C. Then the wafer was transferred to the phosphorus deposition furnace. Phosphorus was deposited for ten minutes. At the end of the deposition, the wafer was removed back to the oxidation furnace for 6.5 minutes of nitrogen treatment. For the photo mask for metal gate $G_1$, the wafer was cleaned before metal evaporation by being boiled in water for 15 minutes and blown dry with nitrogen. Then the wafer was baked before being placed in a small vacuum system. Aluminum was evaporated to 5000 Å thickness and alloyed for five minutes in the alloying furnace at 530°C with nitrogen flow rate of 2.0 cfh. Then the wafer

was annealed for 30 minutes at 400°C in nitrogen. Tests made by Scotch tape assured good ohmic contact. Then photo resist was applied and photography was made and developed the same as in the previous process. Aluminum was etched off the substrate (except for the gate area). Photo resist was removed by acetone, and the DI water rinse was repeated. Next, the wafer was baked for five minutes at 150°C. Then the wafer was ready for deposition of the second layer of $SiO_2$ over gate $G_1$ and the thermal oxide layer. In the application of the second layer of $SiO_2$, two processes were considered to protect the aluminum gate $G_1$ from damage: one was the pyrolitic process, the other was E-gun evaporation.

Pyrolytic Process for $SiO_2$ Film

Silicon oxide film grown by the pyrolytic process is shown in Figure 14. The material consisted of 10% silane ($SiH_4$) in argon, nitrogen, and oxygen. The chemical components of $SiO_2$ are from the gaseous sources of the mixture of oxygen and nitrogen and $SiH_4$ diluted by argon. The composition of $SiH_4$, $N_2$, and $O_2$ introduced into the reactor was controlled with regulation valves.

The flow rate of $SiH_4$ in argon = 215 cc/min.
The flow rate of $O_2$ = 12 cc/min.
The flow rate of $N_2$ = 5428 cc/min.
The deposition rate of $SiO_2$ = 750 Å/min.

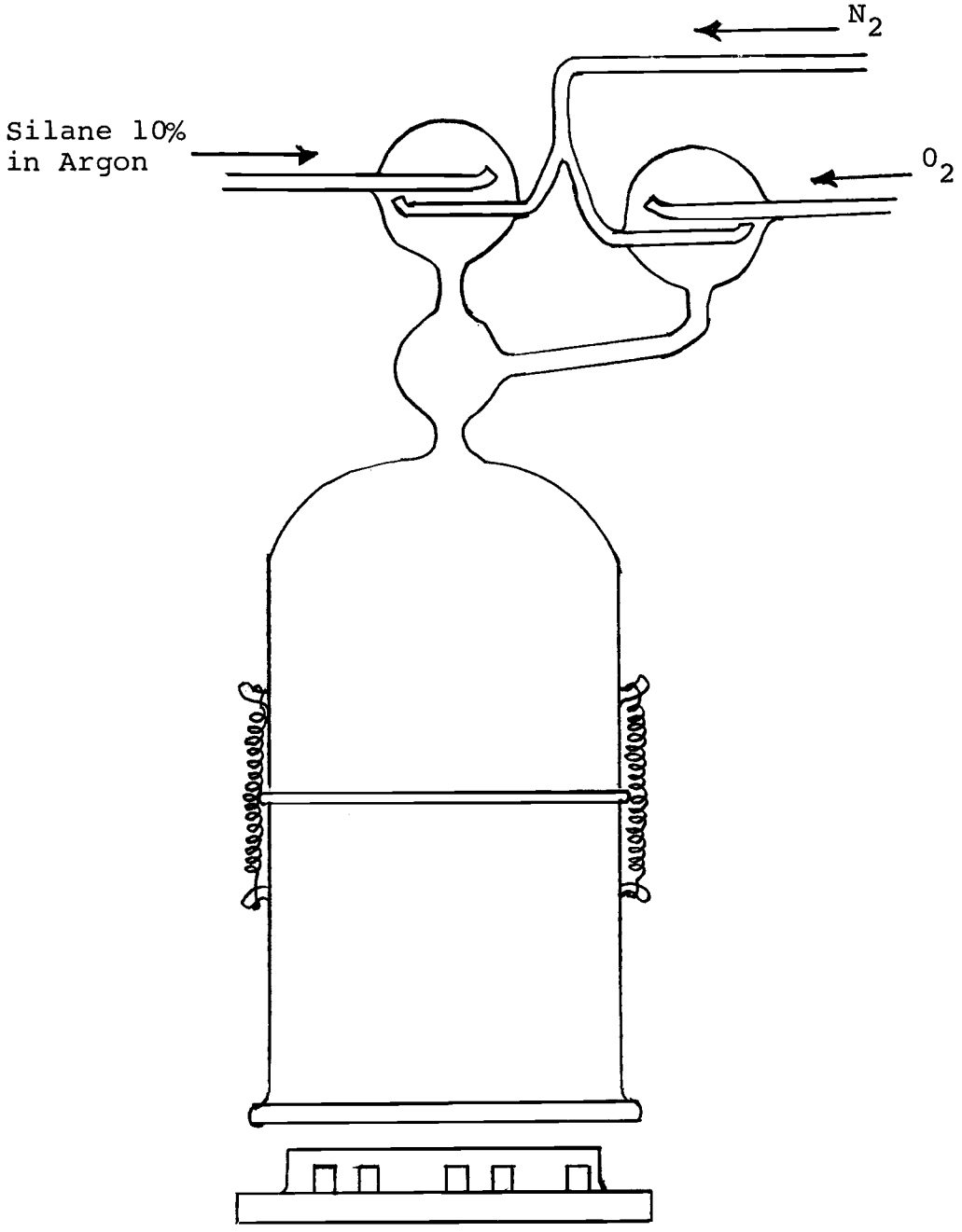



Figure 14. The pyrolytic chamber and the base.

(The base works to support the wafer and to control exhaust of the gases.)

at atmospheric pressure and a wafer temperature of 450°C.

The deposition time for obtaining 5000 Å of $SiO_2$ film was 6.66 minutes. The color of $SiO_2$ is checked by the thickness of the oxide.

TABLE II. THE DEPOSITION OF PYROLYTIC $SiO_2$ FILM.

| Film | Wafer Temperature (°C) | Growth Time (min.) | Thickness Å |
|---|---|---|---|
| A | 450 | 1.25 | 1250 |
| B | 450 | 4.00 | 3100 |
| C | 450 | 6.66 | 5000 |

Electronic Gun Evaporation Process

The silicon oxide was deposited by E-gun evaporation on the aluminum control gate and thermal oxide layer. The equipment for this process was a Varian Vacuum System and control unit. The material for $SiO_2$ deposition was high-purity quartz (diffusion grade). The quartz was washed by trichorethylene to remove grease contamination and then rinsed in acetone.

When the pressure dropped to $10^{-6}$ torr, the main power supply and water for cooling the E-gun were turned on. Then the E-gun was turned on and the emission control adjusted to the proper current. When the $SiO_2$ film, by monitor frequency change, reached a thickness of 5000 Å, the E-gun and main power were turned off. During the

deposition the substrate was also heated and held at 350°C to assure good contact.

Measurement of Thickness of Film Oxide

For obtaining the thickness of $SiO_2$, the technique of monitor frequency change was used. The film thickness refers to the curve of frequency change and film thickness of silicon dioxide that were investigated by D. R. Delzer (4). The curve is shown in Figure 15.

After deposition of the second oxide layer by either the pyrolytic process or the E-gun evaporation process, the wafers were ready for open contact. Then the standard photographic process was applied by the use of contact mask. Etching of the pyrolytic $SiO_2$ or E-gun evaporation of $SiO_2$ was a very critical and complicated process. Many serious problems were encountered, such as:

a. Photo resist contact problems
b. Etching rate problems and undercutting
c. The interface of thermal oxide and oxide grown by the pyrolytic process or E-gun evaporation process
d. Cracking oxide and pinhole problems
e. Aluminum control gate $G_1$ damage before etching through the source-drain areas

These problems will be discussed under Experimental Results.

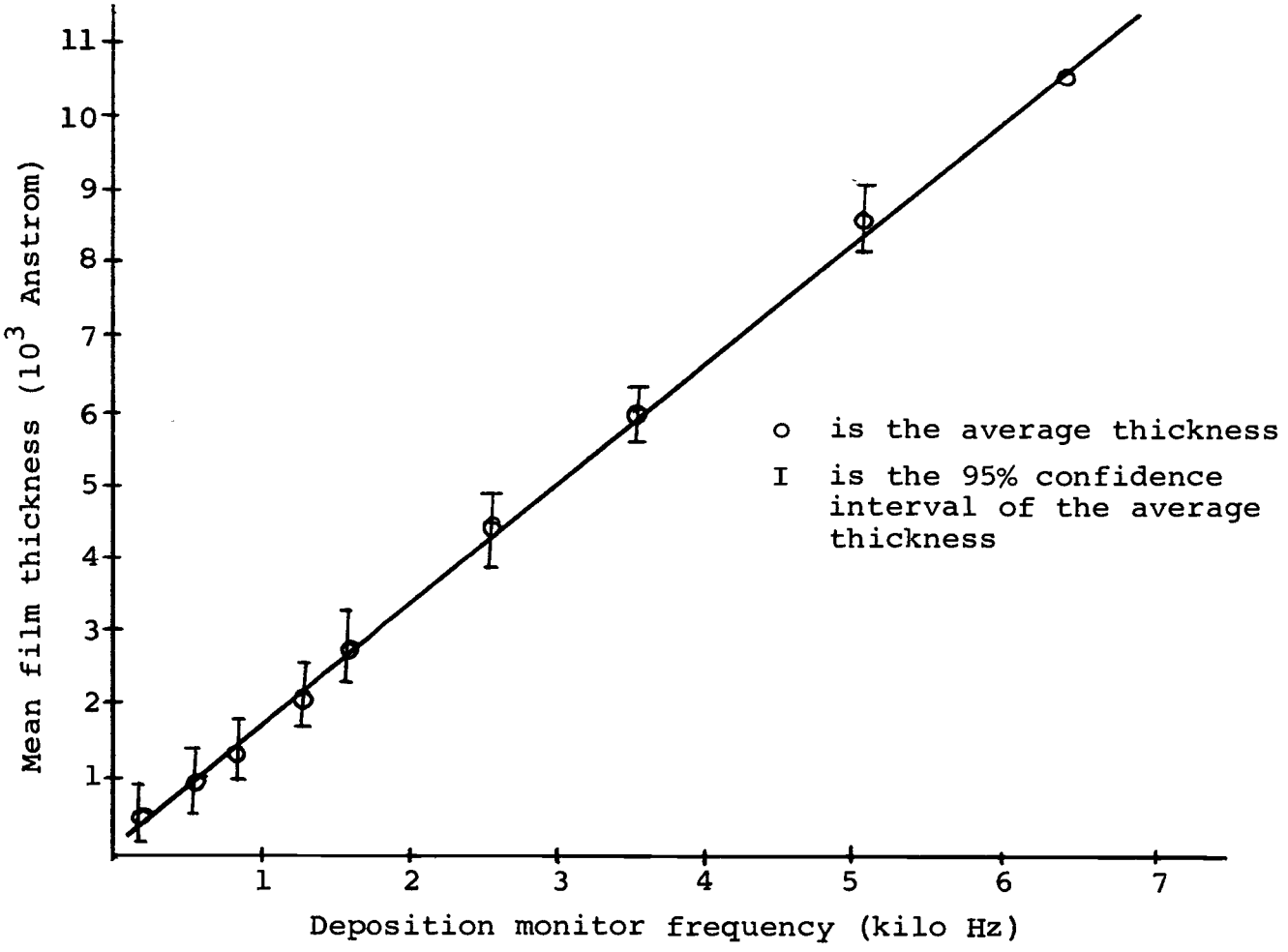



Figure 15. The curve of frequency change and $SiO_2$ film thickness of E-gun evaporation.

After opening contacts, the wafer was rinsed with acetone and rubbed with cotton swabs and placed in the ultrasonic tank. Then it was rinsed with DI water and blown dry with nitrogen. It was baked for three minutes at 550°C. At this point the wafer was ready for evaporation of the metal contact and the second gate $G_2$. Aluminum was evaporated to 5000 Å in the small vacuum pump system, as in the previous process. The wafer was alloyed in the alloying furnace at 530°C with 2.0 cfh of $N_2$ flow, and annealed for 30 minutes at 400°C in $N_2$.

The photo masking for metal contact and the second gate $G_2$ was the same as the previous photo masking process. Then the aluminum was etched and cleaned for the final process. The back of the wafer was stained with copper stain to insure good ohmic contact to the substrate, and was then ready for testing. Details of fabrication are also in the Appendix.

# EXPERIMENTAL RESULTS

After the fabrication process and preparation for testing, the wafer for the MOS tetrode transistors was stained underneath with copper stain to insure good contact to the substrate. The devices were placed on the testing equipment.

Test equipment used included the micro-manipulator probe, the Fairchild Family Characteristic Curve Tracer, and the high voltage power supply capable of varying from zero to 300 volts.

The $V_D$-$I_D$ characteristics of the MOS tetrode transistor without voltage supply at the offset gate $G_2$ are shown in Figure 16.

From the family curve of the MOS tetrode transistor no voltage applies on the offset gate $G_2$ ($V_{G2} = 0$). At $V_{G1} = 11$ volts, $V_D = 6$ volts, and the drain transconductance $Y_{fs} = 65$ micro mho. At $V_{G1} = 10$ volts, $V_D = 10$ volts and the drain transconductance $Y_{fs} = 50$ micro mho, the threshold voltage was nine volts. Breakdown voltage without modulation of the offset gate $G_2$ was 70 volts. After applying a negative voltage to the offset gate $G_2$, varying from zero to 300 volts, the characteristic curve did not change as the voltage was increased until insulator breakdown.

Unfortunately, the device did not function as fully

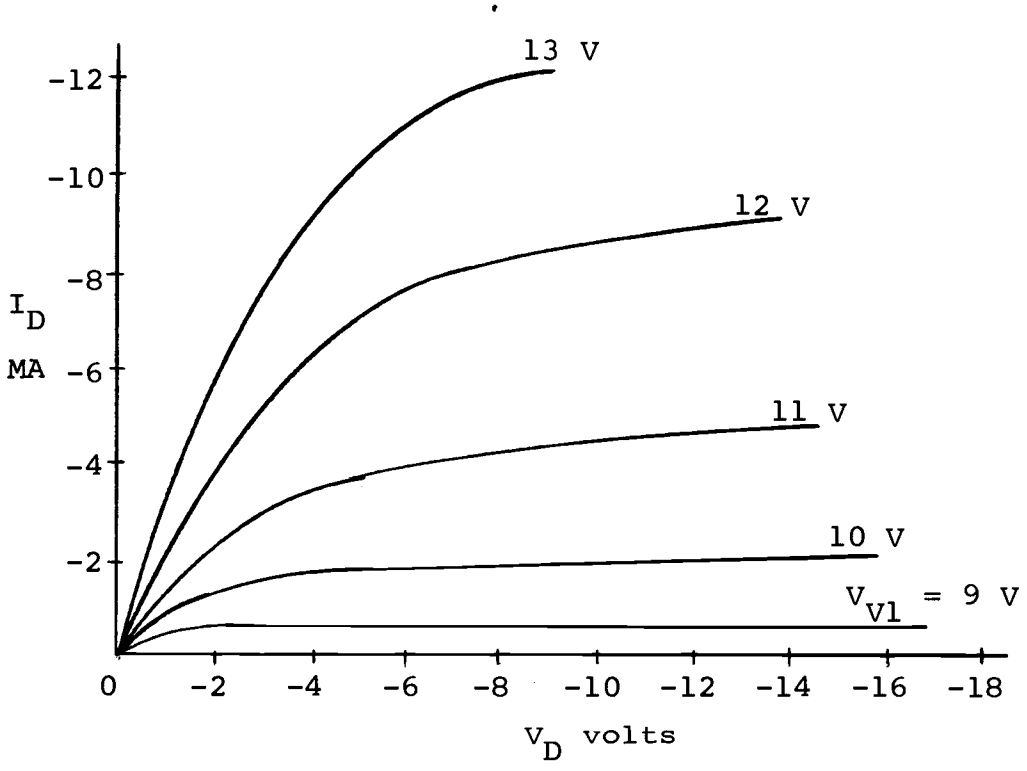



Figure 16. The $V_D$-$I_D$ characteristics of the MOS tetrode transistor without voltage supply at offset gate $G_2$.

as desired because of a defect in offset gate $G_2$. Gate $G_2$ performed the most important function of the MOS tetrode transistor. It was utilized to induce an inversion channel in the offset region between control gate $G_1$ and the drain. The $V_D$-$I_D$ characteristic for any given application can be adjusted by the potential of offset gate $G_2$. The Miller feedback capacitance, the drain breakdown potential, and the frequency response also depended on the bias of offset gate $G_2$. Because offset gate $G_2$ was defective, it prevented experimental verification.

The major problem of the defect of offset gate $G_2$ concerned the interface of the second layer of $SiO_2$. A limited understanding of the properties did not allow good control of the silicon dioxide obtained by pyrolytic deposition and E-gun evaporation. There was not enough technology nor were facilities available in the laboratory. Results of the experiments with the second layer of oxide were poor adherence and low density of film at a low temperature.

Some processing problems were found during the fabrication of the MOS tetrode transistor. The etching pyrolytic $SiO_2$ and E-gun evaporation $SiO_2$ were very critical and complicated processes in the step of open contact etching. The photo resist contact to the surface oxide was not as good as the photo resist to the thermal oxide because the oxide was very soft and easily undercut during

the etching period. Sometimes the photo resist cracked down before the oxide could be etched through the source and drain. Another problem was that the aluminum control gate $G_1$ could not stand the buffered HF before the oxide could be etched through source and drain. It was found that for several devices the gate contact $G_1$ was etched out after the finish of source-drain open contact. Thus, the processing problems and properties of the pyrolytic oxide and E-gun evaporation oxide caused the device to be impractical and not fully useful for production.

For the successful fabrication of the MOS tetrode transistor, the process must be improved through the control of the properties of insulated gate $SiO_2$ of the second layer.

# SUMMARY AND CONCLUSIONS

The structure of the MOS tetrode transistor differs from that of the MOSFET in the addition of the offset gate $G_2$. The first oxide layer for control of gate $G_1$ was grown by the wet thermal oxide process. The thickness of the layer was 1500 Å. The second layer of $SiO_2$ was grown by the pyrolytic process or the E-gun evaporation process. Typical oxide thickness was 5000 Å with the low temperature method. The possible applications of the MOS tetrode transistor are suggested by the low Miller feedback capacitance and the high drain breakdown potential. $V_D - I_D$ characteristics can be adjusted by offset gate $G_2$ for a given application.

The new technique of fabrication of the MOS tetrode transistor is similar to that of the regular MOSFET except for offset gate $G_2$ and the second layer of silicon dioxide. Growing the second oxide layer was a very complicated process. The high temperature process could not be used as it would have caused damage to control gate $G_1$. Two processes were used in this project: the pyrolytic process, and the E-gun evaporation process. The pyrolytic $SiO_2$ is the chemical process, by which the $SiO_2$ film was deposited by the mixture of Silane ($SiH_4$) in argon, oxygen and nitrogen. The typical rate of deposition was 750 Å per minute. The result of the oxide film was still low

adherence and density. Oxide thickness was not quite uniform, probably because of the flow rate of the mixture or the physical appearance of the chamber and the rate of exhaust around the base of the chamber. The quality of $SiO_2$ grown by the pyrolytic process is very soft. Etching of $SiO_2$ by buffered HF is very difficult because the oxide is easily undercut and cracks open. The second problem is that the aluminum of control gate $G_1$ becomes damaged before being etched through the source and drain. Investigation of the two interface layers of $SiO_2$ shows that the undercut of the interface areas always cracks open during the etching period.

E-gun evaporation of $SiO_2$ was also involved in this project. The thickness of the oxide layer was measured by the frequency change of the monitor. The oxide film of E-gun evaporation which was observed through the microscope showed the pinhole density to be somewhat higher than that obtained by the pyrolytic process. The adhesion between two layers still cracked occasionally during etching.

The MOS tetrode transistor was tested after having gone through the fabrication process. The testing results showed that the device was not functioning fully because of the defect of offset gate $G_2$, and this defect prevented experimental verification.

The discussion of this paper is based on the experimental fabrication of the MOS tetrode transistor with

p-channel, and the problems which were encountered. The major problem is that of the offset gate $G_2$ insulator. Further work is needed to find a better method of fabrication and a higher quality of offset gate insulator.

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# APPENDIX

## The MOS Tetrode Transistor Process in Simplest Configuration

1. Water cleaning before oxidation (n-type silicon 10 ohm-cm.)
2. Initial oxidation approx. 8500 Å
3. Photo masking for source-drain window and evaluation window
4. Source-drain window etching
5. Cleaning process before source-drain diffusion
6. Source-drain diffusion evaluation of the result (coat wafer with borofilm using spinner put in boro-diffusion furnace for 15 minutes in air)
7. Cleaning before second photo masking-gate oxide control
8. Photo masking for gate oxide control
9. Gate oxide etching and cleaning process
10. Gate oxide regrow with phosphorus stabilization (wet oxidation 5½ min approx 1500 Å)
11. Cleaning before evaporation of metal (gate 1)
12. Evaporation of metal gate 1
13. Alloying
14. Photo masking for metal gate 1 etching
15. Metal $G_1$ etching and post cleaning process
16. Grow $SiO_2$ by chemical process (pyrolytic)
17. Cleaning before open contact masking
18. Open contact etching

19. Clean after open contact
20. Evaporation of metal (contact and gate 2)
21. Alloying
22. Photo masking for metal and gate 2 etching
23. Metal and gate 2 etching and post cleaning process
24. Prepare for electrical test and storage

## MOS Tetrode Transistor Fabrication in Detail

The MOS tetrode transistor fabrication is divided into five photo masking steps. Fabrication is more complicated than for an MOS transistor, because oxide must be grown over the control gate to form the second gate. The following are steps in producing the MOS tetrode transistor.

### Step #1. For Photo Masking of Source-Drain Window

This step concerns initial cleaning of wafer, oxidation, source-drain window etching and diffusion. The following procedures provide a clean surface for initial oxidation.

#### Initial Cleaning of Wafer

a. Rinse wafer with TCE, follow by acetone, then running DI water, blow dry with nitrogen.

b. Etch in buffered HF solution for 30 seconds to remove any oxide film.

c. Boil in DI water for at least ten minutes to remove HF.

d. Clean with DI water in ultrasonic tank, setting 3

e. Rinse in running DI water

f. Blow dry with nitrogen and bake at 150°C for five minutes.

Initial Oxidation (Wet oxygen process was used)

a. Purge furnace, #7, set water temperature control at 95°C

b. Turn off steam before inserting water into the furnace. Cold water may collect moisture on its surface, causing uneven oxidation if steam is left on. Turn on steam after the slice is at the center zone position, and start to count time of wet oxidation.

c. Net oxidation scheme

(1) Wet oxygen - two hours, $O_2$ - 0.4 cfh, water 95°C

(2) Nitrogen - 30 min $N_2$ - 1.0 cfh

(3) Furnace temperature both at 1100°C

(4) Resulting oxide 8500 Å approx. (indicated by color of the oxide)

Photo Masking of Source and Drain Procedure

a. Apply photo resist AZ-1350 and spin with spinner; set speed control 70, time 15 seconds

b. Bake slice in vacuum oven for ten minutes after coating at 60°C

c. Expose the slice with source-drain window mask, time four seconds

d. Develop in AZ-1350 developer for 30 seconds,

rinse with DI water, and blow dry with nitrogen

e. Inspect under microscope for completeness of developing

f. Bake slice at 150°C for ten minutes

Source-Drain Window Etching. A critical step, as initial channel width depends greatly on this etching. Over-etching causes undercutting which may narrow down the channel to an undesirable degree.

a. Oxide thickness may be checked at the back of slide by etching and ring counting method

b. Etching time of 8500 Å wet oxide is seven minutes (completeness of etching indicated by stop wet at back of wafer and indicated by microscope on surface of source-drain area)

c. Rinse slice in running DI water immediately after etching is complete

d. Remove photo resist by acetone and rub with cotton swab and acetone, cleaning in ultrasonic tank three minutes. Rinse with DI water and blow dry with nitrogen

e. Inspect under microscope for good result

Cleaning the Source-Drain Before Deposition

a. Boil the slice ten minutes in DI water

b. Ultrasonic clean in DI water - setting at 3

c. Rinse in DI water and blow dry with nitrogen

d. Bake dry at 150°C for five minutes

Source-Drain Deposition and Evaluation of Results

a. Coat water with 2:1 borofilm, using spinner; spinner speed setting at 7, time ½ second, and bake on hot plate for three minutes

b. Boron deposition (on N-type wafer) is 15 minutes at 1100°C (boron diffusion furnace) in air

c. Sheet resistance 20 ohms/square

d. Boil wafer in DI water for 30 minutes or more after deposition so as to remove possible boron film

e. Etch slice in buffered HF solution for ½ minute to remove boron film grown during deposition

f. Rinse in DI water and dry with nitrogen

Step #2. Photo Masking for Gate Oxide Control

Cleaning Before Gate Mask Etching

a. Clean the slice in ultrasonic tank with DI water, setting 3

b. Rinse in DI water and dry with nitrogen

c. Bake at 150°C for at least three minutes

d. Clean surface by inserting slice into oxidation furnace and pulling out immediately. It is best to purge the furnace with nitrogen before using.

Photo Masking for Gate Oxide Etching

a. Apply photo resist

b. Use standard photo resist process

Gate Oxide Etching and Post Cleaning Process

a. Gate oxide etching time should be equal to source-drain window etching time plus 30 seconds

b. Rinse slice immediately in DI water after the etching process is completed; dry with nitrogen and inspect the results. The sheet resistance with four-point probe equals 20 ohms/square

c. Rinse slice with acetone and rub with cotton swab, followed by acetone cleaning in ultrasonic tank, setting 3, then rinse in DI water. Inspect under microscope for complete removal of photo resist

d. Boil in 50% nitric acid for 30 minutes. Rinse in DI water

e. Ultrasonic cleaning with DI water, setting 6. Repeat with fresh DI water

f. Rinse in running DI water, dry with nitrogen

g. Bake at 150°C for three minutes

Gate Oxide Regrown with Phosphorous Compensation

a. Use wet oxygen and purge oxidation furnace as described before

b. Wet oxidation time 5½ minutes at 1100°C, water temperature 95°C. Oxygen flow 0.4 cfh. Resulting oxide approximately 1500 Å, color light blue

c. Remove slice from furnace and transfer to phosphorous deposition furnace

d. Follow standard deposition procedure; give the slice ten minutes phosphorous deposition on the gate oxide

e. Move slice back to oxidation furnace at the end of deposition for 6½ minutes nitrogen treatment

f. Remove slice from the furnace for cleaning process

Step #3. Photo Masking for Metal Gate No. 1 Etching

Cleaning Process Before Evaporation

a. Boil slice in DI water for 15 minutes

b. Rinse with DI water, blow dry with nitrogen

c. Bake at least three minutes at 150°C on hot plate

Evaporation of Metal Gate No. 1

a. Follow general instruction (OSU Lab)

b. Heat substrate after the vacuum is down to marked region

c. Use shield to cover slice during filament wetting process. To insure good ohmic contact, test by Scotch tape

Alloying

a. Purge the alloying furnace for at least ten minutes before use

b. Alloy at 530°C with 2.0 cfh nitrogen flow rate for five minutes

c. Anneal at 400°C for 30 minutes in nitrogen

d. Apply photo resist immediately after annealing

Photo Masking for Metal Gate No. 1 Etching

a. Follow general instruction as before

b. Baking time after developing three minutes

Metal Etching and Cleaning Process

a. Follow general instruction

b. For thick aluminum films use fast etching by raising temperature of etching solution to 5o°C

c. Check result of etching by microscope

d. Remove photo resist by repeating acetone and DI water rinse

e. Blow dry with nitrogen and bake at 150°C for five minutes

Grow $SiO_2$ by chemical process (pyrolytic) (see detail on page 32)

E-gun evaporation process (see detail on page 34)

Step #4. Open Contact Etching

Cleaning Before Open Contact Masking

a. Boil slice in DI water for 15 minutes

b. Rinse with DI water; blow dry with nitrogen

c. Bake for at least three minutes at 150°C on hot plate

d. Heat the surface by inserting slice into oxidation furnace and pulling out quickly. It is best to purge furnace with nitrogen before doing so.

e. Photo masking procedure follows standard step (same as before)

Open Contact Etching

a. Etching time is variable

b. Inspect etching result before and after removal of masking photo resist

c. Check sheet resistance

Cleaning Process After Open Contact

a. Repeat rinsing with acetone and rubbinb with cotton swabs to remove photo resist

b. Clean with DI water in ultrasonic tank, setting 6

c. Rinse with DI water; dry with nitrogen

d. Bake at 150°C for two to three minutes

Evaporation of Metal Contact and Gate No. 2

a. Follow general instruction

b. Heat substrate after vacuum is down, marked region

c. Use shield to cover slice during "filament wetting process" to insure good ohmic contact

Alloying

a. Purge alloying furnace for at least ten minutes before use

b. Alloy at 530°C with 2.0 cfh nitrogen flow rate for five minutes

c. Anneal at 400°C for 30 minutes in $N_2$

d. Apply photo resist immediately after annealing

Step #5. Photo Masking for Metal Contact and Gate No. 2

a. Follow general instruction

b. Bake after developing for three minutes

Metal Etching and Post Cleaning Process

a. Follow general instructions

b. For thick aluminum film use fast etching by raising temperature of etching solution to 50°C

c. Inspect the result by microscope

d. Remove photo resist by repeating acetone and DI water rinse

e. Blow dry with nitrogen and bake at 150°C for five minutes

Prepare for Testing

a. Stain back of the wafer with copper stain to insure good ohmic contact to the substrate

b. Rinse with DI water after stain; dry with nitrogen. Bake at 150°C for five minutes

c. Slice is ready for testing.