AN ABSTRACT OF THE THESIS OF

Ean A. Amon for the degree of Master of Science in Electrical and Computer Engineering
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Title: Hybrid Electric Vehicle Active Rectifier Performance Analysis

Abstract approved: _____

Annette von Jouanne

In advanced hybrid electric vehicle development, performance and dependability are essential considerations in the design process. High efficiency is crucial in a successful design and fault tolerance is necessary to provide limp-home capability under faulted operating conditions. The reduction of electromagnetic interference is mandatory to reduce interference in communications and control systems, especially in military applications. This thesis is a performance analysis of several generator and active rectifier configurations for use in military hybrid electric vehicle applications. Simulation results are obtained using Matlab Simulink with experimental hardware testing for verification.

Fault tolerance is explored in generator design through the use of multi-phase generator configurations in both wye-connected and independent phase configurations. Passive rectifier investigations are included as a baseline for active rectifier performance comparison. Simple voltage-controlled active rectifier results are obtained with initial three- and six-phase generator configurations. Current-controlled rectifier models are then simulated with more advanced generator designs. In all simulations, performance is evaluated through harmonic analysis of rectifier input currents and output dc bus voltage, as well as input power factor measurements.

Scaled hardware testing is performed for verification of simulation results. Multiple generator configurations are represented through utilization of a three-phase, fully programmable source with various transformer configurations at the output to achieve six-phase capability. Several active rectifier configurations are obtained through the use of configurable Powerex H-Bridge IGBT assemblies with control provided using an Opal-RT hardware-in-loop rapid prototyping system.

# Hybrid Electric Vehicle Active Rectifier Performance Analysis

by

Ean A. Amon

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Master of Science

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APPROVED:

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Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

_____

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

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Ean A. Amon, Author

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# 1. INTRODUCTION

## 1.1 Background

Fault tolerance and efficiency are paramount in the design of hybrid electric vehicle systems. In the case of military applications, the reduction of electromagnetic interference (EMI) is mandatory to reduce interference in communications and control systems, as well as eliminate "detectable signals" caused by harmonic frequencies. Fault tolerance of generator systems is enhanced through the use of multiphase generator topologies and controlled active rectifier configurations. Active rectifier configurations promote higher efficiencies, particularly in high frequency applications, due to their power factor correction capabilities. The purpose of this thesis is to conduct a performance analysis through simulation with Matlab Simulink of several active and passive rectifier topologies using different generator configurations and control techniques. Hardware testing at a scaled level is also performed for verification of simulation models.

## 1.2 Fault Tolerance of Permanent Magnet Machine Systems

The issues of rapid fault detection, identification, and possible remedial strategies leading to continued operation (albeit with reduced performance) of permanent magnet machine systems have been addressed and documented by several authors [1]-[9] in the past decade or more. Some of the proposed strategies have been relatively simple adaptations of conventional topologies whereas other approaches have been very radical, including multiphase systems. The requirement for rapid detection and response is urgent in order for a single fault not to progress through the system and cause an irrecoverable situation.

At the on-set of a fault, the problems are generally readily observable but may be difficult to overcome due to the need to differentiate the specific problem from a range of possible causes. Also, the very nature of the faults in PM machines and their controller have more severe implications due to the effects of the uncontrolled (and uncontrollable) field: large currents in short circuits and high voltages in open circuits.

The researchers in this field have covered a wide range of potential solutions, in order to obtain limp home capability at less than rated power levels, all of which require some modification to the basic system topology. At the most basic level, pure control of

conventionally configured systems has been investigated, with a reconfigured final system [6], [7]. More commonly, basic modifications are proposed that involve additional connections to the machine windings (e.g. a wye-connection brought out) and an additional switch or switches in the controller [1], [2], [4], [8], [9]. Radical approaches involve independent inverters (multiphase, H-bridge) for each phase [5], [10] and complete redesign of the machine itself to provide isolation of both electrical and magnetic circuits [3], [11]. This latter approach has been pursued by its advocates for several years and initially results from the inherent capability of some configurations of switched reluctance motors to achieve a good degree of fault tolerance in proposed military applications. In general, multiphase systems provide a better degree of fault tolerance, depending on operation.

### 1.3 PWM/Active Rectifier Systems

Pulse-width-modulated (PWM) ac-dc rectifiers, or active front end (AFE) rectifiers, are becoming a highly developed technology with wide industrial acceptance due to improved input and output performance [17]. The main disadvantage of the more simple line-commutated passive rectifiers using diodes is the generation of harmonics and reactive power [18], [19]. Methods to reduce input current harmonics include multi-phase configurations based on transformers and multiple windings (designing appropriate phase shifts among the secondary windings of the input transformer, the harmonics generated by one diode rectifier can be cancelled by the harmonics produced by other rectifiers) [20], passive power filters [21], and active filters [22]-[24]. In addition, several power factor correction (PFC) topologies, e.g. in [25] and [26], have been proposed to reduce harmonics and improve power factor by including power switches such as insulated gate bipolar transistors (IGBTs) in the power circuit of the rectifier to actively change the input waveform and reduce distortion [17]. Many of these approaches are suited for applications where power is transmitted only from the ac source to the dc-bus [17]. However, there are several applications, such as hybrid electric vehicles, where regeneration of energy flow from the dc-bus to the power supply side is desired through the use of a PWM Rectifier.

### 1.4 Three-Phase PWM/Active Rectifiers

PWM/Active rectifiers can offer the advantages of reduced ac side and dc-bus harmonics, improved ride-through capability, and improved fault tolerance. Fault tolerance benefits include the ability to operate as a diode rectifier under no gating signals, and operation with an "open" load [17]. Disadvantages include a more complex and expensive topology and control loop, the presence of switching EMI and higher dc-bus voltage operation. It is well known that voltage source inverters (VSIs) can operate as rectifiers by reversing the power flow from the load to the dc-bus, i.e. operating as a PWM voltage source rectifier (VSR) [17]. These PWM rectifiers (Fig. 1) maintain the dc-bus voltage at a desired reference value using a feedback control loop. This reference value, $V_{o,ref}$ must be high enough to keep the diodes of the converter in Fig. 1 blocked. Once this condition is satisfied, the dc-bus voltage is measured and compared with the reference $V_{o,ref}$. The error signal generated from this comparison is used to switch on and off the switches (e.g. IGBTs) of the PWM rectifier. Thus, the direction of power flow is determined by the dc-bus voltage value. There are several methods of modulation [27], the most popular being sinusoidal PWM (SPWM), which uses a triangular carrier to generate the PWM pattern [17].

For proper operation, the PWM pattern must generate a fundamental ($v_{mod}$) with the same frequency as the power source. Changing the amplitude and phase shift of $v_{mod}$ allows the rectifier to operate in four modes: leading power factor rectifier, lagging power factor rectifier, leading power factor inverter, and lagging power factor inverter. Like VSIs, PWM rectifiers cannot operate in overmodulation mode without generating low-frequency harmonics at the input and at the output [17]. Control of the PWM rectifier is achieved in two different ways: 1) as a voltage-source current-controlled PWM rectifier or 2) as a voltage-source voltage-controlled PWM rectifier. The first method controls the input current and the second controls the magnitude and phase of the voltage [17]. The current controlled method is more stable and can be simpler than the voltage-controlled method; detailed control analysis will be performed in this work. The following references [28]-[33] present different control methods such as discrete control, fuzzy logic, one-cycle control, nonlinear control using complex state-space modeling, as well as the behavior of rectifiers during unbalanced input voltage conditions. Active Filtering functions can also be added to PWM rectifiers, as discussed in [34] – [35].

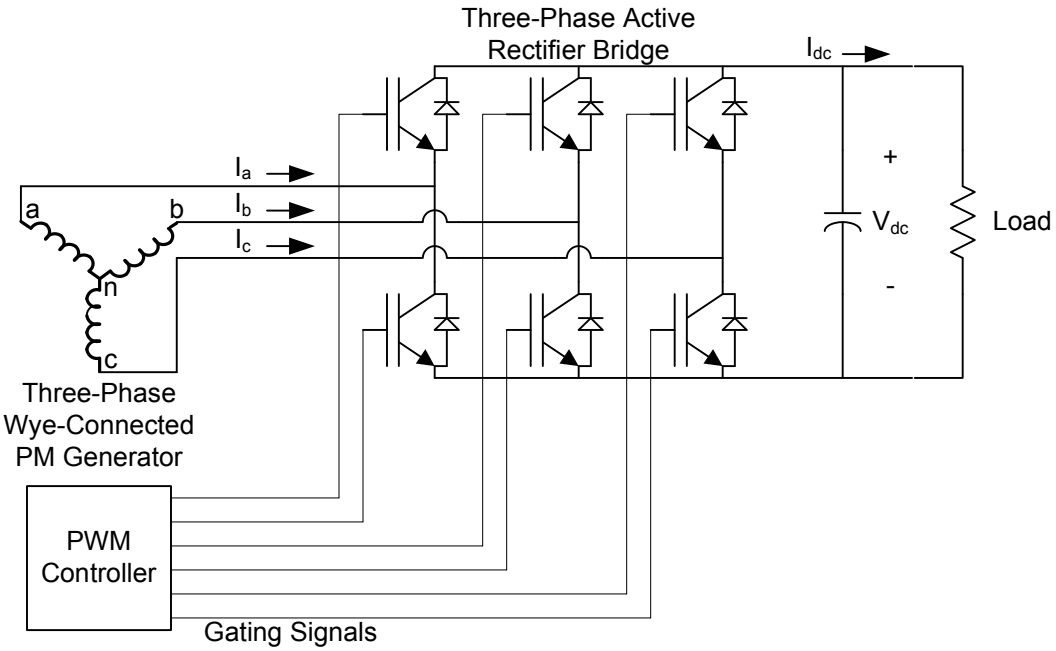


Fig. 1 – Schematic of typical three-phase PWM rectifier.

**1.5 Multi-Phase PWM/Active Rectifier Systems**

Multiple-phase (greater than three-phase) PWM rectifiers can be controlled to generate less dc-bus ripple and harmonics than three-phase PWM rectifiers in part due to the inherently increased ripple frequency, provided by the additional phases of the source, as well as the increased degree of control [36]. This decreased dc-bus ripple and harmonics results in a decreased dc-bus capacitance requirement. In addition, fault tolerance is improved due to the additional phases. The loss of a rectifier phase or phases will decrease the dc-bus regulation and power quality (increasing ripple and harmonics), however the multiphase system will outperform the three-phase system under equivalently faulted conditions. In addition, multiphase independent (H-bridge) topologies will exhibit higher fault tolerance capabilities than multiphase wye configured systems [37], and the H-bridge topology would be immune to the zero sequence produced during unbalanced/faulted operation. Multiple-phase PWM rectifier topologies investigated include the six-phase wye (Fig. 2), and six-phase independent (H-bridge) systems (Fig. 3). The power density benefits of multiphase machines are not realized in multiphase PWM rectifiers since the rectifier components effectively double between a three-phase wye (6 IGBTs) and a six-phase wye (12 IGBTs) system, with six-phase independent (H-bridge) configurations

requiring 24 IGBTs. It follows that the drawbacks of multiple-phase PWM rectifier systems include increased component counts, complexity, size/volume, weight and cost. Note that advances are also being made in "multilevel" PWM rectifier topologies as illustrated in [38].

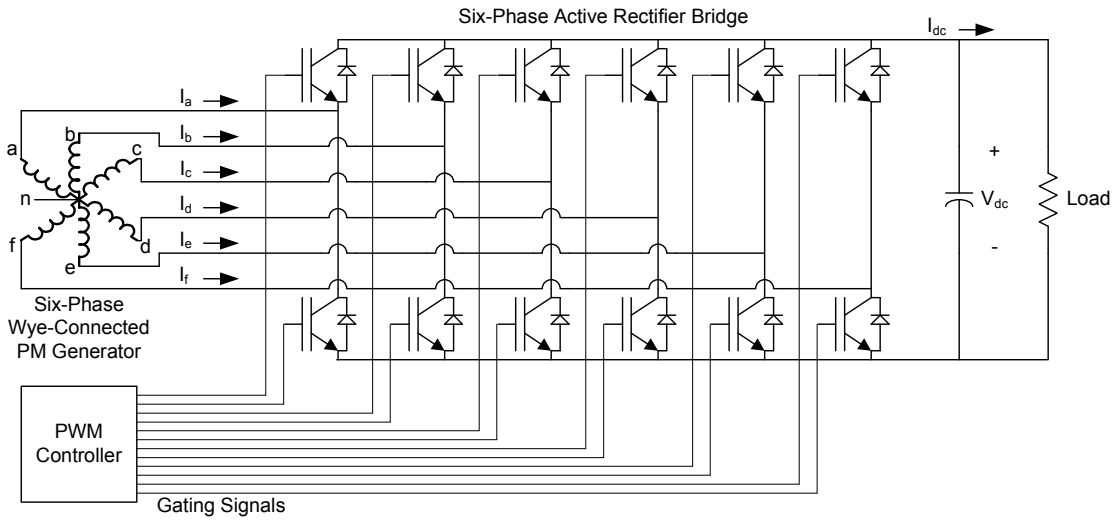


Fig. 2 – Six-phase wye-connected active rectifier bridge.

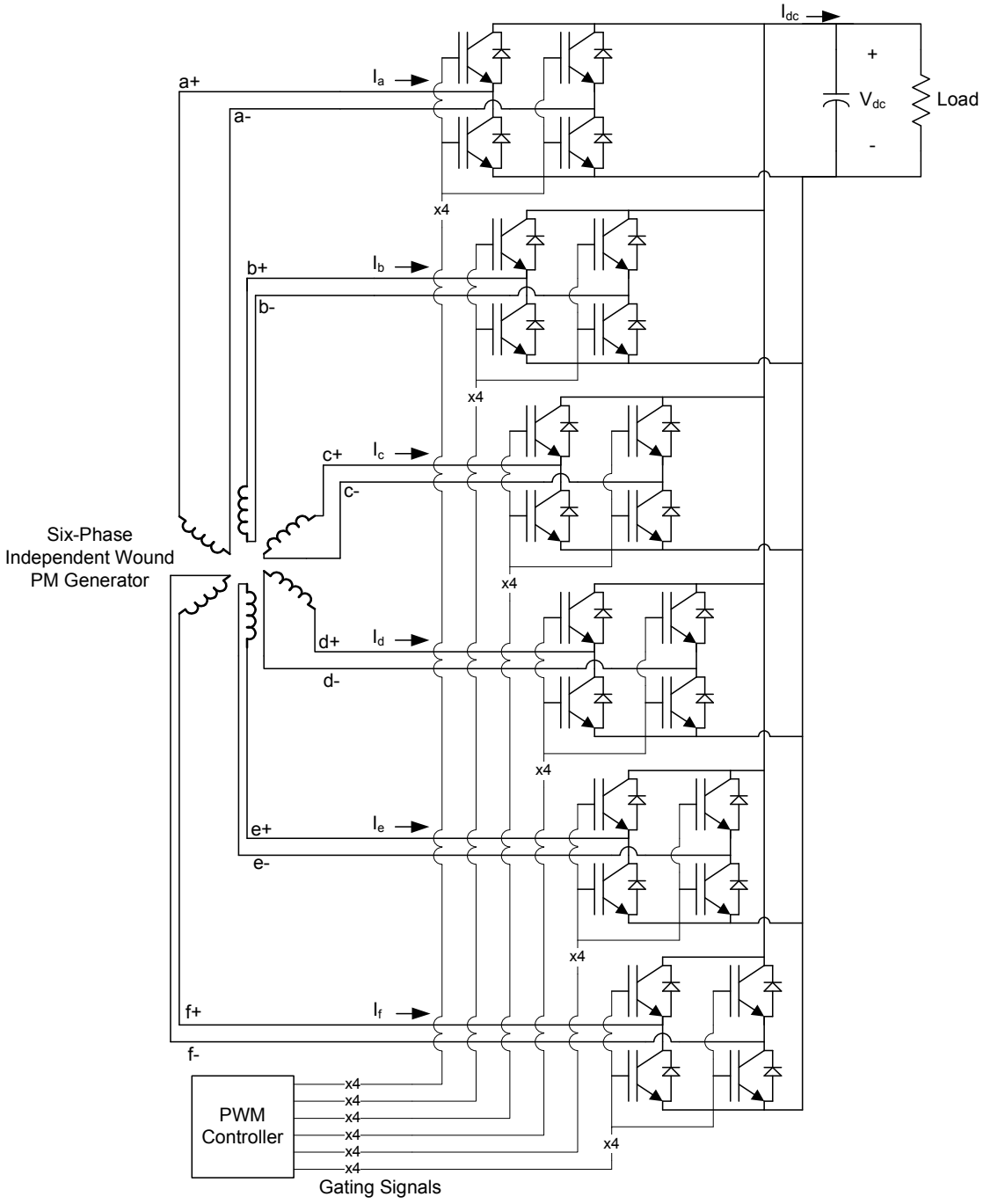


Fig. 3 – Six-phase independent active rectifier bridge.

# 2. PASSIVE RECTIFIER INVESTIGATIONS

## 2.1 Passive Rectifier Simulation

Passive rectifier results were obtained as a reference with which the active rectifier results could be compared. The dc-bus voltage level and rms current were recorded for each configuration for comparison of harmonic levels. Individual harmonic magnitudes in the dc-bus voltage were also recorded for a detailed comparison. Diodes used in construction of the passive rectifier models have an on-resistance of 1.0mΩ, a forward voltage of 2.0V, and a series RC snubber circuit with resistance of 50Ω and capacitance of 250nF connected in parallel with each diode.

## 2.2 PM Synchronous Machine with Passive Rectifier

The PM Synchronous Machine (PMSM) model in Matlab Simulink is torque-driven; desired electrical frequency was obtained through the use of a controlled torque drive with mechanical frequency feedback. The model was set up in a four-pole-pair configuration requiring a mechanical speed of 1885 radians/sec to achieve the desired electrical frequency of 1.2 kHz. Generator peak phase voltage at no-load was 368.55V (451.4$V_{LL}$ rms) to achieve a 600V dc-bus. Stator resistance and inductance were calculated for an efficiency of 98% with a 5% voltage drop under full load. This resulted in a stator resistance of 8.0mΩ and inductance of 2.7μH. With this calculated inductance value, significant voltage distortion was apparent at the generator output. For comparison between rectification schemes and generator configurations, results are included with the inductance multiplied by 0.1 to obtain a more sinusoidal generator voltage (inductance of 0.27μH). A 440kW resistive load was applied to the dc-bus with a parallel capacitance of 2400μF. The Matlab Simulink schematic for this model is shown in Fig. 4.

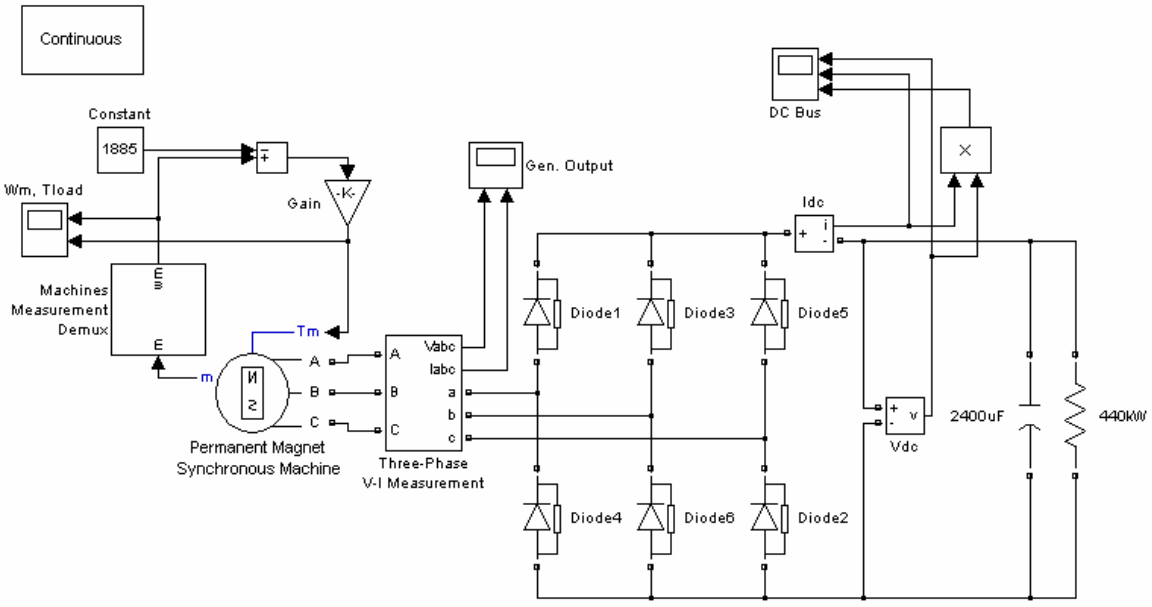


Fig. 4 – PM Synchronous Machine model with passive rectifier.

Plots of dc-bus voltage for the simulated time period and detailed ripple plots are included for both the calculated and reduced inductance values, shown in Fig. 5(a-d). Fig. 6(a-b) shows the FFT plots displaying harmonic content for each case. It is observed that reduction in the input inductance results in an increase in dc-bus voltage ripple and harmonic magnitude. The FFT data contains an expected dominant harmonic of six times the input frequency or 7.2 kHz.

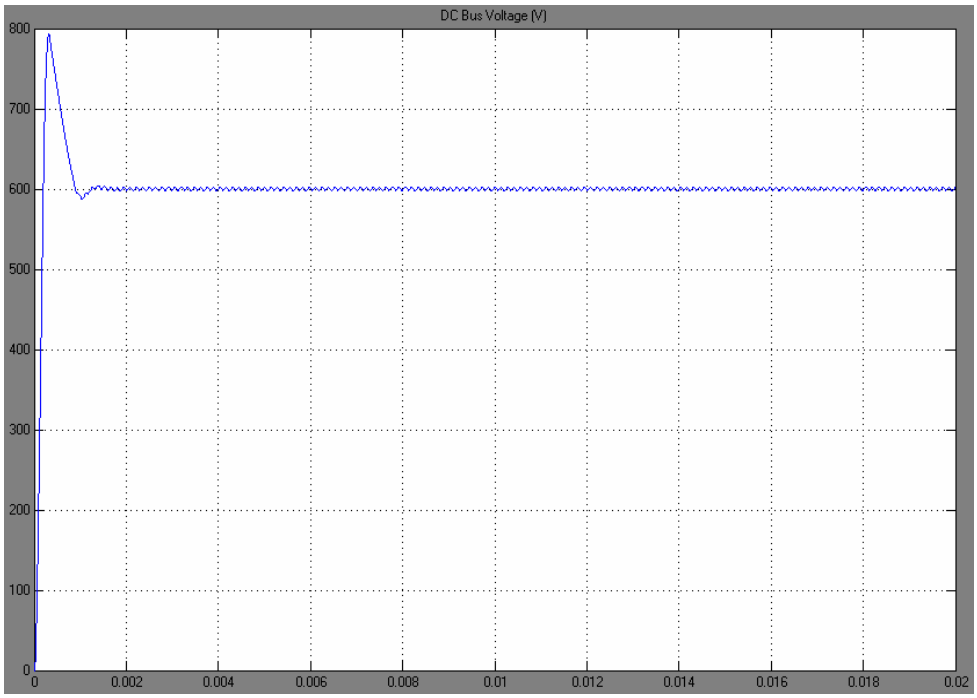


Fig. 5(a) – Dc-bus voltage for the three-phase PMSM passive rectifier model with calculated inductance.

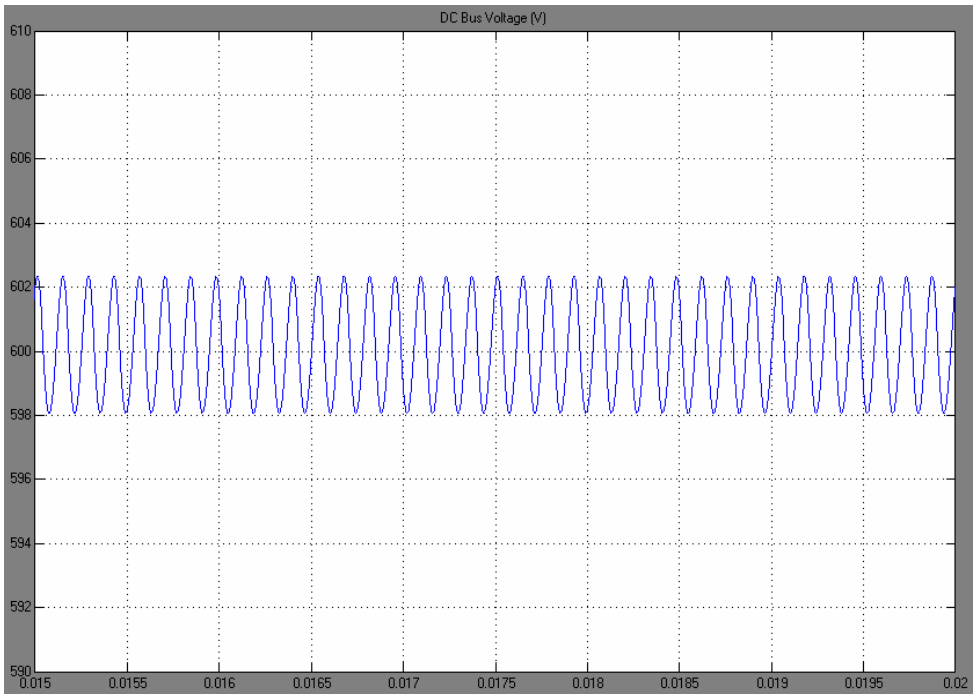


Fig. 5(b) – Dc-bus voltage ripple for the three-phase PMSM passive rectifier model with calculated inductance.

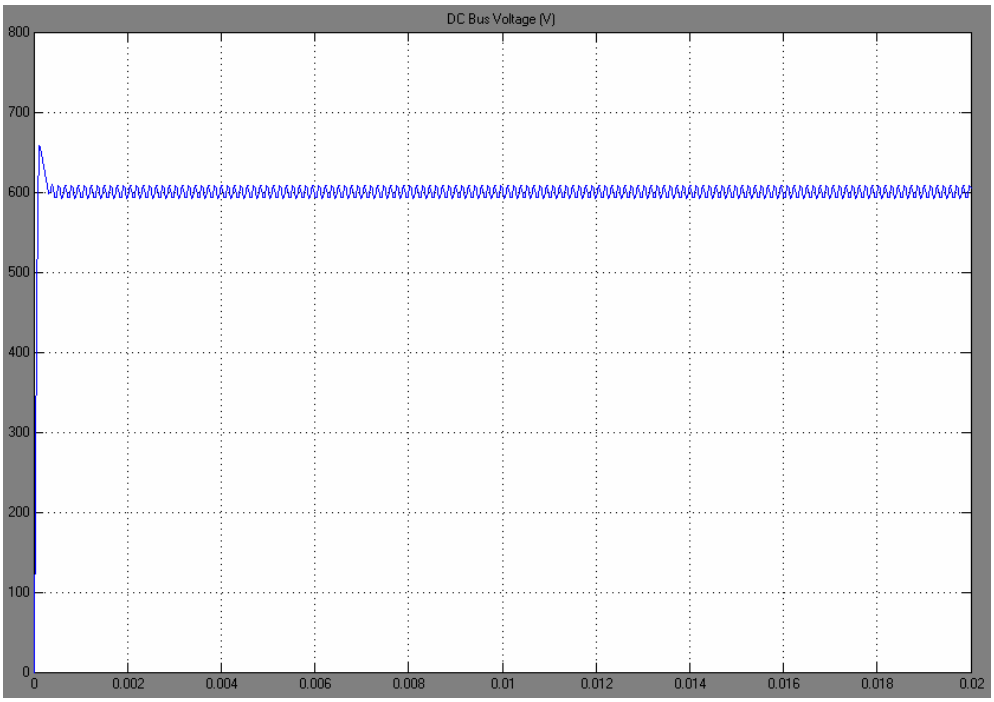


Fig. 5(c) – Dc-bus voltage for the three-phase PMSM passive rectifier model with reduced inductance.

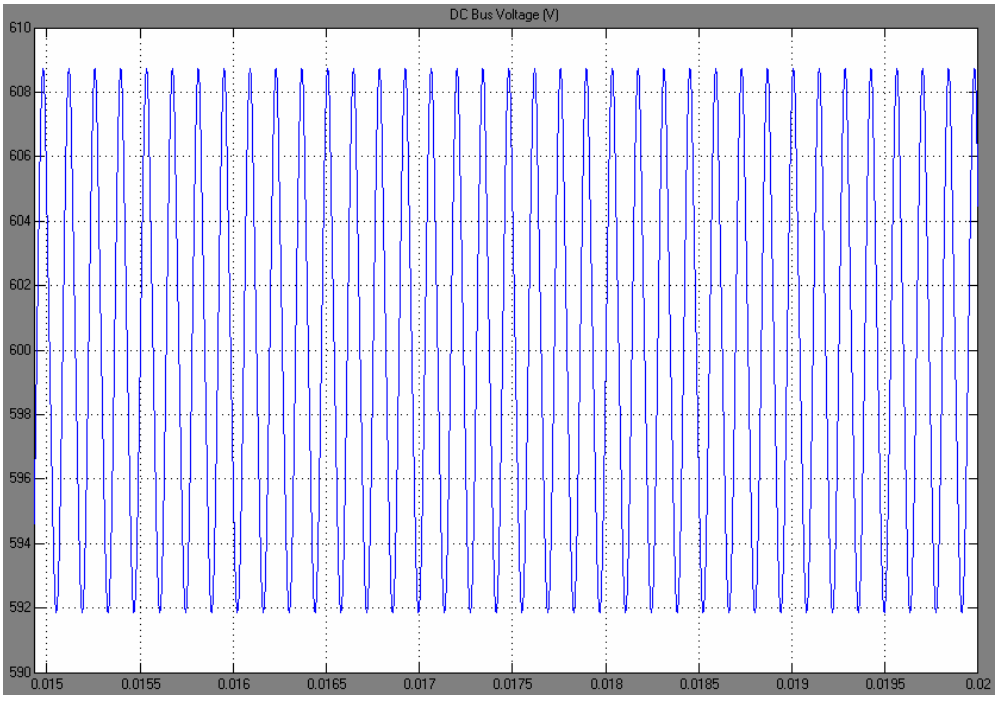


Fig. 5(d) – Dc-bus voltage ripple for the three-phase PMSM passive rectifier model with reduced inductance.

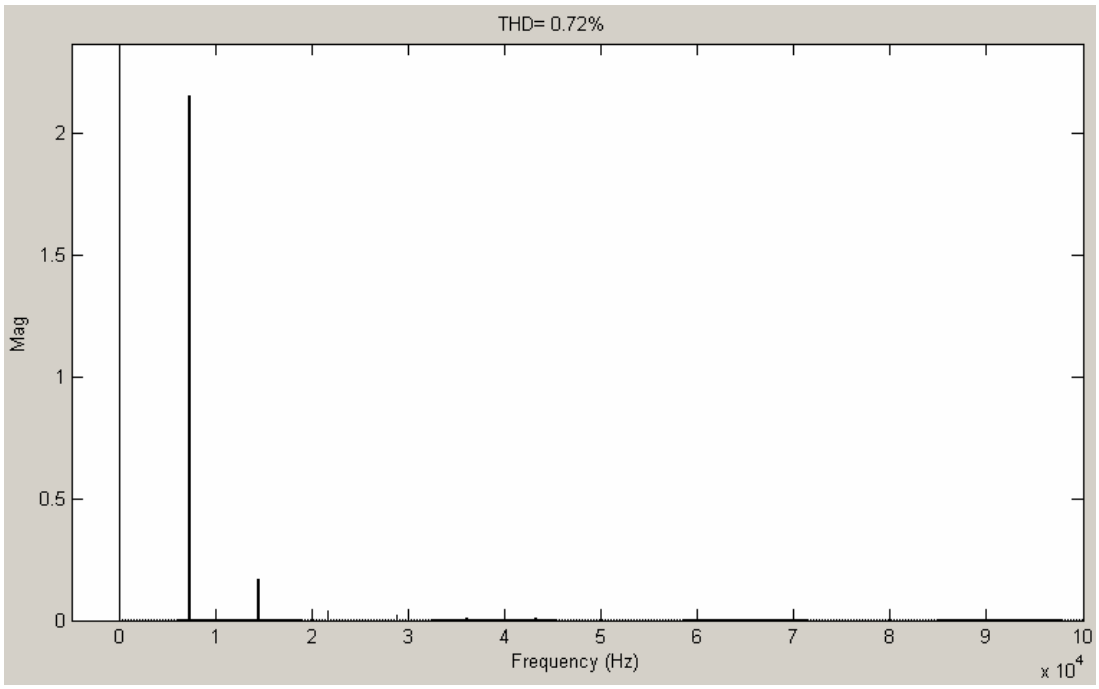


Fig. 6(a) – Dc-bus voltage FFT plot for the three-phase PMSM passive rectifier model with calculated inductance, dc fundamental is 600.12V.

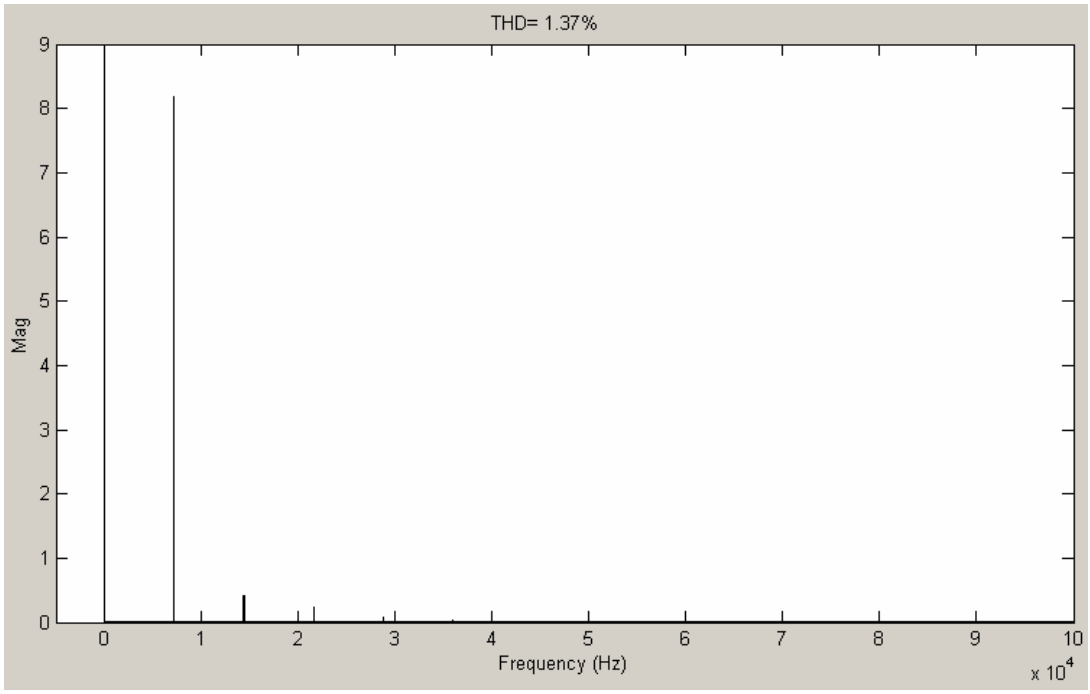


Fig. 6(b) – Dc-bus voltage FFT plot for the three-phase PMSM passive rectifier model with reduced inductance, dc fundamental is 600.02V.

**2.3 Three Wye-Connected AC Sources with Passive Rectifier**

The three-phase wye-connected generator was modeled using three wye-connected ac sources with series resistance and inductance for comparison with results obtained using the PM Synchronous Machine model. The purpose of this test was to justify the use of ac sources in modeling six-phase configurations. The ac sources, which represent the machine's back emf, were set to the peak phase voltage the PM Synchronous Generator produced under no-load, 368.55V (451.4$V_{LL}$ rms). The same series resistance and inductance values were used as in the PM Synchronous Machine model (stator resistance of 8.0mΩ and inductance of 2.7μH). The Matlab Simulink schematic for this model is shown in Fig. 7.

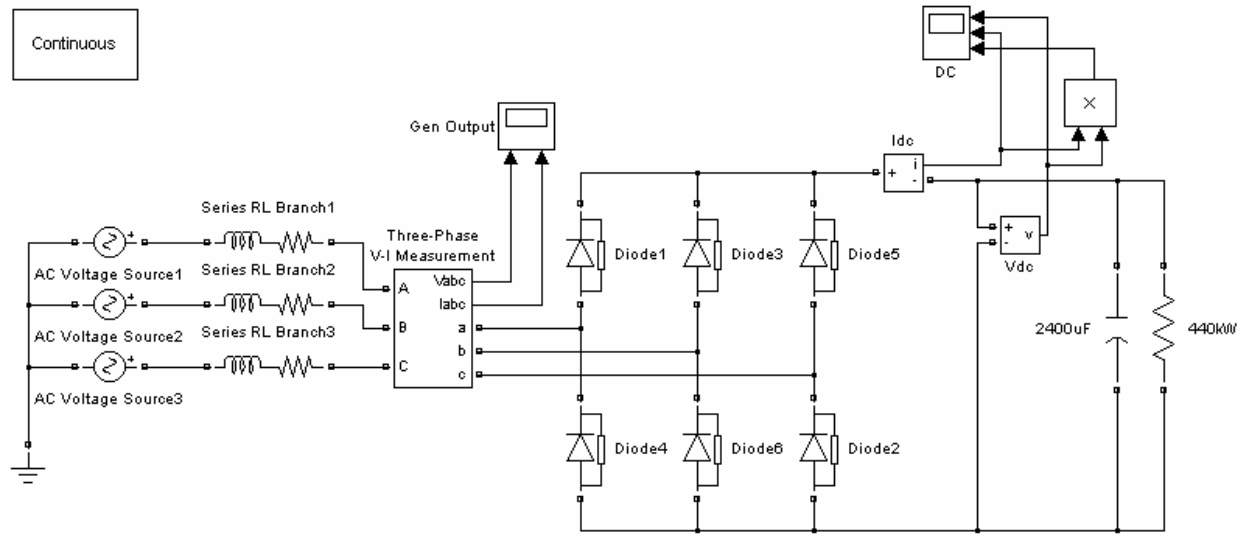


Fig. 7 – Three wye-connected ac sources with passive rectifier.

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are included for both the calculated and reduced inductance values used with the PM Synchronous Machine, shown in Fig. 8(a-d). Fig. 9(a-b) shows the FFT plots displaying harmonic content for each case. As is observed, comparison of results obtained with the PM Synchronous Machine model and three-phase wye-connected ac source model justifies the use of ac sources for the six-phase modeling efforts.

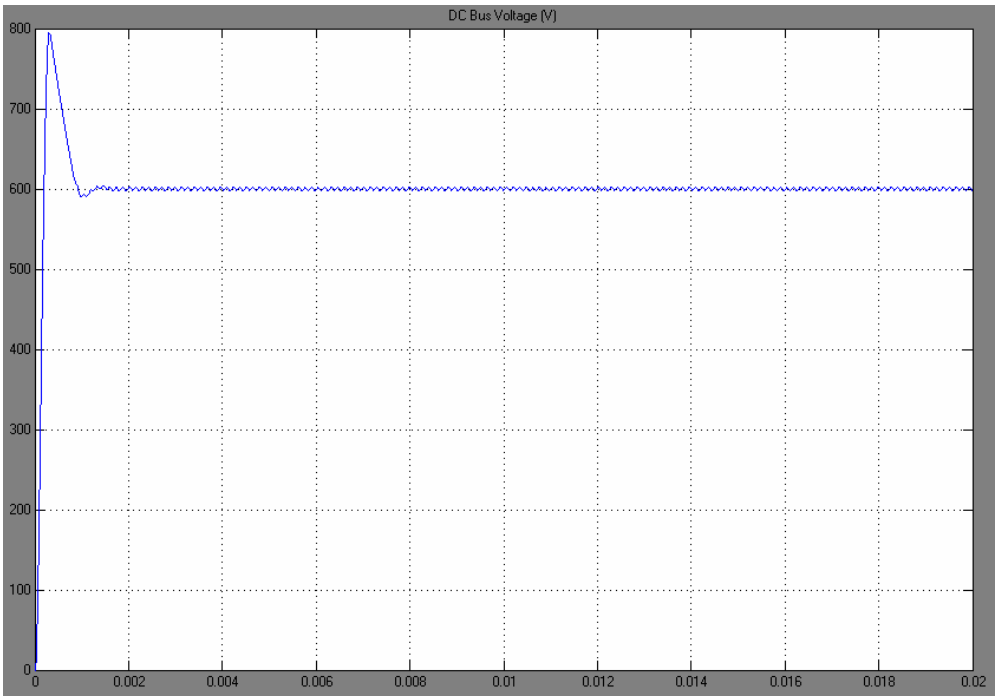


Fig. 8(a) – Dc-bus voltage for the three wye-connected ac source passive rectifier model with calculated inductance.

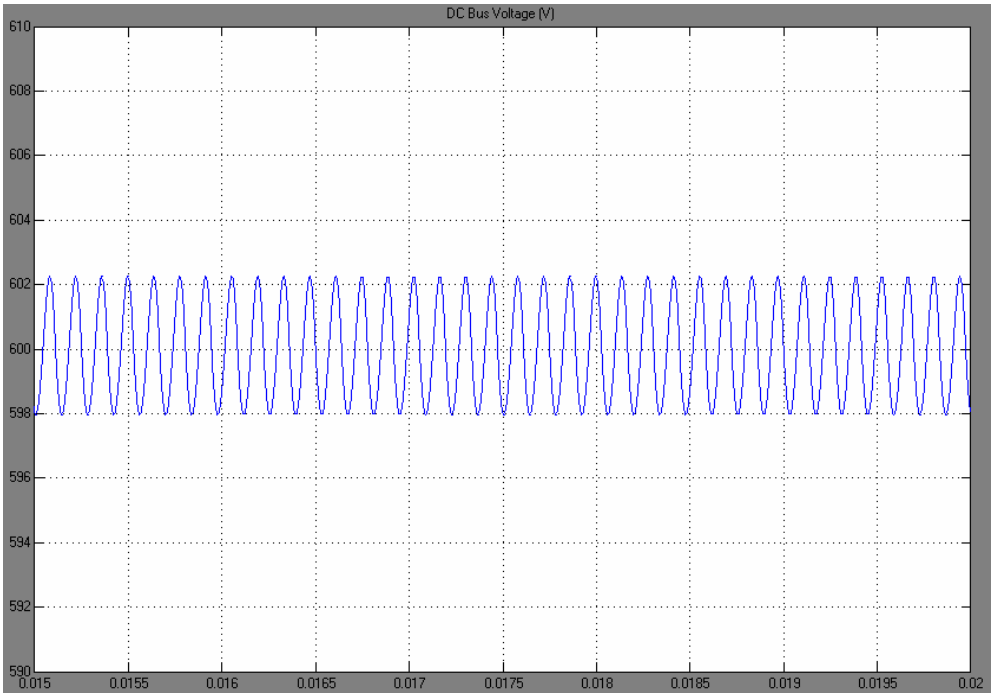


Fig. 8(b) – Dc-bus voltage ripple for the three wye-connected ac source passive rectifier model with calculated inductance.

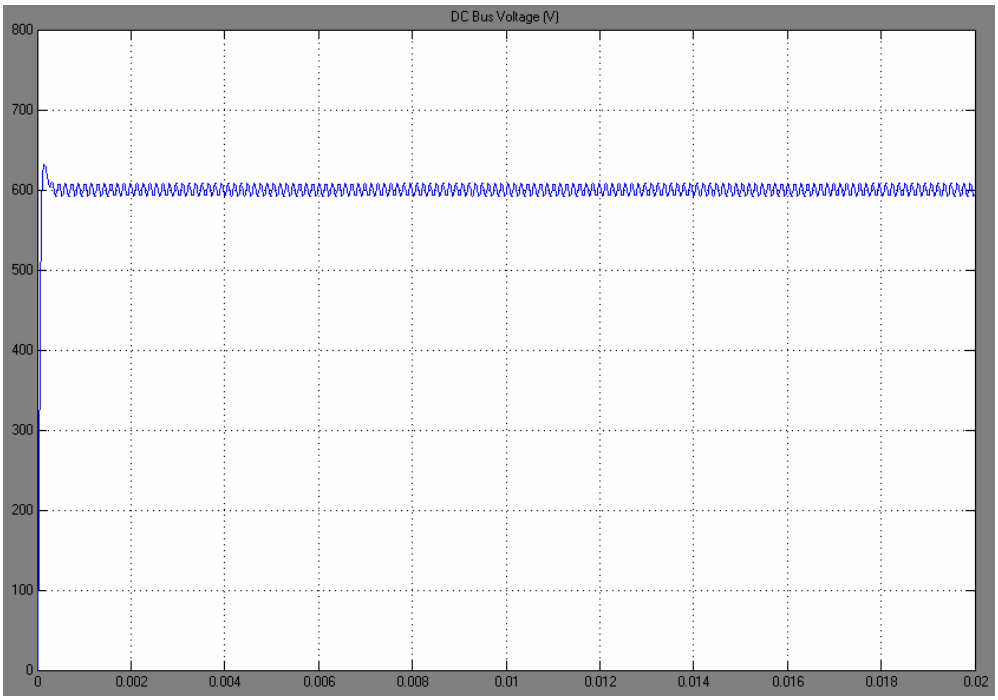


Fig. 8(c) – Dc-bus voltage for the three wye-connected ac source passive rectifier model with reduced inductance.

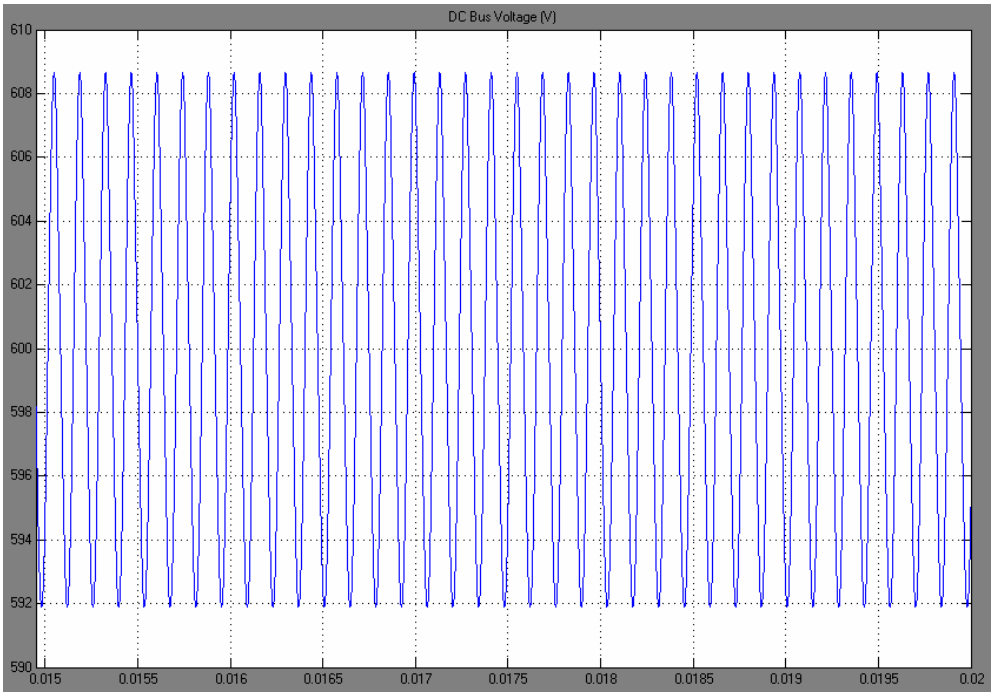


Fig. 8(d) – Dc-bus voltage ripple for the three wye-connected ac source passive rectifier model with reduced inductance.

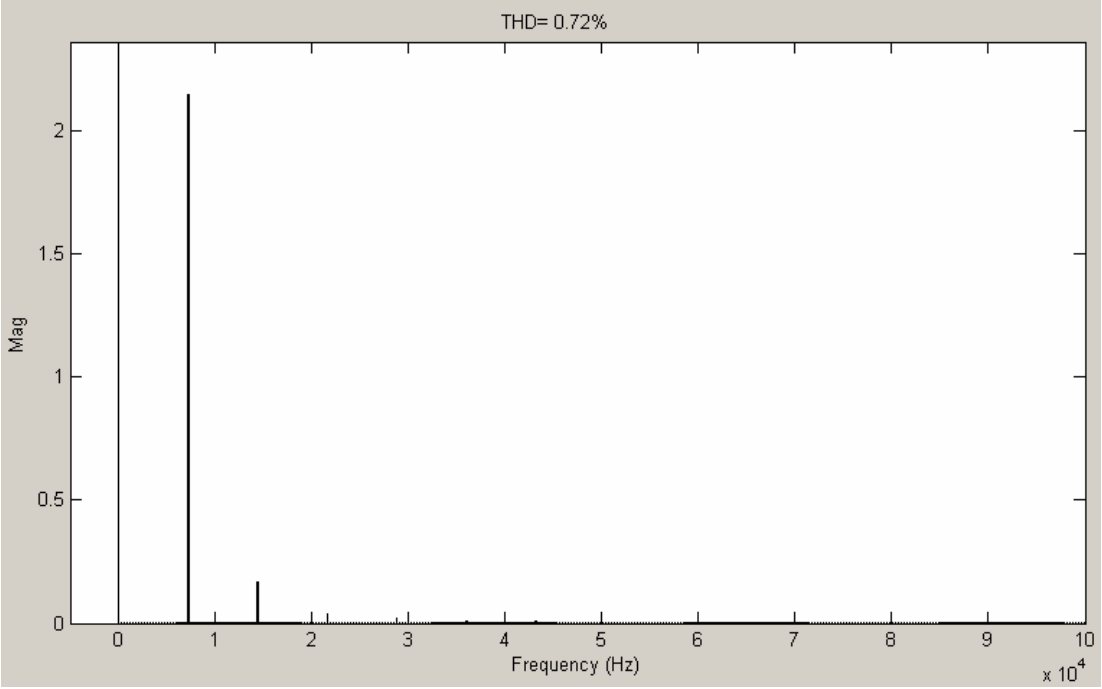


Fig. 9(a) – Dc-bus voltage FFT plot for the three wye-connected ac source passive rectifier model with calculated inductance, dc fundamental is 600.02V.

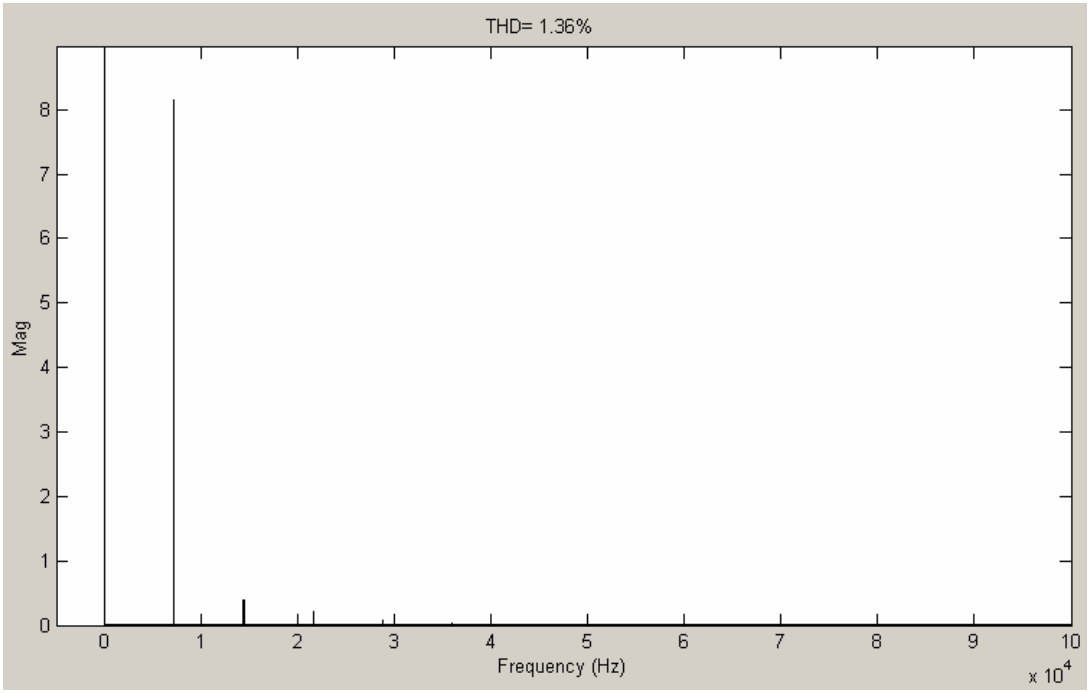


Fig. 9(b) – Dc-bus voltage FFT plot for the three wye-connected ac source passive rectifier model with reduced inductance, dc fundamental is 599.98V.

**2.4 Six Wye-Connected AC Sources with Passive Rectifier**

The six-phase wye-connected generator configuration was modeled using six ac sources displaced by a symmetrical phase shift of 60°, each with a peak phase voltage of 350.0V (428.7$V_{LL}$ rms). Series resistance and inductance values were calculated as 12mΩ and 4.1μH, respectively. Again, for comparison using more sinusoidal source voltages, results were also obtained with the inductance multiplied by 0.1 for a final value of 0.41μH. The Matlab Simulink schematic for this model is shown in Fig. 10.

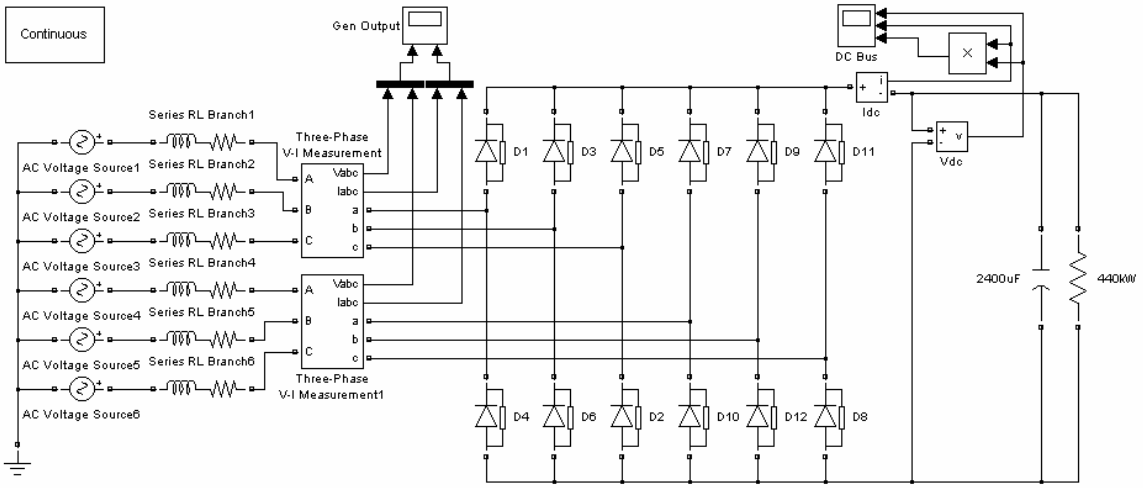


Fig. 10 – Six wye-connected ac sources with passive rectifier.

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are included for both the calculated and reduced inductance values, shown in Fig. 11(a-d). Fig. 12(a-b) shows the FFT plots displaying harmonic content for each case.

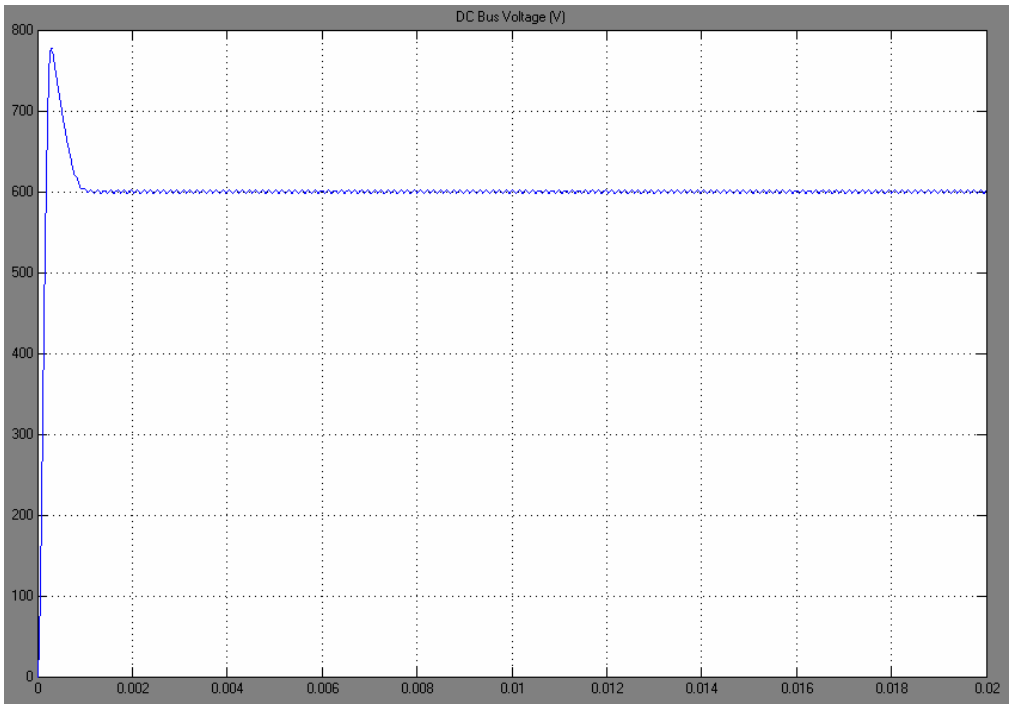


Fig. 11(a) – Dc-bus voltage for the six wye-connected ac source passive rectifier model with calculated inductance.

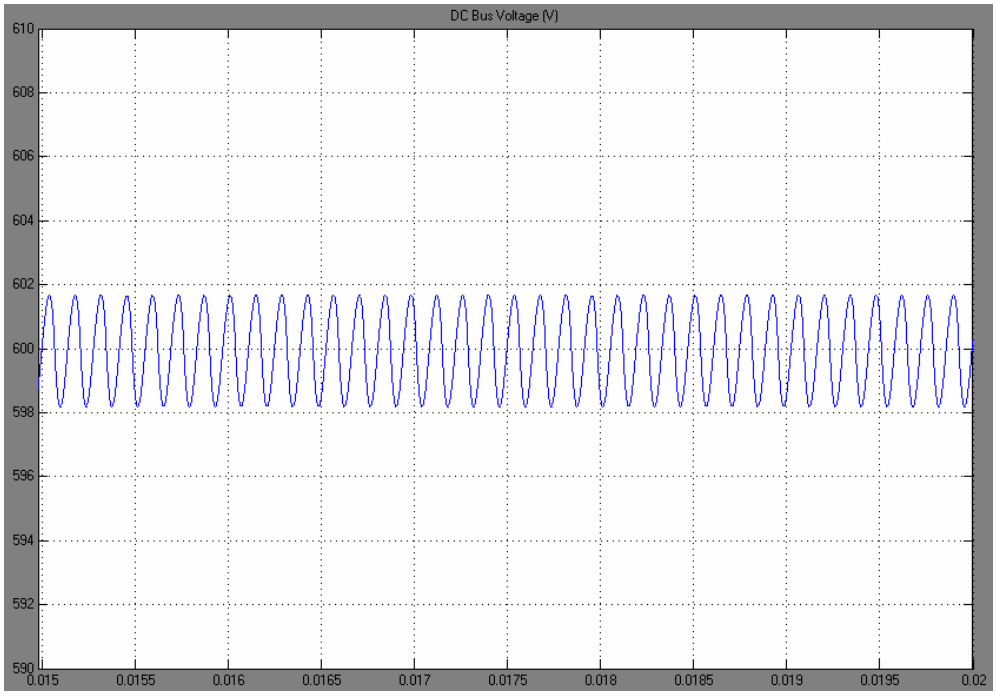


Fig. 11(b) – Dc-bus voltage ripple for the six wye-connected ac source passive rectifier model with calculated inductance.

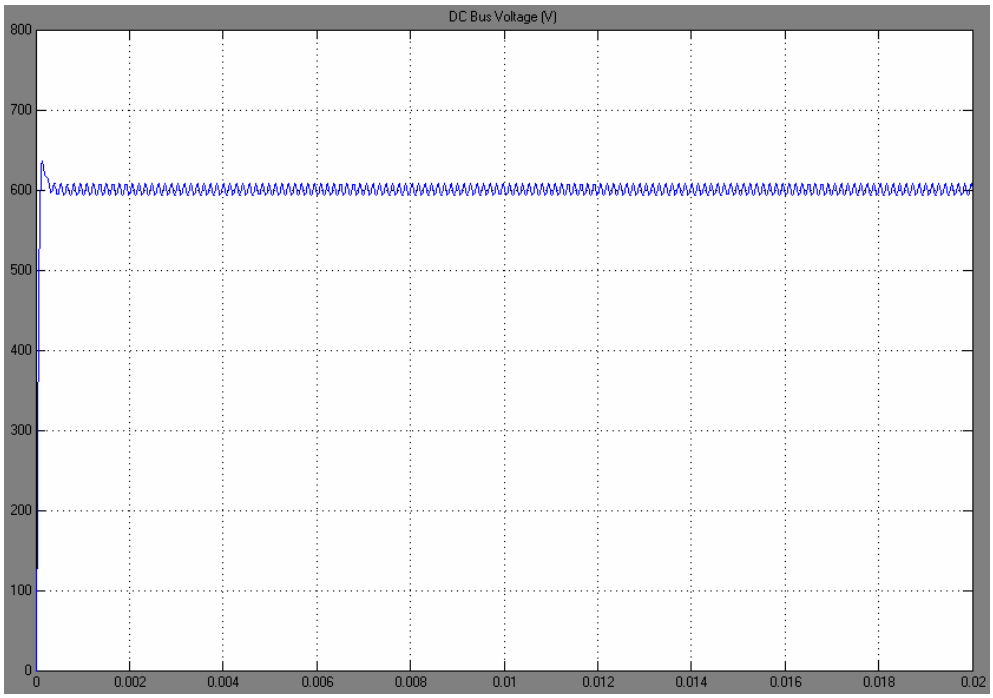


Fig. 11(c) – Dc-bus voltage for the six wye-connected ac source passive rectifier model with reduced inductance.

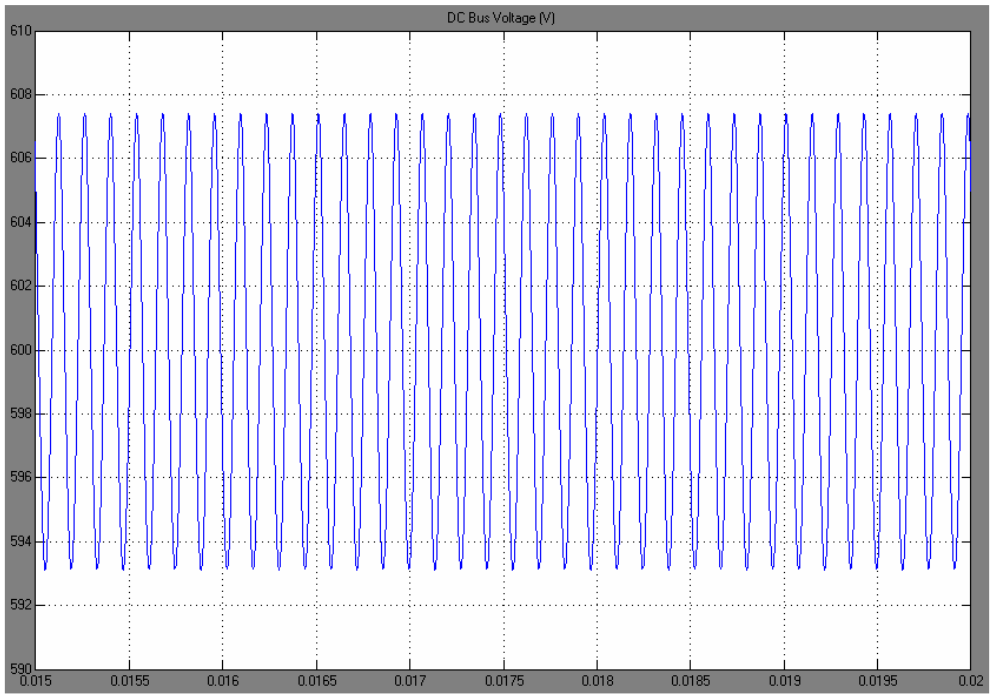


Fig. 11(d) – Dc-bus voltage ripple for the six wye-connected ac source passive rectifier model with reduced inductance.

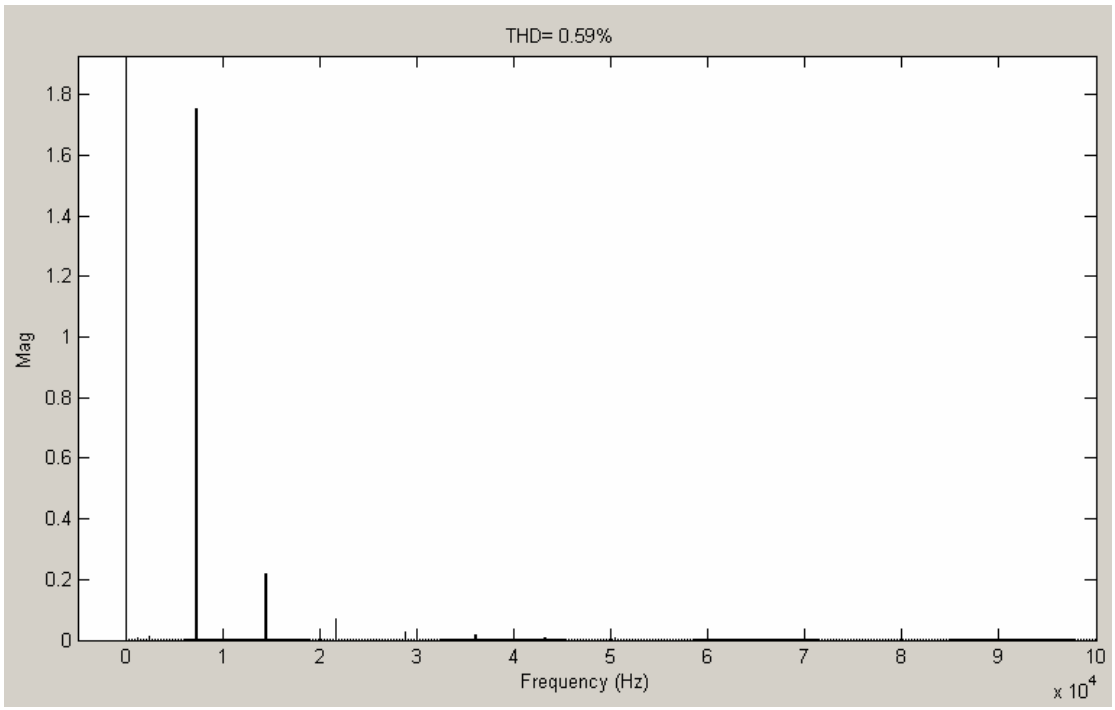


Fig. 12(a) – Dc-bus voltage FFT plot for the six wye-connected ac source passive rectifier model with calculated inductance, dc fundamental is 599.95V.

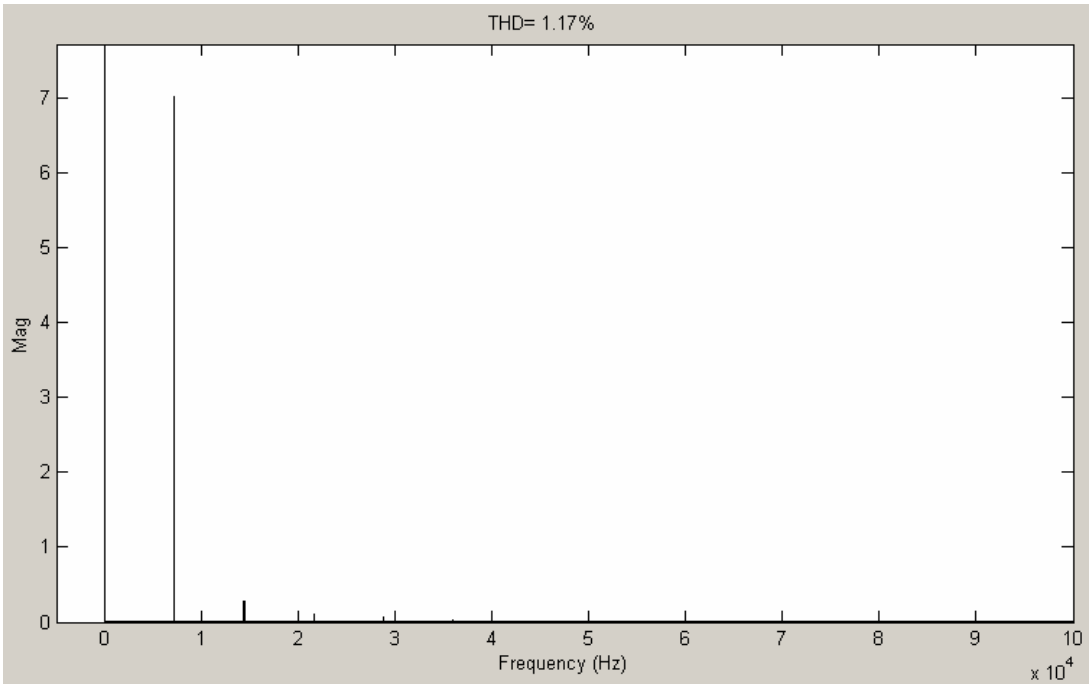


Fig. 12(b) – Dc-bus voltage FFT plot for the six wye-connected ac source passive rectifier model with reduced inductance, dc fundamental is 600.02V.

**2.5 Six Independent Phase Windings with Passive Rectifier**

The six-phase independent winding generator configuration was modeled using six ac sources with series resistance and impedance, each connected to a single-phase full wave H-bridge passive rectifier. The dc outputs of the six rectifiers were connected in parallel to form the dc-bus. In this configuration, the required peak phase voltage of the ac sources to produce a 600V dc-bus was 698.7V (855.7$V_{LL}$ rms). New series resistance and inductance values for the desired efficiency levels were calculated due to this configuration's higher source voltage. A resistance of 49mΩ and an inductance of 16.0μH were calculated with a reduced inductance of 1.6μH also used for comparison. The Matlab Simulink schematic for this model is shown in Fig. 13.

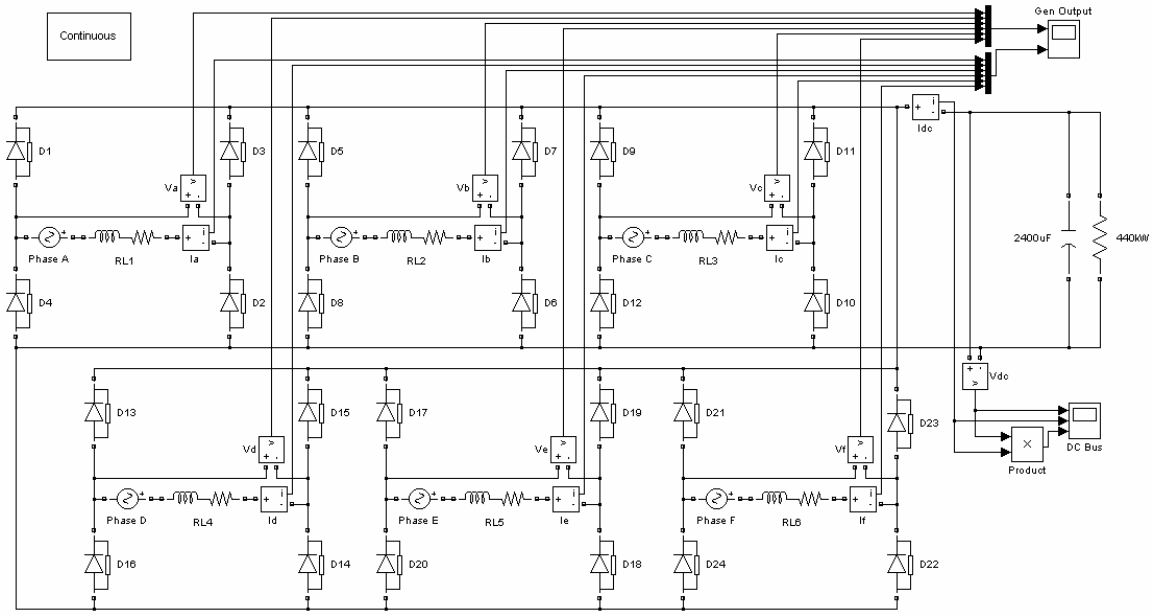


Fig. 13 – Six-phase independent winding configuration with passive rectifier.

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are included for both the calculated and reduced inductance values, shown in Fig. 14(a-d). Fig. 15(a-b) shows the FFT plots displaying harmonic content for each case.

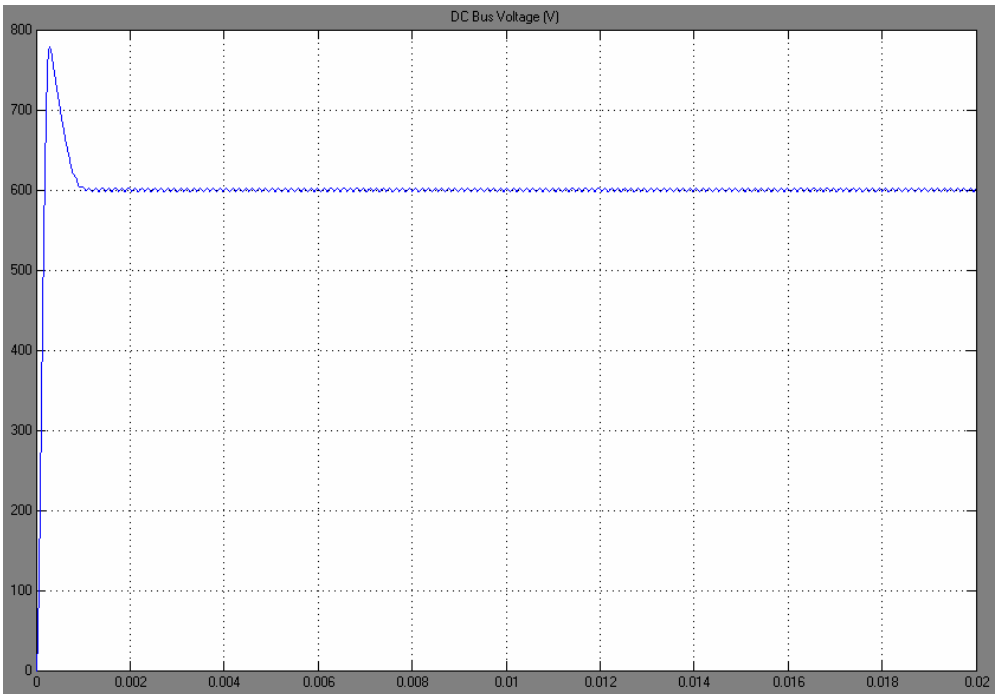


Fig. 14(a) – Dc-bus voltage for the six independent phase passive rectifier model with calculated inductance.

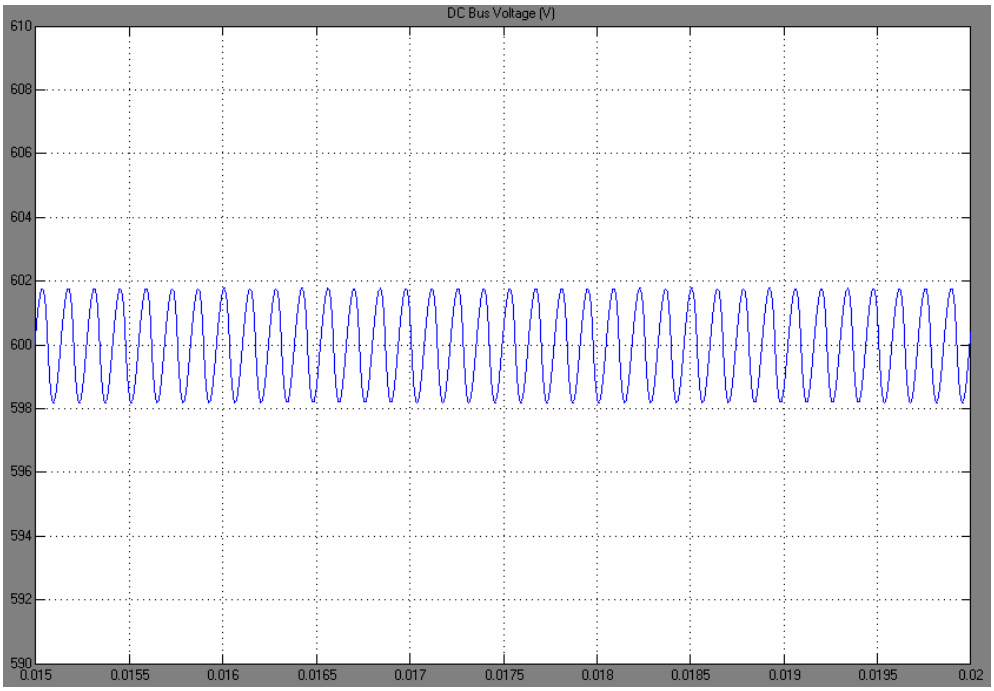


Fig. 14(b) – Dc-bus voltage ripple for the six independent phase passive rectifier model with calculated inductance.

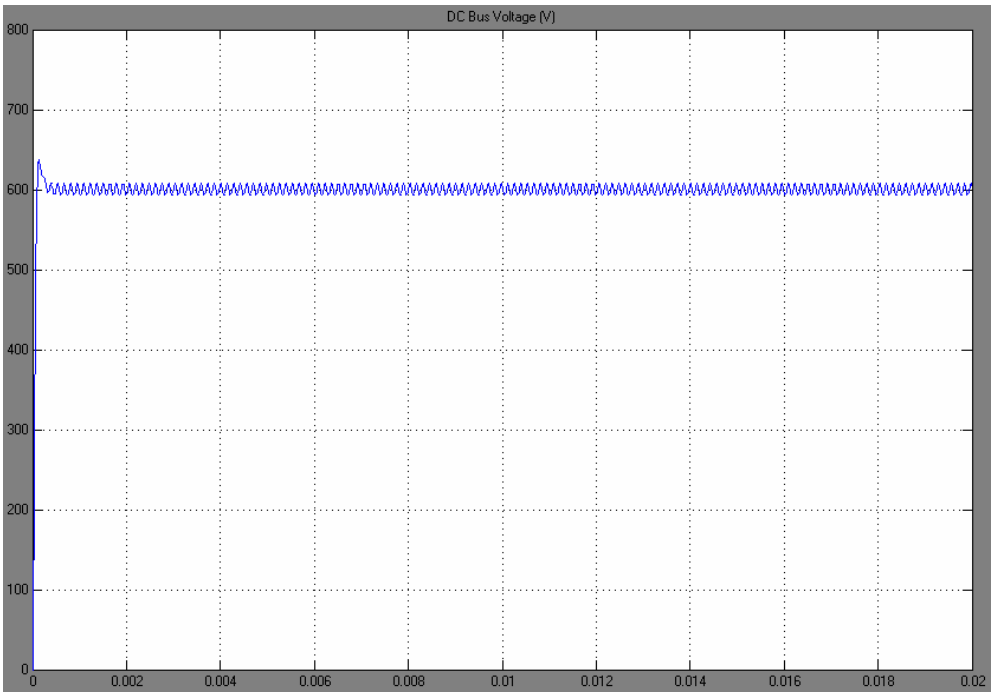


Fig. 14(c) – Dc-bus voltage for the six independent phase passive rectifier model with reduced inductance.

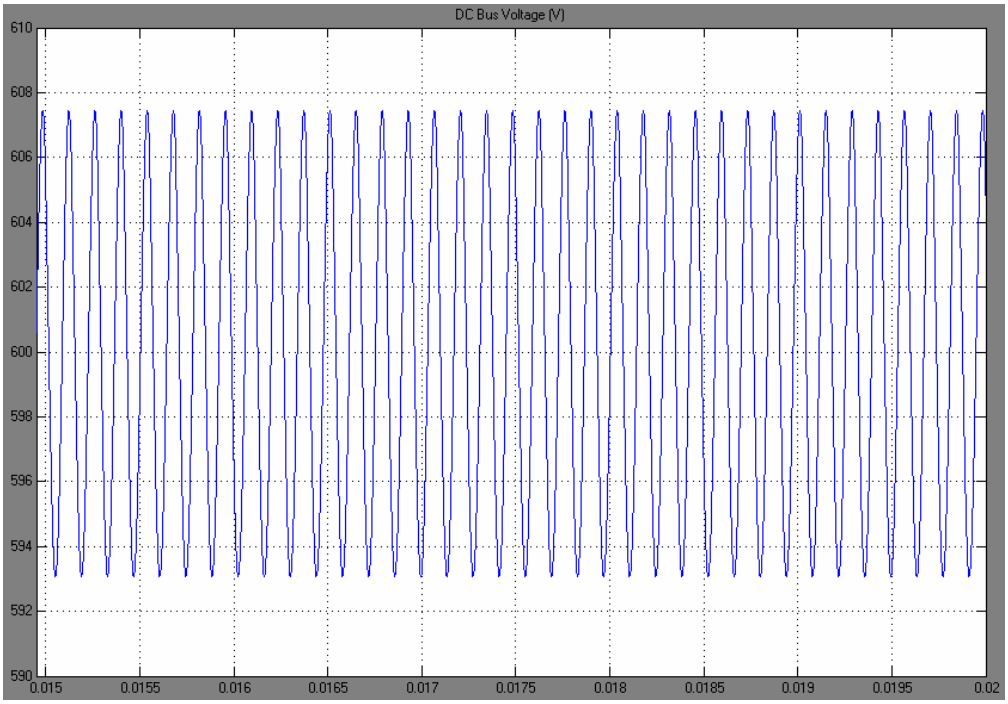


Fig. 14(d) – Dc-bus voltage ripple for the six independent phase passive rectifier model with reduced inductance.

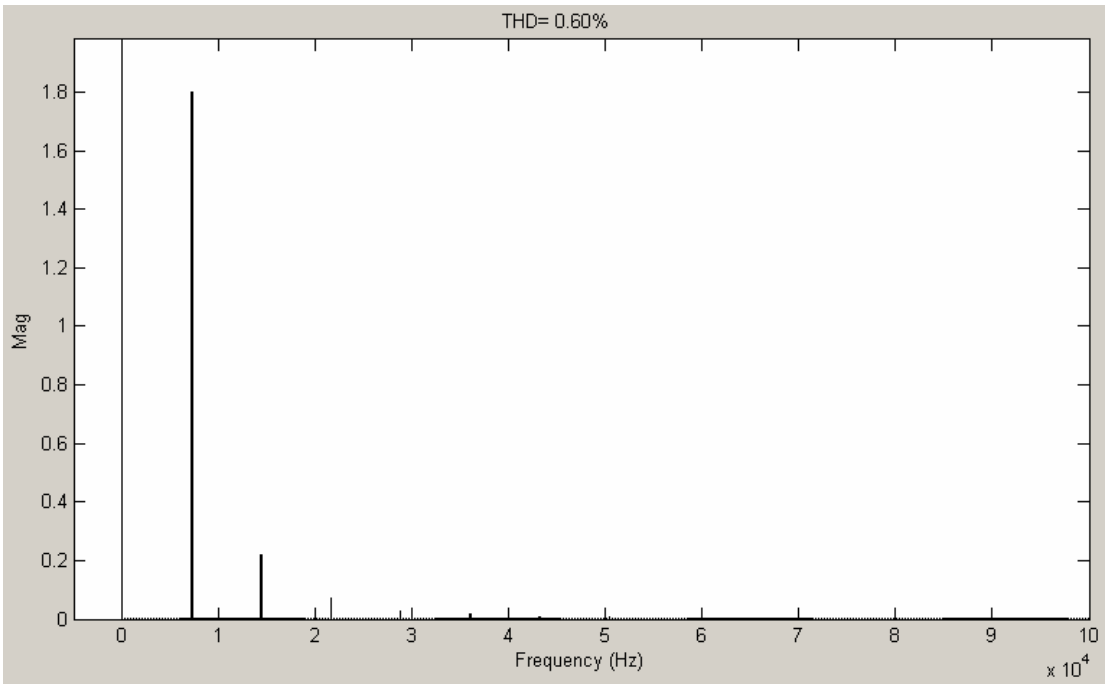


Fig. 15(a) – Dc-bus voltage FFT plot for the six independent phase passive rectifier model with calculated inductance, dc fundamental is 600.00V.

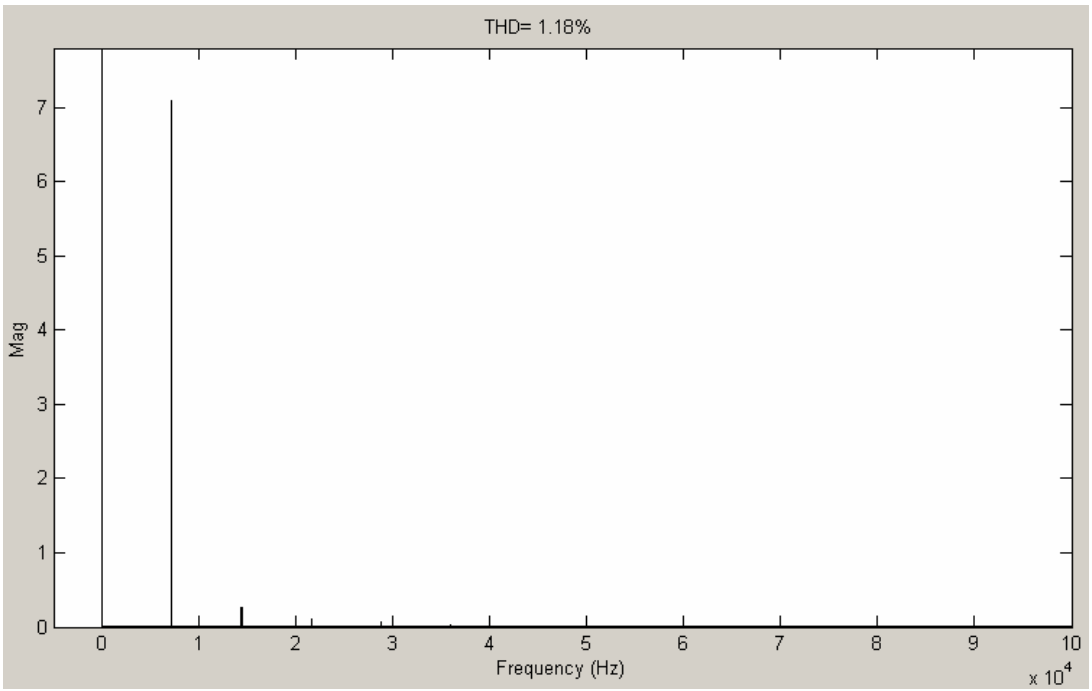


Fig. 15(b) – Dc-bus voltage FFT plot for the six independent phase passive rectifier model with reduced inductance, dc fundamental is 600.01V.

## 2.6 Summary of Passive Rectifier Results

To compare the harmonic content on the dc-bus between the different source configurations, the rms dc-bus current has been measured as well as the average dc voltage. For a more in-depth comparison, harmonic magnitudes and their frequencies are also provided using the calculated inductance values in Table 1 and reduced inductance values in Table 2.

Table 1 – Passive rectifier results using calculated inductance values.

| **Calculated Inductance** | **3-phase PM Synchronous Generator** | **3-phase wye-Connected AC Sources** | **6-phase wye-Connected AC Sources** | **6-phase Independent Windings** |
|---|---|---|---|---|
| **RMS DC-Bus Current (A):** | 752.4 | 752.3 | 746.6 | 747.3 |
| **DC-Bus Ripple Voltage (V):** | 4.2V | 4.2 | 3.6 | 3.7 |
| | | | | |
| **Frequency (kHz)** | **DC-Bus Voltage Harmonic Magnitudes (V)** | | | |
| 0.0 (Fundamental) | 600.12 | 600.02 | 599.95 | 600.00 |
| 7.2 | 2.1513 | 2.1497 | 1.7536 | 1.8000 |
| 14.4 | 0.1698 | 0.1695 | 0.2193 | 0.2191 |
| 21.6 | 0.0405 | 0.0405 | 0.0689 | 0.0704 |
| 28.8 | 0.0196 | 0.0195 | 0.0261 | 0.0262 |
| 36.0 | 0.0113 | 0.0113 | 0.0148 | 0.0150 |
| 43.2 | 0.0063 | 0.0063 | 0.0078 | 0.0079 |
| 50.4 | 0.00356 | 0.00356 | 0.00531 | 0.00535 |
| 57.6 | 0.00238 | 0.00237 | 0.00334 | 0.00340 |
| 64.8 | 0.00182 | 0.00182 | 0.00246 | 0.00246 |
| 72.0 | 0.00135 | 0.00135 | 0.00174 | 0.00178 |
| 79.2 | 0.000954 | 0.000955 | 0.001320 | 0.001320 |
| 86.4 | 0.000707 | 0.000705 | 0.001020 | 0.001050 |
| 93.6 | 0.000585 | 0.000583 | 0.000792 | 0.000786 |

Table 2 – Passive rectifier results using reduced inductance values.

| **Reduced Inductance** | **3-phase PM Synchronous Generator** | **3-phase wye-Connected AC Sources** | **6-phase wye-Connected AC Sources** | **6-phase Independent Windings** |
|---|---|---|---|---|
| **RMS DC-Bus Current (A):** | 970.3 | 968.3 | 913.5 | 915.5 |
| **DC-Bus Ripple Voltage (V):** | 16.4 | 16.4 | 17.0 | 17.1 |
| | | | | |
| **Frequency (kHz)** | **DC-Bus Voltage Harmonic Magnitudes (V)** | | | |
| 0.0 (Fundamental) | 600.02 | 599.98 | 600.02 | 600.01 |
| 7.2 | 8.195 | 8.160 | 7.056 | 7.100 |
| 14.4 | 0.414 | 0.398 | 0.271 | 0.265 |
| 21.6 | 0.227 | 0.224 | 0.106 | 0.110 |
| 28.8 | 0.0834 | 0.0841 | 0.0614 | 0.0633 |
| 36.0 | 0.0292 | 0.0295 | 0.0345 | 0.0351 |
| 43.2 | 0.0192 | 0.0187 | 0.0191 | 0.0191 |
| 50.4 | 0.0149 | 0.0148 | 0.0106 | 0.0104 |
| 57.6 | 0.00945 | 0.00954 | 0.00634 | 0.00626 |
| 64.8 | 0.00555 | 0.00557 | 0.00440 | 0.00448 |
| 72.0 | 0.00424 | 0.00411 | 0.00348 | 0.00361 |
| 79.2 | 0.00363 | 0.00358 | 0.00283 | 0.00291 |
| 86.4 | 0.00273 | 0.00276 | 0.00224 | 0.00226 |
| 93.6 | 0.00193 | 0.00193 | 0.00171 | 0.00169 |

# 3. VOLTAGE-CONTROLLED ACTIVE RECTIFIER INVESTIGATIONS

## 3.1 Three-Phase Wye-Connected Active Rectifier

The three-phase active rectifier model was constructed using three ac sources in a wye-configuration. For comparison, resistance and inductance values identical to those calculated for the three-phase passive rectifier model were used, 8.0mΩ and 2.7μH respectively. The ac sources were set to a peak phase voltage of 285.8V (350.0$V_{LL}$ rms) with a frequency of 1.2 kHz. For construction of the three-phase active rectifier bridge, the Universal Bridge block from the SimPowerSystems library in Matlab Simulink was modified and used. This block allows the choice of utilizing different semiconductor devices and defining their properties, as well as outputting measurements for display using a Multimeter block. For the active rectifier design, IGBT switches and reverse connected diodes with series RC snubber circuits connected in parallel were utilized. Parameters of the switches include an on-resistance of 1.0mΩ, snubber resistance of 50Ω, and snubber capacitance of 250nF. Gating signals for the universal bridge are provided by the PWM Generator subsystem. The Matlab Simulink schematic of the active rectifier model is shown in Fig. 16.

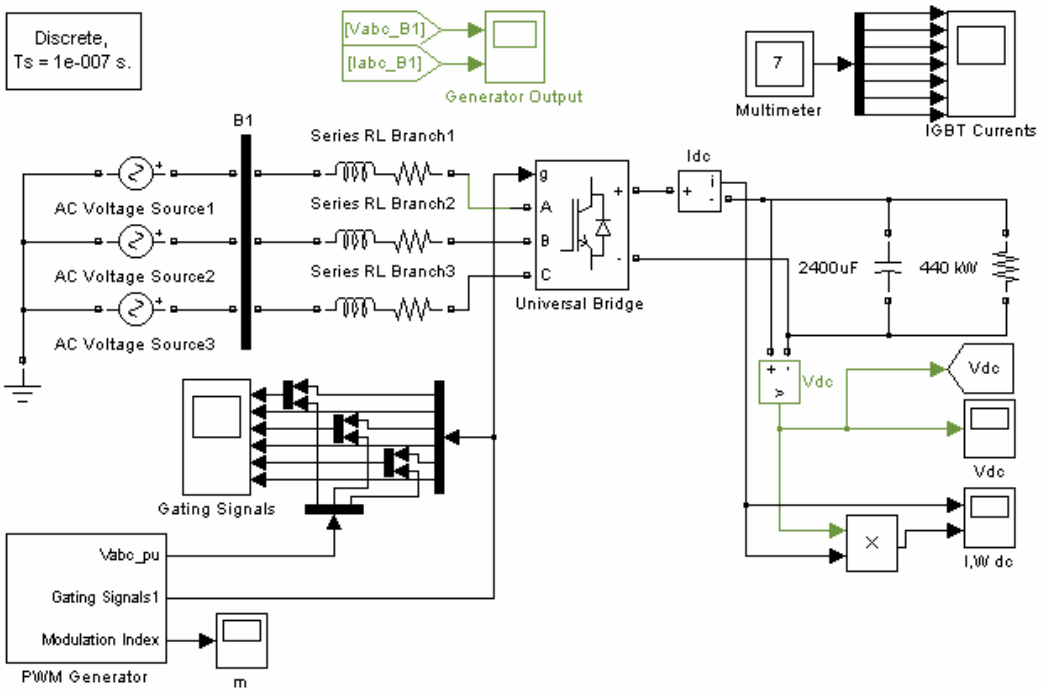


Fig. 16 – Three wye-connected ac sources with active rectifier.

### *3.1.1 Three-Phase Wye-Connected Active Rectifier Voltage Control*

A simple form of voltage control was performed by the PWM Generator subsystem. This block takes the per-unit three-phase source voltage and multiplies this by a calculated modulation index to produce the modulated sine wave used for sine-triangle modulation. The modulation index is calculated as in (1) by multiplying the difference between the actual (*Vdc*) and desired (*Vref*) dc-bus voltage level with a tunable gain (*G*) and adding this value to the product of the average modulation index (*Mavg*) and the actual dc voltage divided by the desired voltage. The modulation index is then limited to the range of 0.5 to 1.0, as this is the range where a near-linear response in the output voltage is observed. The gain used in simulation was 0.001 and the average modulation index was given an initial value of 0.5 with the mean calculated at the fundamental electrical frequency, 1.2 kHz.

$$m = G \cdot (Vdc - Vref) + \frac{(\text{Mavg})Vdc}{Vref} \tag{1}$$

The product of this modulation index and the per-unit three-phase source voltage is then compared with a triangle function to determine the gating signals. Dead time between the on-states of complimentary devices is introduced by shifting the triangle wave up for the top switches and down for the lower switches. The Unit Delay block on the gating signals connection is required to prevent an algebraic loop and greatly reduces simulation time. The delay is one simulation time step, maximum of which is 0.1μs, so there is negligible effect on the active rectifier performance. The Matlab Simulink schematic of the three-phase voltage-controlled PWM Generator is shown in Fig. 17.

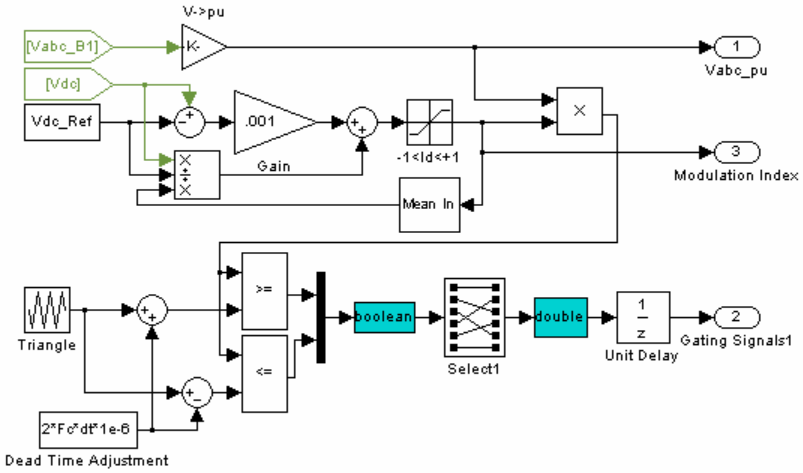


Fig. 17 – Three-phase voltage-controlled PWM Generator.

### *3.1.2 Three-Phase Wye-Connected Active Rectifier Results*

The three-phase active rectifier was simulated with switching frequencies of 10 kHz, 15 kHz, and 20 kHz. For each switching frequency, results were found using dead times of 2µs and 5µs. A 2µs dead time was chosen because the IGBTs have a fall time of 1µs and a tail time of 1µs, however, at this setting, shorting of the dc-bus was occurring. To reduce shorting of the dc-bus, the increased dead time of 5µs was simulated. For comparison with the passive rectifier results, dc-bus voltage and rms current are provided for each case in Table 3. It should be noted that the rms dc-bus currents are higher than with the passive rectifier models due to the increased higher frequency harmonics caused by switching.

Table 3 – Three-phase active rectifier results.

| **Carrier Frequency:** | **10 kHz** | | **15kHz** | | **20kHz** | |
|---|---|---|---|---|---|---|
| **Dead Time:** | **2µs** | **5µs** | **2µs** | **5µs** | **2µs** | **5µs** |
| DC-Bus Voltage (V): | 599.9 | 599.8 | 600.0 | 600.0 | 600.0 | 600.0 |
| RMS DC-Bus Current (A): | 1091.8 | 1013.5 | 956.0 | 900.6 | 899.0 | 862.8 |

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are shown in Fig. 18(a-l) for each carrier frequency and dead time case. Harmonic content for each case is given by the FFT plots in Fig. 19(a-f).

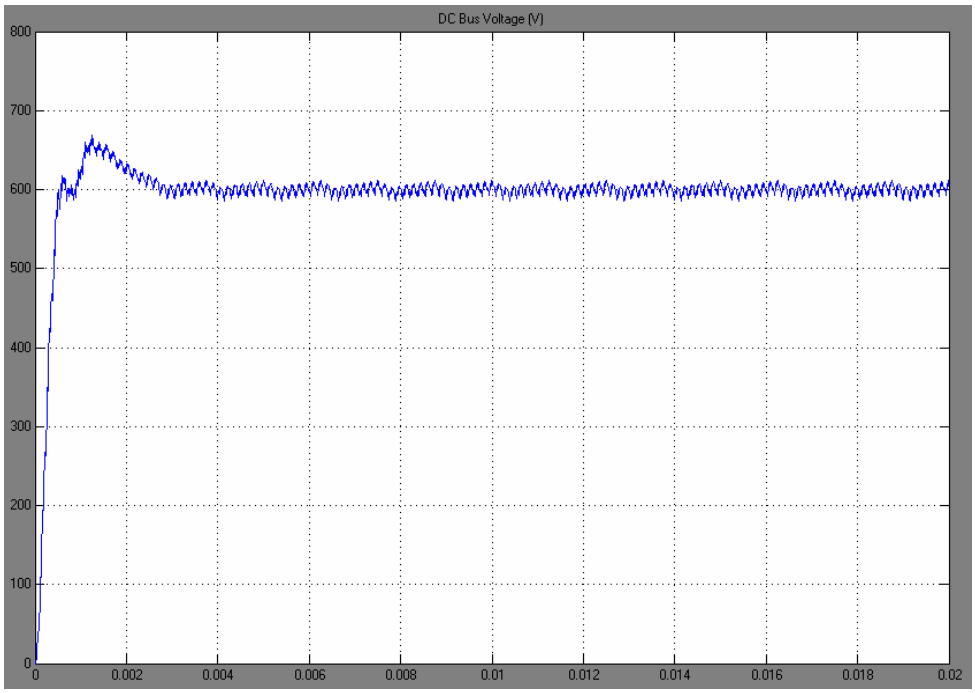


Fig. 18(a) – Dc-bus voltage waveform of the three-phase active rectifier, 10 kHz carrier frequency, 2µs dead time.

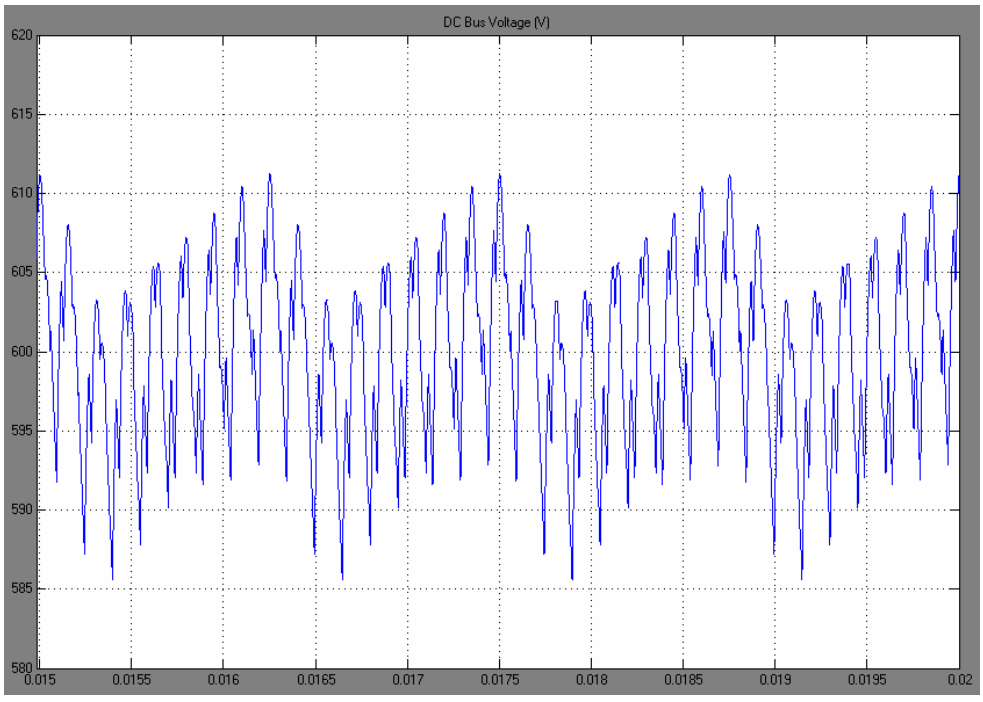


Fig. 18(b) – Dc-bus voltage ripple of the three-phase active rectifier, 10 kHz carrier frequency, 2µs dead time.

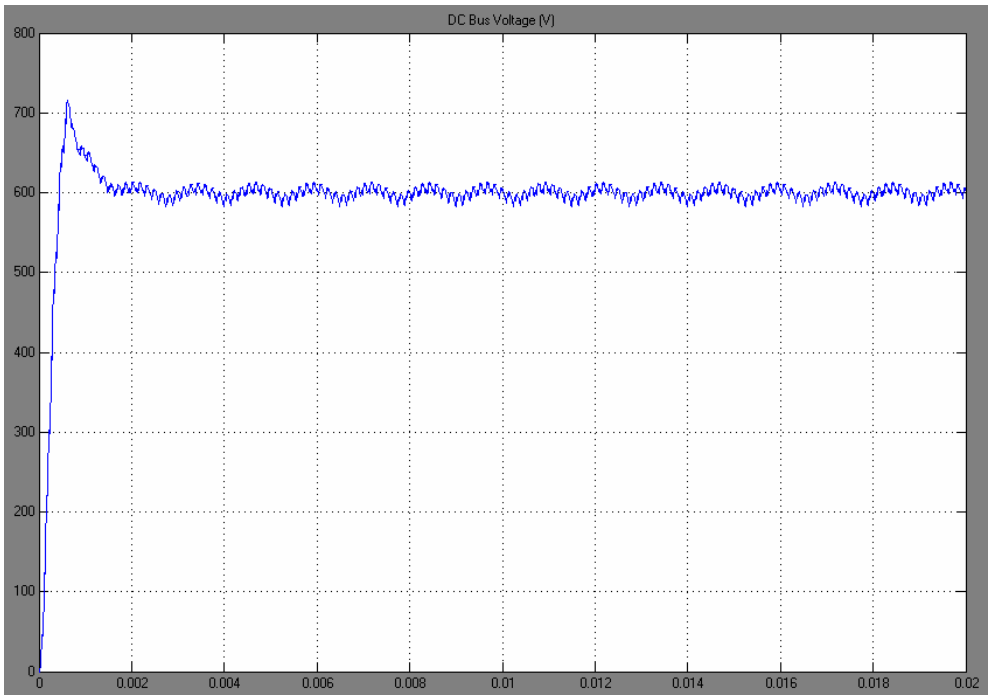


Fig. 18(c) – Dc-bus voltage waveform of the three-phase active rectifier, 10 kHz carrier frequency, 5µs dead time.

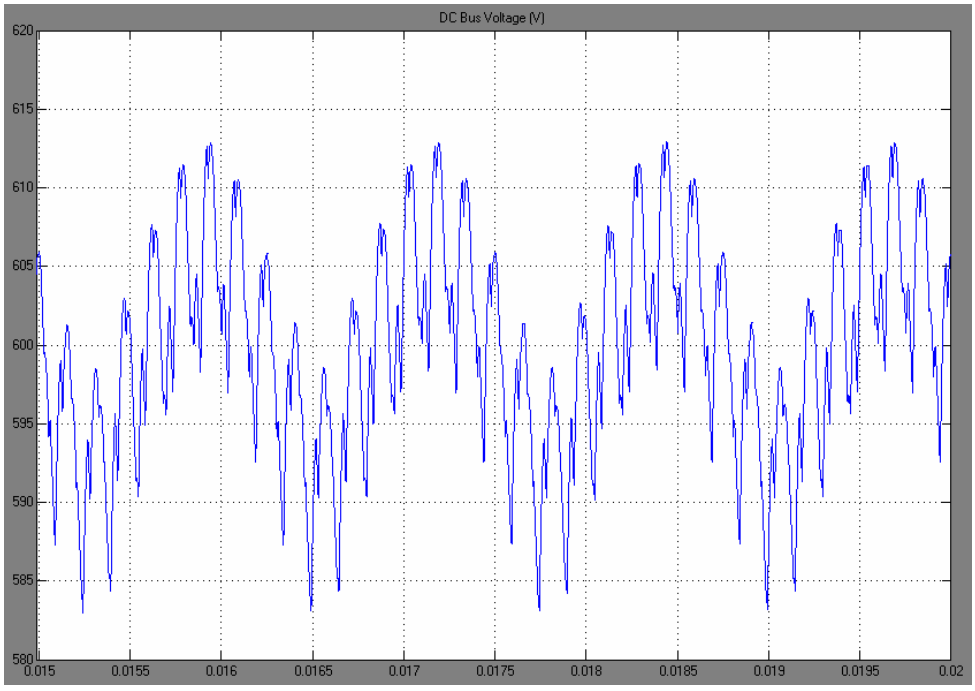


Fig. 18(d) – Dc-bus voltage ripple of the three-phase active rectifier, 10 kHz carrier frequency, 5µs dead time.

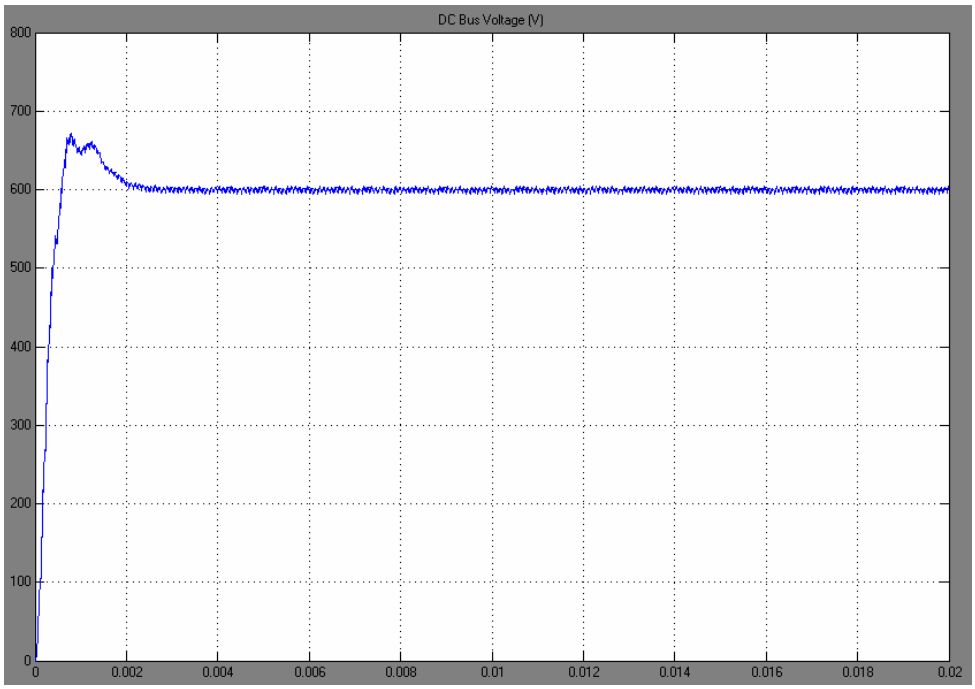


Fig. 18(e) – Dc-bus voltage waveform of the three-phase active rectifier, 15 kHz carrier frequency, 2µs dead time.

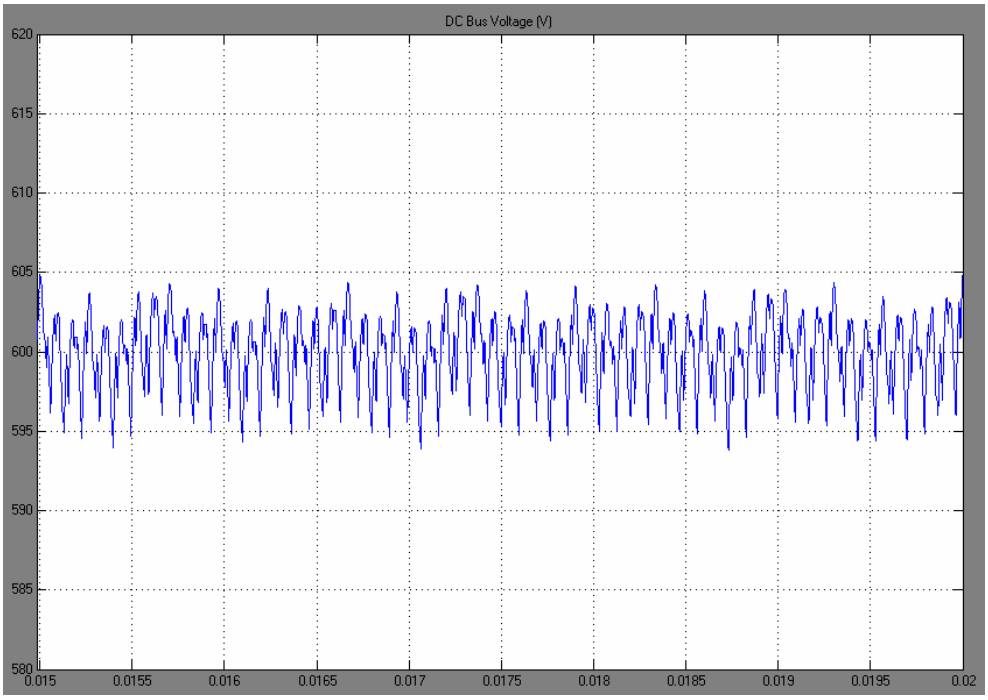


Fig. 18(f) – Dc-bus voltage ripple of the three-phase active rectifier, 15 kHz carrier frequency, 2µs dead time.

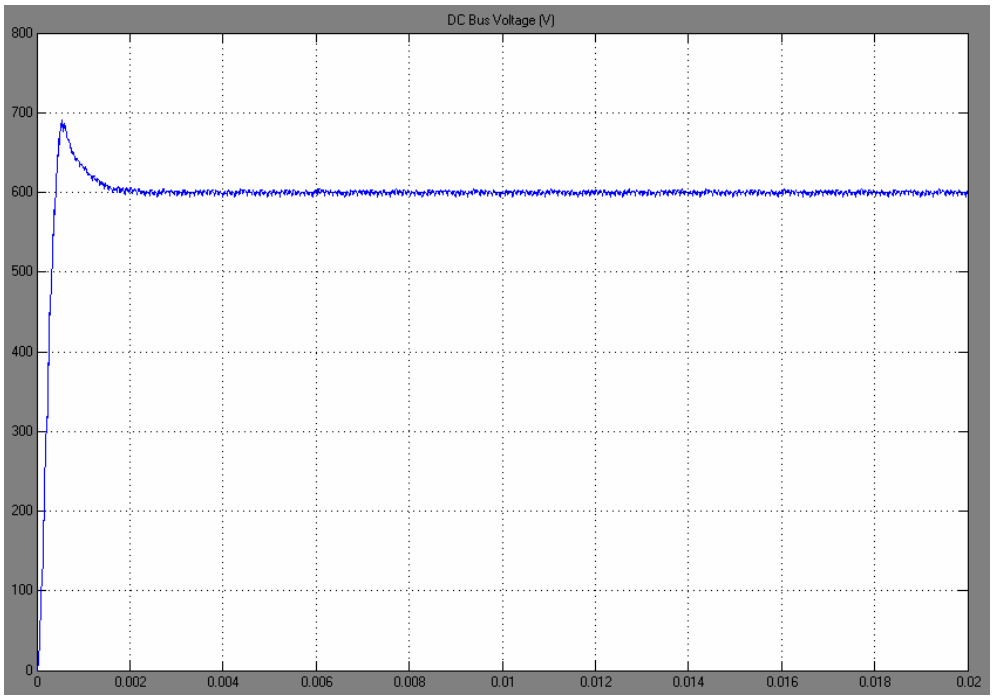


Fig. 18(g) – Dc-bus voltage waveform of the three-phase active rectifier, 15 kHz carrier frequency, 5µs dead time.

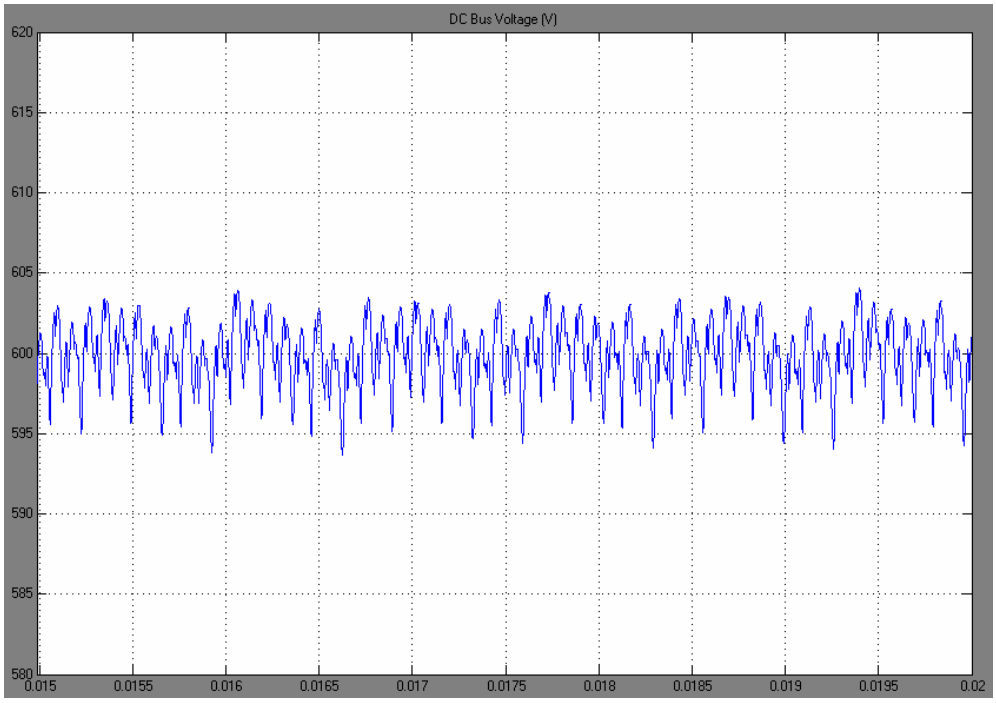


Fig. 18(h) – Dc-bus voltage ripple of the three-phase active rectifier, 15 kHz carrier frequency, 5µs dead time.

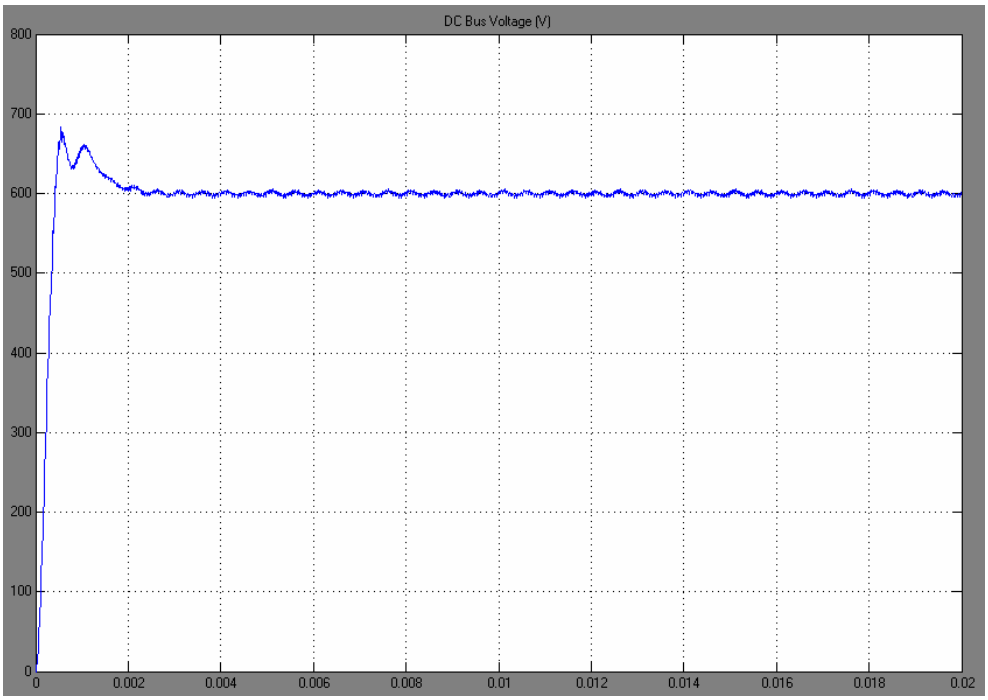


Fig. 18(i) – Dc-bus voltage waveform of the three-phase active rectifier, 20 kHz carrier frequency, 2µs dead time.

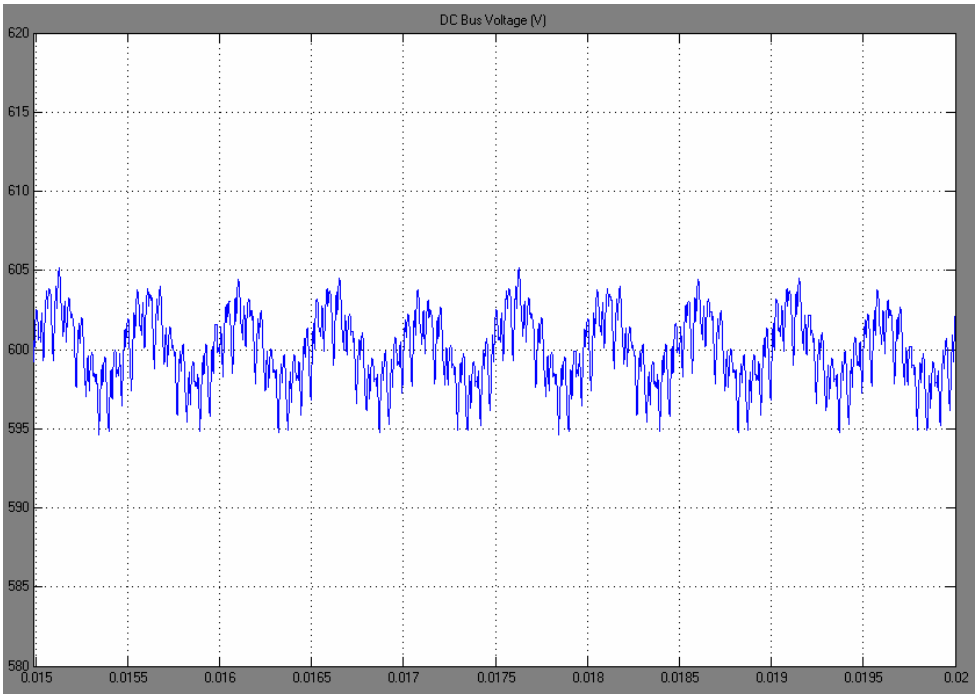


Fig. 18(j) – Dc-bus voltage ripple of the three-phase active rectifier, 20 kHz carrier frequency, 2µs dead time.

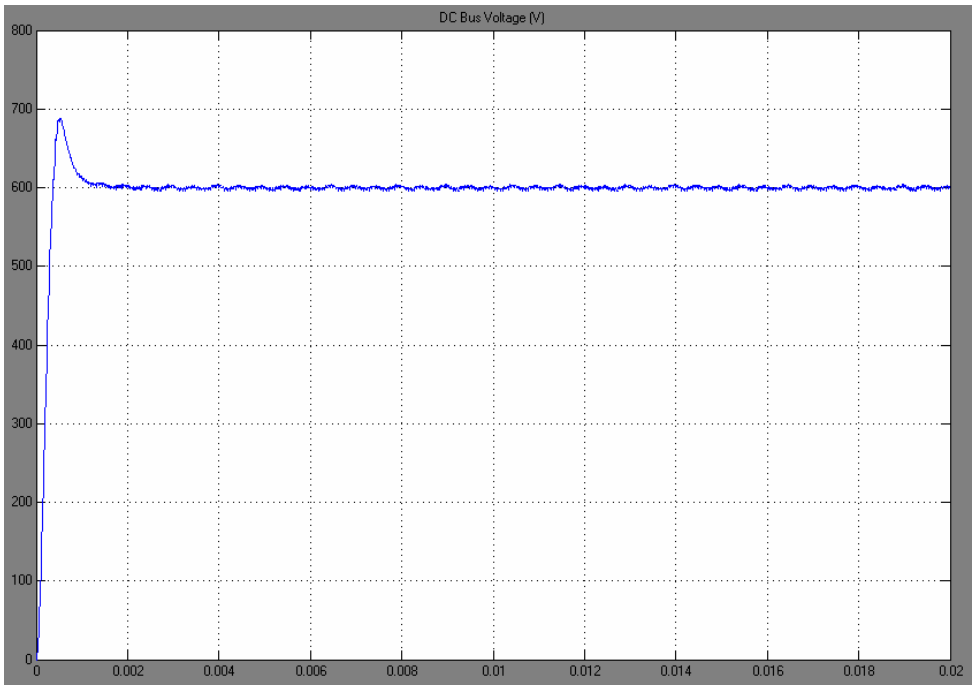


Fig. 18(k) – Dc-bus voltage waveform of the three-phase active rectifier, 20 kHz carrier frequency, 5µs dead time.

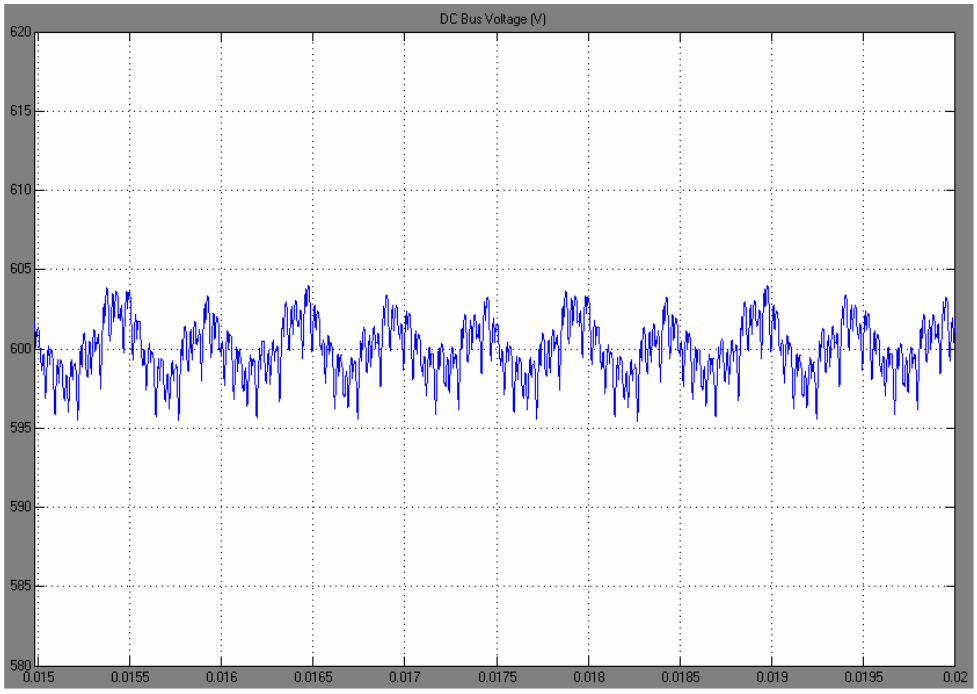


Fig. 18(l) – Dc-bus voltage ripple of the three-phase active rectifier, 20 kHz carrier frequency, 5µs dead time.

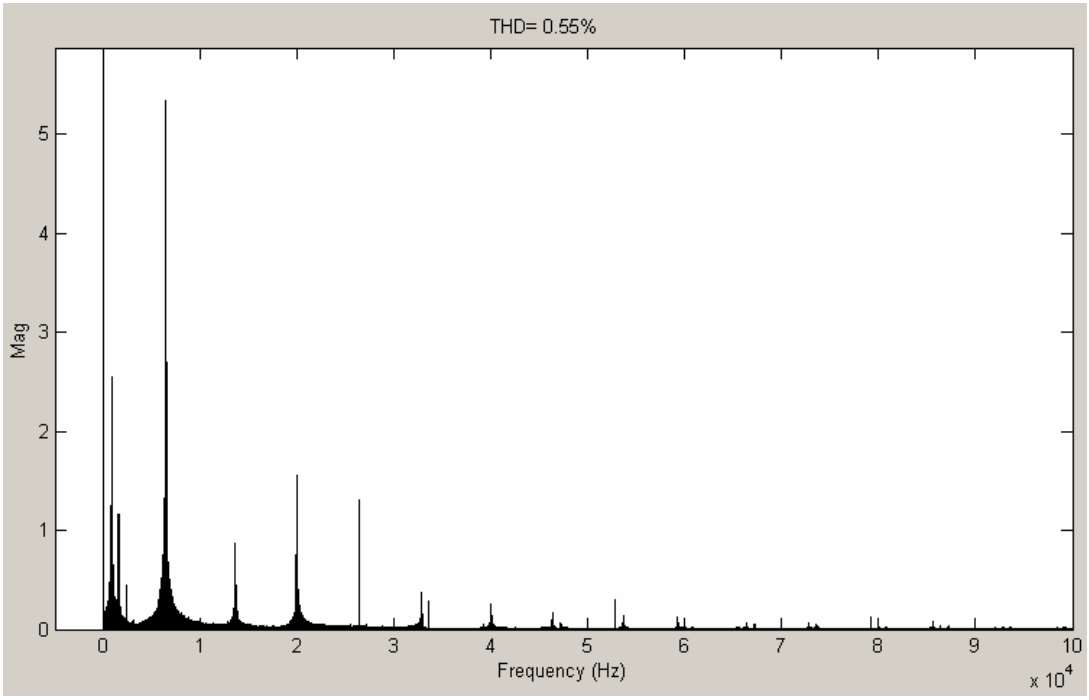


Fig. 19(a) – Dc-bus FFT plot of the three-phase active rectifier, 10 kHz carrier frequency, 2μs dead time, dc fundamental is 599.9V.

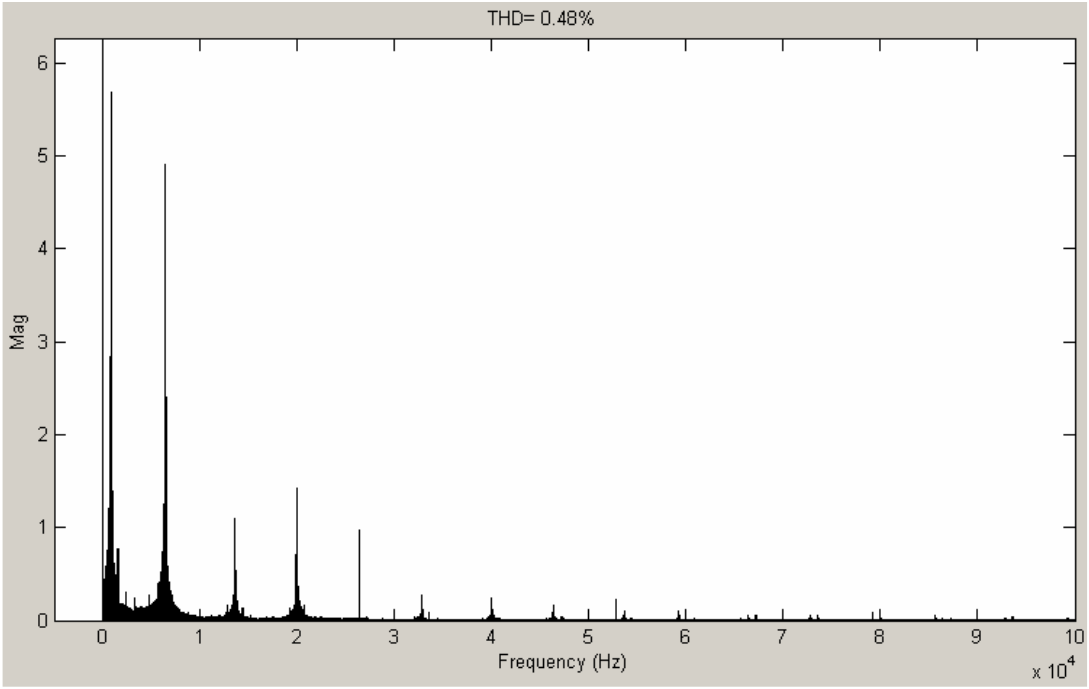


Fig. 19(b) – Dc-bus FFT plot of the three-phase active rectifier, 10 kHz carrier frequency, 5μs dead time, dc fundamental is 599.8V.

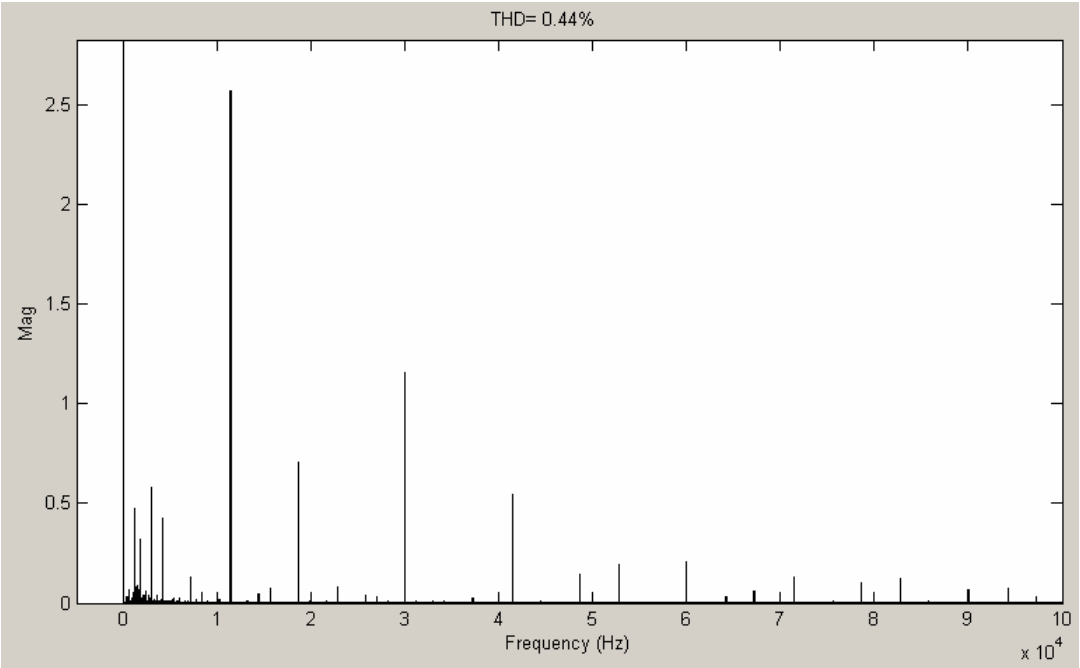


Fig. 19(c) – Dc-bus FFT plot of the three-phase active rectifier, 15 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

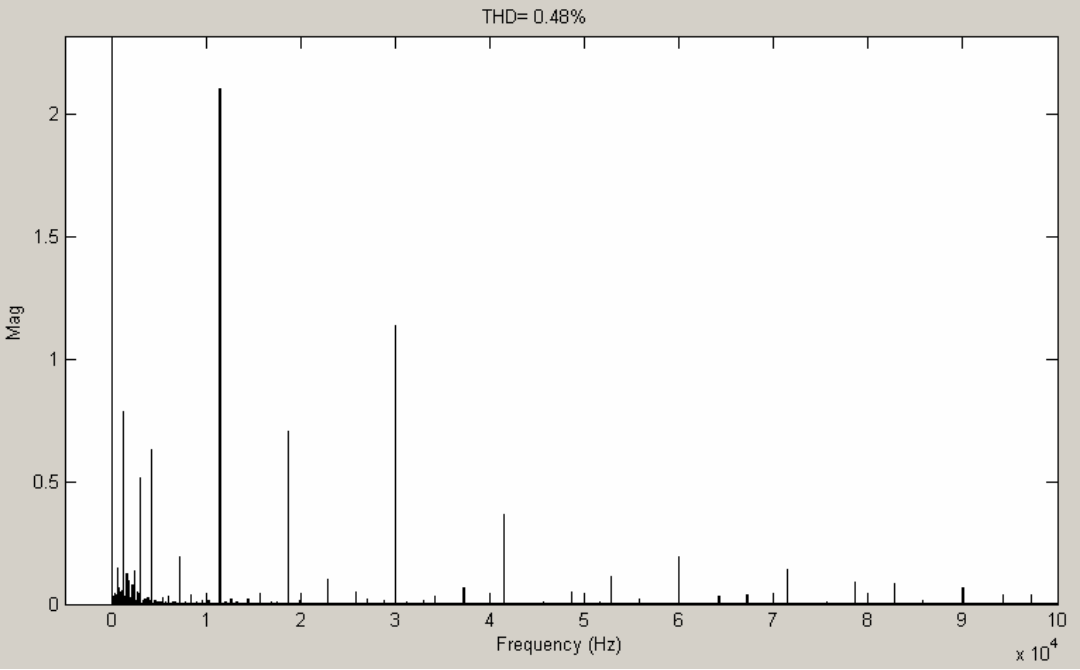


Fig. 19(d) – Dc-bus FFT plot of the three-phase active rectifier, 15 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

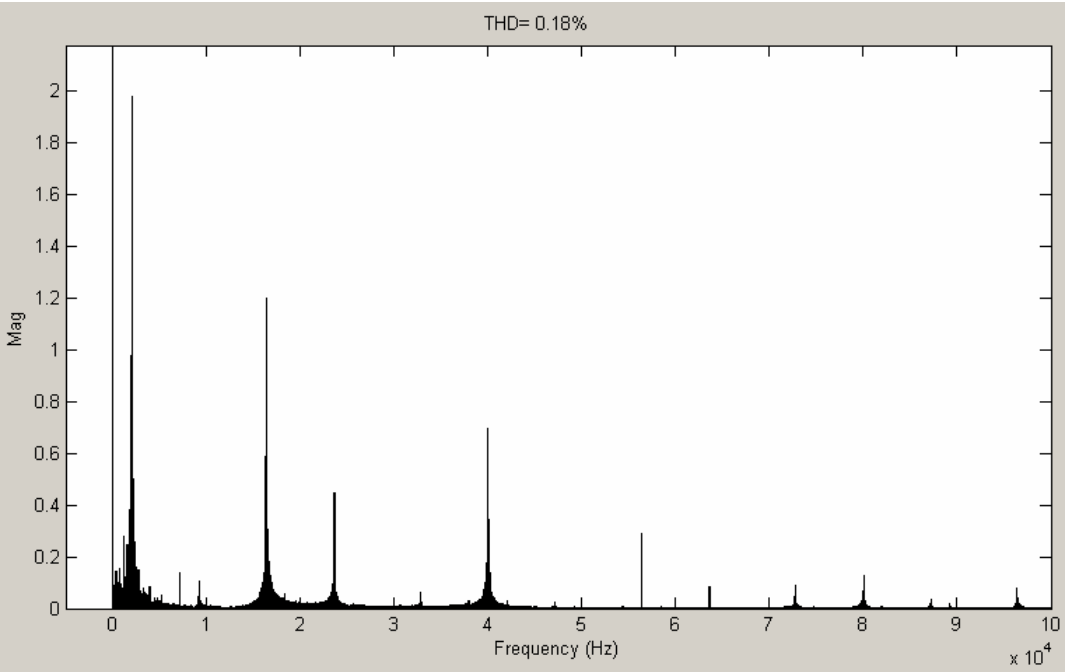


Fig. 19(e) – Dc-bus FFT plot of the three-phase active rectifier, 20 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

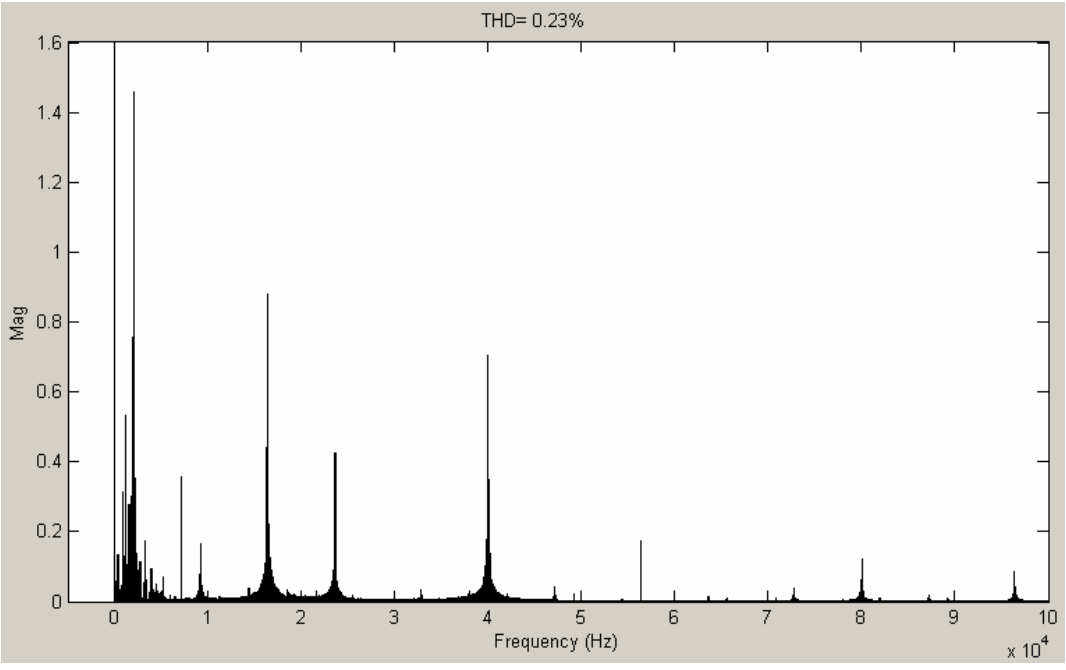


Fig. 19(f) – Dc-bus FFT plot of the three-phase active rectifier, 20 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

### 3.2 Six-Phase Wye-Connected Active Rectifier Model

The six-phase active rectifier model was constructed in the same way as the three-phase model, but utilizing three additional ac sources and a second Universal Bridge. Again, a symmetrical phase shift of 60° was used with an electrical frequency of 1.2 kHz. For comparison, resistance and inductance values identical to those calculated for the six-phase passive rectifier model were used, 12.0mΩ and 4.1μH respectively. The ac sources were given a peak phase voltage of 285.8V (350.0$V_{LL}$ rms). For the active rectifier design, IGBT switches and reverse connected diodes with series RC snubber circuits connected in parallel with each device were again utilized. Parameters of the switches were unchanged and include an on-resistance of 1.0mΩ, snubber resistance of 50Ω, and snubber capacitance of 250nF. Gating signals for the universal bridge are provided by the PWM Generator subsystem, which was modified from the three-phase design to accommodate the six-phase model. The Matlab Simulink schematic of the six-phase active rectifier model is shown in Fig. 20.

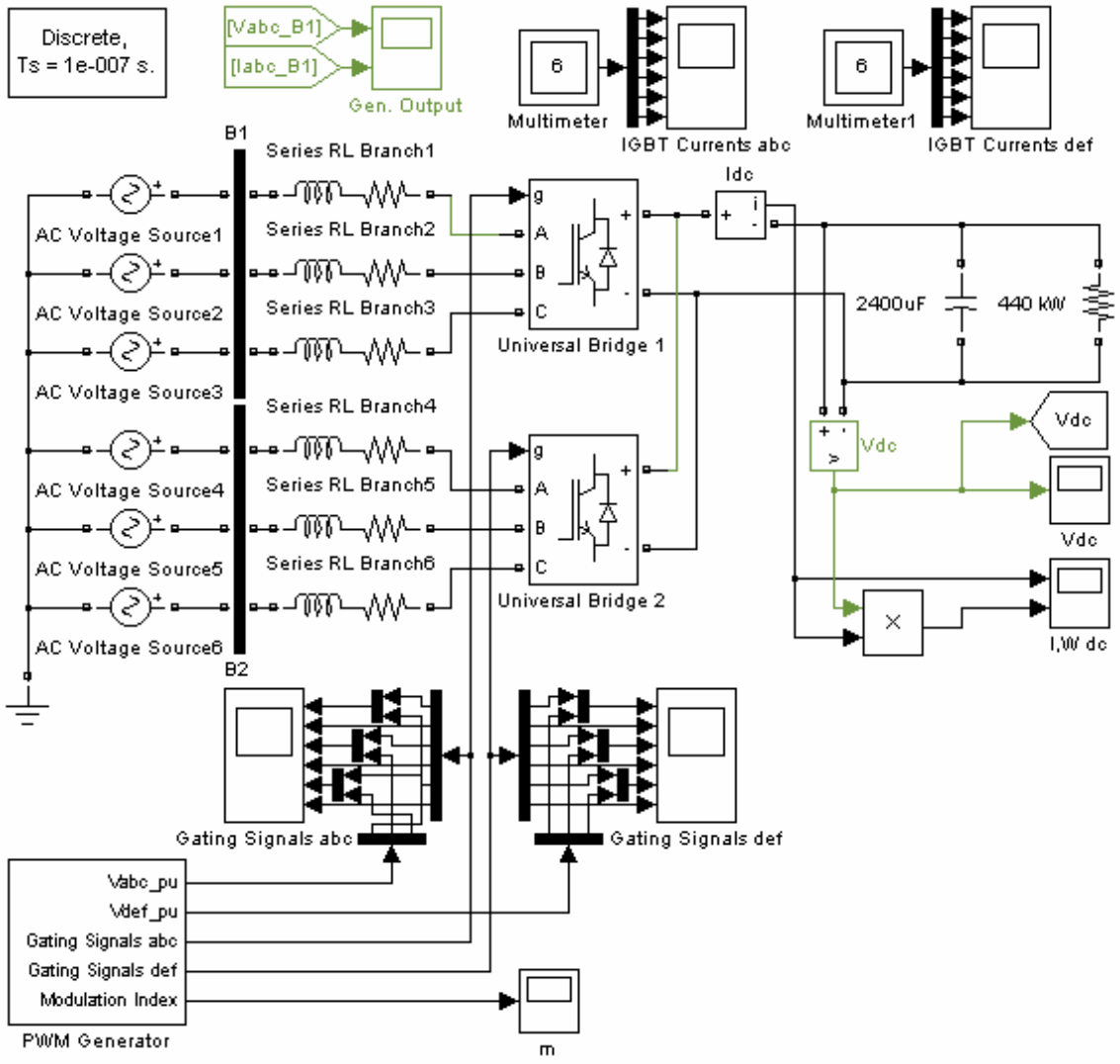


Fig. 20 – Six wye-connected ac sources with active rectifier.

### *3.2.1 Six-Phase Wye-Connected Active Rectifier Control*

Control of the six-phase active rectifier is identical to that of the three-phase model. In constructing the six-phase PWM controller, the three-phase controller was modified by adding a second set of voltage inputs for the additional three phases. A second set of sine-triangle comparators were added, which produce another gating signal output for the second Universal Bridge. The Matlab Simulink schematic of the six-phase PWM Generator is shown in Fig. 21.

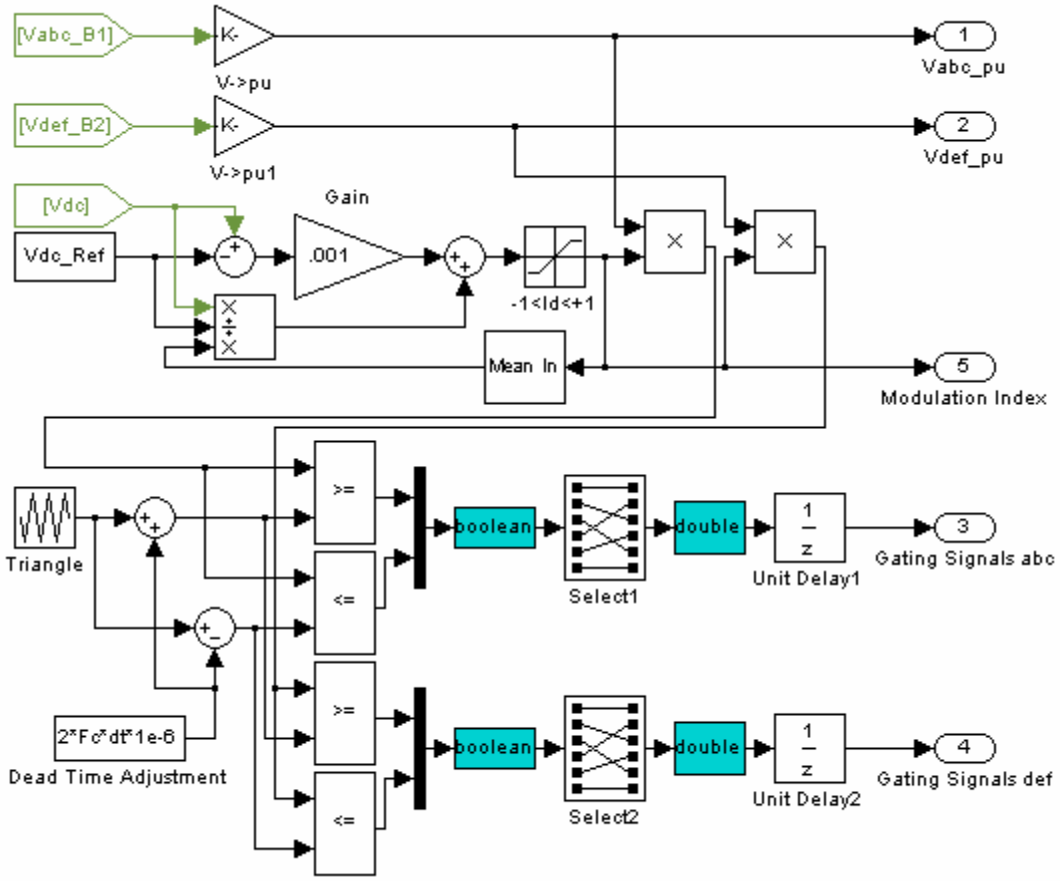


Fig. 21 – Six-phase wye-connected PWM Generator.

### *3.2.2 Six-Phase Wye-Connected Active Rectifier Results*

The six-phase active rectifier was simulated using the same set of carrier frequencies and dead times as the three-phase active rectifier; carrier frequencies of 10 kHz, 15 kHz, and 20 kHz with dead times of 2µs and 5µs. For comparison with the passive rectifier results, dc-bus voltage and rms current are provided for each case in Table 4.

Table 4 – Six-phase active rectifier results.

| **Carrier Frequency:** | **10 kHz** | | **15kHz** | | **20kHz** | |
|---|---|---|---|---|---|---|
| **Dead Time:** | **2µs** | **5µs** | **2µs** | **5µs** | **2µs** | **5µs** |
| DC-Bus Voltage (V): | 600.0 | 600.0 | 600.0 | 600.0 | 600.0 | 600.0 |
| RMS DC-Bus Current (A): | 879.4 | 847.6 | 821.8 | 809.3 | 801.7 | 802.0 |

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are shown in Fig. 22(a-l) for each carrier frequency and dead time case. Harmonic content for each case is given by the FFT plots in Fig. 23(a-f).

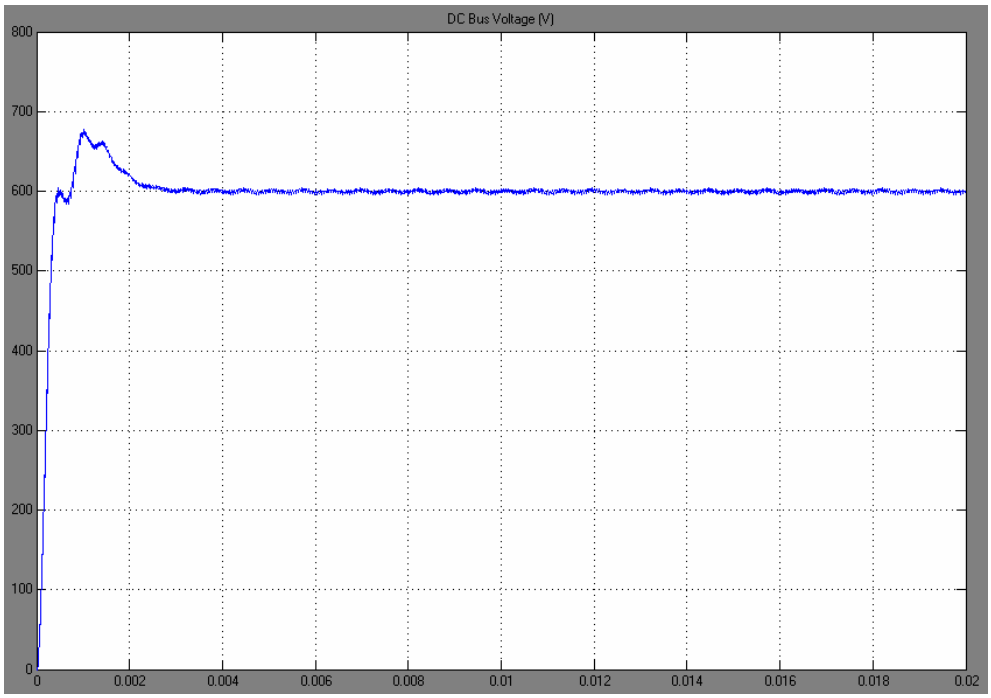


Fig. 22(a) – Dc-bus voltage waveform of the six-phase active rectifier, 10 kHz carrier frequency, 2µs dead time.

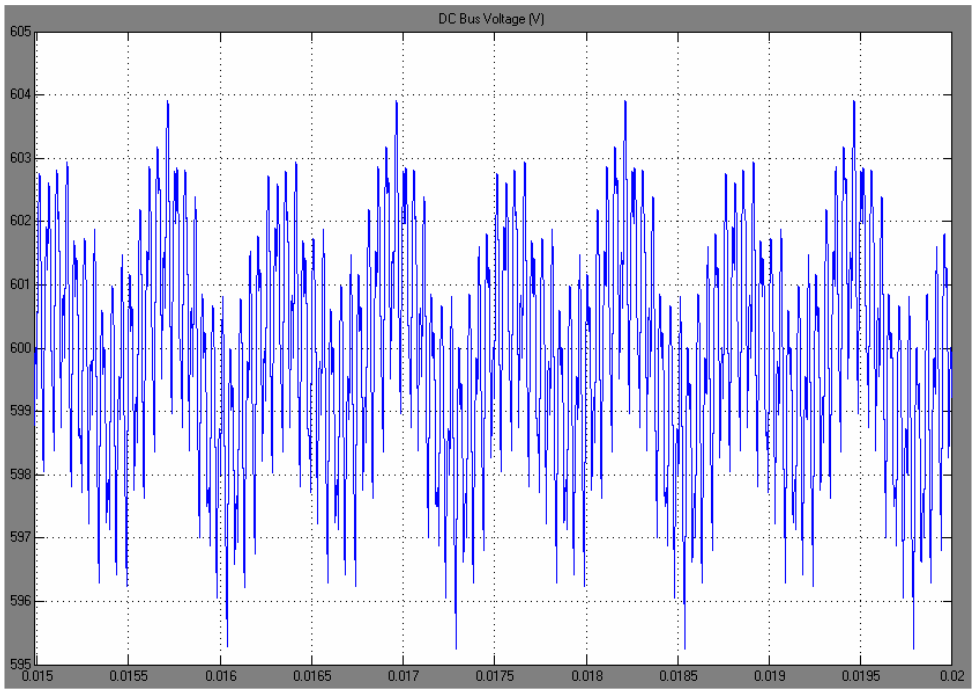


Fig. 22(b) – Dc-bus voltage ripple of the six-phase active rectifier, 10 kHz carrier frequency, 2µs dead time.

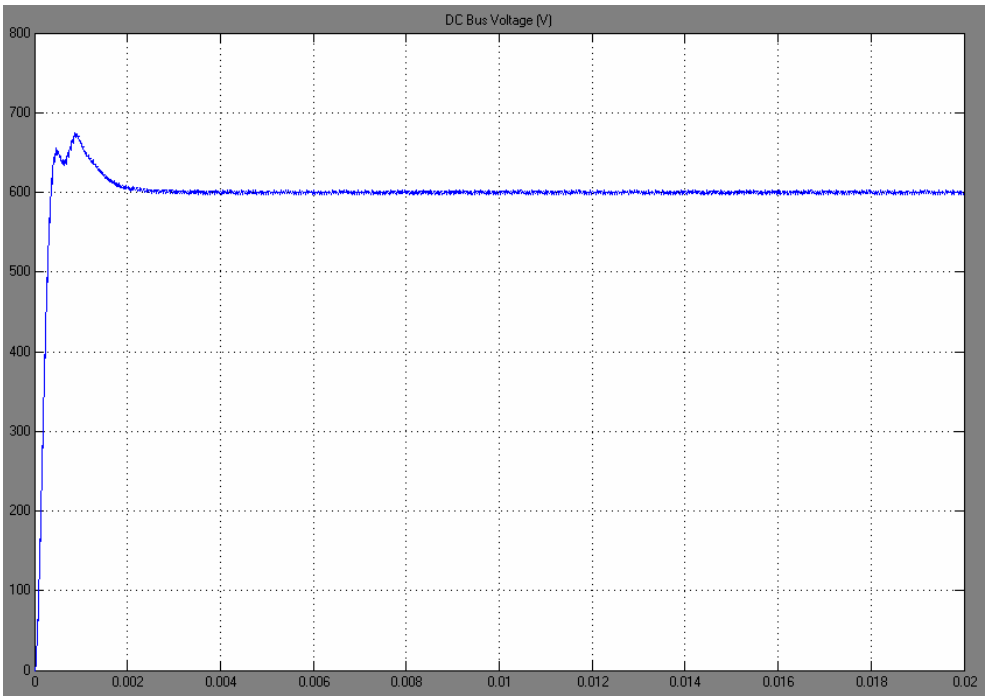


Fig. 22(c) – Dc-bus voltage waveform of the six-phase active rectifier, 10 kHz carrier frequency, 5µs dead time.

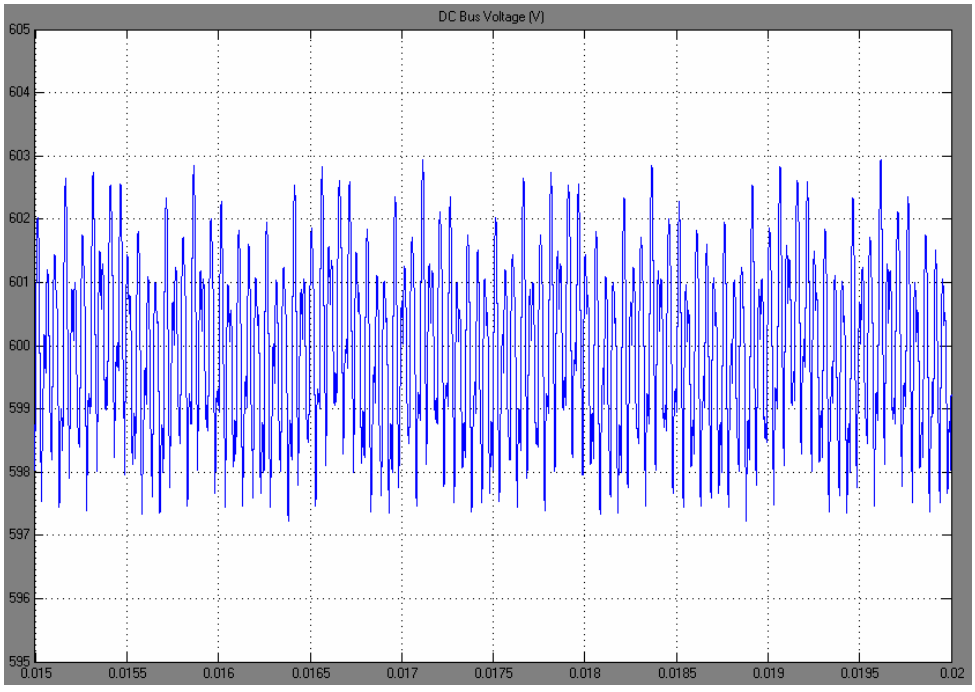


Fig. 22(d) – Dc-bus voltage ripple of the six-phase active rectifier, 10 kHz carrier frequency, 5µs dead time.

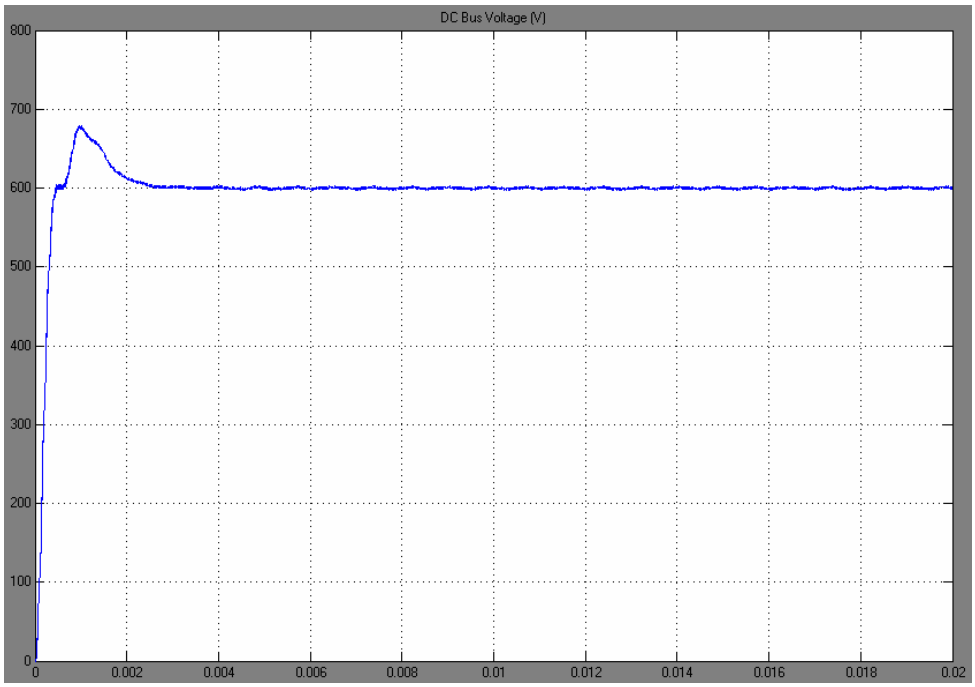


Fig. 22(e) – Dc-bus voltage waveform of the six-phase active rectifier, 15 kHz carrier frequency, 2µs dead time.

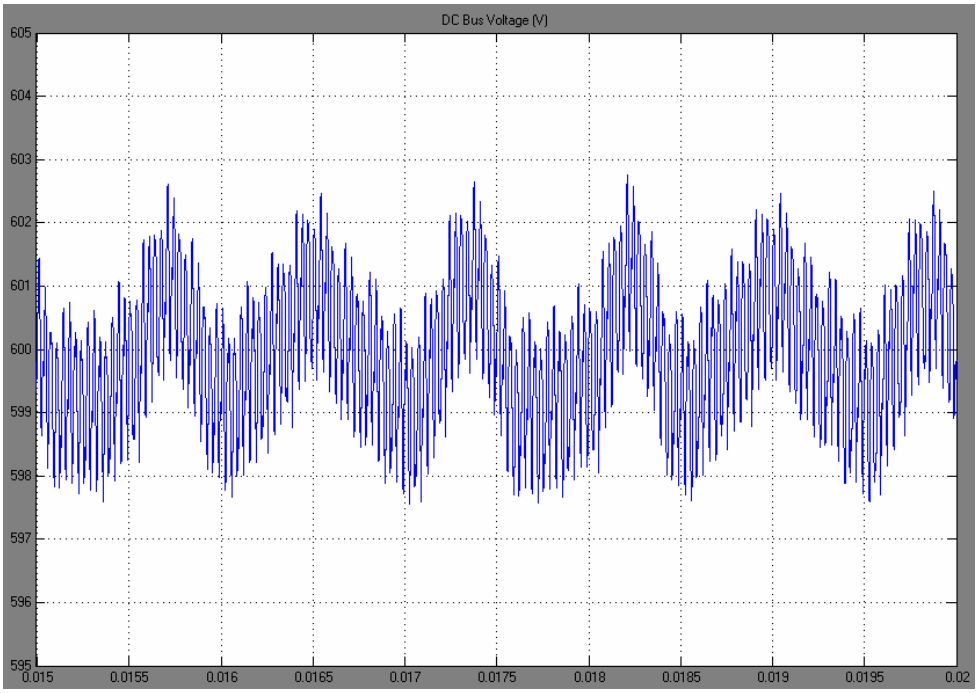


Fig. 22(f) – Dc-bus voltage ripple of the six-phase active rectifier, 15 kHz carrier frequency, 2µs dead time.

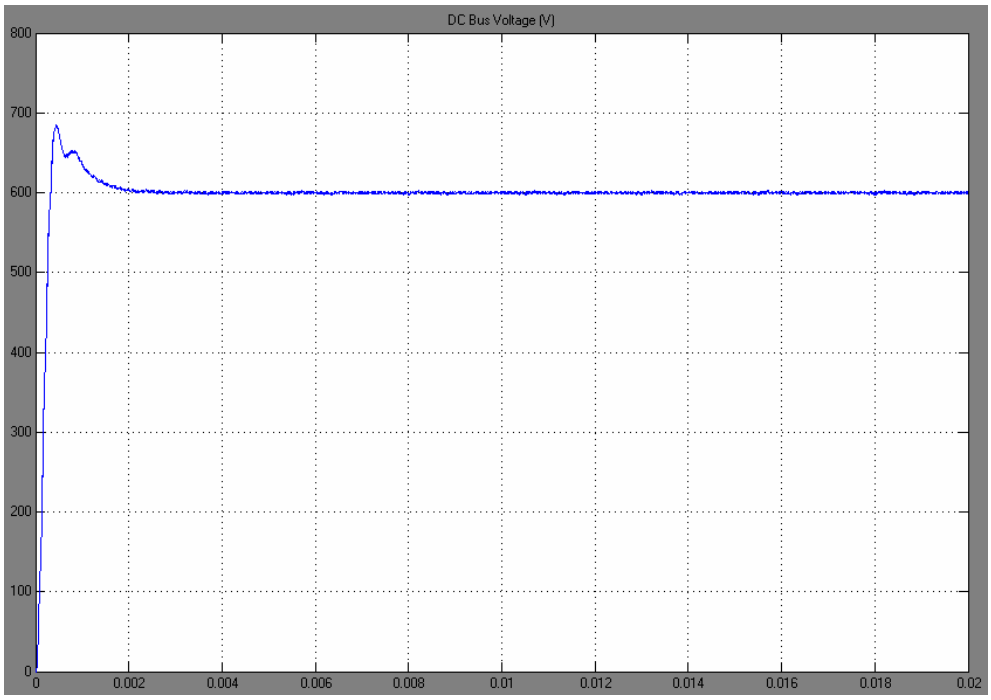


Fig. 22(g) – Dc-bus voltage waveform of the six-phase active rectifier,
15 kHz carrier frequency, 5µs dead time.

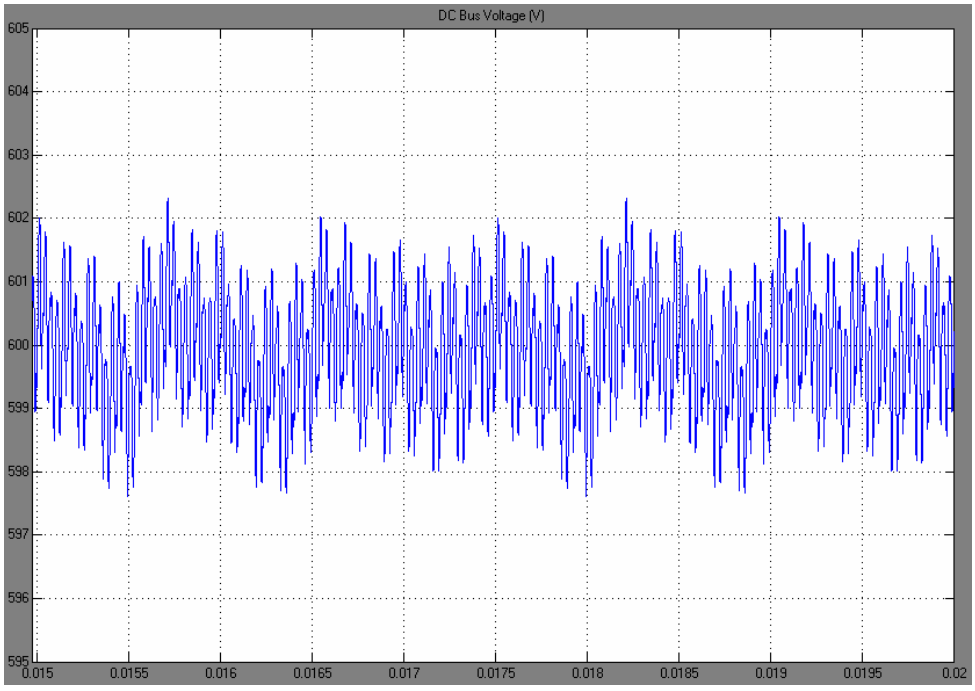


Fig. 22(h) – Dc-bus voltage ripple of the six-phase active rectifier,
15 kHz carrier frequency, 5µs dead time.

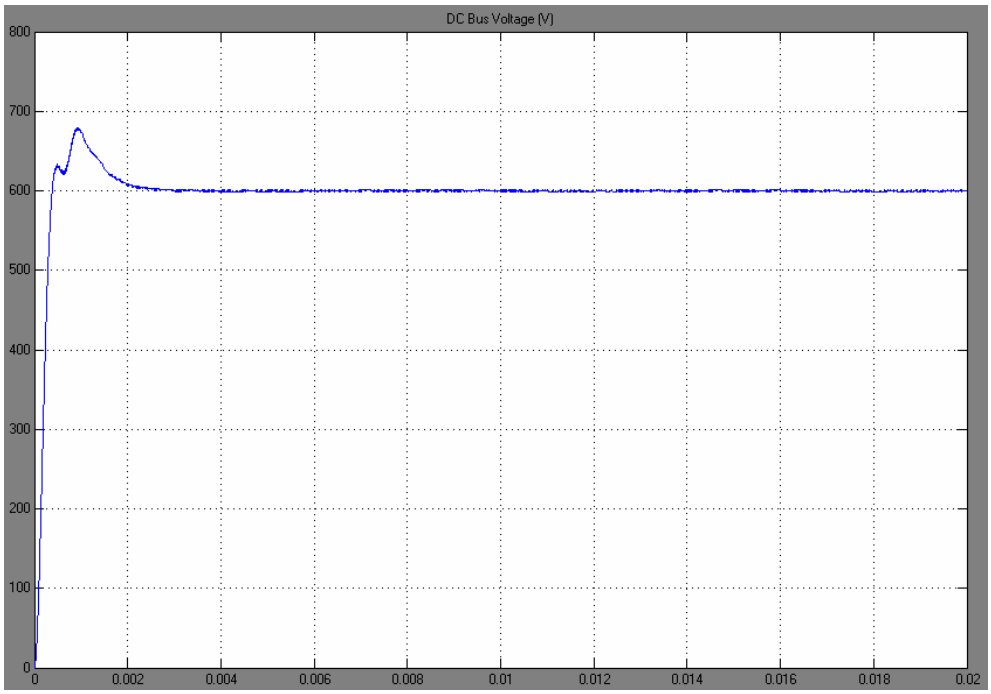


Fig. 22(i) – Dc-bus voltage waveform of the six-phase active rectifier, 20 kHz carrier frequency, 2µs dead time.

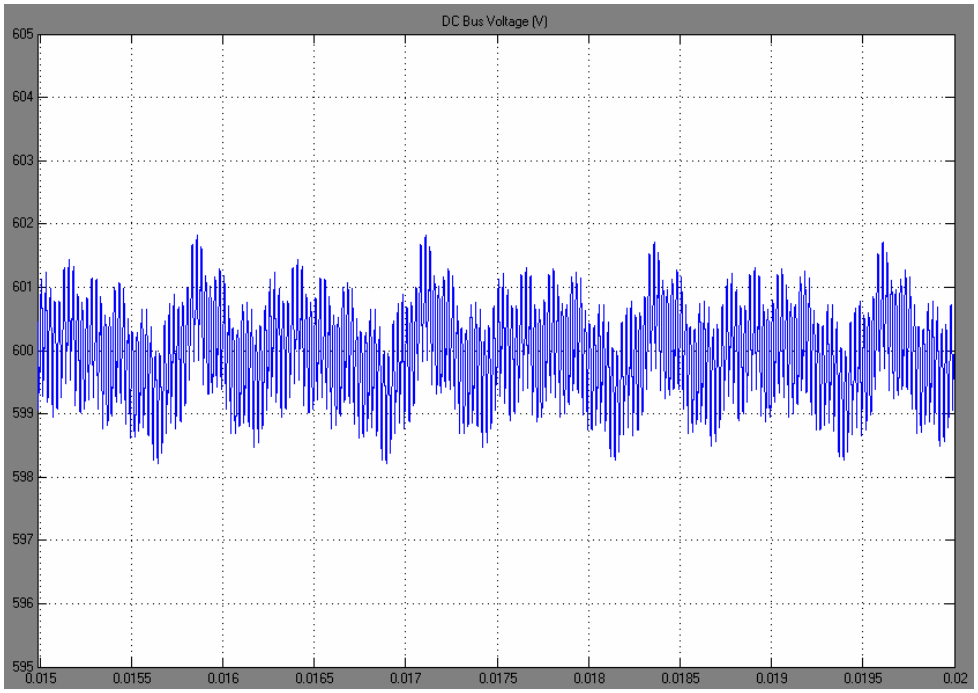


Fig. 22(j) – Dc-bus voltage ripple of the six-phase active rectifier, 20 kHz carrier frequency, 2µs dead time.

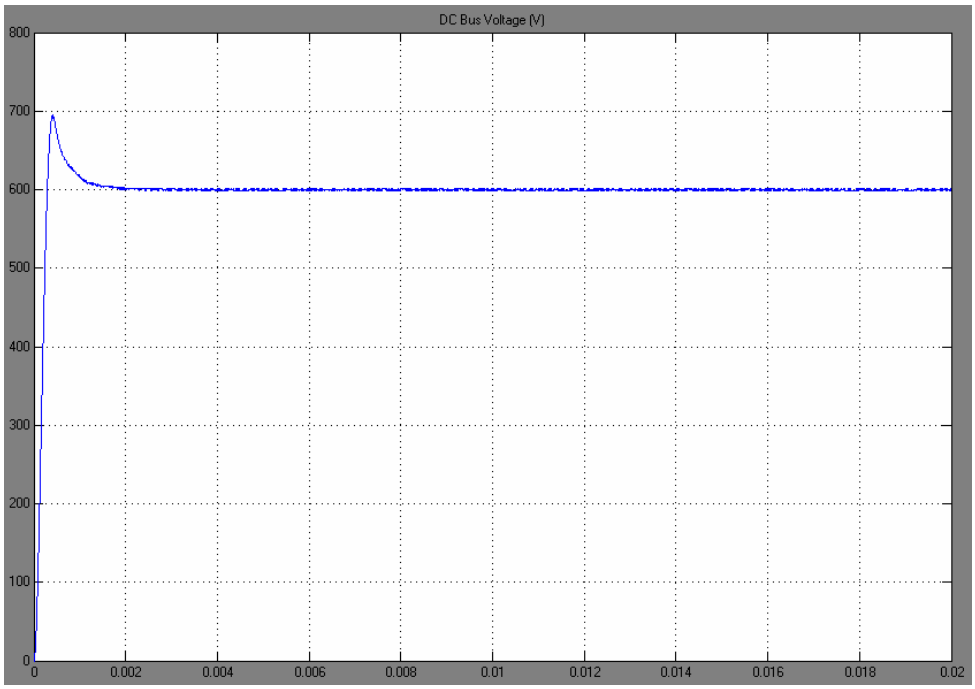


Fig. 22(k) – Dc-bus voltage waveform of the six-phase active rectifier, 20 kHz carrier frequency, 5µs dead time.

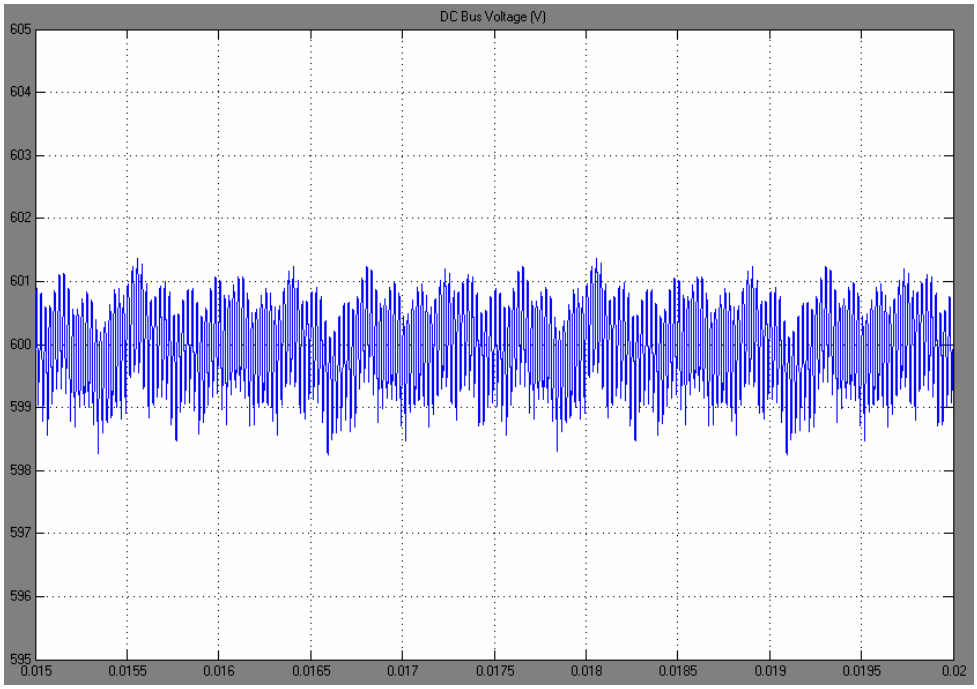


Fig. 22(l) – Dc-bus voltage ripple of the six-phase active rectifier, 20 kHz carrier frequency, 5µs dead time.

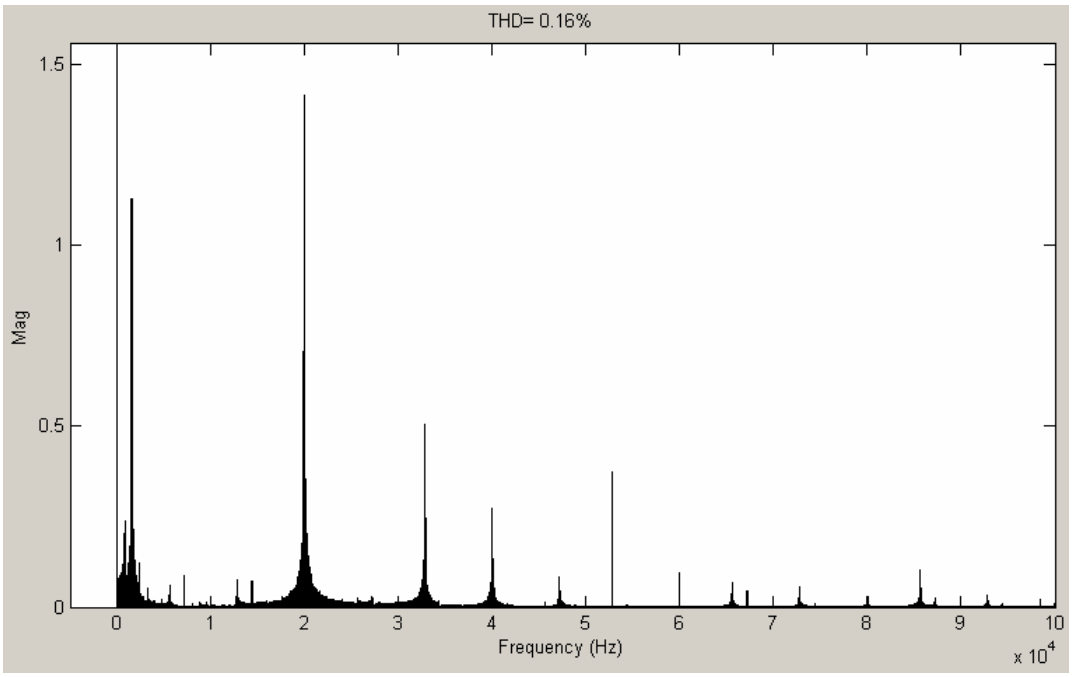


Fig. 23(a) – Dc-bus voltage FFT plot of the six-phase active rectifier, 10 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

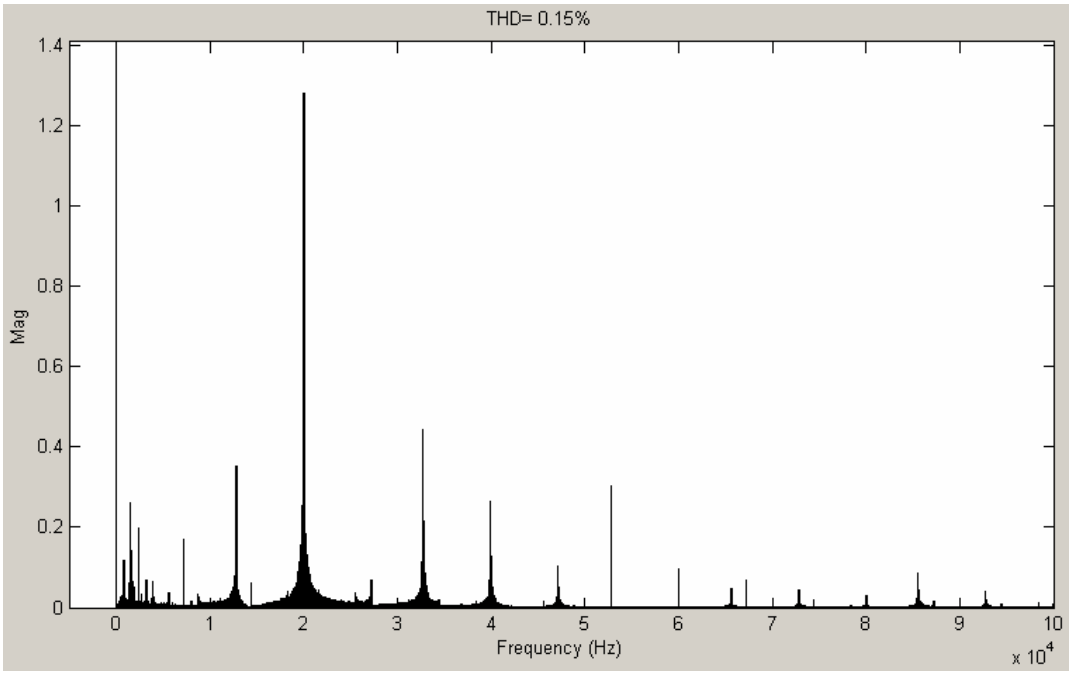


Fig. 23(b) – Dc-bus FFT plot of the six-phase active rectifier, 10 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

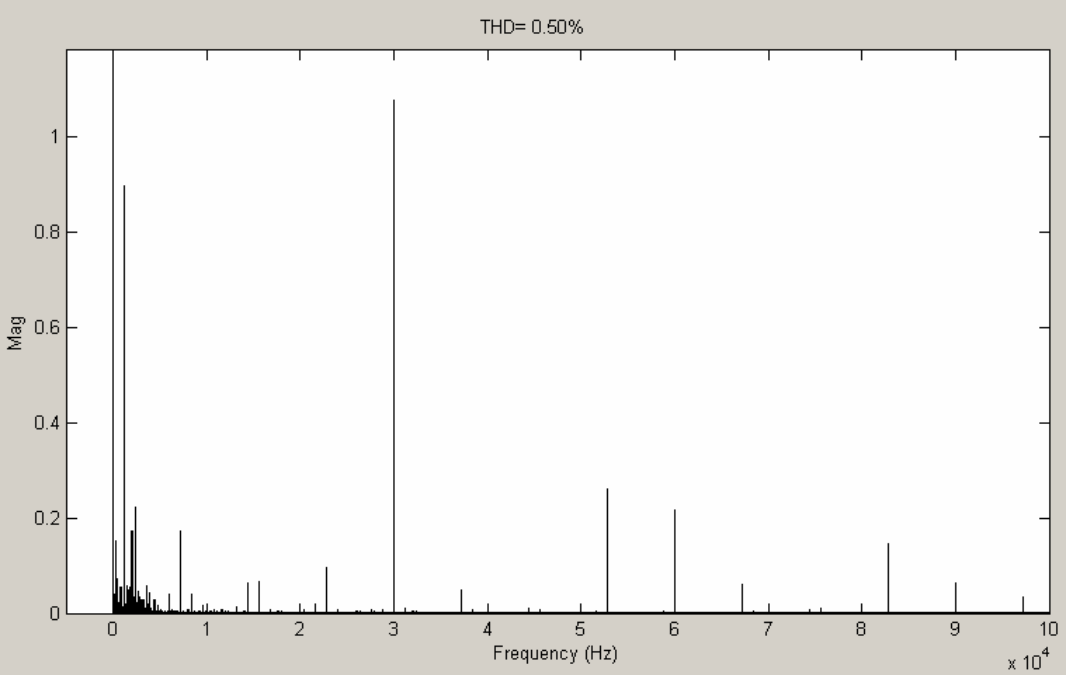


Fig. 23(c) – Dc-bus FFT plot of the six-phase active rectifier, 15 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

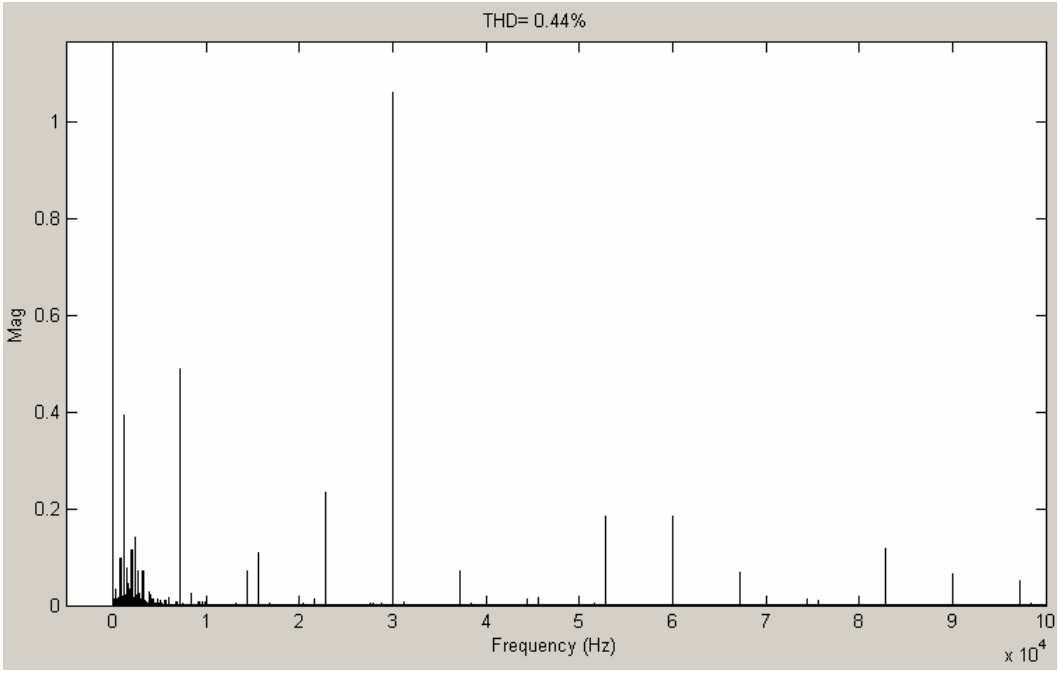


Fig. 23(d) – Dc-bus FFT plot of the six-phase active rectifier, 15 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

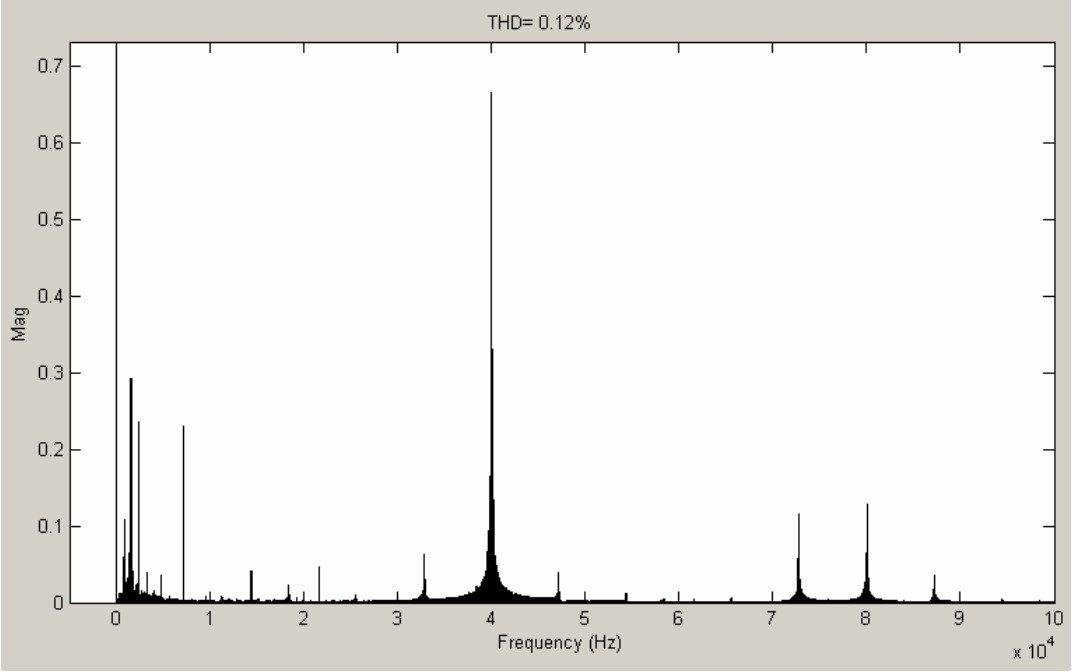


Fig. 23(e) – Dc-bus FFT plot of the six-phase active rectifier, 20 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

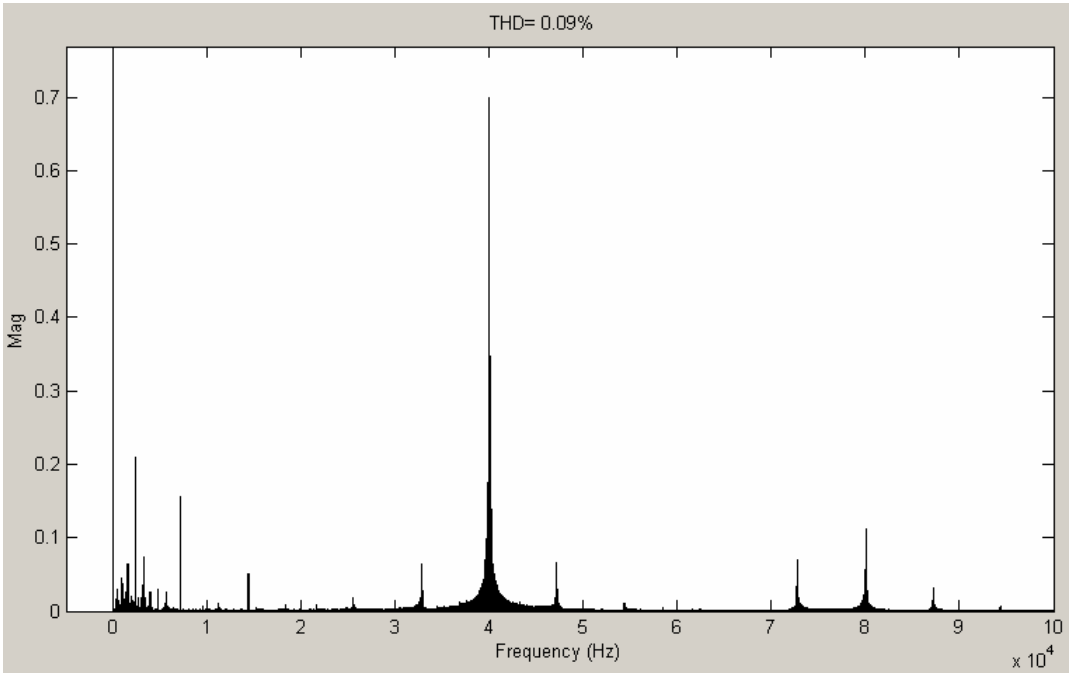


Fig. 23(f) – Dc-bus FFT plot of the six-phase active rectifier, 20 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

### 3.3 Six-Phase Independent Active Rectifier Model

The six-phase independent active rectifier model was constructed using six ac sources with series resistance and impedance, contained in a subsystem for each phase. Each source is connected to a single phase Universal Bridge, modeling a full wave H-bridge active rectifier. Each rectifier contains four IGBT devices; subsequently the PWM Generator produces four gating signals for each bridge. The outputs of the six rectifiers were then connected in parallel to form the dc-bus. The ac sources were set to a peak phase voltage of 495V (350V rms). Resistance and inductance values identical to those calculated for the passive rectifier case were used, 49mΩ and 16.0μH respectively. The Matlab Simulink schematic for this model is shown in Fig. 24.

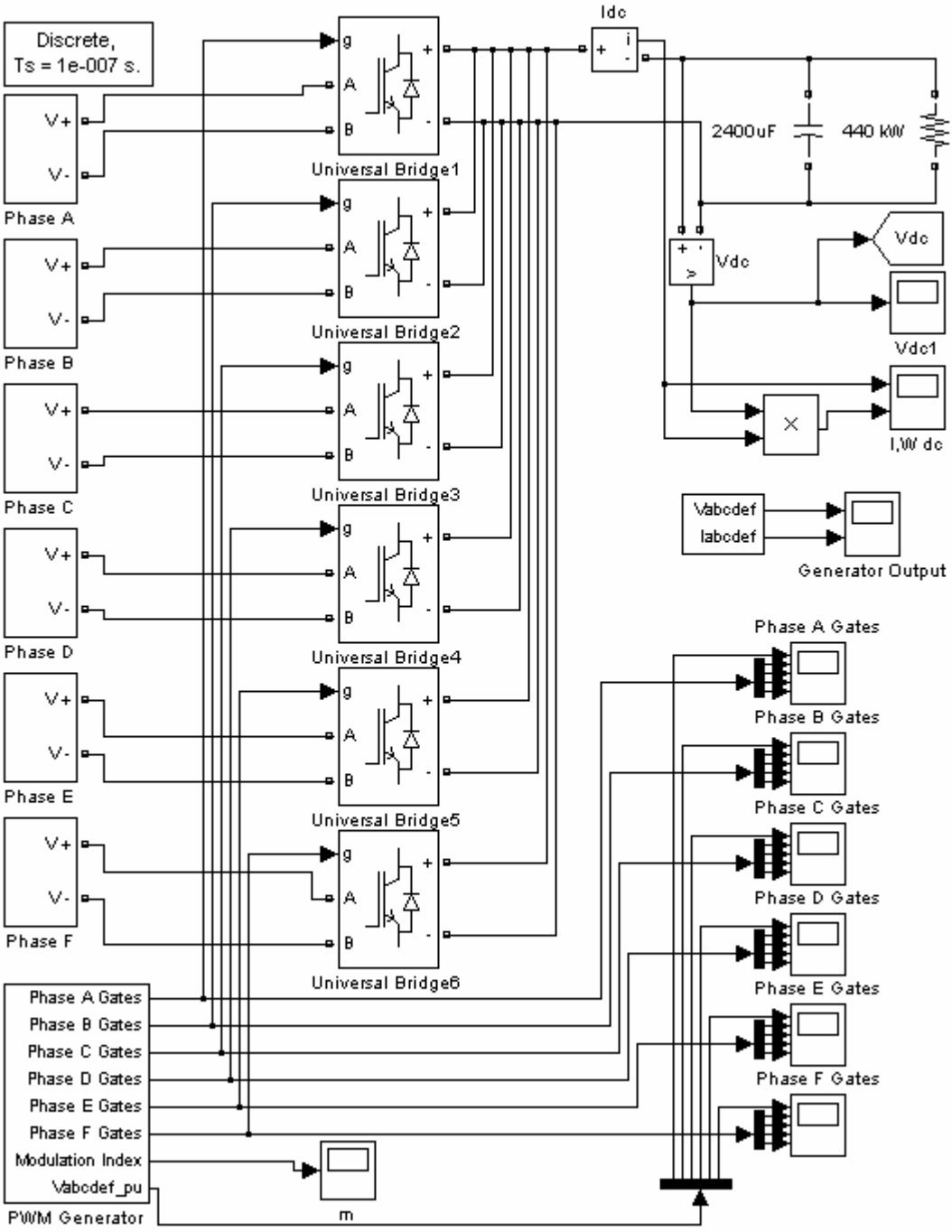


Fig. 24 – Six-phase independent active rectifier.

### *3.3.1 Six-Phase Independent Active Rectifier Control*

The PWM generator in the six-phase independent model operates very similarly to that of the three and six-phase wye-connected models. Modulation is controlled using the same method with an alteration to only the sine-triangle comparison. An offset between the switching times of one half period of the carrier frequency is used to keep a conducting pair from switching at the same instance; this works to reduce input current harmonics at the switching frequency. The Matlab Simulink schematic of the six-phase independent winding PWM Generator is shown in Fig. 25.

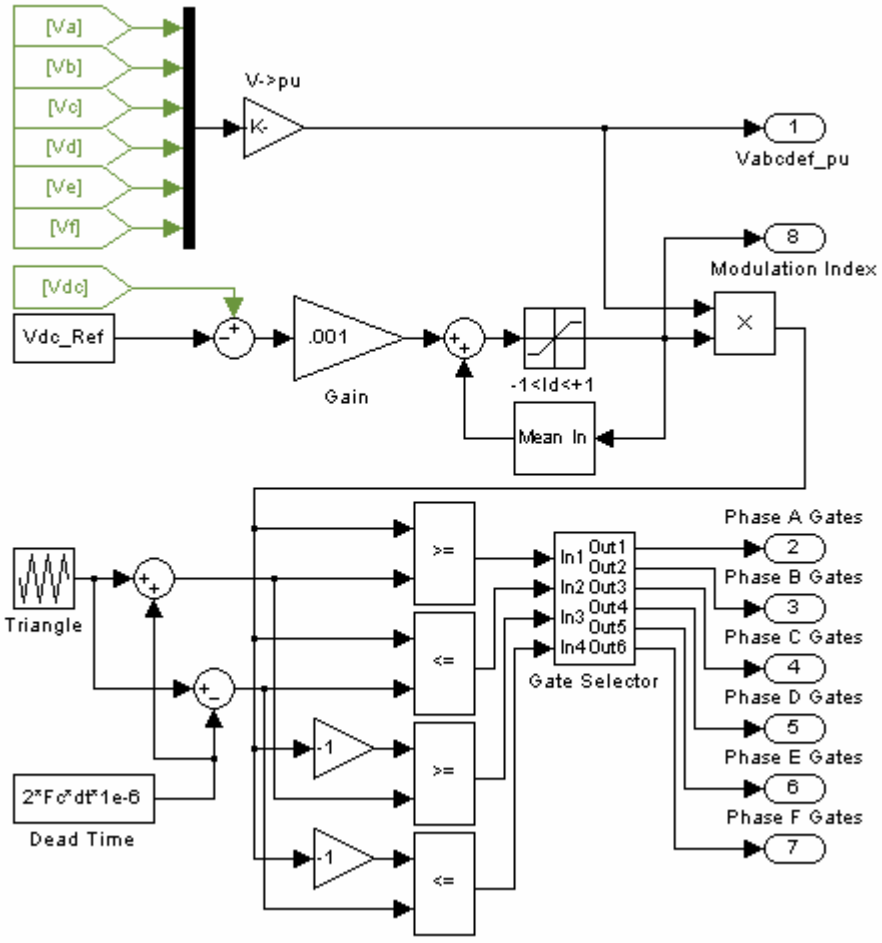


Fig. 25 – PWM Generator for the six-phase independent active rectifier.

### *3.3.2 Six-Phase Independent Active Rectifier Results*

The six-phase independent active rectifier was simulated using the same carrier frequencies and dead times as the three and six-phase wye-connected active rectifiers. Carrier frequencies of 10 kHz, 15 kHz, and 20 kHz were simulated using dead times of 2µs and 5µs. For comparison with the passive rectifier results, dc-bus voltage and rms current are provided for each case in Table 5.

Table 5 – Six-phase independent windings active rectifier results.

| **Carrier Frequency:** | **10 kHz** | | **15kHz** | | **20kHz** | |
|---|---|---|---|---|---|---|
| **Dead Time:** | **2µs** | **5µs** | **2µs** | **5µs** | **2µs** | **5µs** |
| DC-Bus Voltage (V): | 599.9 | 600.0 | 600.0 | 600.0 | 600.0 | 600.0 |
| RMS DC-Bus Current (A): | 965.6 | 944.3 | 912.9 | 915.2 | 903.2 | 903.4 |

Plots of dc-bus voltage and detailed ripple plots for the simulated time period are shown in Fig. 26(a-l) for each carrier frequency and dead time case. Harmonic content for each case is given by the FFT plots in Fig. 27(a-f).

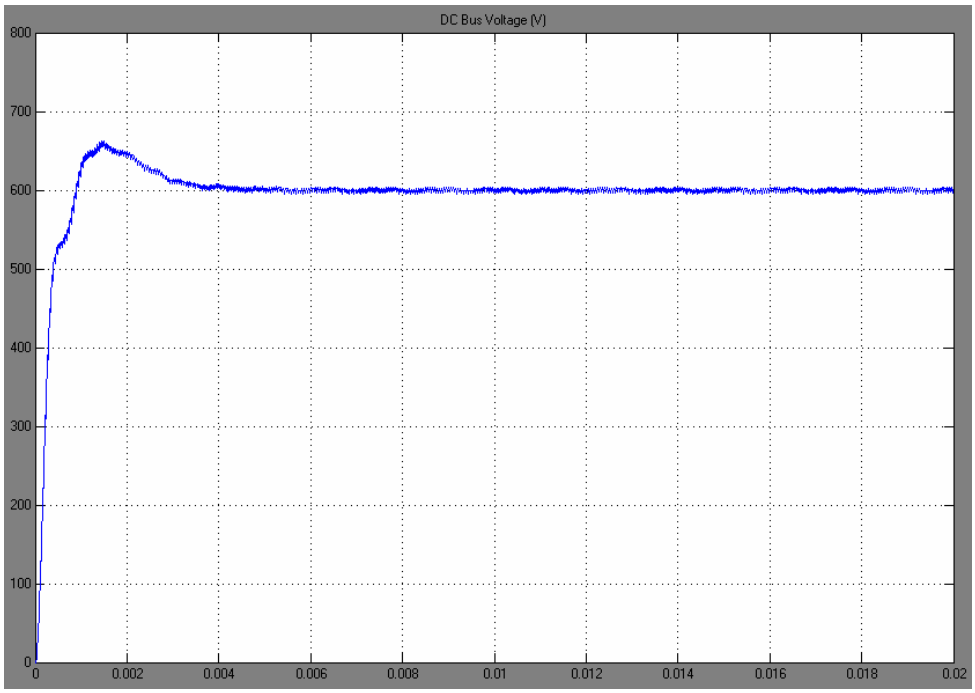


Fig. 26(a) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 2µs dead time.

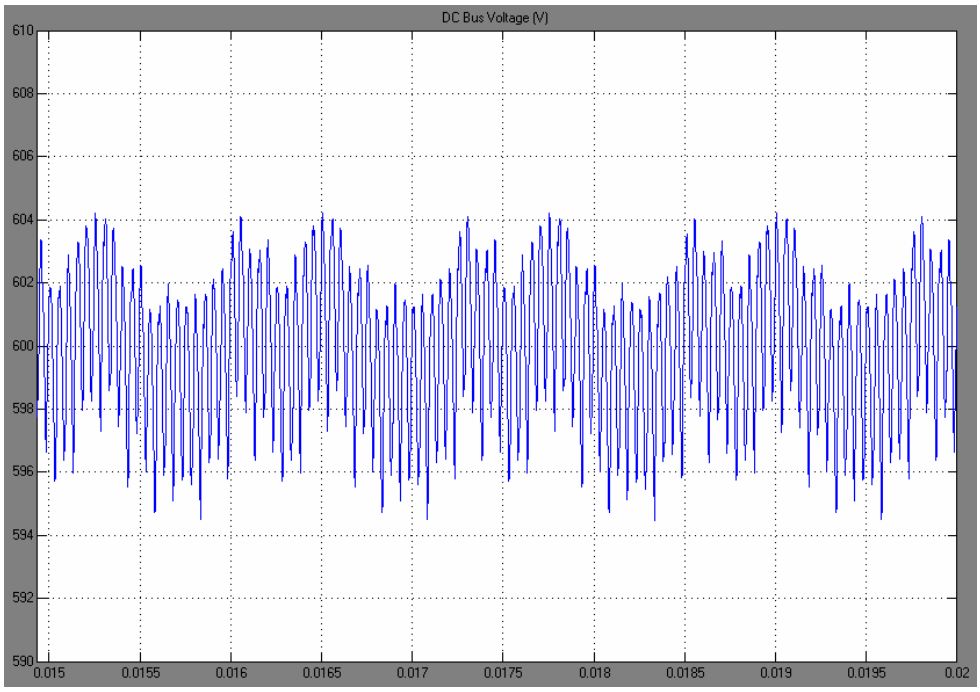


Fig. 26(b) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 2µs dead time.

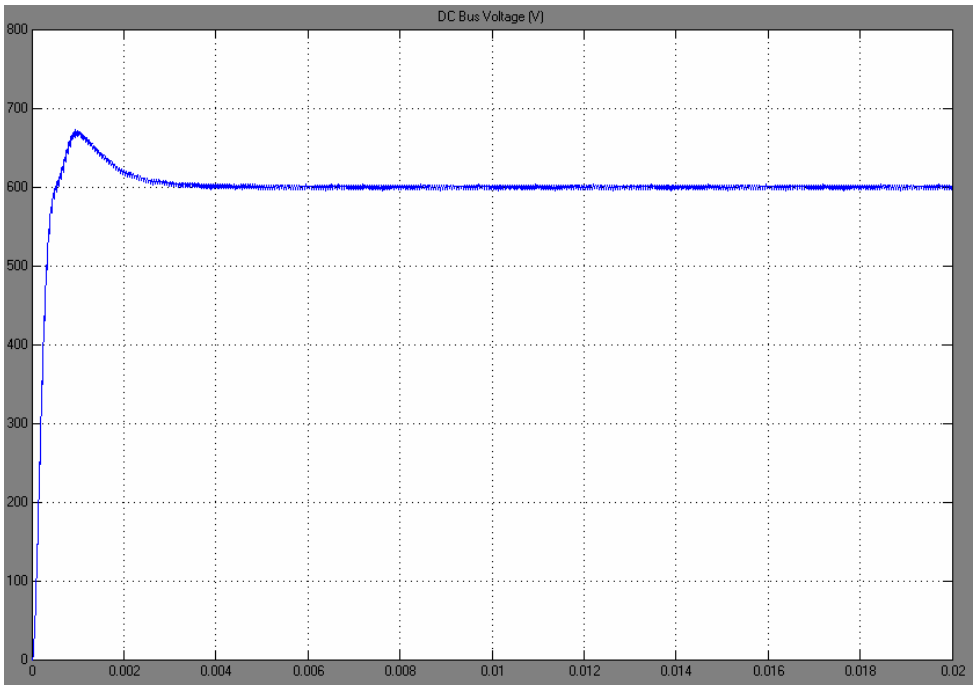


Fig. 26(c) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 5µs dead time.

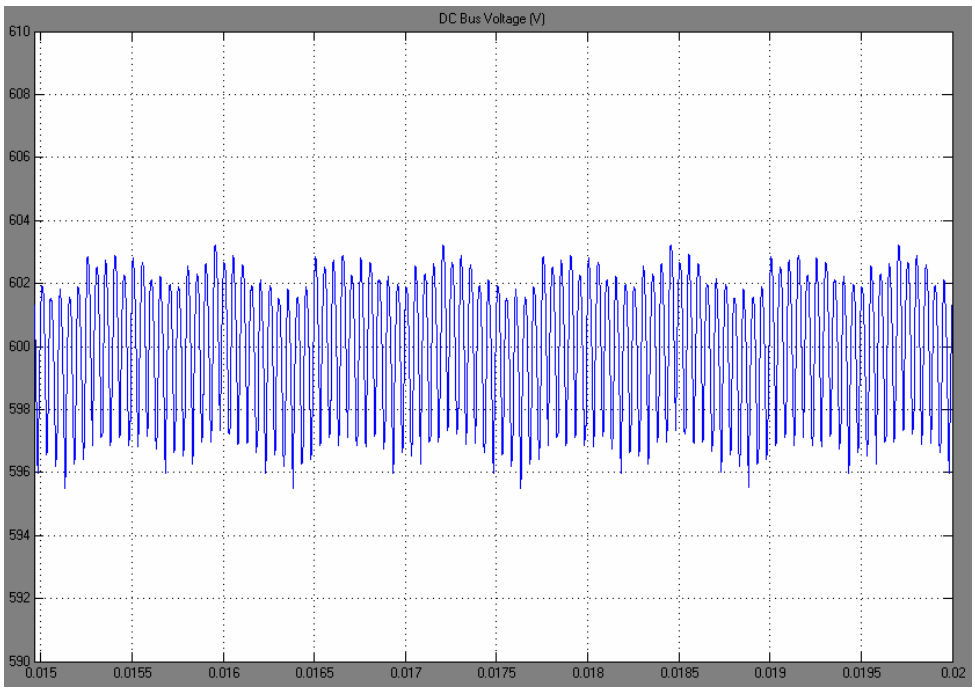


Fig. 26(d) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 5µs dead time.

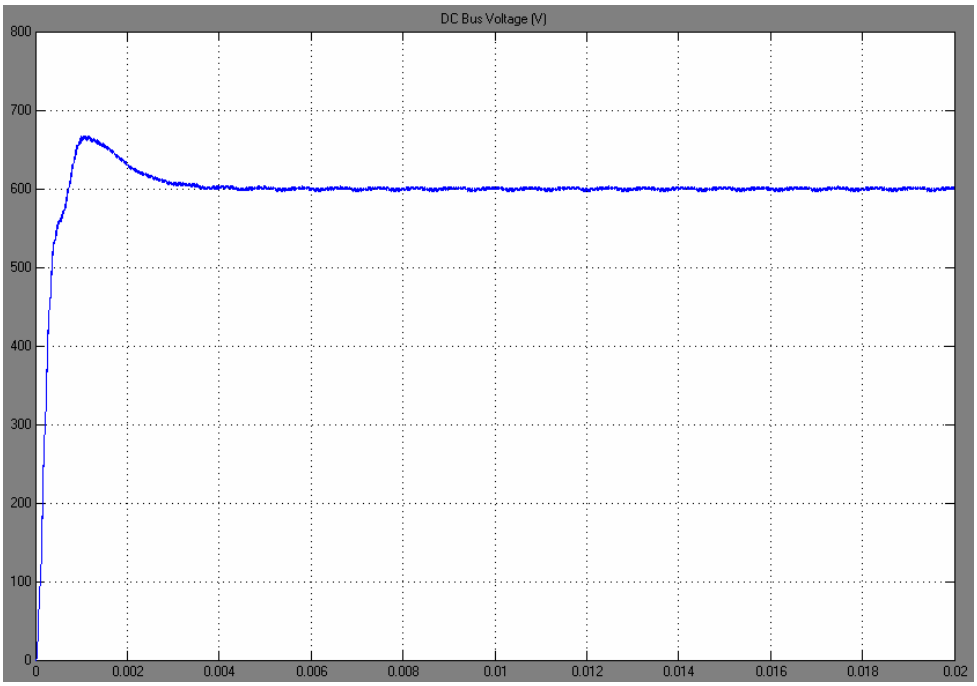


Fig. 26(e) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 2µs dead time.

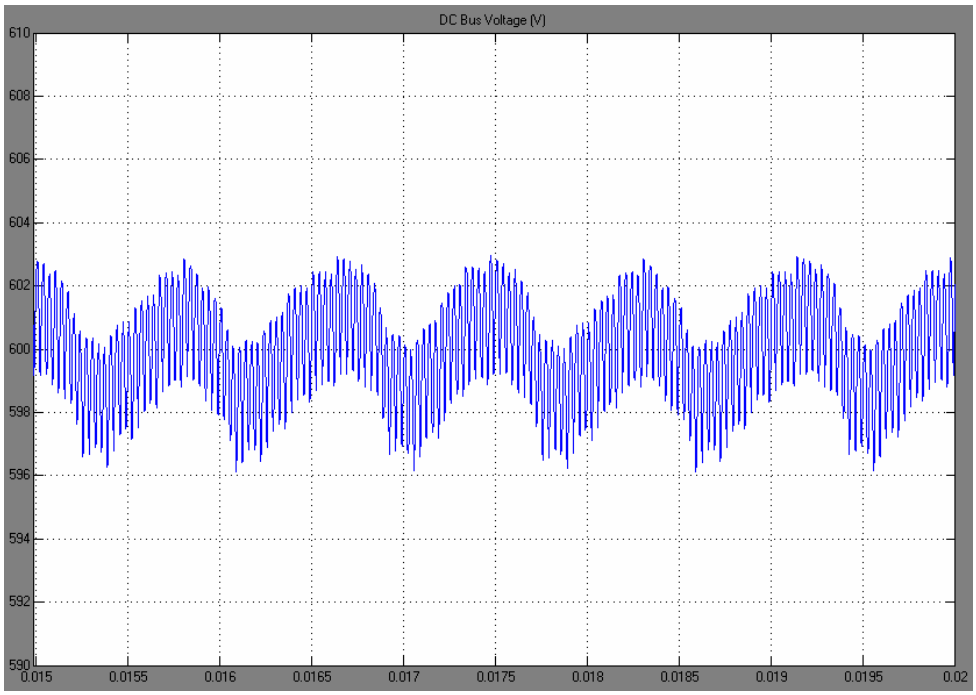


Fig. 26(f) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 2µs dead time.

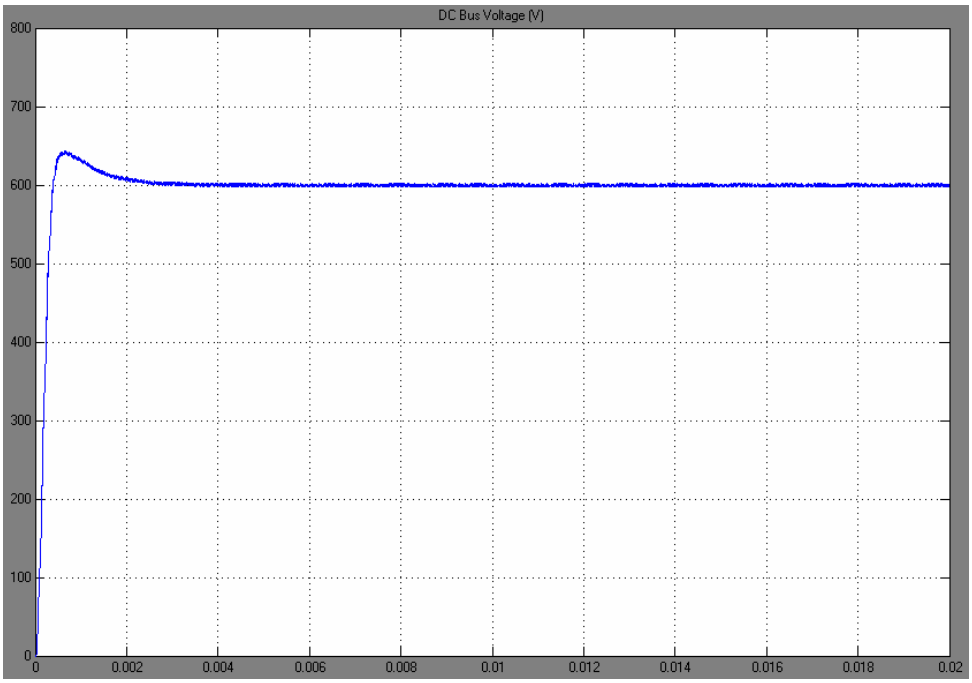


Fig. 26(g) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 5µs dead time.

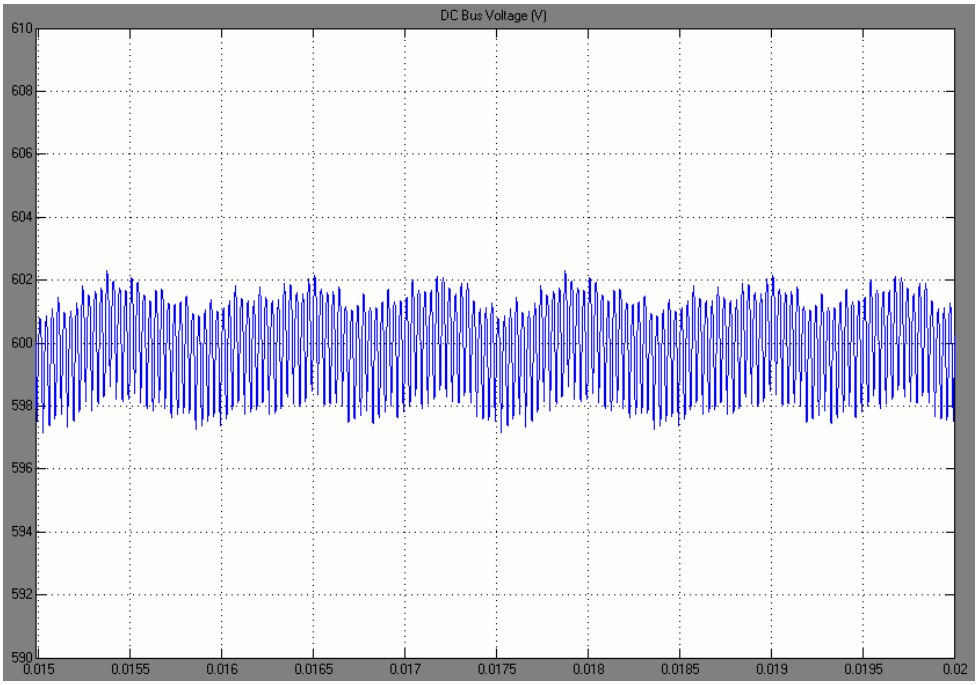


Fig. 26(h) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 5µs dead time.

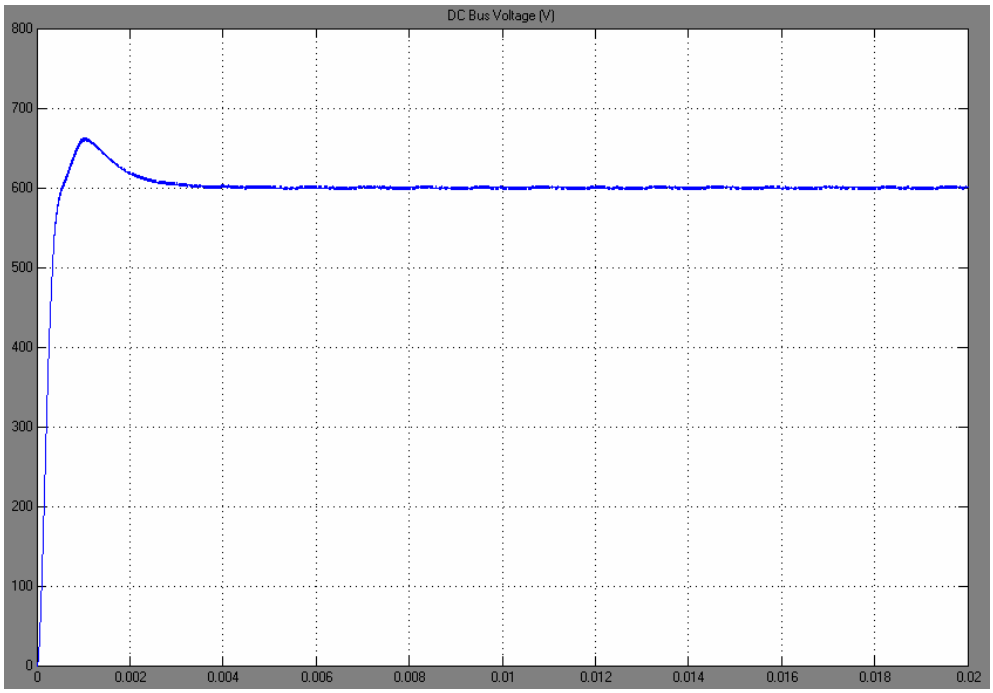


Fig. 26(i) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 2µs dead time.

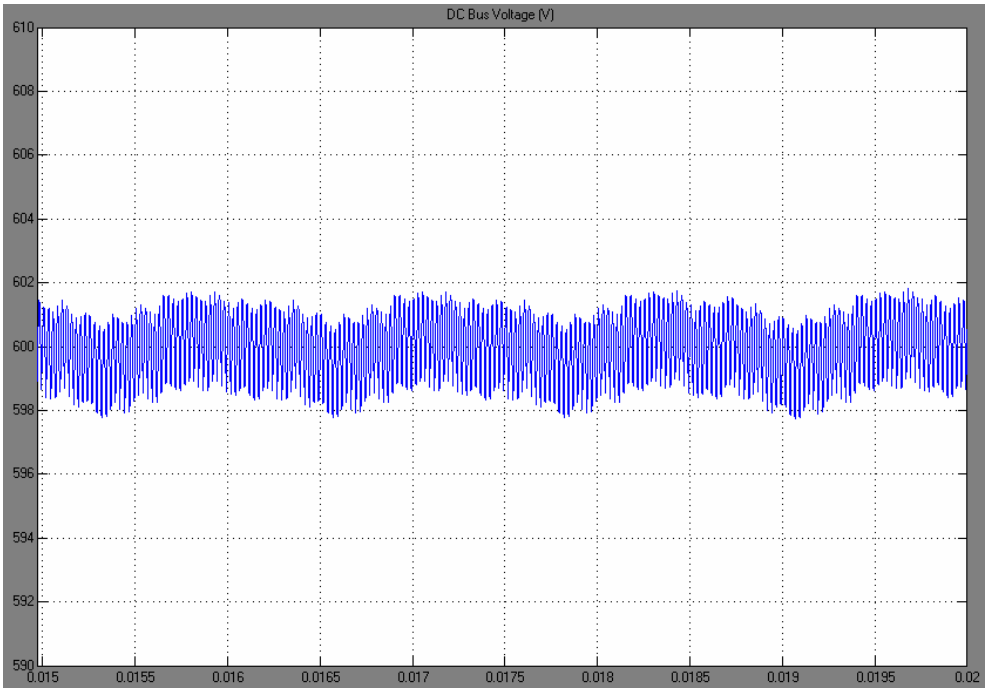


Fig. 26(j) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 2µs dead time.

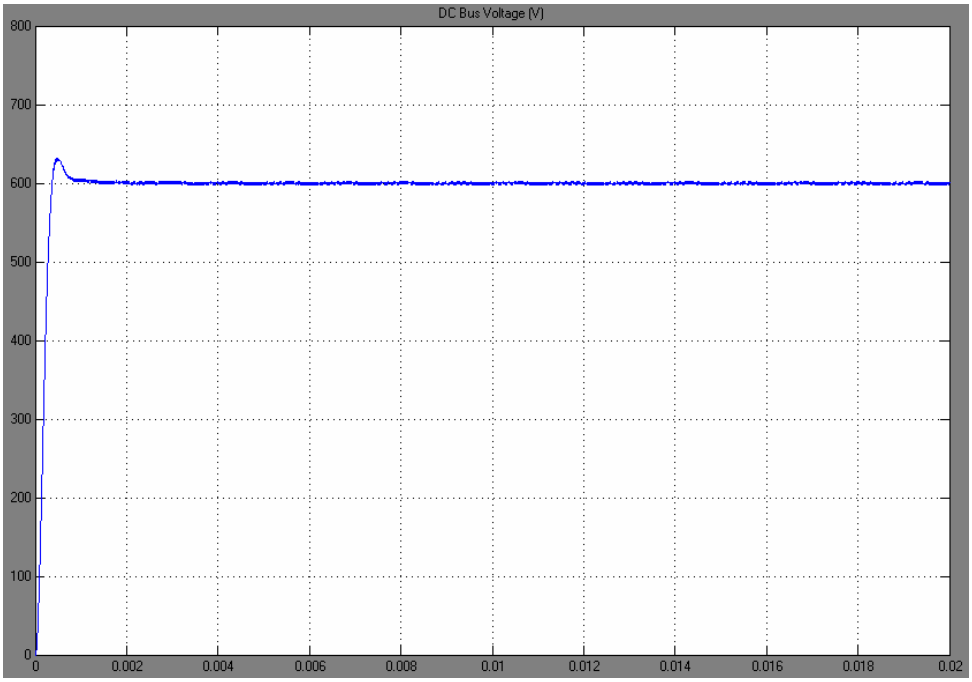


Fig. 26(k) – Dc-bus voltage waveform of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 5µs dead time.

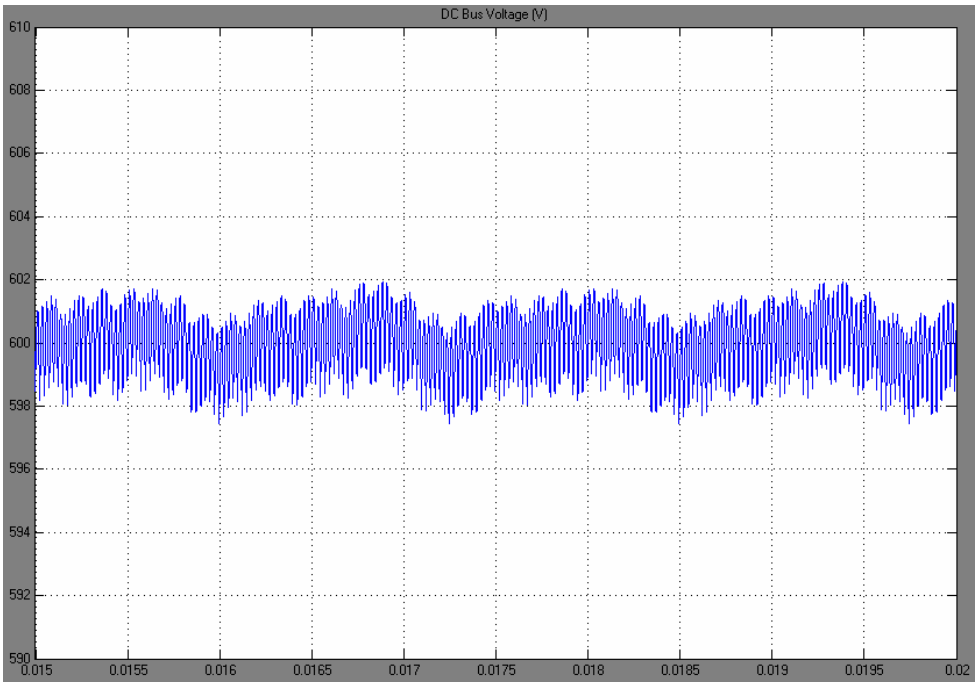


Fig. 26(l) – Dc-bus voltage ripple of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 5µs dead time.

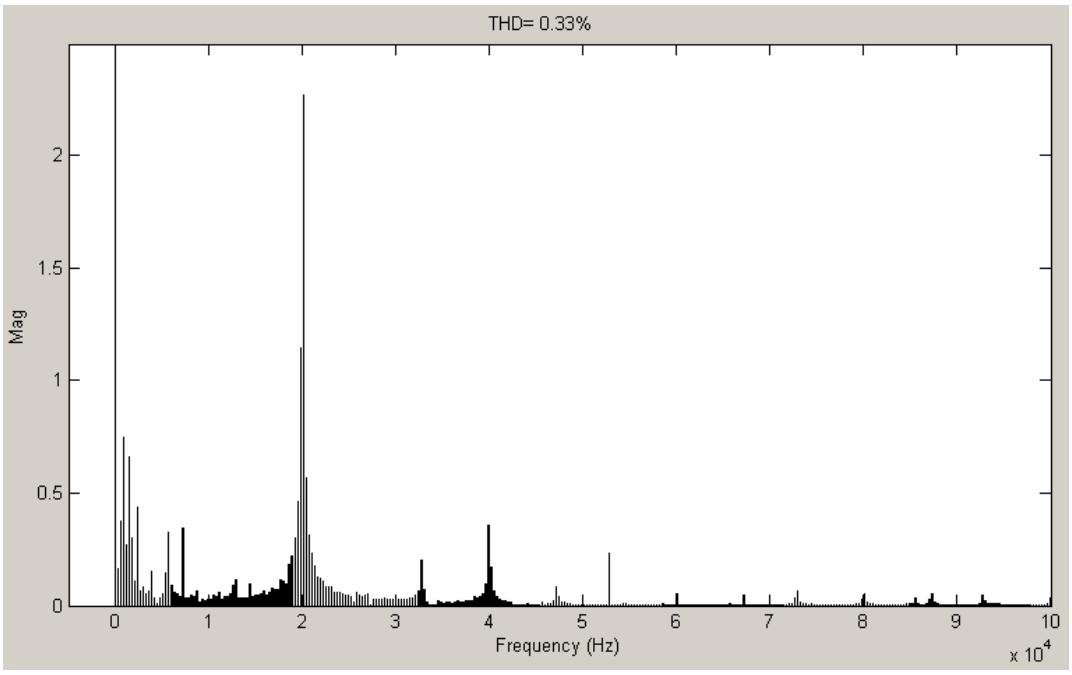


Fig. 27(a) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 2µs dead time, dc fundamental is 599.9V.

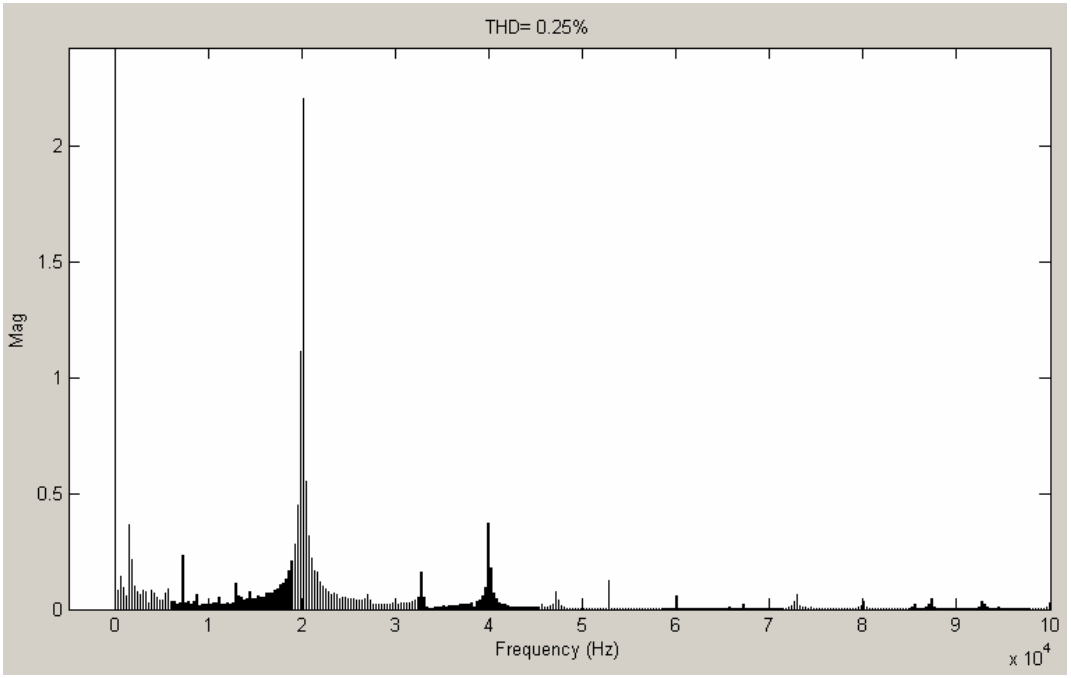


Fig. 27(b) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 10 kHz carrier frequency, 5µs dead time, dc fundamental is 600.0V.

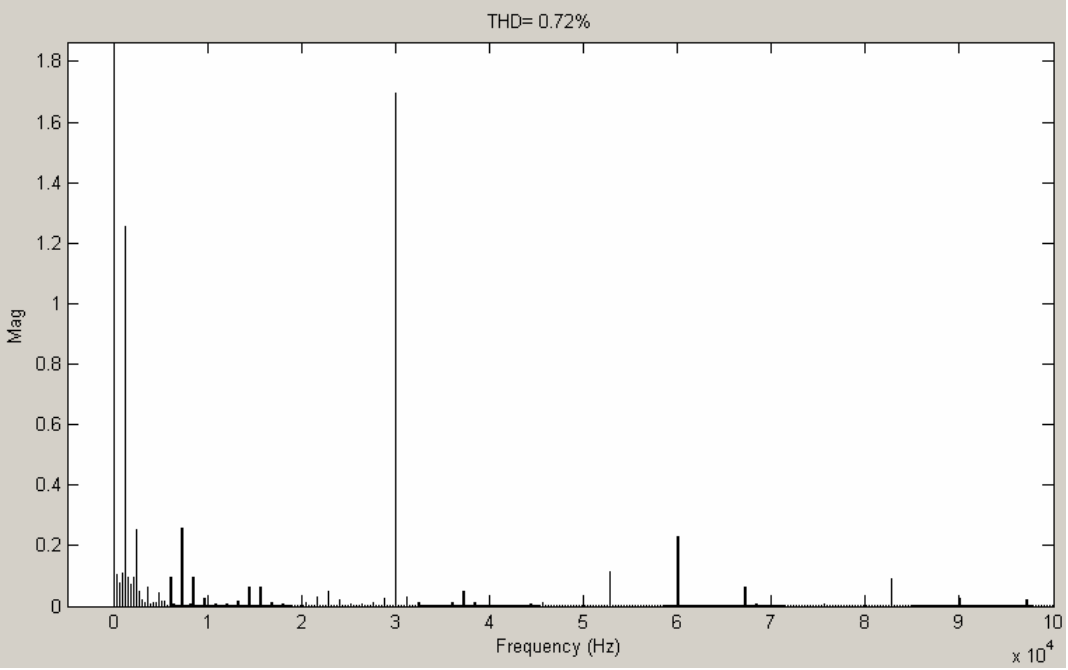


Fig. 27(c) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 2μs dead time, dc fundamental is 600.0V.

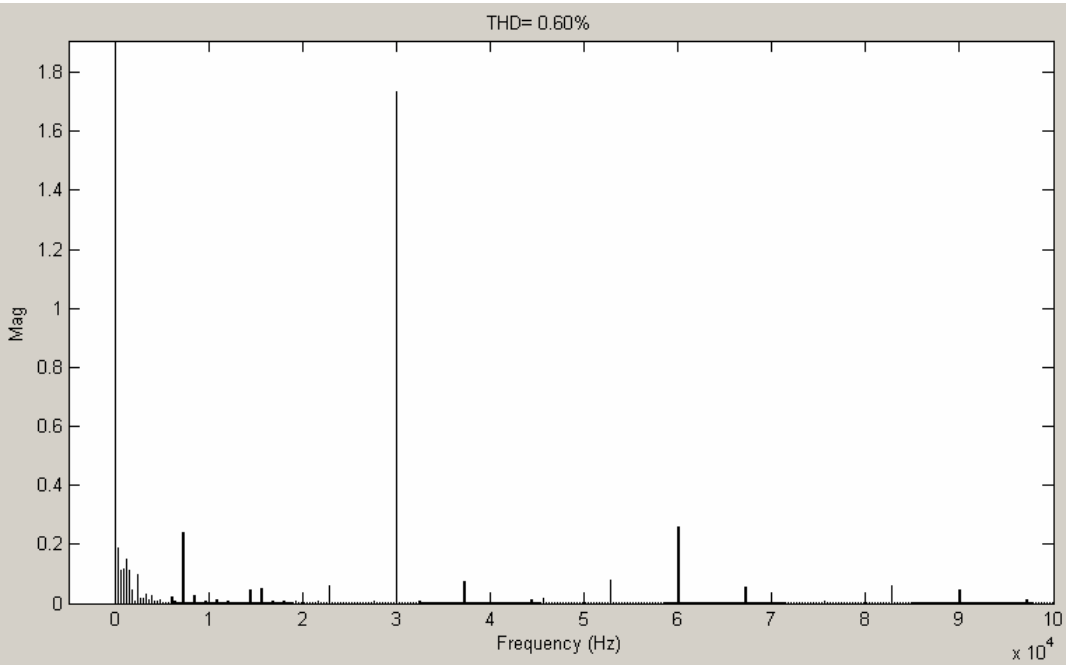


Fig. 27(d) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 15 kHz carrier frequency, 5μs dead time, dc fundamental is 600.0V.

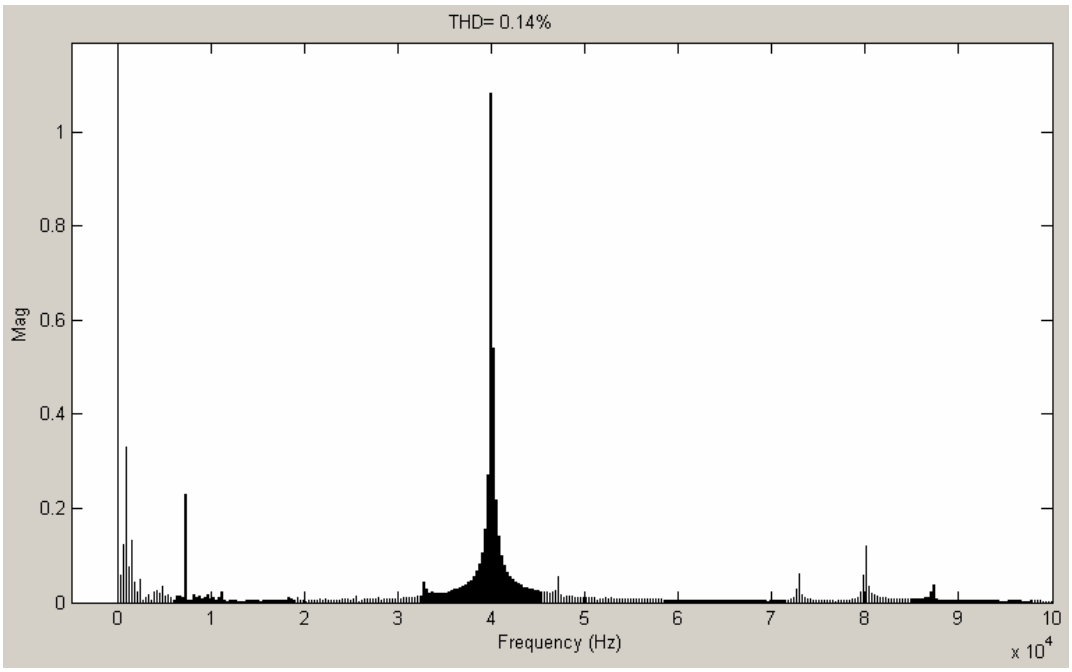


Fig. 27(e) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 2µs dead time, dc fundamental is 600.0V.

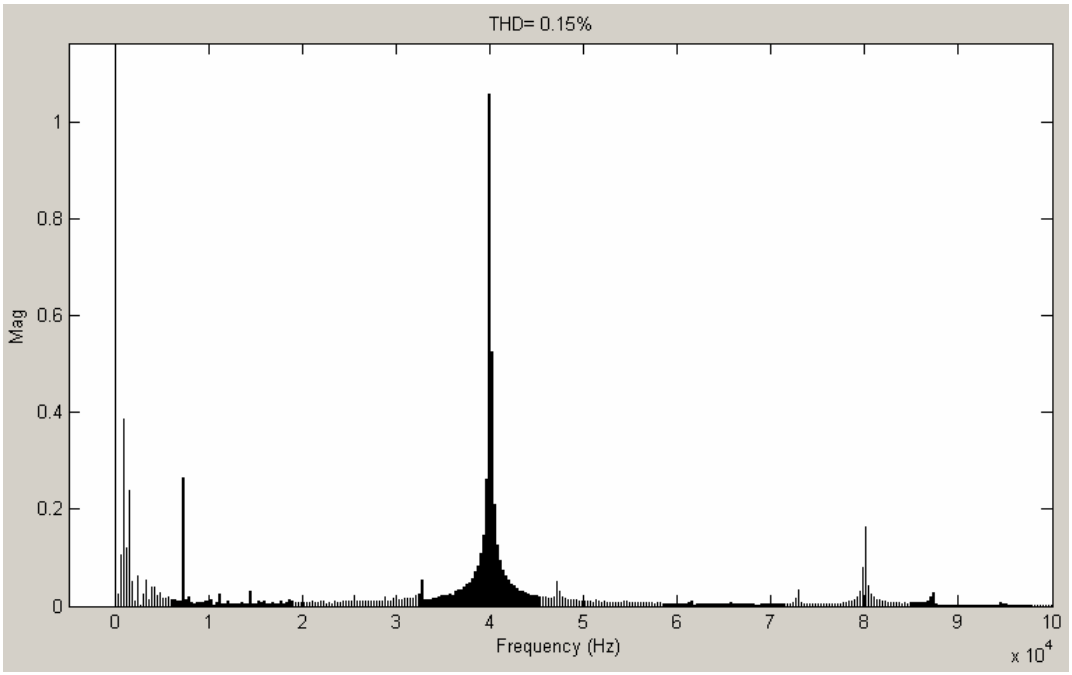


Fig. 27(f) – Dc-bus voltage FFT plot of the six-phase independent windings active rectifier, 20 kHz carrier frequency, 5µs dead time, dc fundamental is 600.0V.

# 4. CURRENT-CONTROLLED ACTIVE RECTIFIER INVESTIGATIONS

## 4.1 Current-Control of Active Rectifiers

Current-control was implemented in the active rectifier models using a modulation scheme similar to that in [17]. Advantages of implementing this current-control scheme over the voltage-control scheme discussed previously include improved control/regulation and power factor. Modulation is again performed by the PWM Generator, which now measures the per-unit instantaneous phase currents $I_{s,pu}$, and compares them to reference currents $I_{ref}$. To improve performance at startup, the magnitude of both signals is limited to 1.5 by saturation blocks. The reference current is formed for each phase by multiplying the dc-bus voltage error with sinusoids synchronized with the source voltage waveforms and a gain $G$. For simplicity in simulation, the per-unit back emf voltages $V_{s,pu}$ were used as these sinusoids, producing a reference current of

$$I_{ref} = \left(V_{dc} - V_{dc,ref}\right) \cdot G \cdot V_{s,pu} . \tag{2}$$

The dc-bus voltage error gain $G$ was implemented using a PID Controller with a proportional gain of 0.01, an integral gain of 20, and a derivative gain of zero; any derivative gains other than zero produced instability in the model. For each phase, the reference current was subtracted from the per-unit phase current to produce a current error signal. For improved dc-bus voltage regulation, this error signal was multiplied with the ratio of actual by reference dc-bus voltage to form the modulation signal, $I_{mod}$, given as

$$I_{\mathrm{mod}} = \left(I_{s,pu} - I_{ref}\right) \cdot \frac{V_{dc}}{V_{dc,ref}} . \tag{3}$$

These modulation signals were limited to a magnitude of 0.95 with a saturation block to prevent overmodulation and used in a sine-triangle comparator to generate gating signals as in the voltage-controlled scheme discussed previously. A dead time of 5μs was implemented in the sine-triangle modulation to eliminate dc-bus shorting. Larger values may be used without significant negative effects in active rectifier performance, allowing for increased simulation speed with the ability to use larger time steps.

**4.2 Updated Simulation Specifications from BAE Systems**

Performance of the current-controlled active rectifier was evaluated using updated generator specifications provided by BAE Systems as follows:

1. six-phase windings configured as dual 3-phase sets with zero degree offset
2. access to neutrals for independent phase testing
3. back EMF of $380V_{LL}$ rms
   (phase back EMF of 219.39V rms for independent phase configuration)
4. phase inductance of 60μH, phase resistance unchanged at 48mΩ
5. electrical frequency of 708 Hz (4250rpm, 10 pole pairs)

Specifications of the power-electronic devices used in further simulations, provided by BAE Systems, were from the Powerex configurable IGBT based power assemply (Powerex model PP75B120). These assemblies contain configurable sets of IGBT/diode modules in a heatsink-mounted package with integrated protection and gate drive circuitry. Specifications used to represent the IGBT/diode modules (Powerex model CM75DU24F) in the Matlab Simulink simulations are as follows:

1. diode forward voltage of 5.0V
2. IGBT forward voltage of 3.2V
3. IGBT fall time of 300ns

All remaining simulations were run with a switching frequency of 15 kHz. A 400kW resistive load was applied to the 600V dc-bus with bus capacitance of 2400μF. Parallel RC snubbers with a resistance of 100Ω and capacitance of 176.84nF were installed on each switching device, necessary to improve simulation speed and eliminate voltage spikes at the motor terminals. It should be noted that BAE Systems did not desire the use of snubber circuits, however there were significant convergence errors in simulation in their absence. High impedance snubber circuits were therefore chosen to improve simulation performance without greatly contributing to system losses.

### 4.3 Current Control in 2x3-Phase Wye Configuration

Simulation of the 2x3-phase wye configuration with updated generator specifications was carried out using current-control. The Matlab Simulink schematic for this configuration is shown in Fig. 28. In this model, the two Universal Bridge blocks were replaced with two three-phase bridges constructed using individual IGBT and diode blocks with parallel RC snubber circuits, as shown in Fig. 29. This change was performed to allow access to individual semiconductor device and snubber currents, as well as to allow for future testing of device fault conditions. With the updated generator specifications, the current-control scheme was able to produce a displacement power factor of approximately 0.95, which may be improved through further control optimization. The PWM Generator for this model utilizing current-control is shown in Fig. 30.

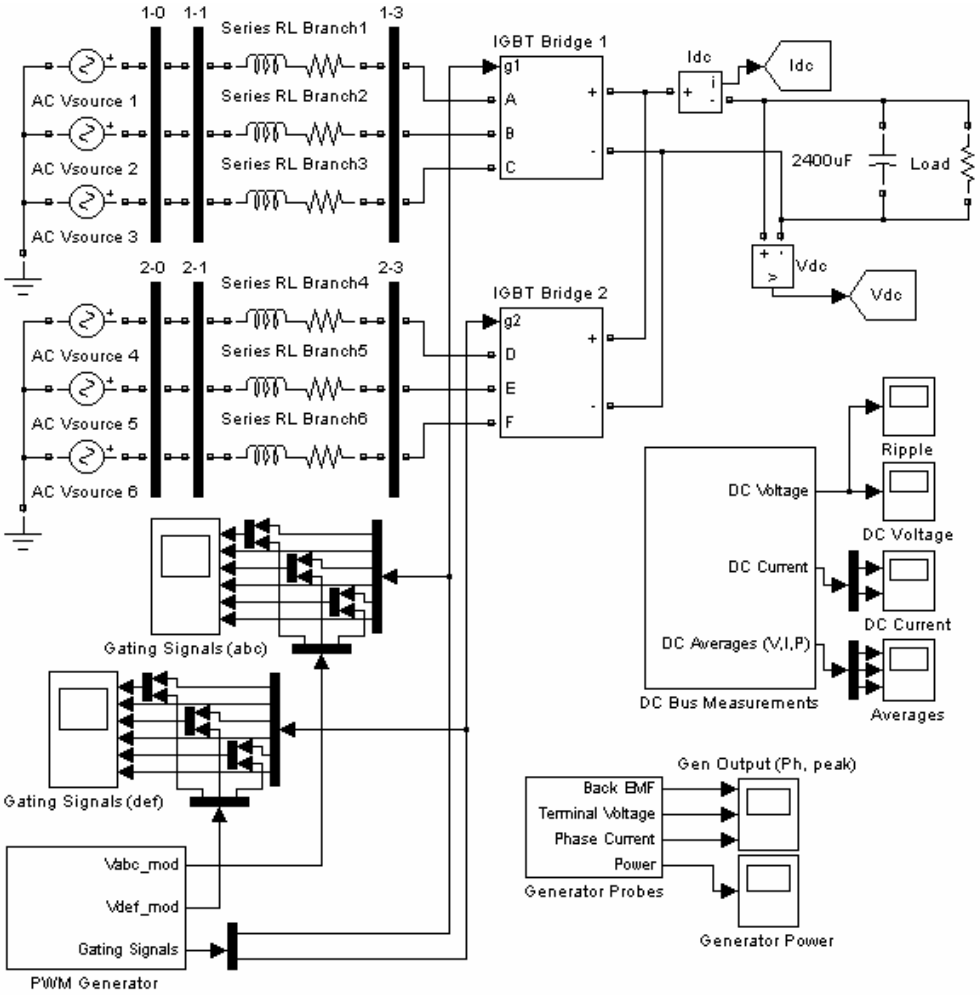


Fig. 28 – 2x3-phase wye system schematic.

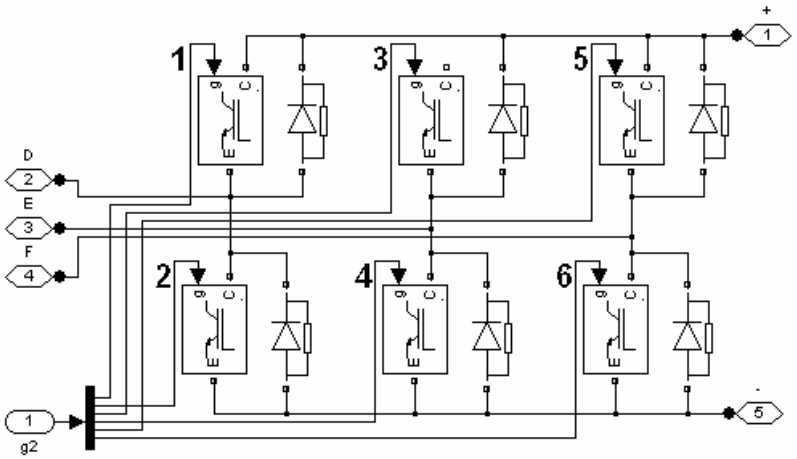


Fig. 29 – Three-phase active rectifier schematic (two utilized).

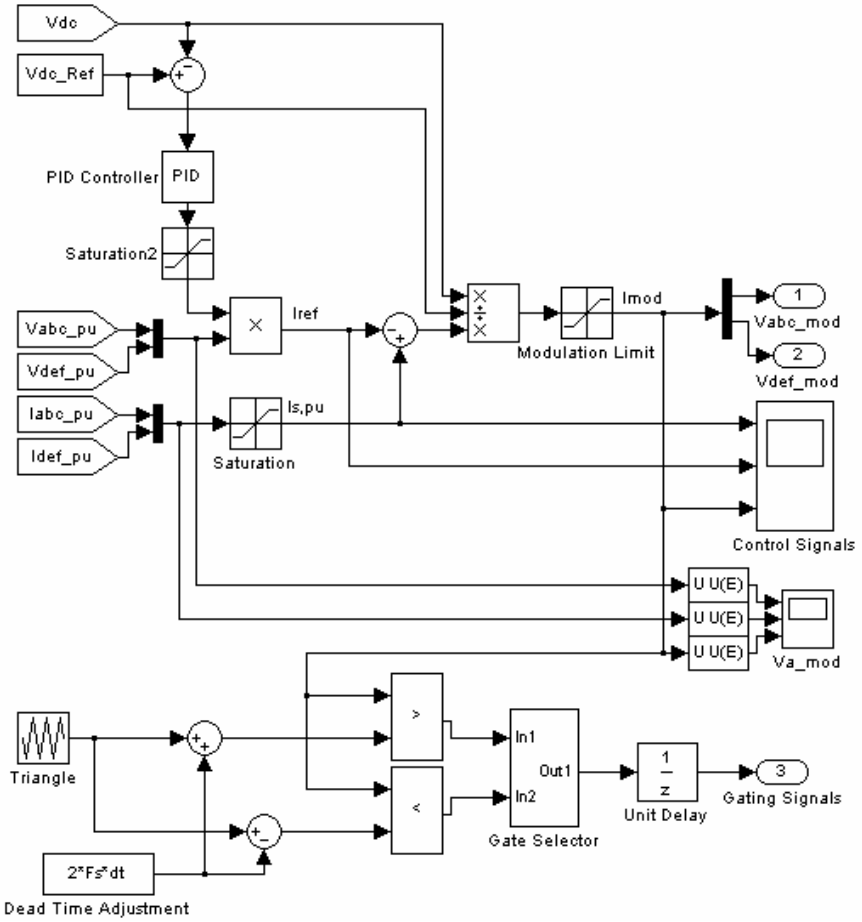


Fig. 30 – 2x3-phase wye PWM Generator schematic.

### *4.3.1 Current-Control Operation in the 2x3-Phase Wye Configuration*

Fig. 31 shows the phase A modulation control signals produced after the system reaches steady state. Due to balanced generator conditions, waveforms for other phases are nearly identical with the appropriate phase shift. As shown by the phase A modulation signal (Ia_mod), the desired dc-bus voltage of 600V was achieved with a modulation index of approximately 0.78.

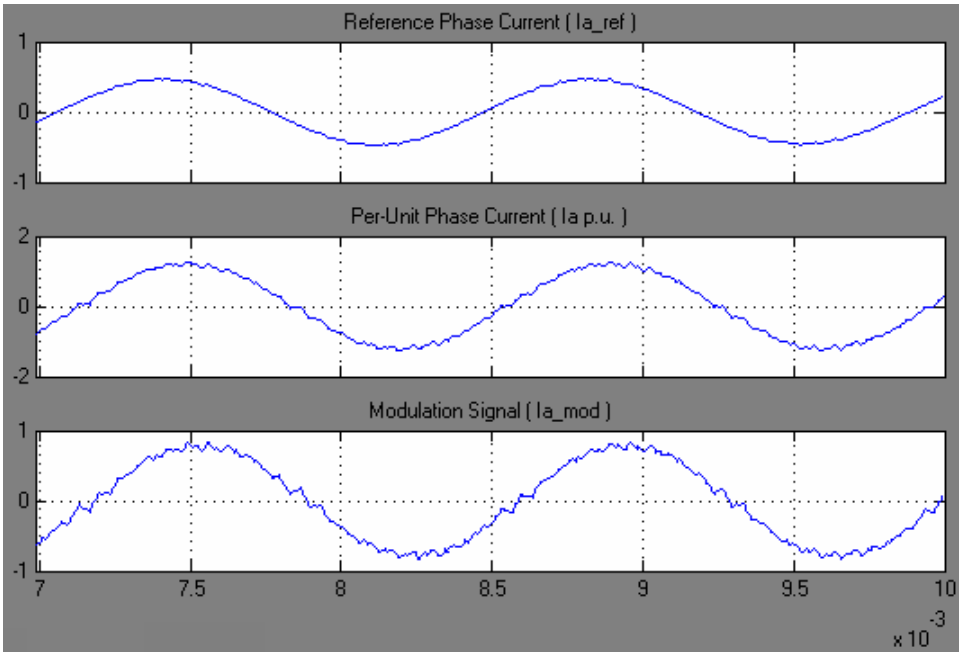


Fig. 31 – Current-control waveforms for 2x3-phase wye configuration.

Gating signals were generated by comparing the modulation signal for each phase with a triangular carrier wave shifted vertically for dead-time compensation. Fig. 32 shows the modulation signals used in sine-triangle modulation as well as gating signals produced for IGBT 1 (TA+) and IGBT 2 (TA-) on the phase A rectifier leg.

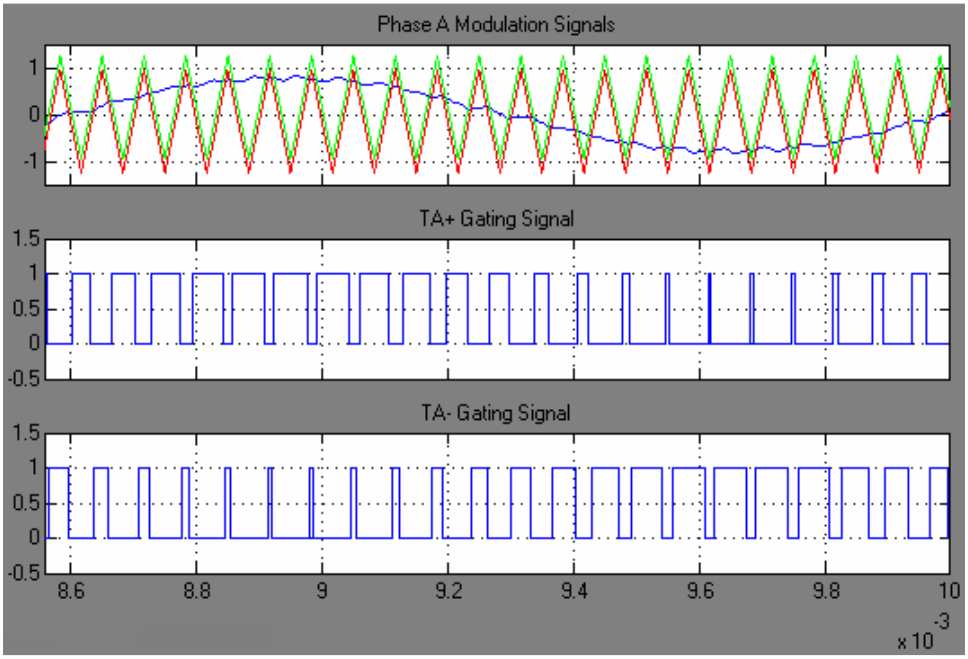


Fig. 32 – Modulation and gating signals for phase A of the 2x3-phase wye configuration.

Device currents at steady state are provided in Fig. 33 for the diodes and IGBTs of the phase A rectifier leg for two periods of the input electrical frequency. In this figure it can be seen how gating the complimentary IGBT controls the current flow through each diode.

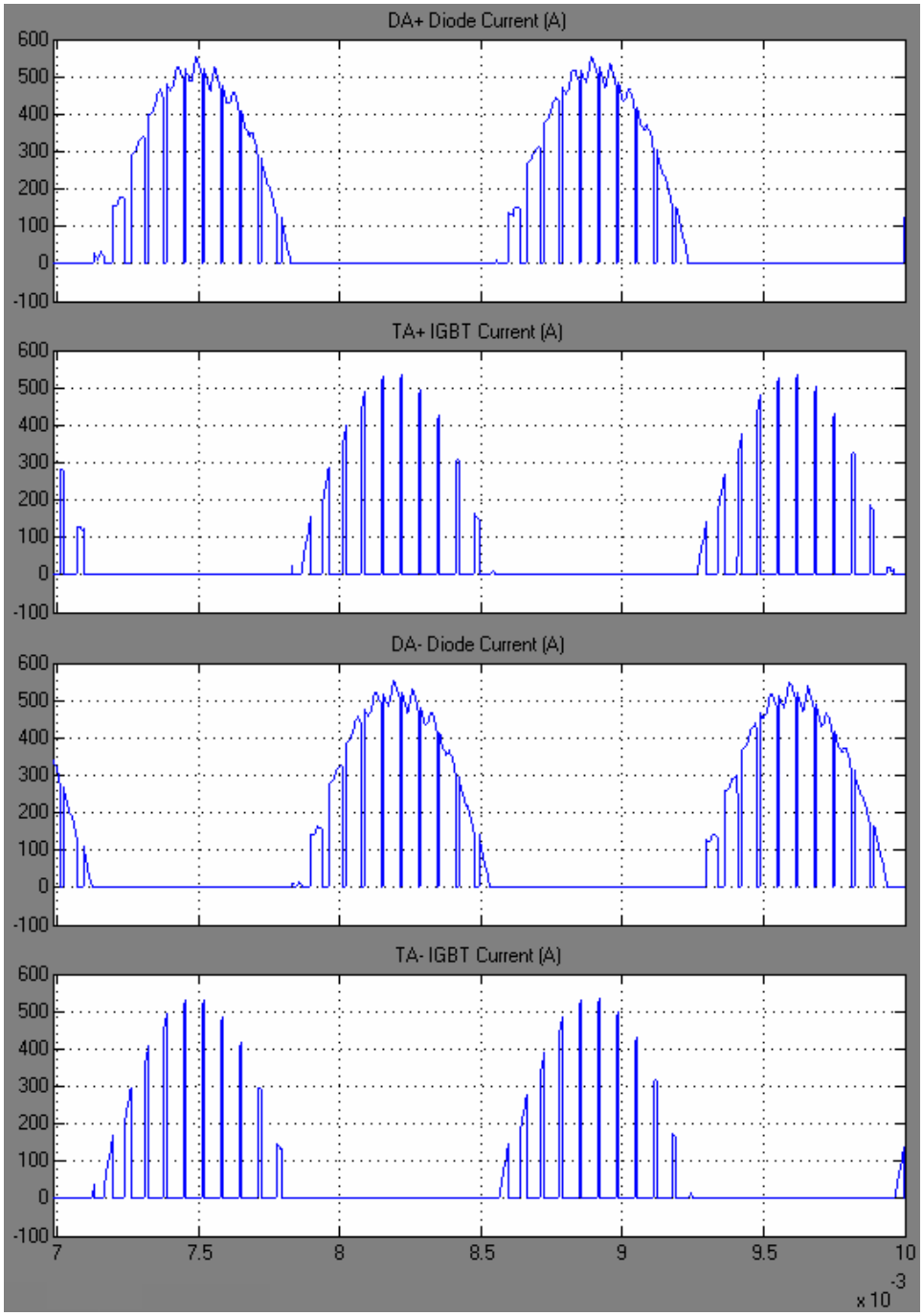


Fig. 33 – Device currents for the phase A rectifier leg of the 2x3-phase wye configuration.

Back emf, generator terminal voltage (after phase impedance), and phase current waveforms are provided in Fig. 34. It should be noted that all six phases are present, however due to a zero degree offset between the two 3-phase wye-connected winding sets and ideal simulation conditions there are only 3 waveforms visible. As shown, the outcome of properly gating the IGBTs is a nearly sinusoidal input current with relatively little phase delay.

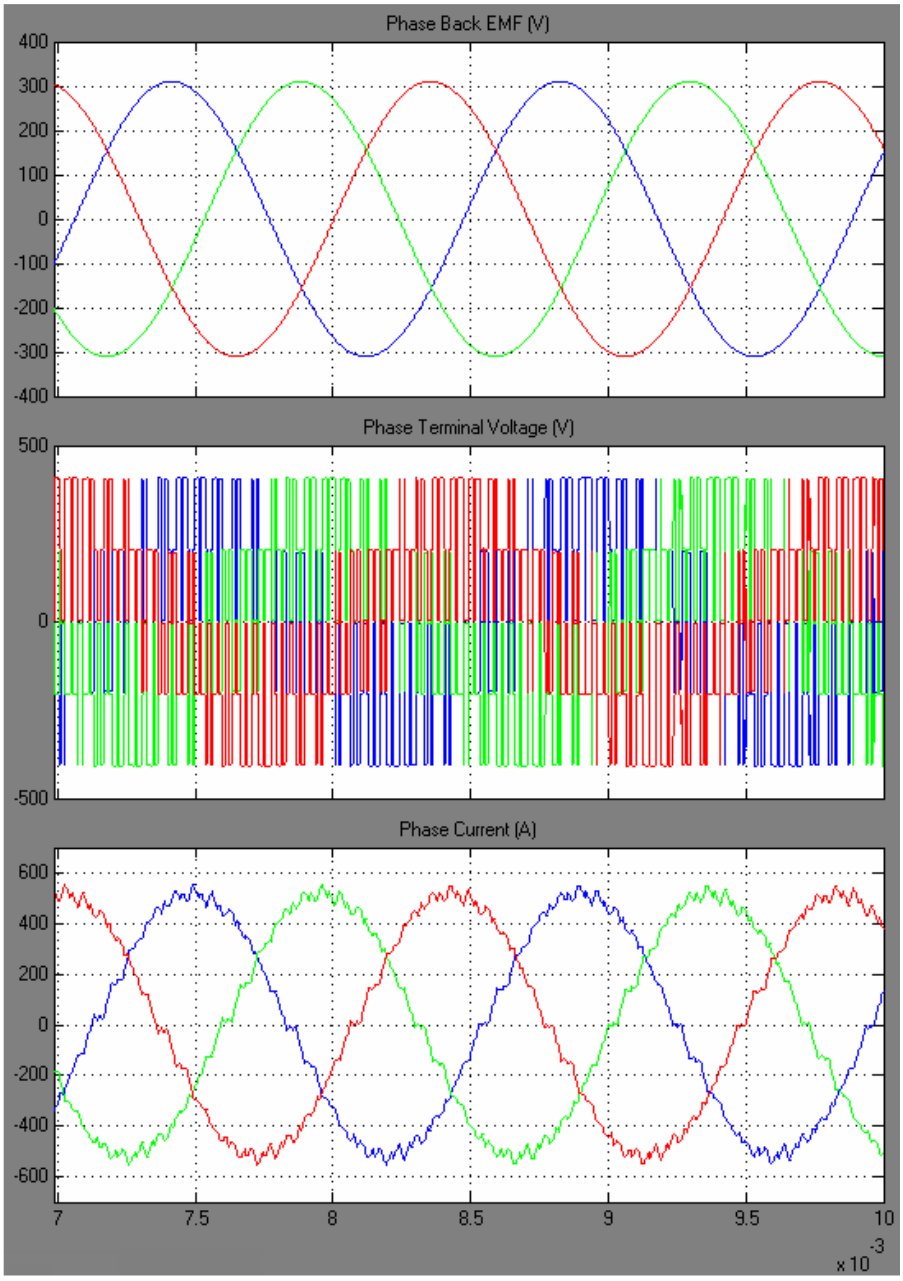


Fig. 34 – Input voltage and current waveforms of the 2x3-phase wye configuration.

The dc-bus voltage and current for the simulated time is shown in Fig. 35 with steady state values after the initial transient shown for two periods of the input frequency in Fig. 36. It is observed that a dc-bus voltage ripple of approximately 4.5V is produced with only positive currents at the output of the rectifier bridge, indicating the absence of switching faults.

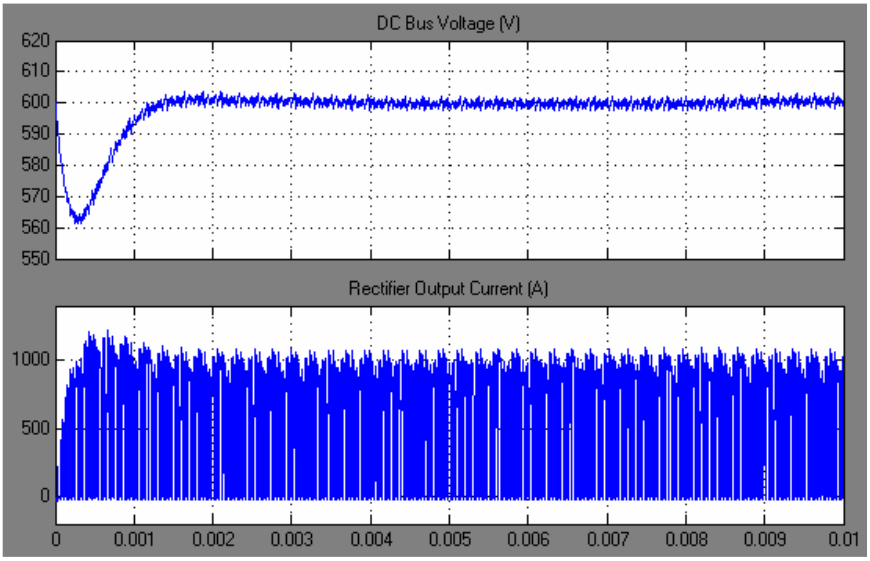


Fig. 35 – Dc-bus voltage and current waveforms of the 2x3-phase wye configuration.

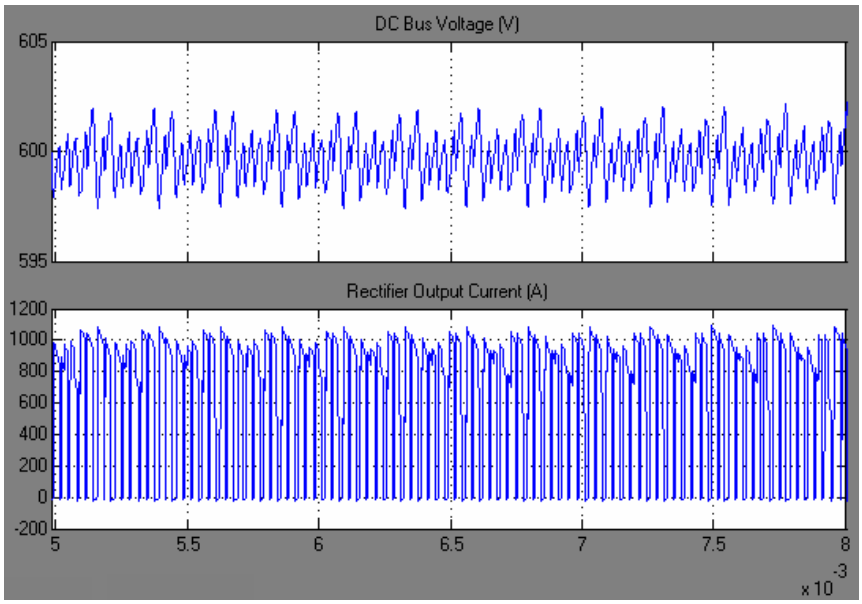


Fig. 36 – Steady-state dc-bus voltage ripple and detailed current waveform of the 2x3-phase wye configuration.

### *4.3.2 Harmonic Analysis of the Current-Controlled 2x3-Phase Wye Configuration*

Harmonic analysis was performed on the input current and output dc-bus voltage of the 2x3-phase wye-connected active rectifier configuration using the FFT Analysis tool in the PowerGUI block of Matlab Simulink. As shown in Fig. 37, dominant harmonics in the phase A input current include the $5^{th}$, $7^{th}$, $11^{th}$, and $13^{th}$, as well as sidebands at multiples of the 15 kHz switching frequency. The fundamental current at 708 Hz has a magnitude of 519.28A and the largest harmonic is a magnitude of 11.14A (2.146%) at a frequency of 13.59 kHz, which is the switching frequency (15 kHz) minus twice the fundamental frequency. The total harmonic distortion (THD) of the phase A input current, including all harmonic content up to 100 kHz, is calculated to be 5.138%.

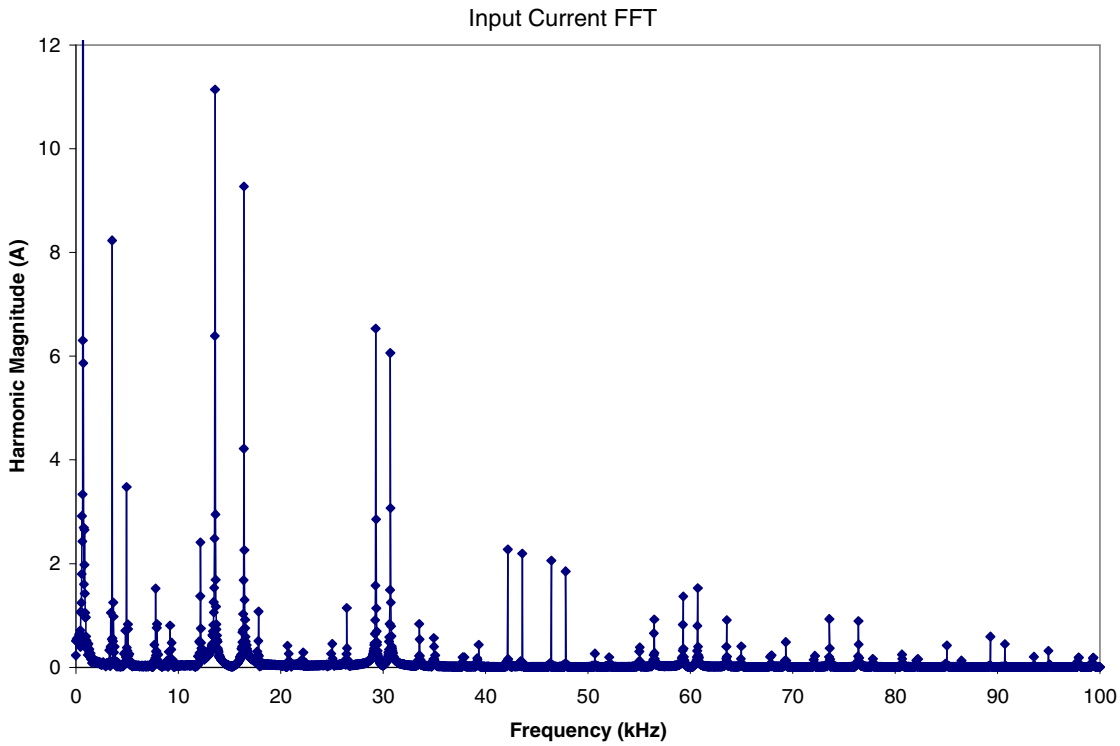


Fig. 37 – Harmonic content of the phase A input current of the 2x3-phase wye-connected active rectifier configuration; 15 kHz switching frequency, 5µs dead-time.

The harmonic spectrum of the dc-bus voltage is shown in Fig. 38. The dominant harmonic in the 600V dc-bus occurred at twice the switching frequency, 30 kHz, with a magnitude of 0.831V (0.1385%). Other harmonics present are located at six-times the input fundamental and multiples and sidebands of the 15 kHz switching frequency. The THD of the dc-bus voltage, including all harmonic content up to 100 kHz, is calculated to be 0.256%.

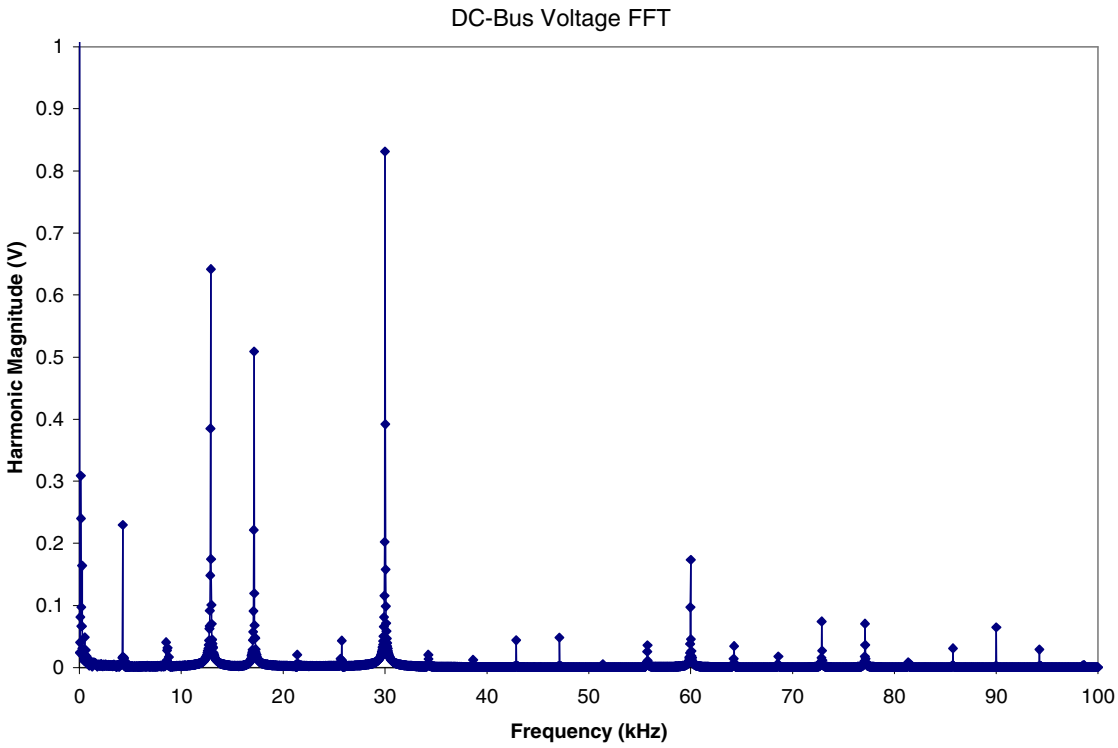


Fig. 38 – Harmonic content of output dc-bus voltage of the 2x3-phase wye-connected active rectifier configuration; 15 kHz switching frequency, 5µs dead-time.

### 4.4 Current Control in the Six-Phase Independent Configuration

Simulation of the six-phase independent configuration with updated generator specifications was carried out using the current-control scheme described previously. The dc-bus reference voltage was reduced to 346.41V due to the inherently lower ($\sqrt{3}$) output voltage potential of the independent phase configuration. A 400kW load was maintained at the lower dc-bus voltage level to produce the same source current magnitudes as in the wye configuration. The Matlab Simulink system model for this configuration is shown in Fig. 39. Each independent phase winding is connected to a single-phase H-bridge active rectifier constructed using individual IGBT and diode blocks with parallel RC snubber circuits, as shown in Fig. 40. With the updated generator specifications, the current-control scheme was able to produce a displacement power factor of approximately 0.96, which again may be improved through further optimization of the control-scheme, shown in Fig. 41.

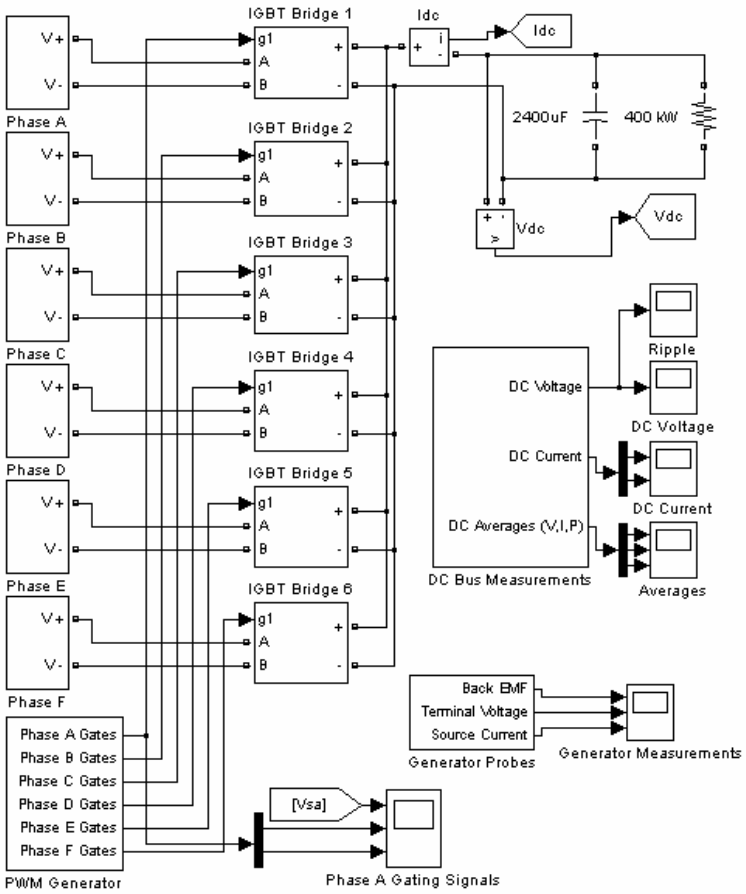


Fig. 39 – Six-phase independent system schematic.

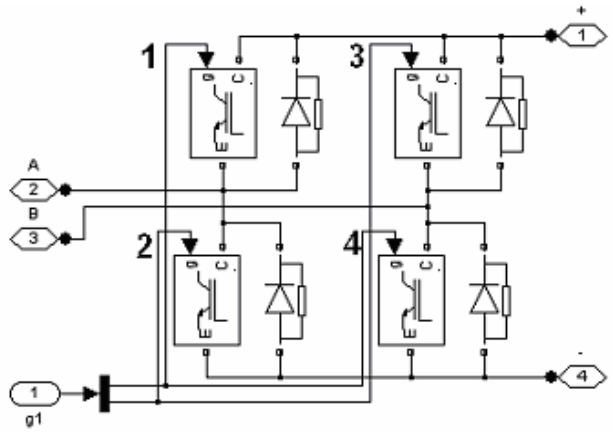


Fig. 40 – Single-phase, H-Bridge active rectifier (six utilized).

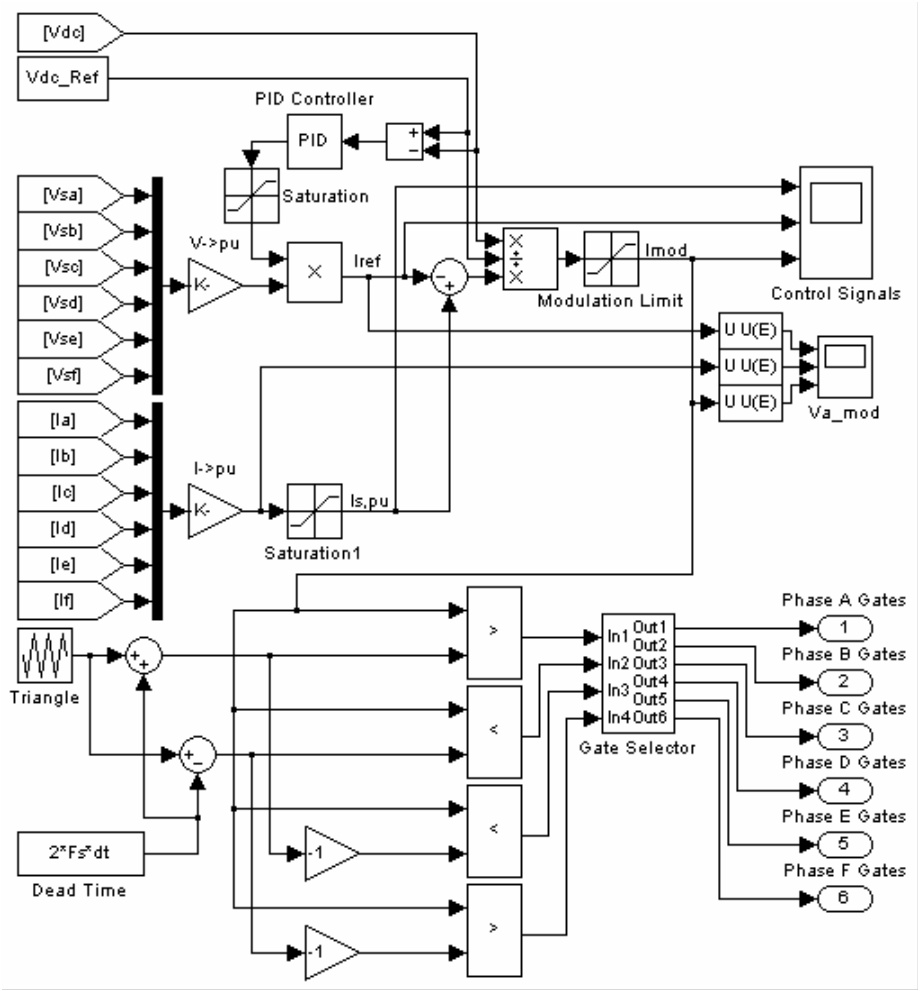


Fig. 41 – Six-phase independent PWM Generator schematic.

### *4.4.1 Current Control Operation in the Six-Phase Independent Configuration*

Control of the six-phase independent configuration was carried out similar to in the wye configuration with the exception of gating signal generation. Fig. 42 shows the phase A modulation control signals produced after the system reaches steady state. Again, due to balanced generator conditions, waveforms for other phases are nearly identical with the appropriate phase shift. As shown by the phase A modulation signal (Ia_mod), the desired dc-bus voltage of 346.41V was achieved with a modulation index of approximately 0.73.

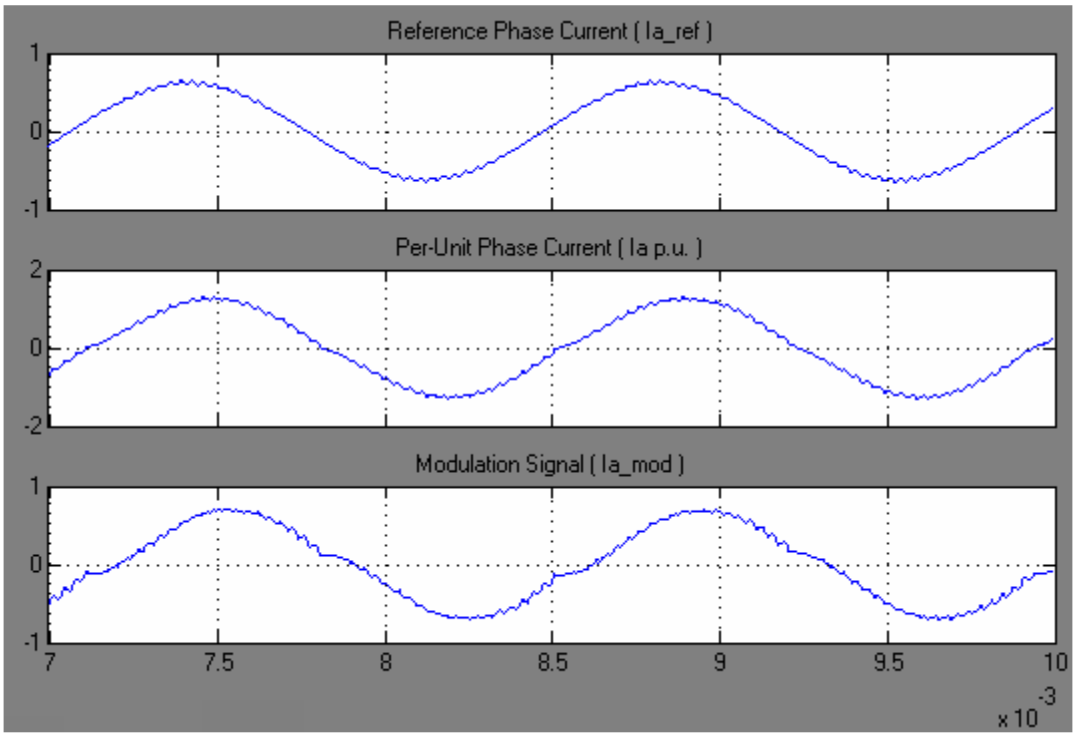


Fig. 42 – Phase A current-control waveforms for six-phase independent configuration.

For each phase, complimentary gating signals are created for IGBTs 1 and 2 as in the wye configuration, utilizing vertically shifted triangle carrier waves to implement dead time compensation. Changes arise in the generation of the gating signals for IGBTs 3 and 4; a triangle carrier signal offset by half the switching period was utilized to prevent conducting device pairs (1 and 4, 2 and 3) from switching in the same instance. This offset switching has the effect of eliminating a dominant harmonic at the switching frequency in both the input current and output dc-bus voltage. Fig. 43 shows the modulation signals used in sine-triangle comparison for

switches 1 and 2 as well as gating signals generated for the four devices in the phase A rectifier. Triangle carriers used for the generation of gating signals 3 and 4 are not shown, but are simply inverted to create the half switching period offset.

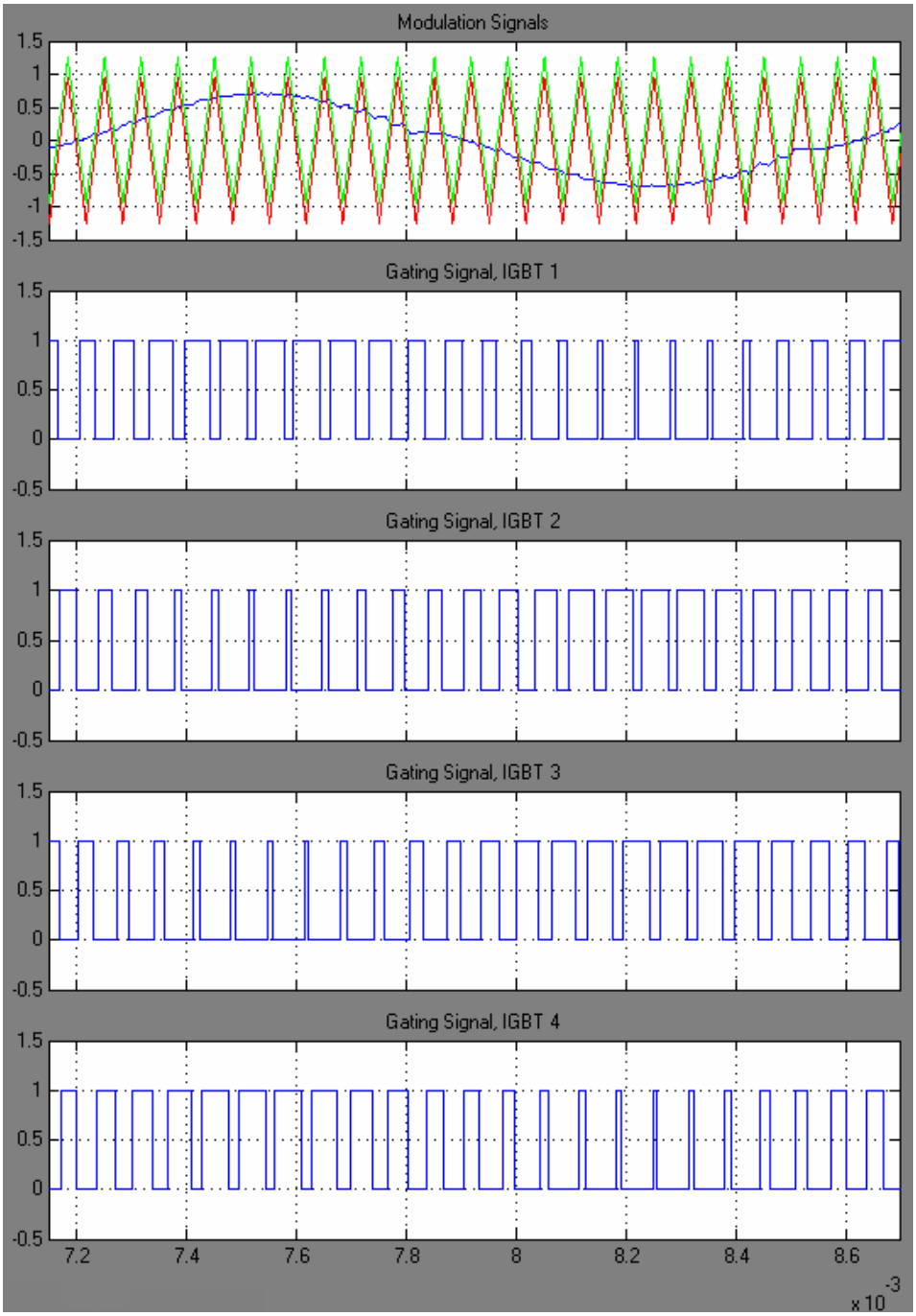


Fig. 43 – Modulation and gating signals for phase A of the six-phase independent configuration.

Device currents at steady state are provided in Fig. 44 for the diode/IGBT pairs 1 and 2 of the phase A rectifier for two periods of the input electrical frequency. As expected, with similar input current magnitudes, device currents on this leg of the single-phase rectifier are comparable to those on the phase A leg of the wye-connected rectifier.

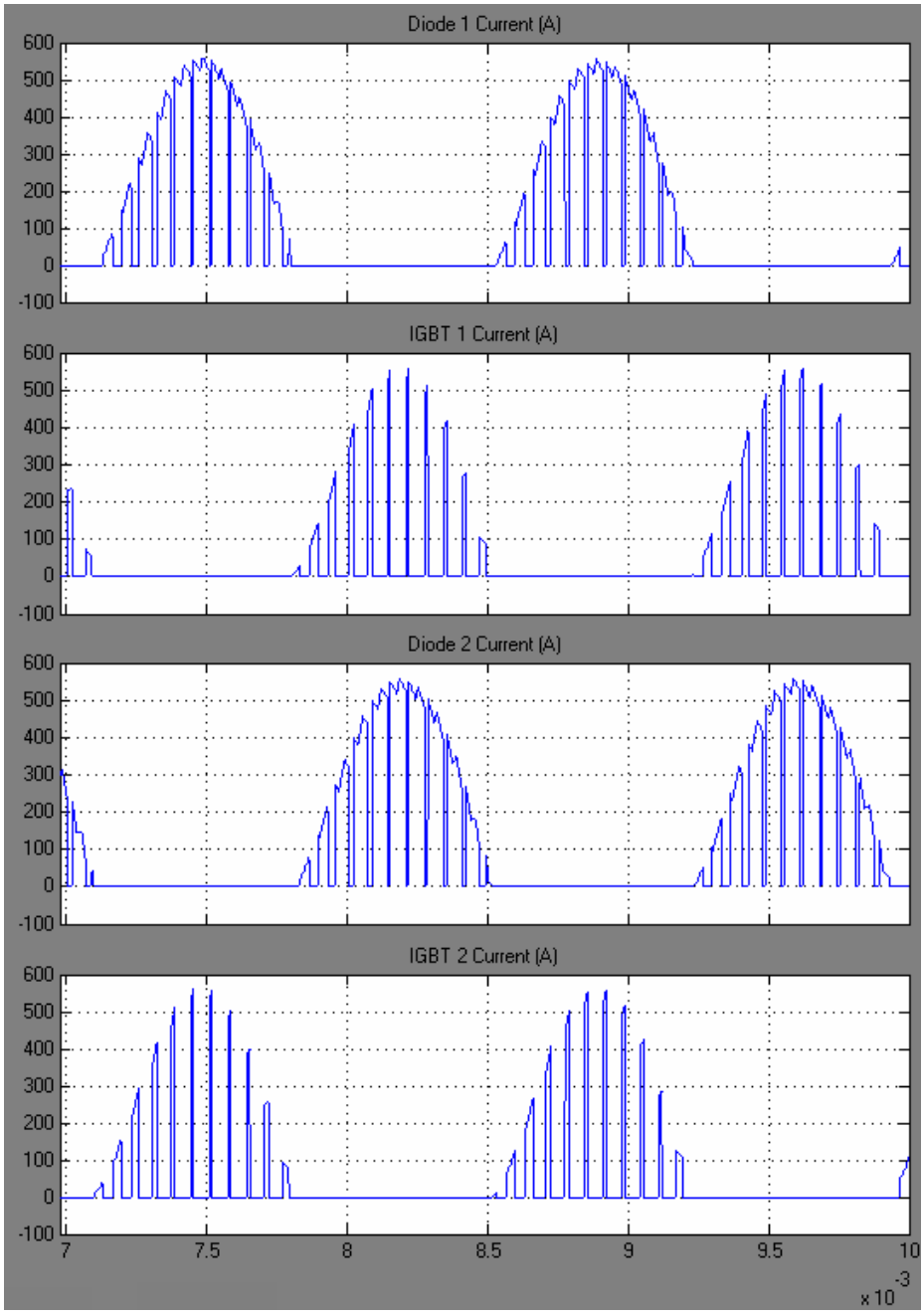


Fig. 44 – Device currents for diode/IGBT pairs 1 and 2 on the phase A H-bridge rectifier.

Back emf, generator terminal voltage (after phase impedance), and phase current for the six-phase independent configuration are provided in Fig. 45. Again, due to the zero degree offset between the three-phase winding sets, all six phases are present though only three waveforms are visible.

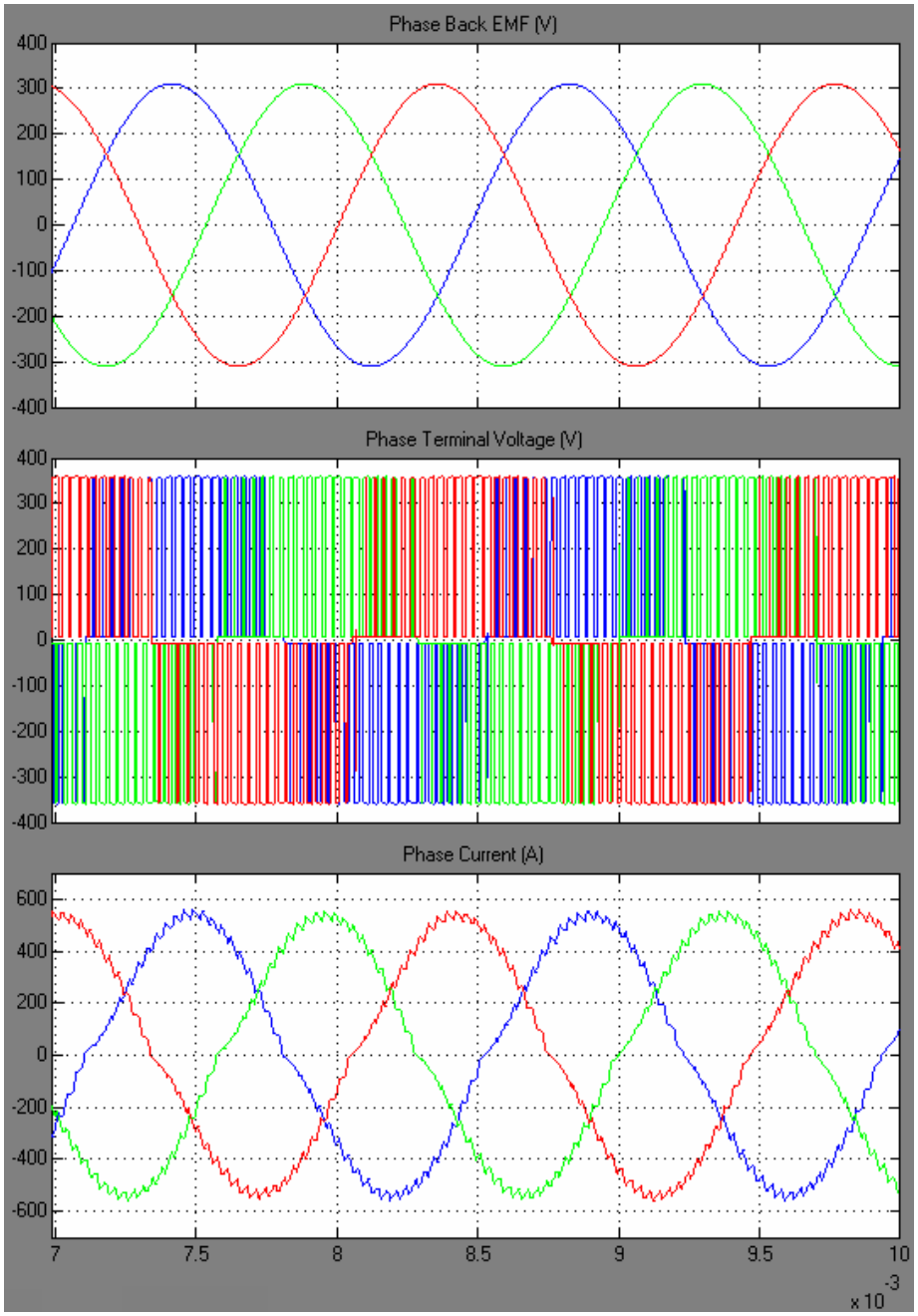


Fig. 45 – Input voltage and current waveforms of the six-phase independent configuration.

The dc-bus voltage and current for the simulated time is shown in Fig. 46 with steady state values shown for two periods of the input frequency in Fig. 47. The dc-bus voltage ripple is slightly higher than in the wye configuration, approximately 6.0V.

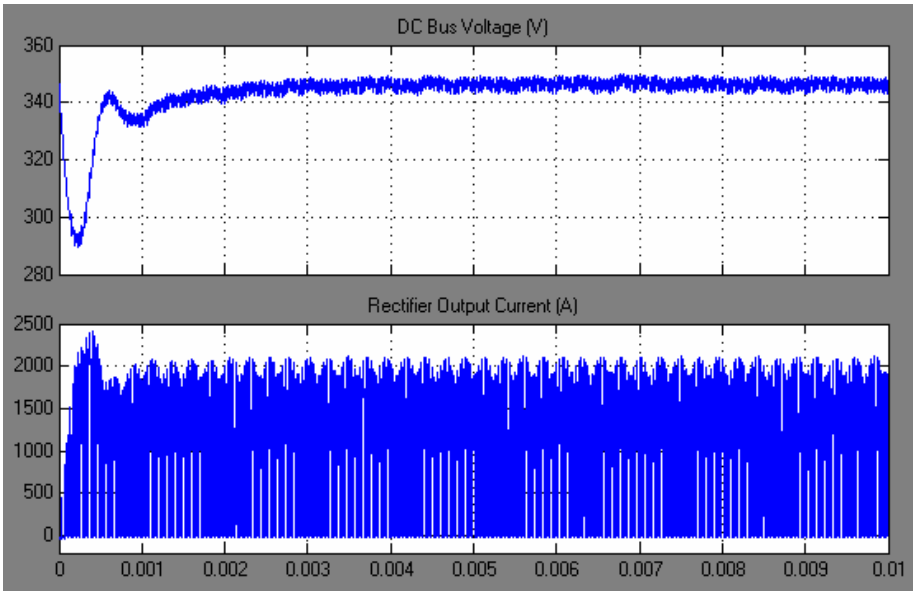


Fig. 46 – Dc-bus voltage and current waveforms of the six-phase independent configuration.

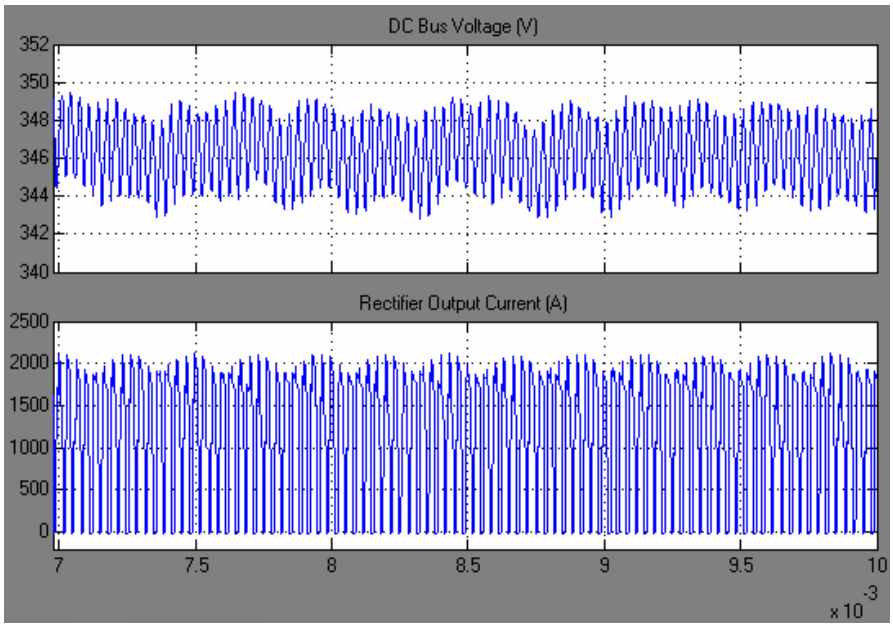


Fig. 47 – Steady-state dc-bus voltage ripple and detailed current waveform of the six-phase independent configuration.

### *4.4.2 Harmonic Analysis of the Current-Controlled Six-Phase Independent Configuration*

Harmonic analysis was performed on the phase A input current and output dc-bus voltage of the six-phase independent active rectifier configuration. As shown in Fig. 48, dominant harmonics in the phase A input current include the 5$^{th}$, 7$^{th}$, 11$^{th}$, and 13$^{th}$, similar to the wye configuration, with the addition of triplen harmonics (3$^{rd}$, 9$^{th}$, etc.) due to single-phase rectifier operation. Switching frequency harmonics are found at sidebands of twice the switching frequency (30 kHz) and multiples of this value with the use of offset gating the conducting device pairs. The fundamental current at 708 Hz has a magnitude of 525.47A and the largest harmonic is a magnitude of 21.86A (4.16%) at a frequency of 2.124 kHz (3$^{rd}$ harmonic). The largest switching harmonic has a magnitude of 8.55A (1.63%), located at twice the switching frequency minus the fundamental (29.292 kHz). The THD of the phase A input current, including all harmonic content up to 100 kHz, is calculated to be 5.698%.

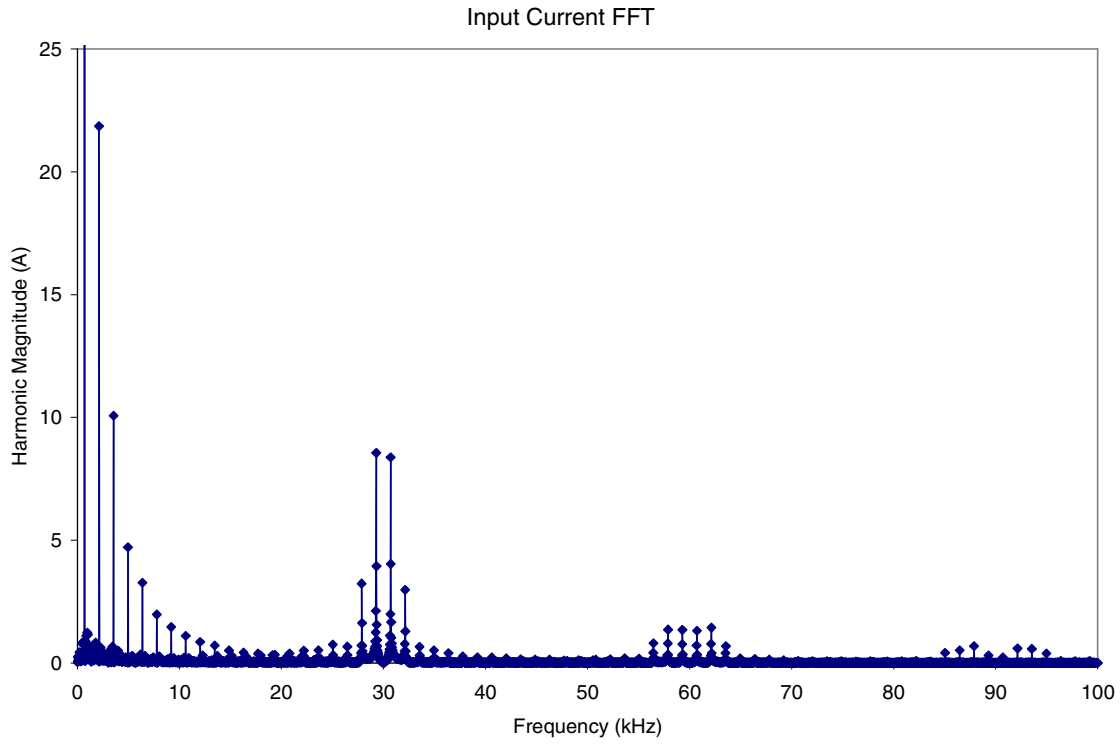


Fig. 48 – Harmonic content of the phase A input current of the six-phase independent active rectifier configuration; 15 kHz switching frequency, 5µs dead-time.

The harmonic spectrum of the dc-bus voltage is shown in Fig. 49. The dominant harmonic in the 346.41V dc-bus occurred at twice the switching frequency, 30 kHz, with a magnitude of 1.891V (0.546%). Other harmonics present are located at six-times the input fundamental and multiples and sidebands of twice the switching frequency. The THD of the dc-bus voltage, including all harmonic content up to 100 kHz, is calculated to be 0.6896%

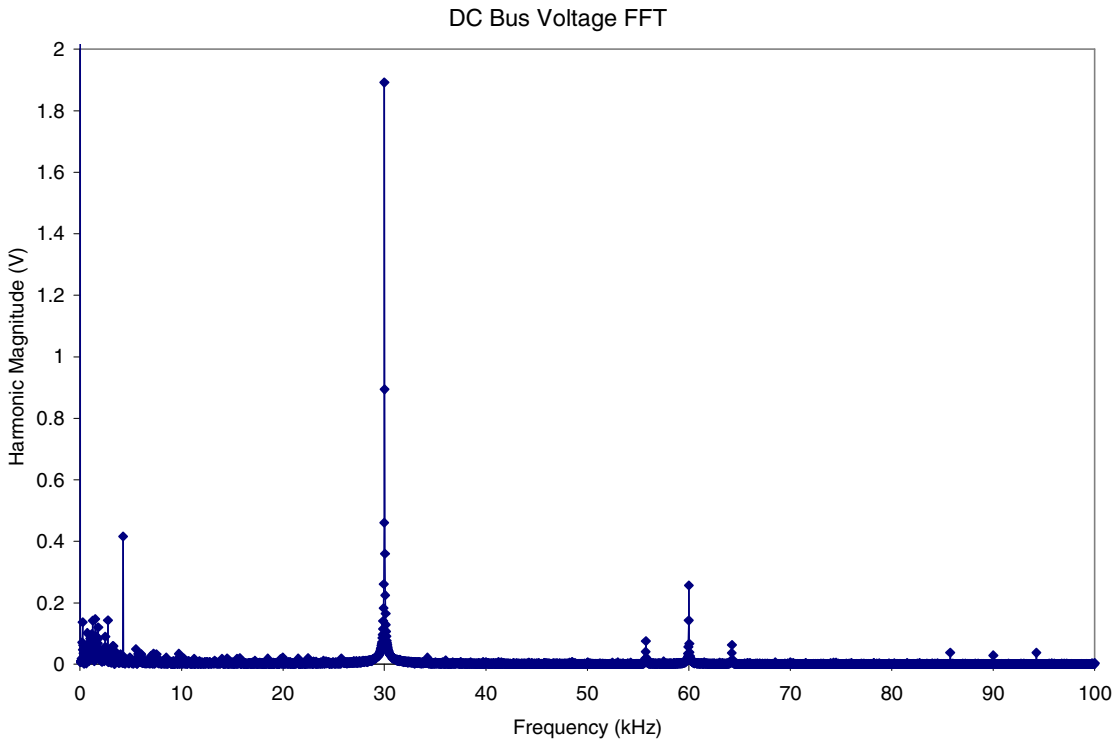


Fig. 49 – Harmonic content of the output dc-bus voltage of the six-phase independent active rectifier configuration; 15 kHz switching frequency, 5µs dead-time.

### *4.4.3 Effects of Offset Gating in the Six-Phase Independent Configuration*

To demonstrate the benefits of offset gating in the single-phase rectifiers of the six-phase independent configuration, harmonic analysis has been performed on the phase A input current and output dc-bus voltage using non-offset gating signals. Changes to the model include removing the offset gating signal generation (gates 3 and 4) from the PWM Generator and connecting the gates of conducting device pairs (1 and 4, 2 and 3). As shown in Fig. 50, with the non-offset gating signal generation there is a dominant harmonic produced in the input current at the 15 kHz switching frequency. The magnitude of this harmonic is 42.019A (8.0605%) with significant sideband harmonics also present. The THD of the input current with the inclusion of these additional switching harmonics is increased to 11.7867% from 5.698% with offset gating signal generation.

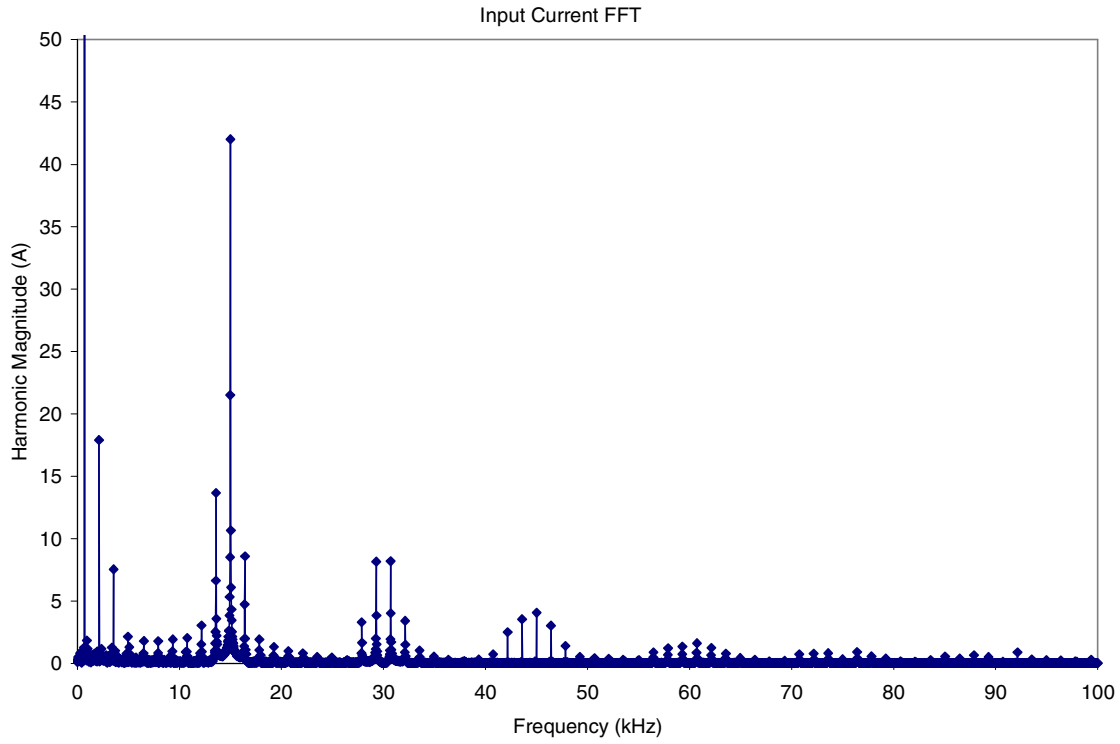


Fig. 50 – Harmonic content of the phase A input current of the six-phase independent active rectifier configuration with non-offset gating signal generation.

Effects of this non-offset gating signal generation is less predominant in the output dc-bus voltage. As shown in Fig. 51, there are additional sideband harmonics at the switching frequency and multiples thereof. Magnitudes of these additional harmonics are significantly smaller than observed in the input current, with the largest a magnitude of 1.2325A located at the switching frequency minus three-times the fundamental (12.876 kHz). The THD of the output dc bus voltage shows a minimal increased to 0.914475% from 0.6896% with offset gating signal generation.

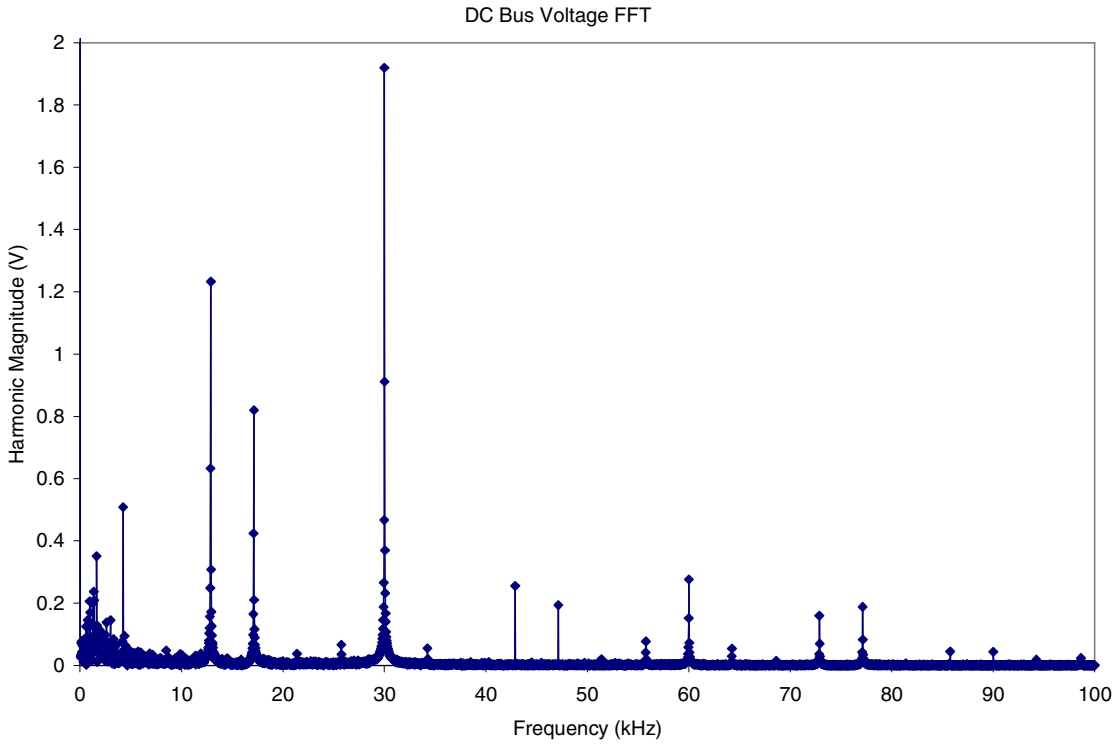


Fig. 51 – Harmonic content of output dc-bus voltage of the six-phase independent active rectifier configuration with non-offset gating signal generation.

It is noted that harmonics which were present with offset gating signal generation are relatively unchanged in magnitude. This leads to the conclusion that utilizing the offset gating signal generation scheme does not "shift" this switching harmonic energy to other frequencies, but eliminates it altogether. This conclusion is supported by the significant decrease in THD in both the input current and output dc-bus voltage.

# 5. SIMULATION VERIFICATION

## 5.1 Hardware Implementation

In order to validate model accuracy, hardware simulations were planned in the following configurations: 2x3-phase wye with zero degree offset, 3-phase wye, and 3-phase independent. The six-phase independent configuration could not be implemented due to hardware availability limitations (only four Powerex modules were provided by BAE Systems).

Hardware testing was carried out utilizing Powerex PP75B120 Pow-R-Pak H-Bridge IGBT assemblies, shown in Fig. 52. These modules contain four IGBTs with reverse-connected anti-parallel diodes in an H-bridge configuration with a control board providing protection and gate drive circuitry. The IGBT modules in these devices are rated at 75A continuous and 150A peak current with high switching frequencies. Gating signals for these modules were provided by an Opal-RT HILbox, or Hardware-In-Loop box, which is a fully integrated PC-based real-time hardware simulator, shown in Fig. 53. Utilizing analog inputs and digital outputs, the Opal-RT HILbox is able to generate gating signals for the Powerex modules by running Matlab Simulink simulations in real-time while sampling hardware signals such as voltages and currents.

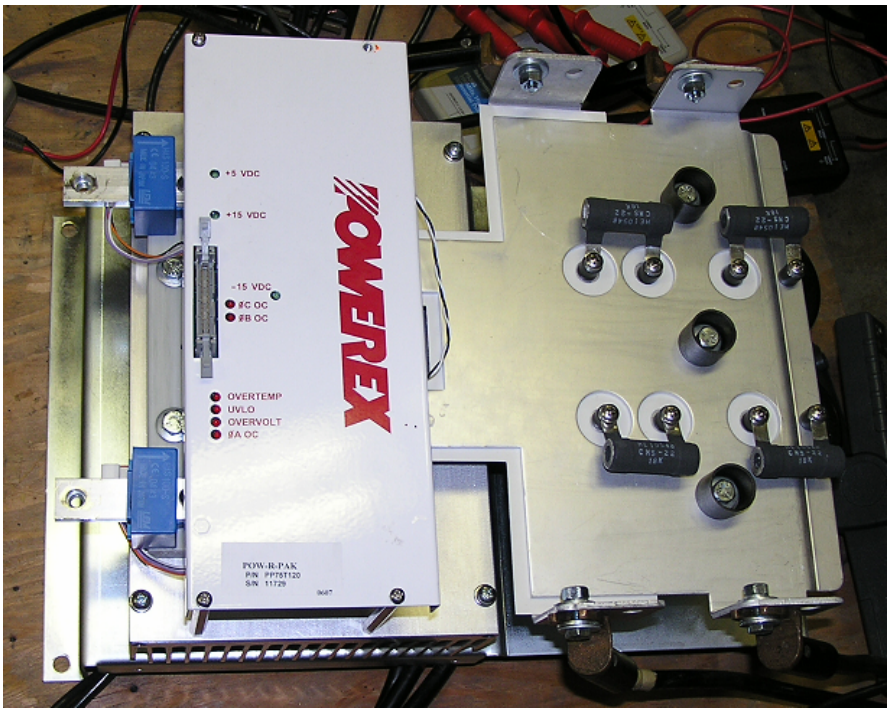


Fig. 52 – Powerex PP75B120 Pow-R-Pak H-bridge assembly.

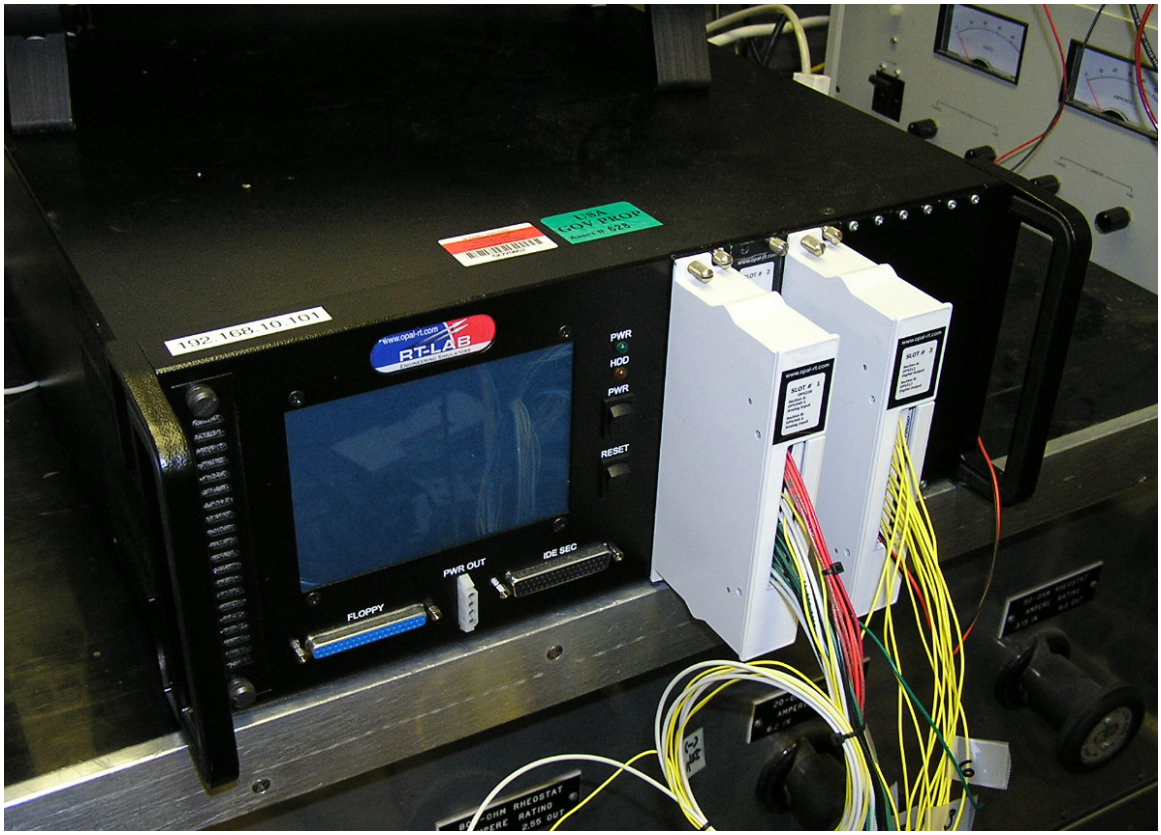


Fig. 53 – Opal-RT HILbox.

A Behlman three-phase 120kVA fully programmable source, shown in Fig. 54, was utilized to represent the permanent magnet synchronous generator for hardware testing. This allowed the desired electrical frequency of 708 Hz to be achieved with the ability to produce a balanced output voltage. Six-phase output was realized by connecting two three-phase 30kVA transformers to the programmable source, thus producing two three-phase synchronized sources representing the dual three-phase generator with zero degree offset. This also provided each phase with individual source impedance, which could not be achieved by directly connecting six inputs to the three-phase output of the programmable source. The impedance of these transformers is rated 3.95% at 60 Hz.

Fig. 54 – Three-phase 120kVA programmable source.

The six source phases were connected to the inputs of three Powerex modules, each having two ac inputs with their dc outputs connected in parallel with fused connections. Each H-bridge contained a 3300uF capacitor bank rated at 900V dc, which was removed from the three bridges receiving ac input. To ensure balanced current paths, the fused dc output of each bridge was connected via matching length cables to the fourth Powerex module which acted as the dc-bus capacitor bank. This fourth bridge was used as the capacitance bank for simplicity as it was a readily available, fully contained bank with a capacitance level of 3300uF, only slightly higher than the 2400uF in BAE Systems previous specification. This fourth bridge was then connected to an 18Ω fan-cooled resistive load, which would equate to 20kW at the desired dc-bus level of 600V. The Powerex gate drive boards were powered via a dc supply set to 24V and the digital

output module of the Opal-RT HILbox, used for outputting the gating signals to the drive boards, was powered by another dc supply set to 15V. Data acquisition was carried out using two model 5104 and one model 7104 Tektronix Digital Phosphor Oscilloscopes with appropriate probes. The entire test setup, minus the source, is shown below in Figs. 55 and 56. A schematic of the test setup is provided in Fig. 57.

Fig. 55 – Experimental test setup.

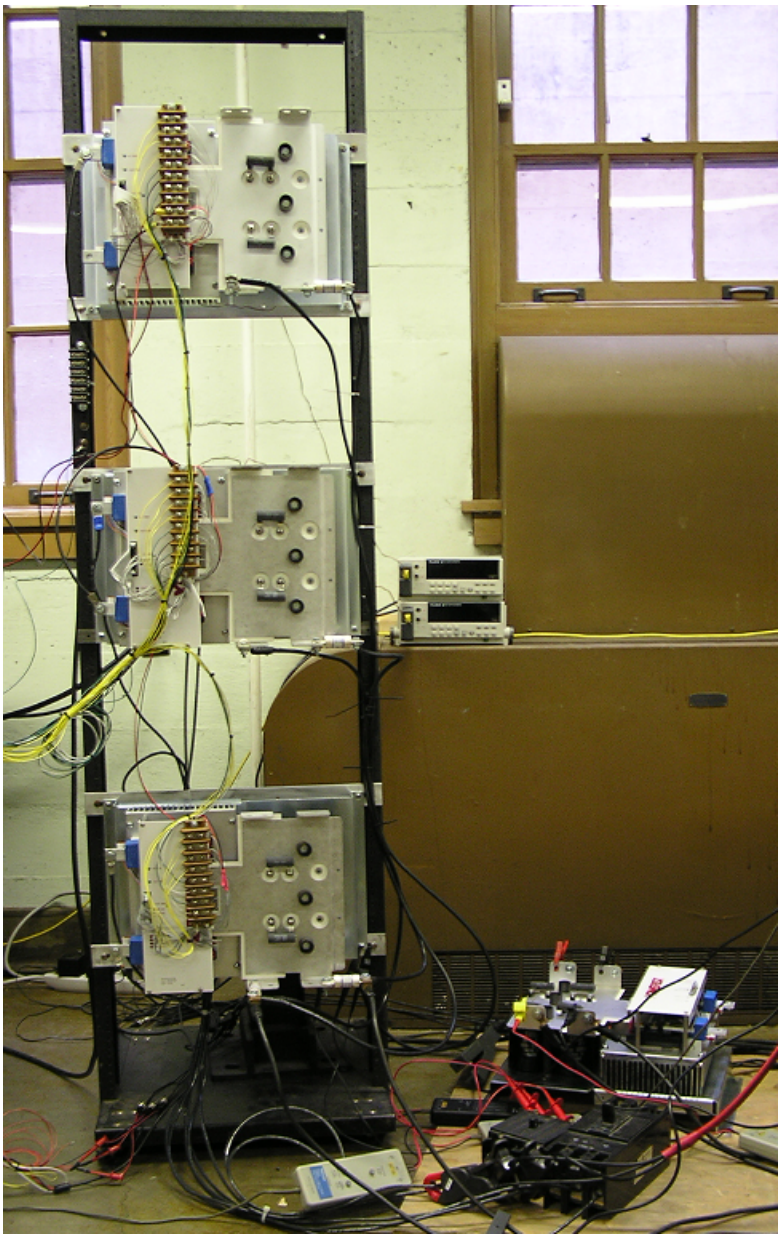

Fig. 56 – Powerex modules and dc-bus capacitor bank.

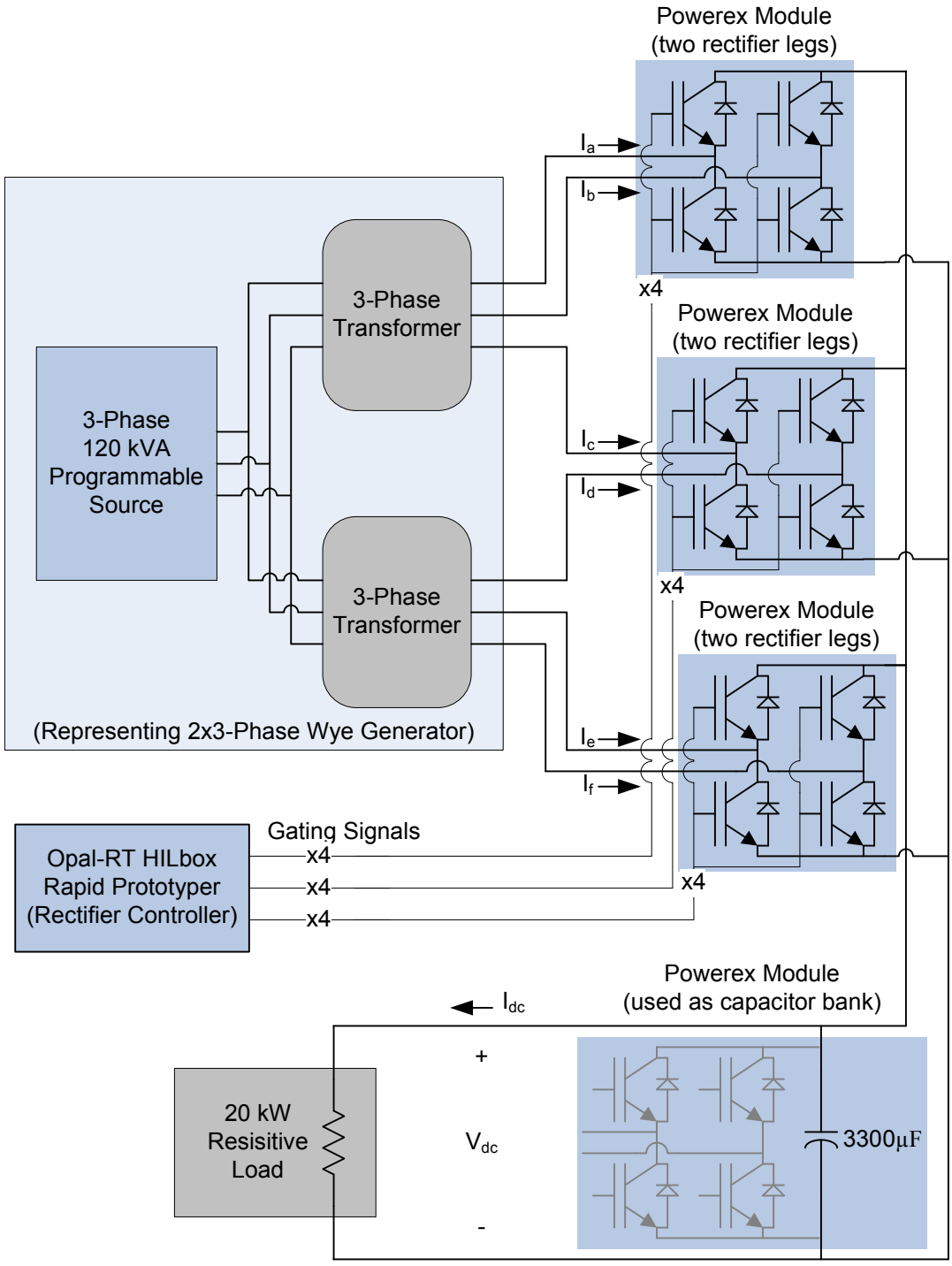


Fig. 57 – Schematic of 2x3-phase wye-connected test setup.

**5.2 Six-Phase Experimental Results**

Initial testing was conducted at lower power levels, beginning with 20V rms phase voltage at 60 Hz. Initial hardware testing was performed using a reduced switching frequency of 10 kHz with dead-time of 5µs. The test plan included slowly increasing the voltage and frequency. During initial testing, with 120V at 60Hz, one of the Powerex diode modules failed, disabling one phase of the bridge. At the time of diode failure, phase currents from the source were under 10A, well below the 75A continuous rating of the modules. At this point, the disabled module was swapped out with the module being used as the dc-bus capacitor bank. Testing was continued, and the frequency was slowly ramped up to 550 Hz, which was the highest frequency allowed by the programmable source before requiring "program mode" of operation. At 550 Hz, the voltage was increased in 20 V increments, and at 140V, a second Powerex module diode failed. At the time of the second diode failure, phase currents from the source were approximately 25A; again well below the 75A continuous rating of the modules. Based on these events, it was determined the failures were likely caused by either an IGBT misfire, or even more likely, by high voltage spikes at the ac terminals caused by the lack of snubber circuits on the switching devices. Recall that snubbers were utilized in all of software simulations to promote faster performance and reduced convergence errors, however BAE Systems decided to proceed in hardware testing without snubbers. These diode failure events resulted in six-phase operation being unobtainable and testing was continued in the three-phase wye configuration by utilizing only one transformer at the output of the programmable source and disconnecting the inactive bridges. Before continuing testing under three-phase operation, the dead time between when complimentary IGBTs can be fired was increased from 5µs to 10µs as an extra precaution to prevent dc-bus shorting caused by IGBT misfire.

**5.3 Three-Phase Experimental Results**

In three-phase operation, voltage and frequency were slowly increased while monitoring performance levels. Data was taken at several intervals, with the last being at 550 Hz with a phase voltage of 140V rms. At this source voltage level, with a modulation index of 0.65, the dc-bus achieved 313.4V with a 5.85kW load. When source voltage was increased beyond this point there was a third diode failure (again, likely due to the lack of snubbers) and three-phase testing could no longer continue due to the lack of operational Powerex modules. Performance results for the highest power achieved in three-phase mode are included in Figs. 58, 59, and 60 in the form of Oscilloscope screen captures. A simple voltage-control scheme was utilized in this initial

testing with the modulation set to 0.65 rather than having the model modulate based on the dc-bus voltage. It should be noted that there was no power factor correction implemented in this simple control model, and thus a significant phase delay in the input current was present.

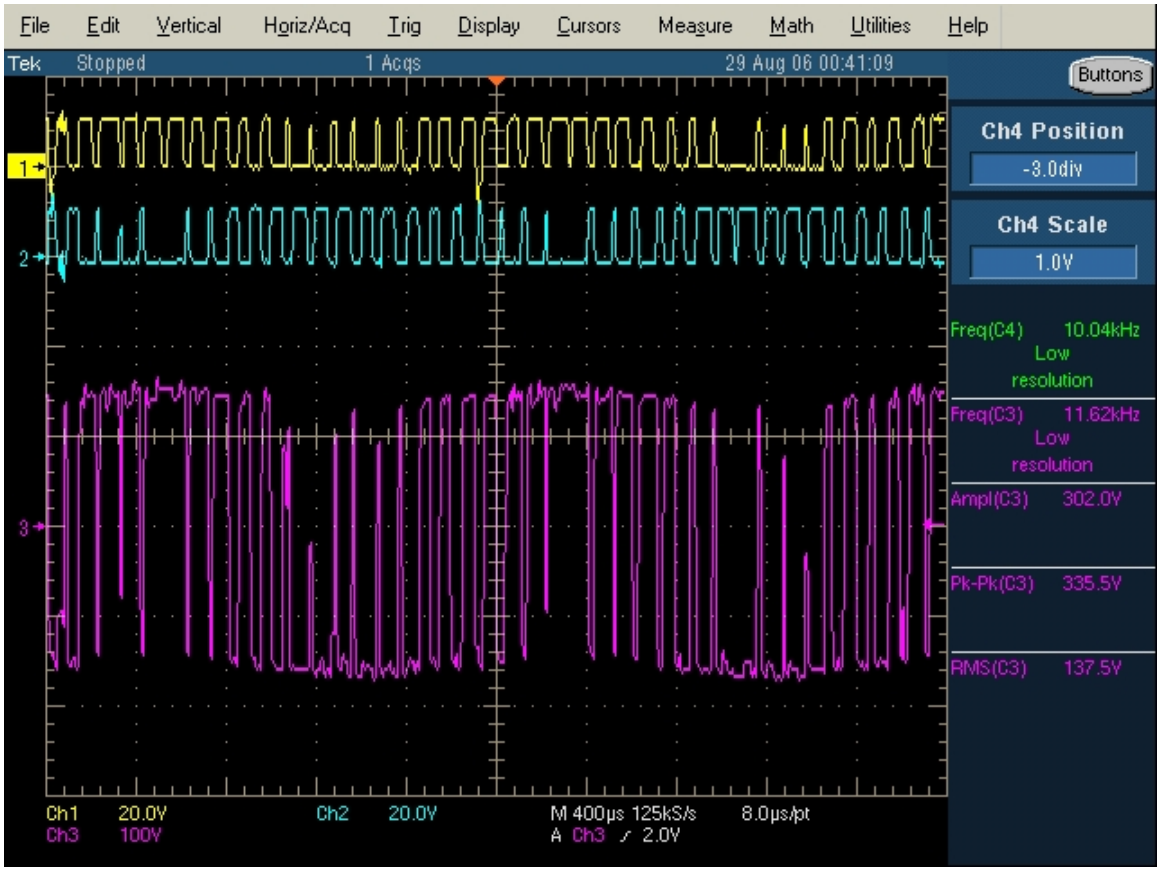


Fig. 58 – Phase A gating signals and phase A voltage at rectifier input. (Note: the sampling rate was decreased to enable clear observation of the input voltage waveform, thus not "catching" the voltage spikes produced by the lack of snubber circuits.)

The first scope capture, shown in Fig. 58, contains the gating signals controlling the IGBTs on the rectifier leg connected to phase A. Channel 1 shows the gating signals for the IGBT connected to the positive dc-bus and channel 2 contains those for the complimentary IGBT connected to the negative dc-bus. Channel 3 displays phase A voltage at the rectifier input, clearly showing the pulse width modulation. As shown, gating signal dead time is sufficient to eliminate the simultaneous firing of complimentary IGBTs, which would cause shorting of the dc-bus.

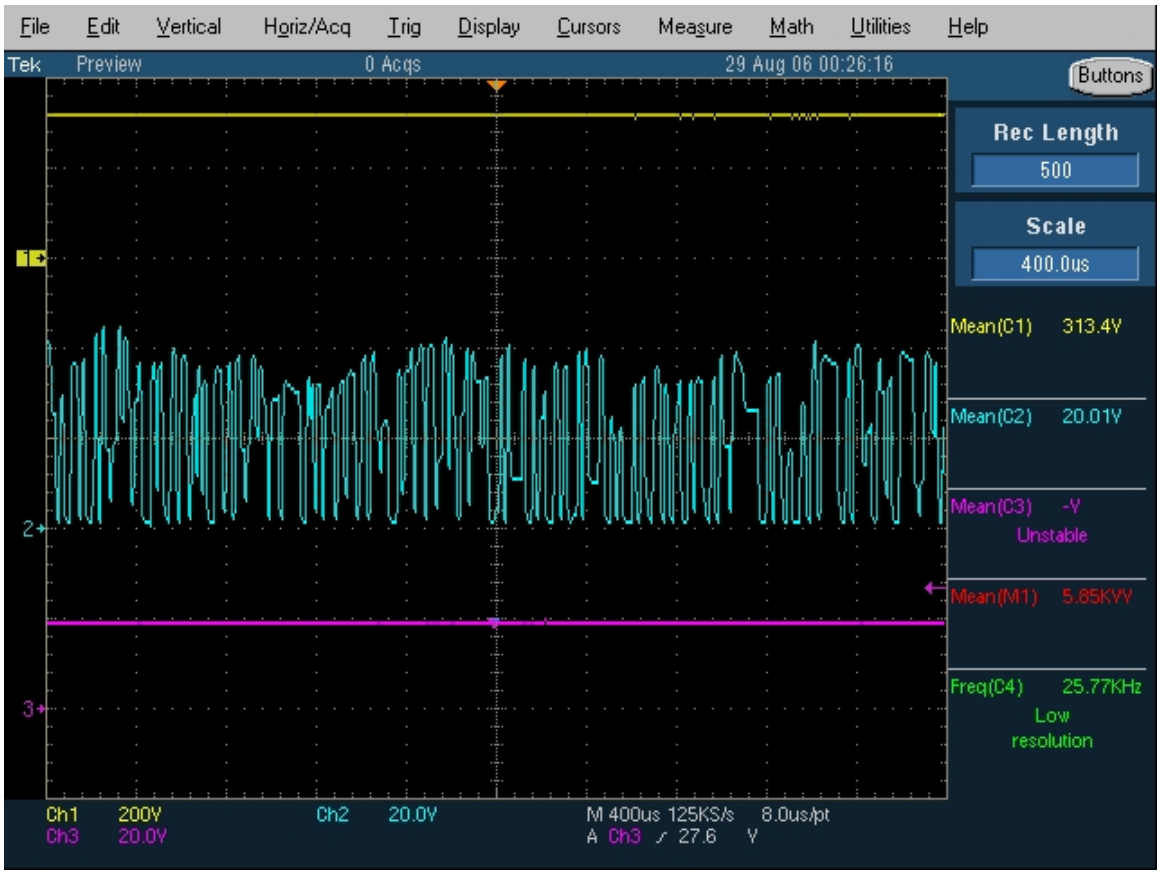


Fig. 59 – Dc-bus measurements.

Dc-bus measurements are shown in Fig. 59 above. Channel 1 displays dc-bus voltage, channel 2 displays current at the input of the dc-bus capacitor bank from the bridges, and channel 3 displays current from the capacitor bank to the resistive load. As shown in the measurements, the dc-bus voltage level is 313.4V, power dissipated to the resistive load is 5.85 kW, and the average dc current is 20.01A. As shown by channel 2, there are no negative current spikes apparent between the bridges and the dc capacitor bank, which would indicate dc-bus shorting through the switches, or other switching errors.

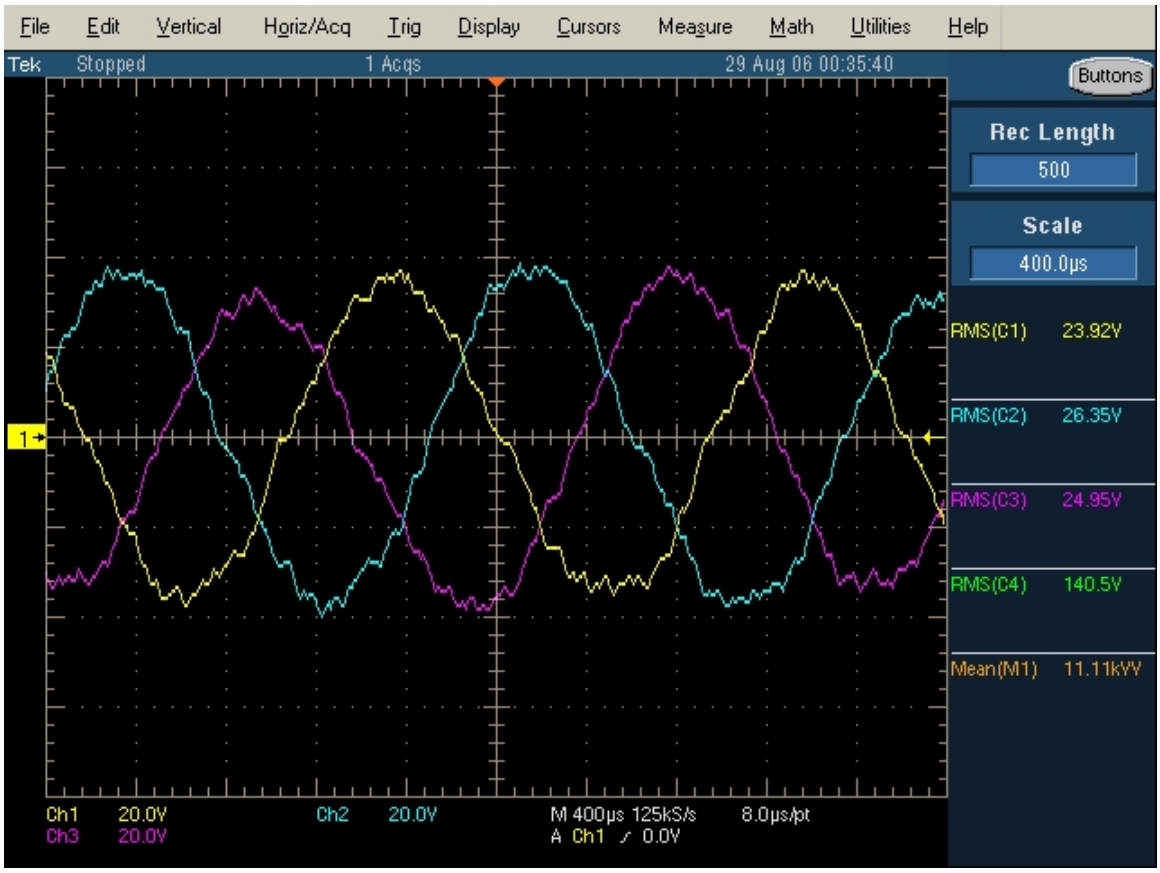


Fig. 60 – Input phase currents.

As shown in Fig. 60, the control scheme was producing sinusoidal currents at the rectifier input. The switching frequency of 10 kHz was high enough to achieve good modulation and there were balanced currents drawn from each of the three phases. Measurements at the right panel of the screen capture display the rms phase currents of approximately 25A, rms phase voltage of 140.5V, and total power delivered by the programmable source of 11.11 kVA. It should be noted; the high power discrepancy between the source and the dc-bus is due mostly to poor power factor achieved with simple voltage control, with a small amount of switching loss present.

# 6. CONCLUSIONS

Active rectifier performance was analyzed with a high frequency permanent magnet synchronous generator for use in hybrid electric vehicle applications. Initial investigations utilized simple voltage control with results compared to standard diode rectification in Matlab Simulink simulations. Generator phase configurations of three-phase wye, six-phase wye, and six-phase independent were simulated with symmetric phase spacing in all configurations. Subsequently, current-control was investigated in the updated generator configuration specifications of 2x3-phase wye and six-phase independent with two separate, synchronous three-phase winding sets. This current-control scheme offered excellent performance in both generator configurations, achieving high power factor with sinusoidal input currents for reduced harmonic content. Harmonic analysis was performed on the input current and output dc-bus voltage showing low THD in both the 2x3-phase wye and, with the use of offset gating, the independent phase configuration.

Hardware testing was conducted utilizing Powerex Pow-R-Pak H-bridge modules for the power electronic devices. A three-phase 120 kVA fully programmable source was used in representing the high frequency permanent magnet synchronous generator. Two transformers were connected at its output to produce two synchronized three-phase connections similar to those of the 2x3-phase wye generator configuration. Gating signals and modulation control were provided by an Opal-RT HILbox real-time hardware simulator running versions of the Matlab Simulink control schemes used in previous software simulations. Initial hardware results showed excellent modulation with highly sinusoidal input currents being drawn by the active rectifier before diode failures prematurely ended testing. These failures were most likely caused by high voltage spikes at the rectifier input, which were the result of high frequency switching in the absence of protective snubber circuits.

Future work could include investigation of adequate protective snubber circuits and advancement to higher power hardware testing. The implementation of more fault-tolerant control schemes for each generator configuration could be carried out, as well as hardware testing with performance analysis under both generator and rectifier fault conditions. Harmonic mitigation techniques could be investigated for the further reduction of harmonics in both the input and output of the active rectifier. Finally, additional equipment could be implemented for testing of the entire hybrid electric vehicle system; this includes generation, rectification, auxiliary dc loads, and traction drives and motors.

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