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Modern wireless System-on-Chips (SoCs), such as mobile handsets, sensor networks, and mm-wave systems, integrate an entire RF system on a single CMOS chip. Such highly complex systems require significant on-chip digital signal processing to help improve the performance of highly sensitive analog/RF components. The IC market being competitive, the ability to achieve first pass silicon success is crucial, due to very high processing and testing time cost. Unfortunately, the ability to achieve first-pass silicon success is becoming increasingly more difficult, due to higher system complexity, higher frequency of operation, increased performance requirements, and higher process skews.

This thesis presents a 2.4 GHz, reconfigurable RF Low Noise Amplifier (LNA) using on-chip peak detection and calibration, to mitigate the deleterious effects of process, voltage and temperature (PVT) variations. The LNA can reconfigure its input impedance matching, as well as its gain. On-chip detection of optimal input/output impedance matching is performed using an amplitude peak detector. A low power, robust maximum peak point calibration scheme is proposed that cali-

brates the LNA to the resonant frequency of interest. Measurement results show that the calibration of the LNA improves the input matching (S_{11}) by a maximum of 5 dB , and power gain (S_{21}) by 3dB, while not significantly degrading the Noise Figure (NF).

A Self-Calibrated, Reconfigurable RF LNA

by

Karthik Jayaraman

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APPROVED:

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Dean of the Graduate School

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Karthik Jayaraman, Author

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1. INTRODUCTION

1.1. Background

Portable communication applications like mobile handsets require the presence of an entire radio frequency (RF) system on a single chip. The advent of submicron MOS technologies makes it possible to use CMOS circuits in RF regime. Integration of RF system in CMOS technologies has the advantage of low cost and high degree of functionality on the same chip. Besides ensuring the presence of other important blocks of a typical transceiver architecture like mixer, oscillator, synthesizer, phase locked loop (PLL) etc., one of the most important requirements lies in design of a high performance low noise amplifier (LNA). Requirement of LNA becomes far more significant considering the fact that, amplitude of the signals received in the applications like Global Positioning System (GPS) is extremely small. This low level further degrades in the presence of physical obstructions such as buildings and trees. Hence, there are certain stringent requirements on the design of the LNA, like minimizing the noise figure, providing gain with sufficient linearity typically measured in terms of the third order intercept point,IP3, and providing a stable 50 Ω input impedance.

1.2. Motivation

As CMOS technology migrates to deep submicron transistor lengths, the sensitivity of circuits towards process, voltage and temperature (PVT) variations in-

creasingly degrades the RF circuit performance. This makes the design of sensitive analog/RF circuits in these technologies extremely difficult. In addition, the foundries that manufacture such integrated circuits have a difficult time in predicting the process skew and variation of devices, as the technology has little time and low manufacturing volume to improve robustness. The limited modeling information and the modeling uncertainties often lead to over-design of the RF section. However, the modeling of these uncertainties are not fool-proof and may not accurately bound the variations. The extraction of passive devices and their parasitics, which often play a significant role in the performance of the chip, is difficult due to the higher operating frequencies and close spacing of the wire interconnects. For example, on-chip spiral inductor characterization requires 3D field solvers to estimate the parasitics which is again tedious and often inaccurate. Moreover, testing occupies a major percentage of the total cost and total time and needs to be minimized.

The LNA is the first block in a radio receiver. Its performance is vital, as it amplifies low power signals from the antenna input to a realizable practical level. The stringent requirements of the LNA are low noise, high forward gain, high linearity, a well-defined input impedance (to match the preselect filter preceding the LNA) and low power consumption. In order to achieve all these important metrics across significant process uncertainty, it is desirable to detect any deviation from the optimal performance using built-in self test (BIST) methods, and then provide a corrective measure to recalibrate the LNA to the optimal performance possible. One of the most important requirements for the LNA is accurate impedance matching, especially of the input reflection coefficient (S_{11}). S_{11} is critical for it also determines the forward gain (S_{21}) of the LNA. The possible factors that can affect S_{11} and S_{21} are detailed below.

1. Variation of on-chip inductor and capacitor values across corners (min,typ,max).
2. Variation of inductance due to bond wire.
3. Temperature variation (-50°C to 70°C).
4. Transistor corner variation (Slow-Slow (SS), Typical (TT), Fast-Fast(FF)).

The first two non-idealities may significantly degrade the frequency of the impedance matching, while the temperature/transistor variations negatively affect the gain of the LNA. In the case of a bond wire used for the input matching, the bond-pad capacitance can reduce the effective bond wire inductance. For low frequencies, this problem can be compensated for post-tapeout by increasing the bond wire length [3]. Considering the effect of all these variations together, the worst case parameters of a conventional 2.4 GHz LNA are shown in Fig. 1.1. Here, 'TT' is the nominal case with no variation, 'SS' is the 'slow-slow' corner with -10% V_{dd} @ +70°C, and 'FF' is the 'fast-fast' corner with $+10\%$ V_{dd} @ -50°C. The worst case, input resonant frequency variation is from 2.2 GHz-2.6 GHz, while the output tank resonant frequency variation is from 1.95GHz-2.5 GHz. This variation in the input and the output resonant frequencies causes the (S_{11}), (S_{21}) and the noise figure (NF) of the LNA to degrade. This is shown in Fig. 1.1. The degradation of the input match is the most affected, with a worst case 8 dB degradation.

1.3. Narrowband Vs Wide band RF LNA

In this work a narrowband 2.4 GHz LNA is designed which accounts for PVT/bond wire variations as opposed to going for a wideband LNA design and

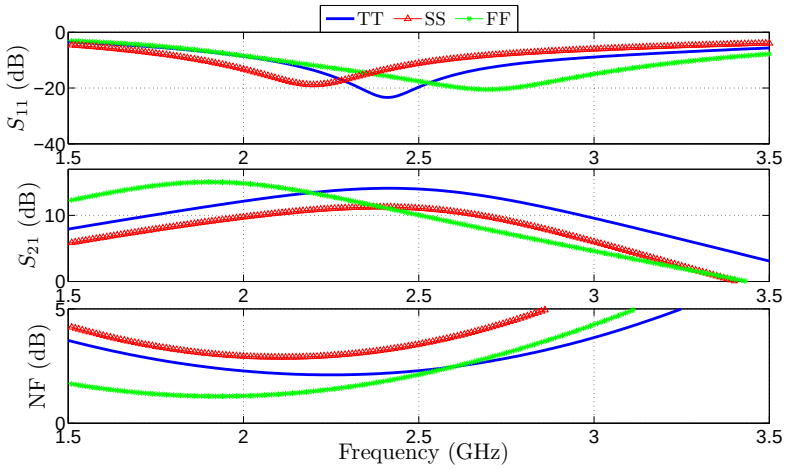

FIGURE 1.1: PVT Variations on a conventional 2.4 GHz LNA

automatically satisfying the specifications across various corners. This approach is adopted because designing a wideband LNA consumes more power as compared to a narrowband LNA. This is because the bias voltage and the width of the transistors need to be increased to have a broadband input matching with minimum noise figure. The input impedance matching in a wideband LNA is done using a bandpass filter structure necessitating the use of extra passive devices which will increase the die area. Achieving simultaneous input and noise matching (SINM) has been an active area of research for wideband LNAs and is difficult. A lower SNR requirement translates to a smaller power amplifier (PA) output power in a transceiver. Lowering the output power of the PA not only reduces power consumption, but also increases linearity due to the operation. Also when operating in a wide band there are chances to pick up interferers which could be problematic. Though the issue of narrowband Vs wideband LNA is double edged, this work has adopted the narrowband approach due to the aforementioned reasons. Table 1.1 compares and contrasts the narrowband approach with the wideband approach, in building a RF

TABLE 1.1: Wideband LNA Vs Narrowband LNA

Block	Wideband	Narrowband
Antenna	High efficiency matched antenna over wide range is difficult. LNA and antenna should be co-designed.	Small, high efficiency,high Q antennas easily achievable.Antenna and LNA can be separately designed.
RF Front End	Wideband LNA has high power dissipation. VGA design is difficult especially at top of band. Rx linearity may be tough given the limited filtering. Stability can be a problem with high gain levels in a single wide band.	Low power consumption, stable Rx blocks. Tough transmit mask to be delivered,high Tx linearity for OFDM.
Mixed Signal	Very high bandwidth ADCs,power consumption issue. Extended time sampling techniques and digital sampling oscilloscope techniques.	Small bandwidth A/D converter (typically twice the data rate.
Other Issues	In band, on-chip noise sources.External CW interferers.	LO leakage. Narrowband rayleigh fading.

transceiver.

The theme of this work is to build a reconfigurable LNA, enabling the ability to tune the LNA to the desired frequency of interest (2.4 GHz) in the case of a resonant frequency shift due to PVT/bond wire variations . The detection of this frequency shift on-die, non-invasively, is a critical requirement for calibrating the LNA. The amplitude detector used in this work is both area/power efficient. It is robust, capable of translating the frequency matching information of the RF signal into DC, such that it can be processed in the digital domain. The detection is aided by the presence of an on-chip frequency synthesizer that is tunable across the frequency range of interest (2GHz-2.7GHz), thereby providing the excitation source.

A novel maximum peak point calibration technique is proposed, including the on-chip detection and calibration algorithm. The measurement results indicate the reconfigurable nature of the LNA amidst variations. The feature of dynamic power supply scaling is also discussed, where the power supply of the LNA is changed dynamically. Though this degrades the performance of the LNA, the automatic detection/calibration helps correct for these variations by tuning the input/output resonant frequency. This method trades gain for power consumption and can be used in short range, low power applications. This dynamic power supply scaling technique can also be extended to power amplifiers (PAs) which can help obtain better efficiencies with low power. All these benefits makes the proposed technique suitable for deep submicron RF/mixed-signal SoC design.

1.4. Thesis Outline

The thesis is organized as follows: Chapter 2 gives an overview of the past work that has addressed the problem of resonant frequency shift in the LNA, their advantages and disadvantages. This chapter gives a broad picture of the different solutions that have been proposed, their shortcomings and advantages. Chapter 3 details the proposed reconfigurable RF LNA architecture, in a system level perspective. Chapter 4 gives insight into the circuit level implementation of the LC VCO, LNA and other internal blocks of the system. It talks about the various design tradeoffs that were considered in the design. Chapter 5 discusses the measurements results and summarizes the effectiveness of the reconfigurable LNA.

2. AN OVERVIEW OF DETECTION SCHEMES IN LNA

2.1. Introduction

The wireless industry is making rapid strides and churning out a number of standards and applications. With the design in the sub-micron processes greatly affected by PVT and bond wire variations, it is mandatory to have a robust, cost effective detection scheme for various wireless blocks. Modern transceivers being integrated systems involving diverse specifications and components at very high frequencies of operation, makes the detection complex and expensive. Addressing this problem, there have been several efforts including defect modeling, automated test algorithms, design for test (DFT) techniques, and BIST techniques. The detection of RF LNA performance requires an efficient architecture, with the target requirements being the following.

1. High input impedance at the frequency of interest to prevent loading and performance degradation of the RF circuit under test.
2. Minimal area overhead.
3. Low power consumption.
4. Robust and less complex.

In this chapter, the main focus will be on the RF LNA detection/calibration schemes.

The objective of self-correction of the LNA, necessitates the following four steps.

1. The sensing of a signal which is indicative of the input/output tank match of the LNA.

2. Process this signal appropriately to relate it to the input/output match of the LNA.

3. Use this information to send a signal to the LNA to correct for the variation.

4. Finally to provide for a mechanism in the LNA which can adaptively change in real time based on the aforementioned feedback signal.

2.2. Various architectures for LNA detection/calibration

2.2.1 Resistive sensing of input resonant frequency mismatch

Sensing the input match is done through a small valued resistor, placed at the source of the input transistor [15, 16]. The voltage generated as a result of the mismatch in the current is indicative of the input frequency of the LNA. The current variations in the LNA due to a shift in the input match are of small magnitude (few μA)[17]. The resistor value used is small, 7 Ω, and so the voltage sensed needs to be amplified before processing. The peak-to-peak amplitude of this voltage contains the input match information and needs to be converted to dc. The amplitude of the test signal, in this case can be higher than the conventional input signal amplitude to the LNA, but needs to be within the linearity and dynamic range limits. This signal is input to a peak detector which outputs a dc signal proportional to the

input match of the LNA.

For a given input match, the spectral output of this sensor chain is a steadily decreasing monotonic (almost linear) curve as frequency increases. The current in the LNA and hence the sensed voltage varies monotonically with the input match. A two-tonal approach was developed, by inputting two frequencies on either side of the frequency of interest. Based on the two outputs recorded, the gate inductance value was modified using a tapped inductor technique. Based on which switch is turned on, only one tap of the coil will be shorted to the input pad of the LNA, and this tap determines the input match of the LNA. This significantly degrades the noise figure by adding the switch thermal noise to the overall noise figure. The disadvantages of this architecture are summed up below.

1. Current sensed and converted to voltage where the baseband processing is done.

2. The resistor used to sense the current, in series with the inductor will degrade the Q_{input}, though not by much as it a 7Ω resistor. It creates a parasitic capacitance from the source inductor terminal to ground which could possibly have an effect on the resonant frequency.

3. A two tonal test is performed each time and depending on the result of these, the inductor value is switched. This is not necessarily the simplest way of sensing the resonant shift and the switches used for choosing a different inductor value adds thermal noise. This degrades the SNR at the input, increasing the noise figure.

4. Two independent schemes have to be used for tuning the input resonant frequency and the output resonant frequency shift, which will be again be an

overhead to the design.

In this work the voltage sensed at the output of the peak detector is directly used to monitor and correct for the input match. This work does come up with a less intrusive and minimal overhead method to do the sensing of the input resonant frequency shift.

2.2.2 Switched loop-back architecture using Peak Detector

The transmitter and receiver chains are linked using a loop back connection and it is one of the early strategies devised for testing wireless and wire-line communication systems. It eliminates the use of an external stimulus, and is effective in detecting catastrophic faults. A similar loop back topology has been implemented and a peak detector is used for the detection [18]. The peak detector topology (common source stage) has a high input capacitance and does load the LNA. The calibration is done using an ADC and the digital signal processing blocks that follow. The block diagram of the implementation is shown in Fig. 2.1. This topology uses only one peak detector to correct for the variations in the input and output resonant frequency shift. The results reported in this work are simulation results and not post silicon.

2.2.3 CMOS RF RMS Detector

A CMOS RF RMS detector for enabling BIST for wireless applications is proposed in [4].It generates a DC signal proportional to the RMS voltage amplitude of the RF signal. It has high input impedance, coupled with small input capacitance and small silicon area, making it suitable for the testing of critical RF blocks of a transceiver. RF RMS detectors [4, 5] and RF power detectors [6, 7, 8] generate

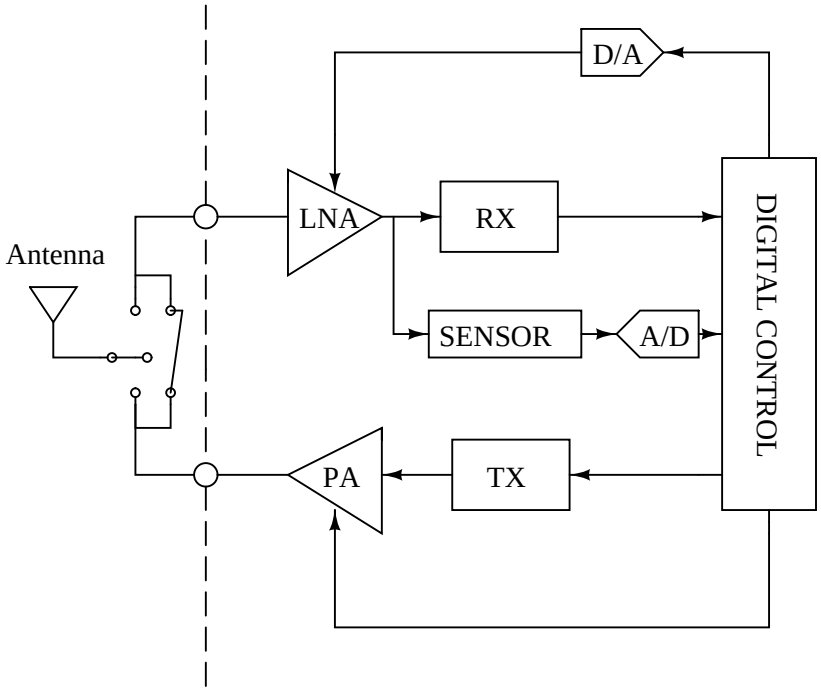

FIGURE 2.1: LNA detection and calibration using switched loop back architecture.

a DC voltage proportional to the amplitude and power of an RF signal, respectively. The performance metrics of the RF blocks such as gain, output power and 1dB compression point are tested with reasonable accuracy by measuring the DC voltages. Power dividers to connect matched RMS detectors to the RF signal path is implemented in [4, 9]. This is not a suitable detection scheme for an integrated transceiver as the performance is affected due to loading and moreover the power dividers increase the area overhead. The model of the RF RMS detector [4] consists of an amplifier with high input impedance followed by a half-wave rectifier and a 2^{nd} order low pass filter. An RF RMS detector is used at the input of the LNA and another at the output. The amplitude of the sinusoidal signal at the input of the LNA (and the first detector) is swept from -20 to 0 dBm in steps of 2 dBm. For a

TABLE 2.1: RMS Detector Performance Summary

Parameter	Value
Gain	60 $\frac{mV}{dBm}$
Area	0.0135 mm^2
Supply Voltage	3.3 V
Power Consumption	10 mW

given input amplitude, the gain of the LNA can be measured as the distance in dB from the response of the detector at the output to the reference response (output of the detector at the input)[4]. Table. 2.1 gives the RMS detector performance summary. A calibration/correction scheme is not proposed in this reference work and this mainly deals with the detection.

2.2.4 Power Detectors

A half wave rectifier, using a diode is the basic form of a power detector . The diode characteristic is non-linear, the diodes pass the positive half cycle completely and do not completely block the negative half cycle. The absence of a sharp cutoff point, causes a small window of the negative cycle to pass through. This results in a non-linear input/output characteristic for the overall detector. Though the current rectification method has a good linearity, it is not suitable for high frequency input signals [6, 10]. Piece wise linear (PWL) detectors are used to measure signal amplitudes spanning large dynamic ranges [6, 8, 11, 12]. [6] uses a power detector which has a dynamic range of more than 25dB within +/- 0.5dB accuracy, but is placed in the die along with the power amplifier in a BiCMOS process. [13] uses

a built in current sensor (BICS) along with two built in power sensors (BIPS) to detect the performance of the LNA. To ensure the accuracy of the bias current extraction, a calibration procedure is performed using several MOS transistors that is an overhead to the LNA (DUT) in terms of the noise added. The proposed power sensor is composed of two building blocks, namely the the amplitude detector and the log amplifier. The role of the amplitude detector is to convert the input voltage amplitude into a proportional dc voltage V_{out}, whereas the log amplifier transfers the V_{out} into logarithmic scale. To avoid loading of the DUT, a voltage divider with large resistance values is inserted between the port and the amplitude detector. This causes huge area penalty and adds noise which is not acceptable to the LNA.

2.3. Conclusion

From analyzing the past work done in the field of detection/calibration of variations in the LNA, two of them have the complete detection/calibration scheme. The two of them are the " Resistive sensing of input resonant frequency mismatch " and " Switched loop-back architecture using peak detector ". The latter uses a similar architecture to the one proposed in this thesis, though the detection/calibration schemes vary. The detection is done using a different peak detector topology (common source), while the calibration is done using switched loop back architecture. This work only reports simulation results and does not give details about the linearity and the power consumption of the LNA. The former uses resistive sensing and converts the variation of change in current to voltage. A two tonal calibration approach is followed that calibrates the LNA to the resonant frequency of interest. This work however only talks about the calibration of the input match and another

dedicated scheme has to be used for the calibration of the output tank resonant frequency. The work implemented in this thesis tries to overcome the shortcomings of the past work, yet retain its advantages and create an effective automatic LNA calibration system.

3. PROPOSED RECONFIGURABLE RF LNA

3.1. Introduction

Detection and calibration of LNA performance in RF transceivers has been an important research area [17, 18]. The area overhead of the detectors used in a transceiver should not entail a significant portion of the overall die area. This is because large input loading may negatively affect the impedance matching performance of the LNA. In addition, the power overhead of including the detector for measuring LNA performance should be minimal [4]. The calibration procedure should also be area/power efficient and fast. This chapter details the proposed reconfigurable RF LNA from a system level perspective. Section 3.2 highlights the system level overview of the proposed scheme. Section 3.3 explains why voltage detection can be used effectively for improving the input matching, followed by Section 3.4, which gives insight into the peak detector used for the translation of the RF signal to DC. Section 3.5 talks about the proposed reconfigurable input match, followed by Section 3.6 which deals with the tuning of the output tank circuit. Section 3.7 helps understand the maximum peak point calibration technique.

3.2. Proposed Detection and Calibration

An overview of the detection and calibration scheme that is used in general for correcting LNA performance is detailed below. This procedure has to be followed to correct for the input and output resonant frequency shift. Figure 3.1 highlights

the detection/calibration scheme from a system level perspective.

1. Detect the deviation from the optimal LNA performance using a suitable on-chip detector.

2. Relate it to a particular parameter of the LNA that can be used to control it.

3. Calibrate the LNA by tuning the relevant parameter to adjust for the deviation.

4. Stop the calibration when the best optimal performance is reached.

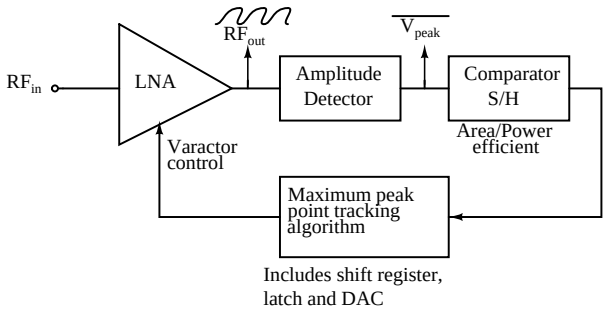

FIGURE 3.1: Proposed detection and calibration for reconfigurable LNA

The proposed detection scheme overcomes the limitations of the other detection schemes by reducing the detector complexity, die area, and power consumption. The calibration is performed using the maximum peak point tracking method, which corrects for variations in the input and output resonant frequencies. This is done by sensing the frequency shift at the input/output tanks and accounting for it by tuning the input and output resonant networks. The exact mechanism used for the calibration is detailed in the later sections.

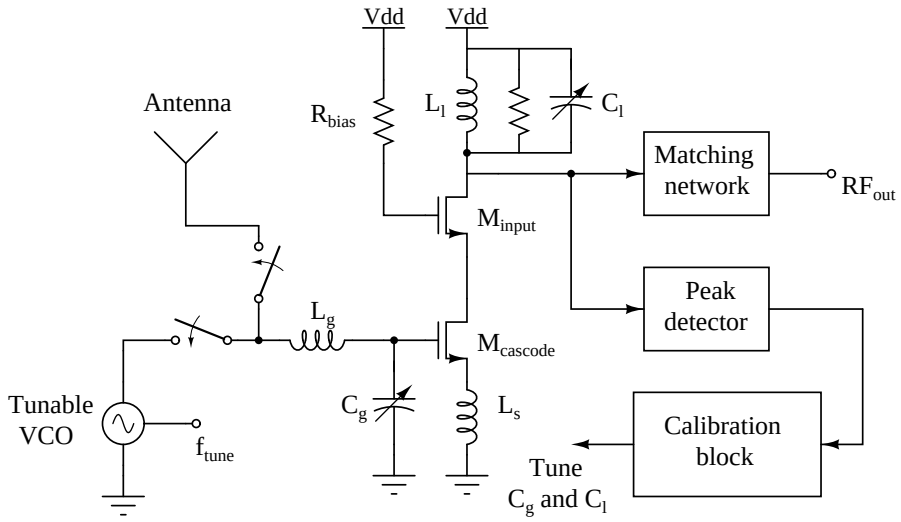

FIGURE 3.2: Reconfigurable LNA topology

3.2.1 Calibration Algorithm

The calibration is performed in the order stated below. When the output load is matched to the best possible accuracy, setting the input match, results in maximum power gain (S_{21}).

1. The LNA is input a fixed sine-wave (frequency of interest) using the on-chip tunable VCO.

2. The RF to DC conversion is done by the peak detector which is placed at the output load tank network.

3. The output tank varactor C_l is tuned and the output of the peak detector is measured. Set C_l for which the maximum amplitude is measured.

4. The input tank varactor C_g is tuned and the output of the peak detector is measured. Set C_g for which the maximum amplitude is measured.

5. Terminate the calibration algorithm once optimal performance is reached.

This gives a high level understanding of how the system functions. In this work, the calibration loop is made simpler and more power efficient by replacing the ADC with a comparator, as well as integrating digital circuitry and a DAC to perform the job of correcting for any process variations. The calibration loop was done off-chip, during the measurements, but was first simulated with the maximum peak point calibration algorithm.

The theme is to use a single peak detector to detect the variations in the resonant frequencies of the input and the output tanks. As the peak detector is placed only at the output tank node, it is hard to see how the input tank frequency variation can be captured. The next section explains the aforementioned fact.

3.3. Maximum voltage gain with best input match

To illustrate this fact, a generic two-port network analysis using S parameters is done. This is shown in Fig. 3.3. The S parameter analysis helps understand why having the best input match results in maximum voltage gain. Maximum voltage gain signifies that the detector at the load tank can indeed detect the input resonant frequency variation. The signal flow graph of the two port network is shown in Fig. 3.4 [22].

$$S_{11} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{3.1}$$

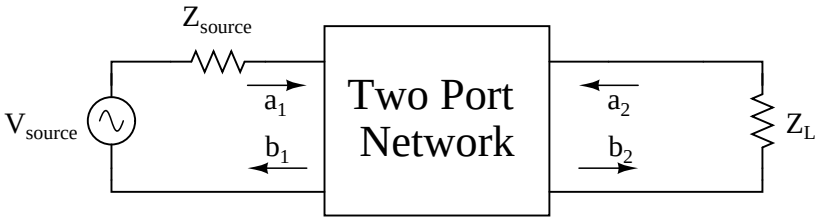

FIGURE 3.3: Two port network analysis using S parameters

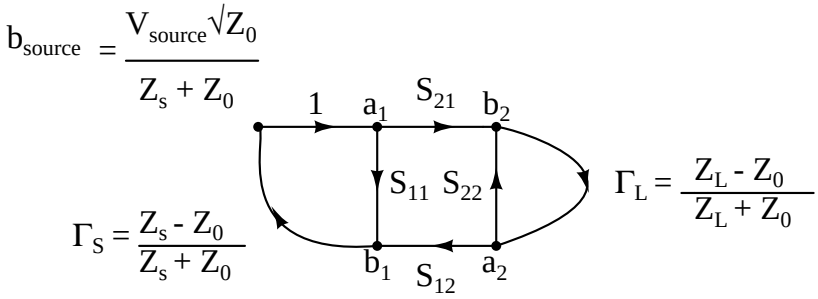

FIGURE 3.4: Signal Flow Graph for the two port network

where,

$$Z_1 = \frac{V_1}{I_1} \tag{3.2}$$

$$S'_{11} = \frac{b_1}{a_1} = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.3}$$

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.4}$$

Voltage gain with arbitrary source and load impedances,

$$A_v = \frac{V_2}{V_1} \tag{3.5}$$

$$= \frac{b_2(1 + \Gamma_L)}{a_1(1 + S'_{11})} \tag{3.6}$$

$$= \frac{S_{21}(1 + \Gamma_L)}{1 - S_{22}\Gamma_L(1 + S'_{11})} \tag{3.7}$$

Under matched load conditions, (i.e) output matching $\Gamma_L = 0$,

$$A_v = \frac{S_{21}}{(1 + S'_{11})} \tag{3.8}$$

$$= S_{21}\ when\ S_{11}\ \rightarrow\ 0. \tag{3.9}$$

The voltage gain is maximum when the input match is optimal, when the S_{11} magnitude value is the smallest, indicating minimal input reflections. Detecting the input match can be performed by tuning the input varactor control and measuring the output voltage of the peak detector.

3.4. Detection of LNA performance

RMS/power detectors [4, 6] detect the power of the RF signal, to enable the LNA calibration. The detector in [4] uses a high input impedance and low input capacitance, thereby minimizing the loading of LNA. This feature coupled with small area, makes this detector ideal for BIST. In [6], a power detector is used which generates a DC signal proportional to the RMS voltage amplitude of the RF signal. An end-to-end strategy connecting the output of the transmitter to the input of the receiver through a loop-back connection has been implemented in [20]. Peak detection has been used in [18] which senses the peak amplitude of the RF signal and converts it to DC. Here, a common source amplifier has been implemented as the sensor, minimizing the voltage swing at the source and the drain of the common source, eliminating the miller effect. Unfortunately, this has the disadvantage of high input capacitance and will load the LNA (DUT).

The proposed detector, detects amplitude level as opposed to power. The peak detector is designed using a source follower and an active load (or current source). The peak amplitude of the incoming RF signal, modified by the gain of the source follower, is stored in the output capacitor. The impedance of the active load/sink current determines the rate of discharge and hence the discharge time constant [19]. The advantage of the proposed peak detector is that it can integrate easily into the RF transceiver and multiple nodes can be observed from a single output pad.

3.5. Reconfigurable LNA Input Match

As observed earlier, the performance metric most affected due to PVT variations is the input resonant frequency shift. It is therefore important to analyze the conventional input match as well as the compensated input match, which integrates the reconfigurable capacitor array.

3.5.1 Conventional Input Match

The input match of LNA is very critical and influences the forward gain of the LNA. The input match is determined by both the active and passive devices of the input front-end. Figure 3.5 shows the small signal model of the conventional input match. It can be seen that at resonance the real part of the input impedance is determined by the g_m, (transconductance), of the input MOS , the parasitic capacitance C_{gs} and the inductance L_s. The resonant frequency is determined by L_g , L_s and C_{gs}.

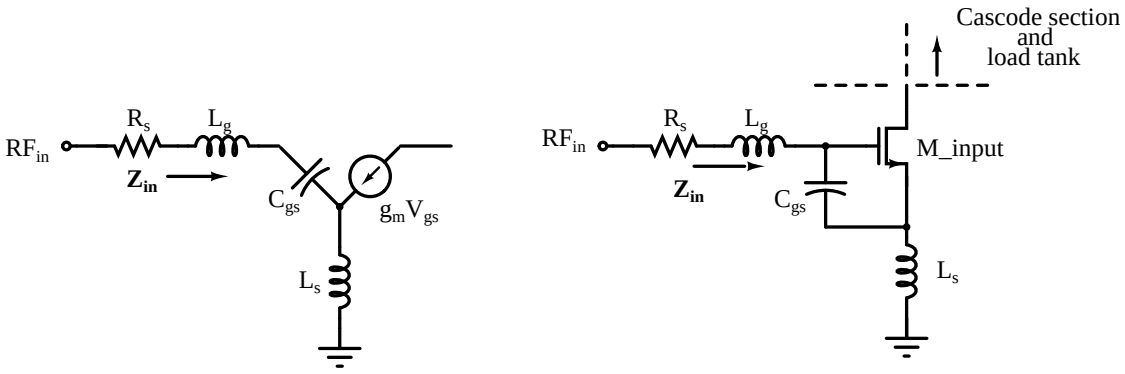

FIGURE 3.5: Conventional Input Match

$$\omega_0 = \sqrt{\frac{1}{(L_g + L_s)C_{gs}}} \tag{3.10}$$

$$Z_{in,real} = \frac{g_m * L_s}{C_{gs}} = \omega_T L_s \tag{3.11}$$

where, $\omega_T = \frac{g_m}{C_{gs}}$

3.5.2 Compensated Input Match

To correct this resonant frequency shift, three parameters can be altered, namely : L_g , L_s or C_{gs}. Since the value of L_s is usually very small, using it to tune the input frequency match is difficult. Tuning the input resonant frequency using a variable L_g suffers from the disadvantages of a series transistor switch, with the switch thermal noise causing increased noise figure (NF). Therefore, modifying C_{gs} to perform tunability is simplest and less invasive, as proposed in [18]. In this proposed work, the input match is modified further by adding a shunt varactor from V_g to ground as shown in Fig. 3.6 [2]. This is done based on the following intuition. At the gate node of the input MOS of the LNA, there is a certain amount of parasitic capacitance present. Part of it might come from the input bonding pad

and another part could stem from an ESD protection network at the input. This parasitic capacitor is going to alter the input series tank network. So why not take advantage of this fact and add an additional varactor at that node to do the compensation. This work exactly does that and achieves the tuning of the input front end.

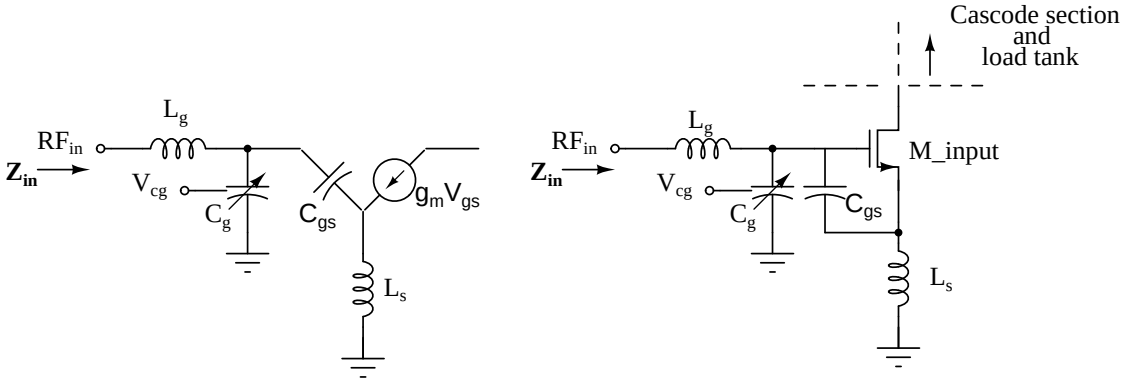

FIGURE 3.6: Reconfigurable Input Match

The choice of adding a varactor C_g, improves the tuning of the resonant frequency shift, by modifying the effective value of L_g. The variation in L_g modifies both the real and the imaginary parts. This is not necessarily a problem as varying C_g adjusts the real part of the input match (S_{11}), thereby calibrating the impedance by counteracting the imaginary part [2]. The net result of this tuning is that it improves the value of S_{11}, which is important, as the preselect filter that precedes the LNA in a receiver architecture is sensitive to its terminating impedance. The resulting modified impedances, due to the addition of the varactor C_g is given below. R_s gets modified to R_b and L_g gets modified to L_b, as shown in Fig. 3.7.

$$Z_{in}(\omega_0) = \frac{g_m L_s}{C_{gs} + C_g} - \frac{g_m \omega_0^2 L_g L_s C_g}{C_{gs} + C_g} \tag{3.12}$$

where ω_0 is,

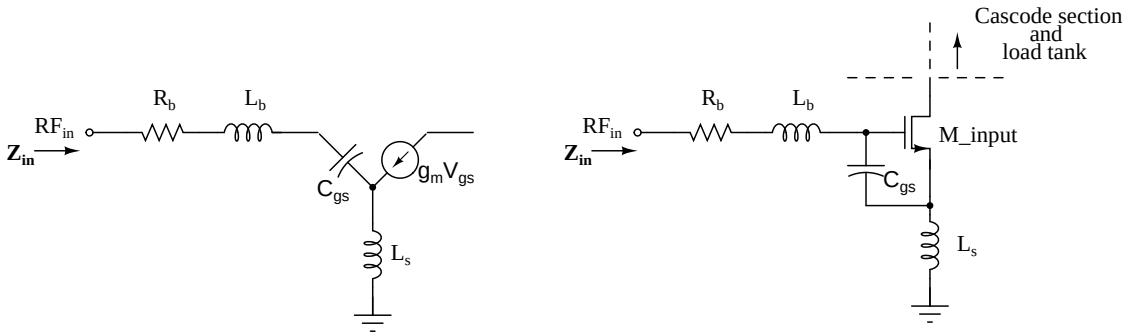

FIGURE 3.7: Modified Input Match

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs} + L_g C_g}} \tag{3.13}$$

$$R_b = \frac{R_s}{\omega_0^2 {C_g}^2 {R_s}^2 + (1 - \omega_0^2 C_g L_g)^2} \tag{3.14}$$

$$L_b = \frac{L_g - C_g(\omega^2 {L_g}^2 + {R_s}^2)}{\omega_0^2 {C_g}^2 {R_s}^2 + (1 - \omega_0^2 C_g L_g)^2} \tag{3.15}$$

There exists some tradeoffs that need to be taken into account when adding the varactor C_g. The introduction of the varactor C_g alters the source resistance,R_s and modifies it to R_b in this case, which is inversely proportional to the quality factor of the input (Q_{input}).

$$Q_{input} = \frac{1}{(R_b C_{gs} + g_m L_s)\omega_0} \tag{3.16}$$

Advantages of having a non 50Ω source resistance are,[36],

1. Power saving for the same Q of input network.

2. Power can be traded off with noise figure.

3. Noise contribution of the gate inductor is reduced.

4. Removes the need for lossy matching circuit between the antenna and LNA, when the antenna is designed at optimum R_s.

5. Ceramic filters, commonly placed between LNA and the antenna favour input/output impedance higher than 50Ω.

Some of the disadvantages are,

1. Equipment with non-50Ω impedance is required.

2. Fewer choices for off-the-shelf filters and antennas.

3. Noise contribution of LNA biasing network and substrate becomes dominant at high signal source resistance.

As the number the advantages in having a non 50Ω R_s, outweighs the latter there is not a huge tradeoff in altering the source resistance.

The initial value of R_b needs to be set, taking into account the noise figure requirements. Noise factor is a measure of how the the signal to noise ratio is degraded by a device.

$$NoiseFactor(F) = \frac{SNR_{IN}}{SNR_{OUT}} = \frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \tag{3.17}$$

where,

SNR_{IN} - signal to noise ratio at the input

SNR_{OUT} - signal to noise ratio at the output

S_{in} - signal level at the input.

N_{in} - noise level at the input.

S_{out} - signal level at the output.

N_{out} - noise level at the output.

Noise figure (NF) is the noise factor, expressed in decibels.

$$NF(decibels) = NoiseFigure = 10 * log(F) \tag{3.18}$$

The noise figure of the LNA is the ratio of the total noise output power to the output noise power contributed by the source resistance (R_s). The LNA is designed using the cascode topology, with inductive source degeneration. The NF for a inductively degenerated cascode LNA is given by [2].

$$NF = 1 + (\frac{\omega_0}{\omega_T})^2 \frac{\gamma}{\alpha} g_m R_b + (\frac{\omega_0}{\omega_T})^2 \frac{2\gamma}{\alpha\kappa} + \frac{\alpha\delta}{\kappa g_m R_b} \tag{3.19}$$

$$PCC = 4(\frac{\omega_T}{\omega})^2 \frac{R_b}{(R_b + R_{in})^2} \tag{3.20}$$

where,

ω_0 - resonant frequency of the LNA.

ω_T - unity current gain frequency.

g_m - transconductance of the input MOS of the LNA

g_{d0} - drain conductance with zero bias.

α - $\frac{g_m}{g_{d0}}$.

γ - coefficient of excess channel thermal noise.

δ - coefficient of gate noise.

κ - coefficient of the drain noise and correlated part of the gate noise

It can be seen that as ω_T increases, the drain noise contribution to the overall noise figure decreases for constant ω_0. The noise figure equation proves that there is a minimum NF, as one term in NF is directly proportional to g_m whereas the other term is inversely proportional to g_m. There is an optimum width of the transistor for a given current that will result in minimum NF. The value of R_b needs to be close to the value at the inflection point where the NF is a minimum, which is obtained by differentiating the NF with respect to R_b. For the case where $R_b \geq R_{in}$, the power to current gain (PCC) improves with Q_{input} and the noise degrades, though not significantly.

$$R_b = (\frac{\alpha\omega_T}{g_m\omega_0})\sqrt{\frac{\delta}{\gamma\kappa}} \tag{3.21}$$

The capacitor C_g that is added for tunability modifies the noise figure of the LNA, as the quality factor of the input matching circuit (Q_{input}) is changed. There are several ways to accomplish 50 Ω termination, like the resistive match,common gate topology, etc , but using the common source with inductive source degeneration gives the least NF [25]. The largest reduction in the channel current noise is obtained by increasing the Q_{input} of the input tank circuit. However, the inductive source degeneration topology is sensitive to gate-induced current noise, which is proportional to Q_{input} [21]. So reducing the Q_{input} using the C_g varactor will increase the channel current noise, but also help reduce the gate induced noise. Therefor the noise figure does not degrade by much. Hence, there exists a tradeoff in the Q_{input} value for the noise optimization. The plot of variation in Q_{input} with the variation in C_g is shown in Fig. 3.8.

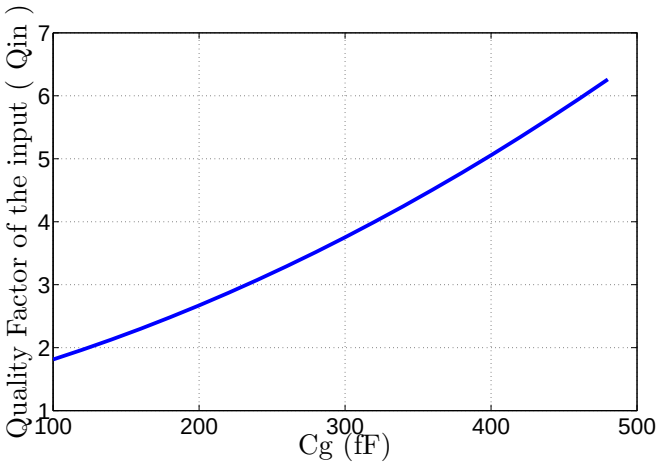

FIGURE 3.8: Quality factor (input) variation with C_g

The Q_{input} is set around 4.5 to optimize the noise figure. This is detailed in the noise optimization technique section in Chapter 4, (section 4.3.4). For $C_g \leq$ 340 fF, the Q_{input} decreases and for $C_g \geq 340$ fF, the Q_{input} increases, and thereby makes the input match more narrowband.

3.6. Tunability of the LNA output

The load tank of the LNA is also subject to resonant frequency shift due to PVT variations. The resonant tank at the load determines the output matching as well as the power gain of the LNA. Detecting the resonant frequency shift is also performed by measuring the amplitude peak of the peak detector that is placed at the output tank.

$$G_m = g_m \frac{v_{gs}}{v_{in}} \tag{3.22}$$

where G_m is the overall transconductance,

$$\frac{v_{gs}}{v_{in}} = \frac{\frac{1}{j\omega C_{gs}}}{R_b + jw(L_b + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s} \tag{3.23}$$

$$\frac{v_{out}}{v_{in}} = g_m \frac{\frac{1}{j\omega C_{gs}}}{R_b + jw(L_b + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s} Z_{load} \tag{3.24}$$

At resonance,

$$G_m = g_m Q_{input} \tag{3.25}$$

$$G_m = g_m \frac{1}{(R_b C_{gs} + g_m L_s)\omega_0} \tag{3.26}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{(R_b C_{gs} + g_m L_s)\omega_0} Z_{load} \tag{3.27}$$

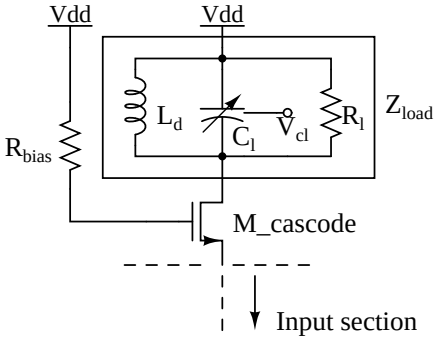

FIGURE 3.9: Load resonant circuit

In the parallel resonant circuit at the output tank, the current at the drain of the cascode transistor splits and flows separately in the inductor , capacitor and resistor. This parallel resonant circuit has its highest impedance at the resonant

frequency and a low impedance at all other frequencies. The current at the node is minimum at the resonant frequency.

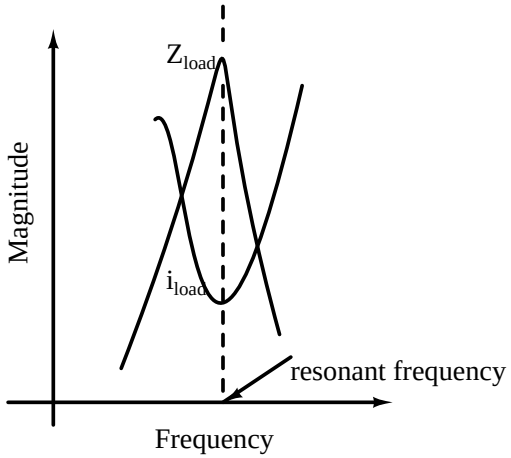

FIGURE 3.10: Impedance and current at load tank resonance

With a reasonably high Q tank, the voltage maximum will signify power maximum, as the impedance dominates in generating the voltage maximum. Hence, the peak detection scheme can be employed for the resonant frequency shift detection in a way analogous to power detection.

3.7. Proposed maximum peak point tracking algorithm

The fact that the voltage gain is maximum only when the S_{11} is maximum has been shown earlier. Hence, for the detection and calibration procedure, first the output tank resonant frequency is tuned to the frequency of interest, followed by the tuning of the input resonant frequency. The detection and the calibration scheme of the source degenerated narrowband single ended LNA is shown in Fig. 3.11. The two varactors included in the design as discussed earlier are C_g and C_l, one varactor is placed between the gate of the input transistor and ground, while

the other is placed between the drain of $M_{cascode}$ and V_{dd}.

The resonant frequency of interest is input to the LNA using the on-chip tunable VCO , similar to a transmitter PA in a transceiver using loop-back connection. The VCO exhibits a tuning range from 2 GHz - 2.7 GHz. The LNA calibration process starts by first tuning the output tank to the frequency of interest followed by setting the input match. The calibration logic detailed in section 3.2 of this chapter performs the tuning of the varactors based on the peak detector output. Once the calibration is finished the loop stabilizes and the calibration is stopped. The calibration procedure is show in Fig. 3.11.

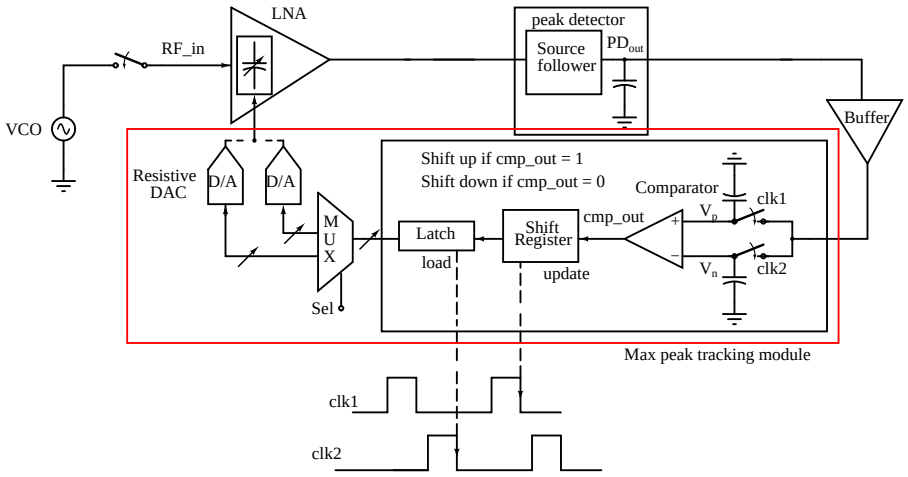

FIGURE 3.11: Reconfigurable LNA topology

Now it is important to see how the calibration block does the tuning of the varactors in an optimal manner to achieve the best LNA performance. The comparator compares the n^{th} and the $(n-1)^{th}$ voltage samples from the peak detector output and updates the shift register during the falling edge of clk1, storing the result in a latch. With the falling edge of clk2, the digital code at the latch output

changes, requiring a modified varactor control at the input/output of the LNA, to correct for the resonant frequency shift at the input/output of the LNA. The calibration is terminated once the LNA is calibrated to the desired frequency, which is determined from the digital latch output code.

The calibration procedure continues until the comparator output toggles between 1's and 0's (10101010..), similar to that exhibited in a bang-bang phase-locked loop. This results in the latch output toggling between two codes and the DAC output switching between two varactor control voltages. Once this mode is detected, the optimal point is reached and the LNA has been tuned to the resonant frequency of interest. Eliminating the ADC and instead using a comparator, register and latch, saves power and reduces area consumption in the calibration loop.

Note that the 'update' and the 'load' actions are executed on the falling edges of clk1 and clk2. This is done deliberately to compare adjacent samples in a cyclic manner . This is done by comparing the current sample with the previous sample, followed by rotating the current sample to be the previous sample. The time between the load cycle and the sampling of the next conversion should be large enough so that the output of the peak detector settles to a constant value. In this calibration procedure, a clock frequency of 5 MHz was used, ensuring robustness until the optimal impedance matching point is reached.

3.7.1 Calibration loop settling

The calibration algorithm is verified by the settling of the input varactor control voltage as shown in Fig. 3.12. This plot is for the simulation of the LNA in the worst case SS transistor corner, with Vdd = -10% @ 70°C. The on-chip detection

and calibration algorithm corrects for the input resonant frequency shift and the power gain by controlling the varactor and modifying the capacitance C_g and C_l. The varactor control, V_{cg} toggles between two voltage levels and is pegged to $\leq \frac{1}{2}$ LSB, when the calibration is automatically terminated. Fig. 3.13 shows the peak detector output settling during the calibration procedure along with the sampled voltages (Vp and Vn), at the input of the comparator. It can be seen that when Vp $\geq$ Vn, the control voltage keeps on increasing. Once the optimal point is reached, where any change in the capacitance C_g does not result in any better input match, the Vp and Vn alternate in a bang-bang fashion. The code needs to be stopped and that the optimal control voltage is found after this final convergence.

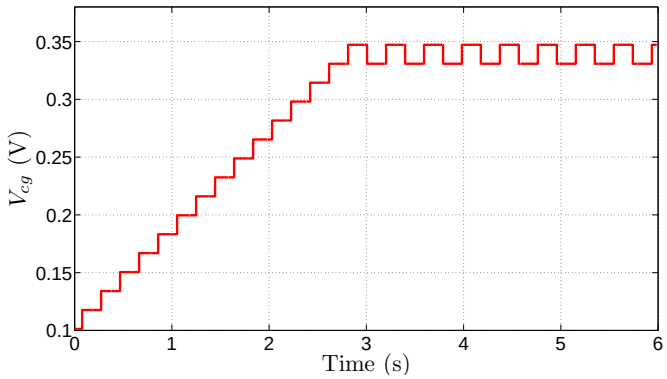

FIGURE 3.12: Varactor Control Voltage Settling (V_{cg})

3.8. Conclusion

A simple detector structure that is able to yield accurate prediction of the deviation from the optimal performance of the LNA is proposed. A single detector, along with two dedicated match networks and a robust calibration routine serves to calibrate both the input and output resonant frequency shifts.

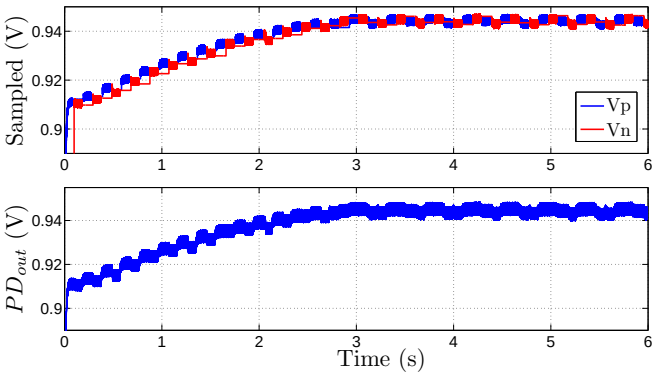

FIGURE 3.13: Peak Detector Output Settling

4. CIRCUIT DESIGN

4.1. Introduction

The system comprises of the design of two individual blocks namely the LC VCO and the LNA, with the off-chip calibration loop completing the feedback. This chapter details the circuit design of the two blocks. The LC VCO is used in a double balanced configuration,(both NMOS and PMOS), with on-chip spiral inductors. The LNA is a single stage cascode topology with on-chip input and output matching networks and with on-chip spiral inductors.

4.2. LC Voltage Controlled Oscillator

There are two major types of VCOs, the waveform oscillators and the resonant oscillators. The waveform oscillators are further classified into ring oscillators and relaxation oscillators. The resonant oscillators are further classified into LC tank oscillators and the crystal oscillators. The LC VCO advantages are its low phase noise (low jitter) at high frequency and a good tuning range. It comes at the expense of an inductor and a varactor which occupy large area. In wireless applications requiring low noise performance at high frequency, the LC VCO is preferred.

4.2.1 Analysis and Design

LC VCO can be thought of as two one port networks connected together. The first port represents the frequency selective tank where the oscillations occur and the second port represents the active circuit element that accounts for the losses in

the tank. This is shown in Fig. 4.1.

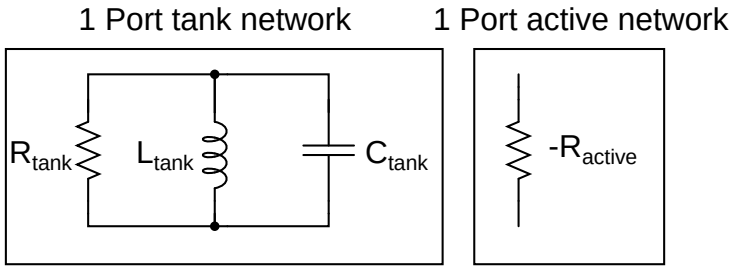

FIGURE 4.1: Two 1 port network combined to create oscillation in VCO

Oscillations are produced only if :

1. The negative conductance of the active network cancels out the positive conductance (loss) of the tank.

2. The closed loop gain has zero phase shift.

The two conditions imply that the closed loop gain should be greater than or equal to the unity magnitude, with no imaginary component. The losses associated with the tank are that of the on chip spiral inductor, varactor and the active MOSFETs. The on chip spiral inductors have low realizable quality. This dominates the losses of the VCO tank [23].

The quality factor (Q_L) of the inductor is given by

$$Q_L = \frac{\omega_0 L}{R} \tag{4.1}$$

where,

ω_0 - oscillation frequency [rad/s]

L - value of the inductance [H]

R - inductors equivalent series resistance (ESR) [Ω]

Q_L ranges from 5 to 10 for RFIC processes

$$Q_{tank} = \frac{R_{tank}}{\omega_0 L} \tag{4.2}$$

where, ω_0 is the resonant frequency of the lossless tank

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{4.3}$$

Generally capacitors have much higher component Q's than inductors in silicon integrated processes and the Q_{tank} is generally dominated by the component Q of the inductor.

$$Q_{tank} = \frac{R_{tank}}{\omega_0 L} = \frac{\omega_0 L}{R} \tag{4.4}$$

$$R_{tank} = \frac{\omega_0 L^2}{R} = \frac{\frac{\omega_0 L}{R}^2}{R} = Q_L^2 R \tag{4.5}$$

where R is the series resistance of the inductor, R_{tank} is the equivalent parallel resistance of the lossy tank, and Q_{tank} is the quality factor of the lossy tank.

It is desirable to have a large R_{tank} for a good oscillator. The maximum Q_L possible is more or less independent on the value of inductance, provided the

particular inductor layout is optimized for maximum Q_L.

4.2.2 Tuning Range

The tuning range of a VCO is required to be in excess of a certain minimum percentage of the center frequency, ω_0. The LC tank is made tunable by implementing the C of the LC tank using a variable capacitance. The varactor is designed to be adjustable over a range from C_{tank_min} to C_{tank_max} such that the tuning range is from 2 GHz - 2.7 GHz.

$$L_{tank\_min}C_{tank\_min} = \frac{1}{\omega_{0,max}^2} \tag{4.6}$$

$$L_{tank\_max}C_{tank\_max} = \frac{1}{\omega_{0,min}^2} \tag{4.7}$$

$$fractional\ tuning\ range = \frac{\omega_{0,max} - \omega_{0,min}}{2} \tag{4.8}$$

In general, the negative resistance of the differential pair must overcome all real resistive losses in the oscillator circuit. An ideal oscillator has no losses, with infinite voltage swing at precisely one frequency. In this work the double balanced LC VCO is designed.

4.2.3 Design Procedure

The LC VCO schematic is shown in Fig. 4.2. The capacitor bank used for the coarse tuning is shown in Fig. 4.3(a), with the switch implementation shown in Fig. 4.3(b). Table. 4.1 gives the component values that were used in the tunable LC VCO.

1. $I_{bias} = \frac{P_{dc}}{V_{supply}}$, where , I_{bias} is the current bias required for sustaining the oscillations, P_{dc} is the power budget allotted to the design of the VCO, V_{supply} is the supply voltage of the VCO (1.8 V).

2. $V_{tank} = I_{bias}R_{tank} = I_{bias}\omega_0 \mathrm{L} Q_L$. The value of L is fixed so as to get the minimum required swing.

3. The range of values of C_{tank} from min to max is selected based on the value of L fixed earlier. This is done to achieve the center frequency and the tuning range.

4. The transconductances of the NMOS and PMOS transistors of the double balanced LC VCO is set, so as to overcome the losses of the tank.

5. The transistor width,W, is found from the transconductance value.

4.3. Low Noise Amplifier

A critical block in this design is the LNA. The function of the LNA is to amplify extremely low signals without adding noise, thus preserving the required Signal-to-Noise Ratio (SNR) of the system. The design implements a narrowband LNA, meaning that the circuit has a resonance frequency at which it has the highest gain. The circuit design of the LNA presents considerable challenge because of the following :

1. Simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current levels.

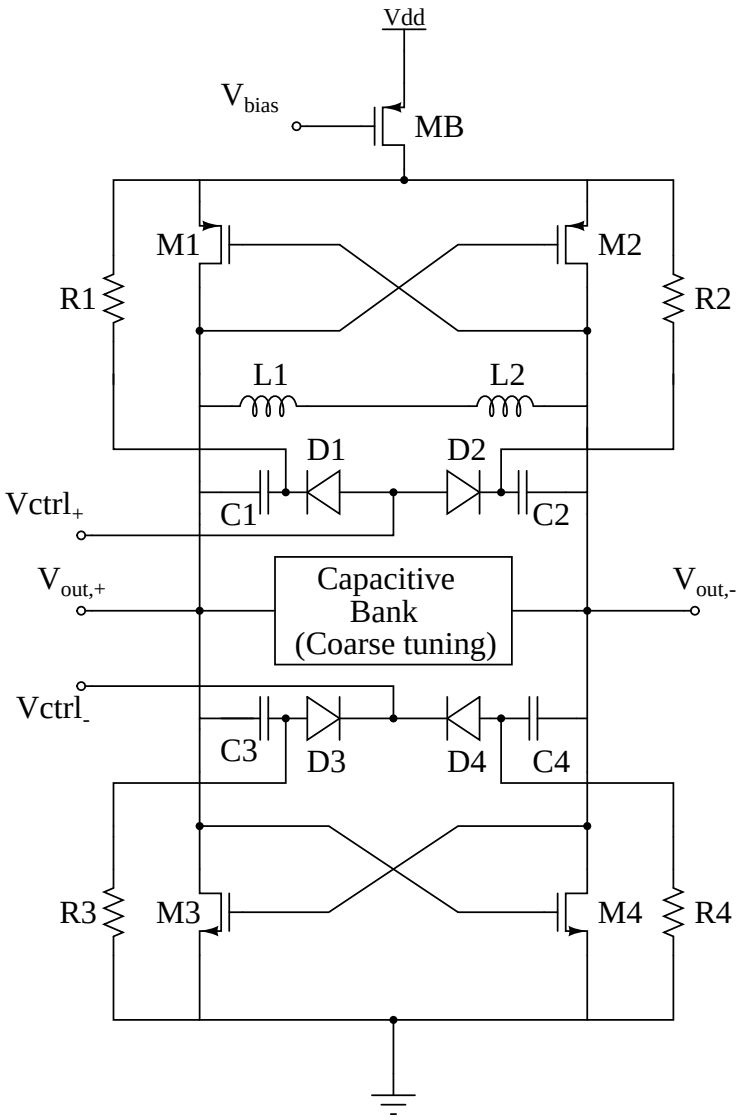

FIGURE 4.2: LC VCO Schematic

2. Interdependence of gain, NF , stability, linearity and input/output match is a tough design challenge.

3. Higher third order intermodulation product (IP3) requires higher current, although the lowest possible noise figure is usually achieved at lower current levels.

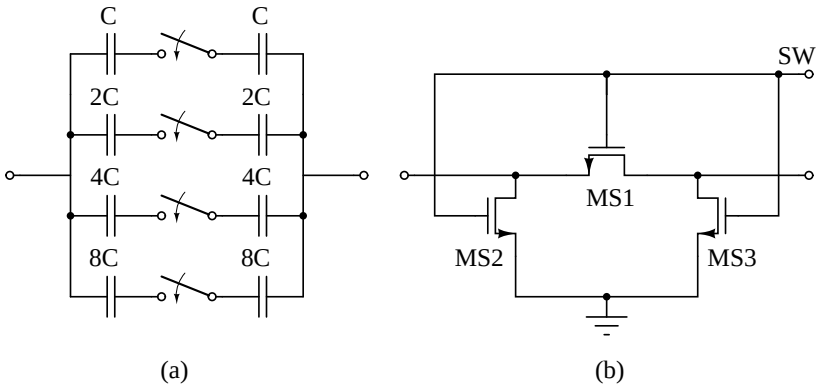

FIGURE 4.3: (a) Capacitor Bank used for Coarse tuning (b) Switch Implementation

4. Transistor selection is the first and most important step in LNA design. The designer should carefully review the transistor selection, keeping the most important LNA design trade-offs in mind.

Design of the LNA was performed, while sticking to basic requirements of an LNA as stated before. The first and foremost requirement of LNA is the optimization of input match. This is done followed by building the cascode stage and finally implementing the output match.

4.3.1 Input Matching Network

Figure 4.4 highlights the different input matching networks considered in this work. The first technique shown in Fig. 4.4(a) uses resistive termination of the input port to provide a 50 Ω impedance [24]. The use of resistors have a negative effect on the amplifiers NF. The noise contribution of the terminating resistors is neglected in [24], because an antenna was mounted directly on the amplifier, eliminating the need for input matching [25].

TABLE 4.1: VCO Component Values

Component	Parameter
NMOS,M3,M4	W = 5μm,L=0.18μm, M=5
PMOS,M1,M2	W = 5μm,L=0.18μm, M=8
R1-R4	10kΩ
D1-D4	W=5μm, L=2μm, M=45
C1-C4	2.4pF
L1-L2	d=136μm,W=20μm,n=2.5,S=2μm
MB	W=32μm,L=5μm,M=500
MS1	W=8μm,L=0.18μm, M=3
MS2-MS3	W=0.24μm,L=0.18μm, M=1

TABLE 4.2: LNA Specifications

Significance	Symbol	Acceptable Range
Input Match	S_{11}	$\leq$ -10 dB
Forward Gain	S_{21}	$\geq$ 10 dB
Output Match	S_{22}	$\leq$ -10 dB
Noise Figure	NF	$\leq$ 3 dB
Linearity	IIP_3	$\leq$ -10 dBm
Stability factor	K	$\geq$ 1

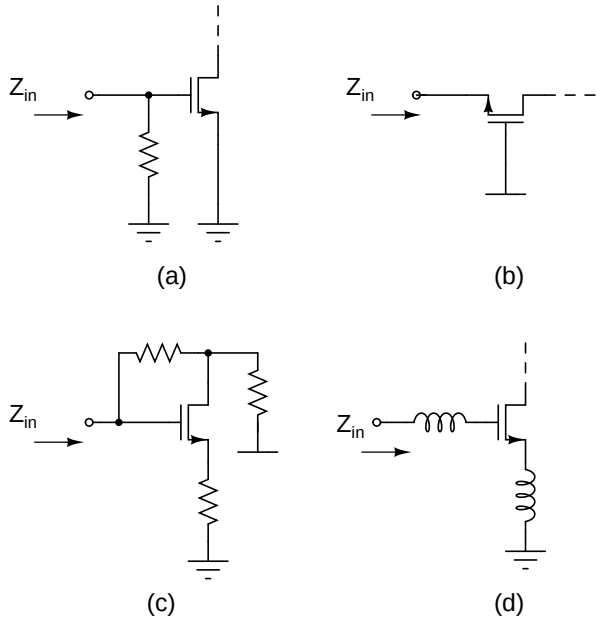

FIGURE 4.4: Input matching networks

The second topology shown in Fig. 4.4(b) uses the source or emitter of a common gate or common base stage as the input termination. A simplified analysis of the matching network, yields a lower bound on noise factor for the cases of bipolar and CMOS amplifiers [25]. Though the common-gate stage provides a wide-band input match and is less sensitive to parasitics, it has an inherently high noise figure.

The third topology as shown in Fig. 4.4(c) uses resistive shunt and series feedback to set the input and output impedances of the LNA[26]. The variation in the on-chip resistor values, is the disadvantage of this topology.

The final topology as shown in Fig. 4.4(d) uses inductive source degeneration , to generate a real term in the input impedance. Tuning of the amplifier input becomes necessary, making this a narrowband approach. The inductive source de-

generation input match technique is widely used in CMOS and GaAs MESFET amplifiers [27]. This topology gives the best noise performance of any architecture. Inductive degeneration (L_s), also improves the linearity by forming a negative series feedback. [25].

The final topology, the inductive source degeneration, shown in 4.4(d) is used in the this design due to its inherent noise advantages.

4.3.2 Cascode Stage

Since the input matching network is finalized, the next task is to build the cascode stage of the LNA. The input matching is done using a common source topology, using inductive source degeneration. To improve the gain and stability of this common source stage, a common gate stage is added on top, to make it a cascode topology. The cascode transistor also shields the output node from the parasitic C_{gd} of the input transistor. The cascode transistor reduces the miller effect by ensuring a low impedance at the drain of the amplifying device. Therefore the miller effect does not degrade the power gain and the input referred noise. In addition, the cascode improves the reverse isolation, increases the stability, and causes the output and input matching network to no longer influence each other. The cascode stage is shown in Fig. 4.6.

4.3.3 Output Matching Network

The source follower architecture is shown in Fig. 4.5. The output impedance of a source follower is as follows. If the gate resistance at the input of the source follower is R_s (the parasitic resistance at this node), the Z_{out} finally becomes

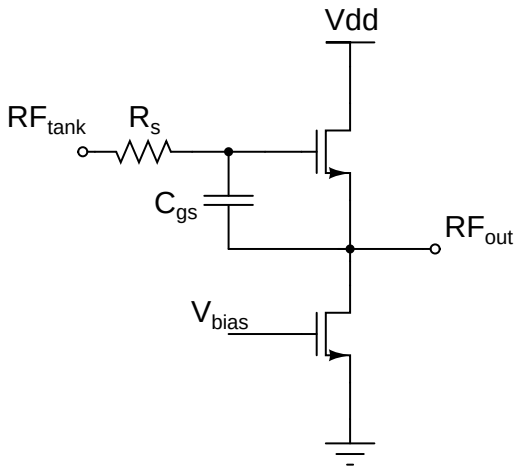

FIGURE 4.5: Output matching network(Source follower)

$$Z_{out}(s) = \frac{sR_sC_{gs} + 1}{g_m + sC_{gs}} \tag{4.9}$$

So at low frequencies, the z_{out} is $\frac{1}{g_m}$, and then there is a capacitive behavior at intermediate frequencies (for $R_s \leq \frac{1}{g_m}$) and then finally reaches a value of R_s . If $R_s \geq \frac{1}{g_m}$, there will be an inductive behavior at intermediate frequencies which might cause ringing. In this case, optimized layout technique is done to ensure that the parasitic at that node will never be greater than $\frac{1}{g_m}$ of the source follower.

4.3.4 Noise Figure Optimization

Another parameter of prime importance in the design of LNA, is noise figure. According to the noise figure optimization method for fixed power dissipation for short channel devices given by [25],the optimum $Q_{input,opt}$ is given by,

$$Q_{input,opt} = c\sqrt{\frac{5\gamma}{\delta}[1 + \sqrt{(1 + \frac{3}{c^2}(1 + \frac{\delta}{5\gamma}))}]} = 4.5 \tag{4.10}$$

where,

c = correlation between gate noise and drain induced noise

γ = coefficient of channel thermal noise

δ = coefficient of gate noise

$Q_{input,opt}$ = Quality factor of the series resonance circuit at the input

The value of Q_{input} was fixed around 4.5 and this yields width of M_{input} as approximately 700 μm. Simulation of the circuit with this width of M_{input} generated a NF of over 3.5 dB. So optimization of the width is done to get a low NF value of close to 2.3 dB at center frequency of 2.4 GHz, with a power consumption of 27 mW. Optimized width of M_{input} is found to be 315 μm (length = 0.18um), which is close to the value found earlier while satisfying the condition of providing stable input impedance of 50 Ω.

The total power dissipation is 27 mW. Of this power, only 12.6 mW is attributed to the first amplifier stage. The other 14.4 mW is used in the output matching network to drive the 50 Ω. This added power could be nearly eliminated if the LNA were to drive an on-chip mixer. The reconfigurable LNA implemented is shown in Fig. 4.6.

4.4. Linearity

Linearity metric of the LNA is characterized by the input third order intermodulation point(IIP_3). The IIP_3 of the reconfigurable LNA can be written as

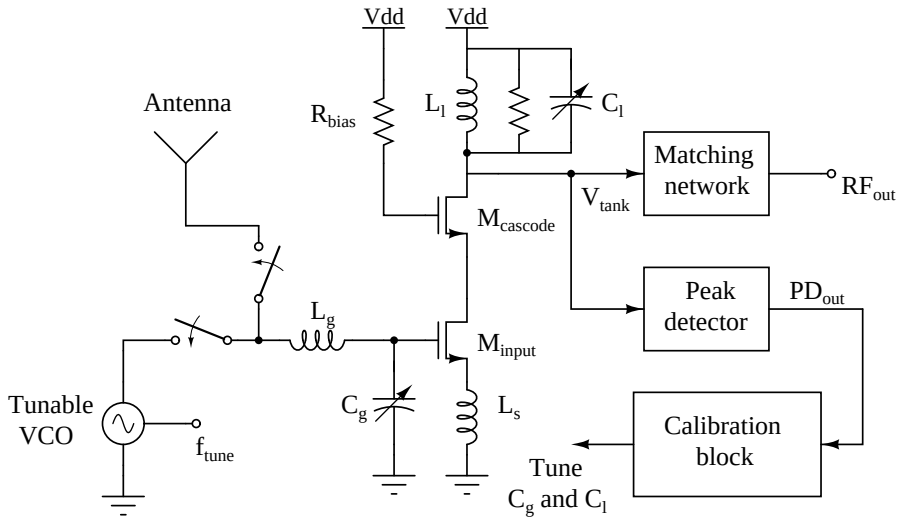

FIGURE 4.6: Narrowband RF CMOS LNA with inductive source degeneration

$$IIP_3(dBm) = IIP3_{in}(dBm) - 20 * log_{10}(\frac{1}{\omega_0 C_{gs} R_b}) \tag{4.11}$$

Here, an input match is assumed. The first term, represents the intrinsic linearity of the input transistor of the LNA and is due to the velocity saturation effect of short channel CMOS transistors which linearizes the ideal drain current (i_d). The second represents the additional voltage boost across C_{gs}.

4.5. Peak Detection and Calibration

4.5.1 Peak Detector

Different peak detector topologies are shown in Fig. 4.7.

The topologies shown in Fig. 4.7(a) and Fig. 4.7(b) can be used in cases where the DUT node of interest can directly bias the peak detector in the saturation re-

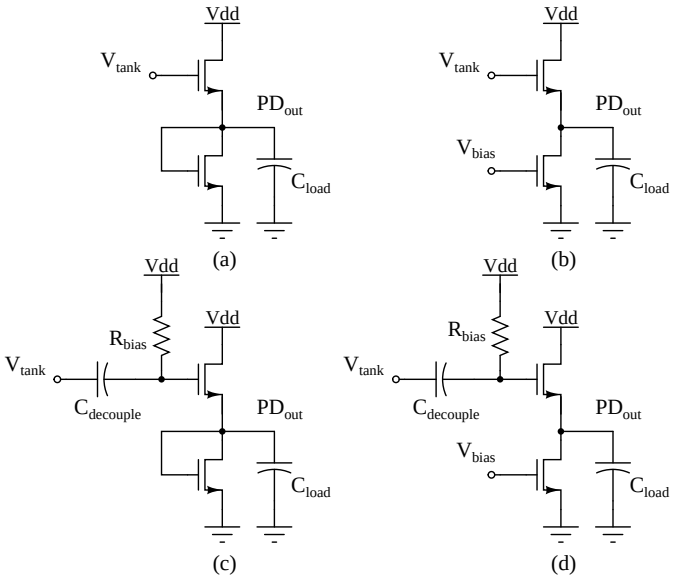

FIGURE 4.7: Different Peak Detector Topologies [19]

gion. The detectors shown in fig. 4.7 (c) and Fig. 4.7(d) can be used to self bias the detector by AC decoupling the input of the detector by a DC blocking capacitor.

The capacitor value at the input gate of the source follower has to be chosen with great care. The capacitor value cannot be $\gg C_{gs}$, as there must be maximum signal swing at the detector input. This type of detector will load the DUT node, due to its high input capacitance. If the value of the capacitor is chosen to be very small, the capacitor divider will allow only a fraction of the RF signal amplitude to reach the detector input, thereby decreasing the resolution of the detection scheme. In this work, the peak detector (a) has been used and the inherent input capacitance that it provides is 88 fF. The proposed peak detector exhibits high input impedance, low input capacitance (the parasitic capacitance C_{gs} of the input MOS of the detector whose aspect ratio is small), consumes low power and is easy to integrate at multiple

nodes of RF transceiver.

4.5.2 Varactor Design

The varactor design is an important aspect in the detection and calibration process, as it sets the tuning range as well as the degradation of the quality factor of the input tank. There are two varactors, one being C_g between the gate of the input MOS and ground, and the other is C_l, used as the varactor from the drain node of $M_{cascode}$ to V_{dd}. For the latter varactor, a NMOS operated in the inversion region is used. For the former varactor, an NMOS triple well process varactor is used where the gate terminal of the MOS varactor is connected to the gate of the input MOS transistor and the bulk terminal is connected to ground. The capacitance is tuned by using the third terminal of the MOS, which is the drain/source terminal's that are shorted together.

The structure of the varactor is similar to an n channel MOSFET with the exception of being fabricated in an deep n-well instead of p-substrate. This eliminates the parasitic pn-junction capacitance at the source and drain nodes which would otherwise limit the tuning range possible. The advantages of this tuning is wider transition from C_{min} to C_{max} as inversion mode varactors. This architecture has one of the lowest parasitic resistance and the best $\frac{C_{max}}{C_{min}}$ ratio. The tradeoff for these advantages is that we have to live with a non-linear tuning range which is not so problematic. Another possibility is to use a p-channel MOSFET in a p-well/substrate. The lower career mobility is the bottleneck in this case [28]. For the output tank tuning a relatively simple varactor is used since it is between the output tank node and the AC ground in V_{dd}. Figure 4.8 shows the topology of the

two varactors designed in this process.

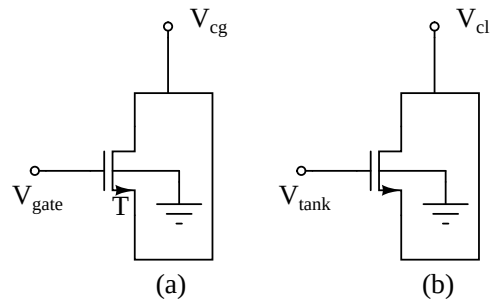

FIGURE 4.8: Varactors used for tuning (a) Input Resonant frequency (b) Output tank frequency

4.6. Conclusion

The design of the LC VCO and the LNA comprehensively ensure that the LNA can be made reconfigurable using the dynamic input/output tank matching. The reconfigurability helps improve the input match and the power gain of the LNA without causing much degradation to NF and linearity. Chapter 5 discusses the measurement results in detail and highlights the practical use of this dynamic voltage scaled reconfigurable LNA.

5. RESULTS AND DISCUSSION

5.1. Introduction

The peak detection and calibration scheme discussed earlier is implemented in 0.18μm UMC process with a supply voltage of 1.8 V. The die photo of the reconfigurable RF LNA is shown in Fig. 5.1, along with the detection and calibration measurement setup that is used.

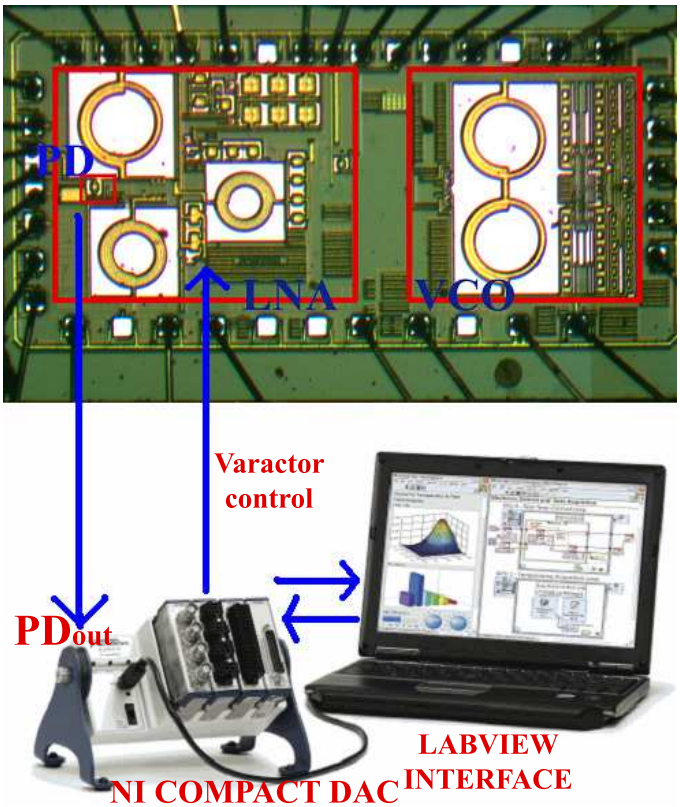

FIGURE 5.1: Measurement setup of the reconfigurable RF LNA.

The LNA, VCO and the peak detectors are implemented on-chip, while the calibration routine is implemented off-chip using a NIDAQ and LabView interface,

as shown in Fig. 5.1. As explained earlier, the LNA is input with the frequency of interest (2.4 GHz), using the on-chip VCO. The peak detector output is sensed by the NIDAQ and Labview interface. Then the interface modifies the value of the output varactor to first set the output tank resonant frequency . This is done by sensing the peak detector output and incrementing/decrementing the varactor value. The varactor value is set once the maximum peak detector output is reached. This is followed by setting the input resonant frequency using the same procedure detailed above. Once the optimal performance is reached, the varactor voltages are freezed. The calibration can run at very low frequencies of the order of few MHz.

5.2. Reconfigurable RF LNA

5.2.1 Process Compensation

The LNA performance is degraded due to PVT and bond wire variations. The worst affected parameter is the input reflection coefficient, which determines the amount of input power into the LNA. Consequently, the power gain of the LNA is dependent on the input match as detailed earlier. The degradation in specific parameters that negatively affect the performance is shown in the table below.

It can be seen from Table. 5.1 that the worst affected parameter is the input transistor's transconductance (g_m) and intrinsic capacitance (C_{gs}). The variation in g_m affects the real part of the input impedance and the variation in C_{gs} affects the resonant frequency of interest. The LNA detection and the calibration restores the LNA to the optimal performance. The LNA performance, input matching and the power gain, with/without the detection and calibration is shown in Fig. 5.2

TABLE 5.1: LNA performance degradation summary due to PVT variations

PVT Corner	g_m	C_{gs}	i_d
TT, V_{dd} = 1.8 V @ + 27°	65.09 mS	308.04 fF	6.36 mA
SS, V_{dd} = 1.62V @ + 70 °	52.55 mS	325.98 fF	5.87 mA
FF, V_{dd} = 1.98V @ - 50 °	87.65 mS	302.31 fF	6.87 mA

and Fig. 5.3. Due to process variations the LNA performance is degraded, and the detection/calibration helps improve the performance.

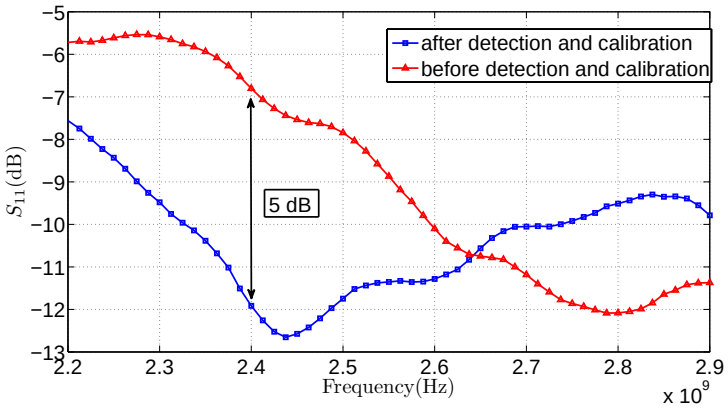

FIGURE 5.2: Input reflection coefficient of the LNA with/without the detection and calibration.

It can be seen that the input reflection coefficient, S_{11} is degraded due to reflections at the input port of the LNA. This could be due to any of the imperfections like PVT variations or increased bond wire lengths. The degradation in the input

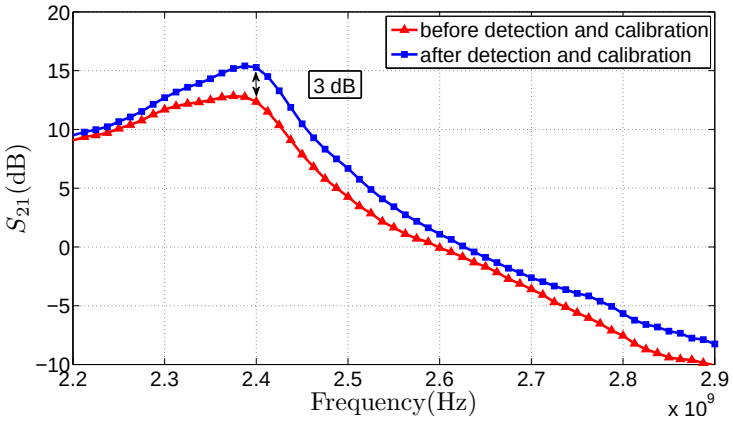

FIGURE 5.3: Power gain of the LNA with/without the detection and calibration.

match decreases the gain to 12.4 dB. The LNA was designed for a gain of around 15 dB. From Fig. 5.3, it can be seen that the output tank resonant frequency is still well oriented at 2.4 GHz and does not suffer a shift, while the major problem is with the input match. The detection and calibration algorithm detects the resonant frequency shift and tries to correct for it. As explained in Chapter 3, this is done by first dynamically changing the varactor voltage, thereby modifying the capacitance at the input tank and measuring the peak voltage output. This output voltage is then compared with the previous sample and based on the result, the capacitance is either incremented or decremented at the input tank to change the real and imaginary part of the impedance. It can be seen that the S_{11} has improved by over 5 dB which causes the S_{21} to improve by over 3 dB. The concept of having the dynamic frequency agile RF front end for the LNA using the automatic detection and calibration has helped in improving the input match and power gain of the LNA.

The peak detection closely mimics the power detection, which makes the de-

tection scheme unique, area/power efficient and robust (as explained in Chapter 3). The peaks obtained through the detection scheme correlate to a great degree of accuracy in providing an optimal performance to the LNA. This can be seen in Fig. 5.4 and Fig. 5.5. The peaks from the peak detector output closely correspond to the power peaks in S_{11} and S_{21}, confirming the sanity of the detection and the calibration process. Any minor deviation in the peaks could be due to the fact that during the calibration the varactor capacitance might be altered by the voltage swing at one of its terminals, causing the capacitance to deviate. There will be an averaging effect of the capacitance, due to the small signal swing at one of the terminals of the varactor, which could be causing a minor shift in the peak voltage. The off chip calibration loop is done using a National Instruments compact DAC (NIDAQ) and the loop terminates once the peak voltage is reached, rendering optimal performance.

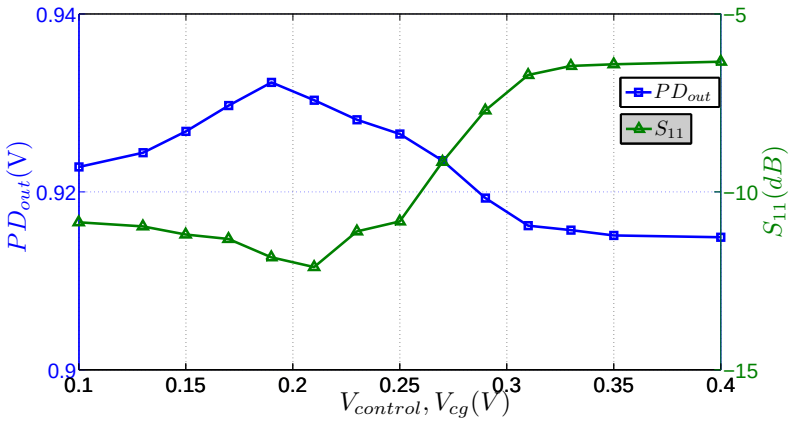

FIGURE 5.4: Peak detector voltage peak in comparison to the input reflection coefficient S_{11} with Vdd = 1.8 V

The linearity of the LNA is still within reasonable bounds. The linearity of the LNA was measured using the 1 dB compression point analysis. The LNA is shown to have a P_{1dB} = -23.6 dBm. With P_{1dB} = -23.6 dBm , the IIP3 is approximately + 10 dBm higher, -13.6 dBm. So the linearity of the LNA is not a huge tradeoff in

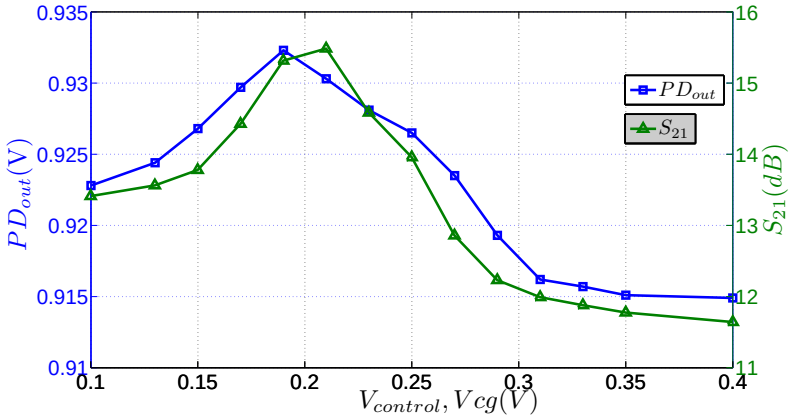

FIGURE 5.5: Peak detector voltage peak in comparison to the power gain, S_{21}, with Vdd = 1.8 V

the introduction of the varactors at the input and output tanks. Figure 5.6 shows the 1 dB compression plot of the LNA.

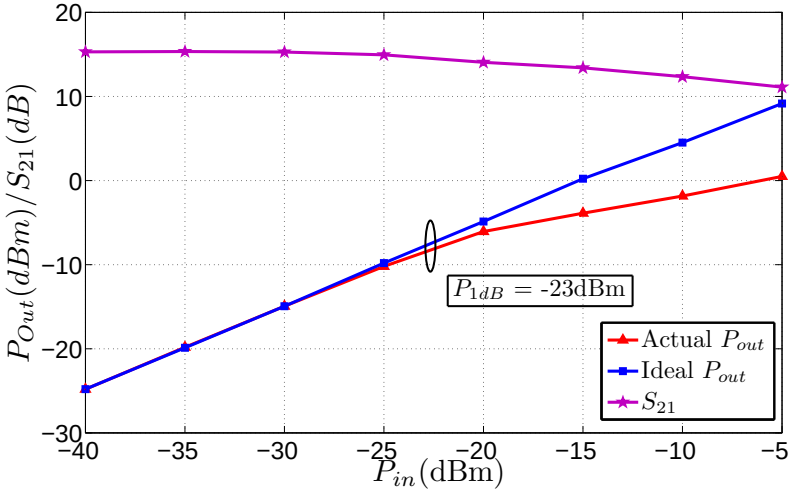

FIGURE 5.6: P_{1dB} of the LNA

5.2.2 Dynamic Supply Voltage Scaling

This being a 0.18μm process and the LNA requiring high power gain, the power supply of the LNA was set to 1.8 V. It would be good to have the supply

scale down when the gain required for the amplification of signals, can be small for some applications, but not too small that it renders the LNA inactive. Slamming the power supply down will help reduce the power consumption in a great way, which is very critical in Analog/RF IC design. The same LNA can be used in different applications with varying power gains depending on the applications requirement. This dynamic voltage scaled LNA saves 7 mW of power as the power supply is slammed from 1.8 to 1.1 V. As soon as the power supply is reduced to 1.1 V the LNA performance degrades, which is expected, as the input match, which is dependent on the transconductance (g_m) of the input MOS changes. This modifies the resonant frequency and the real part of the input impedance. The resonant frequency in this case shifts from 2.81 GHz to 2.72 GHz and the real part of the input impedance drops from -12 dB to around -9 dB at the resonant frequency of 2.72 GHz. The degraded LNA performance with power supply scaling is shown in Fig. 5.7 and Fig. 5.8.

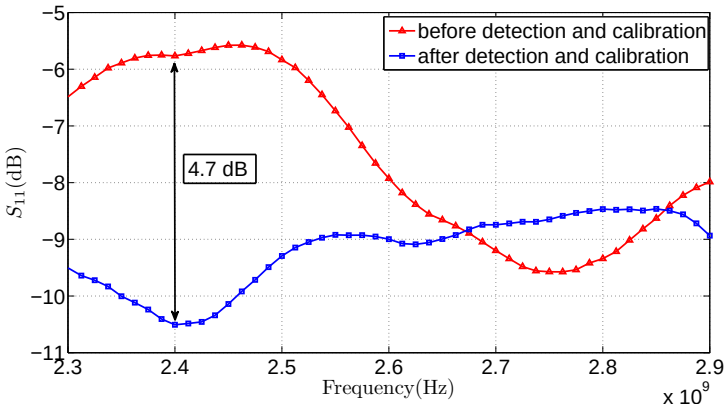

FIGURE 5.7: Input reflection coefficient of the LNA with/without the detection and calibration (with reduced power supply, $V_{dd} = 1.1$V)

The automatic calibration scheme helps better the S_{11} by 3.5 dB, thereby im-

proving the power gain close to 3.1 dB. It can be seen that the calibration loop helps by modifying the resonant frequency in parallel to altering the real part of the impedance in a counteracting manner to better the input match and power gain.

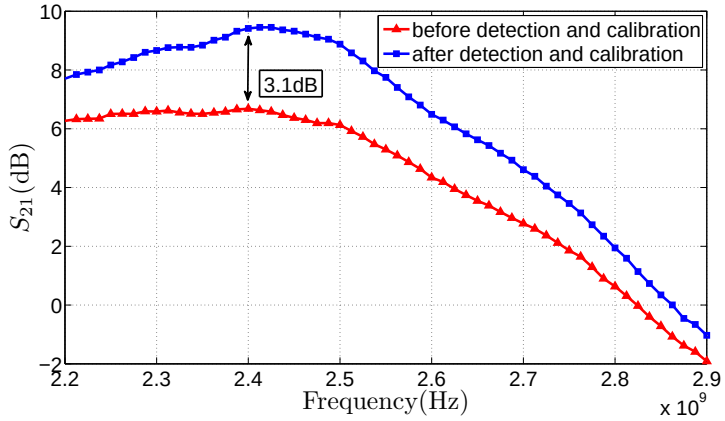

FIGURE 5.8: Power gain of the LNA with/without the detection and calibration (with reduced power supply, $V_{dd} = 1.1$V)

The dynamic power supply scaling trades gain for power consumption as mentioned earlier. The power consumption is reduced from 12.6 mW to 5.2 mW, while the gain degrades close to 6.4 dB, which is 9 dB reduction from the normal value and is unacceptable. The detection and calibration helps better the power gain from 6.4 to 9.3 dB, which is almost a 34% improvement in power. Table. 5.2 summarizes the performance improvement in using the automatic detection and calibration by comparing the LNA performance before and after the dynamic power supply scaling.

Power amplifiers (PA) universally suffer from reduced efficiency when operated below the maximum output power, limited by the battery voltage. This phenomenon is called power back-off. This problem is also increased due to the use of higher data rate standards. Due to the higher order standards, the transmitters need to operate

TABLE 5.2: Dynamic voltage scaled LNA performance improvement @ 2.4 GHz

Parameter	After calibration	Before calibration	After calibration
S_{11}	-11.2 dB	-5.8 dB	-10.5 dB
S_{21}	15.3 dB	6.5 dB	9.4 dB
Power Supply	1.8 V	1.1 V	1.1 V
Power Consumption	12.2 mW	5.6 mW	5.6mW

with increasing amounts of power back-off. This necessitates the power amplifier to operate at lower efficiencies. Class A PAs are widely used in WLAN systems, especially OFDM 802.11 a/b/g. These PAs are very linear and in order to retain their high linearity, they need to be operated below saturation. Due to this the efficiency of PAs is not good.

The dynamic biasing scheme talked about in this work can be very well extended to power amplifiers, enabling higher efficiencies while still retaining the linearity. One of the ways to maintain good efficiency at low power is to dynamically bias the supply voltage of the PA [35]. This can done by tracking the envelope of the signal and reducing the supply voltage dynamically to prevent saturation. In addition, the bias current of the PA can also be controlled to zero in to the optimum performance of the PA. So the dynamic voltage scaling of the LNA done in this work can be extended to other blocks like the PA, helping reduce power consumption and also improve other important metrics like efficiency.

5.2.3 Frequency Hopping

As seen in the earlier detection and calibration, the input match is affected and the output resonant tank is good to begin with, so the detection and calibration, had to only adjust the input match , by tuning the input varactor, without having to adjust the output resonant tank varactor. In case of operating the LNA in a different band, say the 2 GHz band, it is logical to tune the output and input varactors in order to orient both the input and the power gain peaks around 2 GHz. So first the output tank resonant frequency is set to 2 GHz, followed by the input resonant frequency. Figure 5.9 shows the power gain before and after the detection and the calibration process.

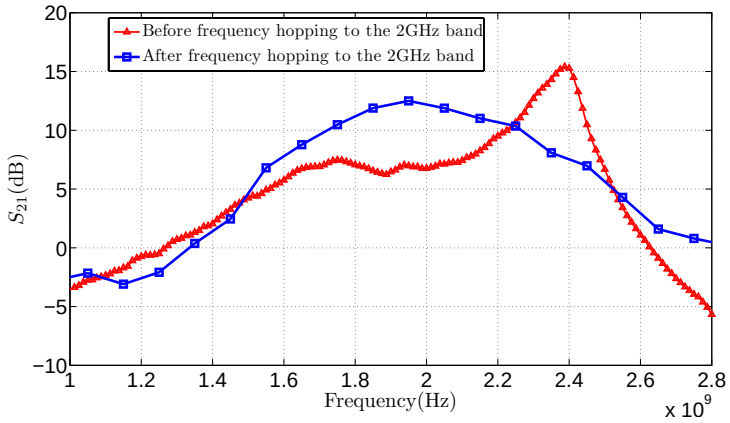

FIGURE 5.9: Power gain of the LNA with/without detection and calibration @ 2 GHz

The automatic calibration scheme helps better the S_{11} by 1 dB, and the power gain by 4 dB and enables operating the LNA in the 2 GHz band as well.

5.2.4 Peak Detector Performance Comparison

The peak detector performance as compared to the state of the art detectors is shown in Table. 5.3 [19]. All the three detectors were experimented with the

detection process of a 2.4 GHz LNA, with the technology used for fabrication being different. After evaluation, the peak detector used in this work is most appropriate, as it is area/power efficient and is easy to implement. Though the gain of the detector is somewhat smaller, it is within tolerance for the post processing circuitry that follows.

The P_{in} Vs V_{out} for the peak detector is shown in Fig. 5.10.

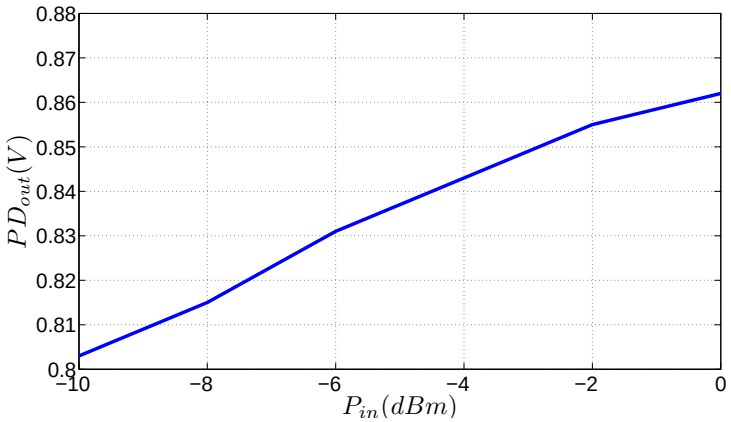

FIGURE 5.10: Peak detector output voltage with varying input amplitude

5.2.5 Reconfigurable LNA Vs Conventional LNA

To give a better insight into the effectiveness and importance of the the detection and calibration, the variation across corners is discussed with the help of post layout extracted results. Huge advantages can be seen in terms of improvement in the input match and the power gain. Table. 5.4 compares and contrasts the reconfigurable LNA with the conventional LNA. The worst case in terms of the input match occurs for SS corner , Vdd = -10% Temp = + 70°C. The detection and the calibration helps measure this offset, calibrates and improves the final S_{11} by 14 dB. The worst case in terms of the power gain occurs at the FF corner, Vdd = +10% and Temp = - 50°C. At this corner, the reconfigurable LNA improves the power

TABLE 5.3: Peak detector performance comparison

Detector type	Peak Fig. 4.7(a)	RMS [4]	Power [6]
Technology[nm]	180 CMOS	350 CMOS	250 BiCMOS
Frequency[GHz]	2.4	2.4	2.4
Power Supply[V]	1.8	3.3	3
Input Capacitance [fF]	88	22.5	—
Area[mm^2]	0.026	0.013	0.260
Gain[mV/dBm]	8.3	60	–
Power[mW]	3.4	10	15

TABLE 5.4: Reconfigurable LNA Performance Vs Conventional LNA (Post Layout Extracted Results)

Parameter	Reconfigurable LNA	Conventional LNA
Typical		
S_{11}(dB)	-23.32	-22.10
S_{21}(dB)	14.11	14.23
NF(dB)	2.27	2.12
20% extra L_s		
S_{11}(dB)	-18.5	-14.5
S_{21} (dB)	13.1	12.5
NF (dB)	2.64	2.42
SS		
Vdd = -10%		
Temp = + 70°C		
S_{11}(dB)	-27.78	-13.54
S_{21}(dB)	12.75	11.26
NF(dB)	3.39	3.21
FF		
Vdd = +10%		
Temp = - 50°C		
S_{11}(dB)	-17.73	-15.53
S_{21}(dB)	16.21	11.18
NF(dB)	2.08	1.95

gain, S_{21} by about 5 dB. 20% increase in L_s resulted in degrading the input match by almost 5 dB and the power gain by 1.7 dB. The improvement using the detection and calibration in input match and power gain is 4 dB and 0.6 dB respectively. It can be seen that the noise figure does not degrade much in the presence of the extra varactors that are added, making the detection and calibration system robust with minimal tradeoffs.

5.3. LC Voltage Controlled Oscillator

The LC VCO designed using the NMOS and PMOS balanced structure spans a frequency range 2 - 2.74 GHz with an output power of -9.85 dBm, single ended and -5 dBm, differential. Figure 5.11 shows the tone of the VCO at 2.4 GHz, the frequency of interest. Figure 5.12 shows the frequency tuning characteristic of the LNA using both the analog(fine) and digital(coarse) tuning. The analog tuning is done by varying the varactor using V_{diff} as shown in Fig. 5.12.

5.3.1 Frequency tuning

LC VCO is designed for a fixed bias current, minimizing the power dissipation. Phase noise of the LC VCO is measured to be -102.65 dBc/Hz @ an offset of 600 kHz from the carrier. Figure 5.13 shows the phase noise of the LC VCO.

5.3.2 Performance Summary

The Table. 5.5 summarizes the performance of the on-chip LC VCO.

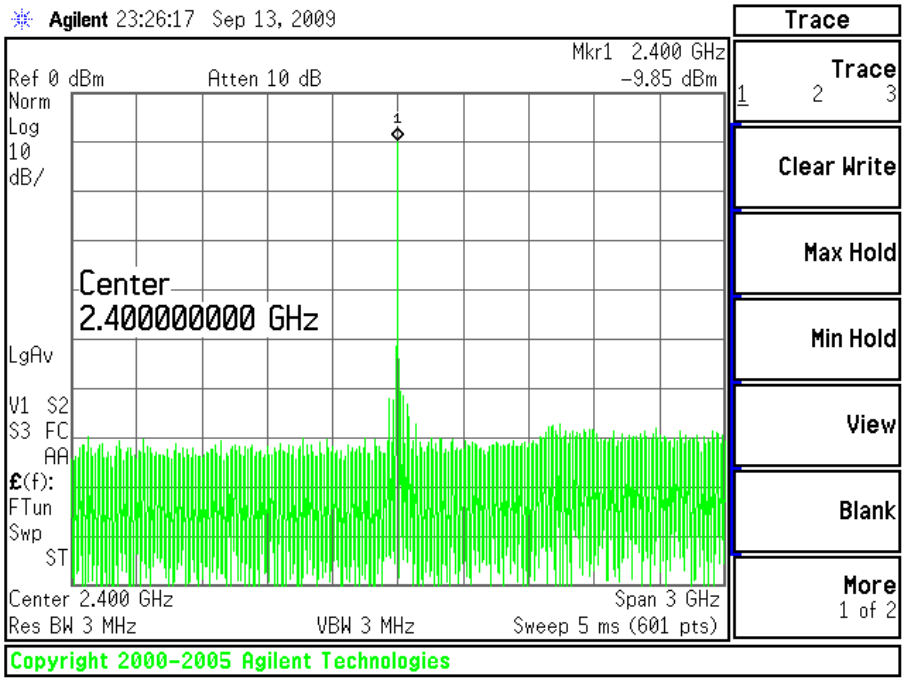

FIGURE 5.11: VCO tone at 2.4 GHz

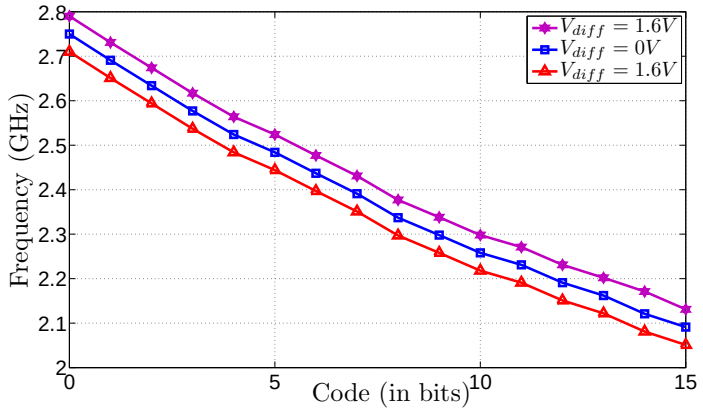

FIGURE 5.12: Frequency tuning characteristic of the LC VCO

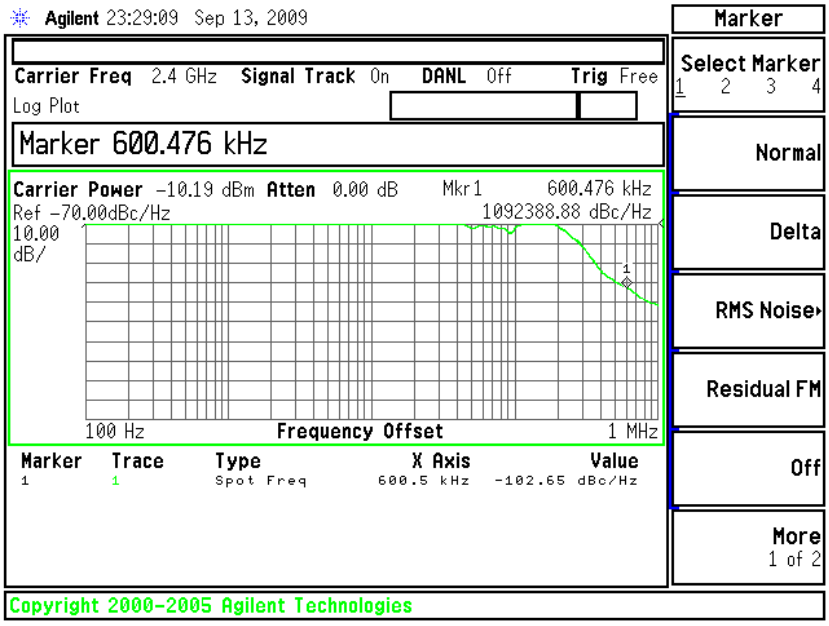

FIGURE 5.13: Phase noise characteristic of the LC VCO.

TABLE 5.5: VCO Performance Summary

Parameter	Value
Frequency Range(GHz)	2.05-2.78
Output Power (differential)	-4.9 dBm
Phase Noise @ 600kHz offset, 2.4 GHz carrier	-102.65 dBc/Hz
Power dissipation	7.812 mW
Area	1.44 mm^2

5.4. Conclusion

A novel yet simple peak detection and calibration scheme has been proposed which integrates with the RF LNA to reconfigure and improve performance across process variations and reduced power supply. The proposed maximum, peak-point calibration algorithm is area and power efficient when compared to the conventional calibration schemes. A reconfigurable 2.4 GHz narrowband LNA has been designed using on-chip detection and calibration of the input match and power gain. The measurement results show that the LNA can reconfigure its input matching as well as power gain to optimal performance, without significant degradation in the noise performance and linearity. The feature of dynamic supply voltage scaling has also been tested which show significant improvement in power by trading gain. This feature can be extended to power amplifiers with much more benefits in efficiency. The resonant frequency shift detection and calibration of RF LNAs can help alleviate the major problems in most RF transceivers. This integrated measurement and calibration technique will be useful for next generation software defined radios (SDRs).

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APPENDIX

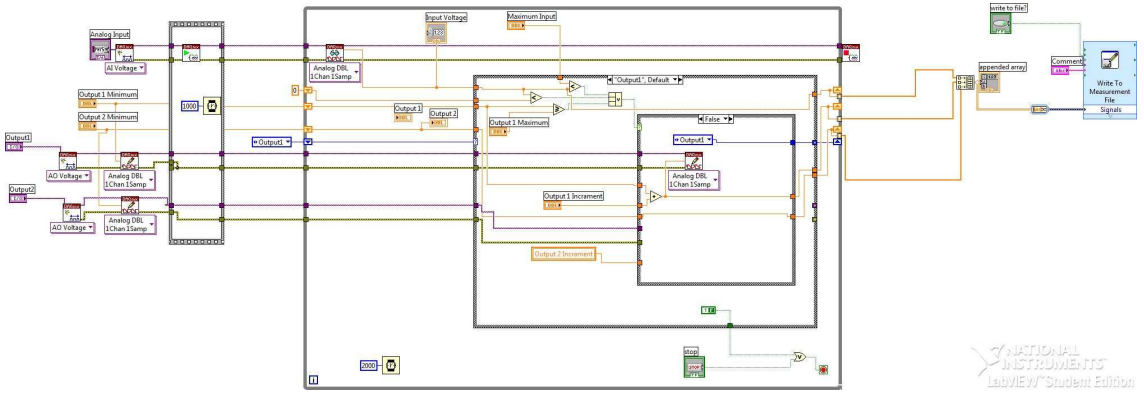

FIGURE 0.14: Labview interface enabling the calibration