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David J. Allstot

As Si MOS approaches its maximum limits in speed and bandwidth, new devices are desired to meet the needs of high speed communications and signal processing. A device that exhibits superior performance to Si MOS, BJT, and GaAs technology is the HEMT (high electron mobility transistor).

The HEMT offers superior transconductance, mobility, speed, and noise performance compared to Si MOS, BJT, and standard GaAs technology. The high performance is a result of improved channel mobility due to a heterojunction. At the heterointerface, the majority carriers are confined to a very thin sheet forming what has been termed a 2DEG (two dimensional electron gas).

The purpose of this thesis is to demonstrate the suitability of Honeywell's delta-doped self-aligned complimentary HIGFET procces for the realization of high speed analog circuits. An operational amplifier and switched-capacitor circuit are presented. The operational amplifier has been fabricated at Honeywell and preliminary tests have been performed on the op-amp which are also presented.

High Speed Analog Circuit Design using the Heterostructure Insulated Gate Field Effect Transistor

by

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Major Professor, representing Electrical and Computer Engineering

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Alexander B. Smith, Author

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1. INTRODUCTION

As Si MOS technology approaches its upper limits in speed and bandwidth, new devices are desired that meet the needs of high speed communications and signal processing. A device that exhibits superior performance to Si MOS, BJT and GaAs technology is the HFET, heterostructure GaAs FET. This device has received much attention in the areas of microwave, millimeter wave, and digital processing such as SRAMs. To date, the HFET has not received much attention in the area of analog circuits due to a lack of a complementary process. Recently, however, research institutions have been successful in fabricating p-channel HFETs with useful transconductances.

Analog design based upon CHFET technology offers advantages similar to CMOS in terms of design flexibility and voltage gain, while giving increased speed and bandwidth performance for high frequency signal processing and A/D conversion.

The goal of the present work is the realization of high speed signal processing circuits using Honeywell's CHIGFET process. The CHIGFET process provides complimentary heterostructure insulated gate FETs that operate under the same principles as the HEMT (high electron mobility transistor), as described in chapter two. An advantage of the HIGFET is that it operates in enhancement mode, and its current-voltage relationship is similar to that of NMOS or PMOS. An operational

amplifier is presented based on a typical CMOS topology. Also presented is the design of a switched capacitor gain cell which incorporates the operational amplifier.

Because these circuits can be operated at speeds significantly higher than the current state-of-the-art CMOS, they are ideally suited for the next generation of delta-sigma modulators, radio receivers, and other analog applications.

Chapter two covers the background and operation of the Heterostructure Field Effect Transistor. Chapter three covers the design and analysis of an operational amplifier and a switched-capacitor gain cell. Chapter four covers device parameter extraction which is done to obtain more accurate simulations and to determine if the model is reliable. Chapter five covers test considerations of the op-amp and preliminary test results. The paper ends with the conclusions of chapter six.

2. THE HETEROSTRUCTURE FIELD EFFECT TRANSISTOR

2.1 HFET Device Operation

CMOS technology has become the standard in analog and digital data processing due to its low power consumption and high density characteristics. Current trends in data processing require very high speeds, and Si based circuits may not be able to meet the demands. New devices are therefore desired that meet the needs of high speed communications and signal processing and take advantage of the CMOS characteristics. Such a device, called the heterostructure transistor, is receiving much attention in the area of high speed digital processing, and microwave and millimeter wave applications [1]. The heterostructure transistor, also called the HEMT (high electron mobility transistor), MODFET (modulation doped FET), TEGFET(two dimension gas FET), SDHT (selectively doped heterostructure transistor), and HFET, has proven to operate faster, with less power dissipation, lower noise figure, higher gain-bandwidth product than Si MOS, BJT, and standard GaAs technologies. Other advantages are small source resistance and high output resistance. Transconductances as high as $1160\frac{ms}{mm}$ with f_t=205 GHz have been reported [2]. Mobilities of $8000\frac{cm^2}{Vs}$ can be achieved, versus $4000\frac{cm^2}{Vs}$ for a MESFET. For a given gate length f_t is approximately two times higher than for MESFETs [2]. Noise figures of 2.4dB at 62 GHz and f_{max} greater than 250 GHz have been demonstrated [2]. Another advantage is its radiation hardness and low temperature operation, making it ideal for space applications. A number of HFET circuits have been de-

veloped by different groups which demonstrate the HFET's superiority to other technologies. Fujitsu and Rockwell have reported a sub-nanosecond 1kbit SRAM [4,5], A 500 MHz 16x16 complex multiplier was reported by Honeywell Sensors [6], and Honeywell Systems and Research Center has fabricated a 1kx4 SRAM that operates at 284 MHz [13].

The advantages of the HFET arise from the use of a heterojunction to increase the channel mobility. A heterojunction is a junction between semiconductors of different compositions typically of the III-V group such as GaAs and AlGaAs. The two semiconductors that form the heterojunction have different band energies. It is this difference in bandgap at the junction that gives rise to the superior mobility of the device. The standard single heterojunction HEMT, shown in figure 2.1, consists of four layers. The first layer is a semi- insulating GaAs substrate, the second is an undoped GaAs buffer which forms the channel at the heterointerface, the third is an undoped AlGaAs spacer, and the fourth is doped AlGaAs which supplies electrons to the channel and acts as a gate dielectric. There are also highly doped 'cap' layers to facilitate low resistance ohmic contact to the drain and source. Due to the band offset between the doped AlGaAs (high bandgap layer), and the undoped GaAs (lower bandgap layer), electrons diffuse from the doped AlGaAs layer to the AlGaAs/GaAs interface causing a mobile sheet charge layer to develop at the interface. The resultant positive charge in the AlGaAs sets up a very strong electric field normal to the heterojunction which causes band-bending to occur. Aided by the band discontinuity, the electrons are confined to the heterointerface in the higher purity GaAs layer, as shown in figure 2.2. The confinement of electrons at the heterointerface was first predicted by Esaki and Tsu in 1969 and experimentally observed by Dingle, Stormer, and Gossard at Bell Labs in 1978 [7,8,9]. The 2DEG is a very thin sheet of electrons, tens of angstroms thick. In conventional MESFETs,

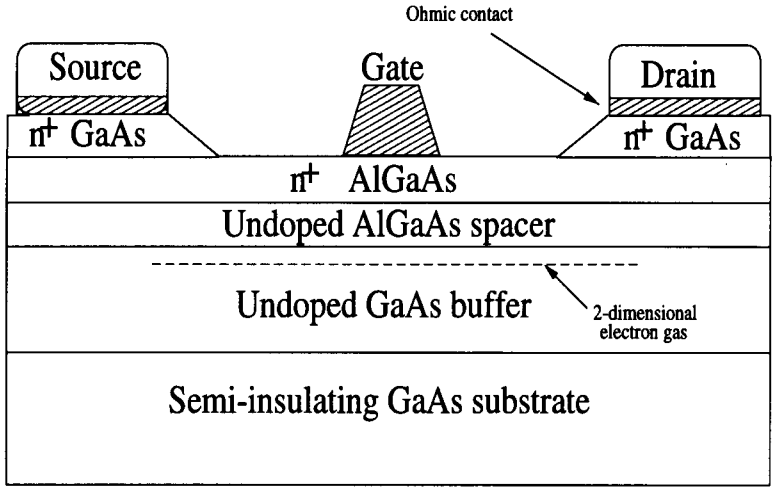


FIGURE 2.1. Cross sectional view of a simple HEMT.

the channel is doped. When the channel is conducting ionized donors interfere with the electrons. In a HFET, however, there are no donors in the channel to interfere with the electrons, and the mobility of undoped GaAs is preserved. The spacer layer serves to further separate the 2DEG from the ionized donors at the interface, thus increasing the mobility.

A HFET is a normally on device, just like a MESFET. If the gate is recessed, however, as shown in figure 2.3, the device is converted to enhancement mode (normally off). A recessed gate reduces the separation between the gate and the 2DEG allowing the Schottky barrier at the gate metal-semiconductor interface to completely deplete the 2DEG under the gate. The threshold of the device is adjusted by the thickness of the layer under the gate and the Al mole concentration. Because the transconductance and output resistance of the device increases as the separation between the gate and the 2DEG is reduced, enhancement HFETs are preferred to depletion HFETs [10]. In the enhancement HFET, the gate-built in voltage depletes the doped AlGaAs, which overcomes the built in potential at the

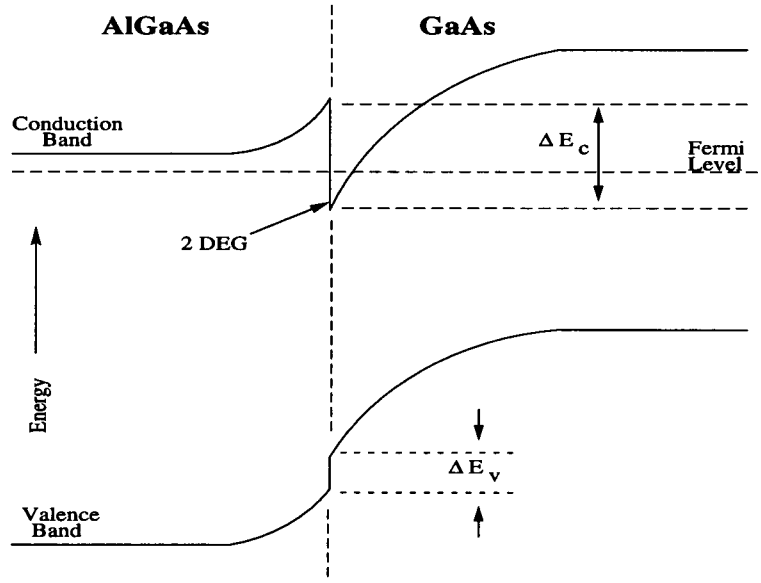


FIGURE 2.2. Energy level diagram at the heterointerface.

interface, and depletes the 2DEG. When the gate is raised above V_t (normally .2 or .3 volts) the built-in voltage of the heterojunction pushes the depletion region back into the undoped AlGaAs layer, thus allowing current to flow because the 2DEG is no longer depleted.

The main parameters of enhancement HFETs are the Al mole concentration and the thickness and doping of the AlGaAs layer. Increasing the Al mole concentration allows for higher turn on voltages, which reduces unwanted injection of extra-energetic electrons from the GaAs to the AlGaAs, and permits a higher electron concentration in the channel without conducting in the spacer layer. Higher Al mole concentrations also serves to reduce gate leakage. To maximize the switching speed, the donor layer should be as thin as possible and highly doped. The limit is achieved at a Si doping concentration of about $10^{18} \frac{atoms}{cm^3}$. Above this level, gate leakage becomes excessive. P channel devices can be formed using Be doped AlGaAs.

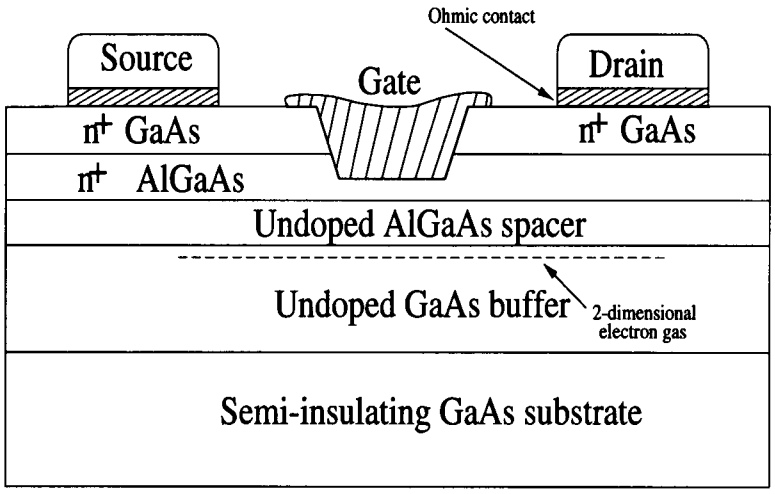


FIGURE 2.3. Cross section of enhancement HEMT.

In a standard HFET, the channel layer is lattice matched to the donor layer and the spacer layer. If the channel layer is replaced by a semiconductor that is not lattice matched to the donor, the device is called a pseudomorphic HEMT. For example, if the channel layer of figure 2.3 is replaced by InGaAs, lattice matching no longer exists. The InGaAs crystal conforms to the GaAs crystal in the horizontal dimension, but in order to do so, must strain, and the device becomes a pseudomorphic, or 'strained' HFET. Because lattice mismatch allows for higher flexibility in fabrication, and the low-field mobility and peak velocity of free electrons in (In,Ga) are among the highest of all semiconductors, pseudomorphic HFETs outperform the standard lattice matched HFET. The lower bandgap of InGaAs also allows for better carrier confinement and lower output conductance. The first transistor to break the 200 GHz barrier was a pseudomorphic HFET. A .1μm InP substrate fabricated at Hughes Research Labs had a transconductance of $1160\frac{ms}{mm}$ with an extrapolated cut-off frequency of 205 GHz [2]. A 50 percent higher carrier velocity has been reported for pseudomorphic InGaAs compared to the standard GaAs HFET.

A HFET device similar to a MOSFET can be achieved if the wider bandgap layer (donor layer) is not doped [3]. The undoped AlGaAs layer is used as a gate insulator and the n+ GaAs layer is used as a metal gate. This device allows for threshold voltages to be more easily controlled because it is no longer a strong function of the thickness and doping density of the donor layer, rather it is determined by the difference in work functions at the two GaAs/AlGaAs interfaces. Because there are no donors under the gate, the regions outside the gate (source, drain) must be made conductive by ion implantation. When the gate is forward biased, electrons accumulate at the AlGaAs/GaAs interface to form the conduction channel. Devices such as this are called HIGFETs, heterostructure insulated gate FET, and are the GaAs analog to the MOSFET.

2.2 The Honeywell Process

The operational amplifier presented in this paper was fabricated at Honeywell using their self-aligned delta-doped complimentary HIGFET process [11,12,13,14,15,16], which Honeywell calls CHFET. A cross section of the heterostructure grown by Molecular Beam Epitaxy, MBE, is shown in figure 2.4 and a cross section of the process is shown in figure 2.5. The heterostructure of the Honeywell process is similar to a single heterojunction pseudomorphic transistor, except a layer of Si doping has been added beneath the pseudomorphic channel. No dopants exist in the wider bandgap GaAs layer, rather this layer is used as a gate insulator. Majority carriers are created by ion implantation into the source and drain. Delta doping refers to an approximate atomic thickness of silicon dopants and serves to shift both the n-HIGFET and p-HIGFET threshold voltages to more

negative values [17]. A delta-doped HIGFET also has a higher 2DEG density than a conventional HFET of the same spacer width.

A high AlAs mole fraction (x value:$Al_xGa_{1-x}As$) of .75 and a high InAs mole fraction (y value:$In_yGa_{1-y}As$) of .25 in the channel serves to reduce the gate leakage current. A InAs mole fraction of .25 is about as high as the pseudomorphic layer allows for a 150 angstrom thick channel without degrading device performance. With this process, Honeywell has fabricated HIGFETs with transconductances greater than $300\frac{ms}{mm}$ for N-type devices and $70\frac{ms}{mm}$ for P-type devices for 1μm gate length devices.

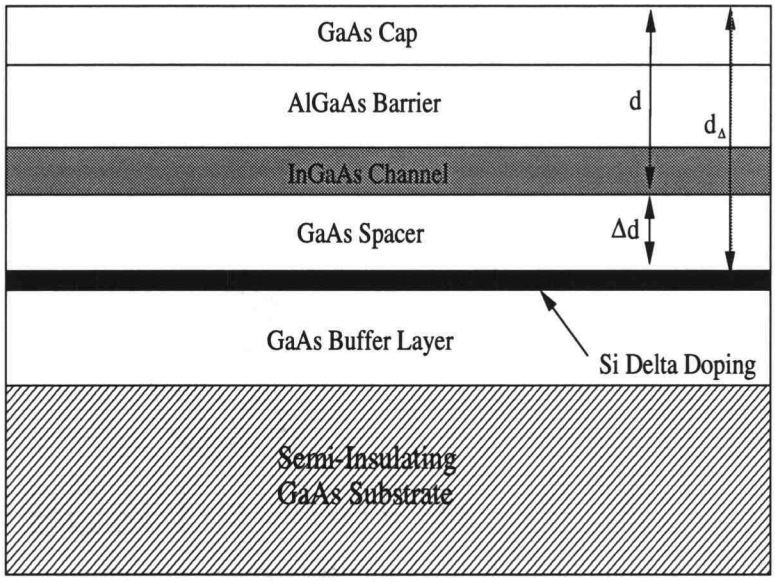


FIGURE 2.4. Cross section of HIGFET heterostructure.

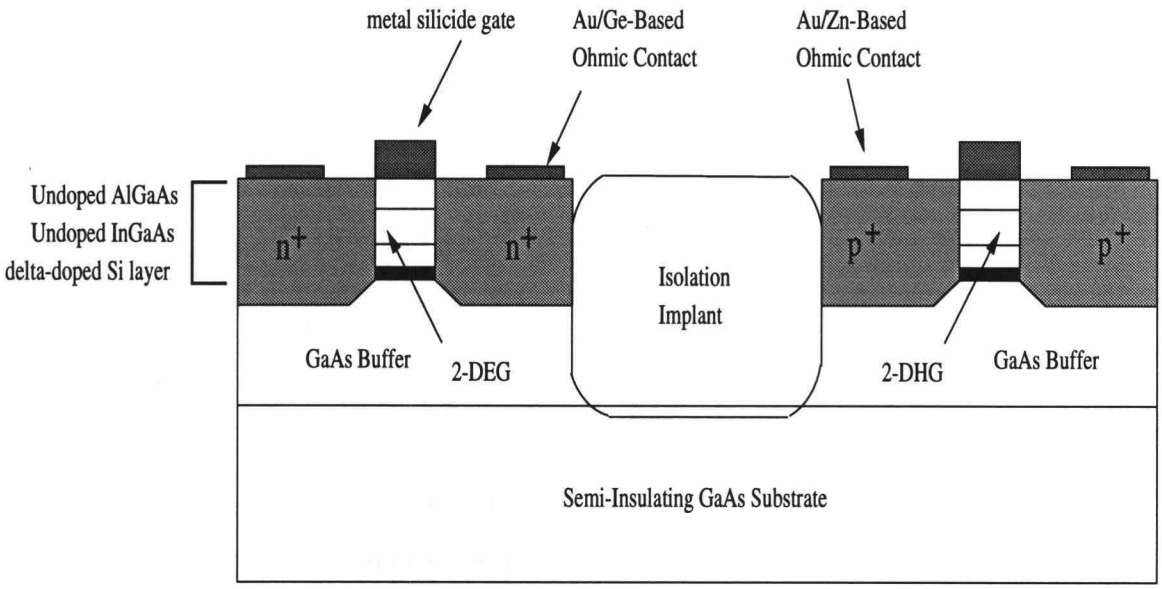


FIGURE 2.5. Delta-doped CHIGFET process cross section.

3. ANALOG CIRCUIT DESIGN USING THE HIGFET

As stated previously, Si technology, in particular, CMOS, has been the industry standard for analog applications. As speed and bandwidth requirements grow, however, CMOS will struggle to keep pace. A device that will be able to keep up, and has some of the same desirable characteristics as CMOS, is the C-HIGFET. A problem that has kept complementary heterostructure FETs out of the picture is that it has been difficult to fabricate a P-type device with a high transconductance. Recently, such devices have been successfully fabricated. Because the P-type transconductance is not nearly as high as the N-type, they only serve as high impedance loads and current sources. The main limitation of the HIGFET is its gate leakage through the Schottky diode gate. At a gate bias of about 1.5 volts, excessive current begins to flow into the gate-to-drain and gate-to-source diodes. However, this leakage is significantly lower in CHFET technology than MESFET technology. Because of this limitation, the voltage swing on the sources and drains of the op-amp will be limited.

The operational amplifier that was designed and laid out at OSU and fabricated at Honeywell is shown in figure 3.1. This op-amp is an OTA (operational transconductance amplifier), which is very popular in switched capacitor implementations. It has fully-differential inputs and fully-differential outputs. The fully-differential implementation has several advantages compared to single-ended amplifiers. The fully-differential implementation increases the gain and output swing by a factor of two. Assuming no mismatch, the common-mode rejection ratio and

power supply rejection ratio are infinite because the output signal is the difference between two outputs, not one output and ground. Errors due to input offset voltage are also eliminated and even-order harmonics are canceled. The main disadvantage of the fully-differential circuit is that it requires a common-mode feedback circuit to stabilize the common-mode output voltage. The common-mode feedback circuit is implemented in continuous time, and is shown in figure 3.2. Also laid out with the op-amp is a 1pF compensation and load capacitor on each end. The op-amp is a standard fully-differential cascode topology, with current source load biases provided by transistors J3 and J4. The transistor J1N provides common-mode sensing, and prevents J2P and J2M transistors from coming out of saturation if the input common-mode voltage changes. The design specifications for the op-amp are a DC gain of 60dB, which is typical for switched capacitor circuits, a unity-gain bandwidth of at least 2 GHz, and a slew rate of $1000\frac{v}{\mu s}$ for fast switching speeds. Because the Honeywell HIGFET is the GaAs analog to the MOSFET, a similar current-voltage relationship exists. A new charge control model has been developed and used successfully by Shur et. al. [18]. The op-amp was designed using the MOSFET equations with parameters supplied by Honeywell, such as the threshold voltages for the n and p transistors, gain term β, and channel length modulation factor λ. It was then simulated using HSPICE and the JFET model parameters supplied by Honeywell. Honeywell finds that by simply converting the threshold voltage of a JFET to a positive value, effectively changing the device from depletion to enhancement, high-speed simulations match experimented results well for digital applications. This is exactly what was done here for the simulation of the op-amp.

3.1 Operational Amplifier Design

The slew rate of the op-amp determines how fast the output can follow the input, and is a function of the current being supplied to the load. It is defined as

$$SR = \frac{I}{C_L} \tag{3.1}$$

where I is the current in each branch of the op-amp and C_L is the load capacitance. This is of course neglecting parasitic capacitances on the output node. Substituting a slew rate of 1000 $\frac{v}{\mu s}$ and a load capacitance of 1pF, the current is found to be 1mA.

If it is assumed that the op-amp has a one pole roll-off, then the DC gain and the -3dB frequency can be related to the unity gain frequency as:

$$a_v \omega_p = 1 * \omega_u \tag{3.2}$$

where a_v is the DC gain and ω_p and ω_u are the -3dB and unity-gain frequencies, respectively. The DC gain a_v is a function of the transconductance of the driver and the output conductance and the -3dB roll-off frequency is determined by the lowest frequency pole; thus, the equation above can be rewritten as:

$$\left(\frac{g_{m(driver)}}{g_{out}}\right)\left(\frac{g_{out}}{C_L}\right) = \omega_u \tag{3.3}$$

The output conductances cancel and the driver transconductance can be found in terms of the load capacitance and the unity gain frequency:

$$g_m = C_L \omega_u = C_L 2\pi f_u \tag{3.4}$$

substituting 2 GHz for f_u and 1pF for C_L the transconductance of the drivers is found to be g_m=1.257x10^{-2}s.

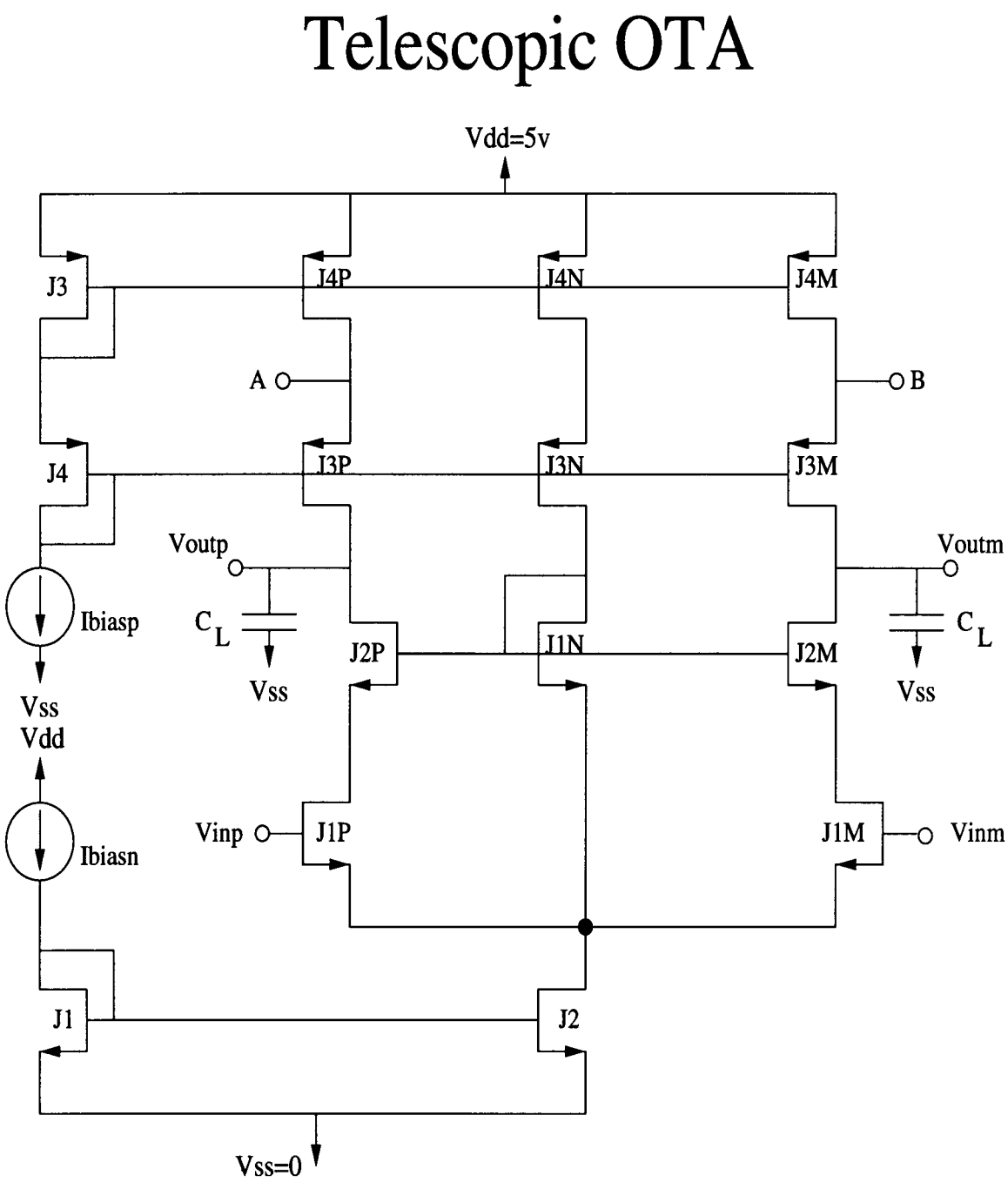


FIGURE 3.1. Fully-differential operational amplifier.

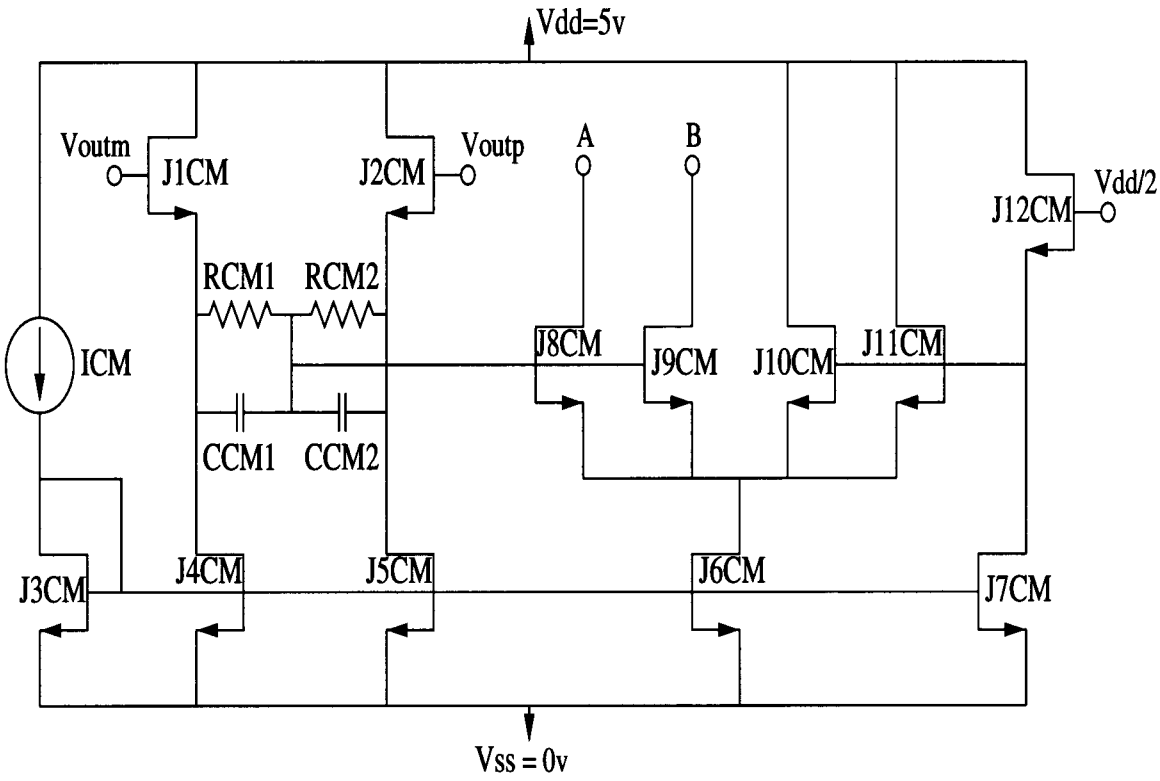


FIGURE 3.2. Common-mode feedback circuit.

The driver transconductance and current is used to determine the aspect ratio of the drivers, which is the ratio of width to length for the device. The standard MOSFET equations are used here, and the current-voltage relationship for the HIGFET in saturation is given as:

$$I_{ds} = \beta \frac{W}{L}(V_{gs} - V_t)^2 \tag{3.5}$$

where BETA is:

$$\beta = \mu \frac{\epsilon}{d + \Delta d} \tag{3.6}$$

where μ is the mobility of the 2DEG, ϵ is the dielectric constant of GaAs, and d+Δd is the distance from the gate to the 2DEG. The term $\frac{\epsilon}{d+\Delta d}$ is analogous to the oxide capacitance of the MOSFET.

The transconductance is given as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = 2\sqrt{\beta \left(\frac{W}{L}\right) I} \tag{3.7}$$

and solving for the aspect ratio of the driving transistors gives:

$$\left(\frac{W}{L}\right)_n = \frac{\left(\frac{g_m}{2}\right)^2}{\beta_n I} \tag{3.8}$$

Honeywell provided the parameters for their N and P-type HFETs, in which β is specified. For the n-type device β is 3.0x10^{-4}s for a 1.0μm wide device. The aspect ratio for the driving transistors is therefore approximately W/L=132.

One of the drawbacks of the HIGFET is that its swings are limited because the gate contact is a Schottky barrier that will conduct excessively if the forward bias voltage becomes too large. The design therefore assumes a large signal voltage swing of a few volts. If the minimum saturation voltage across the P-type current sources is taken to be .5 volts then the aspect ratio can be found. Manipulating the equation above, and setting (V_{gs} - V_t) to V_{dsat}, the aspect ratio is given as:

$$\left(\frac{W}{L}\right)_p = \frac{I}{\beta_p V_{dsat}^2} \tag{3.9}$$

and substituting 1mA for I and $3.0\text{x}10^{-5}$ for β_p the aspect ratio is 133. Note that the aspect ratio is inversely proportional to the square of V_{dsat} and the low mobility, which means that if the op-amp were designed for higher swing, the width would be much greater, causing excessively high parasitic capacitances and excessively large transistors.

Because the N-channel devices have a β an order of magnitude higher than the P-channel, the saturation voltage can be lower. If V_{dsat} of the N devices are assumed to be .15 volts, then by the same procedure as above, the aspect ratio of the N-devices is 148.

The aspect ratio of the tail current transistor J2 can be found similarly, but because it must sink the current from both branches, the current must be set to 2mA. The aspect ratio of this device then becomes 296.

A constant current sink must be assumed to bias the load devices. If I_{biasp} is assumed to be 200uA, and the same current of 200uA flows through the common mode sensing branch, then as above, the aspect ratio turns out to be 27 for J4N and J3N. Similarly for the tail current, a constant current source must be assumed. If I_{biasn} is also set to 200uA then the aspect ratio of J1 becomes 27.

The desired DC gain is used to determine the lengths of the devices. The single-ended DC gain is equal to the transconductance of the driver transistor divided by the output conductance, or,

$$A_v = \frac{g_{m(driver)}}{g_{out}} = \frac{g_{m(driver)}}{g\uparrow + g\downarrow} \tag{3.10}$$

where g↑ is the conductance looking up into the P-channel load devices J3M and J4M, and g↓ is the conductance looking down into the N-channel devices J2M and J1M, and are given as:

$$g\uparrow = g_{ds_{(J4P)}}\left(\frac{g_{ds_{(J3P)}}}{g_{m_{(J3P)}}}\right) = \frac{(\lambda_p I)^2}{2\sqrt{\beta_p\left(\frac{W}{L}\right)_{J3P} I}}$$

$$g\downarrow = g_{ds(driver)}\left(\frac{g_{ds_{(J2P)}}}{g_{m_{(J2P)}}}\right) = \frac{(\lambda_n I)^2}{2\sqrt{\beta_n\left(\frac{W}{L}\right)_{J2P} I}} \tag{3.11}$$

Substituting (3.11) into (3.10) and assuming that the aspect ratios of the transistors in each branch are approximately the same, the gain is expressed as:

$$A_v \simeq \frac{4\left(\frac{W}{L}\right)\beta_n\sqrt{\beta_p}}{I\left(\sqrt{\beta_n}\lambda_p^2 + \sqrt{\beta_p}\lambda_n^2\right)} \tag{3.12}$$

If it is now assumed that λ_p=$2\lambda_n$, as specified by Honeywell, then solving for λ_n gives λ_n=$.11v^{-1}$; therefore λ_p=$.22\ v^{-1}$.

It can be approximated that the λxL product is a constant by the following equation:

$$\lambda_0 L_0 = \lambda L \tag{3.13}$$

with λ_0 being $0.1v^{-1}$ and L=0.7μm. Therefore the lengths of the N and P devices become $.7\mu$m, which is the minimum size for this process. Using this value, the widths of all the devices can now be determined.

The aspect ratio of the common-mode sensing transistor J1N is still to be determined. Because this device is used to keep the driving transistors J1P and J1M in saturation if the input common-mode voltage changes, it can not have the same V_{dsat}. For example, if the input common-mode increases, the voltage at the drain of J2 increases and the voltage at the drains of the input transistors increases. If J2P and J2M were biased by a constant voltage, then the voltage at the drains of the driving transistors would decrease, forcing them out of saturation as the input common-mode voltage increased. Because there is always a constant current through J1N, its gate voltage must increase due to the voltage increase at its source.

This increase in the gate at J2P causes the source voltage of J2P to increase also. If the gate voltage of J1N is not high enough, the driving transistors will come out of saturation. This method of sensing the common-mode voltage increases the input common-mode range significantly. Because this device is diode-connected, its V_{dsat} is always equal to V_{ds}=V_{gs}. If a V_{ds} of 0.4v is assumed, then by the same procedure as above, the aspect ratio is one. Best results were obtained through simulation if the device has a Length of 7μm and a width of 10μm. The aspect ratios for all the op-amp transistors that were calculated by hand and those that were used in the layout are shown in table 3.1. For ease of layout all device widths are rounded.

Devices	calculated width	layout width
drivers	92	100
J4P,J3P,J4M,J3M	93	100
J2P,J2M	104	100
J2	207	200
J3,J4	19	20
J3N,J4N	19	20
J1	21	20
J1N	-	W=10u L=7u

TABLE 3.1. Calculated and simulated widths of op-amp transistors

4.2 The Common-Mode Feedback Circuit

In a fully-differential output amplifier, the common-mode output should be unaffected by either feedback or changes in the common-mode input voltage. Because a change in either of these will change the common-mode output voltage, separate feedback circuitry is required that stabilizes the output over a certain range of input common-mode voltage. The common-mode circuit used here is shown in figure 3.2. This circuit consists of two parts, the first is a differential-mode rejection circuit, and the second is a differential pair. The purpose of the differential-mode rejection circuit is to obtain the output common-mode voltage; to do this, the differential voltage must be eliminated. The output of the this circuit is given as:

$$V_{cmfb} = \frac{(Vout_m + \Delta V - V_{gs}) + (Vout_p - \Delta V - V_{gs})}{2} \tag{3.14}$$

$$= \frac{Vout_m + Vout_p}{2} - V_{gs} \tag{3.15}$$

Where Vout_m and Vout_p are the output common modes. The equation shows that this circuit eliminates the differential signals leaving only the common-mode output. Vout_m and Vout_p may not necessarily be equal, but their average is the output common-mode voltage. So the output of the differential-mode rejection circuit is equal to

$$V_{cmfb} = Vout_{cm} - V_{gs} \tag{3.16}$$

The voltage V_{cmfb} must be compared with another voltage such that if there is a difference, a correction is made. This is done using the differential pair in figure 3.2. The output common-mode voltage is chosen as the midpoint between the supply and ground, which is 2.5 volts. The output common mode, then, should be compared to

2.5 volts, but the output of the differential rejection circuit has a V_{gs} drop, so the differential pair must compare V_{cmfb} to (Vdd/2)-V_{gs}.

The analysis of the differential pair is as follows; if V_{cmfb}=2.5-V_{gs}, then the current through J8CM and J9CM does not change, and the common-mode output is set to 2.5 volts. If the input common-mode voltage decreases, the output common-mode voltage increases and $V_{cmfb} > 2.5\text{-}V_{gs}$; therefore the current in J8CM and J9CM increases (while the current in J10CM and J11CM decrease) thus lowering the potential at nodes A and B, therefore lowering the potentials at Voutp and Voutm. The current in J8CM and J9CM is adjusted until V_{cmfb} is equal to 2.5-V_{gs}, at which point the output common-mode voltage will become 2.5 volts.

It is arbitrary as to what value of current to use for the constant current source and what aspect ratio to use for the current mirrors. It is important, however, that the same V_{gs} be dropped across J1CM, J2CM and J12CM; therefore, the same current must flow in each of these branches. If a constant current source of 100uA is assumed, and a width of 20μm for J3CM, then J4CM, J5CM, and J7CM must also have a width of 20μm (the length is set to 0.7μm). The Width of J1CM, J2CM and J12CM is also arbitrary, but they must be the same to give the same V_{gs} drop, so for simplicity they are set to 20μm as well. A current of 500uA is arbitrarily chosen to flow through J6CM. If V_{dsat} of J6CM is chosen as 0.1 volts, then its aspect ratio is 166, which gives a width of 116μm, which is rounded down to 100μm for simplicity. Simulation shows that a width of 80μm works well for the differential pair transistors J8CM, J9CM, J10CM, and J11CM.

3.3 Frequency Response

It should be noted that the derivation of the lengths of the current source and sink devices were found using a DC gain, A_v, of 1000. This is in fact the gain of only one side. The fully differential gain would therefore be 2000. So the expected simulation result for the fully-differential output is 2000. If a gain of 500 were assumed, for a fully differential gain of 1000, the lengths of the sink and source devices would end up being smaller than minimum size. Figures 3.3 shows the frequency and phase response for the amplifier. The results of figure 3.3 were obtained using the fully-differential output as shown in figure 3.4, where the fully differential output is the voltage across the output nodes. The expected gain from hand analysis was 2000, which is close the simulated value of 2,240 (67dB). The fully-differential unity-gain frequency is 1.7 GHz and The phase margin is 77.3 degrees.

As stated previously, the desired characteristics of the amplifier are a DC gain of 60dB and a unity-gain frequency of at least 2 GHz. At this stage of the design the fully-differential gain is 67db and the UGF 1.7 GHz, so the design requirement for the UGF is not met. There are a few solutions to obtain the desired results. One solution is to increase the width of the driving transistors. This would result in higher gain and bandwidth according to equations 3.7 and 3.12. Since the widths shown in table 3.1 have been used in the layout, altering the widths offers only an academic solution. The other solution, which can be used in the actual testing of the op-amp, is to increase the biasing current sources. This will increase the transconductance of the drivers as shown by equation 3.7, and therefore increase the UGF. The gain does decrease however, according to equation 3.12. If both of the current sources are increased to 450uA then the fully-differential DC gain is reduced to 60.27dB

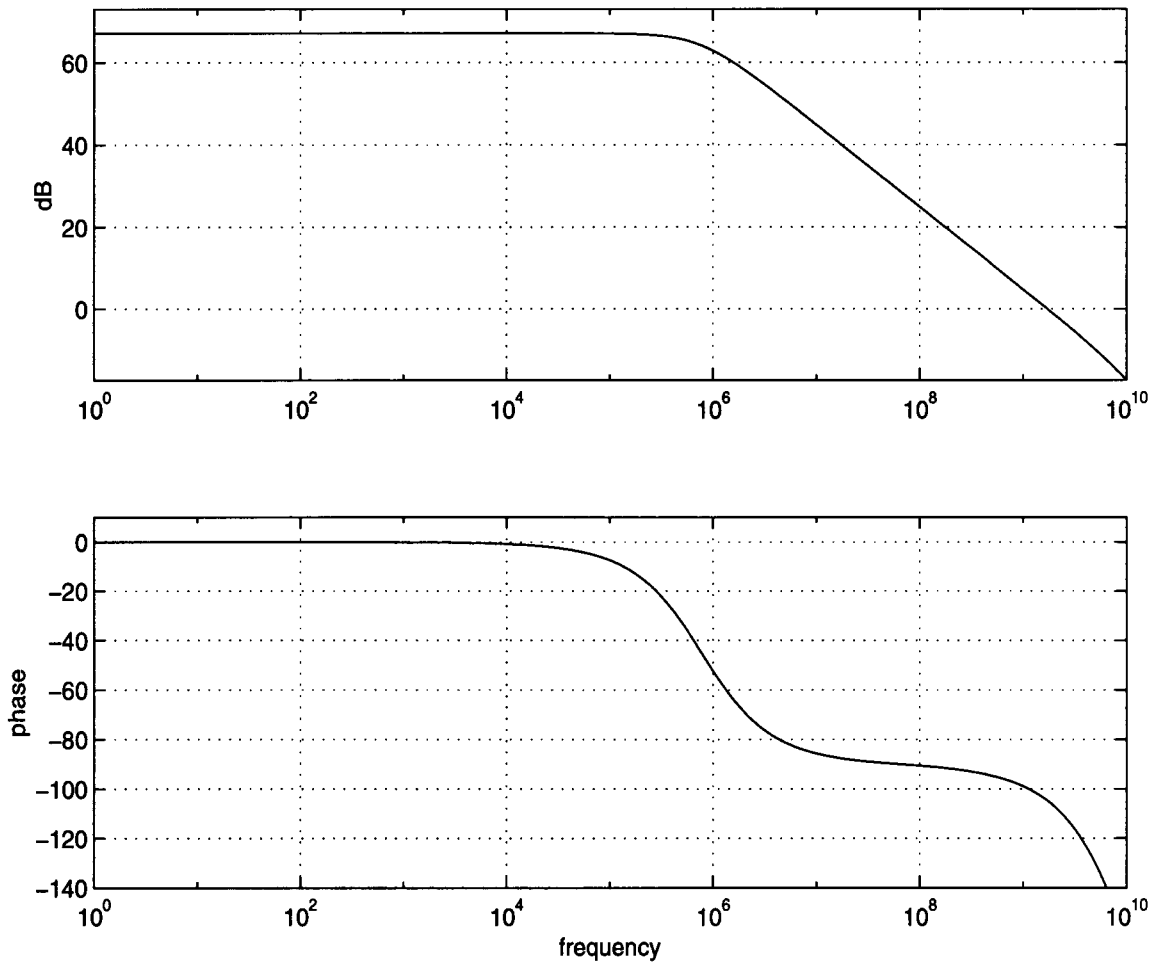


FIGURE 3.3. Frequency and phase response for a bias current of 200uA.

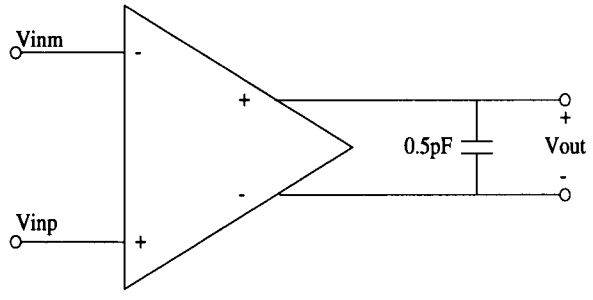


FIGURE 3.4. Circuit used to determine fully-differential frequency response.

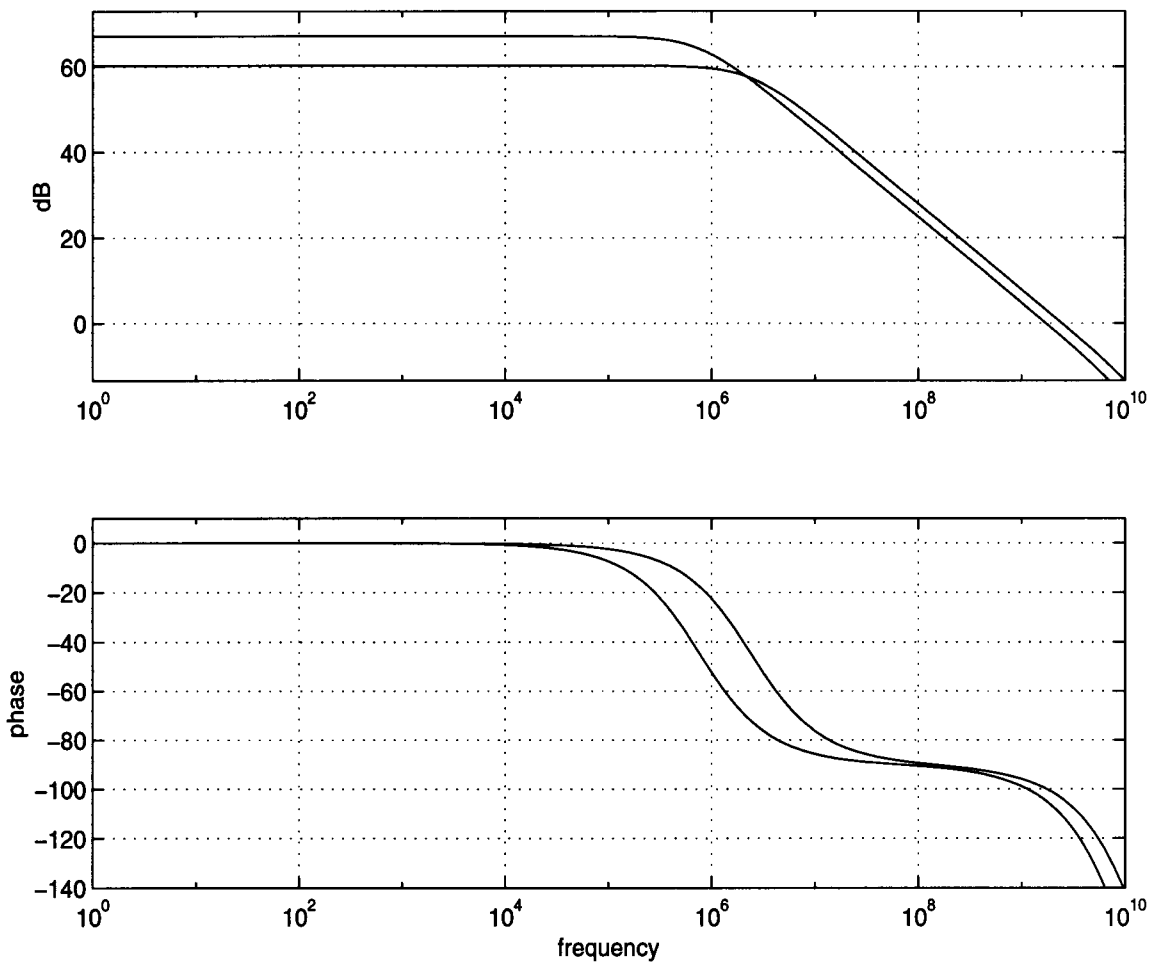


FIGURE 3.5. Bode plots for a bias current of 450uA compared to 200uA.

and the UGF is increased to 2.44 GHz. Since at different values of biasing current there are different input common-mode ranges, a new input biasing voltage has to be chosen for a change in biasing current. At a biasing current of 450uA, an input voltage level of 1.2 volts gives the desired output common-mode level of 2.5 volts. A plot of the frequency response for the amplifier using 450μA is compared against the response of the the amplifier using 200μA in figure 3.5. As the figure shows, the DC gain is reduced while the UGF is shifted out, and the phase response is also shifted out giving a phase margin of 76 degrees.

3.4 Input common-mode range and large signal output swing

The input common-mode range is the range of DC voltages that the input is allowed to be biased at while keeping all transistors in the branch in saturation. It is obtained by determining when one of the transistors in the branch comes out of saturation as a function of input voltage level. For the simple single-ended output amplifier of figure 3.6, it is easy to obtain the CMR. The minimum common-mode voltage that is allowed is that which forces the tail current transistor out of saturation. When observing the common-mode range, the amplifier can be looked at as a source follower. As the input level decreases, the tail node will also decrease, eventually forcing the tail current transistor out of saturation. The minimum voltage level is given as:

$$Vcm_{(min)} = Vgs_{(in)} + V_{dsat} = 2V_{dsat} + V_t \tag{3.17}$$

because for saturation we require that V_{ds}>V_{gs}-V_t. Similarly, as the input level increases, the driving transistor will eventually come out saturation because as the input level increases, the tail node also increases, and the output node decreases,

causing V_{ds} across the driving transistor to decrease, until it eventually comes out of saturation.

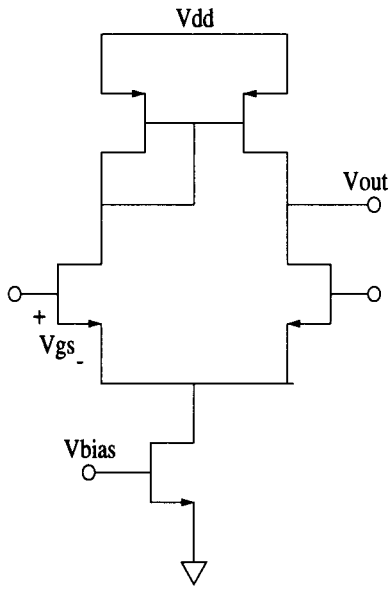


FIGURE 3.6. Simple single stage op-amp.

The analysis of a fully-differential amplifier such as that presented here is not as easy as described above because the circuit is in a cascode topology and the output voltage level is set by the common-mode feedback. It cannot be assumed that $Vcm_{(min)}$ is the same as that given above because when the input level is low, either J2 or J4P may be out of saturation, and it is not a trivial matter to perform hand analysis of this. It is also not known for what values of input level the common-mode feedback circuit will set the output to the desired level. If it is assumed that J2 comes into saturation at a higher voltage than J4P, then the $Vcm_{(min)}$ can be assumed according to the above equation, and is .51 volts because V_{dsat} is .15v and V_t is 0.2v. The common-mode feedback, however, might not necessarily begin to operate as desired until a higher input voltage. Because of these difficulties, the characterization of the input common-mode range is performed by simulation. By applying the same input level to both inputs and sweeping from zero to V_{dd}, the

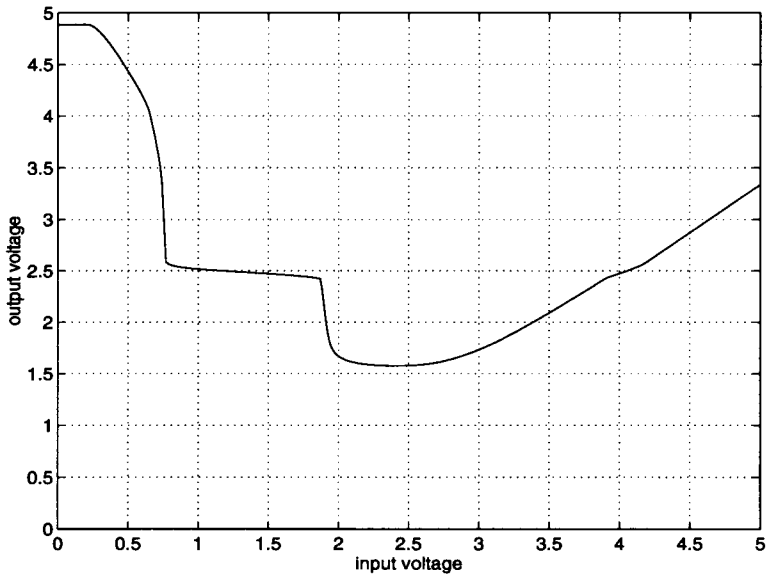


FIGURE 3.7. Input common-mode range.

CMR can be determined by observing when the output is set to a constant value. Figure 3.7 shows a plot of the output as a function of the input. As the figure shows, there is a range of input voltage such that the output is linear about 2.5 volts. The input CMR range is .77 to 1.87 volts. In this range the amplifier will have the desired gain, and the common-mode output will be near 2.5 volts, but not exactly. To achieve a common-mode output of exactly 2.5 volts it must be determined which input level gives a common mode output of 2.5 volts. This occurs at an input of approximately 1.2 volts. A more common method of determining the input common-mode range is to apply a DC sweep on an input in a unity-gain configuration shown in figure 3.13. Here, the input CMR is determined from the range in which the output follows the input and has a slope of unity. Figure 3.8 shows the result of such a simulation and the results are identical to that obtained using the other method.

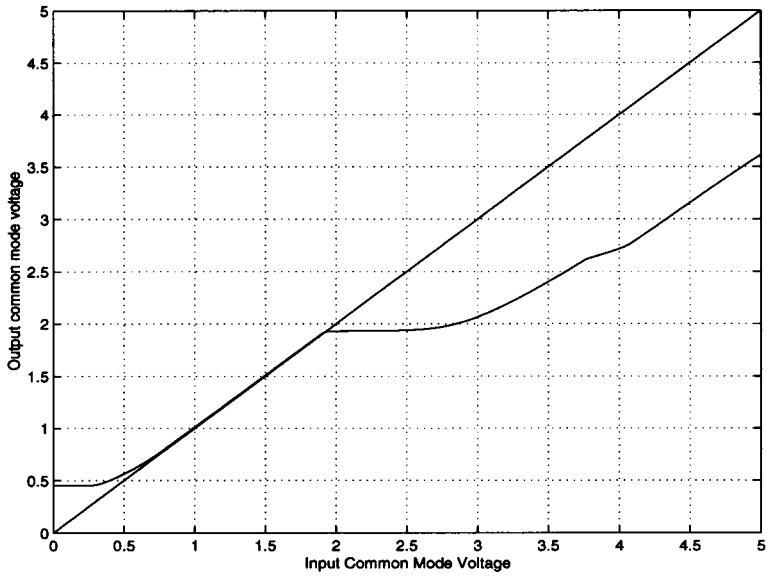


FIGURE 3.8. Common-mode range using unity-gain feedback.

The large signal output swing is determined similarly to the method above, but one of the inputs is set to the desired bias level. By setting V_{inm} to 1.2 volts and sweeping V_{inp} from 0 to 5 volts, the output large signal swing can be determined, and is shown in the figure 3.9. The figure shows that the large signal output appears to be between 1.4 and 3.6 volts, centered at 2.5 volts. This is of course with some non-linearity. A zoomed in view, figure 3.10, shows the non-linearity. The amplifier appears to be very linear over 1v peak-to-peak, with some non-linearity and a decrease in gain as the output swing increases. This plot can be used to approximate the single-ended DC gain of the amplifier. The DC gain is simply the slope of the curve at the input voltage of 1.2 volts. By taking the derivative of the curve at 1.2 volts, the gain is shown to be 54dB, as was determined by the ac analysis.

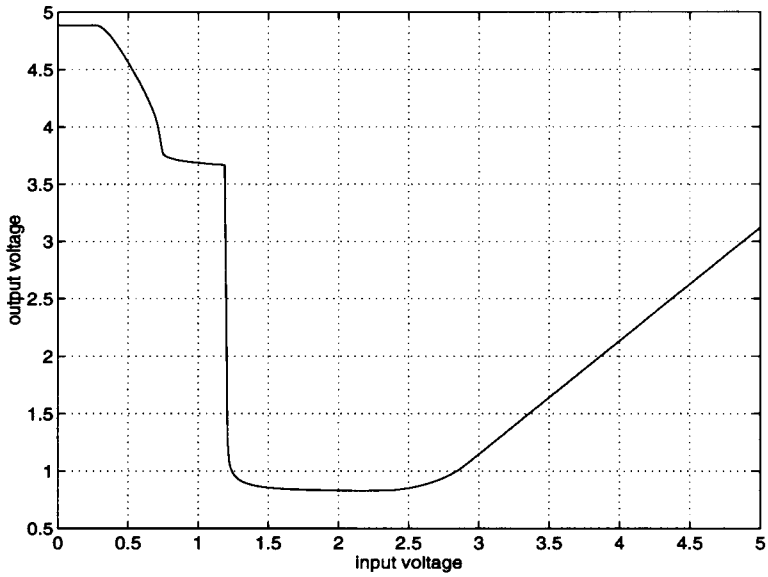


FIGURE 3.9. Large signal output swing.

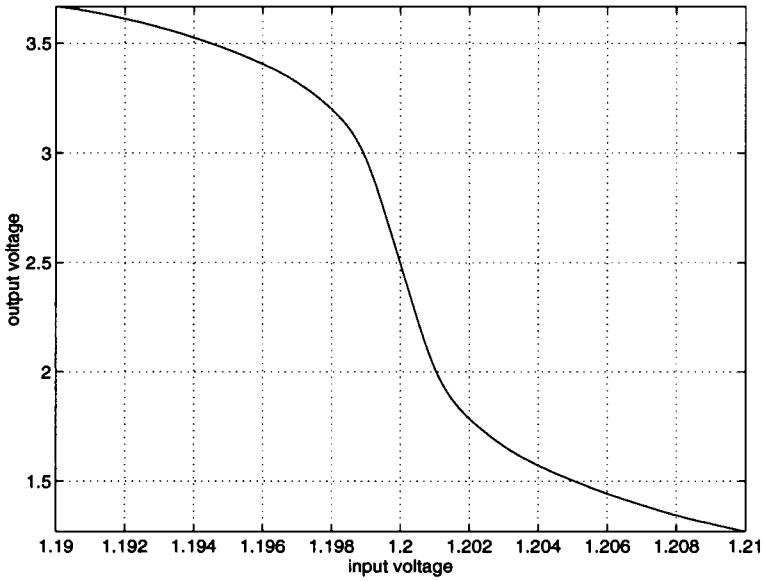


FIGURE 3.10. Large signal output swing (zoom view).

3.5 Harmonic Distortion

The linearity of the amplification is characterized by its total harmonic distortion when a pure sine wave is applied to the input of the amplifier. As figure 3.10 shows, the transfer curve is not linear, and the distortion increases as the desired output swing increases. THD, the Total Harmonic Distortion is defined as follows:

$$THD = \frac{\sqrt{a_2^2 + a_3^2 + a_4^2 + ... + a_n^2}}{a_1} \tag{3.18}$$

where a_m represents the magnitude of the mth harmonic. Simulations were performed on the amplifier to obtain the THD at various desired output ranges in open-loop and unity-gain feedback configurations with perfect matching assumed. Table 3.2 shows the results for various input signal levels that were required to meet the desired single-ended output swing in open-loop configuration. The input signals are applied 180 degrees out of phase to give maximum fully-differential gain. For a single-ended output swing of 2 volts$_{p-p}$ the THD as determined by SPICE is 20.5 percent. This is large. Good results do not occur until the single-ended output swing is about 1 voltv_{p-p}. The results of table 3.2 were obtained through the 10th harmonic. Figure 3.11 shows the 32,768 point FFT with rectangular windowing of approximately 10 cycles of a 1 KHz sine wave that produced a single-ended 2 volt peak-to-peak output swing. The fundamental is at 1 KHz, and the odd harmonics, 3rd at 3 KHz, 5th at 5 KHz, and so on, are also shown. Table 3.3 shows the results using unity-gain feedback. Due to the nature of unity gain feedback, only one signal is applied to the input, and only one signal is observed at the output. As long as the input signal level is less than the input common-mode range (clipping occurs otherwise), the THD is good.

Input (v_p mv)	Single-ended output range (v_{p-p} volts)	THD %
2.75	2	20.5
1	1.4	10.6
.5	1	2.5
.25	.5	.2

TABLE 3.2. THD as a function of desired output swing in open-loop configuration.

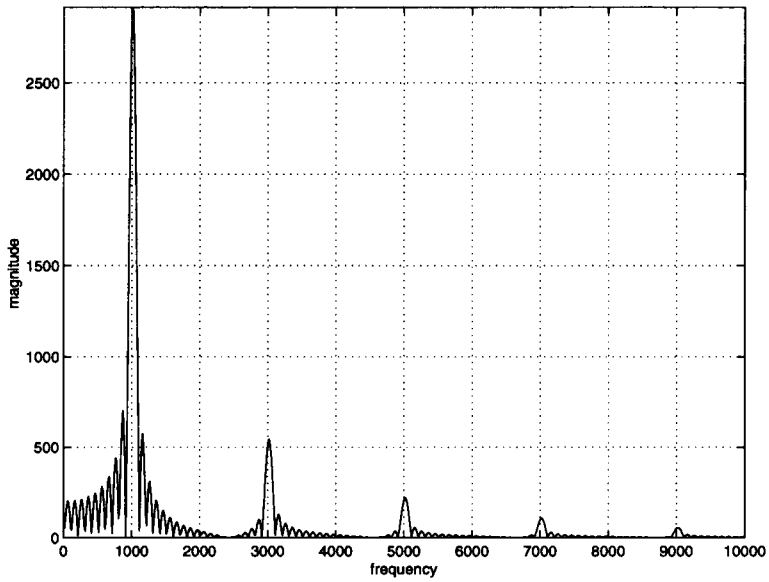


FIGURE 3.11. FFT of single-ended output with 20.5% THD (open-loop).

Input (V_p volts)	THD %
1	10.85
.75	2.85
.5	.29
.25	.13

TABLE 3.3. THD as a function of input signal level with unity-gain feedback.

3.6 Common mode rejection ratio

Theoretically, the common-mode gain for this amplifier is zero. This assumes a perfectly symmetric layout and no processing errors. This is because whatever common-mode gain that exists for one side is subtracted by the other, leaving a net common-mode gain of zero, and an infinite common-mode rejection ratio, CMRR. Because processing errors have not been considered in the SPICE netlist, it is not possible to determine by simulation the fully-differential CMRR. By performing a half-circuit analysis on the amplifier, the common-mode gain of one branch is found to be,

$$A_{cm} = \frac{-G_{m(eff)}}{g\uparrow} \tag{3.19}$$

where $G_{m(eff)}$ is the effective transconductance of the input due to source degeneration of the tail current transistor J2, which can be approximated as g_{ds_n}, and $g\uparrow$ is the conductance looking into the P-type sources. Substituting $\lambda_n I$ for g_{ds_n} and the conductance of $g\uparrow$ gives,

$$A_{cm} = \frac{-\lambda_n g_{m(p)}}{\lambda_p^2 I} = \frac{2\lambda_n}{\lambda_p^2}\sqrt{\frac{\beta_p \left(\frac{W}{L}\right)_p}{I}} \tag{3.20}$$

Substituting the appropriate values gives a single ended common-mode gain of -10. This is a very large common-mode gain, and it causes the single-ended CMRR to by only 40dB. If there are any fabrication mismatches, this poor CMRR may be apparent. Simulation shows, however, that the DC common-mode gain is 66mv/v, or -23.6dB. This discrepancy of the hand analysis compared to simulation is caused by the common-mode feedback circuit because it sets the output voltage. Figure 3.7 shows that in the region of operation, the slope of the curve, which is the common-mode gain, is about $10\frac{mv}{.1v}$, or -20dB. By simulating the common-mode gain and the differential-mode gain independently, a plot of the single-ended CMRR can be obtained as is shown in figure 3.12. Simulation shows the DC CMRR to be 85dB.

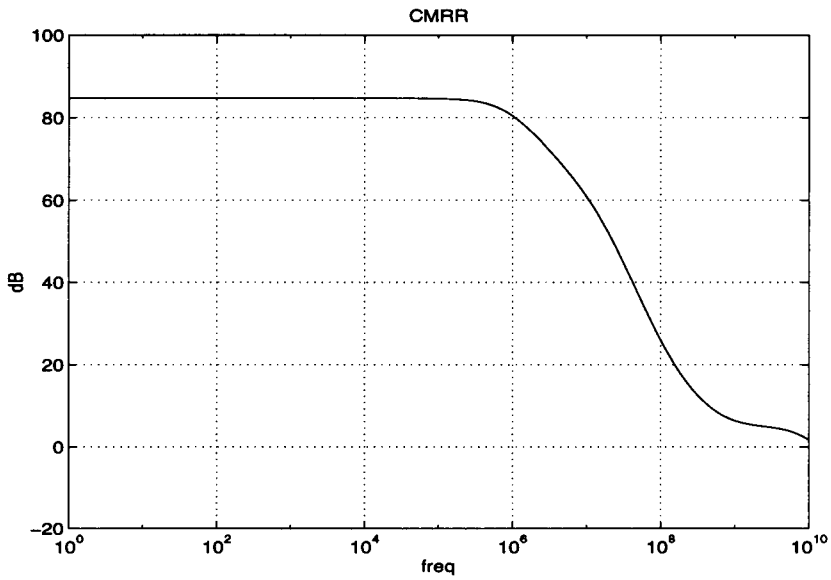


FIGURE 3.12. Common-mode rejection ratio.

The CMRR is a function of the quality of the tail current sink. The high conductance of the tail current transistor J2 compared with the very low conduc-

tance ($g\uparrow$) of the P-type sources produces the large common-mode gain as shown by hand analysis.

3.7 Stability, slew rate, transient response, and DC offset voltage

Because the amplifier has a fully-differential phase margin of about 76 degrees, it is assumed stable. In order to test for stability the amplifier is set up in a unity-gain feedback configuration as shown in figure 3.13. Because the amplifier is fully-differential, there are two configurations to test. Because of symmetry, however, the results would be the same for both cases. The unity-gain feedback configuration is the least stable configuration for an amplifier, therefore if it is stable under this test, it will be stable under higher gain configurations. To test for stability, a step is applied at the input, if the output follows the input without increasing oscillations the amplifier is assumed stable. The slew rate of the amplifier is the rate at which the output can change, and can be determined from the stability test transient response. Figure 3.14 shows the result of a transient simulation. The output does follow the input, therefore the amplifier is stable. The slew rate can be determined directly from the figure. There are two slew rates to consider; one is the charging rate of the load capacitor, the other is the discharging rate. The charging slew rate is determined to be approximately $1700\frac{v}{\mu s}$, and the discharge slew rate is approximately $875\frac{v}{\mu s}$. Simulation shows the the op-amp to settle to within .1% of its final value in under 2.4ns for a 1 volt negative differential step on the output and it settles to within .2% of its final value in under 1.3ns for a 1 volt positive differential step on the output. Assuming that this settling time comprises 1/2 the period of the sample clock in a switched-capacitor circuit, this suggests clock rates on the order of 200 MHz.

The DC input offset voltage is the difference between the output and the input with a DC signal applied at the input. The test for this can be done using the unity-gain feedback configuration and applying the nominal DC bias to the input and observing the output level. The difference between the input and output is the input offset voltage, and was determined to be 11mv.

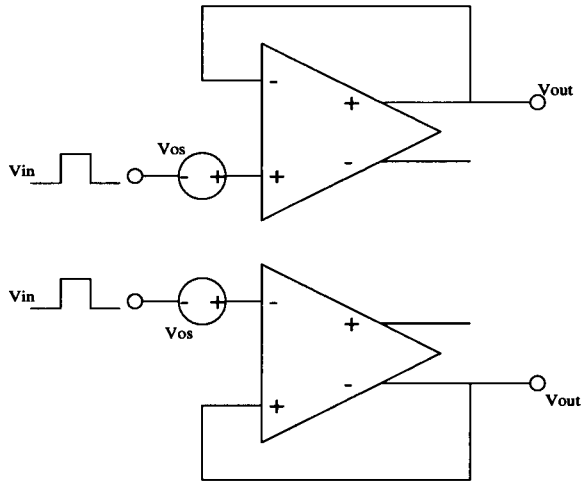


FIGURE 3.13. Unity-gain feedback configurations.

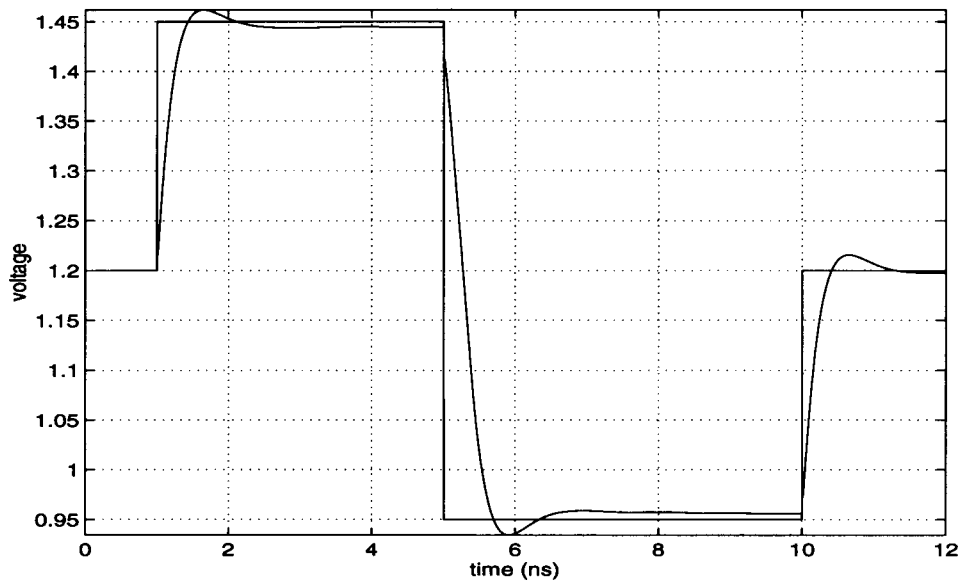


FIGURE 3.14. Transient response to verify stability and to determine slew rate.

3.8 Power supply rejection

The power supply rejection is the amount of ripple that appears at the output given a ripple added to either of the supplies with the differential input set to zero. The power supply rejection ratio, PSRR, is the gain of the open-loop frequency response divided by gain due to power supply noise, or

$$PSRR = \frac{Av}{Add_{|Vdiff=0|}} \tag{3.21}$$

Idealy, because the differential output is taken as the difference between the two outputs, the power supply rejection will cancel out, leaving an infinite PSRR. Realistically however, device mismatches will cause some power supply rejection. Simulations were done to find the single-ended power supply rejection for both the supply and ground, then these are divided into the open loop frequency gain, A_v, performed

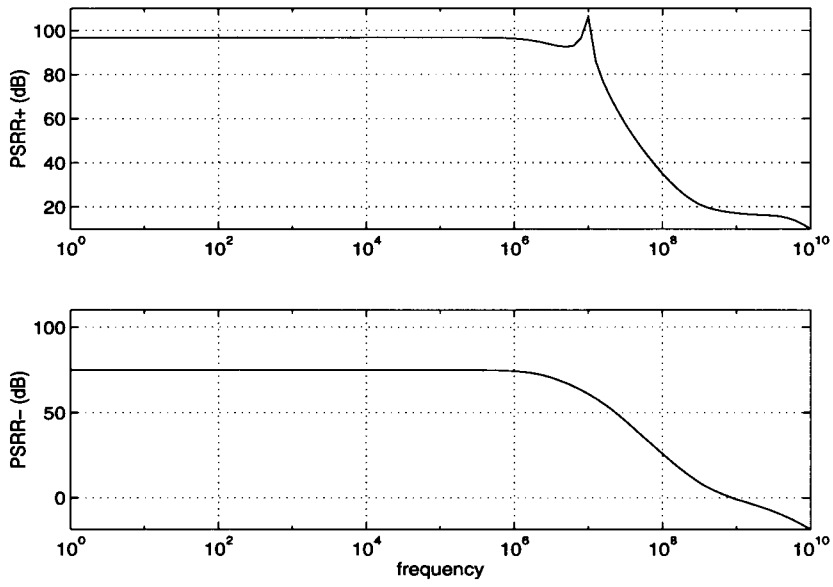


FIGURE 3.15. Supply and ground PSRR.

previously. The PSRR+ and PSRR- frequency responses are shown in figure 3.15. AC signals connected between a supply or ground and a current source have no effect in the PSRR due to the infinite input impedance of the current source. The PSRR simulation did not take into effect ripple on the gate of J12CM. If the same ground ripple is applied to the gate of J12CM, the PSRR due to ground ripple becomes one, an excessively large gain, and a potential problem for this method of common-mode feedback.

Table 3.3 shows the simulated parameters for this op-amp for single-ended load capacitances of 1pF or a fully-differential capacitance of .5pF. Due to the nature of the differential output, the CMRR and PSRR is theoretically infinite, the input offset voltage is zero, and the large signal output swing is twice that of the single-ended version.

Op-Amp Parameters	single-ended	double-ended
Open Loop Gain	54 dB	60dB
Phase Margin	83 degrees	76 degrees
Unity Gain Bandwidth	1.3 GHz	2.44 GHz
Input common-mode range	.8v-1.6v	.8v-1.6v
Large signal output swing	$1v_{p-p}$ @ 2.5% THD	$2v_{p-p}$ @ 2.5% THD
Slew rate	$\approx 875\frac{v}{us}$ discharge, $\approx 1700\frac{v}{us}$ charge	$\approx 1750\frac{v}{us}$
Input offset voltage	11mv	0
CMRR	85 dB	infinite
PSRR+	96 dB	infinite
PSRR-	75 dB	infinite
Power Dissipation	4 mW	4 mW

TABLE 3.4. Simulated op-amp parameters (load capacitance is 1pF per side).

3.9 Common-Mode Feedback Stability

The phase margin and frequency response of the common-mode loop is of importance because if it is not well compensated, it can become unstable, and it sets the maximum operating limit of the amplifier to avoid common-mode feed through. The capacitors in the CMFB circuit provide the compensation. To test for open-loop gain and phase margin, a simulation is done in which the loop between the output of the op-amp and the input of the CMFB circuit is broken as shown in figure 3.16. Because the loop has been opened, an additional CMFB circuit must be put on the output of the op-amp to load it as if the loop were closed. For correct biasing, 1.2 volts is applied into the op-amp and the ac input signals are added to the nominal 2.5 volts and applied into the CMFB circuit. The objective is to apply an oscillating common-mode signal into the CMFB circuit, which will become amplified at the output of the op-amp. This gives the open loop gain. The path the signal takes in this configuration is similar to that of a folded cascode op-amp. Figure 3.17 shows the frequency and phase response of the open loop. The DC gain is about 44dB with a phase margin of 83 degrees.

As figure 3.17 shows, the open-loop common-mode response has unity gain of only 200 MHz. This means that for any common-mode fluctuation on the output of the op-amp greater than 200 MHz, the common-mode feedback loop will have no gain, and will not be able to force the output to 2.5 volts. This represents a potentially disastrous problem for a switched-capacitor implementation where the output may change at the rate of the switching clocks. The common-mode feedback circuit can be altered such that the open loop gain is larger and the unity gain frequency is higher; however simulation shows that a unity gain of 400 MHz is the limit for this configuration. By increasing the bias current to 300uA and changing the widths of

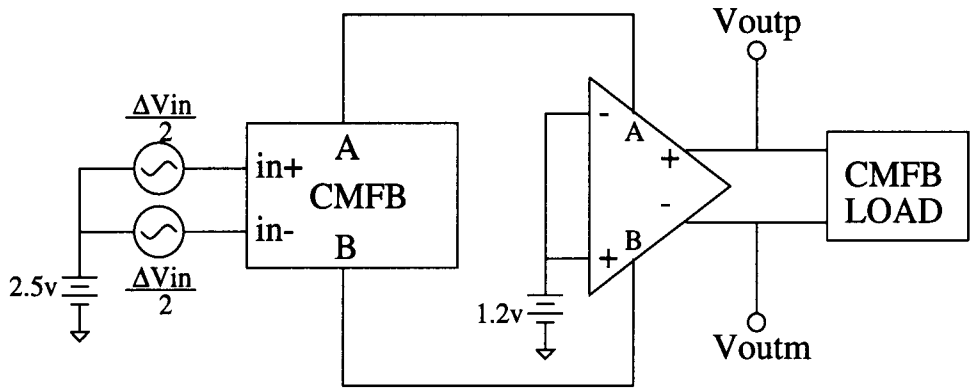


FIGURE 3.16. CMFB open-loop configuration

the devices, a gain of 500 can be achieved at a unity gain bandwidth of 400 MHz, at the expense of power and area.

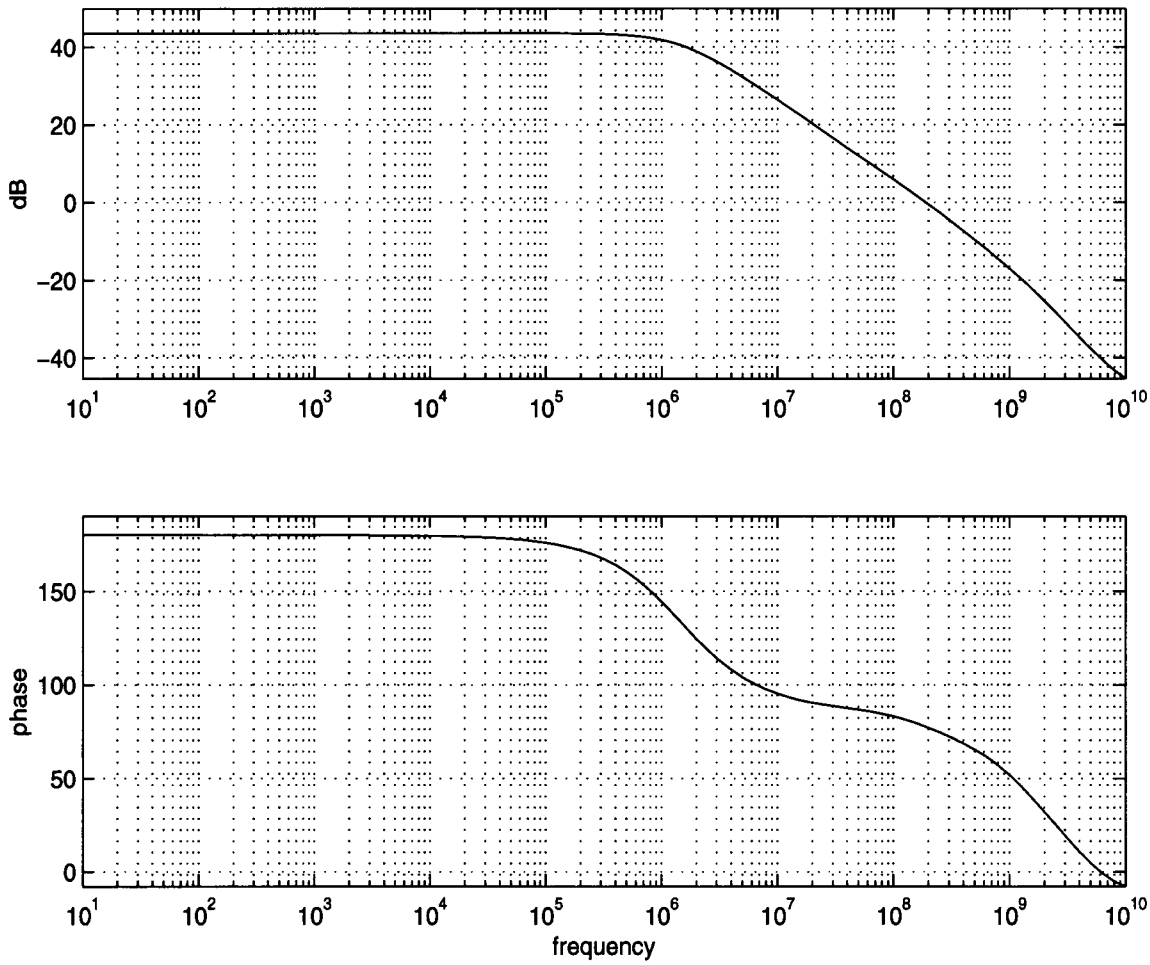


FIGURE 3.17. CMFB open-loop frequency response.

3.10 Switched-Capacitor Voltage Amplifier

The successful demonstration of a HIGFET switched-capacitor voltage amplifier would be of great importance in the areas of high-speed applications such as oversampled delta-sigma modulators. Such an amplifier, or gain cell, shown in figure 3.18, incorporates the operational amplifier presented previously. The gain cell uses two non-overlapping clocks $\phi 1$ and $\phi 2$. The operation is as follows; assume $\phi 1$ is low (switch is open) and $\phi 2$ is high (switch is closed). The source capacitor Csrc is set at the input bias level, The feedback battery forces the output to slew to 2.5 volts, and applies a bias of 1.2 volts into the amplifier. During this cycle there is no gain, only a set up of correct amplifier biasing. Then $\phi 2$ is low and $\phi 1$ is high, this is the gain cycle of the amplifier. When the switch closes, because the DC offset bias and the op-amp input bias are the same, the differential charge ΔVin is transferred through the source capacitor Csrc and into the the feedback capacitor Cfb. A charge of ΔQsrc is transferred across source capacitance Csrc, and is given as:

$$\Delta Qsrc+ = \frac{+\Delta Vin}{2} Csrc \tag{3.22}$$

$$\Delta Qsrc- = \frac{-\Delta Vin}{2} Csrc \tag{3.23}$$

This charge is transferred across the feedback capacitance Cfb, and is equal to ΔQsrc. Therefore the differential voltage at the output is;

$$\Delta Voutp = \frac{-\Delta Vin}{2} \left(\frac{Csrc}{Cfb}\right) \tag{3.24}$$

$$\Delta Voutm = \frac{+\Delta Vin}{2} \left(\frac{Csrc}{Cfb}\right) \tag{3.25}$$

And taking the fully-differential output gives;

$$Vout = Voutp - Voutm = -\left(\frac{Csrc}{Cfb}\right) Vin \tag{3.26}$$

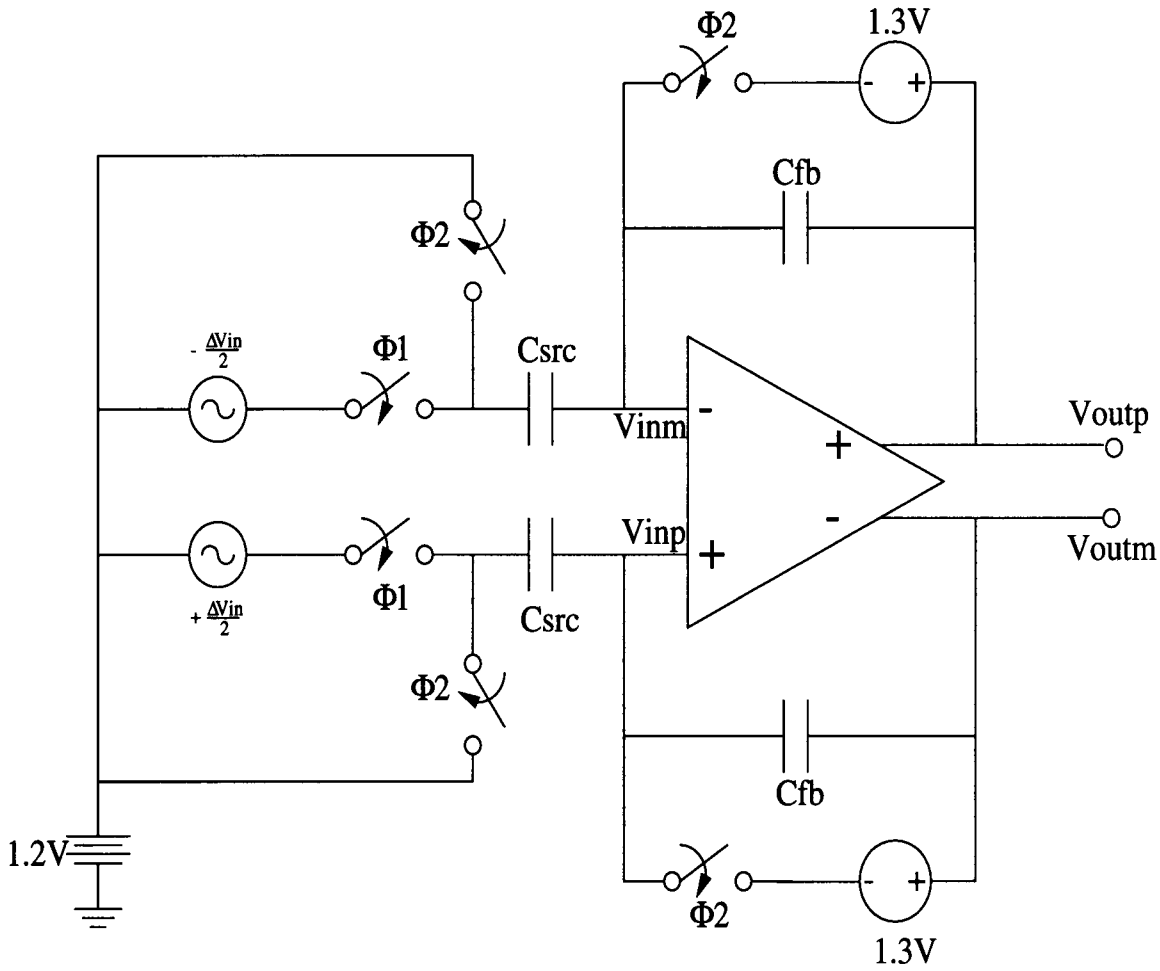


FIGURE 3.18. Switched-capacitor gain cell.

The batteries in the feedback loop can be implemented as a series of source follower stages with a certain V_{gs} drop in each stage. This battery circuit is shown in figure 3.19. It consists of three source follower stages, each of which has a V_{gs} drop of the battery voltage divided by the number of stages, or 1.3/3=.4333 volts. Multiples stages are required to avoid the gate leakage problem. The use of the feedback battery requires that the output swing of the amplifier minus the drop due to the battery not exceed the limits of the input common-mode range, which is approximately 0.8v to 1.8v. If the output does exceed these limits, the amplifier

will come out of saturation and the outputs will diverge toward V_{dd} or ground. This implies that the single-ended output cannot exceed 1 $volt_{p-p}$.

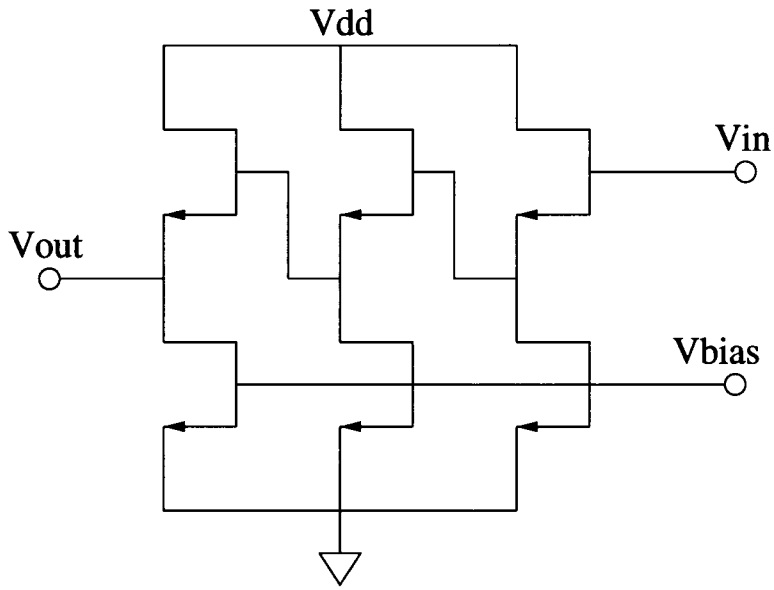


FIGURE 3.19. Feedback battery implemented as a series of source followers

The gate leakage of the HIGFET is of critical concern in the design of switched-capacitor circuits. Because switches are to be implemented using these transistors, the gate leakage must be minimized. There are two solutions to this problem. The first is to use an analog switch which senses the signal level at the input, and adjusts the voltage level at the gate of the switch such that the Schottky diode does not turn on while at the same time remaining above the threshold voltage. Work into such a switch [19], however, has shown that this circuit consumes 1mW of power using only 5 transistors. The other approach to avoiding the gate leakage problem in the switches is to limit the voltage range on the output of the op-amp to within a few volts. In switched-capacitor circuits, it is very important that the switches have very low leakage to avoid false charge being built up on the

feedback capacitors; therefore all of the switches should be p-channel because these devices have lower leakage than n-channel devices. Figure 3.20 shows the result of a transient simulation of the switched capacitor gain cell using an ideal op-amp with transistor switches and the battery of figure 3.19. The p-channel switches are turned on with a gate voltage of -2.5v. The gain of the gain cell is 100, with a source capacitance of 10pF and a feedback capacitance of 0.1pF. The input signal is a fully-differential sine wave of amplitude .01 volts peak.

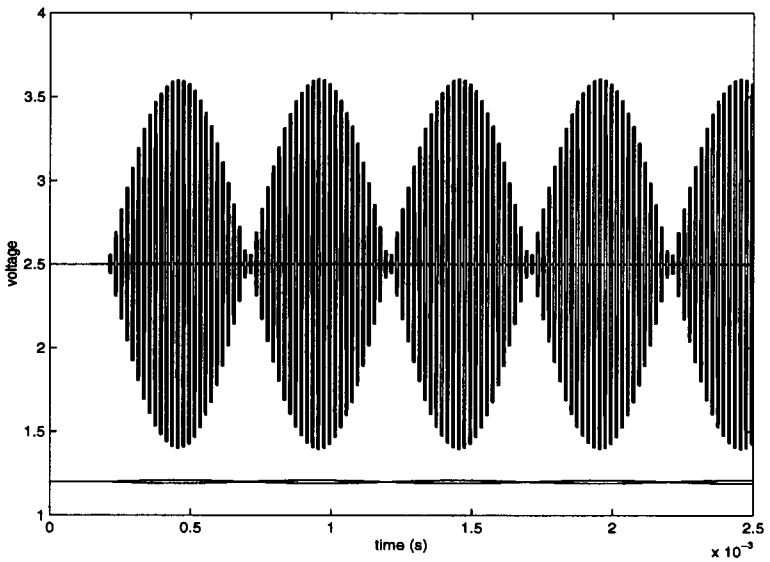


FIGURE 3.20. Transient simulation of gain cell using ideal op-amp.

Figure 3.20 shows that the switched-capacitor circuit functions as expected with an ideal op-amp. The ideal op-amp assumes that the output voltage level is not a function of the input voltage level, and therefore no common-mode feedback is required. The real op-amp does not share these characteristics. Transient simulations with the the real op-amp show the feedback method using the battery to be unstable, as the outputs eventually diverge toward V_{dd} and ground. This is most probably due to the fact that if different voltage levels are applied to the inputs, as

is the case when the feedback turns on, the amplifier does not exhibit gain, therefore the outputs are not driven to the nominal 2.5 volts, but instead diverge. With a gain of 60dB, a difference of bias levels on the input as much as 1mv would cause a 1.0 volt difference on the output. When the feedback turns on, the difference in levels between the two inputs which is much more than 1mv, cause the outputs to diverge. Figure 3.21 shows a circuit that does not require the input bias to be a function of the output, rather it is biased directly from the same common-mode that the input signals are biased at. This circuit requires an extra voltage reference, Vcmout, the output common-mode voltage, which is used to remove the charge across the feedback capacitor.

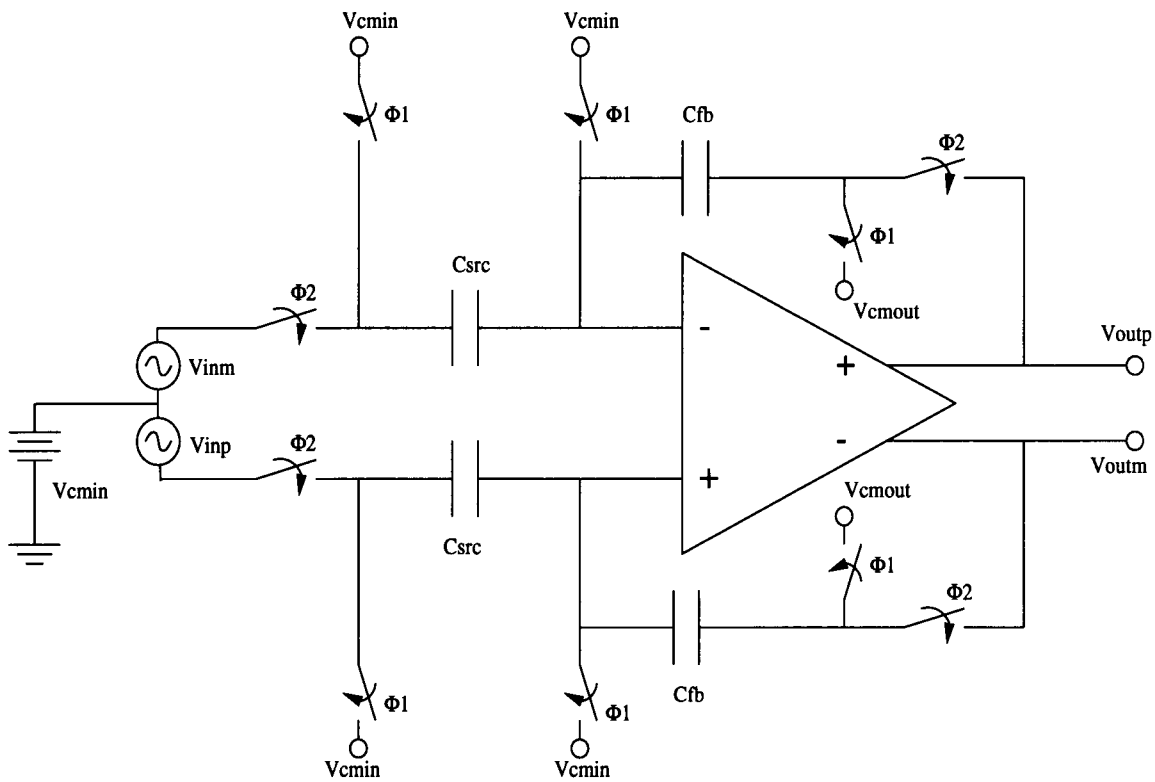


FIGURE 3.21. Alternative switched-capacitor gain cell.

This circuit, however, seams to succumb to the gate leakage problem (so could the previous circuit). A transient simulation was performed on this circuit in which a differential step of .2 volts is applied to the input with both capacitors equal to 1pF for a gain of one. Figure 3.22 shows the result. When the clock of the gain stage is ramping up, turning on a N-channel switch, the gate current into the driving transistors becomes excessive and the input voltages begin to separate. Also shown in figure 3.21 is the tail bias. This is of interest because it shows the gate-to-source voltage level for the input driving transistors. V_{gs} for the driving transistors is the difference between the input voltage level and the tail voltage, which is initially about .5 volts, well within the allowed voltage to prevent significant gate leakage. However, gate leakage does occur at about 2.5ns, even though V_{gs} is at an acceptable level. Figure 3.23 shows the results of a simulation in which $\phi 1$ never turns on. After only a few nanoseconds, excessive gate leakage occurs and the op-amp becomes unstable.

These simulations would suggest that switched-capacitor circuits suffer too much from gate leakage. These simulations were performed using a JFET model. Because the bandgap of AlGaAs in the HIGFET is greater than that of MESFETs with a GaAs gate, it is expected that gate leakage should be less in a HIGFET than in a MESFET. Other GaAs switched-capacitor circuits have been reported [20] in which gate leakage was not a factor.

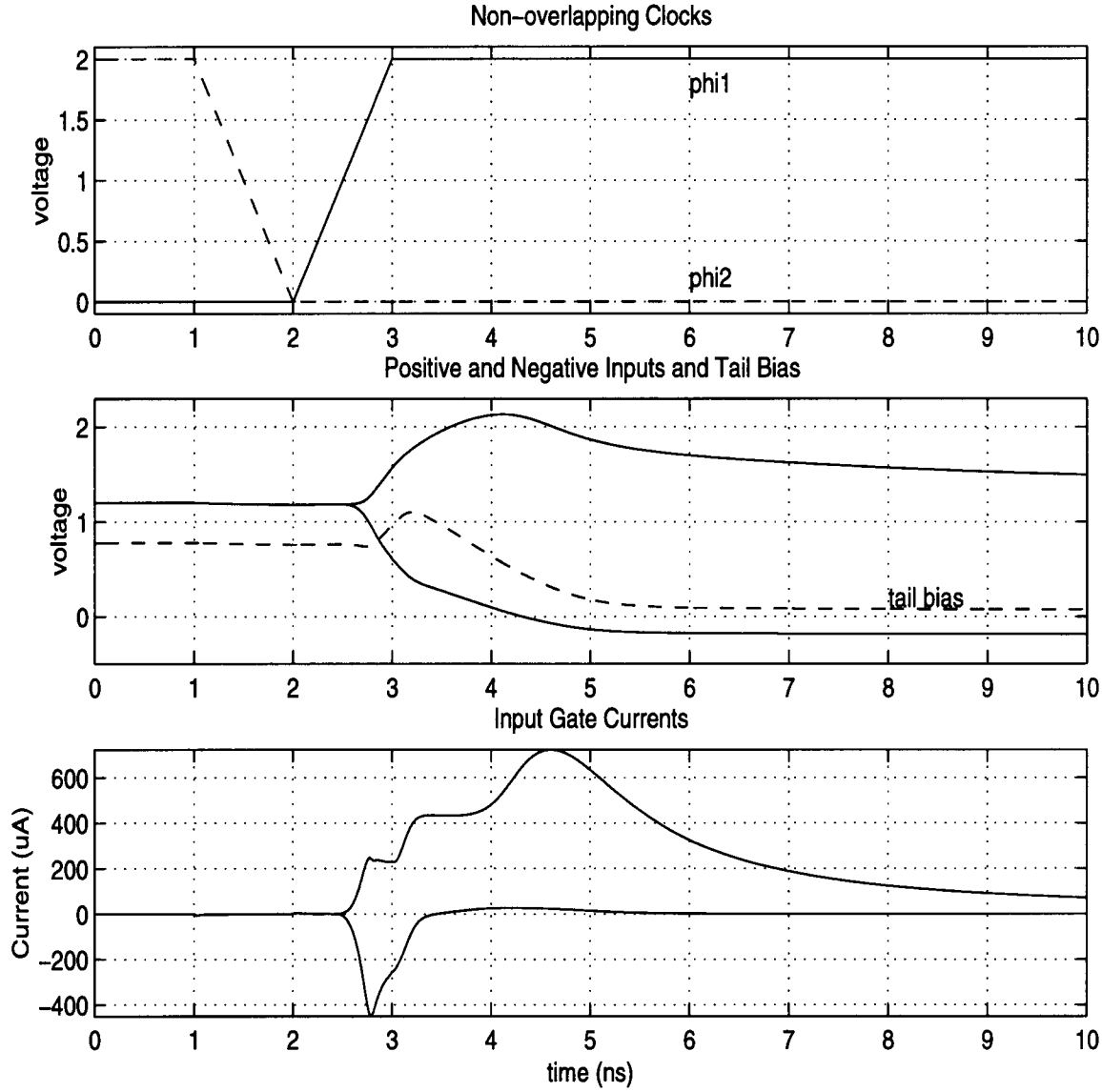


FIGURE 3.22. Transient simulation of modified gain cell (I).

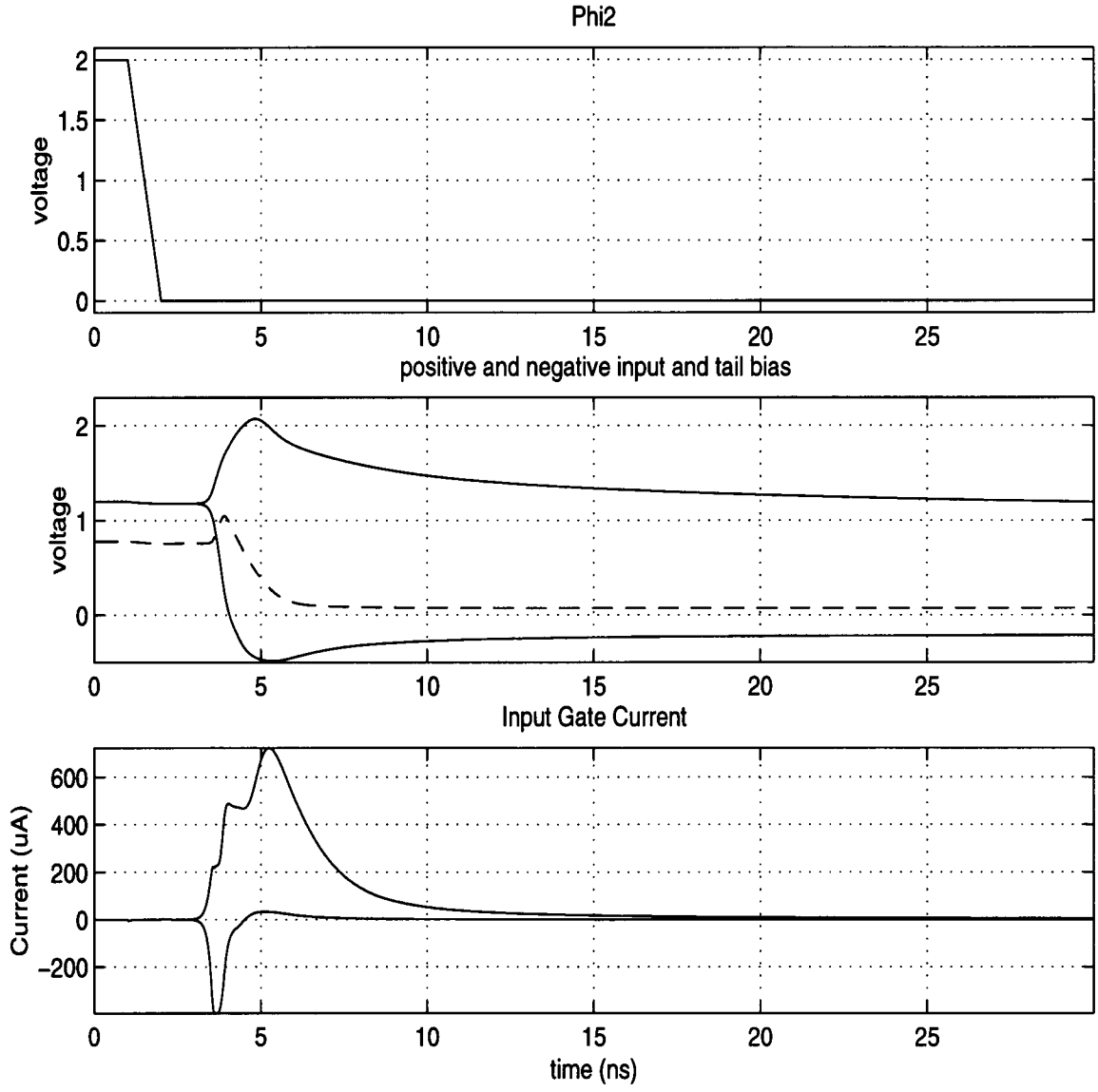


FIGURE 3.23. Transient simulation of modified gain cell (II).

4. HIGFET DEVICE CHARACTERIZATION

4.1 Equivalent Circuit Models

The design of an analog circuit using the HFET, or any transistor for that matter, requires an accurate transistor model for AC, DC, Transient, and noise simulations. Then parameters such as the channel modulation factor, λ, gain term, β, threshold voltage, V_t, and other parameters based on the model must be extracted through physical measurement. These parameters are then substituted into the model for simulation. There are a few models that exist for the HIGFET. One model that has been used by Honeywell is based on a charge control model for the two dimensional densities of electron and hole gases at the heterointerface [18]. This model has been incorporated into UM-SPICE [18], and used in the design of high speed MODFETs. Another model was created at Rensselaer Polytechnic Institute, RPI, and incorporated into their AIM-SPICE [21]. The analysis and simulation of the operational amplifier presented here was done using the device parameters supplied by Honeywell and the JFET models of Meta-Software HSPICE. The values of the supplied model parameters for the P and N HFETs can be found in the appendix. Honeywell has found that by using the JFET model as an enhancement device, digital simulations match experimented results rather well. The HSPICE models derive from work done by Curtice [22,23,24]. The Curtice model has been improved using work done by Statz et.al. [25] and Meta-Software. HSPICE uses three equivalent circuits in the analysis of JFETs: Transient, AC, and noise circuits.

The transient and AC circuits of N-channel JFETs are shown in figures 4.1 and 4.2. For DC simulations the capacitors are removed from the transient circuit. Figure 4.1 shows the diodes that can conduct if the gate voltage becomes too large.

The objective of this chapter is to determine, through simulation and measurement of transistors supplied by Honeywell, the reliability of the model and the accuracy of the simulations of chapter 3.

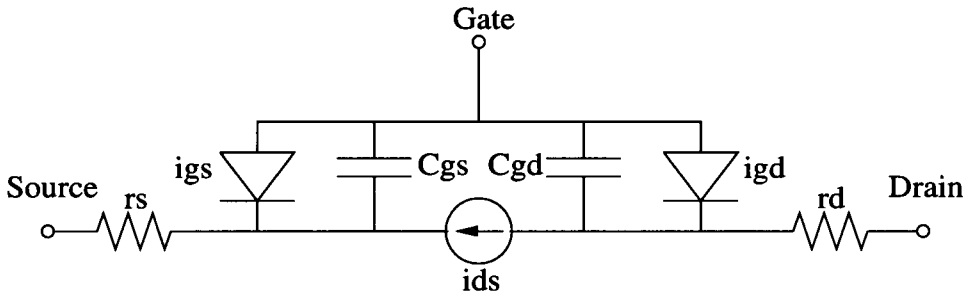


FIGURE 4.1. JFET transient analysis circuit.

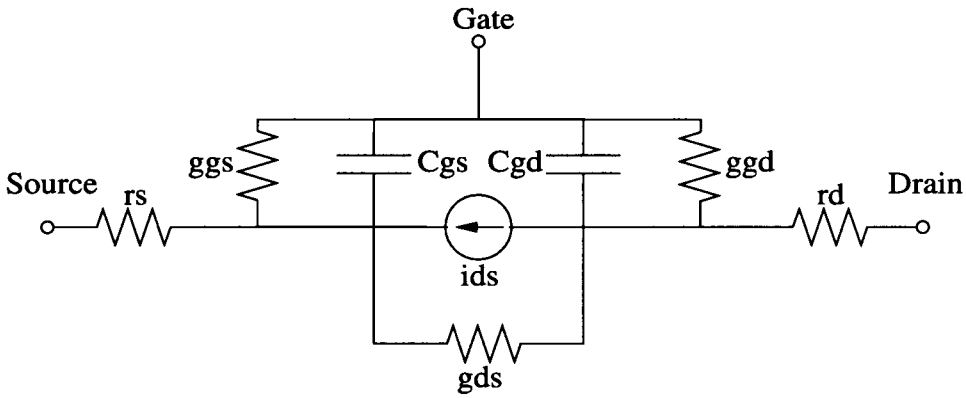


FIGURE 4.2. JFET AC analysis circuit.

4.2 Device Parameter Extraction

As stated previously, parameters based on the model are extracted from the measured data of the transistor under test. Table 4.1 lists the parameters supplied by Honeywell [26]. The values can be found in the Appendix. In order to determine whether the Honeywell parameters are correct, measurements were done on test transistors supplied by Honeywell. The measurements involved the determination of the first five DC parameters of table 4.1, since these parameters are relatively easy to obtain and are the most significant in terms of matching the model simulation to that of a real device. The measurements were done using an HP 4145 parameter analyzer connected to a probe station. The probe station allowed three probes to come into contact with the test transistors on a die. Figures 4.3 and 4.4 compare the $I_{ds} - V_{ds}$ curves of simulation using the Honeywell parameters to that of measurements taken at OSU. These measurements were done by sweeping V_{ds} from 0 to 5 volts, and incrementing V_{gs} by .2 volts beginning at .4 and ending at 1.4. Because these devices suffer from gate leakage at high gate biases, they are typically not operated at higher gate voltages than this. As these figures show, There is not a good match between simulation and measurement.

The channel length modulation, λ, can be extracted from the measured curve by finding the slope in the saturation region and dividing it by the y-intercept of the extrapolated linear line. Table 4.2 shows the results for a few of the gate voltages for the N and P HFETS. As this data shows, the channel length modulation is a function of the gate voltage. Since the model requires a constant value for this parameter, either an average can be chosen over a certain range, or it can be taken from a particular gate voltage. Honeywell chooses the modulation factor from the

Parameter	Physical Meaning	Unit	Analysis
V_t	Threshold Voltage	volts	DC
β	Transconductance	$\frac{mA}{V^2}$	DC
λ	Channel Length Modulation	v^{-1}	DC
rs	source resistance	Ω	DC
rd	drain resistance	Ω	DC
Cgs	gate to source capacitance	F	AC
Cgd	gate to drain capacitance	F	AC
Is	gate junction saturation current	Amp	DC
vbi	gate diode built in voltage	V	DC
pb	gate junction potential	V	DC
m	grading coefficient for diodes	-	-
fc	coefficient for forward-bias depletion capacitance formula	-	-
sat	saturation factor	-	-
alpha	saturation factor	v^{-1}	-

TABLE 4.1. Parameters supplied by Honeywell to be used in SPICE

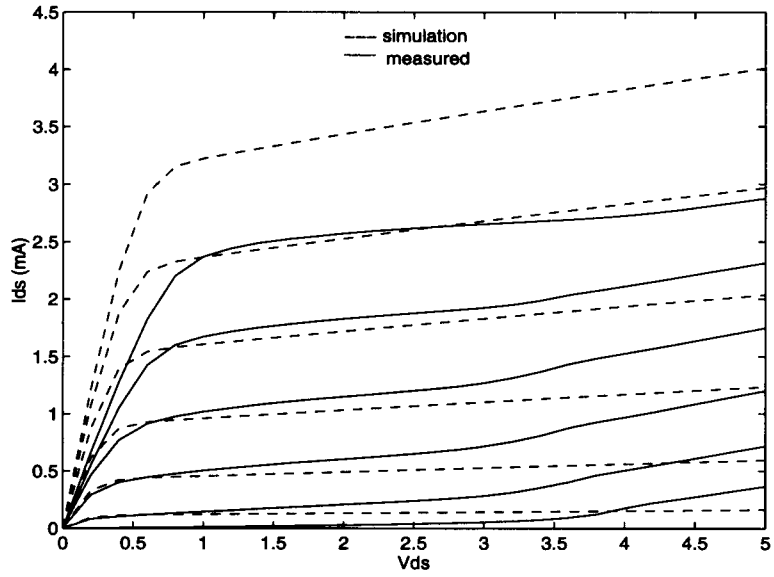


FIGURE 4.3. I_{ds}-V_{ds} curves for N-HIGFET

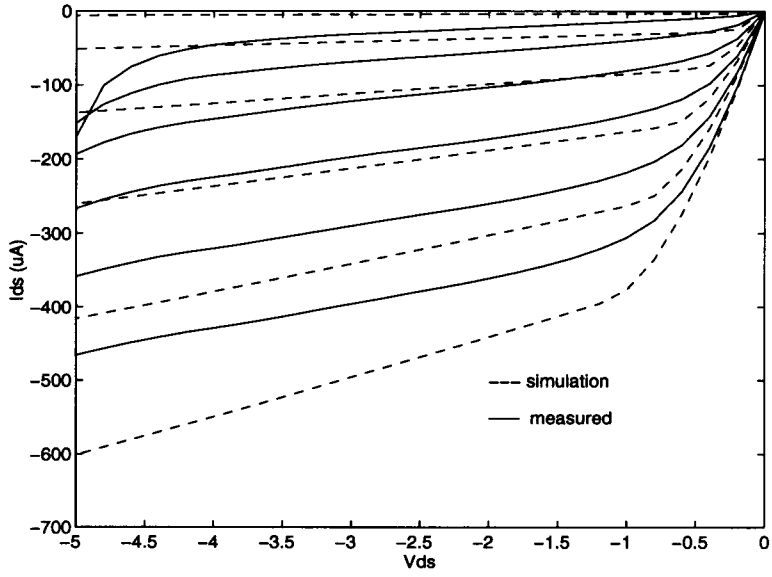


FIGURE 4.4. I_{ds}-V_{ds} curves for P-HIGFET

V_{gs}	λ_N	λ_P
.4	-	1.27
.6	.76	.55
.8	.23	.344
1	.12	.21
1.2	.06	.15
1.4	-	.12

TABLE 4.2. Variation of channel length modulation with gate voltage

data at $V_{gs} = 1v$. If λ is chosen from the data using this criterion, it is 0.1v^{-1}, a very good match to Honeywell. Similarly for the P-type, λ is 0.2v^{-1}.

The parameters β and V_t are measured off the same curve. The theoretical equation of the device in the saturation region is given as:

$$I_{ds} = \beta\frac{W}{L}(V_{gs} - V_t)^2(1 + \lambda V_{ds}) \tag{4.1}$$

Assuming the λV_{ds} term is negligible, with a slight manipulation and taking the square root, this equation represents a strait line of the form y=mx+b [27],

$$(I_{ds})^{\frac{1}{2}} = (\beta\frac{W}{L})^{\frac{1}{2}}V_{gs} - (\beta\frac{W}{L})^{\frac{1}{2}}V_t \tag{4.2}$$

where

$$y = (I_{ds})^{\frac{1}{2}}$$

$$x = V_{gs}$$

$$m = (\beta\frac{W}{L})^{\frac{1}{2}}$$

$$b = -(\beta \frac{W}{L})^{\frac{1}{2}} V_t \tag{4.3}$$

V_t is the x-intercept and β times the area of the device is the slope. Due to weak inversion at low gate voltages and mobility degradation and gate leakage at high gate voltages, the curve will not be linear. The point at which the linear region of the curve intersects the V_{gs} axis is the threshold voltage, and the maximum slope of the curve is β times the area. The parameter β that is used in SPICE is actually an effective β, β_{eff}, that is a function of the area,

$$\beta_{eff} = \beta \frac{W}{L} \tag{4.4}$$

so the above equation is effectively

$$(I_{ds})^{\frac{1}{2}} = (\beta_{eff})^{\frac{1}{2}} V_{gs} - (\beta_{eff})^{\frac{1}{2}} V_t \tag{4.5}$$

The measurements are done by sweeping V_{gs} from 0 to 1.5 volts while holding V_{ds} at 1.5 volts. Figures 4.5 and 4.6 show comparisons of $V_{gs} - \sqrt{I_{ds}}$ curves for N and P devices. From these figures, β_{eff} for the N and P HIGFETs are $2.5 * 10^{-3}$ and $2.3 * 10^{-4}$ respectively, and the threshold voltage for the N and P HIGFETs are .35v and .125v, respectively.

Many techniques to determine the drain and source resistances have been presented. Some of these are based on the physical model and the equations [28,29], while others are based only on the measured data [30]. The method presented here is based on the 'End' resistance technique [31]. This basic idea of this technique is illustrated in figure 4.7. A current is applied into the gate which creates a voltage drop across the source resistance, Rs, and the channel. Because no current is flowing in the floating drain, Rd, there is no voltage drop across it, therefore the voltage across the drain and source can be measured which relates the series channel and source resistance to the gate current.

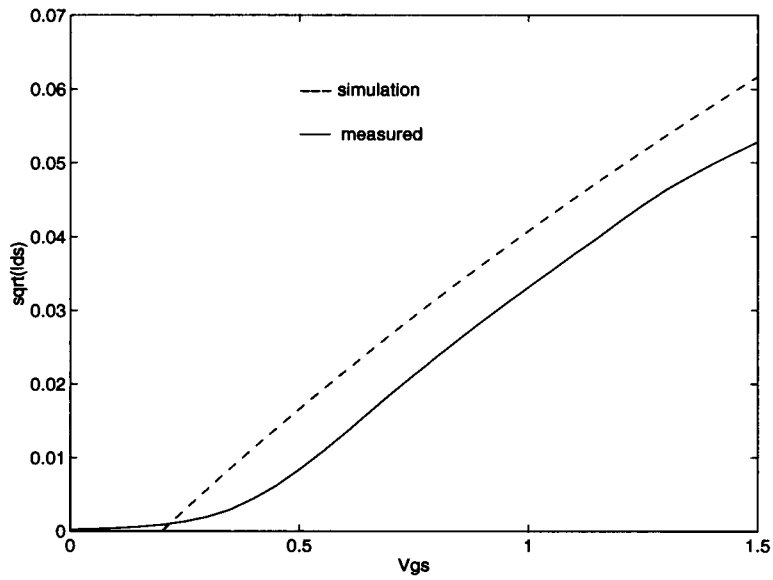


FIGURE 4.5. $V_{gs} - (I_{ds})^{\frac{1}{2}}$ for N-HIGFET.

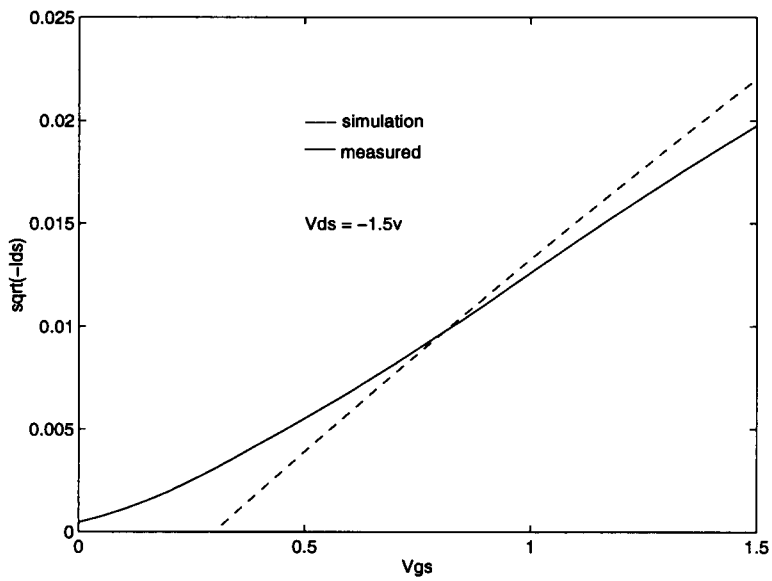


FIGURE 4.6. $V_{gs} - (I_{ds})^{\frac{1}{2}}$ for P-HIGFET.

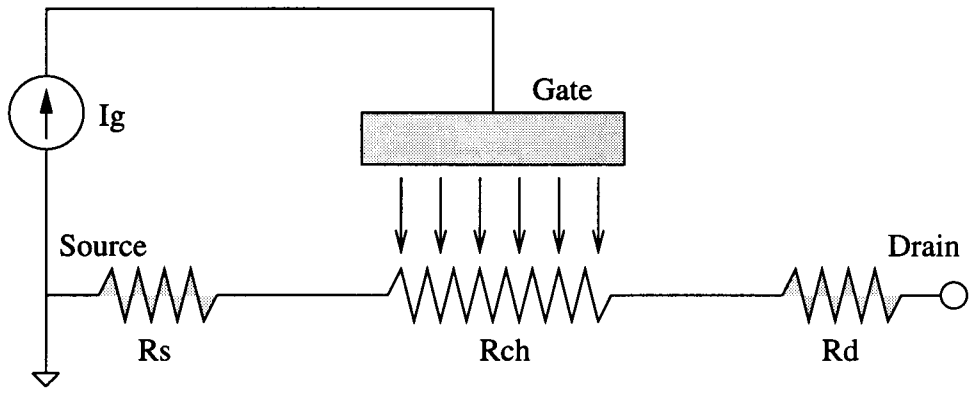


FIGURE 4.7. 'End' measurement technique to determine source resistance

$$V_{ds} = I_g(R_s + \alpha R_{ch}) \tag{4.6}$$

where α is a constant. The source and drain resistances can be found by using this technique on several different transistors of the same width, but of different length. The idea is that the graph of length versus resistance can be extrapolated down to a length of zero (y-intercept), at which point all the voltage drop is across the source resistance, R_s. Figures 4.8 and 4.9 show the length versus source resistance for N and P channel HFETs. These figures seem to show that there is not a linear relationship as the above equation describes. The data seems to be linear in different variations of length. For example, The P devices seem to be linear at large lengths (2-10μ), and linear at very small lengths (.3-.9μ), but not overall. If the submicron length data is extrapolated down to zero the source resistance is about 200 ohms. If the overall curve is extrapolated down to zero the resistance is about 150 ohms. This matches the model supplied by Honeywell. Similarly for the N devices, extrapolation down to zero gives a source resistance of 60 ohms.

The measurements to determine β, λ, and V_t were done on 10μm wide and .7μm long devices. In order to prevent scaling problems in the netlist file of a circuit, all parameters that are linearly scalable with the area, (Area=W/L), are scaled

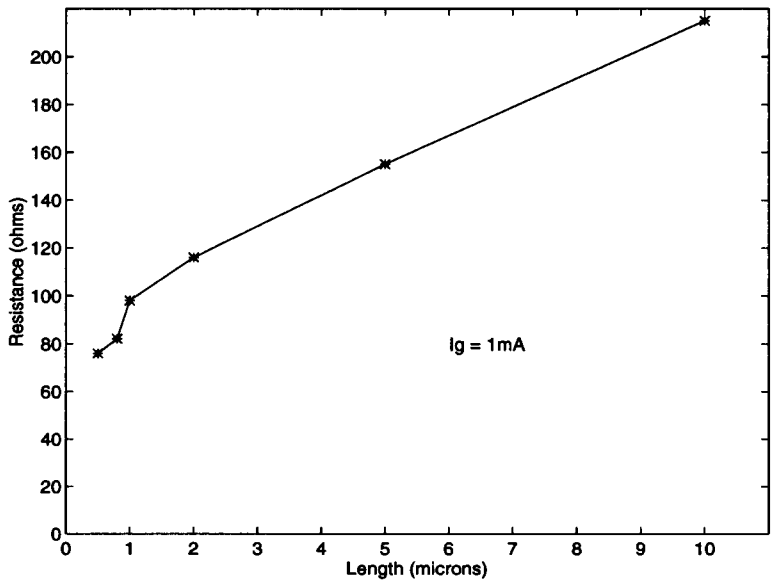


FIGURE 4.8. Length versus source resistance for N-HIGFET.

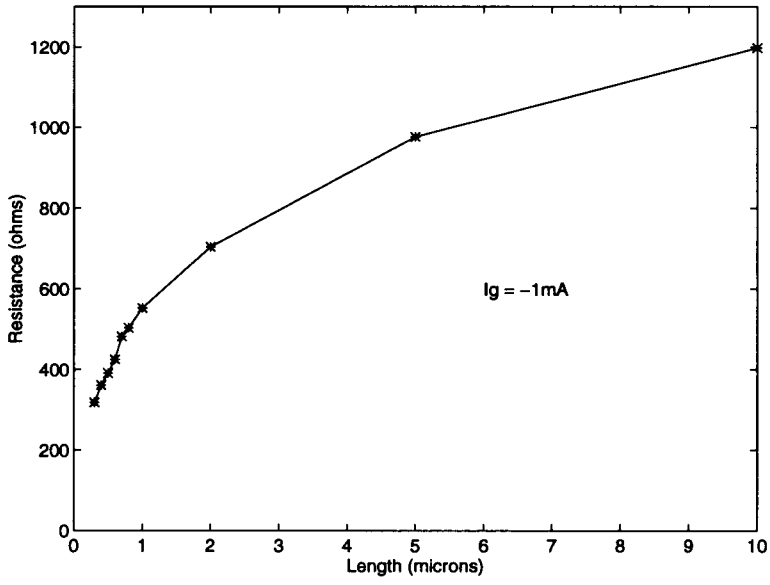


FIGURE 4.9. Length versus source resistance for P-HIGFET.

such that the effective width is 1μm. This means that β_{eff} becomes $2.9 * 10^{-4}$ and $2.3 * 10^{-5}$ for the N and P HIGFETs, respectively. The drain and source resistance and capacitances are also scaled by ten. The resistances increase by a factor of ten and the capacitances decrease by a factor of ten. This is, of course, assuming that these parameters are linear with respect to the Area. This is, in fact, how SPICE works. This linear relationship, however, begins to break down at low gate widths, therefore the model becomes incorrect. A more precise method of simulating a circuit would be to have a separate model for each device being called in the netlist. This would eliminate the scaling errors. When this method is used scaling becomes a non-factor because the models are already automatically scaled.

The parameters supplied by Honeywell are averages over all of their wafers. The testing done at OSU to extract device parameters was done only on 4 dies, each of which was on the same wafer as the op-amp. Device parameters do vary from wafer to wafer, and even from die to die on the same water, so the results shown here are not necessarily absolutely correct. Even measurements done on the same transistor can be different when performed at different times. One reason for this is that the probe to pad contact is different each time a transistor is tested. Table 4.3 compares the DC parameters measured at OSU and those supplied by Honeywell.

The main discrepancy is in the turn on voltage, which is a function of the gate thickness, the delta-doping density, and the Al mole concentration. Figure 4.10 compares OSU measured data to simulation results using the parameters extracted at OSU for the $I_{ds} - V_{gs}$ curves and for the $V_{gs} - \sqrt{I_{ds}}$ curves. As this figure shows, the measured curves for the NHFET compare favorably to the curves generated by spice using the extracted parameters. The measured data and the spice generated curves for the PHFET do not match very favorably however. This may be due to the fact that, although the threshold voltage is extrapolated as .125v, the device is in

Parameter	$\beta(\frac{A}{v^2})$	$V_t(v)$	$\lambda(v^{-1})$	$R_s, R_d(\Omega)$
Honeywell (N-type)	$3 * 10^{-4}$	.2	.1	60
OSU (N-type)	$2.9 * 10^{-4}$	.35	.1	60
Honeywell (P-type)	$3 * 10^{-5}$	.3	.2	150
OSU (P-type)	$2.3 * 10^{-5}$	.125	.2	175

TABLE 4.3. OSU and Honeywell extracted DC parameters.

fact on at a zero gate voltage. This depletion characteristic for the p-channel HFET was observed on all the dies tested at OSU. Another reason for the discrepancy is that the model is a level 1 HSPICE model, which uses a simple spice JFET model, as opposed to the level 3 Curtice model, which is used for the N devices.

The measured DC curves and the DC curves generated by spice using Honeywell parameters are slightly different, with the main differences being the threshold voltages and the non-constant Early voltage as a function of V_{gs}. These differences cause a significant change in the simulation results. Due to the large difference in turn on voltages, the DC characteristics are altered as shown in figure 4.11. Plot (A) shows the input common-mode range and the large signal output swing. The new parameters cause the input common-mode to shift up by .5 volts, although no change in overall input range is discernible. This results in a shift of the input biasing level from 1.2 to 1.7 volts. Plot (B) shows that the new parameters cause the single-ended DC gain to drop to 388 and the output linear range to decrease, and thus the open-loop THD is increased by a factor of 10 for an input ac signal level of .25mv to 2% as opposed to .2%. However, biasing the input at 1.2 volts

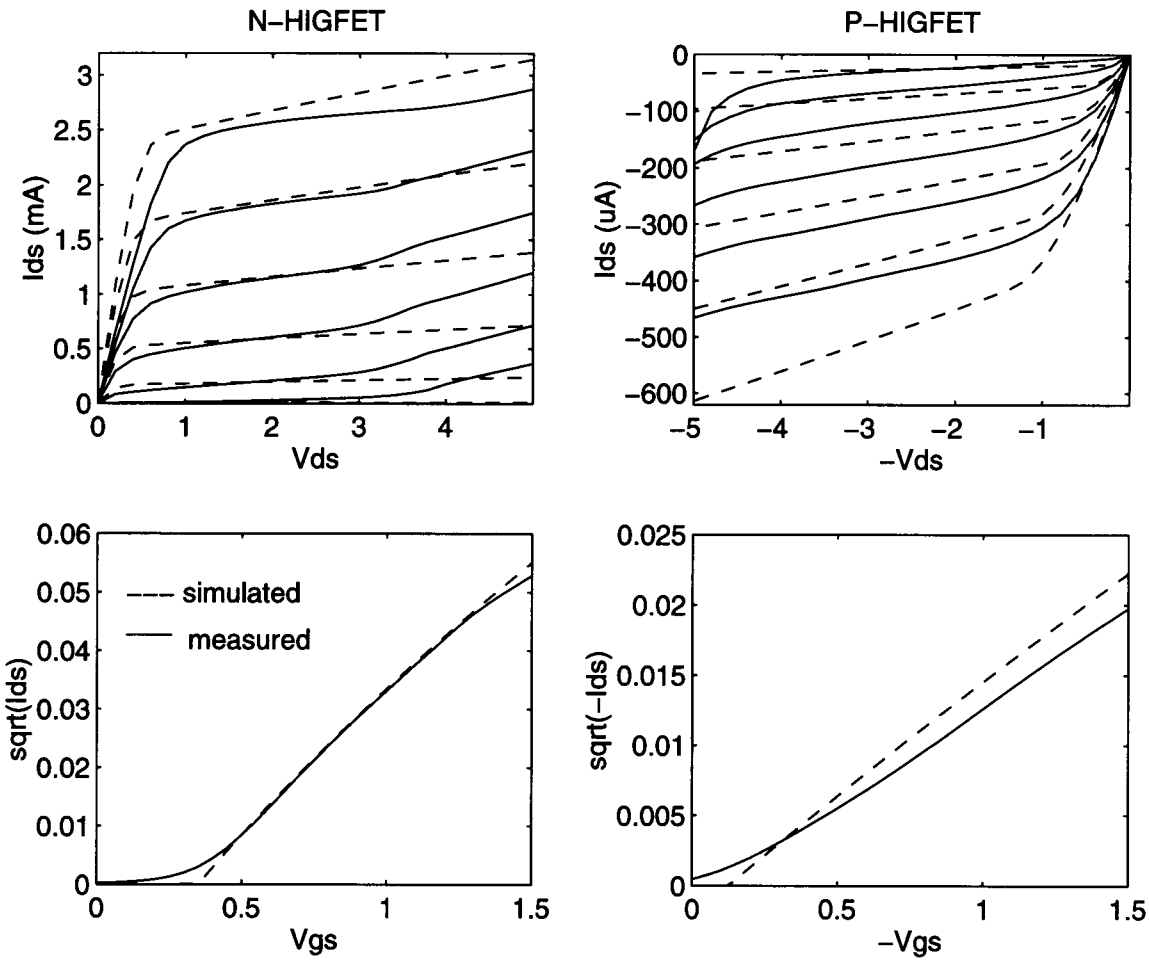


FIGURE 4.10. DC measured and simulated curves using extracted parameters.

as before yields a gain of 444 and a larger linear output swing as shown in plot (E). At a biasing level of 1.2 volts, however, the input range is near its lower limit and the output is not biased at 2.5 volts. Plot (C) shows the frequency response using the extracted parameters. The unity gain frequency is not altered, due to the fact that ac parameters were not changed. The upper curve is the fully-differential output taken as the difference of two single-ended outputs, and the lower curve is a single-ended output. Plot (D) shows the output swing obtained using the original Honeywell parameters for comparison.

Figure 4.10 shows that, for V_{gs} less than 1.2 volts, the model works moderately well for N-channel devices. There are two sources of error, the first being the fact that the model yields a nearly constant Early voltage, over all ranges of V_{gs}, while measurements of the HFET show that the Early voltage changes as the gate bias increases. The other source of error as seen in figure 4.10 for the n-channel device is that at high drain to source voltages, the output conductance increases. Because few HFETs were tested, it is not known if this is a phenomenon of the measurement method or if this is typical for n-channel HFETs. Publications by Honeywell, however, do not show this phenomenon [32]. Figure 4.10 shows that for p-channel devices, the model is poor. This can mainly be attributed to attempting to model an enhancement device that is actually on at zero gate voltage. The data obtained from parameter extraction seem to suggest that for more accurate simulations, a better model is required. For simulations to match measured data, a better control over the threshold voltage during fabrication is required.

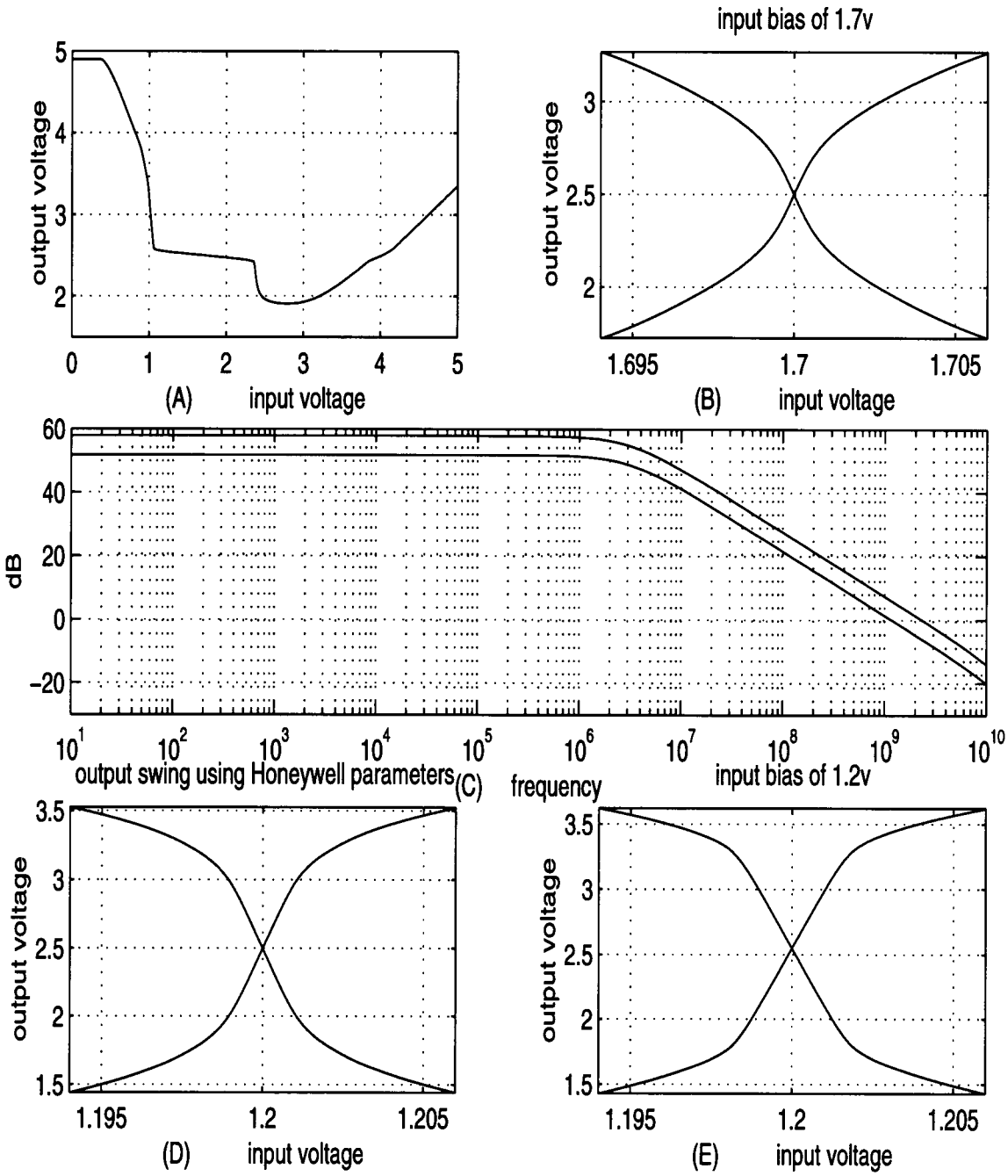


FIGURE 4.11. Op-amp simulation results using extracted parameters.

5. OP-AMP TESTING

The op-amp that has been presented here was fabricated at Honeywell. The layout is shown in figure 5.1. Due to minor errors in the layout, only preliminary results have been obtained. The errors in the layout have since been corrected, but at the time of this writing the corrected layout has not finished the fabrication process. The test results presented here is that of the large signal output swing, from which can be determined the DC gain and the output range. The test for the large signal output swing, and for all of the other DC tests, are done virtually the same way as in the simulations of chapter 3. Due to errors in the layout however, modifications to some of the internal DC biases were required. The tests were done using a parameter analyzer, a probe station, and a 14 pin probe card custom designed to fit the pad layout. Figure 5.2 shows the single-ended result of a large signal output test with an input bias of 1.3 volts. The gain, determined by the parameter analyzer at an output swing of about 2 volts_{p-p} is 116, or about 41dB, significantly lower that that predicted by simulation. However the gain at 1 volt_{p-p} would be higher. The main reasons for the discrepancy are due to an inaccurate model and the mismatch between the simulation parameters and the actual device parameters as was discussed in chapter 4. Gain and output swing varied from die to die with single-ended gain ranging from 77 to 230.

Because the op-amp operates into the RF range, its frequency response must be tested under RF conditions using a network analyzer. A testing package was built that allows ac signals to come in via SMA connectors. The PC board is ϵ=10.8 25 mil duroid. In order to obtain a 50Ω line into the package the standard microstrip equations were used to obtain the required trace width. The die is glued to the

case of the gold plated package and is wire bonded to the leads. This package will be used to fully test both the DC and AC characteristics of the op-amp. When designing test packages for RF circuits, it is important to consider the parasitics of the package, as it affects the frequency response and can potentially cause instability and oscillations. The RF package has been characterized up to 6 GHz [33]. Figure 5.3 shows the results of the characterization. Essentially the package can be modeled as an inductive lead, a capacitive interconnect, and an inductance due to wire bonding. The inductance due to wire bonding can be approximated as 1nH per millimeter. Due to the size of the die compared to the package case, the length of the wire bonds is about 5mm, which gives an inductance of 5nH. When the package parasitics are incorporated into the simulation of the op-amp, the frequency response changes near the unity gain frequency, as shown in figure 5.4. Although the phase margin is 82 degrees at unity gain, the gain margin is negative at a phase transition of 180 degrees, meaning that the op-amp exhibits gain after a phase transition of 180 degrees. This is potentially unstable.

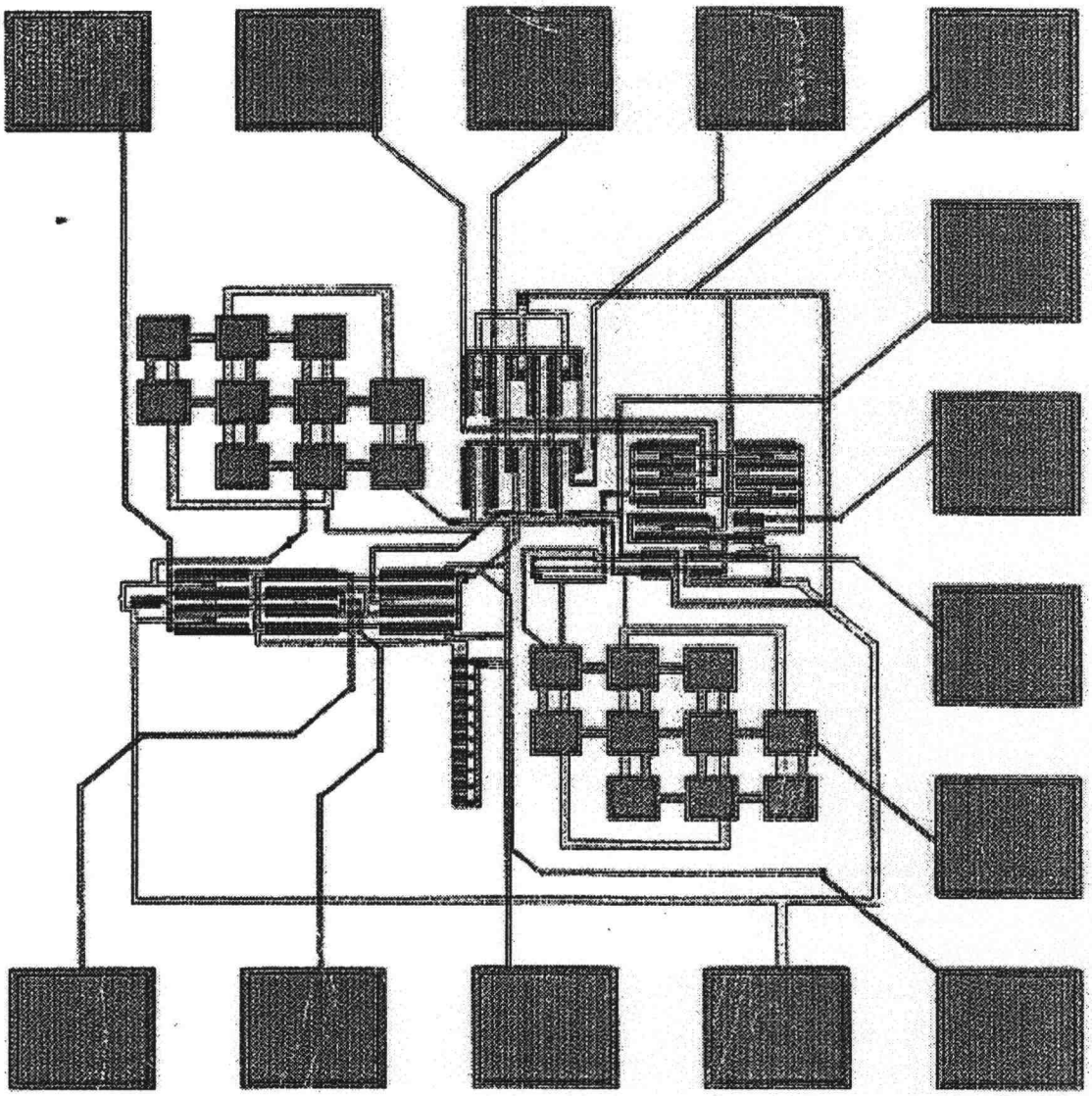
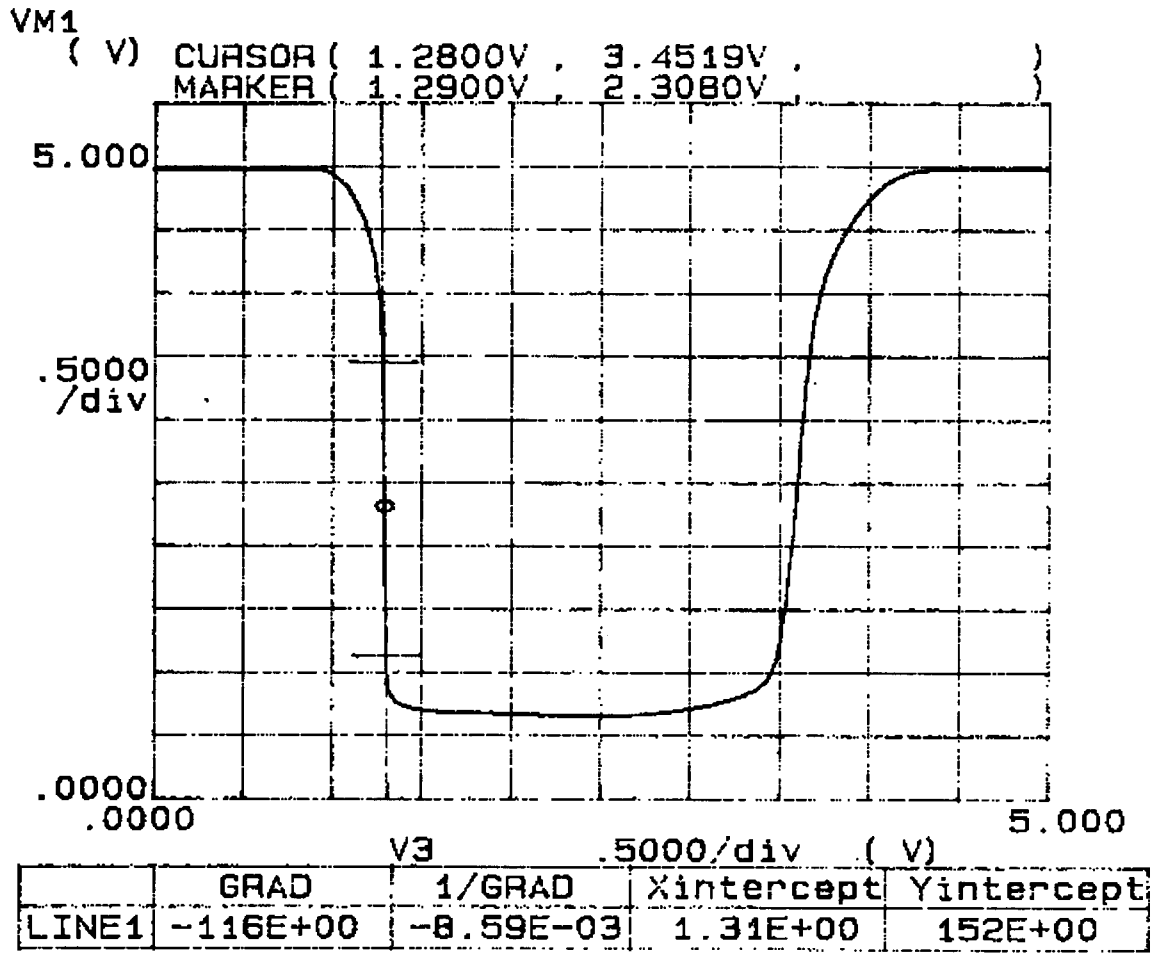


FIGURE 5.1. Op-amp layout.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-116E+00	-8.59E-03	1.31E+00	152E+00

FIGURE 5.2. Measured op-amp large signal output swing and DC gain.

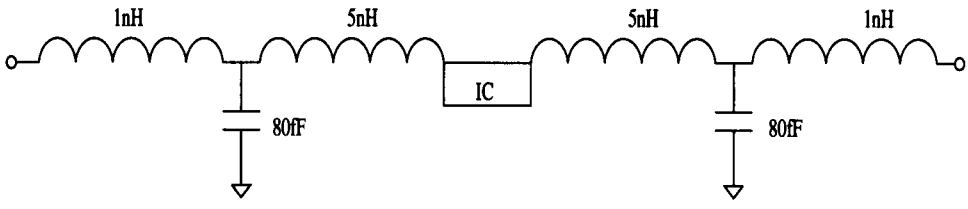


FIGURE 5.3. Package parasitics.

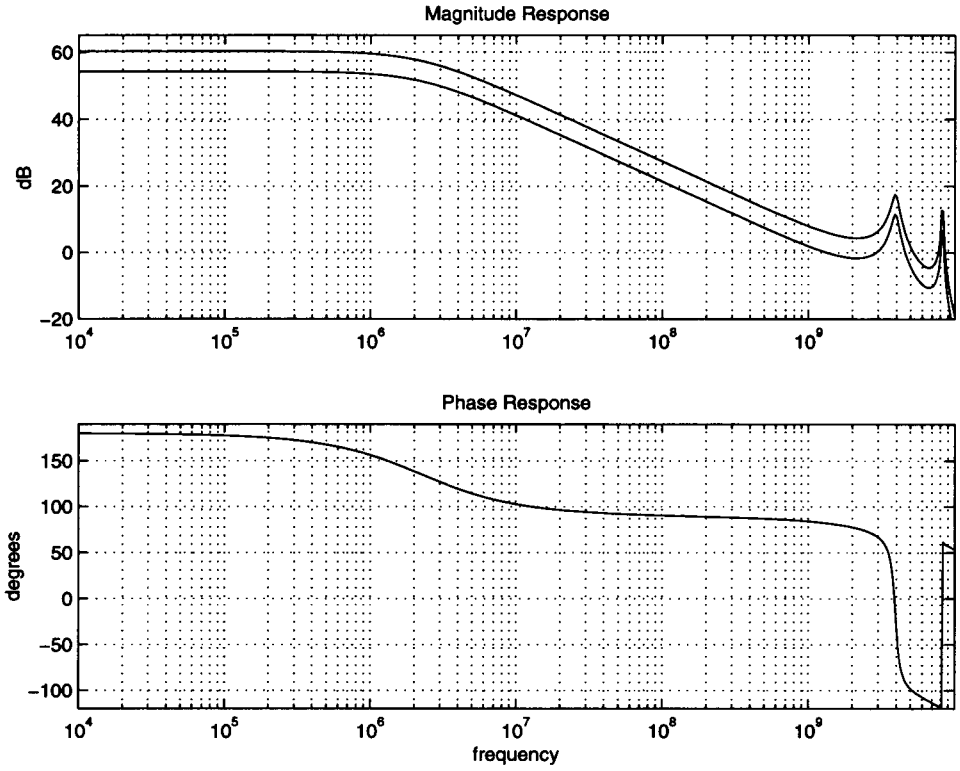


FIGURE 5.4. Frequency response including package parasitics.

6. CONCLUSIONS

The goal of this research was to demonstrate the suitability of the GaAs HIGFET technology for the realization of high speed analog circuits. A formal design and analysis of an operational amplifier and a switched-capacitor gain cell was presented. The operational amplifier was fabricated at Honeywell using their C-HIGFET process. Device parameter extraction was performed at OSU to obtain more accurate simulations. The operational amplifier presented here demonstrates the advantages of HFET analog circuits, high speed and high bandwidth, with other characteristics comparable to that of CMOS, such as gain, input offset voltage, and CMRR. The operational amplifier simulations suggest a fully-differential gain of 60dB with a unity gain bandwidth of 2.44 GHz. With modification to device sizes, these values can be even higher. The major design concern in GaAs HFET design is gate leakage. The gate leakage problem can be overcome in continuous time circuits by restricting the output swing to within a few volts. Simulations showed, however, that gate leakage in these devices is too significant for switched-capacitor implementations. The high speed characteristic of the HFET is ideally suited for switched- capacitor circuits, and should still be investigated. A more reliable model should be used and a simple single ended output op-amp should be considered for simplicity. The model used for these simulations was HSPICE's JFET, using the advanced Curtice model. One of the desired results to be obtained from this work is whether this model is accurate enough to simulate analog circuits to a good degree of accuracy. The parameter extraction results and the actual op-amp testing seems suggest that, although the model works, it does not allow for a high degree of accuracy such as exists in MOSFET models. The equations used for a first order

design of the amplifier are analogous to the MOSFET. Although these equations gave results that worked, it can be shown that the current-voltage relationship of the device is governed by a 3/2 law, and not a square law like the MOSFET [17]. It can also be shown that for p-channel devices, the saturation current is a function of $\frac{\beta}{2}$, as opposed to β [34]. It can also be shown through simulation that adjusting the lengths of the devices affects the simulations differently in a HFET circuit compared to a CMOS circuit, implying the analogous first order equation is not correct. More accurate first order models will help give the designer a better idea of how the device works, and a better first order approximation to the design. It is also important for the fabrication process to have better control over the threshold voltages, else large differences will exits between simulation and testing as was shown chapter 4. In HFETs, it is typical that saturation is due to velocity saturation and not pinch off, therefore simple first order analysis may be slightly incorrect.

The corrected layout will go into the next available CHFET fabrication run at Honeywell. With the corrected layout, more data can be obtained to determine how well simulation matches measured results.

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Appendix

The JFET model supplied by Honeywell for N and P channel HIGFETs:

.model n1 njf(vto=0.2 level=3 alpha=6 lambda=.1 beta=3.0e-4 + pb=0.6 rd=600 rs=600 is=0.5e-11 m=0.5 vbi=0.6 + cgd=7.0e-16 cgs=7.0e-16 fc=0.6 n=5 capop=0 acm=0 sat=0)

.model p1 pjf(vto=0.3 level=1 lambda=.2 beta=3.0e-5 m=0.5 + is=0.1e-11 rd=1500 rs=1500 n=5 cgd=5.0e-16 cgs=5.0e-16 + fc=0.6 n=5 pb=0.6 capop=0 acm=0 sat=0)