AN ABSTRACT OF THE THESIS OF

WILLIAM Y. JIANG for the degree of Master of Science in Electrical and Computer Engineering presented on April 28, 1989.

Title: A CMOS Differential Line Driver.

Abstract approved: Redacted for Privacy

David J. Allstot

A short-circuit-protected line-driver circuit is particularly adapted for use in a CMOS differential line-driver system, where one line-driver circuit provides a true output signal, and another line-driver circuit provides a complementary false output signal. A short-circuit is sensed by measuring current through a secondary pull-up transistor, and disabling a primary pull-up transistor, if a short-circuit fault occurs, which exceeds a predetermined current level for a predetermined time.

A CMOS Differential Line Driver

by

William Jiang

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed April 29, 1989

Commencement June 1989

APPROVED:

Redacted for Privacy

Professor of Electrical & Computer Engineering
in charge of major

Redacted for Privacy

Head of Department of Electrical & Computer Engineering

Redacted for Privacy

Dean of Graduate School

Date thesis is presented April 28, 1989.

TABLE OF CONTENTS

LIST OF FIGURES

A CMOS Differential Line-Driver

I. INTRODUCTION

Differential line driver circuits are frequently used to drive transmission lines. Differential line-driver circuits provide two differential output signals, that is, signals which are equal in magnitude but of opposite phase. These signals are complementary; one is called a true signal, and its complement is called a false signal. Differential line-driver circuits typically use two separate line-driver circuits, one fed with a true input signal, and the other fed with a false input signal [4]. These circuits are required to have nearly identical propagation delays. Differences in propagation delays, between the two signals, is measured by a skew characteristic, which measures the time difference for a signal transition at the output of a differential line-driver. The time difference is measured between the 50 percent amplitude points of each of the signals.

Line-driver circuits typically include a pull-up transistor, which determines high output signal levels, and a pull-down transistor, which determines low output signal levels. The current delivered by a pull-up transistor depends on the load impedance. For a very low impedance

or for a short-circuit fault condition, a pull-up transistor begins to supply current, as the output voltage goes from a low state toward a high state. If excessive current is drawn through a pull-up transistor, it may be damaged. Note that a pull-down transistor serves as a current sink for the output load and does not need short-circuit protection. The more detailed design consideration will be discussed in section II.

In this design, a current-sensing short-circuit protection is provided which does not degrade the skew characteristic of the complementary output signals, the pull-up time, and the rise time performance of the line-driver. In addition, a delay circuit and a comparator circuit are designed to distinguish between a low to high transient current and a true short-circuit fault current. These features will be discussed in detail in section III, and the circuit operation will be described in section IV. The circuit simulation results are given in section V, and some of the design techniques are discussed in section VI.

II. BACKGROUND OF THE DESIGN

Line driver circuits are used to drive transmission lines. If the output terminal of such a device is shorted to ground or is coupled through an excessively low impedance to ground, excessive current is drawn from the output terminal of the line driver. In order to prevent the output line-driver from being damaged, it is necessary to detect a short-circuit fault condition and take action to prevent the line driver from being damaged. Various schemes are available in the prior articles for such short circuit detection and protection. These schemes may be classified into one of two categories. The first category is for short-circuit protection schemes, which sense an excessive amount of output current, such as occurs when a short-circuit fault is present [1]. The other technique involves various voltage-sensing techniques to detect a short-circuit condition [2]. A problem may exist with short-circuit protection system. It is called the false-trip problem, which may occur during start-up, that is, when power is first applied to a circuit or during rise time, when the output voltage is required to switch from a low level to a high level [3].

For line-driver circuits, conventional current-sensing short-circuit protection schemes typically have a

current-sensing resistor in series with the pull-up transistor, because a short-circuit condition causes excessive current to be drawn through the pull-up transistor, while the pull-down transistor does not require a current-sensing resistor [5]. Insertion of a resistance in series will increase the pull-up-rise time, while the pull-down-fall time is unaffected. A differential line-driver system uses two line-driver circuits, one providing a true output signal and the other providing a complementary false output signal. For a given signal transition, such as, for example, a low to high transition, the pull-up transistor of the one circuit is active, and the pull-down circuit of the other circuit is active. The pull-up circuit has a slower time constant than the other. Consequently, the skew characteristic will be degraded because the one circuit, with a series current-sensing resistor, reaches its 50 percent amplitude value more slowly than the other circuit, without a series resistor [6].

Therefore, it should be appreciated that conventional current-sensing schemes for short-circuit protection adversely affect the operating characteristics of line-driver circuits. In particular, differential line-driver systems, using line-driver circuits operating in complementary modes, are adversely affected by use of series current-sensing resistors.

Therefore, the circuit design is required to provide an improved current-sensing, short-circuit protection technique for a line-driver circuit, which does not degrade the pull-up time, the skew characteristic of the complementary output signal, and the rise time performance of the line driver.

In addition, the circuit design needs to provide a short-circuit protection scheme, which must distinguish between a low to high transient current and a true short-circuit fault current.

III. CIRCUIT DESCRIPTION

Figure 1 shows a schematic diagram of a line-driver circuit 10 according to the design. An enable signal En is provided at the enable input signal terminal 12. This signal, when in the high state, enables the circuit to provide an output signal Ya, and, when the enable signal En is at a low state, the output terminal for signal Ya is at a high-impedance state, or tri-state mode. A true input signal T is provided at an input terminal 14 of the circuit, and a complementary input false signal F is provided at an input terminal 16 of the circuit. Both of these signals are complementary, that is, they are equal in magnitude but opposite in phase. The true input signal T is coupled to one input of a NAND1 gate 18. As long as the signal on the other input to the NAND1 gate 18 is at a high state, then the true signal T is gated to pass through, with inversion, to the NAND1 gate 18 to an inverter 20. The gated output signal of the inverter 20 is connected to a terminal T4. The true signal T also is transmitted through two more inverters 22 and 24, and is provided as an ungated signal at a terminal T3 as shown. The gated true signal T and the true signal T are to arrive at respective terminals, T4 and T3, at substantially the same time, because the propagation

delays through NAND1 gate 18 and inverter 20, are set equal to the propagation delays through inverters 22 and 24.

Similarly, the false input signal F at input terminal 16 is passed through a pair of inverters, 26 and 28, to a terminal T5. An output signal from inverter 26 is coupled to an input of inverter 30, which has its output connected to a terminal T6. Because the inverters 26, 28 and 26, 30 have the same propagation delays, the false signal F is simultaneously present at terminals T5 and T6. Note that the gated and ungated true signal T and the false signal F are complements of each other, so that, when the true signal T is at the high state, the false signal F is at a low state, and, when the true signal T is at a low state, the false signal F is at a high state.

The purpose for having true signals T connected to terminals T3 and T4 is to have the gated and ungated true signals drive the respective gates of NMOS pull-up transistors Q3 and Q4 to control their conduction. Both of these transistors have their drains connected to a Vdd supply voltage, typically a +5 volt source. Similarly, the false signal F is coupled to the gate terminals of a pair of NMOS pull-down transistors, Q5 and Q6, which have their drains connected to the output terminal 32 of the

circuit and their sources to a ground potential. The source of the primary pull-up transistor Q4 is directly connected to the output terminal 32. The source of the secondary pull-up transistor Q3 is connected to a source-terminal node 34. A current sensing resistor R1 is connected in a series between the node 34 and the output terminal 32. The current sensing resistor R1 is an N-type diffusion resistor with a relatively large resistance value, in comparison to the value of a typical current-sensing resistor, where the typical prior article resistor must be kept low in value to avoid a large voltage drop across the sensing resistor. The current flowing through the primary pull-up Q4 is designed to be six times greater than the current flowing through the secondary pull-up transistor Q3, so that the voltage drop across the sensing resistor R1 does not significantly affect the output signal, because the rise time of the secondary pull-up transistor is slowed by a series resistance. Current at the output terminal 32 flows primarily through the pull-up transistor Q4, when the output signal Ya is initially at a low level and begins to rise, or pull-up, to a high level. In that case, transistor Q3 is turned on and provides current, through the current-sensing resistor R1 to the output terminal 32. Transistors Q5 and Q6 are pull-down transistors, respectively for Q3 and Q4. The true signal T and its complement false signal F are present at the

same time to control the operation of transistors Q3, Q4, Q5, and Q6. Note, however, that the operation of Q4 is also controlled by the operation of the NAND1 gate 18. Operation of this gate determines whether transistor Q4 is activated by the true signal T to provide the primary output current to the output terminal 32 of the circuit. Transistors Q4 and Q3 are designed so that the current passing through transistor Q4 is approximately six times greater than the current passing through transistor Q3. Inhibiting gating, the true signal to Q4, permits the pull-up transistor Q4 to be cut-off while still permitting transistor Q3 to provide a short-circuit current of approximately 50 milliamperes, when the output terminal 32 is short circuited to the ground potential.

When the enable signal En, present at terminal 12 is high, a pass transistor Q7 is turned on and couples the voltage at terminal 34, on the source of the secondary pull-up transistor Q3, to a terminal 40. A shunt transistor Q8 has its drain connected to the terminal 40 and its source connected to the ground potential. The enable signal En at the input terminal 12 of the circuit is also coupled to the input terminal of an inverter 42, and its output is connected to the gate of the shunt transistor Q8. Transistor Q8 is turned on when the enable signal is inactive, or low, so that Q8 pulls the terminal

40 to near the ground potential. Terminal 40 is connected to the gate of a pass-gate transistor Q9, which has its source connected to the output terminal 32 of this circuit. The pass-gate transistor Q9 responds to the voltage developed across the current sensing resistor R1. When this voltage exceeds a predetermined value, the pass-gate transistor Q9 is turned on. The drain of the pass-gate transistor Q9 is connected to a terminal B, which is, in turn, connected to the positive voltage supply through a load device, for example, a diode-connected transistor Q2. When transistor Q9 turns on, the voltage at terminal B drops to a low level.

Terminal B has two delay circuits connected to it. The first delay circuit, CELL 1, designated by reference number 50, and the second delay circuit, CELL 2, designated by reference number 52. CELL 1 includes a pair of inverters 54 and 56 connected in a series. Similarly, the second delay unit CELL 2 has four inverters 58, 60, 62, and 64 connected in a series with terminals B.

All of the inverters are formed as complementary MOS, that is CMOS, inverter circuits. In Figure 2 the dotted line 70 shows the voltage transfer characteristic for a CMOS inverter in the case where the transition voltage is designed by proper selection of circuit parameters to be

approximately midway between the 5 volt supply voltage and the ground. In the case of inverter 54, the transistors of the device are designed to provide a transition, at approximately 1.25 volts. This is accomplished by adjusting the channel with the N device to be four times greater than the channel with the P device. This transfer characteristic permits the inverter 54 to turn on a low voltage input level and to react quickly to a rising voltage level. Figure 2 also shows the voltage transfer characteristic for the CMOS inverters used for the second inverter 56 and for each of the inverter stages of the second delay circuit 52. This transfer curve, 72, has a transition which occurs at an input voltage level of approximately 2.5 volts.

Note that the propagation delay of CELL 2 is designed to be much greater than the propagation delay of CELL 1. If the output voltages of the first delay unit 50 and a second delay unit 52 are both simultaneously low, the output level of a NOR1 gate 80 goes to a high level. This causes a switch transistor Q10 to be turned on which causes a connection to be made between the circuit output terminal 32 and terminal A. Transistor Q1 is a diode-connected transistor connected between terminal A and the power supply voltage, which holds terminal A normally high. A low voltage at terminal A, which is coupled to an

input terminal of a NAND1 gate 18, disables the NAND1 gate and inhibits the true signal T from passing through. A low level is placed on the gate of the primary pull-up transistor Q4, which turns off.

IV. CIRCUIT OPERATION

1. Operation of the Circuit in Its Normal Mode

Figure 3 shows waveforms for signals at various terminals, when the circuit 10 is operating in the normal mode of operation, that is, when the output terminal 32 is not short-circuited.

The waveform labeled I represents the voltage input waveform for an input signal I (described herein below in connection with Figure 6), from which are derived, with equal propagation delays, the true input signal T and the false input signal F. The low-to-high transition is significant because, if the output terminal 32 happened to be short-circuited, this signal would ordinarily cause the circuit to set the output voltage level for signal Ya to a high level, and, thereby, force current into a short circuit. The case where the input signal I goes from a high to a low state is not of concern, because, in the low state, no current is drawn from the circuit, and the circuit cannot be damaged. Therefore, attention will focus on the low-to-high transition for the input signal I. When this transition occurs, as indicated by reference numeral 90, and, after some propagation delay at time 92, the output currents IYa begin to increase. Since some of

the current is provided by the secondary pull-up transistor Q3, the voltage Vr across the current-sensing resistor R1 also begins to rise at time 92. As the voltage Vr begins to rise, the voltage at terminal B falls slightly. However, the voltage at terminal B never falls below the threshold or transition voltage of the inverter 54. The output voltage at terminal L, therefore, does not drop. The inverters of the second delay unit 52 are much slower, but they do not change state because the signal at terminal B does not fall low sufficiently. A short time later the output current IYa begins to fall off so that the voltage Vr across the current sensing resistor R1 also begins to decline.

2. Operation of the Circuit with its Output Short-Circuited

Figure 4 shows the waveforms of signals at various terminals, when the terminal 32 has a short-circuit or excessive current drain condition present. In this case, the output terminal 32 is assumed to be short-circuited to ground. The input signal I is positive at time 100, and, after a delay, the secondary pull-up transistor Q3 is turned on and begins to deliver current through resistor R1 to the output terminal 32. The current provided by the secondary pull-up transistor, Q3, passes through the

current-sensing resistor R1 and provides a voltage Vr, which turns on the pass-gate transistor, Q9, causing the voltage at terminal B to drop from a high level to a low level and remain at the low level for the duration of the high level portion of the input signal I. The low level at terminal B, after a slight delay, td1, causes the terminal L at the output of the first delay unit 50 to drop to a low level. After the propagation delay time, td2 provided by the second delay circuit 52, elapses, the voltage level at terminal M drops to a low level. Both terminal L and M, being at low levels, cause the voltage at terminal N to go to a high level. This, in turn activates Q10 and causes output terminal 32 to be connected to terminal A. The output signal Ya, at terminal 32, is at a short-circuited, or low level, which causes a low level to be present at terminal T4, on the gate of the primary pull-up transistor Q4. Therefore, transistor Q4 cannot turn on. The short-circuit current IYa through Q3 causes Vr to clamp the pass-gate transistor Q9 in the on-state, which holds Q4 off for the duration while I remains in a high state.

CELL 1 has a finite propagation delay, which can be used to advantage. If a short-circuit fault occurs on the output terminal, signal Y is at a low level, which is fed through to terminal A for disabling the primary pull-up,

transistor Q4. If no short-circuit occurs, signal Y goes from a low to high state.

3. A Differential Line-Driver System

Figure 5 shows a second line-driver, circuit 110. This circuit is the same in structure as the line-driver circuit 10, as described previously. In operation, the difference between these circuits is that the second line-driver, circuit 110, operates with a true input signal T at an input terminal 112 and at a false input signal F at an input terminal 114. These signal connections are the reverse of those signals as shown in connection with the first line-driver circuit 110 to provide a complementing output signal at Yb.

Figure 6 shows a complete differential line-driver circuit, having a first line driver circuit, designated block A, which is the same configuration as the line-driver circuit 10, as shown in figure 1. The other line-driver circuit, designated as block B, has the same configuration as the line-driver circuit 110, as shown in Figure 5.

An input signal I to this differential line-driver circuit is coupled to an input terminal 120, and an enable

signal En is provided at an input terminal 122, which is coupled to the input terminals 12 and 116, respectively, of Block A and Block B. The input signal I is inverted in a first input signal inverter 124. The output signal of that inverter is then three times inverted through a series of three inverters, 126, 128, 130, and then fed to one input of a NAND gate 132. The other input of the NAND gate 132 is the enable signal En, which serves to gate the input signal I to the input of another inverter 134, the output signal of which is the true signal T, as described in connection with figure 1.

The output signal of the inverter 124 is also passed through inverter 136 and 138 to one input terminal of another NAND gate 140, which is also activated by the enable signal En. The output signal of the other NAND gate 140 is inverted by inverter 142, the output of which is the false signal F. The delay through the inverters 126, 128 and 130 and the delay through the inverters 136 and 138 are matched, so that the true signal T and the false signal F are complementary.

Both Block A and Block B for the differential line-driver system, as shown in figure 6, have the protection circuitry. With this circuit design, the complementary output signals Ya and Yb of this differential line-driver

system have a skew characteristic of less than 1.5 nanoseconds, where skew has been defined as the time difference between the respective signals passing through their 50 percent amplitude points. This skew characteristic is possible, even though current-sensing was used to trigger a short-circuit protection circuit, because the current sensed was not the pull-up current of the primary pull-up transistor, but, rather, the pull-up current of the secondary pull-up transistor. It should be appreciated that the design provides a protective scheme, which does not interfere with the normal operation of the circuit. For example, the current-sensing resistor does not cause a difference between the rise-time and fall-time of a line-driver stage. Since Block A and Block B are operating in complementary modes, the rise-time of Block A coincides with the fall-time of Block B, and vice-versa. Therefore, any difference between rise-time and fall-time would produce significant degradation in the skew charateristic for the complementary, differential output signals Ya and Yb.

V. SIMULATION RESULTS

The circuit design is based on 1 micron, P-well CMOS technology, and the simulation was done by using AMD CS21 SPICE models. A 0.5ns output skew, 6ns propagation delays and less than a 200uA quiescent power supply current was achieved from a 5-volt power supply over the -55°C to 155°C temperature range.

The simulation results of major specifications are given in table 1 on page 32. Figure 7 shows the circuit test condition. The SPICE program list and the output waveforms are included in the Appendices. The circuit layout is shown in Figure 8.

VI. DISCUSSION

The line driver circuit includes two pull-up transistors, coupled between the positive voltage supply and the output terminal. One, called the primary pull-up transistor, provides a primary current to a load. The other, called a secondary pull-up transistor, provides a secondary current to the load. Protecting the current against short-circuits at its output terminal, means are providing for disabling conduction of the primary pull-up transistor, when the secondary current exceeds a predetermined level for a period greater than a predetermined time period. Typically, the predetermined time period is set to be greater than the usual transition time for a pull-up transistor, connected to an output terminal going from a low to a high state. During that transition time, a transient current spike is produced. A short-circuit protection scheme must distinguish between that transient current and a true short-circuit fault current.

Note that, since there is no power supply involved on a transmission line, the chances for output load short circuits to positive voltage supply are very small, therefore, the output load short circuits to positive

voltage supply is not protected in this design.

A fault signal, indicative of a short-circuit condition, is active when the secondary current exceeds the predetermined level for the predetermined time period. To prevent false triggering of the protection mechanism, the fault signal is delayed and compared to the fault signal. A cutoff signal is provided by the comparator when the fault signal and the delayed fault signal are active at the same time.

The cutoff signal drives a switch, which couples the output terminal to a control input terminal of a logic gate. The logic gate inhibits drive signals to the primary pull-up transistor, when the cutoff signal is active, which occurs when the output terminal is short-circuited.

According to another aspect of the design, a means for sensing the current through the secondary pull-up transistor is provided, which includes, for example, a current-sensing resistor, connected in series with the secondary pull-up transistor. The current through the resistor develops a sensing voltage, which activates a pass-gate transistor to produce the fault signal.

Still another aspect of the design provides a differential line-driver system, using a pair of short-circuit protected line-driver circuits arranged to provide complementary, differential output signals. Each of these line-driver circuits is configured with the short-circuit protection capability of the invention. Since the short-circuit detection and protection circuitry does not significantly change the performance characteristics of each line-driver circuit, the skew characteristic for a differential system, using two complementary line-driver circuits will not be significantly affected.

Each of the respective line-driver circuits is driven by producing a true input signal and a complementary false input signal from a single input signal. To ensure accurate phasing between the true signal and the complementary false signals, appropriate signal delays are introduced in each signal path, prior to the line-driver circuits. A system-enable signal directs the true and false input signals to the respective line driver circuits. When the system-enable signal is inactive, each output terminal is in a high impedance state.

VII. CONCLUSION

A CMOS differential line-driver with short circuit protection is presented. The protection circuit provided is one in which the output current is sensed and the output device is shut-off for protection, when the output is shorted to the ground. Furthermore, a comparator is added to distinguish between a transient current and a true short-circuit fault current.

The circuit was designed, using 1 micron p-well CMOS technology with TTL compatible input, and operates from a 5-volt power supply. The driver could drive up to 1 kilometer cable at a 24 mega-hertz data rate over the -55°C to 155°C temperature range.

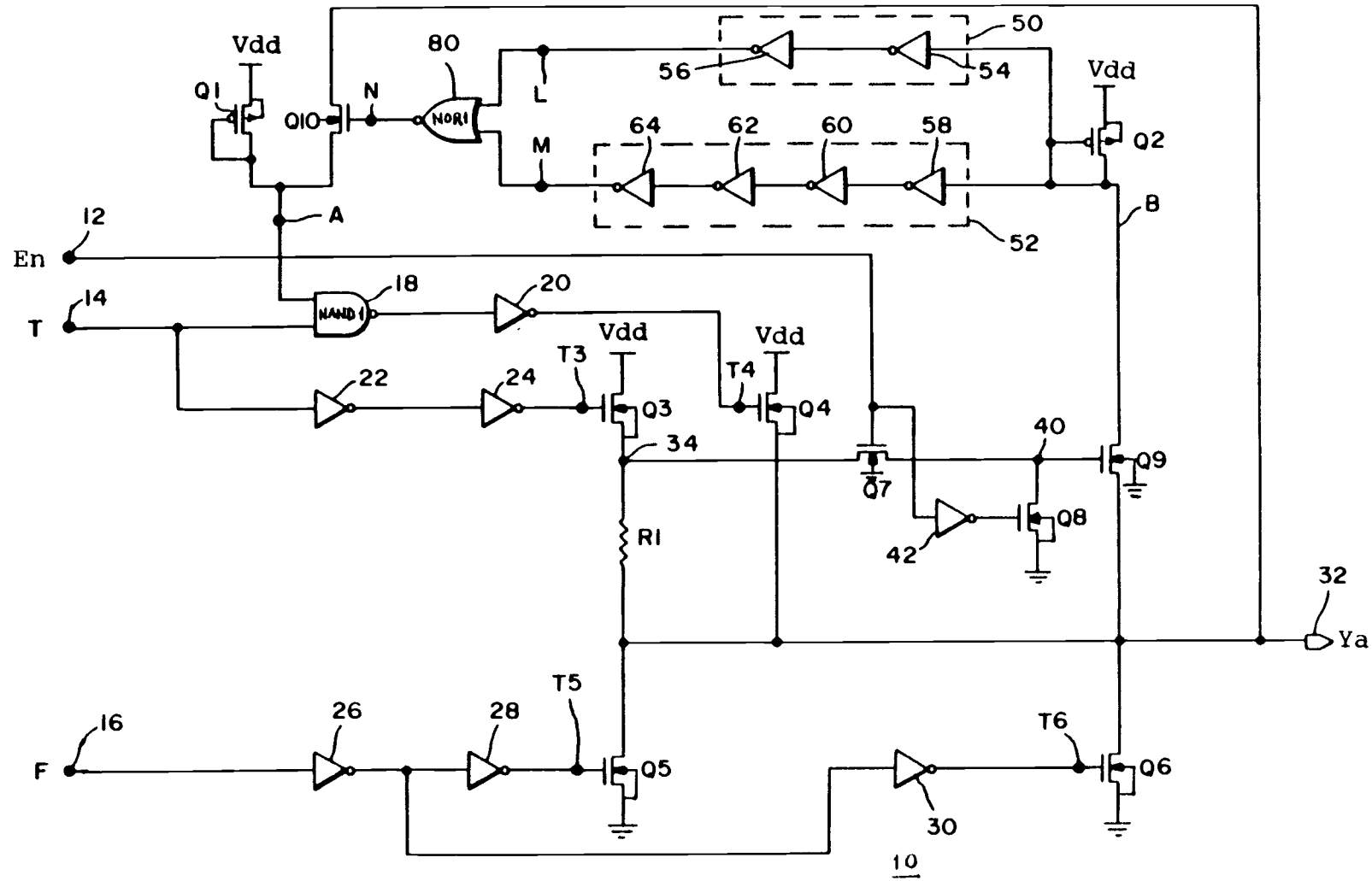


Figure 1. Schematic for line driver circuit

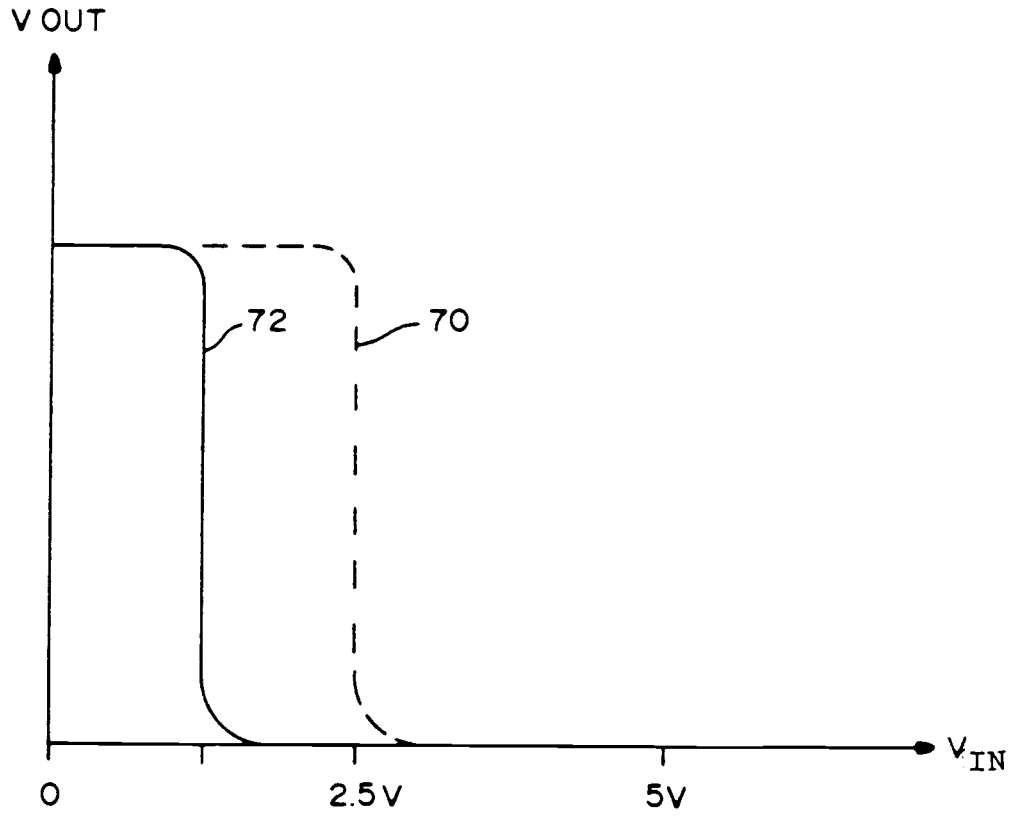


Figure 2. DC transfer curve of CMOS inverter

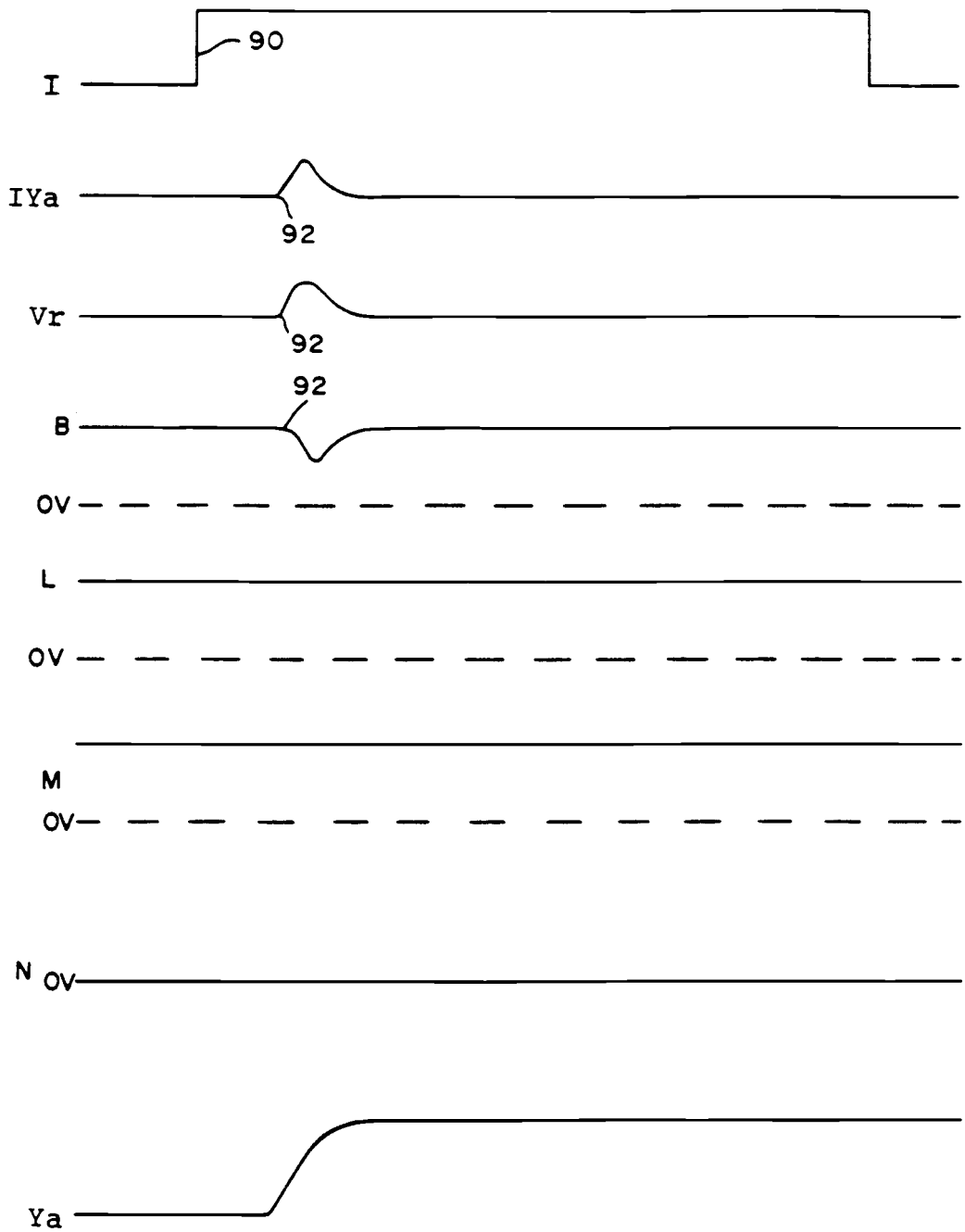


Figure 3. Signal waveforms at various terminals with the output non-shorted

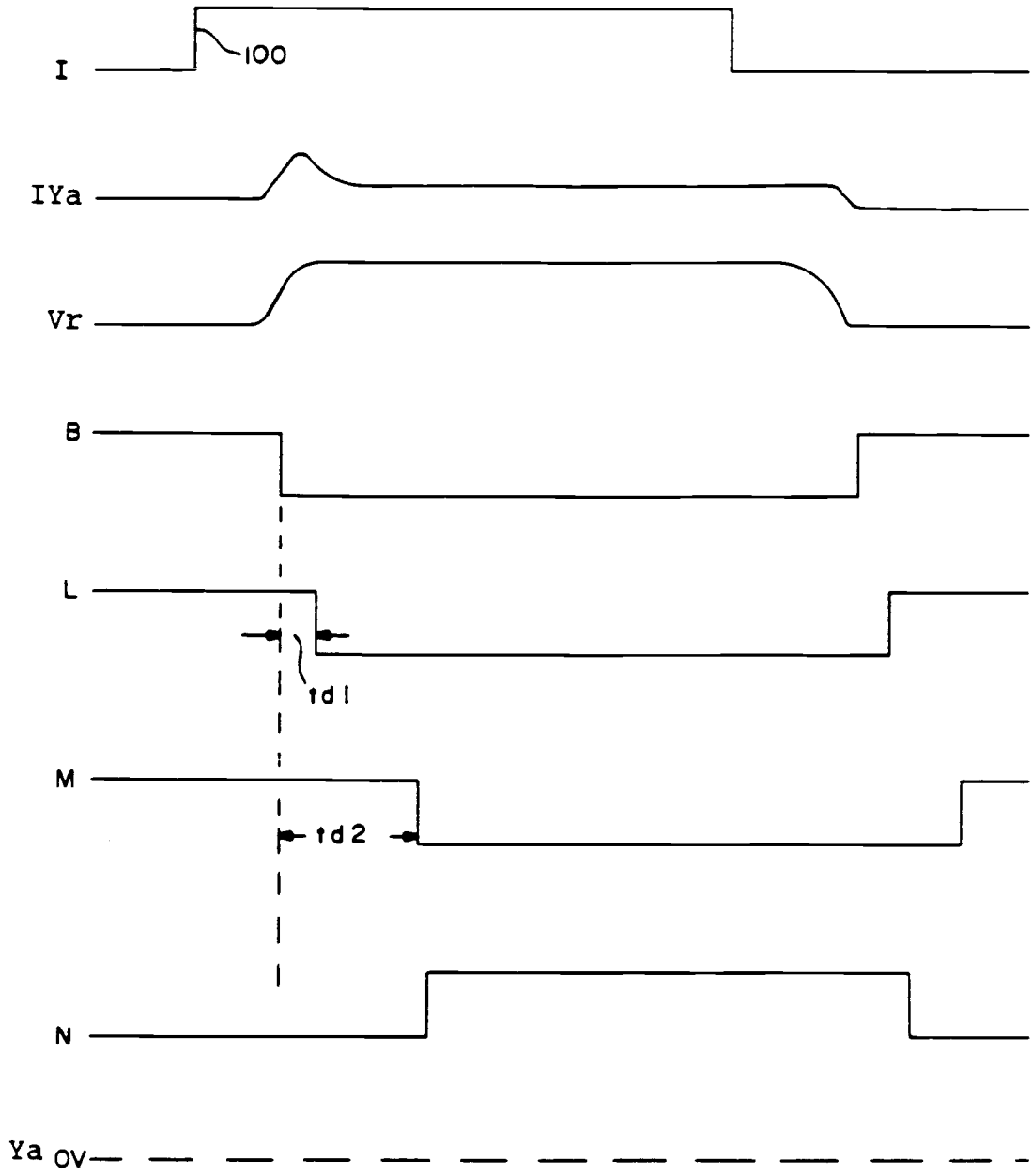


Figure 4. Signal waveforms at various terminals with the output shorted

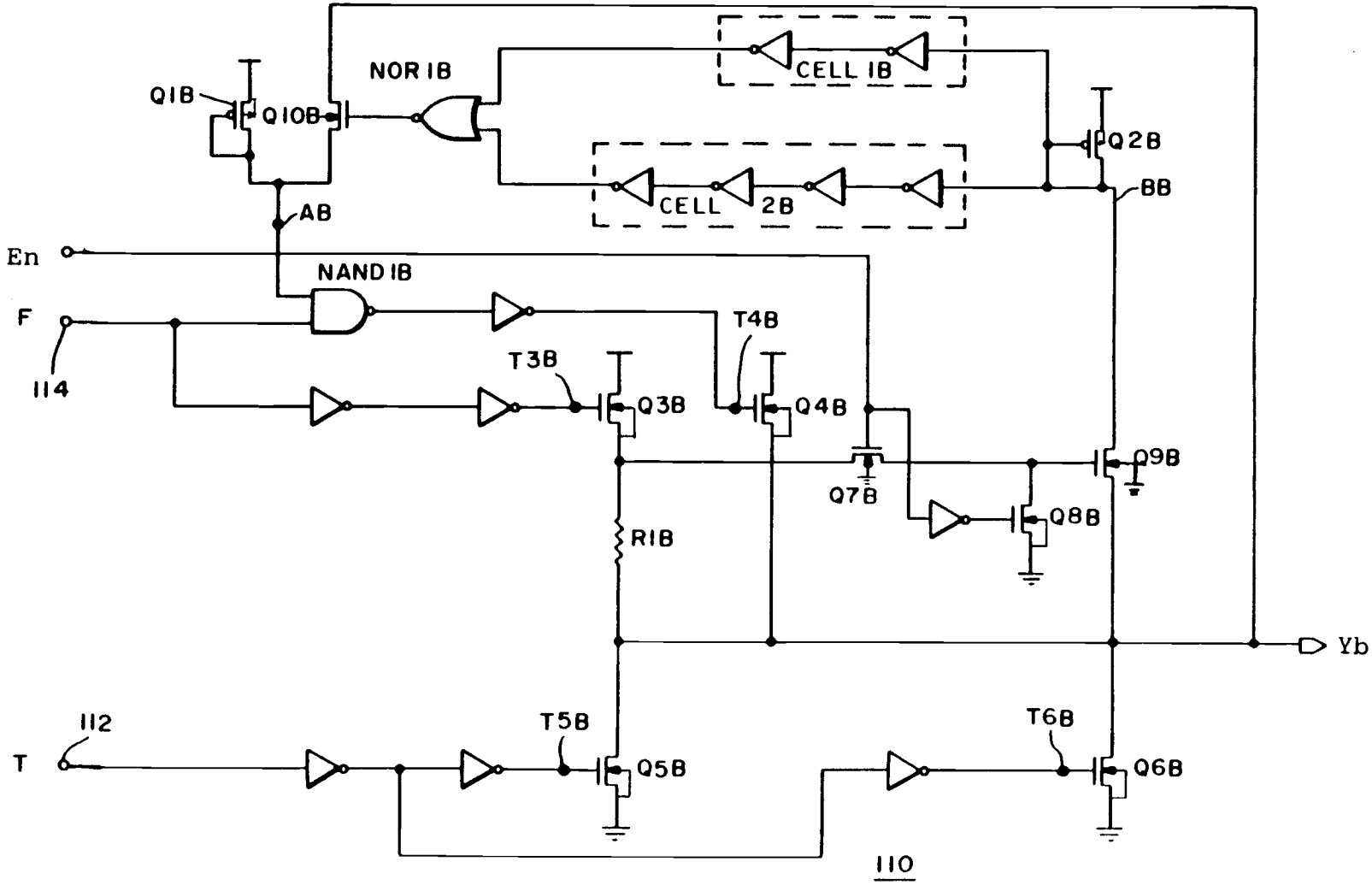


Figure 5. Schematic for complementary driver circuit

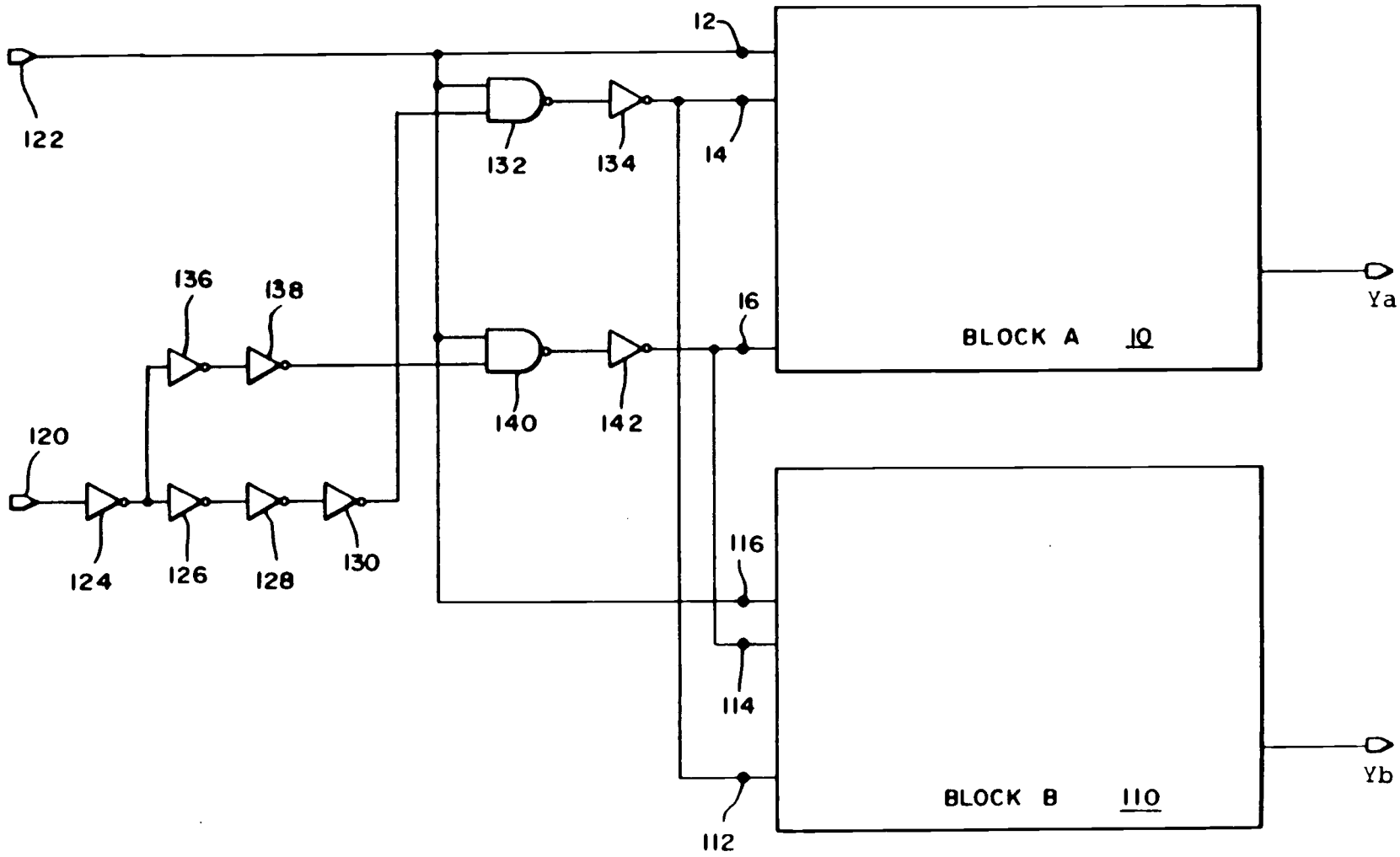
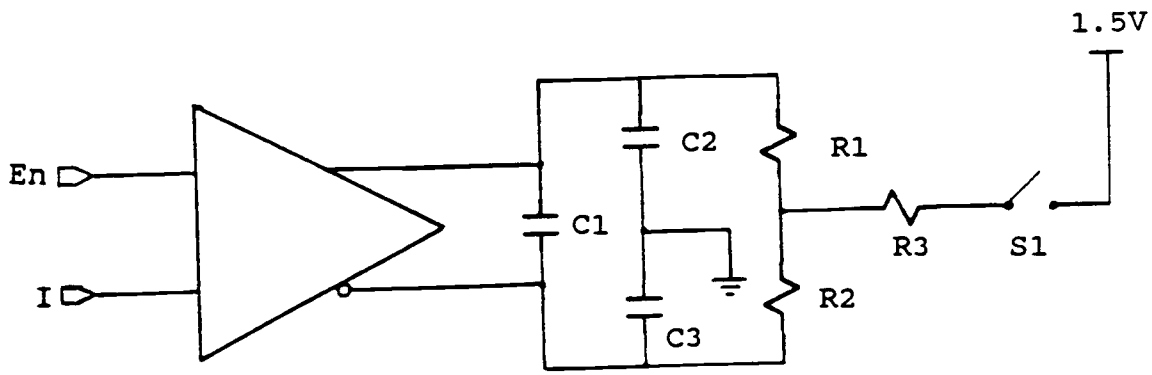


Figure 6. Schematic for complete differential line-driver system



C1 = C2 = C3 = 40pf R1 = R2 = 50 Ohm R3 = 500 Ohm

Figure 7. The line-driver test condition

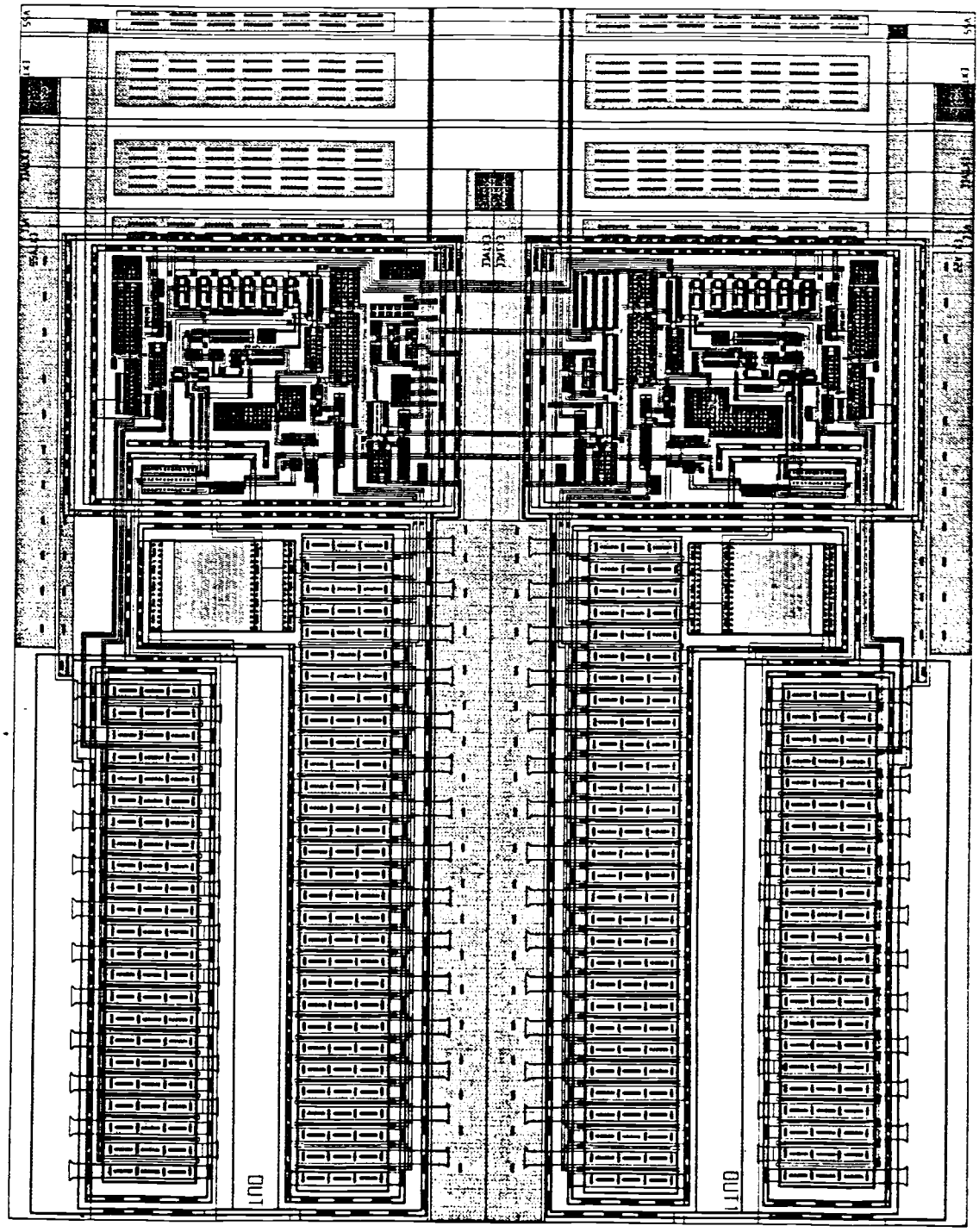


Figure 8. A layout for the differential line driver

Table 1. CMOS Differential Line Driver Simulation Results

symbols	parameters	conditions	typ	max	unit
Voh	Output high	Vcc=4.5 Vin=4.5 Temp=155 °c Iload=-20ma	2.6		V
Vol	Output low			320	mV
Isc	Output short current	Vcc=5.5v Vin=5.5v Temp=-55 °c		-70	mA
Skew		S1 open	0.5	1.5	ns
tTLH tTHL	Diff output Rise & Fall time	S1 open	4.0	8.0	ns
tPLH tPHL	Propagation delay input to output	S1 open	6.0	10.0	ns
tPZH	Output enable time	S1 closed	6.0	8.0	ns
tPZL	Output enable time	S1 closed	6.0	8.0	ns
tPHZ	Output disable time	S1 closed	5.0	7.0	ns
tPLZ	Output disable time	S1 closed	5.0	7.0	ns
Icc	Quiescent power supply current	Vin=Vcc/GND Vin=2.4/0.5	200 0.8		uA mA

VIII. REFERENCES

[1] D. Conway, "Short-Circuit Protection Circuit", U.S. Patent No. 3,944,889, March 16, 1976.

[2] R. R. Laupman, "Device For Protecting an Audio Amplifier Against Overload or Short-Circuit", U.S. Patent No. 4,291,357, March 30, 1982.

[3] J. J. Hong, "Short-Circuit Protection Circuit", U.S. Patent No. 4,291,357, Sept. 22, 1981.

[4] L. Y. Chan, "Universal Differential Line Driver Integrated Circuit", U.S. Patent No. 4,042,840, Aug. 16, 1977.

[5] A. J. Leidich, "PNP Output Short Circuit Protection", U.S. Patent No. 4,232,273, Nov. 4, 1980.

[6] W. Y. Jiang, S. K. Kong, W. Chan, "Differential Line Driver with Short Circuit Protection", U.S. Patent on pending, Nov. 18, 1988.

IX. APPENDICES

APPENDIX A. The SPICE Program List

```
*********************************************************************
*
*  Drawing Name : DRIVER_SPM
* ------------------------- Output Pins ----------------------*
*
*  90 99
*
* ------------------------- Input Pins -----------------------*
*
*  100 101 102
*
* ------------------------- I/O Pins -------------------------*
*
.OPTIONS NOMOD NOPAGE NODE ACCT ASPEC
.GLOBAL 1 0
.OPTIONS DCFOR=5 DCHOLD=5 ITL1=400 GMINDC=1E-10 DV=0.5
.TEMP 25
.TRAN 0.2NS 35NS
.NODESET V(91)=3V V(191)=0V V(192)=5V V(92)=0 V(268)=1.5 V(248)
VCC 1 0 5.0
V101 101 0 5.0V
V102 102 0 0V
V100 100 0 PL 0V 0NS 0V 9.0NS 3.0V 11.0NS 3.0V 19.0NS 0V 21.0NS
*** LOADING ***
RL1 90 391 50
RL2 391 99 50
CL1 90 99 40PF
CL2 90 0  40PF
CL3 99 0  40PF
C80 80 0 1.5PF
C23 23 0 0.5PF
```

```
MN0031  70 94 0 0 TN 16 1
MP0032  18 17 1 1 TP 48 1
MN0033  18 17 0 0 TN 24 1
MP0034  80 17 1 1 TP 48 1
MN0035  80 17 0 0 TN 24 1
MP0036  26 25 1 1 TP 16 1
MN0037  26 25 0 0 TN 10 1
MP0038  16 92 1 1 TP 80 1
MN0039  16 92 0 0 TN 40 1
MP0040  23 22 1 1 TP 16 1
MN0041  23 22 0 0 TN 10 1
MP0042  25 24 1 1 TP 13 1
MN0043  25 24 0 0 TN 7 1
MP0044  191 91 1 1 TP 36 2
MN0045  191 91 0 0 TN 88 2
MP0144  192 191 1 1 TP 10 1
MN0145  192 191 0 0 TN 7 1
MP0146  92 192 1 1 TP 32 1
MN0147  92 192 0 0 TN 16 1
MP0046  22 21 1 1 TP 9 2
MN0047  22 21 0 0 TN  7 2
MP0048  24 21 1 1 TP 9 1
MN0049  24 21 0 0 TN  7 1
MP0050  15 14 1 1 TP 16 1
MN0051  15 14 0 0 TN 8  1
MP0052  21 100 1 1 TP 40 2
MN0053  21 100 0 0 TN 120 2
MP0054  12 11 1 1 TP 16 1
```

```
MN0057  14 13 0 0 TN 7 1
MP0058  11 101 1 1 TP 40 2
MN0059  11 101 0 0 TN 120 2
MP0060  13 102 1 1 TP 40 2
MN0061  13 102 0 0 TN 120 2
MN0062  268 66 90 90 TN 40 1.8
MN0063  90 73 0  0  TN 68 1.8 M=20
MN0064  248 46 99 99 TN 40 1.8
MN0065  99 53 0  0  TN 68 1.8 M=20
MN0066  66 67 0  0  TN 8  1
MN0067  46 47 0  0  TN 8  1
MN0068  66 80 65 0  TN 24 1
MN0069  46 80 45 0  TN 24 1
MN0070  1  64 90 90 TN 68 1.8 M=25
MN0071  1  44 99 99 TN 68 1.8 M=25
MN0072  1  62 65 90 TN 68 1.8 M=4
MN0073  90 72 0  0  TN 68 1.8 M=2
MN0074  1  42 45 99 TN 68 1.8 M=4
MN0075  99 52 0  0  TN 68 1.8 M=2
MN0076  17 12 0  0  TN 8  1
MN0077  17 15 0  0  TN 8  1
MN0078  1 1 91 91 TN 5 1
MN0079  91 91 0 0 TN 5 1
MP0080  268 268 1 1 TP 7 3
MP0081  248 248 1 1 TP 7 3
MP0082  19 12 1 1 TP 32 1
MP0083  17 15 19 1 TP 32 1
MP0084  93 80 1 1 TP 30 1
```

```
MN0001  67 80 0 0 TN 6 1
MP0002  47 80 1 1 TP 12 1
MP0003  47 80 0 0 TN 6 1
MP0004  73 71 1 1 TP 200 1
MN0005  73 71 0 0 TN 80  1
MP0006  53 51 1 1 TP 200 1
MN0007  53 51 0 0 TN 80  1
MP0008  64 63 1 1 TP 200 1
MN0009  64 63 0 0 TN 100 1
MP0010  44 43 1 1 TP 200 1
MN0011  44 43 0 0 TN 100 1
MP0012  62 61 1 1 TP 32 1
MN0013  62 61 0 0 TN 16 1
MP0014  42 41 1 1 TP 32 1
MN0015  42 41 0 0 TN 16 1
MP0016  72 71 1 1 TP 60 1
MN0017  72 71 0 0 TN 20 1
MP0018  52 51 1 1 TP 60 1
MN0019  52 51 0 0 TN 20 1
MP0020  61 60 1 1 TP 24 1
MN0021  61 60 0 0 TN 12 1
MP0022  71 70 1 1 TP 36 1
MN0023  71 70 0 0 TN 12 1
MP0024  41 70 1 1 TP 24 1
MN0025  41 70 0 0 TN 12 1
MP0026  51 60 1 1 TP 36 1
MN0027  51 60 0 0 TN 12 1
MP0028  60 93 1 1 TP 32 1
```

```
MN0087  93 80  210 0 TN 24 1
MN0088  210 26 220 0 TN 24 1
MN0089  220 16 0 0 TN 24 1
MP0090  94 80 1 1 TP 30 1
MP0091  94 23 1 1 TP 30 1
MP0092  94 16 1 1 TP 30 1
MN0093  94 80 230 0 TN 24 1
MN0094  230 23 240 0 TN 24 1
MN0095  240 16 0 0 TN 24 1
MP0096  63 68 1 1 TP 32 1
MP0097  63 60 1 1 TP 32 1
MN0098  63 68 111 0 TN 32 1
MN0099  111 60 0 0 TN 32 1
MP0100  43 48 1 1 TP 32 1
MP0101  43 70 1 1 TP 32 1
MN0102  43 48 122 0 TN 32 1
MN0103  122 70 0 0  TN 32 1
MN0301 274 268 0 0 TN 32 2
MP0302 274 268 1 1 TP 8  2
MN0303 273 274 0 0 TN 10 1
MP0304 273 274 1 1 TP 12 1
MN0305 270 273 0 0 TN 7 1
MN0306 270 271 0 0 TN 7 1
MP0307 270 273 371 1 TP 26 1
MP0308 371 271 1 1 TP 26 1
MN0309 68 270 90 90 TN 40 1.8
MP0310 68 68 1 1 TP 7 3
X1 268 279 INV
```

```
X4 272 261 INV
X5 261 262 INV
X6 262 271 INV
MN0401 474 248 0 0 TN 32 2
MP0402 474 248 1 1 TP 8  2
MN0403 473 474 0 0 TN 10 1
MP0404 473 474 1 1 TP 12 1
MN0405 470 473 0 0 TN 7 1
MN0406 470 471 0 0 TN 7 1
MP0407 470 473 571 1 TP 26 1
MP0408 571 471 1 1 TP 26 1
MN0409 48 470 99 99 TN 40 1.8
MP0410 48 48 1 1 TP 7 3
X7 248 479 INV
X8 479 478 INV
X9 478 472 INV
X10 472 461 INV
X11 461 462 INV
X12 462 471 INV
R104 90 65 50
R105 99 45 50
.MACRO INV 10 20
MN0913 20 10 0 0 TN 5 4
MP0914 20 10 1 1 TP 10 4
.EOM
.LIB 78 CS21TYP
*.LIB 78 CS21BC
*.LIB 78 CS21WC
```

```
.OPTIONS POST=2

.PLOT TRAN V(90) V(99)

.PLOT TRAN V(80) V(100)

*.PRINT TRAN V(90) V(99)


.END $DRIVER_SPM
*
```

APPENDIX B. The Simulation Waveforms

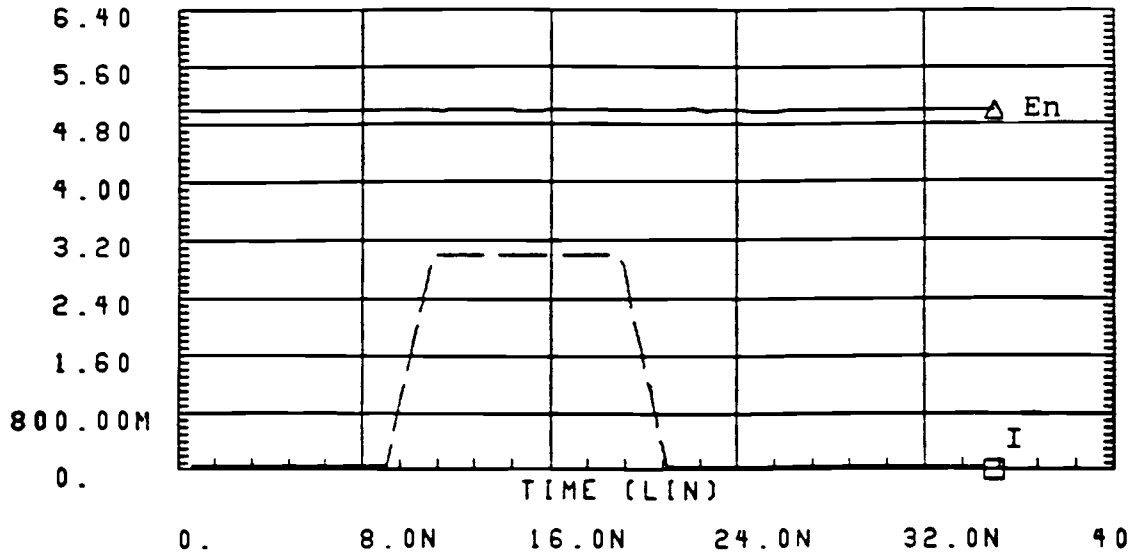


Figure 9. Input waveform of the line driver

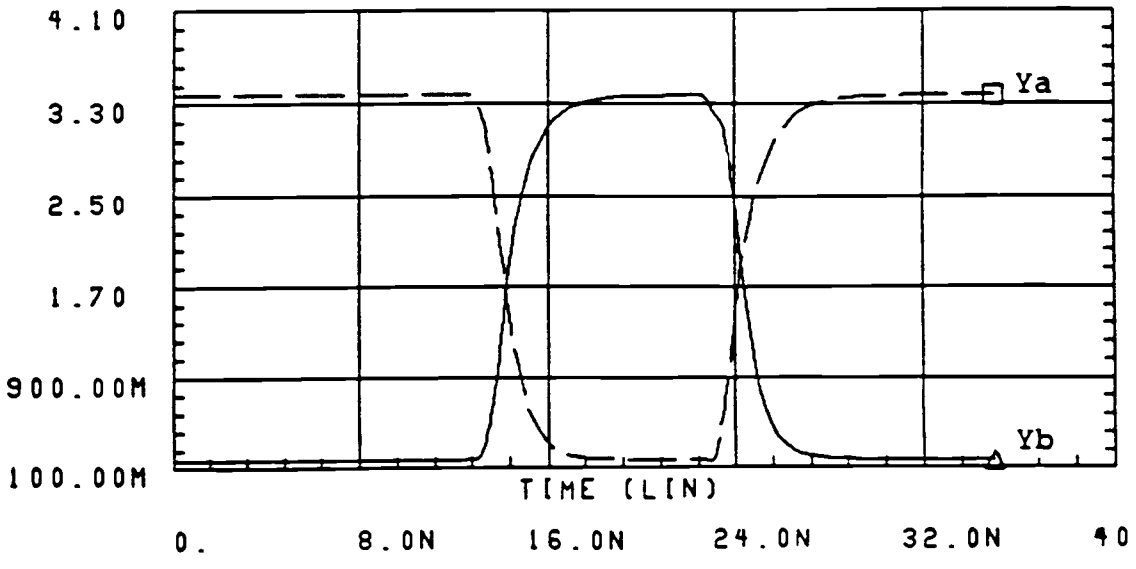


Figure 10. Output waveform of the line driver