Title: **AN INTEGRATED MOS VOLTAGE-CONTROLLED LOW FREQUENCY OSCILLATOR**

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James C. Looney

In this work the use of linear MOS integrated circuits in the design of a phase-shift oscillator is presented. By multiplying the capacitors of the RC feedback network through the use of the Miller effect, large effective capacitance values are obtained which enable the low frequency operation of the oscillator. MOS devices are also used as resistors in the feedback network. Thus the oscillator is easily tuned by an external voltage over a range of 30 Hz-8 KHz. In the design range of 500-1500 Hz the output frequency is directly related to the tuning voltage with a slope of -500 Hz/volt.

A scheme of automatic frequency stabilization is suggested. The design and results of a typical fabricated device of this variety are also presented.

It is thus shown that a complete system employing only MOS devices is practical and may replace some of the present bipolar circuits in due course.
An Integrated MOS Voltage-Controlled Low Frequency Oscillator

by

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AN INTEGRATED MOS VOLTAGE-CONTROLLED LOW FREQUENCY OSCILLATOR

I. INTRODUCTION

In recent years many large and complex digital circuits have been produced by the semiconductor industry. Most of these circuits employ all Metal-Oxide-Semiconductor (MOS) devices and it is the rapid advancement in the MOS technology which has made the large scale integration (LSI) possible. MOS devices have several advantages over their bipolar counterparts: production is simpler, less expensive, and more efficient; sizes are smaller so higher package density is allowed. In spite of all these, linear circuits have been very rare and only discrete devices have been produced.

This work is aimed at application of MOS linear integrated circuits (IC's) in building an oscillator capable of producing a nearly sinusoidal output. The objective is to develop linear MOS IC's for operation in the audio frequency range where component values may be very large and essentially not possible in the bipolar IC regime. The choice of this frequency range is also due to the many applications of such oscillators in various instruments. The techniques presented in this paper enhance the usefulness of MOS devices as well as some circuits which in the past were used with vacuum tubes and bipolar transistors.
II. MOS CONCEPTS AND CIRCUITS

Basic Structure and Operation Principles

MOS structure consists of a layer of metal on a thin layer of insulating oxide which has been deposited or thermally grown on a semiconductor substrate. Typically, the metal is aluminum, and the oxide is thermally grown $\text{SiO}_2$ on a p-type or n-type silicon substrate. With an n-type substrate the devices will have p-type channels as shown in Figure 1. The source and drain $p^+$ areas are the result of a thermal diffusion carried out for this purpose. The gate metal and the substrate channel area act as the two electrodes of a parallel plate capacitor with the $\text{SiO}_2$ dielectric in between them. If it is assumed that there is no charge in the thin oxide, any electric field in the oxide will start and terminate on equal and opposite charges, thus extending between the gate and the channel area. When polarity of the gate voltage with respect to the semiconductor substrate is of the same sign as the sign of majority carriers in the substrate, the charges required in the channel area will be the minority carriers of the substrate. Thus the minority carrier density increases in the channel area at the expense of majority carriers. Subsequently a transition from one type to intrinsic, then to the other type will take place as gate bias is increased, and a depletion layer is formed between the inverted region (channel) and the substrate. (In this work p-channel devices are of interest so the gate bias must be negative to invert the n-type substrate in the channel area.) The source and drain $p^+$ areas are then electrically connected through the inverted region.
Figure 1. View of the cross-section of an MOS (p-channel) device. (not to scale)
and electrical conduction may take place via the mobile carriers in the channel. The device is then bilateral as carriers may move from source to drain or vice versa. Since the conduction involves essentially one type of charge carriers (holes in the case of a p-channel device), the device is unipolar.

In practical devices there is some net charge in the oxide due to surface states at the silicon-silicon dioxide interface, and also mobile ionic contaminants such as Na⁺. Thus the required gate bias for inducing the channel may be of either polarity! If the channel exists with no gate bias the device is called a depletion-mode device, since voltage must be applied to the gate in order to stop conduction. The enhancement-mode devices require a gate bias above a minimum threshold to initiate the current flow. This threshold voltage is necessary to compensate for the surface state charges, for maintaining a depletion region between the channel and substrate, for cancelling the work function difference between the metal and semiconductor, etc. (2, 6).

**Behavior at the Terminals and Equations**

As for other two-port active devices, the output V-I characteristic curves as a function of the input (voltage) are of interest. Only p-channel devices will be considered in the rest of this paper. The results obtained could apply to n-channel devices only after proper change of signs and threshold voltage consideration. Figure 2a shows the source-drain V-I curves for an MOS transistor. The symbology is shown in Figure 2b. Two distinct regions can be recognized immediately: one is the linear region where drain current and drain voltage are al-
Figure 2. V-I characteristics and symbol of an MOS p-channel transistor
a) Voltage-current behavior for different gate biases as indicated.
b) Symbol generally used for p-channel devices.
(this symbol will be used throughout this paper.)
most linearly related. The other is the saturated region where drain current and drain voltage show a much smaller slope, representing a high resistance. Ideally, in this region the current must be independent of drain voltage.

By using a model as shown in figure 3, it has been shown (2, 6, 13) that the terminal current-voltage relationship in the linear region can be expressed as:

\[ I_D = -\frac{\varepsilon_{ox} W}{t_{ox}} L \left( V_G - V_{th} - \frac{1}{2} V_D \right) V_D \quad |V_D| < |V_G - V_{th}| \quad (1) \]

where

- \( I_D \) is the drain current
- \( \varepsilon_{ox} \) is the permittivity of the oxide
- \( t_{ox} \) is the thickness of the oxide
- \( W \) is the channel width
- \( L \) is the channel length
- \( \mu \) is the mobility of holes in the inversion layer (channel)
- \( V_G \) is the applied gate voltage
- \( V_{th} \) is the threshold voltage = \( (Q_{ss} + Q_D) t_{ox}/\varepsilon_{ox} \)
- \( Q_{ss} \) is the charge of the surface states
- \( Q_D \) is the charge induced inside the semiconductor by the gate bias
- \( V_D \) is the drain voltage

As the drain voltage approaches the condition \( |V_D| = |V_G - V_{th}| \) the inversion layer becomes thinner near the drain and the validity of Eq. (1) decreases. At \( V_D = V_G - V_{th} \) the knee of the V-I curve is reached.

The effective gate bias at the area immediately adjacent to the drain
Figure 3. A p-channel MOS device model for calculation of terminal characteristics. (2,6,13)
is zero and the inversion layer thickness is minimum. The terminal behavior in this mode can be given (5) as

\[ I_D = \frac{-\mu_{ox}}{2\tau_{ox}} \frac{W}{L} (V_G - V'_{th})^2 \quad |V_D| < |V_G - V_{th}| \]

where

\[ V'_{th} = V_{th} + 2/3\phi (V_G - V_{th})^{1/2}, \quad \phi = \frac{\phi}{\varepsilon_{ox}} (2\varepsilon_s qN)^{1/2} \]

\[ \varepsilon_s \text{ is the permittivity of silicon} \]
\[ q \text{ is the electronic charge} \]
\[ N \text{ is the density of electrons in the semiconductor} \]

Beyond the knee (\(|V_D| > |V_G - V_{th}|\)) the channel length (L) decreases due to the extension of the drain depletion region into the channel area. As a result the saturation current increases from the value at the knee given by Eq. (2) by a factor of \(L/(L - L')\) where \(L'\) is the length of the drain depletion region extending into the channel and

\[ L' = \left( \frac{2\varepsilon_s (V_D - V_G + V_{th})^{1/2}}{qN} \right) \]

This increase in current results in the finite slope of the curves in the saturation region (2, p.35)

If the substrate is returned to a positive voltage, and/or if the source is connected to a negative voltage, with respect to the substrate, the depletion region between the inversion layer and substrate becomes wider due to larger junction reverse bias and extends into the substrate. The resulting uncovered immobile charges in the semiconductor which are at the expense of the mobile one in the channel become terminating charges for some of the electric field lines from the
channel and the electric field between the gate electrode and the channel is reduced. Thus there is a decrease in the effective gate bias and this can be considered as an increase in the threshold voltage. To a good degree of approximation, the new threshold voltage can be expressed as (2, p. 44)

$$V_{th}(V_{BG}) = V_{th} + \Delta V_{th}$$

where

$$\Delta V_{th} = -\frac{t_{ox}}{e_{ox}} (2q\varepsilon_s N)^{1/2} ((2\phi_F + V_{BG})^{1/2} - (2\phi_F)^{1/2})$$

$V_{BG}$ is the applied back gate bias

$\phi_F = \frac{kT}{q} \ln\left(\frac{N}{n_i}\right)$ is the Fermi potential

$k$ is Boltzmann's constant

$T$ is the absolute temperature

$N$ is the donor impurity concentration in the substrate

$n_i$ is the intrinsic impurity concentration in the semiconductor

Figure 4 shows the threshold voltage increase as a function of back gate bias in the region pertinent to this work.

The transconductance of an MOS device is defined by

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D}$$

and represents the available gain of the device. From Eq. (1) one obtains upon differentiation

$$g_m = -\frac{\mu e_{ox}}{t_{ox}} \frac{W}{L} V_D \quad \text{linear region, } |V_D| < |V_G - V_{th}|$$

If the dependence of mobility upon gate voltage is also considered,
Figure 4. Increase of the threshold voltage of p-channel MOS devices as a function of back gate bias. (2)

Figure 5. Schematic diagram of a common-source MOS IC amplifier stage employing a saturated load device. (p-channel devices)
the expression for transconductance becomes (2, p.66)

\[ g'_m = g_m - \left| \frac{\partial u}{\partial V_G} \right| \left( \frac{\mu \varepsilon_{ox} W}{t_{ox}} \right) \left( (V_G - V_{th}) V_D - \frac{V_D^2}{2} \right) \]  

For the saturation region differentiation of Eq. (2) yields

\[ g''_m = -\frac{\mu \varepsilon_{ox}}{t_{ox}} \frac{W}{L} (V_G - V_{th}) \left| \frac{V_D}{V_D} \right| \text{ saturation region, } |V_D| \geq |V_G - V_{th}| \]  

\[ (7) \]

**MOS Resistor**

Equation (1) expressed the V-I behavior of an MOS device in the linear region where \(|V_D| < |V_G - V_{th}|\). For small drain voltages where \(|V_D| << |V_G - V_{th}|\), the \(V_D/2\) term inside the square brackets can be neglected and the resulting equation is

\[ I_D = -\beta (V_G - V_{th}) V_D \]  

\[ (8) \]

where

\[ \beta = \frac{\mu \varepsilon_{ox}}{t_{ox}} \frac{W}{L} \]

This implies that for small drain voltages, the device acts as a voltage-dependent resistor of the approximate form

\[ R_{dc} = r_{ac} = \left( -\beta (V_G - V_{th}) \right)^{-1} \text{ linear region} \]

\[ (9) \]

(For more detailed analysis see (15)). If such a device is used as the load resistor, the source voltage acts as the back gate bias and the threshold voltage is raised in accordance with Eq. (4). Although this effect adds to its nonlinearity, the MOS resistor can be used in linear circuits with a fair degree of success. In digital applications the use of MOS resistors is quite satisfactory and has been extensively employed in industry. Comparison of Eq. (7) and Eq. (9) gives
The effective resistance represented by the V-I relationship for the MOS device in the saturation region is also available to the IC designer. In this case $|V_D| > |V_G - V_{th}|$ and in general $V_D = V_G$, i.e., the gate is connected to the drain. Then

$$I_D = -(\beta/2)(V_G - V_{th})^2 = -(\beta/2)(V_D - V_{th})^2$$

but

$$g_m'' = -\beta(V_D - V_{th})$$

and

$$I_D = \frac{g_m''}{2} (V_D - V_{th})$$

or

$$I_D = \frac{(V_D - V_{th})}{(2/g_m'')}$$

and the dc resistance of the device is

$$R_{dc} = \frac{2}{g_m''} \quad \text{saturation region} \quad (11)$$

and the minimum drain voltage must be $V_{th}$. The expression for the ac resistance is rather complicated. The drain current is

$$I_D = I_{DSAT} \frac{L}{L - L'}$$

where

$L$ is the channel length

$I_{DSAT}$ and $L'$ are given by Eqs. (2) and (3) respectively.

So

$$r_{ac} = -\frac{2qN}{L} \left( \frac{L - L'}{L} \right)^2 \left( \frac{L - L'}{L} \right)^2 = \frac{g_m''}{2} \left( \frac{L - L'}{L} \right)^2 \left( \frac{L - L'}{L} \right)^2 \frac{2}{g_m''} \quad (12)$$
More details can be found in (3) and (11).

**MOS Capacitor**

The MOS capacitor uses the thin oxide grown during the gate oxide formation as the dielectric. The top electrode is the evaporated metal and the bottom electrode could be either the substrate or a p$^+$ diffused area. If the substrate is to be used as the back electrode, the thick oxide must be etched through during gate area etching (see Appendix C). The thickness of the oxide may result in severe undercutting of the gate areas due to long etching periods required. In addition to this, accumulation, depletion and inversion of the substrate may take place when a negative voltage is applied to the top electrode. This will result in capacitance variations and is undesirable. Therefore, the bottom electrode is almost always diffused into the substrate during source-drain diffusion. If there are no mobile charges in the oxide, the capacitance will then be relatively constant even if some positive voltage is applied to the gate, as the p$^+$ area is hard to invert.

**MOS IC Amplifier**

The MOS amplifier in the integrated form consists of a "driver" transistor and a "load" transistor. The two configurations are common source and source follower.

**Common Source**

The configuration is shown in Figure 5. Since both transistors are on the same chip, both have a common, grounded substrate. Usually
$V_{GG} = V_{DD}$ and this case will be considered here. For the load device the condition $V_{DD} = V_{GG}$ implies that $|V_{DS}| \geq |V_{GS} - V_{th}|$ and the device is operating in the saturation region. The drain current of this transistor is then given by

$$I_{D1} = -\frac{\beta_L}{2} (V_{DD} - V_{th} - \Delta V_{th} - V_{out})^2$$

(13)

The driver device can be operated in either linear or saturation region, depending on the input voltage. In the linear region

$$I_{D2} = -\beta_D ((V_{in} - V_{th}) - \frac{V_{out}}{2}) V_{out} \quad |V_{out}| < |V_{in} - V_{th}|$$

(14)

and in the saturation region

$$I_{D3} = -\frac{\beta_D}{2} (V_{in} - V_{th})^2 \quad |V_{out}| \geq |V_{in} - V_{th}|$$

(15)

Equating the currents in the load and driver devices yields

$$\{V_{DD} - (V_{th} + \Delta V_{th}) - V_{out}\}^2 = \frac{2\beta_D}{\beta_L} \{V_{in} - V_{th} - V_{out}/2\} V_{out}$$

$$|V_{out}| < |V_{in} - V_{th}|$$

or

$$\{V_{DD} - (V_{th} + \Delta V_{th}) - V_{out}\}^2 = \frac{\beta_D}{\beta_L} (V_{in} - V_{th})^2$$

$$|V_{out}| \geq |V_{in} - V_{th}|$$

After defining $\beta_R \equiv \beta_D/\beta_L$,,

$$\frac{V_{in} - V_{th}}{2} + \{V_{DD} - (V_{th} + \Delta V_{th}) - V_{out}\}^2 (2V_{out}\beta_R)^{-1}$$

$$|V_{out}| < |V_{in} - V_{th}|$$

(16)

and
\[
V_{\text{out}} = -(\beta_R)^{1/2} V_{\text{in}} + V_{\text{DD}} - (1 - (\beta_R)^{1/2}) V_{\text{th}} - \Delta V_{\text{th}}
\]
\[
|V_{\text{out}}| \geq |V_{\text{in}} - V_{\text{th}}| \tag{17}
\]

The small signal gain of the amplifier is found to be

\[
A_v = \frac{3V_{\text{out}}}{3V_{\text{in}}}
\]

\[
A_{vl} = 2 \left(1 + (1/\beta_R) - (1/\beta_R) \frac{(V_{\text{DD}} - V_{\text{th}} - \Delta V_{\text{th}})^2}{(V_{\text{out}})^2}\right) \]
\[
|V_{\text{out}}| < |V_{\text{in}} - V_{\text{th}}| \tag{18}
\]

\[
A_{vl} = - (\beta_R)^{1/2} \left|V_{\text{out}}\right| \geq \left|V_{\text{in}} - V_{\text{th}}\right| \tag{19}
\]

As seen, in the case of saturated driver transistor the amplifier has a constant gain which is essentially dependent only on the geometry of the two devices. For a non-saturated driver transistor however, the gain depends on the drain bias, threshold voltage and output voltage. Since \(|V_{\text{DD}} - V_{\text{th}} - \Delta V_{\text{th}}| > |V_{\text{out}}|\), the gain decreases and approaches zero monotonically. This can be easily shown by first substituting in Eq. (17) the value of \(V_{\text{out}}\) at the boundary, i.e., \(V_{\text{out}}^{\text{max}} = V_{\text{in}} - V_{\text{th}}\). Then

\[
V_{\text{out}}^{\text{max}} = \frac{V_{\text{DD}} - V_{\text{th}} - \Delta V_{\text{th}}}{1 + \sqrt{\beta_R}}
\]

However, in the non-saturated region \(|V_{\text{out}}| < |V_{\text{in}} - V_{\text{th}}|\), so

\[
|V_{\text{out}}| < \frac{|V_{\text{DD}} - V_{\text{th}} - \Delta V_{\text{th}}|}{1 + \sqrt{\beta_R}}
\]

When this is substituted in the expression for gain, Eq. (18), the result is
Figure 6. Input-output relationship for the common-source MOS IC amplifier of Figure 5.

Figure 7. Small signal ac gain of the common-source amplifier.
\[ A_{v1} \leq 2\left(1 + \frac{1}{\beta R} - \frac{1}{\beta R}(1 + \sqrt{\beta R})^2\right) \]

or

\[ A_{v1} \leq \frac{2}{-2/(\beta R)^{1/2}} \]

That is

\[ A_{v1} \leq -(\beta R)^{1/2} \]

which is consistent with the value of the gain of the amplifier in the saturated driver case at the boundary!

**Source Follower**

In this configuration there are four possible cases depending upon the gate voltage supply of the source device. These will be considered separately. The general circuit diagram is shown in Figure 8 for all four configurations. In each case \( V_{GG} \) will be specifically designated.

**Gate of Resistor Device Returned to the Main Drain Supply**

When \( V_{in} = 0, V_{out} = 0 \) and \( |V_{GG} - V_{th}| > |V_{out}| \). So \( Q_L \) operates in the linear region. \( Q_D \) will operate initially in the saturation region. The currents in the devices are

\[ I_{DL} = -\beta L (V_{DD} - V_{th} - \frac{1}{2}V_{out})V_{out} \]

\[ I_{DD} = -(\frac{1}{2} \beta D) (V_{in} - V_{th} - \Delta V_{th} - V_{out})^2 \]

and equating the right hand sides leads to

\[ (V_{in} - V_{th} - \Delta V_{th}) = -(\beta R)^{-1/2} \left(2(V_{DD} - V_{th})V_{out} - V_{out}^2\right)^{1/2} + V_{out} \]
where
\[ \beta_R = \beta_D / \beta_L \]

Eq. (20) is valid until either \( Q_D \) enters the linear region or \( Q_L \) becomes a saturated device. \( Q_D \) becomes a linear device when
\[ (V_{in} - V_{th} - \Delta V_{th} - V_{out}) = (V_{DD} - V_{out}) \]

The turnover point for \( Q_L \) is when \( V_{DD} - V_{th} = V_{out} \). The input-output relationships can be expressed for each case by the following two equations:

For \( Q_D \) and \( Q_L \) both in linear region

\[ (V_{in} - V_{th}) = \frac{2(V_{DD} - V_{th})V_{out} - V_{out}^2}{2R(V_{DD} - V_{out})} + \frac{1}{2}(V_{DD} + V_{out} + 2\Delta V_{th}) \]

(21)

For \( Q_D \) and \( Q_L \) both in saturation

\[ (V_{in} - V_{th}) = \frac{1}{\sqrt{R}} (V_{DD} - V_{th}) + V_{out} + \Delta V_{th} \]

(22)

In order to determine which one of these equations is applicable first, one must substitute \( V_{out} = V_{DD} - V_{th} \) in Eq. (22). The result is

\[ V_{in} - V_{th} - \Delta V_{th} = (V_{DD} - V_{th})(1 + 1/\sqrt{R}) \]

(23)

Comparison of Eq. (23) with \( V_{in} - V_{th} - \Delta V_{th} = V_{DD} \) leads to a condition on \( \beta_R \), i.e., for \( \beta_R < (V_{DD}/V_{th} - 1)^2 \) the driver device becomes linear before \( Q_L \) enters saturation so Eq. (21) holds in the intermediate region; and for \( \beta_R > (V_{DD}/V_{th} - 1)^2 \) Eq. (22) holds in the transition region. The case when \( \beta_R = (V_{DD}/V_{th} - 1)^2 \) is trivial as Eqs. (21) and (22) become identical. Beyond the intermediate region the driver device operates in the linear region while the load device is in the saturation region. Hence
\[ I_{DD} = -\beta_D \left( (V_{in} - V_{th} - \Delta V_{th} - V_{out}) - (V_{DD} - V_{out} / 2) (V_{DD} - V_{out}) \right) \]

\[ I_{DL} = -\left( \beta_L / 2 \right) (V_{DD} - V_{th})^2 \]

so

\[ (V_{in} - V_{th}) = \frac{1}{2} \left( \frac{1}{\beta_R} \frac{(V_{DD} - V_{th})^2}{V_{DD} - V_{out}} + V_{DD} + V_{out} + 2 \Delta V_{th} \right) \] (24)

**Gate of Resistor Device Connected to the Input**

Again since \( V_{in} = 0 \) gives \( V_{out} = 0 \), \( Q_D \) begins in the saturation region and its turnover point is reached when \( V_{in} - V_{th} - \Delta V_{th} = V_{DD} \).

As in the previous case, \( Q_L \) initially operates in the linear region, but since \( V_{GG} = V_{in} \) and \( |V_{in} - V_{th}| > |V_{out}| \) at all times, \( Q_L \) always remains in this region. The input-output relationships are

\[ V_{in} - V_{th} = \{ \Delta V_{th} + V_{out} (1 + 1/\beta_R) \} \]

\[ - \frac{1}{2} (1/\beta_R)^{\frac{1}{2}} \{ \Delta V_{th} + V_{out} (1 + 1/\beta_R) \} \frac{1}{2} V_{out}^2 \]

\[ |V_{in} - V_{th} - \Delta V_{th}| \leq |V_{DD}| \] (25)

\[ V_{in} - V_{th} = \frac{V_{DD}^2 + 2 \Delta V_{th} (V_{DD} - V_{out}) - V_{out}^2 (1 + 1/\beta_R)}{2 (V_{DD} - V_{out}) (1 + 1/\beta_R)} \]

\[ |V_{in} - V_{th} - \Delta V_{th}| > |V_{DD}| \] (26)

**Gate of Resistor Device Returned to the Output**

In this case, when \( |V_{out}| \geq |V_{th}| \), \( Q_L \), the load device will operate in the saturation region. For \( |V_{out}| < |V_{th}| \), \( Q_L \) is "off" and \( V_{out} = V_{in} - V_{th} - \Delta V_{th} \). \( Q_D \) begins in the saturation region and goes into the linear region when \( |V_{in} - V_{th} - \Delta V_{th}| \) becomes greater than \( |V_{DD}| \).

Equating the currents in the two devices yields
\[ V_{in} - V_{th} - \Delta V_{th} - V_{out} = (1/\beta_R)^{1/2} (V_{out} - V_{th}) \quad |V_{out}| > |V_{th}| \text{ and} \]

\[ |V_{in} - V_{th} - \Delta V_{th}| \leq |V_{th}| \]

and

\[
\{(V_{in} - V_{th} - \Delta V_{th} - V_{out}) - \frac{1}{2}(V_{DD} - V_{out})\} (V_{DD} - V_{out})
\]

\[ = \frac{1}{2}(1/(2\beta_R)) (V_{out} - V_{th})^2 \quad |V_{in} - V_{th} - \Delta V_{th}| > |V_{DD}| \]

Upon doing some algebraic rearrangement,

\[
V_{in} - V_{th} = V_{out} (1 + 1/\sqrt{R}) - V_{th}/\sqrt{R} + \Delta V_{th} \quad |V_{out}| > |V_{th}| \text{ and} \]

\[ |V_{in} - V_{th} - \Delta V_{th}| \leq |V_{DD}| \]

\[ \text{(27)} \]

and

\[
V_{in} - V_{th} = \frac{1}{2} (1/\beta_R) \left( \frac{V_{out} - V_{th}}{V_{DD} - V_{out}} \right)^2 + (V_{DD} + V_{out} + 2\Delta V_{th}) \quad |V_{in} - V_{th} - \Delta V_{th}| > |V_{DD}| \]

\[ \text{(28)} \]

**Gate Bias of Resistor Device Applied Externally**

In this case any of the previous cases may be encountered and no additional relationships are necessary. In general the bias will be larger than \( V_{DD} \) so that the load device always remains in the linear region and the situation will be similar to the second of the above mentioned cases. Thus Eqs. (25) and (26) will apply with some modification.
Figure 8. Schematic diagram of the MOS IC source follower configuration. (p-channel devices)

Figure 9. Input-output relationship for the source follower of Figure 8.
  a) \( V_{GG} = V_{DD} \)
Figure 9. (continued)
b) $V_{GG} = V_{in}$

c) $V_{GG} = V_{out}$
III. RC OSCILLATORS

General Considerations

The choice of the RC-network to be used in the feedback loop of an amplifier to produce an oscillator depends on several requirements. Stability, spectral bandwidth and frequency selectivity are the main considerations (1, 9, 12). In discrete systems one can choose the best circuit which fits the economical and physical specifications as well as the requirements mentioned above. In an integrated form, however, one is faced with realizability. The phase-shift RC-network was the choice that for the desired frequency range best fit this latter constraint. Thus, in spite of the superiority of other networks such as wien-bridge or bridged-T, the phase-shift scheme was chosen.

Phase-Shift Scheme

The two forms of phase-shift networks shown in Figure 10 are the most common configurations of RC-networks.

Series Capacitance

The circuit of the form shown in Figure 10a is more conventionally used because the capacitors allow dc isolation of input and output. When used as the feedback network of an inverting amplifier, this circuit will provide an extra 180° of phase shift at \( f_{sc} = \frac{1}{2\pi \sqrt{C} R} \) (4, 8, 14). If the magnitude of voltage gain of the amplifier is 29 or greater, the network loss will be covered and oscillations will build up.
Figure 10. Two simple 3-stage RC phase-shift networks.

a) Series capacitance (SC)

b) Series resistance (SR)
Series Resistance

The second form, in Figure 10b, introduces 180° phase shift at

\[ f_{sr} = \frac{6}{2\pi\sqrt{6}} \frac{1}{RC} \]  

(29)

The required gain of an inverting amplifier to produce oscillation is again 29. This latter circuit also allows dc feedback and since for an inverting amplifier the dc feedback will be negative, the biasing of the input stage can be accomplished by incorporating proper circuit design in the amplifier system. It was for this reason and also because of excessive size of the required series capacitors that this configuration was chosen and will be discussed further.

Stability and Tuneability

The change of frequency as a function of circuit parameters is a measure of tuneability. We have

\[ f_{sr} = \frac{\sqrt{6}}{2\pi} \frac{1}{RC} \]

so

\[ \frac{df}{f_{sr}} = \frac{\sqrt{6}}{2\pi} \left\{ \frac{\partial}{\partial R} \left( \frac{1}{RC} \right) dR + \frac{\partial}{\partial C} \left( \frac{1}{RC} \right) dC \right\} = \frac{\sqrt{6}}{2\pi} \left( \frac{1}{RC} \right) \left\{ -\left( \frac{dR}{R} + \frac{dC}{C} \right) \right\} \]

or

\[ \frac{df}{f} = -\left( \frac{dR}{R} + \frac{dC}{C} \right) \]  

(30)

Thus a relative change of R or C will be directly reflected in the frequency, while the direction of change of frequency is opposite that of the parameters. Eq. (30) also implies that the frequency stability as a function of R and C is the same as the component stabilities.
IV. MOS RC OSCILLATOR

Basic Building Blocks

The basic building blocks of an RC oscillator are 1) an amplifier and 2) a phase-shift RC-network. As mentioned in Chapter III, the three-stage RC-network with series resistors requires an inverting amplifier with a voltage gain of 29.

Amplifier

The MOS single stage amplifier was described in Chapter II in detail, so only a general schematic diagram of the three-stage amplifier will be reproduced at this point. Complete design calculations are presented in the next chapter.

The RC Network

The RC network consists of three MOS capacitors and three MOS resistors. At the low frequency ranges of interest, the values of resistors and capacitors are rather large. At 1000 Hz, using
\[ f_{sr} = \frac{1}{2\pi RC} \]
gives
\[ RC \approx 389 \mu \text{sec} \]

Capacitors

For an oxide layer of 1500 \( \text{Å} \) the capacitance per unit area is 0.152 pf/mil\(^2\). If a reasonable value is chosen for R, say 389K\( \Omega \), then
Figure 11. Block diagram of the MOS IC phase-shift oscillator.

Figure 12. Schematic diagram of the MOS IC 3-stage amplifier. The dc feedback shown is through the series resistance of the RC feedback network.
C = 1000 pf and the required area is nearly 6600 mil$^2$, or a square nearly 26 mils on each side! This is clearly prohibitive. The remedy was found in using the Miller effect which is described below.

**Miller Multiplier**

Consider the circuit shown in Figure 13. The input impedance is given by

\[ Z_{\text{in}}' = \frac{V_i}{I_i} = \frac{V_i}{I_i + I_f} \]

or

\[ Z_{\text{in}}' = \frac{V_i}{(\frac{V_i}{Z_i}) + \frac{(V_i - V_f)}{(Z_f)} \alpha} \]  \hspace{1cm} (31)

but

\[ V_o = -A \frac{V_i}{\alpha} \]

so

\[ Z_{\text{in}}' = \left\{ \frac{1}{Z_i} + \frac{A \alpha + 1}{Z_f} \right\}^{-1} \]  \hspace{1cm} (32)

Now if \( Z_i >> Z_f \),

\[ Z_{\text{in}}' = \frac{Z_f}{A \alpha + 1} \]  \hspace{1cm} (33)

and for

\[ Z_f = \frac{1}{j\omega C_f}, \quad Z_{\text{in}}' = \frac{1}{j\omega (A \alpha + 1) C_f} \]

the input capacitance of the circuit appears \((1 + A)\) times the feedback capacitance. With \( A = 29 \) and \( C_f = 33 \) pf, \( C_i = 1000 \) pf and the required area for \( C_f \) is only 220 mil$^2$ or a 20 x 11 mil$^2$ pad. This is reasonable although still large. The reason for choosing \( A = 29 \) is to allow the use of the same amplifier for both Miller multiplication and feedback loss compensation.
Figure 13. Schematic diagram of the Miller multiplier arrangement showing the parameters which are used in the text to calculate the input impedance of the circuit.
Resistors

The series resistors can be MOSFET's in the triode region where
as explained in Chapter II, the resistance value is given by

\[ R = \frac{1}{g_m} = (1/\beta)(V_G - V_{th} - \Delta V_{th} - V_{SB})^{-1} \]

Since the dc current through these resistors is extremely small, the
voltage drop across them will be essentially negligible and \( V_{DS} = 0 \).
The dc component of \( V_{SB} \) will then be the dc output voltage of the last
amplifier and will be constant. With small ac voltages at the output
the ac component of \( V_{SB} \) can also be ignored compared to \( (V_{th} + V_{SB})_{DC} \).
Thus \( \Delta V_{th} \) will be essentially a constant; and the result is

\[ R = (1/\beta)(V_G - V_B)^{-1} \]

where

\[ V_B = V_{th} + \Delta V_{th} + V_{SB} \approx \text{constant} \]

Now since \( \beta \) is equal to \( \frac{\mu C_{ox} W}{t_{ox} L} \) and is a constant of the device, the
variation of \( R \) with gate voltage is a simple hyperbolic relation.

Tuning Equation

Reference to the frequency-components relationship for the RC
oscillator yields

\[ f = \frac{\sqrt{\beta(V_G - V_B)}}{2\pi (1 + A)C_f} = \alpha(V_G - V_B) \] (34)

where

\[ \alpha = \frac{\sqrt{\mu C_{ox} W}}{2\pi (A_V + 1)C_f \frac{1}{L}} \]
This relationship is linear over a wide range of frequencies and voltages. Thus the oscillator is easily tuned by varying the gate bias of MOS transistors which act as coupling resistors in the phase-shift network.

Another feature of the device is that it can be frequency stabilized by using a simple frequency to voltage converter the output of which will provide the gate bias for the coupling MOSFET's.

Amplitude of oscillations can also be stabilized if one uses dual-gate MOSFET's in at least one of the amplifier stages and establishes the bias on the second gate through an AC/DC converter the input of which is the oscillator output.
V. DESIGN OF THE INTEGRATED CIRCUIT

Design Parameters

The following parameters were used in the design of the integrated circuit:

- \( \varepsilon_{\text{ox}} \) is the permittivity of SiO\(_2\) = 4.0 \( \varepsilon_0 \) farad/m
- \( t_{\text{ox}} \) is the gate oxide thickness = 1500 \( \text{Å} \)
- \( \mu_p \) is the mobility of holes in the channel = 200 cm\(^2\)/volt-sec
- \( V_{\text{th}} \) is the threshold voltage = -4.0 volts

From these, two of the design parameters can be calculated.

\( C_0 \) is the gate capacitance per unit area

\[
C_0 = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} = 0.152 \text{ pf/mil}^2
\]

\( \beta \) is the material and geometry parameter of devices

\[
\beta = \mu_p C_0 \frac{W}{L} = (4.72 \times 10^{-6}) \frac{\text{W}}{L} \text{ mho/volt}
\]

where

- \( W \) is the channel width
- \( L \) is the channel length

Complete Oscillator Block Diagram

The integrated circuit consists of three amplifiers, three capacitors and three resistors in a circuit configuration as shown in Figure 14. The amplifiers are identical in design and will be described first. Since a dc feedback loop is provided, the first requirement is that \( V_{\text{out}} \) (quiescent) = \( V_{\text{in}} \) (quiescent). It is also
Figure 14. Complete block diagram of the MOS IC phase-shift oscillator employing Miller capacitance multipliers, MOS capacitors and resistors. In addition to the main output, there are two other outputs available at Aux1 and Aux2. These are 120° and 240° out of phase with respect to the main output, respectively.

Figure 15. Designation of devices for the design of the 3-stage MOS IC amplifier.
required that $|A_v| = 30$, $|V_{DD}| = 15$ volts. For stable feedback, the amplifier must be inverting; so to obtain the desired gain, three stages are necessary, i.e., $A_v = -30$. With p-channel devices on n-type starting material the bias supply will be $V_{DD} = -15$ volts.

**Design of Three-Stage Amplifier**

The three input-output relationships for the stages are, in the linear amplification region:

$$V_{out_i} = -\beta_{R_i} \frac{1}{2} (V_{in_i}) + V_{DD} - (1-\sqrt{\beta_{R_i}}) V_{th} - \Delta V_{th_i}, \quad i = 1, 2, 3$$  \hspace{1cm} (35)

Also,

$$V_{out_1} = V_{in_2}$$  \hspace{1cm} (36a)

$$V_{out_2} = V_{in_3}$$  \hspace{1cm} (36b)

$$V_{out_{3dc}} = V_{in_{1dc}}$$  \hspace{1cm} (36c)

$$A_v = -(\beta_{R_1} \beta_{R_2} \beta_{R_3})^{\frac{1}{2}} = -30$$  \hspace{1cm} (37)

Since $\Delta V_{th_1}$ is determined after knowing $V_{out_1}$, the design is easiest if the last stage is considered first. By arbitrarily choosing $\beta_{R_3} = 9$, reference to the graph of Figure 6 shows that for such a stage an output quiescent voltage of -6 volts biases this stage in the middle of its linear range of operation. Substituting $V_{out} = -6$ volts, $V_{th} = -4$ volts, $V_{DD} = -15$ volts, $\sqrt{\beta_{R_3}} = 3$, $\Delta V_{th} (-6v) = -1.6$ volts (determined from Figure 4) leads to

$$V_{in_3} = -5.13 \text{ volts}$$

Now since $V_{in_3} = V_{out_3}$, $\Delta V_{th_2}$ can be determined. Thus $\Delta V_{th_2} = -1.4$ volts
and one obtains

\[ V_{in_2} + 4 = \beta_{R_2}^{-\frac{1}{2}} (-15 + 4 + 1.4 + 5.13) \]  
(38)

\[ V_{in_1} + 4 = \beta_{R_1}^{-\frac{1}{2}} (-15 + 4 - \Delta V_{th_1} - V_{in_2}) \]  
(39)

But

\[ V_{in_{1dc}} = V_{out_{3dc}} = -6 \text{ volts} \]  
(40a)

\[ \beta_{R_1}^\frac{1}{2} \beta_{R_2}^\frac{1}{2} = 10 \]  
(40b)

So \( V_{in_2} \) and \( \beta_{R_2}^\frac{1}{2} \) can be eliminated from the above equations. Rearranging Eq. (38) and using Eq. (40b) yields

\[ V_{in_2} = -4 - 0.45 \beta_{R_1}^\frac{1}{2} \]  
(41)

Substituting this and Eq. (40a) in Eq. (39) leads to

\[ -2 = \beta_{R_1}^{-\frac{1}{2}} (-11 - \Delta V_{th_1} + 4 + 0.45 \beta_{R_1}^\frac{1}{2}) \]

or

\[ 2.45 \beta_{R_1}^\frac{1}{2} = 7 + \Delta V_{th_1} \]  
(42)

Re-substituting this result in Eq. (41) yields

\[ V_{out_1} = V_{in_2} = -4 - 0.45 \left( \frac{7 + \Delta V_{th_1}}{2.45} \right) \]

or

\[ V_{out_1} = -5.29 - 0.184 \Delta V_{th_1} \]  
(43)

From Figure 4, \( V_{out_1} = -5.1 \text{ volts} \) implies \( \Delta V_{th_1} = -1.4 \text{ volts} \) and no further iteration is necessary as these values satisfy Eq. (43). The immediate results at this point are
Now that operating voltages and $\beta_R$ ratios are known, the choice of operating currents will result in actual physical sizes of devices. Since

$$\beta_R = \beta_D/\beta_L = \left(\frac{\mu_{e ox} W}{L}\right)_D / \left(\frac{\mu_{e ox} W}{L}\right)_L$$

and normally

$$t_{ox D} = t_{ox L},$$

the result is

$$\beta_R = (W/L)_D / (W/L)_L$$

Thus

$$\frac{(W/L) Q_{1D}}{(W/L) Q_{1L}} = (2.22)^2 = 5$$

$$\frac{(W/L) Q_{2D}}{(W/L) Q_{2L}} = (4.5)^2 = 20$$

$$\frac{(W/L) Q_{3D}}{(W/L) Q_{3L}} = (3)^2 = 9$$

The quiescent output voltage of $Q_{3D}$ was chosen to be -6 volts; an 500\textmu a quiescent current is selected to give

$$R_{Q_3} = \frac{(V/I)_{\text{quiescent}}}{-500\text{\mu a}} = 12\text{K}\Omega$$
Since $Q_{3D}$ operates in the saturation region,
\[ R_{Q_{3D}} = \frac{2}{g_m}Q_{3D} = -2\{β(V_G - V_{th})\}^{-1} \]
or
\[ (W/L)_{Q_{3D}} = -2\{(4.72 \times 10^{-6})(-5.13 + 4)(12K\Omega)\}^{-1} \]
Thus
\[ (W/L)_{Q_{3D}} = 36, \quad (W/L)_{Q_{3L}} = \frac{36}{9} = 4 \]

For the second stage a current of 250\(μ\)a was selected. The transconductance of $Q_{2L}$ is then
\[ (g_m)_{Q_{2L}} = \frac{2}{R}Q_{2L} = 50 \, μa/volt \]
and
\[ (W/L)_{Q_{2L}} = 50\{(4.72 \times 10^{-6})(-15 + 4 + 1.4 + 5.13)\}^{-1} = 2.36 \]
so
\[ (W/L)_{Q_{2D}} = (20)(2.36) = 4.72 \]
Similarly for the first stage $I_D = -200\, μa$ gives
\[ (W/L)_{Q_{1L}} = 2 \]
\[ (W/L)_{Q_{1D}} = (2)(5) = 10 \]

In order to control the gain of the amplifier a source degeneration resistor device was introduced in the first stage. The $(W/L)$ ratio chosen for this device was 70 and the $(W/L)_{Q_{1D}} / (W/L)_{Q_{1L}}$ ratio was raised to 6 so as to allow for more available gain.
In the actual device the p-type impurities which are diffused into the substrate to form the source and drain areas will also diffuse sideways. For a one micron diffusion depth, the channel length will be reduced by approximately two microns. With this fact in mind, the mask openings must be designed larger in length by two microns. The final (W/L) ratios are given in Table 1.

Design of Capacitors

The capacitors of the phase-shift network are 30pf each. Hence the area required can be obtained

\[
(30\text{pf})/(0.152\text{pf/mil}^2) = 200 \text{ mil}^2
\]

The effective capacitance will then be \((30\text{pf})(A + 1)\) where \(A\) is the gain of amplifiers \(\approx -30\). Thus \(C_{\text{eff}} = 930\text{pf}\).

Design of Resistors

For \(f_o = 1000 \text{ Hz}\),

\[
R = \frac{\sqrt{R}}{2\pi} \frac{1}{(10^3) (930 \times 10^{-12})}
\]

\(= 420 \text{ K\Omega}\)

This resistance consists of an MOS transistor and with its source-drain voltage very small, it is then operating in the linear region and

\[
R = 1/g_m
\]

or

\[
g_m = 1/R
\]

and

\[
(W/L) = \{(-4.72 \times 10^{-6})(V_G - V_{th} - \Delta V_{th} - V_D) R_L\}^{-1}
\]
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<td>Q4</td>
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<td>0.4 2.8</td>
<td></td>
<td>0.16 1.14</td>
</tr>
<tr>
<td>Capacitors</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>-</td>
<td>10 20</td>
<td>30 pf, 4 8</td>
<td>200 mil²</td>
</tr>
</tbody>
</table>
With \( V_D = -6 \text{v}, V_{th} = -4 \text{v}, \Delta V_{th} = -1.6 \text{ volts} \),

\[
(W/L) = \left\{ -4.72 \times 10^{-6} (420 \times 10^3) (V_G + 11.6) \right\}^{-1}
\]

Choosing \( V_G = -15 \) volts results in

\[
(W/L) = 0.148
\]

In selecting the physical size for each device the minimum dimension was taken to be 0.4 mil so as to facilitate mask cutting and also to reduce registration problems.

**Physical Layout**

Figures 16 and 17 show the mask layout of the three-stage amplifier and the entire oscillator, respectively. Note that in the latter case the two amplifiers which function mainly as capacitance multipliers do not include the gain control device in the source of the first stage.
Figure 16. Physical layout of the 3-stage MOS IC amplifier. Heavy lines (--) enclose diffused areas, [ ] indicates gate areas, [ ] indicates contact hole areas, thin lines (--) enclose metallized areas. Drawing scale: 400x.
Figure 17. Photomicrograph of the complete MOS IC oscillator.

a) Amplifiers, capacitors and resistors all electrically isolated to allow individual device testing and evaluation.

b) All interconnections made by an extra metallization step (mask #5).
VI. EXPERIMENTAL RESULTS AND DISCUSSION

Characteristics of Transistors

The characteristics of a typical device fabricated on a 3-5 Ω-cm, N-type, <100>-cut substrate is shown in Figure 18a. The extrapolated threshold voltage from $-\frac{V_T}{D}$ versus $V_G$ data for this device is $V_{th} = -3.8$ volts, which agrees with the assumption of $V_{th} = -4$ volts within five percent.

Characteristics of Resistors

Figure 18b is the photograph of the V-I characteristics of a typical resistor device as seen on a Fairchild model 6200-B curve-tracer. This device comprises one of the three resistors in the RC feedback network. The slope at the origin for a gate voltage of -10 volts is ~3.0 µa/volt, implying an effective resistance of 330kΩ. Since in the actual IC there is a bias voltage on the source, the effective gate bias will be less than -10 volts. For example, with a -6 volt back bias the effective bias with $V_G = -15$ volts would be \{-15 - (-6) - (-1.6)\} = -7.4. The device at this gate voltage represents a resistor the value of which is in excess of 500 KΩ!

Characteristics of Amplifiers

The amplifiers typically had a gain of 35-40 and the input and output waveforms of one such amplifier are shown in Figures 19a and 19b.
Figure 18. V-I characteristics of typical fabricated devices.
a) MOS transistor device ($W/L = 70$)
   - Vertical scale: 1 ma/major division
   - Horizontal scale: 2 volts/major division
   - Gate voltage steps: 1 volt/step, last step = 10 volts
b) MOS resistor device ($W/L = 0.144$)
   - Vertical scale: 10 μa/major division
   - Horizontal scale: 1 volt/major division
   - Gate voltage steps: 2.5 volts/step, last step = 25 volts
Figure 19. Input and output waveforms of a fabricated 3-stage MOS IC amplifier
a) Sine-wave response at 1 KHz
   input, upper trace, 50 mv/major division vertical scale
   output, lower trace, 0.5 v/major division vertical scale. Horizontal scale 0.5 msec/major division
b) Square-wave response at 1 KHz
   input, upper trace; output, lower trace. Vertical scales as in (a), horizontal scale 0.2 msec/major div.
Total Performance of Oscillator

The oscillator unit operated in a wide frequency range. The waveforms at the output terminals of the three amplifiers are shown in Figure 20 for three output frequencies. It was necessary to introduce a 270 millivolt dc bias in series with the input to the main amplifier so that the devices would be properly biased. This is attributed to many design and production variables. In particular, the solution to the three simultaneous equations for the amplifier stages was determined here by trial and error. The use of a digital computer in this connection would allow the tabulation of parameters so that the best and most accurate choice would be readily evident.

Data

The variation of frequency with control voltage appears in Figure 21, while frequency versus temperature data are shown in Figure 22. Effect of supply variation and harmonic content of the output follow in Figures 23 and 24.

Discussion

The slope of the curve in the frequency-gate voltage data is quite linear from 100 Hz to 2,000 Hz and its value is -500 Hz/volt. Comparison to the expected value of -440 Hz/volt shows good agreement. The twelve percent difference can be accounted for by the possibility that the gate oxide is thinner than 1500 Å and/or amplifier gains are larger than 40. Above 2000 Hz the slope decreases continuously and at
Figure 20. Output waveform of the MOS IC phase-shift oscillator at three different frequencies.

a) $f = 100$ Hz

- $V_{cf} = -12$ volts, $V_{DD} = -15$ volts at 3.4 mA
- Upper trace output of A3, 5 volts/major vert. division
- Middle trace output of A1, 1 volt/major vert. division
- Bottom trace output of A2, 2 volts/major vert. division
- Horizontal scale 5 msec/major division
Figure 20. (continued)

b) $f = 1 \text{ KHz}$
$V_{cf} = -13.9 \text{ volts}$
same vertical scales and trace descriptions as in (a)
horizontal scale 0.5 msec/major division

(c) $f = 8 \text{ KHz}$
$V_{cf} = -39 \text{ volts}$
same vertical scales and trace descriptions as in (a) and (b); horizontal scale 50 µsec/major division
the upper limit (8850 Hz) it is -157 Hz/volt. This is due to decreased mobility of holes in the channel (2, p.65-69, 7). The straight line behavior suggests that a simple scheme of frequency stabilization can be employed. Such a device was fabricated and tested. Although it was not compatible with the oscillator, it proved feasible. Appendix B includes design and performance data of the frequency to voltage converter.
Figure 21. Tuning curves of the MOS IC phase-shift oscillator showing
a) Full range of operation
b) Region covering ±100% of the design center frequency
Figure 22. Variation of frequency as a function of the temperature of the TO-5 package containing the MOS IC PSO.

\[ \Delta f = f - f_0 \]
\[ f_0 = 1 \text{ KHz} \]

slope \(-3.15\) Hz/°C

Figure 23. Variation of frequency as a function of the supply voltage variations for the MOS IC PSO.

\[ \Delta V_{DD} = V_{DD} - (V_{DD})_0 \]
\[ (V_{DD})_0 = -15 \text{ volts} \]
Figure 24. Harmonic content of the output of the MOS IC PSO. 0 dB reference point chosen as the tenth harmonic magnitude (about 300 μvolt rms). Output level at the fundamental frequency (1 KHz) = 630 mV rms.
VII. CONCLUSION

The use of linear MOS integrated circuits was investigated by fabricating an all-MOS low frequency oscillator which included amplifiers, resistors and capacitors. The oscillator was voltage tuneable over a wide frequency range (100-8000 Hz) and exhibited very linear frequency-voltage relationship over the range extending from 100Hz to 2000 Hz, which included the design specification. Thus it was established that MOS linear circuits promise more than just discrete MOS elements, and MOS integrated circuits when properly designed can replace their discrete or bipolar counterparts in many applications.

Audio oscillators, amplitude calibrators in oscilloscopes, and signal generators are only a few of the cases in which an MOS oscillator with its frequency stabilization could be readily used.
BIBLIOGRAPHY


APPENDIX A

Determination of Frequency of Oscillation
in a Phase-Shift Oscillator

The system is shown in Figure A1. The feedback network consists of a three-stage RC circuit as shown. The simplest case will be discussed here. The output impedance of the amplifier is assumed small and resistive and included in $R_1$, while the input impedance is assumed to be very large and its capacitive component (if any) is included in $C_3$. The nodal equations in the complex domain are

$$\frac{(V_1 - V_{in})}{R_1} + \frac{V_1}{(1/sC_1)} + \frac{(V_1 - V_2)}{R_2} = 0$$
$$\frac{(V_2 - V_1)}{R_2} + \frac{V_2}{(1/sC_2)} + \frac{(V_2 - V_{out})}{R_3} = 0$$
$$\frac{(V_{out} - V_2)}{R_3} + \frac{V_{out}}{(1/sC_3)} = 0$$

Let

$$R_1 = R_2 = R_3 = R$$
$$C_1 = C_2 = C_3 = C$$

then rearranging terms yields

$$\begin{pmatrix}
(2 + RCs)V_1 & -V_2 & +0 & = V_{in} \\
-V_1 & +(2 + RCs)V_2 & -V_{out} & = 0 \\
0 & -V_2 & +(1 + RCs)V_{out} & = 0
\end{pmatrix}$$

or
Figure A1. RC phase-shift oscillator and the feedback network.

a) oscillator block diagram
b) series resistance, RC phase-shift feedback network
\[
\begin{bmatrix}
(2 + RCs) & -1 & 0 \\
-1 & (2 + RCs) & -1 \\
0 & -1 & (1 + RCs)
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_{out}
\end{bmatrix}
= \begin{bmatrix}
V_{in} \\
0 \\
0
\end{bmatrix}
\]

Solving for \( V_{out} \) by Cramer's rule gives

\[
V_{out} = \frac{V_{in} \{(-1)(-1) + 0 \}}{(2 + RCs) \begin{vmatrix} 2+RCs & -1 \\ -1 & 1+RCs \end{vmatrix} + \begin{vmatrix} -1 & -1 \\ 0 & 1+RCs \end{vmatrix}}
\]

or

\[
T(s) = \frac{V_{out}}{V_{in}} = \frac{1}{(RCs)^3 + 5(RCs)^2 + 6(RCs) + 1}
\]

Substituting \( j\omega \) for \( s \) gives the frequency domain transfer function, that is,

\[
T(s=j\omega) = \left(1 -5(RC)^2 -j\omega(RC)((RC\omega)^2-6)\right)^{-1}
\]

and for a real transfer function the imaginary part must vanish. Thus

\[
j\omega RC \{(RC\omega)^2-6\} = 0
\]

or

\[
\omega = \{0 \text{ or } \sqrt{6}/(RC) \}
\]

At dc the transfer function is equal to unity, since the capacitors have no effect. The frequency at which the input and output are \( \pi \) out of phase is

\[
f_o = (\sqrt{6}/2\pi)(RC)^{-1}
\]

The value of the transfer function at this frequency is
\[ T(j\omega) = \left(1 - 5(\text{RC}\omega)^2\right)^{-1} \]

\[ = \left(1 - 5(\text{RC} \cdot \sqrt{6}/\text{RC})^2\right)^{-1} = -(1/29) \]

Thus the amplifier must provide a gain of 29 and a phase shift of π, i.e., an inverting amplifier is needed. More complicated cases are discussed in the literature (4, 14).
APPENDIX B

Frequency Stabilization System

Since the frequency-voltage curve of the MOS oscillator has a linear slope of \(-500 \text{ Hz/volt}\), if the frequency is detected and converted to a dc voltage such that the voltage-frequency relationship of the converter device is \(2 \text{ mv/Hz}\), and if this device provides the frequency tuning voltage, then the stable operating point of the system would be the intersection of the two curves as schematically indicated in Figure B1.

The technique of frequency to voltage conversion used here was the simple method frequently used in pulse circuits. The oscillator output triggers a one-shot circuit. With a constant pulse width, the zero level of the output pulse with respect to the top or bottom of the pulse reflects the repetition rate. Quantitatively, since the zero level is at a position such that the areas under the waveform above and below this level are equal, one arrives at

\[
\text{zero level with respect to the bottom} = \frac{A\tau}{T} = A\tau f
\]

(of a positive pulse)

where

- \(A\) is the amplitude of the pulse
- \(\tau\) is the pulse width

\(T = 1/f = \text{time period of the waveform}\)

Thus

\[
\frac{d}{df} \text{(zero level)} = A\tau
\]

and the slope can be easily adjusted by changing \(A\) or \(\tau\) or both.
Figure B1. Frequency stabilization of a voltage tuneable oscillator.
   a) system block diagram
   b) tuning and control curves
Figure B2. Definition of the parameters of a periodic pulse train.

Figure B3. Schematic diagram of the frequency to voltage converter.
The circuit of Figure B3 is next considered. The ac to dc converter section consists of two amplification stages for wave-shaping and output level adjusting. The use of an MOS device (Q15) permits the detection of the peak value of the voltage. Since the drain of Q15 is connected to its gate, the output voltage at the source is \((V_D - V_{th} - \Delta V_{th})\). Once the capacitor \(C_4\) is charged up to this voltage, the device acts like an open circuit and no current will flow through it until the charge on \(C_4\) becomes dissipated through a load or by leakage. The capacitor \(C_3\) ac couples the ac/dc converter input to the one-shot output. Thus only voltage excursions beyond the threshold voltage will result in operation of the input amplifier stage.

The one-shot section produces a pulse of constant width with the period of the input voltage. Normally Q2 is "off", Q8 is "on" so that Q4 is "off" and Q5 is also "off" thus biasing the gate of Q1. Input signals are coupled to the gate of Q2 through Q1. With an input excursion larger than the threshold voltage (-4 volts), Q2 turns "on". \(C_1\) is normally charged up to some value depending on the pulse-width controlling voltages. The gate voltage of Q8 is generally less than the drain voltage of Q2 in the "off" state. So when Q2 is turned "on" and its drain voltage becomes more positive, \(C_1\) transfers this change to the gate of Q8. Of course the gate bias cannot become greater than +0.6 volt at any case since the source-substrate junction of Q10 becomes forward biased. As soon as Q8 output becomes less than -4 volts Q4 turns "on" thus clamping the drain of Q2 at the "on" voltage. \(C_2\) begins to charge up and Q5 is turned "on", which causes Q1 to turn "off" and the input is disconnected from Q2. When \(C_1\) is charged sufficiently,
Q₈ turns "on" again and the circuit is reset to its starting point.

The circuit was designed on the basis of the following requirements:

- DC output of ac/dc converter = -11 volts at fₒ
- Slope of output as a function of frequency = 2 mV/Hz
- V_DD = -25 volts
- V_th = -4 volts
- fₒ = 1000 Hz

Since the input to the MOS peak detector is (V_outdc + V_th + ΔV_th),

the required peak output of the second amplifier stage is = -16.6 volts.

The input-output relationship for this amplifier stage is then

\[ V_{in2} - V_{th} = \beta R_2 \left( V_{DD} - V_{out2} - V_{th} - ΔV_{th2} \right) \]

or

\[ V_{in2} + 4 = -1.43 R_2 \]

A similar equation for the first amplifier stage gives

\[ V_{in1} + 4 = \beta R_1 \left( -25 + 4 - V_{out1} - ΔV_{th1} \right) \]

but

\[ V_{out1} = V_{in2} \]

also V_{in1} is the peak value of the negative excursion of the output of

one-shot, i.e.,

\[ V_{in1} = -A(1 - \tau f_o) \]

where
A is the peak-to-peak value of the output of one-shot

τ is the width of the pulse

fo is the pulse repetition rate

In addition, the slope of output voltage (versus frequency) is

\[ \frac{d}{df}(V_{out}) = \left\{ \frac{1}{\beta_{R1} \cdot \beta_{R2}} \right\}^{\frac{1}{2}} A\tau \approx 2 \text{ mv/Hz} \]

So the set of equations to be solved is

\[ V_{in1} + 4 = \beta_{R1}^{\frac{1}{2}} (-21 - V_{out1} - \Delta V_{th1}) \]

\[ V_{in2} + 4 = \beta_{R2}^{\frac{1}{2}} (-1.4) \]

\[ V_{in1} = -A(1 - \tau f_0) \]

\[ A\tau = (0.002)/(\beta_{R1} \cdot \beta_{R2})^{\frac{1}{2}} \]

Choose \( \beta_{R2} = 1 \), then \( V_{in2} = -5.4 \) volts = \( V_{out1} \), \( \Delta V_{th1} = -1.4 \) volts and the substitution in the set reduces it to

\[ V_{in1} = -4 - 14.2 \beta_{R1}^{\frac{1}{2}} \]

\[ V_{in1} = -A(1 - 1000\tau) \]

\[ A\tau = 0.002 \beta_{R1}^{\frac{1}{2}} \]

Eliminating \( V_{in1} \) and \( \beta_{R1}^{\frac{1}{2}} \) yields

\[ A = 4/(1 - 8100\tau) \]

A reasonable value for \( A \) is 8 volts, which leads to \( \tau = 61.7 \mu \text{sec} \).

Hence \( \beta_{R1}^{\frac{1}{2}} = 4.05 \), and \( V_{in1} = -7.52 \) volts, which gives -5.4 volts as the
output of the first stage. Thus the consistency of the calculation is verified.

For the one-shot circuit the output stage is to produce 8 volts peak-to-peak. Use of two saturated load devices limits the most negative output voltage to $\approx -11$ volts. The "on" voltage is chosen to be $-3$ volts, giving a total swing of 8 volts. It is easily seen by equating the currents in each load resistor device and the driver device that when the geometry of the two resistor devices is the same,

$$V_{\text{in}} - V_{\text{th}} = \beta_R \left\{ -V_{\text{DD}} - 2V_{\text{th}} - \Delta V_{\text{th1}} - \Delta V_{\text{th2}} - V_{\text{out}} \right\}/2$$

where

$$\beta_R = \beta_D/\beta_{L1} = \beta_D/\beta_{L2}$$

$\Delta V_{\text{th1}}$ is the threshold voltage change of the first load device

$\Delta V_{\text{th2}}$ is the threshold voltage change of the second load device

The ac gain is then $dV_{\text{out}}/dV_{\text{in}} = -2\sqrt{\beta_R}$. The complete input-output information is obtained with the help of another equation which determines $\Delta V_{\text{th1}}$. This equation is the result of equating the currents of the two load devices:

$$V_{\text{DD}} - 2V_{D2} + V_{\text{out}} - (\Delta V_{\text{th1}} - \Delta V_{\text{th2}}) = 0$$

where

$$V_{D2} = V_{G2} = \text{drain and gate voltage of the second load device}$$

A choice of $(W/L)_{Q8} = 9$, $(W/L)_{Q9} = (W/L)_{Q9'} = 2$ results in a gain of
-5.3 for this stage and with a -5.8 volt input, the output will be -3 volts. The input voltage is then properly set by adjusting the bias of Q10.

The input coupling device, Q1, has to charge up the gate capacitance of Q2. For a short time constant, \( \tau < 100 \\mu \text{sec} \), since \( \tau_s = \frac{C}{g_m} \), where C is the gate capacitance of Q2 and \( g_m \) is the transconductance of Q10, the value chosen for \( g_m \) must be large enough. If the highest limit on C is set at 4.0 pf, then a \( g_m = 50 \) \( \mu \)mho is sufficient for Q1. The gate bias of -17.5 volts on Q1 yields \( \frac{W}{L}Q1 = 2 \).

Transistors Q2 and Q4 are chosen identical. Then when the gate of Q4 is biased at -11 volts, the output of Q8, i.e., the "on" voltage at the drain must be at most -2.5 volts. Thus calculations give \( \sqrt{5} > 2.5 \). A reasonably good choice is \( \frac{W}{L}Q4 = \frac{W}{L}Q3 = 9 \), and with \( \frac{W}{L}Q3 = 1 \), \( \frac{W}{L}Q2 = \frac{W}{L}Q4 = 9 \). The output in this case will be -2.1 volts. Therefore, when Q4 is turned "on" at \( t = 0 \), the voltages at the terminals of C2 will be -2.1 volts and +0.6 volts (with respect to substrate) and C2 will begin to charge up through Q10.

If the gate of Q10 is connected to the \( V_{DD} \) supply, the device will operate in the linear region (unless the voltage applied to the drain is larger than \( V_{DD} - V_{th} \)). With respect to the drain of Q2, the voltage across the capacitor C1 is initially \( (0.6 + 2.1) = 2.7 \) volts and when the charging process is completed it will be \( (V_{pwd} + 2.1) \) volts. When \( V_{pwd} = -6 \) volts, the final voltage across C1 will be -3.9 volts while the final voltage at the gate of Q8 is -6 volts. Thus the resulting output of this stage is about -3 volts. The bias parameter for Q10 is

\[
\frac{V_{DD}}{V_{G} - V_{th} - \Delta V_{th}}
\]
and the time constant is

\[ \tau = \frac{C_1}{-Q_{10} (V_G - V_{th} - \Delta V_{th})} \]

Also the voltage across the capacitor, \( v(t) \), is described by

\[ \int_0^t \frac{dt}{\tau} = \int \frac{x(t)}{x_0} \frac{dy}{(m/2)y^2 - y + (1 - m/2)} \]

where

\[ x(t) = \frac{v(t)}{(V_{DD})_{eff}} , \quad x_0 = \frac{v(0)}{(V_{DD})_{eff}} \]

The result after integration and exponentiation of both sides is

\[ e^{-(1 - m)t/\tau} = \frac{(x - 1)(x_0 - 2/m + 1)}{(x_0 - 1)(x - 2/m + 1)} \]

Substitution of numerical values leads to

\[ m = \frac{-6 + 2.1}{-25 + 4 + 1.8} = 0.203 \]

\[ x_0 = \frac{2.7}{-3.9} = -0.693 \]

and for \( x(t) = 90\% x(\infty) \) at \( t = 60 \mu s \), \( x(60) = 0.9 \). Then

\[ e^{-(1 - 0.203)60/\tau} = \frac{(0.9 - 1)(-0.693 - 2/0.203 + 1)}{(-0.693 - 1)(0.9 - 2/0.203 + 1)} \]

or

\[ -47.8 \tau^{-1} = \ln(0.0718) \]

and finally \( \tau = 18.1 \mu s \). Substituting this in the expression for \( \tau \) and solving for \( (W/L)_{Q10} \), with \( C_1 = 30 \text{ pf} \), results in

\[ (W/L)_{Q10} = \left( \frac{C_1}{\tau} \right) \left( -4.72 \times 10^{-6} (V_G - V_{th} - \Delta V_{th}) \right)^{-1} = 0.0182 \]
The \((W/L)_{Q10}\) was chosen in the mask to be \(=(1/60)\) and the device was designed in two sections to allow for more flexibility and an added voltage drop if necessary.

The inverter stage consisting of \(Q_5\) and \(Q_6\) is required to provide a bias of less than \(-4\) volts on the gate of \(Q_1\) when \(Q_5\) is turned "on". So the gain for this stage may be chosen immediately. For a gain of 3, the \(W/L\) ratio for each transistor is conveniently selected as \((W/L)_{Q6}=1\), \((W/L)_{Q5}=9\). Thus the required input voltage for \(|V_{out}| \leq -4\) volts is found by using the appropriate values in

\[
V_{in} - V_{th} \leq \beta^{-1} (V_{DD} - V_{th} - \Delta V_{th} - V_{out})
\]

or

\[
V_{in} \leq -4 + \frac{1}{3} (-25 + 4 + 1.4 + 4)
\]

so

\[
V_{in} \leq -9.2 \text{ volts}
\]

The final value of \(V_{in}\) will be \(-11\) volts supplied through \(Q_7\), so for the calculations the 90% value of the maximum voltage may be used as the value which turns \(Q_1\) fully "off". \(Q_7\) operates in the linear region. Here the parameters are

\[
m = \frac{-11}{-25 + 4 + 2.5} = 0.595
\]

\[
x_0 = \frac{-3}{-11} = 0.272
\]

\[x(90\%) = 0.9\]
So for a 0.5 μsec delay

\[ -0.5(1 -0.595)\tau^{-1} = \ln \left( \frac{(0.9 -1)(0.272 -2/0.595 +1)}{(0.272 -1)(0.9 -2/0.595 +1)} \right) \]

or

\[ \tau = -0.203/\ln \left( \frac{0.209}{1.05} \right) = 0.126 \mu\text{sec} \]

and for \( C_2 = 1.5 \, \text{pf} \), the expression for \( \tau \) leads to

\[
\frac{(W/L)}{Q_7} = \frac{1.5 \, \text{pf}}{(0.126 \, \mu\text{sec})(-4.72 \times 10^{-6} \, \text{mho/volt})(-18.5 \, \text{volts})}
\]

\[ = 0.136 \]

The value for \( (W/L)_{Q_7} \) in the mask was selected as 0.12, thus assuring a 0.5 μsec delay in the turn-on time of \( Q_5 \). The turn-off is also delayed by about 0.4 μsec. The final design size parameters are summarized in Table B1. The physical layout is shown in figure B4 and the actual product appears in Figure B5.

The performance of the one-shot circuit is presented in Figure B6. (The input waveform was inverted at the oscilloscope.) The ac/dc converter section output is shown in Figure B7. A rather wide pulse was applied in this case. Hence the output voltage is larger than -11 volts and a larger \( V_{DD} \) is required to prevent the non-linear operation of the amplifiers. The slope of the output voltage versus frequency is nearly the desired one. The tested devices were from the only two primary fabrication runs. It is expected, however, that better devices would have been produced had the difficulties been eliminated. The results would have been more satisfactory in that case.
<table>
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<th>W/L</th>
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<th>Comments</th>
<th>Artwork dimensions in inches (400x)</th>
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<td>0.6 0.4</td>
<td></td>
<td>0.24 0.16</td>
</tr>
<tr>
<td>Q_10</td>
<td>1/30</td>
<td>0.25 7.5</td>
<td></td>
<td>0.1 3</td>
</tr>
<tr>
<td>Q_10'</td>
<td>1/30</td>
<td>0.25 7.5</td>
<td>one shot devices</td>
<td>0.1 3</td>
</tr>
<tr>
<td>Q_11</td>
<td>16.2</td>
<td>4.9 0.4</td>
<td></td>
<td>1.96 0.16</td>
</tr>
<tr>
<td>Q_12</td>
<td>1</td>
<td>0.3 0.4</td>
<td>to dc devices</td>
<td>0.12 0.16</td>
</tr>
<tr>
<td>Q_13</td>
<td>1</td>
<td>0.3 0.4</td>
<td>to dc devices</td>
<td>0.12 0.16</td>
</tr>
<tr>
<td>Q_14</td>
<td>1</td>
<td>0.3 0.4</td>
<td>to dc devices</td>
<td>0.12 0.16</td>
</tr>
<tr>
<td>Q_15</td>
<td>1</td>
<td>0.3 0.4</td>
<td>to dc devices</td>
<td>0.12 0.16</td>
</tr>
<tr>
<td>C_1-</td>
<td>10</td>
<td>20</td>
<td>30 pf, A = 200 mil^2</td>
<td>4     8</td>
</tr>
<tr>
<td>C_2-</td>
<td>1.5</td>
<td>7</td>
<td>1.5 pf, A = 10 mil^2</td>
<td>0.6    2.8</td>
</tr>
<tr>
<td>C_3-</td>
<td>8.3</td>
<td>8.3</td>
<td>10 pf, A = 70 mil^2</td>
<td>3.3    3.3</td>
</tr>
<tr>
<td>C_4-</td>
<td>6.2</td>
<td>11.5</td>
<td>10 pf, A = 70 mil^2</td>
<td>2.52    4.6</td>
</tr>
</tbody>
</table>
Figure B4. Physical layout of the frequency to voltage converter. Thick lines enclose diffused areas, thin lines enclose metallized areas, □ indicates gate areas, □ indicates contact holes.
Figure B5. Photomicrograph of the fabricated MOS IC frequency to voltage converter.

Figure B6. Input and output waveforms of the fabricated MOS IC one-shot. Top trace is the input at 5 v/major division vert. scale (input was inverted at the oscilloscope). Bottom trace is the output of the one-shot at 0.5 v/major division. The horizontal scale is 200 \( \mu \)sec/major division. \( V_{DD} = -25 \) volts at 340 \( \mu \)a, \( V_{pwd} = -7.3 \) volts.
$\Delta V_{out} = V_{out} + 9.3\ \text{volts}$

pulse width = 500 $\mu$sec

pulse height = 8 volts (negative going pulse)

$V_{DD} = -35\ \text{volts}$

Figure B7. Output of the fabricated MOS IC ac to dc converter as a function of the input frequency.
APPENDIX C

MOS Fabrication Process

Devices produced in the laboratory were fabricated by careful execution of a series of procedural steps. The following is a presentation of these steps in some detail:

1. Preliminary Cleaning

The starting material (N-type <100> silicon with ρ = 3-5(Ω-cm)) is cleaned in hot concentrated H₂SO₄, etched in buffered HF briefly and rinsed. Then it is cleaned in trichloroethylene, then acetone, and then de-ionized water in an ultrasonic tank. It is blown dry with nitrogen after the final rinse.

2. Thick Oxide Growth

A 6000-8500 Å thick layer of SiO₂ is thermally grown on the wafer in a furnace at 1100°C and in an atmosphere of wet oxygen (O₂ flowing over de-ionized H₂O at 95°C).

3. Photomasking I

A 1-2μ thick layer of photoresist (AZ-1350, positive) is applied on the oxide by high speed spinning of the wafer (2000 rpm). The resist is baked at 60°C in a vacuum oven for 10 minutes, then exposed to high intensity light (ultraviolet) under a mask which is in intimate contact with the resist layer. During developing, the resist is removed on the exposed areas (positive imaging). The first mask is the source-drain mask.
4. **Source-drain preparation**

The exposed oxide is etched in a buffered HF solution (4:1, HF:NH₄F₂). A doping impurity (boron for p-type) is then deposited on the wafer after removal of resist with acetone.

Vapor deposition from a solid source (boron nitride) or contact deposition from a liquid source (borofilm) may be used. Initial diffusion is done at a furnace temperature of 1100°C for fifteen minutes. (More diffusion takes place during growth and stabilization of the gate oxide.) The doped top layer of the oxide after the initial diffusion is etched off in buffered HF for 30-45 seconds. The sheet resistance of the p+ layer at this point is 20-30Ω/□.

5. **Photomasking II**

Step Three is repeated but the gate area mask is used this time.

6. **Gate Oxide Preparation**

After etching the exposed oxide of the gate areas, the wafer is thoroughly cleaned by boiling in a 50% HNO₃ solution and then rinsed, as explained in Step One. The 1500 Å gate oxide is grown in a wet O₂ atmosphere in the 1100°C oxidation furnace for 5½ minutes. A stabilization step is carried out by depositing phosphorous (from a P₂O₅ or phosphorous nitride source) on the new oxide at 950°C and N₂ atmosphere for 10 minutes. The resulting phosphosilicate glass is then heat treated at 1100°C for 6½ minutes in a nitrogen atmosphere.
7. Photomasking III

This step uses the contact-openings mask. But before application of the resist, the wafer is boiled in DI \( \text{H}_2\text{O} \) for 45-60 minutes to enhance the adhesion of the resist to the phosphorous-doped oxide.

8. Contact Openings Etch and Pre-evaporation Cleaning

The etching and cleaning procedures follow the same pattern as explained in the previous steps. No acid is used for cleaning here, however.

9. Metal Evaporation and Annealing

Aluminum is vacuum-evaporated on the wafer. The thickness may vary between 5000-10,000 \( \text{Å} \). The ohmic behavior of contact between the silicon and the evaporated aluminum is enhanced by alloying the two in a 530\( ^\circ \text{C} \) furnace under \( \text{N}_2 \) flow. The sheet resistance of the metal is typically 0.025 \( \Omega/\square \).

10. Photomasking IV

The metallization mask used here allows for the interconnection of parts of the circuit. If it is desired to connect only some functional sections together, another metallization mask may be required for final total device operation.

11. Aluminum Etching and Wafer Testing

The unwanted areas of evaporated aluminum are etched in a concentrated \( \text{H}_3\text{PO}_4 \) solution at 70\( ^\circ \text{C} \). The devices may be tested after removal
of the photoresist and the bad ones are usually marked.

12. Scribing and Dicing, Bonding and Encapsulation

A diamond point is used for scribing between the rows and columns. The chips are broken along the scribe lines by proper application of pressure. Si-Au eutectic composition pellets are used for bonding the chips to gold-plated headers. Aluminum wires (1 mil dia) are ultrasonically bonded to the connecting pads (3 x 3 mil²) and binding posts. The cap is then welded onto the header flange in an inert atmosphere. The device is now ready for testing and labeling.