A HIGH SPEED, TRANSISTORIZED, VOLTAGE ANALOG-TO-DIGITAL CONVERTER

by

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TABLE OF CONTENTS

LIST OF FIGURES

A HIGH SPEED, TRANSISTORIZED, VOLTAGE ANALOG-TO-DIGITAL CONVERTER

INTRODUCTION

Analog-to-digital converters are becoming increasingly more important and necessary to facilitate handling and transmission of large quantities of data with a high degree of accuracy. It is much easier to detect the presence or absence of a pulse than to sense to a high degree of accuracy an analog voltage quantity.

Several methods of coding analog voltages into digital codes have been developed (4, p. 368-404). Among these are time encoders and encoders of the counting type, including time-base encoders and angle encoders; binary-mask voltage encoders; binary weighing encoders; feedback encoders; and a reference-comparison encoder (3, p. 168-173), a solution of which is to be described in this thesis.

DECIMAL TO BINARY CONVERSION:

The explanation of the manner of operation of this reference-comparison analog-to-digital converter can best be initiated by a simplified review of the manner in which a decimal number is converted to its binary equivalent. As an example, consider conversion of the decimal number 21 to its binary equivalent. This is done by subtracting decreasing powers of 2 from the number 21 where the result of the subtraction leaves a positive remainder. When a

subtraction is performed it is recorded as a "one"; when it is not performed a "zero" is indicated. Therefore, as shown in Figure 1 on the next page, the binary equivalent of the decimal number 21 is 10101.

It would be nice, as far as electronic circuitry is concerned, to subtract the same quantity or reference each time a subtraction is performed rather than the decreasing powers of 2. This can be easily accomplished by multiplying each line in Figure 1 by successively increasing powers of 2 as shown in Figure 2. The binary indication is, of course, still the same because it is still simply an indication of whether or not a subtraction has been performed. The quantity being subtracted is always 2^4 or 16 which is the desired result.

FUNCTION OF A CODING UNIT

Now a description of the function to be performed by a single coding unit can be set forth.* If the input to the coding unit is less than the reference, no subtraction would be performed so a binary "zero" should be indicated. The output of the coder should be two times the input. If the input to the unit is greater than the reference, a

* (By a "coding" unit is meant a unit which will perform the necessary functions required for one line of "conversion" as illustrated in Figures 1 and 2. The nomenclature "encoder" will be used to describe the entire analog-to-digital converter.)

	Binary Indication
A) $21 - 2^4 = 5$	1
B) $5 - 2^3 = SNP^*$	0
C) $5 - 2^2 = 1$	1
D) $1 - 2^1 = SNP$	0
E) $1 - 2^0 = 0$	1

*SNP - Subtraction not performed

Fig. 1. Conversion of a Decimal Number to a Binary Number.

	Binary Indication	
A) $2^0(21) - 2^0(2^4) = 2^0(5)$	1	$21 - 2^4 = 5$
B) $2^1(5) - 2^1(2^3) = SNP$	0	$10 - 2^4 = SNP$
C) $2^2(5) - 2^2(2^2) = 2^2(1)$	1	$20 - 2^4 = 4$
D) $2^3(1) - 2^3(2^1) = SNP$	0	$8 - 2^4 = SNP$
E) $2^4(1) - 2^4(2^0) = 2^4(0)$	1	$16 - 2^4 = 0$

Fig. 2. Modified Conversion of a Decimal Number to a Binary Number Using a Fixed and Constant Reference of 2^4.

binary "one" should be indicated and the output of the coder would be two times the input-minus-reference quantity. One coder is required for each binary digit.

Figure 3 shows a block diagram of a coding unit which will perform this function. If $(V_{in}-V_r)$ is less than zero, the switch turns on the AND gate and the output of the AND gate and the OR gate is equal to V_{in} (neglecting losses). A binary output of "zero" would be indicated and the output of the amplifier will be two times V_{in}.

If $(V_{in}-V_r)$ is greater than zero the switch turns off the AND gate and the output of the OR gate is $(V_{in}-V_r)$. A binary output of "one" would be indicated and the output of the amplifier is two times $(V_{in}-V_r)$. Figure 4 shows these two functions graphically. $2V_r$ is the maximum input to the coder.

ENCODER DESCRIPTION

A block diagram of a ten binary place encoder is shown in Figure 5. It simply consists of a series of ten coding units with the characteristics just described. The accuracy of each coding unit will determine the maximum number of binary bits which can be assigned to the input voltage. An accuracy of 1 part in 1024 (or 2^{10}) would be desirable and will be attempted in the design of the individual coding units. Therefore, the maximum error of a ten bit encoder would be one bit.

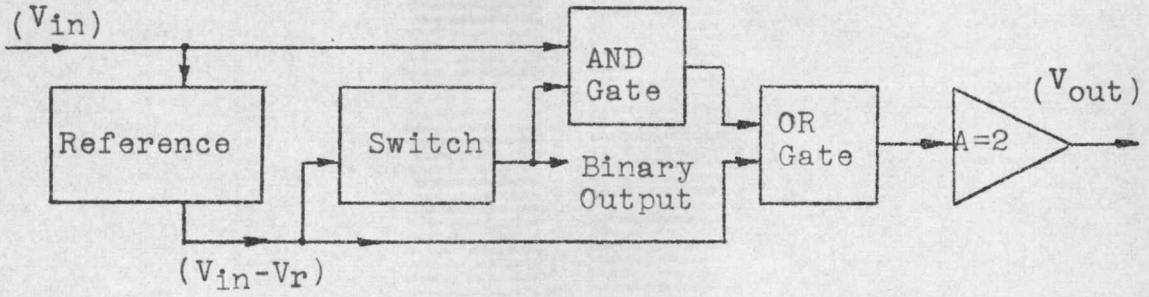
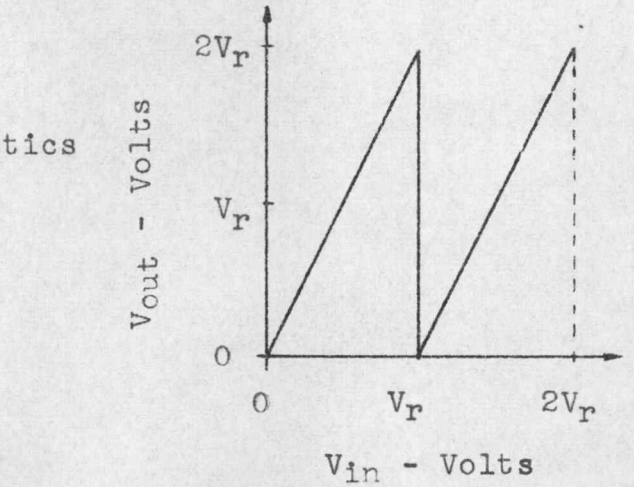
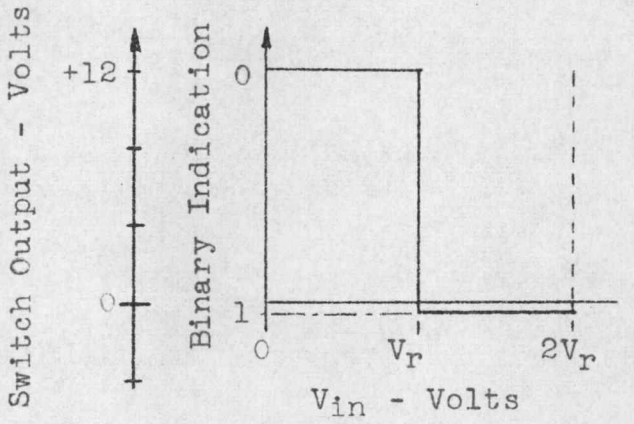


Fig. 3. Block Diagram of Coding Unit.

Fig. 4.

Transfer Characteristics of a Coding Unit: Input V/s Output and Input V/s Binary Indication.





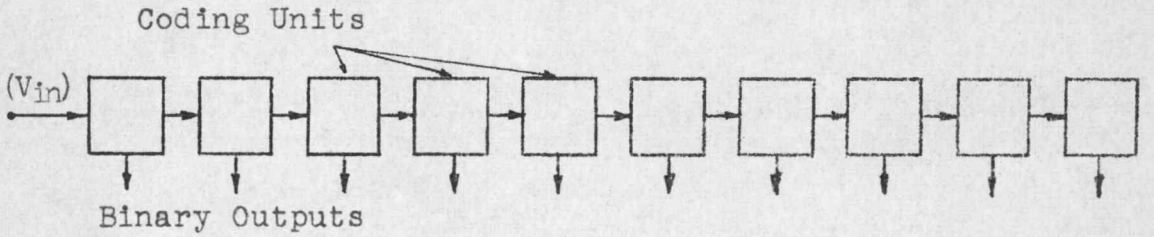


Fig. 5. A Block Diagram of the Encoder.

Direct coupling will be incorporated throughout so that inputs from d-c to high-frequency a-c may be accommodated. The upper limit of the frequencies which can be coded will be limited by the types of transistors used, by the circuit configurations, and by inherent stray capacities as far as each individual coding unit is concerned. Later, another frequency limitation which is the result of cascading coding units will be discussed. With this background it is possible to design circuits to fill the blocks of Figure 3 which will meet the accuracy requirements.

OBTAINING THE REFERENCE VOLTAGE

There are several ways in which the required reference voltage could be obtained. Because of the limitation on the amplitude of the input signal due to transistor rating, a reference voltage in the vicinity of 2 to 4 volts would be desirable. Standard cells could be used for this purpose other than for severe frequency limitations. Zener diodes were also considered but it was found that low voltage zener diodes have much too "round" a knee on their reverse bias characteristic. This results in a wide variation of dynamic impedance as the reverse current flow is varied; this wide variation can't be tolerated. In addition to this problem is the added problem of dynamically

and statically matching ten zener diodes to a tolerance of less than 0.05%.

Certain silicon diodes seem to offer a solution to the problem because of their sharp forward bias knee, low dynamic resistance, and a reasonably high frequency response (or a short recovery time). Several such diodes in series would have a reasonable d-c voltage drop and a fairly low forward dynamic impedance. Figure 6 illustrates how the subtraction of V_r from V_{in} might be performed. Attenuation of V_{in} due to forward resistance of the diodes can be minimized by making R much larger than this forward resistance, about 1500 times larger if the desired accuracy of 1 part in 1024 is to be maintained. R can be varied somewhat to change the quiescent current through the diodes thereby adjusting the value of V_r and eliminating the necessity of precise matching of the reference diodes in the ten coding units. As the series dynamic impedance of the three silicon diodes is about 150 ohms, it is easily seen that R must be about 250 kilohms or greater. If a d-c current of approximately 2 milliamperes flows in the circuit a negative supply voltage of about 500 volts is required. This high supply voltage is the penalty which must be paid to achieve the desired accuracy. The result is worth the price. The value of V_r is about 2.0 volts. This value will be somewhat altered in the final complete circuit.

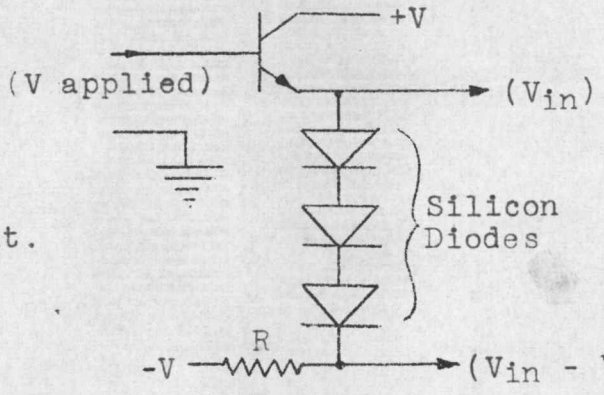


Fig. 6.

Subtraction or
Reference Circuit.

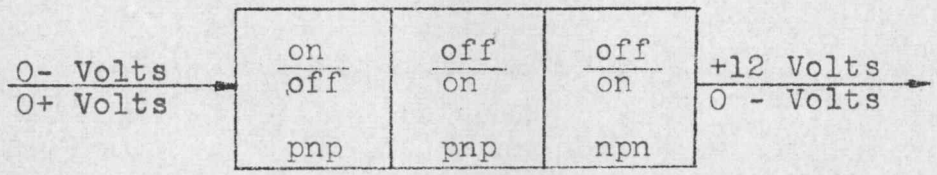


Fig. 7. Preliminary Block Diagram of Switching Circuit

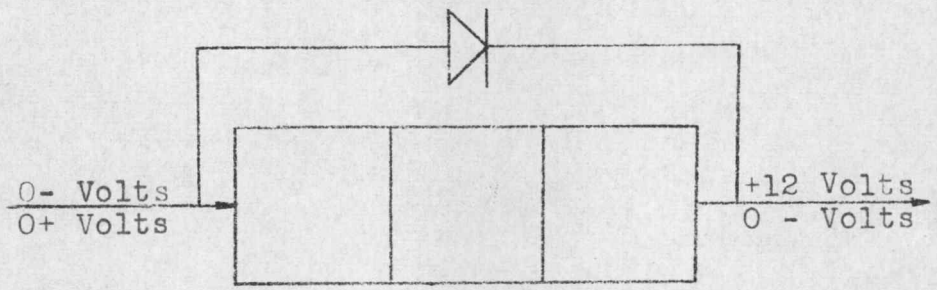


Fig. 8. Theoretical Feedback Applied to the Switching Circuit to Minimize Saturation Effects.

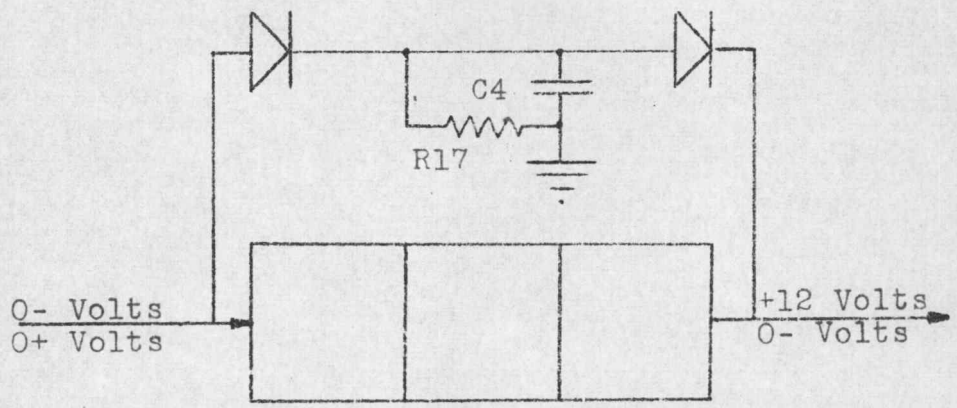


Fig. 9. A Practical Feedback Loop Applied to the Switching Circuit to Minimize Saturation Effects.

THE SWITCHING CIRCUIT

The requirements of the switching circuit following the reference or subtraction circuit (Figure 3) are somewhat difficult to satisfy. The requirements or specifications for this circuit are as follows:

1. The output must switch completely from one level to the other for a change of only 2 millivolts on the input.
2. The input should be able to handle voltage amplitudes of plus or minus 3 volts without damage to circuit.
3. For a change of 2 millivolts on the input, the output should change 12 volts; therefore, a minimum voltage gain of 6000 is required.
4. Response time should be made as short as possible.
5. Direct coupled circuitry must be used throughout to maintain d-c input response.

Figure 7 shows a block diagram of the switching circuit and the condition of each stage relative to the input and output voltages. Saturation of any of the transistor stages must be avoided if high-speed operation is to be maintained (1, p. 593). The input transistor is cut off by positive inputs and therefore presents a high impedance to the input voltage at a time when excessive loading is important, as

will be pointed out later. Saturation of the switching circuit theoretically could be avoided by connecting a diode feedback loop as shown in Figure 8. As might be expected, the result of this is oscillation but a cure in the form of the compensation network and feedback loop shown in Figure 9 is quite effective. The "trial-and-error" method was used to determine the optimum values for R_{17} and C_4. A mathematical analysis of the switching circuit to determine the values of R_{17} and C_4 is impractical because of the nonlinearity of both the amplifier and the feedback loop and because of the difficulty of accurately correlating the gain and phase relationships of the transistors involved.

Figure 10 shows a schematic diagram of the complete switching circuit. The first stage is operated at a low collector current so that a small base current change will turn it on or off. The variable resistors in the emitter circuit are used to set the bias point of the stage or in effect the point at which the switching action will occur. It is desirable that the resistance in the emitter circuit be small so as to introduce as little degeneration as possible.

The second and third stages are simple amplifiers. The second stage operates fairly linearly but its output voltage swing is sufficiently large to drive the third stage from cutoff to near saturation. A separate 1.5 volt

Fig. 10.

Schematic Diagram of Switching Circuit.

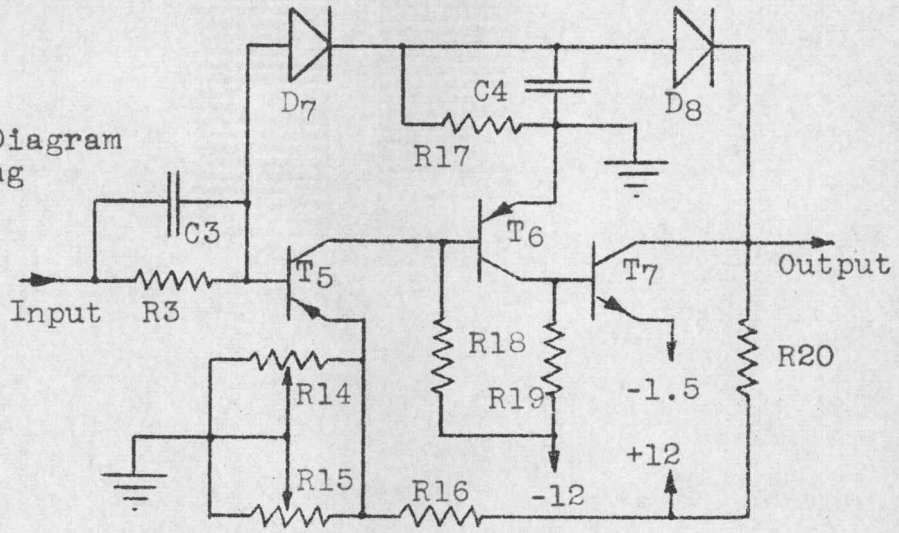
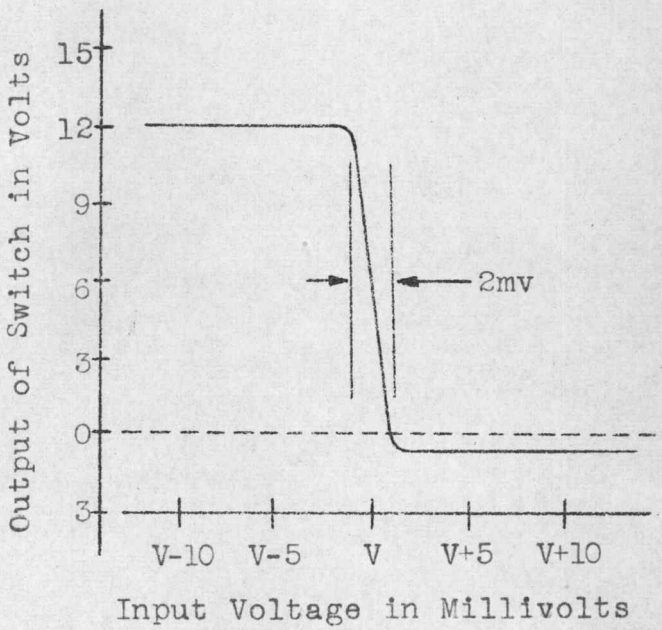


Fig. 11.

Switching Characteristics of the Circuit Shown in Fig. 10



supply is used on the emitter of the third stage to avoid degeneration which would be introduced if a voltage divider were used to furnish the 1.5 volts.

Figure 11 shows graphically the function of the switch. The value of V is a function of the bias setting for the first stage. It is important to keep in mind that the switch circuit should have an output of plus 12 volts when the input to the coding unit is less than the chosen reference voltage and an output of less than zero volts when the input is greater than the reference.

THE LOGIC CIRCUITS

The output of the switch circuit is applied along with V_{in} to a positive input AND gate as shown in Figure 12 (1, p. 397). The output of this gate is also shown in Figure 12. Note the d-c displacement due to the d-c voltage rise across the signal input diode in the AND gate. As will be shown later, this d-c level change will become part of V_r.

The output of this AND gate and the signal $(V_{in}-V_r)$ are both applied to a positive input OR gate (1, p. 394). It should be kept in mind that the output of this OR gate will be a result of the most positive input signal. Figure 13 shows the OR gate, its inputs, and its output.

Losses due to resistance in the diodes must be minimized in both the AND and OR gates (2, p. 93-113).

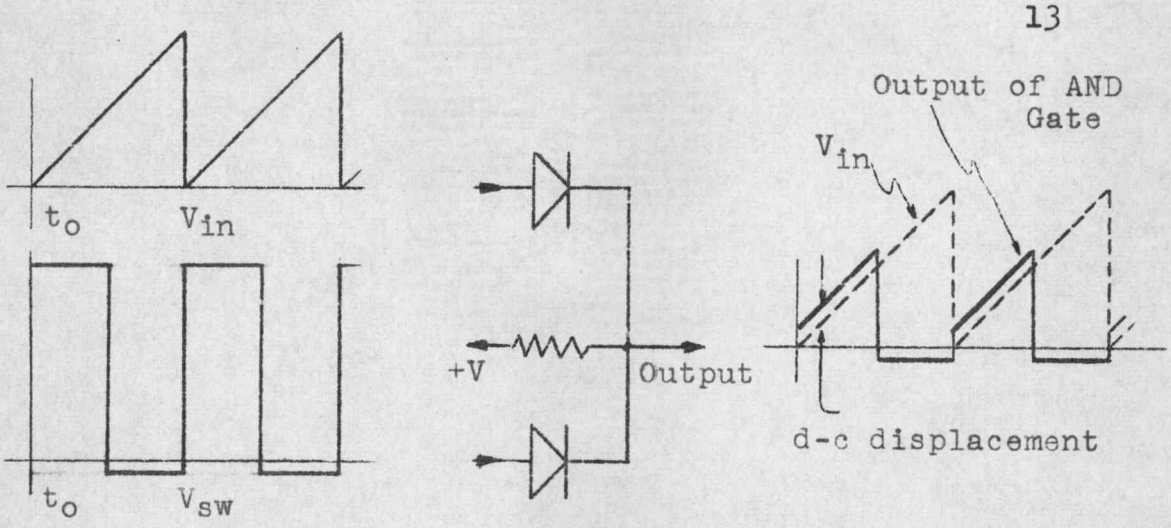


Fig. 12. Schematic & Function of the AND Gate

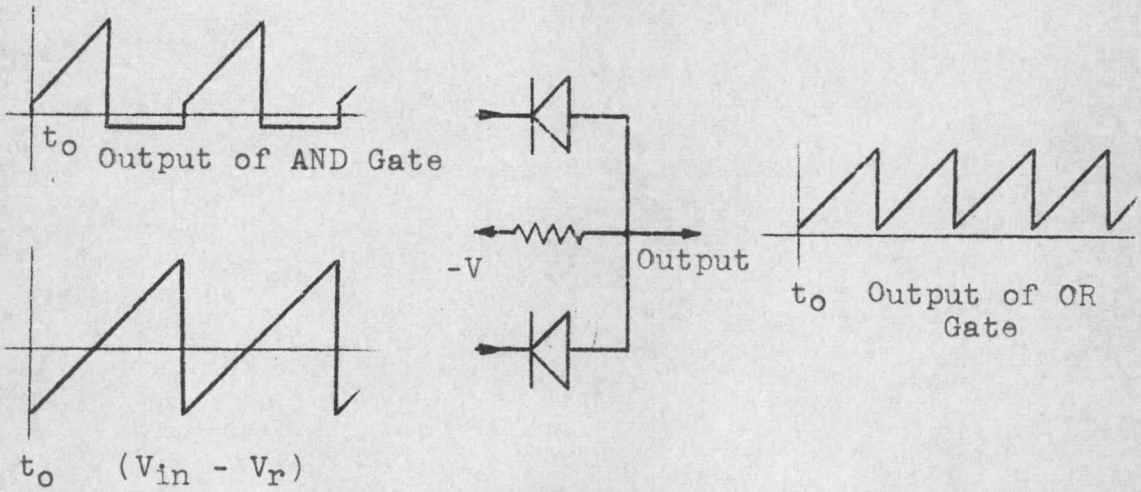
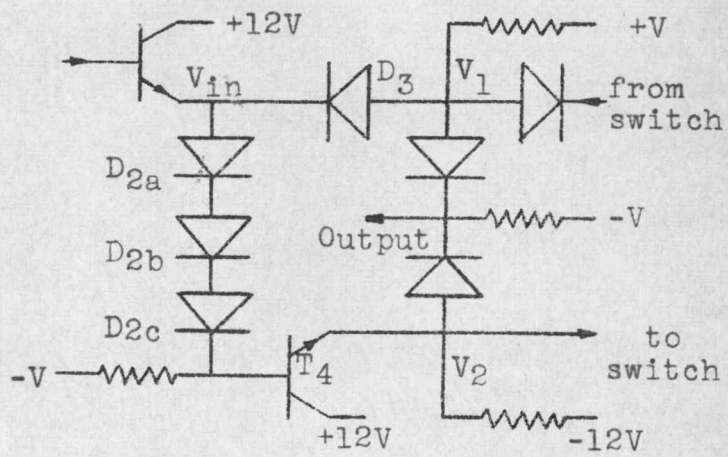


Fig. 13. Schematic & Function of the OR Gate

Fig. 14.

The Complete Logic Circuit Showing the True Reference Voltage

$V_r = V_1 - V_2$



This can be done by making the pull-up resistors very much larger than the dynamic resistance of the diodes. In the case of the OR gate this can be easily done as a high negative voltage is already available. An OR gate resistor of 470 K was chosen allowing an OR gate current of about 1.0 milliampere. Because of the total input impedance of the signal input on the AND gate (due both to the diode and the signal source impedance) a pull-up resistor of about 270 K is necessary. This means that a positive supply voltage of about 350 volts is necessary for the AND gate.

THE TRUE REFERENCE VOLTAGE

At long last the exact reference voltage can be ascertained. It is the sum of the d-c voltage drops across D_3, D_{2a}, D_{2b}, D_{2c}, and the emitter junction of transistor T_4. This amounts to the difference of the d-c potentials at each of the OR gate inputs with no signal applied to the circuit.

This reference voltage should be set at a fixed level in each of the individual coding units by adjusting the current flow through diodes D_{2a}, D_{2b}, and D_{2c}. The switching point should then be adjusted to occur when the input signal, V_{in}, raises the lower input to the OR gate to the same potential at which the upper input to the OR gate was before the input signal was applied. In other

words, when the input signal has reached the value, V_r, the switching action should occur.

THE TIMES-TWO AMPLIFIER

Finally the output of the OR gate must be applied to the input of a times-two amplifier having a very high input impedance (to minimize any loading effect). A very large amount of feedback is incorporated in this amplifier for the two reasons of maintaining a gain of $2 \pm 0.05\%$ and minimizing d-c drift on the output. To accomplish this without running into serious phase shift (and oscillation) problems two stages of amplification are necessary. In order to maintain the desired d-c levels on the input and output, one p-n-p and one n-p-n stage must be used.

Feedback from the collector of the second stage would have to be to the emitter of the first stage as negative feedback is desired. Therefore, unbypassed resistance must be present in the emitter circuit of the first stage. This unbypassed resistance increases the input impedance of this stage to a very high value, making an emitter follower isolation stage between the output of the OR gate and the input of the amplifier unnecessary. Of course, direct coupling must be used throughout to maintain the low frequency response.

With these restrictions the amplifier circuit shown in Figure 15 was evolved. During the development process

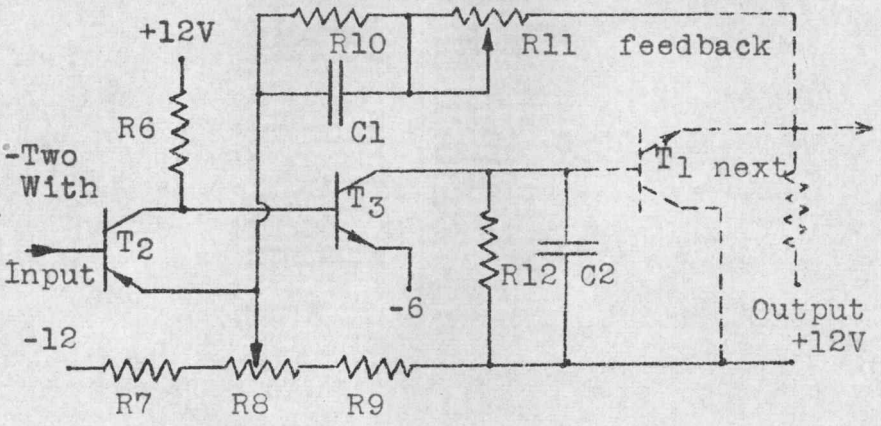


Fig. 15.

The Times-Two Amplifier With Stability Equations

$$A_{fb} = \frac{A}{1-BA} = 2$$

$$\frac{dA_{fb}}{dA} = \frac{d}{dA}\left(\frac{A}{1-BA}\right) = \frac{1}{1-BA} - \frac{-BA}{(1-BA)^2} = \frac{1}{(1-BA)^2}$$

$$\text{Ergo } \Delta A_{fb} = \frac{\Delta A}{(1-BA)^2}$$

Therefore, the fractional change in gain with feedback is:

$$\frac{\Delta A_{fb}}{A_{fb}} = \frac{\Delta A}{(1-BA)^2} \div \frac{A}{(1-BA)} = \left(\frac{1}{1-BA}\right)\frac{\Delta A}{A}$$

If $A = (50)^2 = 2500$, then $\frac{A}{A_{fb}} = (1-BA) = 1250$

So if $\frac{\Delta A_{fb}}{A_{fb}} = 0.0005$,

$$\frac{\Delta A}{A} = (1-BA)\frac{\Delta A_{fb}}{A_{fb}} = (0.0005)(1250) = 62.5\%$$

it was decided to include the input emitter follower of the next coding stage in the feedback loop. This, along with some equations showing the effect of feedback, is also included in Figure 15. These equations demonstrate how much open loop gain variation can be tolerated.

Because of the high gain and the large amount of feedback around the amplifier, high frequency compensation as provided by C_2 was found to be necessary. This so curtailed the high frequency feedback of the circuit that the high frequency gain of the amplifier was found to be considerably greater than two. C_1 remedied this situation very well. The values of C_1 and C_2 were determined experimentally because of the difficulty of accurately determining the phase-gain relationships of the transistors and accurately calculating the needed compensation.

A diode connected between the base at the first transistor in the times-two amplifier and ground prevents large amplitude negative spikes from saturating this stage.

THE COMPLETE CODING CIRCUIT

Figure 16 shows the complete coding circuit along with all component values. Without using close-tolerance components better than 20%, this circuit achieves a high degree of accuracy. The signal path is through low loss AND and/or OR gates and through a stabilized amplifier.

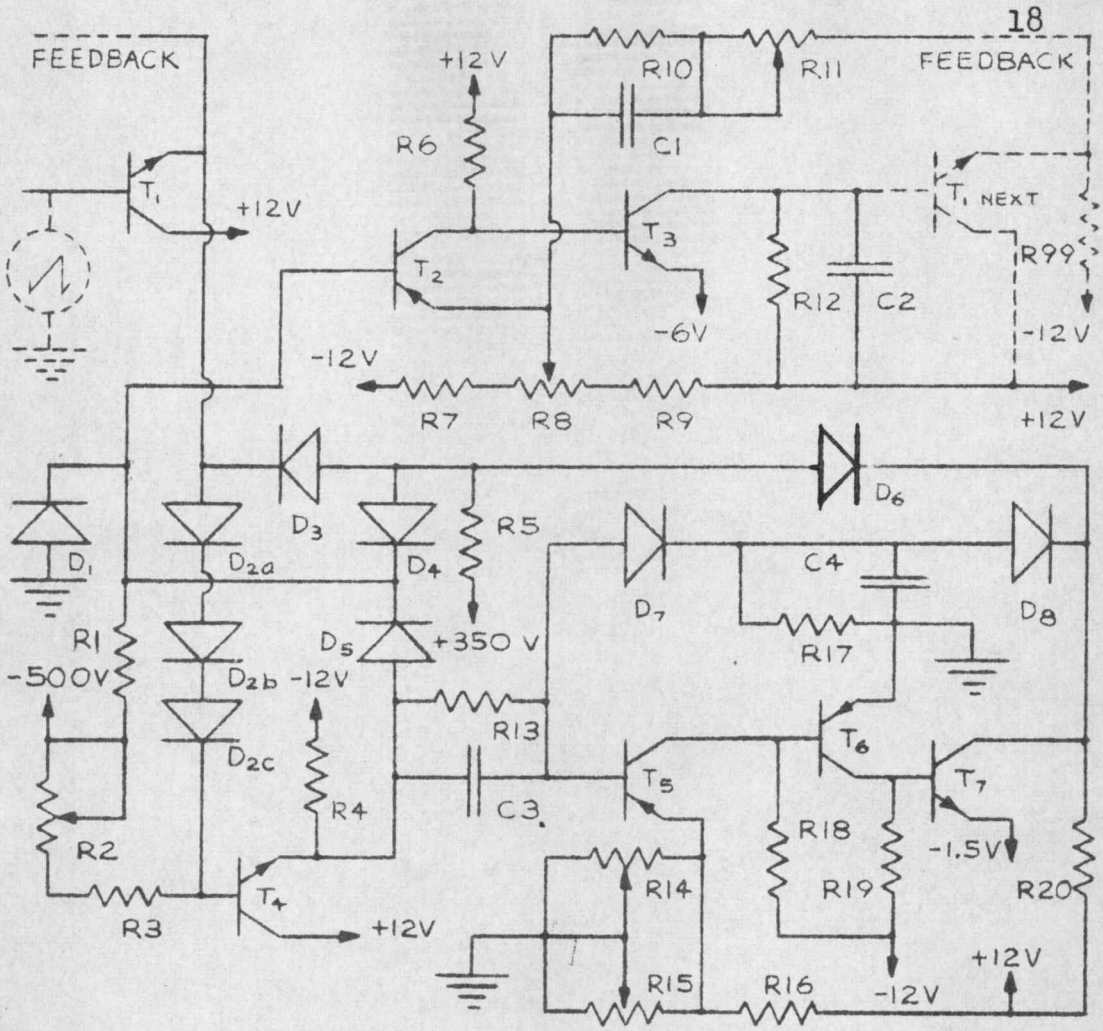


Fig. 16. The Complete Circuit Showing Component Values

R1 - 470K	R8 - 1.0K Pot	R18 - 22K
R2 - 500K Pot	R10, R16 - 620 ohm	R19 - 6.2K
R3 - 240K	R11, R15 - 2.0K Pot	R20 - 1.0K
R4 - 3.3K	R12 - 4.7K	C1 - 0.002 uf, 50 volt
R5 - 270K	R13 - 10K	C2 - 0.006 uf, 50 volt
R6 - 12K	R14 - 50 ohm Pot	C3 - 250 pf, 50 volt
R7, R9 - 1.2K	R17 - 5.6K	C4 - 0.1 uf, 50 volt

R99 - 3.3K (used for test purposes only)

D_1, D_4, D_5, D_6 - WE400D Germanium Diodes
D_{2a}, D_{2b}, D_{2c}, D_3, D_7, D_8 - Silicon Diodes
T_1, T_3, T_4, T_7 - 2N169A NPN Transistors
T_2, T_5, T_6 - 2N544 PNP Transistors

All active elements through which the input signal travels are stabilized via feedback.

Within reason, component selection is not necessary. This is because of the ability to adjust to some extent the value of V_r and the level at which the switch action takes place.

The +350 volt and -500 volt supplies can vary over a range greater than $\pm$20% of their nominal value. Other supply voltages should be regulated but some variation in unison is permissible (such as would result from line voltage variations).

Resistor R99 is used for test purposes only. Actually the next coding unit would be cascaded in place of R99.

THE TWO ALTERNATE SIGNAL PATHS

Figure 17 shows the signal path through the coding device when V_{in} is less than V_r. The signal actually passes through one diode in the AND gate and one diode in the OR gate, both of which are very low loss gates, and through an amplifier and emitter follower which are enclosed inside of a feedback loop. Therefore it can be said that a high degree of accuracy has been achieved in this signal loop.

The signal path when V_{in} is greater than V_r is shown in Figure 18. For this situation the path through the AND gate has been turned off by the switch circuit

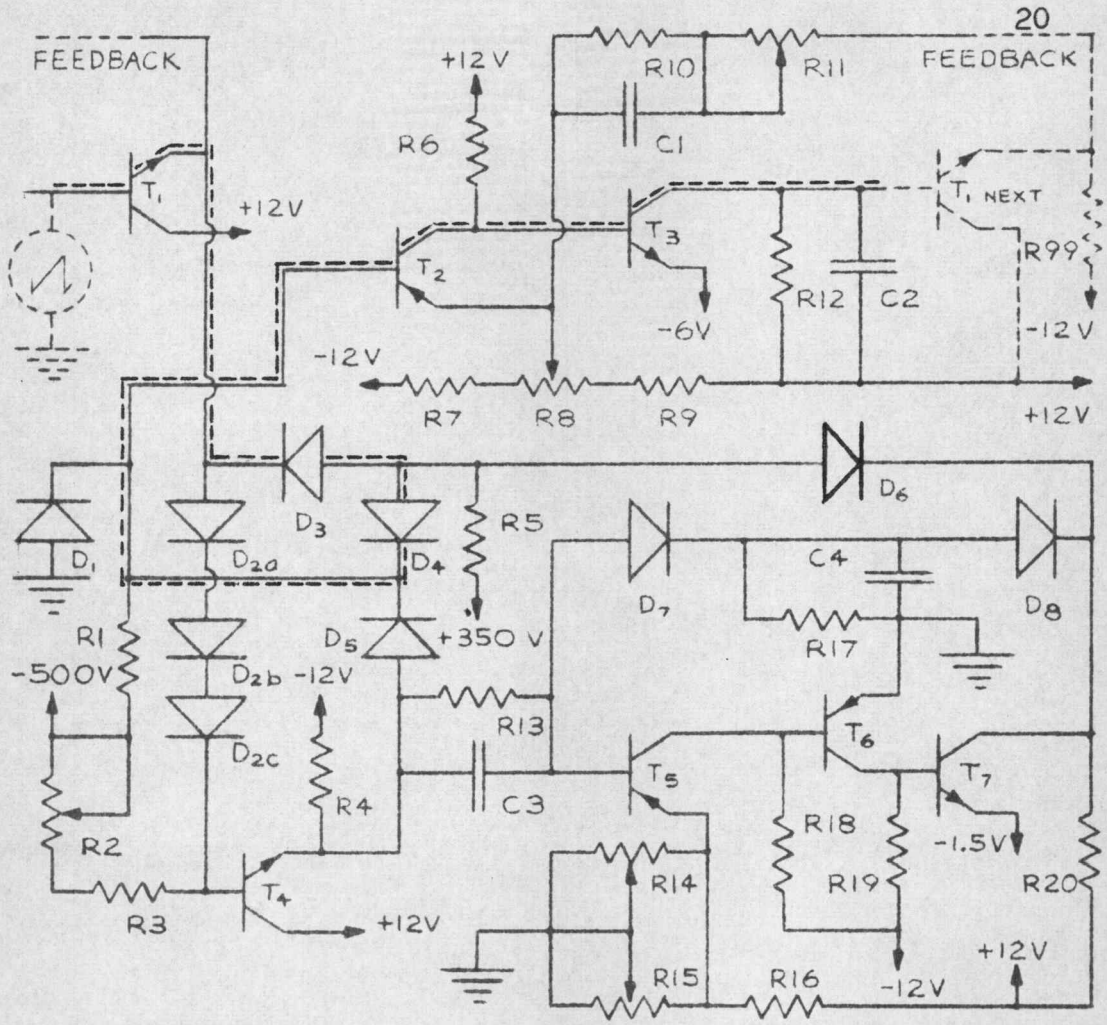


Fig. 17. The Coding Circuit Diagram Showing The Signal Flow Path When V_{in} is Less Than V_r (follow the dotted line).

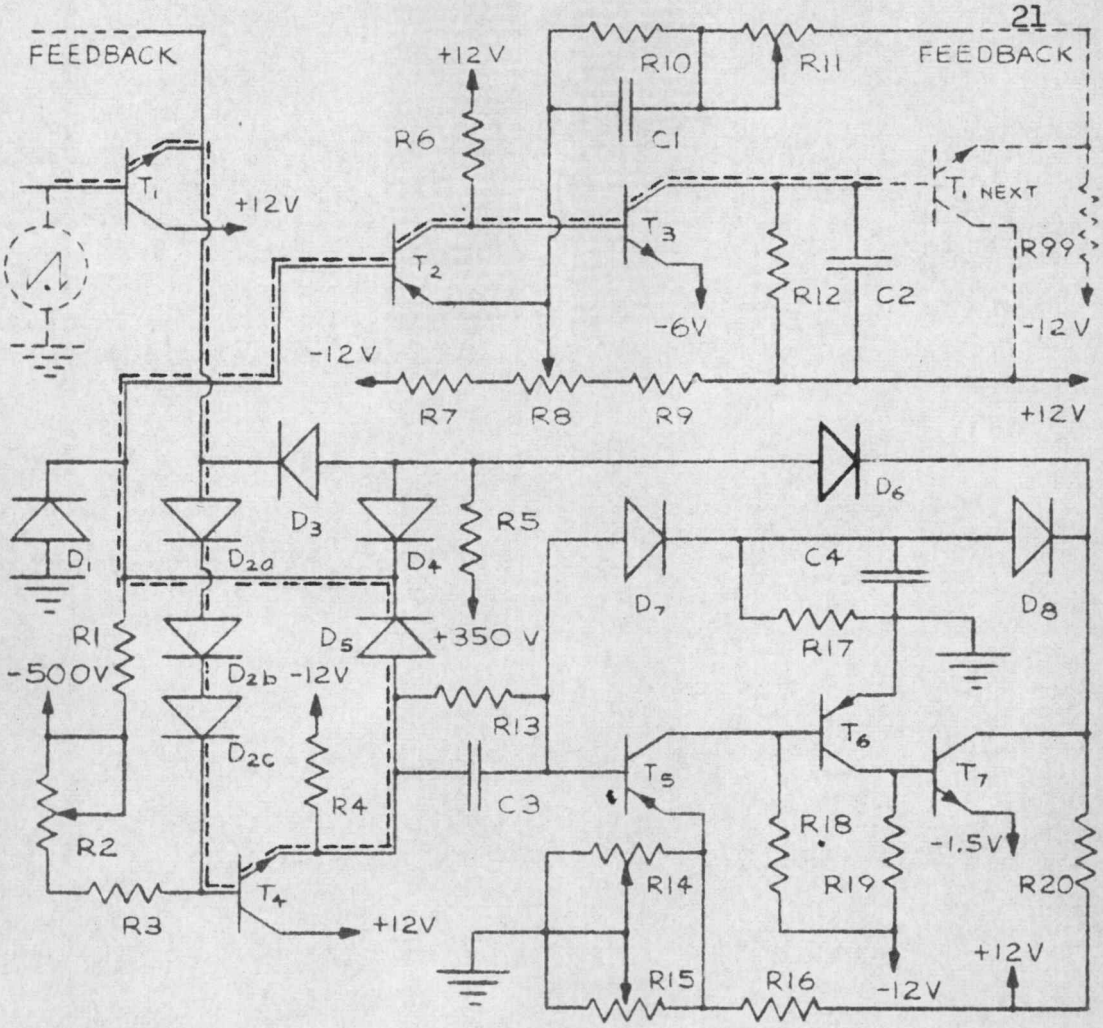


Fig. 18. The Coding Circuit Diagram Showing The Signal Flow Path When V_{in} is Greater Than V_r (follow the dotted line)

so the only signal path left is through the reference diode string, through the emitter follower (T_4) and the OR gate, and finally the amplifier circuit. The switch circuit input transistor is now cut off so it presents a very high impedance to the circuit and causes no loading effect on this signal path.

CORRELATION OF ACTUAL WITH EXPECTED WAVEFORMS

The complete coding circuit is shown again in Figure 19 along with eight test points. The following waveform pictures will refer to this diagram. In Figures 20 through 23, the ground reference is 1 centimeter below midscale. The same trigger point is used for Figures 20, 21, 22, 23 (upper), and 27. For Figures 20 through 27, the abbreviations "V.S." and "H.S." stand for "vertical scale" and "horizontal scale" respectively.

Figure 20 (upper) shows the type of input signal used. A sawtooth wave was chosen because of the ease of observing linearity deviations and the ease of making relative time measurements. The fall of the sawtooth wave furnishes an excellent trigger source making proper phase relationships between observed signals easy to maintain.

Figure 20 (lower) shows the d-c displacement across the reference diode string. The value of this d-c displacement is about 2 volts and can be varied approximately plus-or-minus 0.2 volts about this center point. This d-c

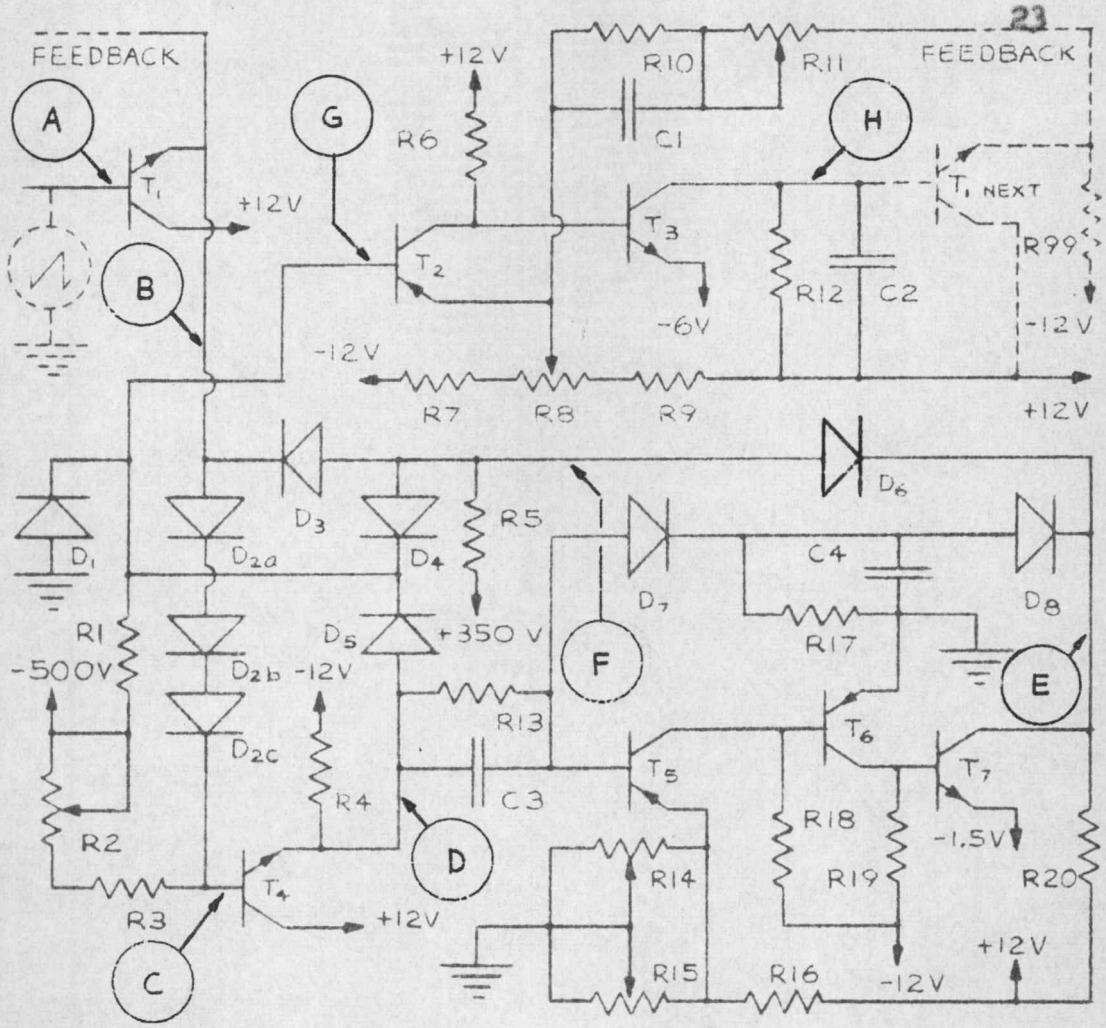


Fig. 19. The Schematic Diagram - Showing the Test Points Which will be Referred to in the Next Several Illustrations.

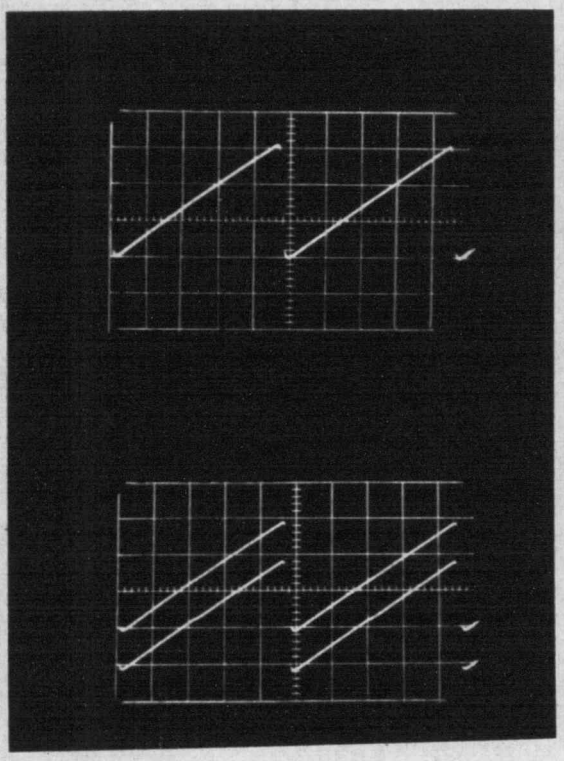


Fig. 20.

Point "A" on Diagram:
Output of Test
Voltage Source.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

Points "G" and "C"
D-C Displacement
Across Reference
Diodes.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

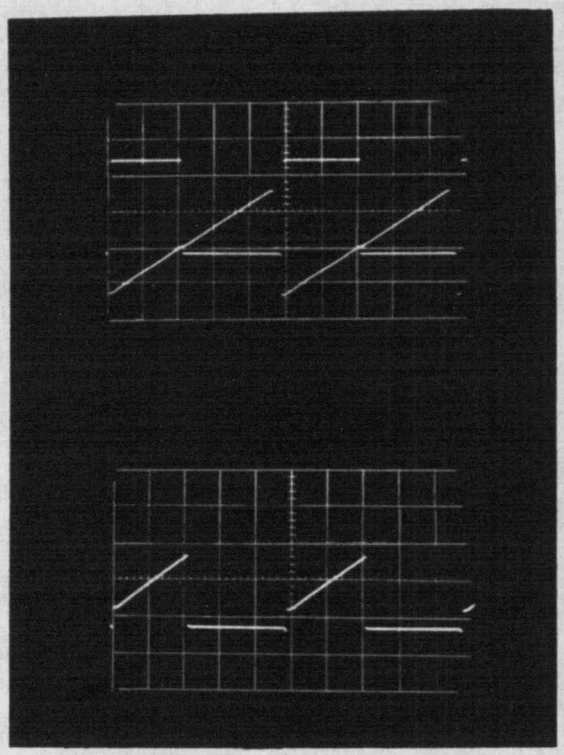


Fig. 21.

Point "D": Sawtooth
Input to Switch
Circuit.
V.S.: 2 volt/cm
and Point "E":
Square Wave Output
of Switch Circuit
V.S.: 5 volt/cm.
H.S.: 20 usec/cm.

Point "F": Output of
AND Gate and Upper
Input to OR Gate.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

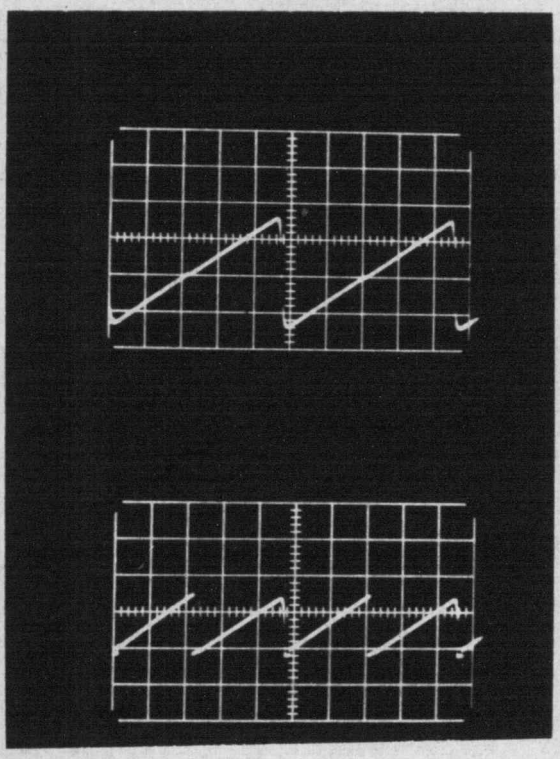


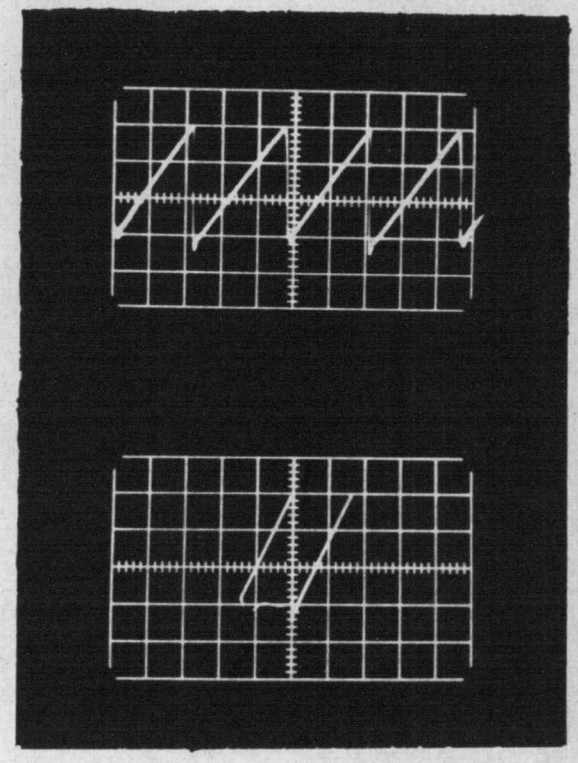
Fig. 22.

Point "D": Lower Input to OR Gate.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

Point "G": Output of OR Gate and Input to Amplifier.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

Fig. 23.

Point "H": Output of Amplifier.
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.



Signal at Point "H" Versus Signal at Point "A".
V.S.: 2 volt/cm.
H.S.: 2 volt/cm.

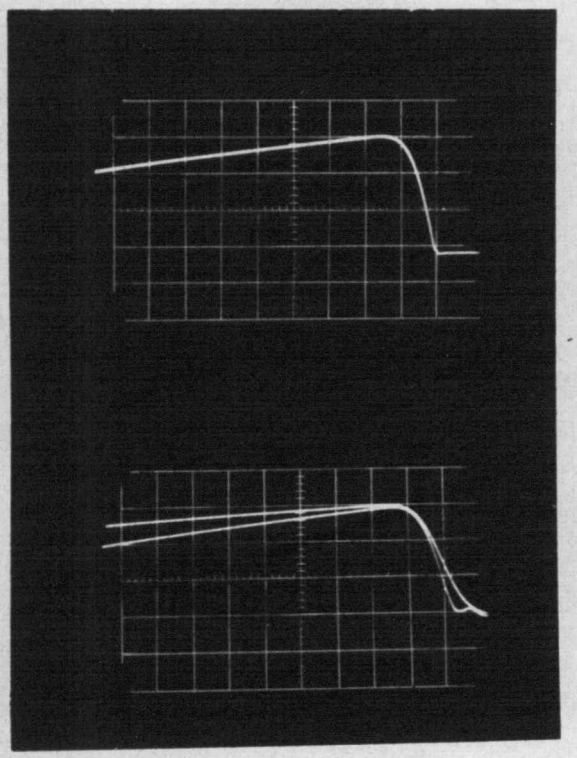


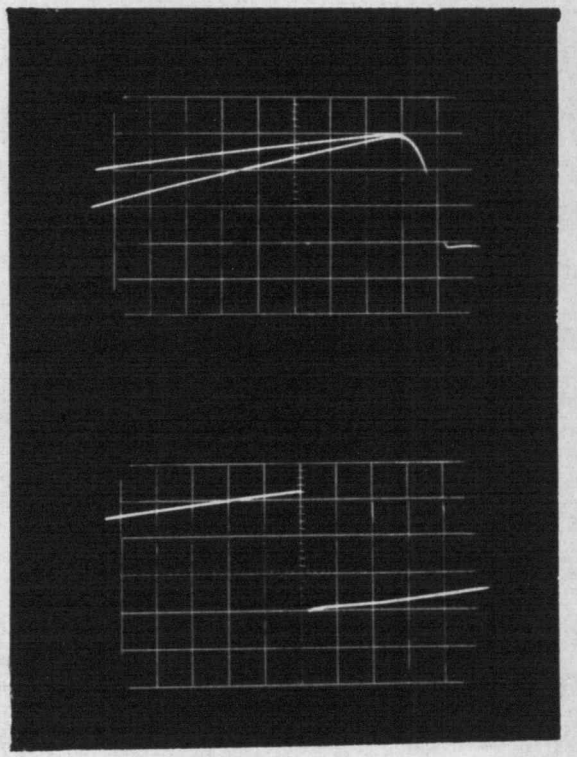
Fig. 24.

Response Time
Comparison Between
Points "A" and "G"
V.S.: 1 volt/cm.
H.S.: 2 usec/cm.

Response Time
Comparison Between
Points "A" and "H"
V.S.: 2 volt/cm.
H.S.: 2 usec/cm.

Fig. 25.

Response Time
Comparison Between
Points "G" and "H"
V.S.: 1 volt/cm.
H.S.: 2 usec/cm.



Point "G": Midsignal
Falltime of Output
of OR Gate.
V.S.: 1 volt/cm.
H.S.: 2 usec/cm.

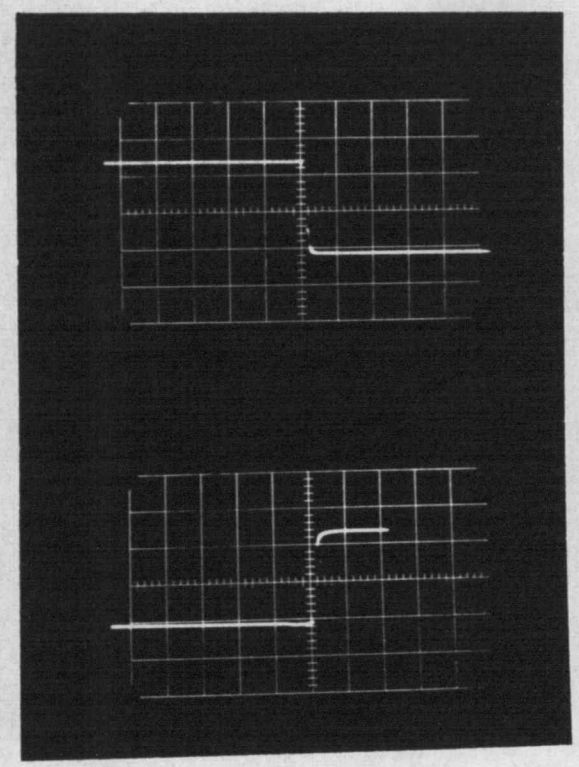


Fig. 26.

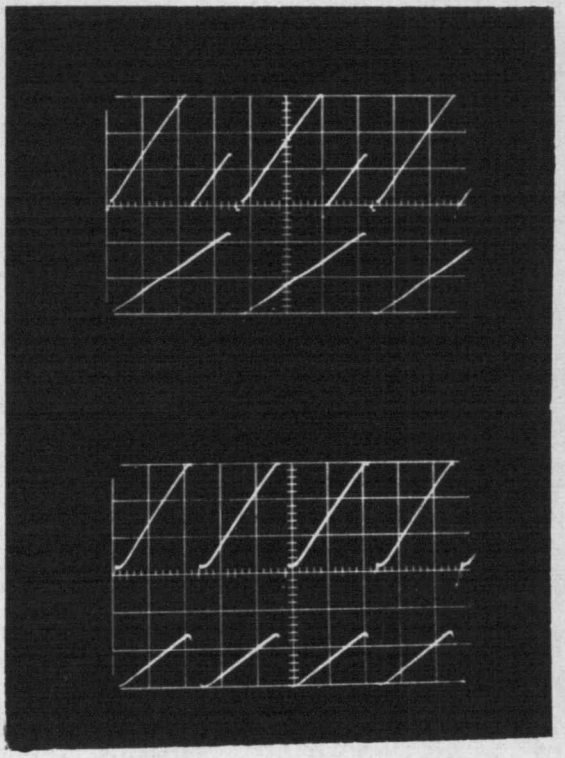
Point "E": Risetime
of Switch Output
V.S.: 5 volt/cm.
H.S.: 2 usec/cm.

Point "E": Falltime
of Switch Output
V.S.: 5 volt/cm.
H.S.: 2 usec/cm.

Fig. 27.

Point "H" Displayed
Above Point "A":
Input is 3/4 of
Full Range
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.

Point "H" Displayed
Above Point "A":
Input is 1/2 of
Full Range
V.S.: 2 volt/cm.
H.S.: 20 usec/cm.



displacement is not the total reference voltage as it does not include the voltage drops across the AND gate diode D_3 and the emitter follower T_4. No visible attenuation of V_{in} after it has passed through the reference diode string is observable. This observation was made after adjusting the gain of each input to the oscilloscope to as nearly the same value as possible using a very fine line trace (low intensity and proper focus).

Figure 21 (upper) shows the input to the switching circuit (sawtooth) and the output of the circuit. Note that the input to the switch is $V_{in}-V_r$. This result can be compared with Figure 11 in which the function of the switch is shown graphically.

Figure 21 (lower) shows how the output of the switch along with the AND gate is used to gate the input signal. This picture shows exactly the same result as specified by Figure 12.

Figure 22 (upper) along with Figure 21 (lower) are the two actual inputs to the OR gate. Their relative instantaneous levels are quite important as it is the more positive of the two inputs which will appear at the output as Figure 22 (lower) illustrates. The function of the OR gate as set forth in Figure 13 is verified by the waveforms shown in Figure 22.

Figure 23 (upper) shows the output of the amplifier. The amplitude of this output is the same as the amplitude of the input since the input was equal to $2V_r$. Figure 23 (lower) shows the output versus the input. Other than for frequency limitations, this picture should look the same for any type of input (sinusoidal, triangular, etc.). The actual results shown in Figure 23 (lower) compare quite favorably with the desired results depicted by Figure 4.

TRANSIENT RESPONSE WAVEFORMS

Figure 24 (upper) compares the input to the coder circuit with the input to the times-two amplifier. Any delay between these signals would be caused primarily by capacitive loading of the AND and OR gates. Shunt capacities in these gate circuits can be minimized by using pull-up resistors having an exceptionally small shunt reactance and by properly laying out the circuit wiring and components.

The delay of the entire coder unit is shown by Figure 24 (lower). This compares the input to the coder with the output of the amplifier. It is difficult to properly interpret this comparison because by looking at the picture one would think that there was a "negative" delay. This of course is not the actual case. The true delay could be found by decreasing the amplitude of the amplifier output by a factor of two before superimposing the signals

to make the comparison. If this were done, a delay time of approximately 0.4 usec. would be observed.

Figure 25 (upper) compares the input and output of the amplifier. The maximum delay observable here is also about 0.4 usec. which seems to indicate that most of the delay in the entire coder occurs in the times-two amplifier.

Figure 25 (lower) shows the turn-off time of the AND gate. This, of course, is a function of how fast the switching circuit turns off. This turn-off time is about 0.3 usec. This is not a limiting feature of the circuit, although, if it were, faster diodes would probably help to decrease it.

The response of the switching circuit is shown in Figure 26. The upper picture shows the risetime of the circuit to be about 0.5 usec. The falltime as shown by the lower picture is about 0.5 usec. also. The speed-up capacitor on the input to the switch helps to attain these relatively fast rise and fall times.

Due to pure delay time the maximum repetition rate of the switch is about 250 kc. This delay time through the switching circuit definitely limits the speed of the coding device because it allows the input to get too large before subtracting V_r from it or too small before ceasing to subtract V_r. The result can be likened to a hysteresis effect.

INPUTS LESS THAN FULL RANGE

Figure 27 (upper) shows the output of the coder (top trace) when the input (bottom trace) is approximately 3/4 of full range ($2V_r$). Figure 27 (lower) shows the output of the coder when V_{in} is slightly greater than V_r or half of full range. These pictures are included to help clarify the operation of the coding unit. If the input were less than V_r, all that the coding unit would do is to amplify the input two times and indicate a binary zero (the switch output would be +12 volts).

THE TEST SETUP

Figure 28 shows the test setup including the high voltage power supplies used. The test jig upon which the coding unit was built is sitting in front of these power supplies. A close-up of this jig is shown in Figure 29. In this day and age miniaturization seems to be the byword. With this in mind the coding unit prototype was laid out on three 1 3/8" by 1 7/8" boards. These three boards contain one entire coding unit exclusive of the adjustment potentiometers. The rest of the paraphernalia is present for the purpose of simplifying testing. The switch bank on the left hand side of the test jig turns off and on all six power sources simultaneously. The three boards (from left to right) contain the input emitter follower and logic

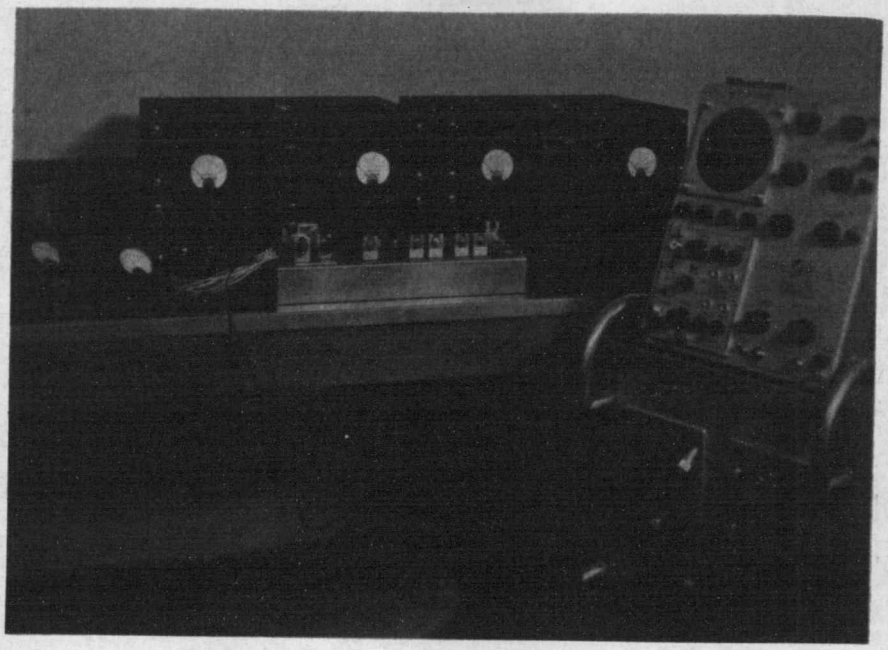


Fig. 28. The Test Setup for a Single Coding Unit

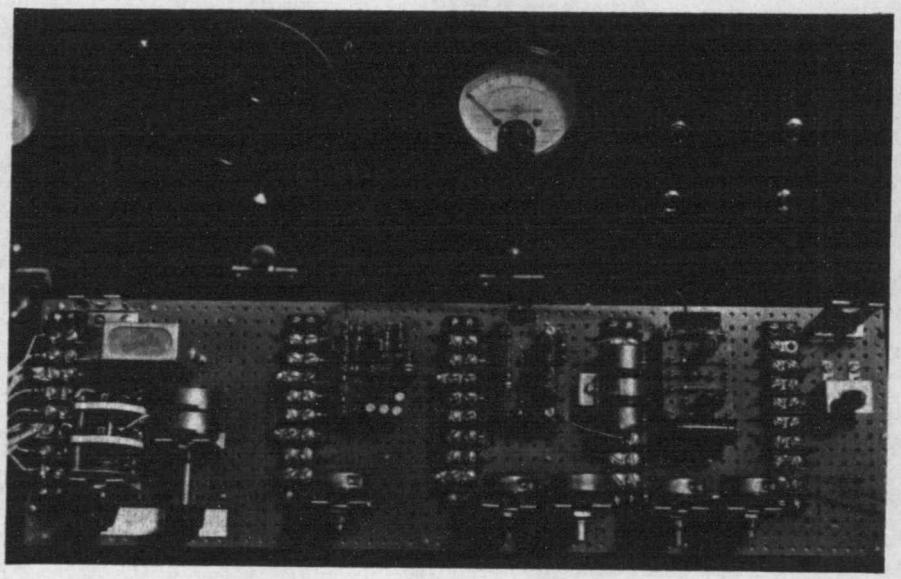


Fig. 29. A Close-up of the Single Coding Unit

circuits, the switching circuit, and the amplifier circuit in that respective order. The simulated next stage emitter follower is outboarded on the extreme right side of the test jig.

AN ADDITIONAL CODING SPEED LIMITATION

After constructing and testing a coding unit, an additional - not so obvious - speed limitation became apparent. Figure 30 will help to explain this. Assume an input to the first coding stage of a positive half of a sine wave, the amplitude of which is equal to $2V_r$. When the amplitude of this input exceeds V_r, V_r is subtracted from it. This results in two nearly triangular shaped wave segments each of which has a fundamental frequency component that is <u>six times</u> greater than the input fundamental frequency. In each successive coding unit this triangular wave is approximately cut in half and then amplified two times. After passing through ten coding units, the width of the first and last triangular wave segments would be equal to the arcsin of 1/1024 or about 3.3 minutes.

Therefore the fundamental frequency component of one of these segments would be $(180)(60) \div 3.3$ or about 3273 times the fundamental frequency of the input signal. But to reproduce this triangular wave as accurately as is necessary would require the reproduction of at least the

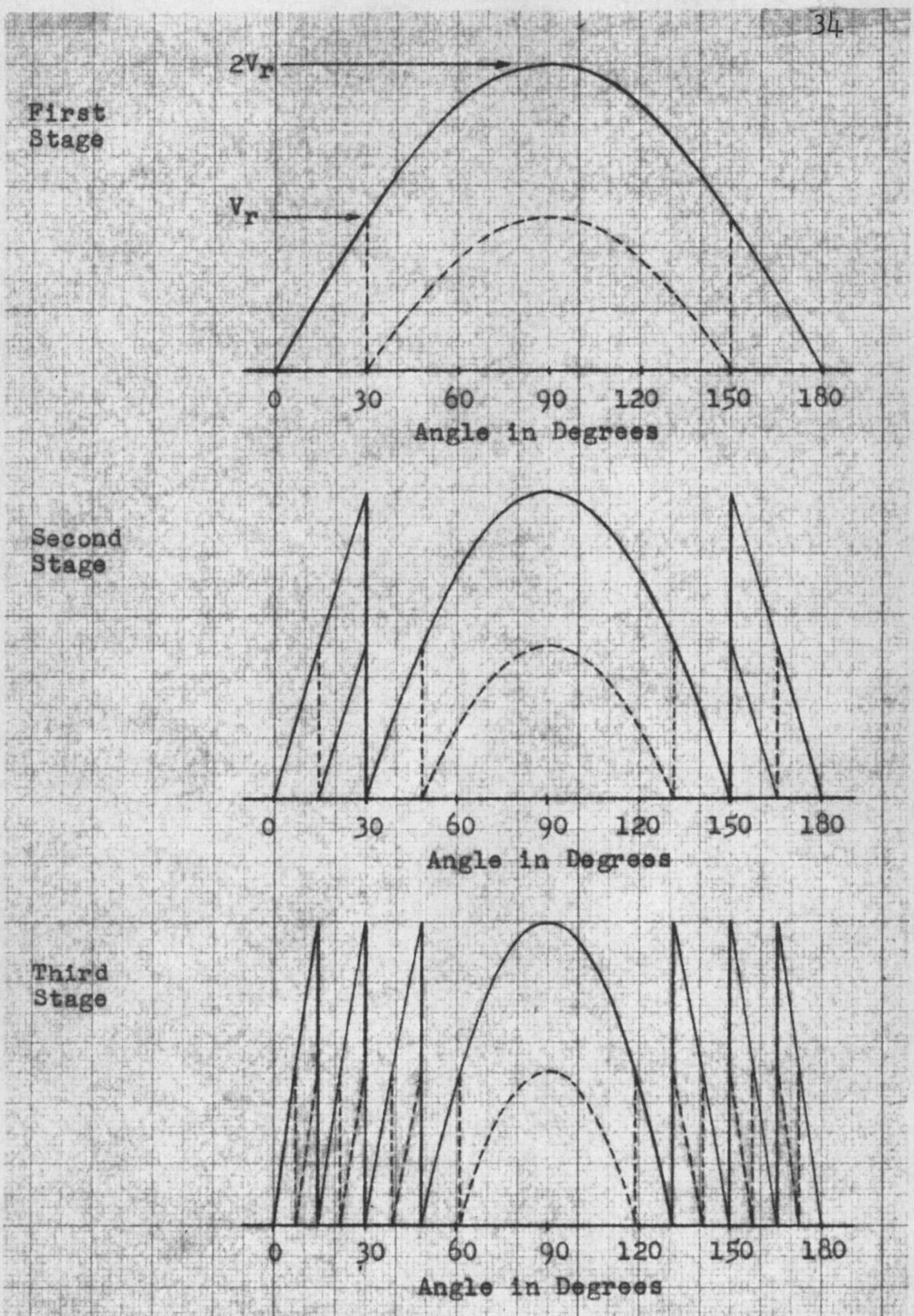


Fig. 30 Consecutive Inputs (solid) and Outputs (dotted) of Three Cascaded Coding Units

tenth harmonic. Therefore, the frequency response of the last coding unit in a string of ten such units would have to be about 33,000 times higher than the highest frequency component present in the input.

The situation isn't really quite as bad as this figure of 33,000 indicates because in general the input signal will not be varying so rapidly that all of the coding units will be changing state in succession.

Obviously the accuracy of the coding units can decrease from a value of 1 part in 1024 for the first unit to 1 part in 2 for the last unit in a string of ten units.

A parallel can be drawn between the gain-band width product associated with normal amplifier circuits and a conversion rate-accuracy product associated with these coding units. It is easily seen that the conversion rate must approximately double for each successive stage while the accuracy of each successive stage can be half that of the preceding stage.

POSSIBLE IMPROVEMENTS

As the coding circuit now stands it consists of three major segments---the logic circuits, the switching circuit, and the times-two amplifier circuit. Each of these blocks can stand considerable improvement which will result in a higher speed encoder.

The amplifier circuit could be made to operate at high frequencies by using higher frequency transistors and compensation networks commensurate with these higher frequency transistors. Improvements in temperature characteristics would also be desirable.

The switching circuit as it is has practically no temperature stabilization. Also, there is a considerable pure delay time associated with its operation which limits its maximum repetition rate to about 250 kc. The rise and fall times of the switch output do not presently have any effect on the speed of operation of the coding unit but if the circuit is otherwise speeded up then these response times would become important. Higher frequency transistors would improve the operation of this circuit as well as the amplifier circuit.

Finally, there is the problem of speeding up the logic circuits. In order to make the logic circuits very efficient, large AND and OR gate resistors must be used; this limits the gate operating speeds because of the sizeable effect of shunt capacity. It seems that the only way to speed up the logic circuits is to make them "lossy" in a way that would cancel the loss effects. Maybe this is possible. Following are some transfer functions defined as shown:

K_a = AND gate transfer function

K_r = reference string transfer function

K_o = OR gate transfer function

K_{ef} = emitter follower transfer function

In addition, there are the following voltage level changes to be defined as shown:

V_a = voltage rise across the AND gate

V_r = voltage drop across the reference string

V_o = voltage drop across the OR gate

V_{ef} = voltage drop across the emitter follower

The following equations can now be written relating the input voltage to the output voltage (see Figure 14):

(for V_{in} less than V_r)

$$(V_{in} K_a K_o + V_a K_o - V_o) A = V_{out} \quad \text{and}$$

(for V_{in} greater than V_r)

$$(V_{in} K_r K_{ef} K_o - V_r K_{ef} K_o - V_{ef} K_o - V_o) A = V_{out}$$

Subtracting the last of these equations from the first yields the true reference voltage:

$$V_{in} (K_a K_o - K_r K_{ef} K_o) + V_a K_o + V_r K_{ef} K_o + V_{ef} K_o = V_{r_{actual}}$$

$$V_{in} (K_a - K_r K_{ef}) + V_a + V_r K_{ef} + V_{ef} = V_{r_{actual}} / K_o$$

Therefore, making $(K_a - K_r K_{ef})$ equal to zero makes $V_{r_{actual}}$ independent of V_{in} and constant. Losses incurred by V_{in} passing through the logic circuits can be made up by increasing the gain of the so-called times-two amplifier so that

$(A_{actual})(K_a\ K_o) = (A_{actual})(K_r\ K_{ef}\ K_o) = 2$

$(K_a - K_r\ K_{ef})$ could be made to equal zero by adding resistance in series with the signal input diode on the AND gate.

The accuracy problem of the logic circuits has now changed from one of making the dynamic resistance of the diodes negligible to one of making the change of this dynamic resistance negligible. This means that smaller resistors can be used which will increase circuit speed by a factor of ten while at the same time making possible a reduction of the OR and AND gate supply voltages by an order of magnitude.

CONCLUSION

The feasibility of this coding circuit has been illustrated both in theory and actuality. Through proper circuit design it seems entirely within the realm of possibility to achieve sufficient accuracies to warrant ten binary place conversion.

While the maximum conversion rate of the coding circuit tested was not exceptionally high, many improvements could be made which would increase the maximum conversion rate such as using higher frequency transistors and diodes with a lower forward dynamic resistance (which would allow use of smaller pull-up resistors resulting in an increase of the AND and OR gate operating speeds). Also, it is

possible that "lossy" AND and OR gates and a "lossy" reference string could be used in which the loss effects were cancelled out. The advantage of using "lossy" circuits is that resistors could be smaller which would minimize the speed-reducing effect of shunt capacity.

The repetition rate of the input signal was about 10 kc; the output signal had a fundamental component of about 20 kc and important harmonics up to about 200 kc all of which were fairly well reproduced.

Observations made with a Tektronix 531 oscilloscope indicated visually that the accuracy of the coding device exceeded the accuracy of any available instruments (about 1%). Accuracy comparisons were made by superimposing two signals simultaneously (by using a two-channel, alternate-sweep preamplifier with the Tektronix oscilloscope) and comparing their amplitudes or slopes as appropriate. Low intensities and optimum focus and astigmatism adjustments were used for making these comparisons.

One of the main advantages of the circuit is that inexpensive, non-precision components are used throughout.

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APPENDIX

THE TEST-SIGNAL GENERATOR

Following is a circuit of the test-signal generator used for examining the operation of the coder circuit. The sawtooth output of this circuit is quite linear as a result of using the emitter-follower feedback circuit. There is no frequency adjustment provided although varying the amplitude of the signal (by adjusting the interbase voltage of the unijunction transistor) causes the output repetition rate to vary. At a repetition rate of approximately 10 kc, the sawtooth falltime is about 4% of the risetime. The output reference was positive about 1.5 volts with respect to ground; the 1.5 volt battery in the output circuit remedied this situation.

Fig. X1.

The Sawtooth Generator Circuit