ABSTRACT OF THE THESIS OF

Yung-jin(Jin) Gang for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 23, 1998.

Title: ULTRA LOW VOLTAGE DRAM CURRENT SENSE AMPLIFIER WITH BODY BIAS TECHNIQUES

Redacted for Privacy

Abstract approved: Leonard Forbes

The major limiting factor of DRAM access time is the low transconductance of the MOSFET's which have only limited current drive capability. The bipolar junction transistor(BJT) has a collector current amplification factor, β, times base current and is limited mostly by the willingness to supply this base current. This collector current is much larger than the MOSFET drain current under similar conditions. The requirements for low power and low power densities results in lower power supply voltages which are also inconsistent with the threshold voltage variations in CMOS technology, as a consequence at least pulsed body bias or synchronous body bias will probably be utilized. Given that of the CMOS body will be driven or the CMOS gate and body connected a BJT technique is proposed for ultra low voltages like Vdd=0.5. Utilizing present CMOS process technology good results can be achieved with ultra low power using gate-body connected transistors and a current sense amplifier.

ULTRA LOW VOLTAGE DRAM CURRENT SENSE AMPLIFIER WITH BODY BIAS TECHNIQUES

by

Yung-jin(Jin) Gang

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Completed November 23, 1998
Commencement June 1999

Doctor of Philosophy thesis of Yung-jin(Jin) Gang presented on November 23, 1998

APPROVED: Redacted for Privacy

Major Professor, representing Electrical and Computer Engineering

Redacted for Privacy

Head of Department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Redacted for Privacy

Yung-jin(Jin) Gang, Author

ACKNOWLEDGMENTS

I would like to express my deepest gratitude to my advisor Professor Leonard Forbes. His contribution to this thesis has been not only through his advice, patience, many hours of detailed discussion, but also through his continuous encouragement and support during the course of this research.

I wish to thank Professor Ben Lee, David G. Ullman, S. Subramanian, Vijai K. Tripathi, Shih-Lien Lu, and Andreas Weisshaar for being my committee members. I appreciate the entire electrical engineering faculty for their wisdom.

I also wish to thank Dr. Kye-hwan Oh who is the vice-president in Hyundai Electronics Industries for his constant encouragement and support during my study in USA.

Thanks to Professor Yeon-gon Koo in Hong-ik University and Hee-chang Kang in National Seoul Industrial University for their encouragements.
The financial support of Hyundai Electronics Industries was greatly appreciated.

Finally, I would like to give special thanks to my parents, my sister Gi-hyung, and my wife Mi-duk and two sons Kye-wol and Han-wol for their love and sacrifice in all aspect of my study life in USA.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES(Continued)

LIST OF FIGURES (Continued)

LIST OF FIGURES(Continued)

LIST OF TABLES

ULTRA LOW VOLTAGE DRAM CURRENT SENSE AMPLIFIER WITH BODY BIAS TECHNIQUES

1. INTRODUCTION

Various types of lateral transistors have been historically described and utilized in CMOS technology [1-9]. Recently the action of newer devices has been described in new terms and a more careful distinction made between the different types of transistor action possible. Both gate-body connected MOS transistors [5, 6] and gated lateral bipolar transistors have been described [7, 8]. The term gate-body connected transistors is used here [5, 6] to describe vertical [7, 8] or other device structures where the gate of the MOS is connected to the backgate or body. Applying the gate voltage to the body serves primarily to change the threshold voltage of the MOS transistor and MOS transistor action is dominant. Other structures are possible where the gate and base are common and the bipolar transistor and MOS transistor are in parallel but the bipolar current is in dominant.

In a gated lateral transistor not only the structures but also the operation is merged and most current flows along the surface under the gate in either MOS or bipolar operation. In the case of a gated lateral bipolar transistor at low voltages around threshold, V_T, they can act as gated-body connected MOS transistors, at higher input voltages, V_T or more, the bipolar action can dominate and they are more appropriately described as gated lateral bipolar transistors [1].

In this paper the gate-body connected MOSFET (GB-MOS) and gate-base-body connected MOSFET (GBB-MOS) are described. The word line access time characteristics of DRAMs using a clamped bit line current sense amplifiers [27] with GB-MOS and GBB-MOS are evaluated with Vdd=0.5 V and 0.6V. Finally the proposed gated lateral BJT current sense amplifier for DRAMs using GBB-MOS transistors was simulated and shows good results under low power supply voltages.

2. THRESHOLD VOLTAGE ADJUSTMENT

For zero substrate bias, the threshold voltage V_{TO} is expressed as follows.

$$V_{TO} = \Phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \tag{2.1}$$

For nonzero substrate bias, the depletion charge density term must be modified to reflect the influence of V_{SB} upon that charge, resulting in the following generalized threshold voltage expression.

$$V_{TO} = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} \tag{2.2}$$

The generalized form of the threshold voltage can be written as

$$V_{TO} = \Phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_B - Q_{BO}}{C_{OX}} = V_{TO} - \frac{Q_B - Q_{BO}}{C_{OX}} \tag{2.3}$$

The threshold voltage differs from V_{TO} only by an additive form. This term is a simple function of the material constants and of the source-to-substrate voltage V_{SB}

$$\frac{Q_B - Q_{BO}}{C_{OX}} = -\frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{OX}} \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{2.4}$$

Thus, the most general expression of the threshold voltage V_T can be found as follows.

$$V_T = V_{TO} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{2.5}$$

where $\gamma = \dfrac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{OX}}$ is the body effect coefficient.

For the NMOS case, ϕ_F, Q_B, and Q_{BO} are negative but γ and V_{SB} are positive. For the ultra low supply voltage, V_T should be reduced to a appropriate level which depends on the noise margin. This can be accomplished if V_{SB} is made minus (positive backgate bias) instead of the conventional negative value. This can be implemented by connecting the gate and body together. Fig. 2.1 shows the threshold voltage trend due to the body bias by using the scaled model parameters. It yields V_T =0.18 v for the Vsb=0.5 V with Vdd=0.5V. Fig. 2.2 shows the straight line relationship we can easily recognize. The data of Fig. 2.1 and Fig. 2.2 were obtained the level=3 HSPICE [30] simulations.

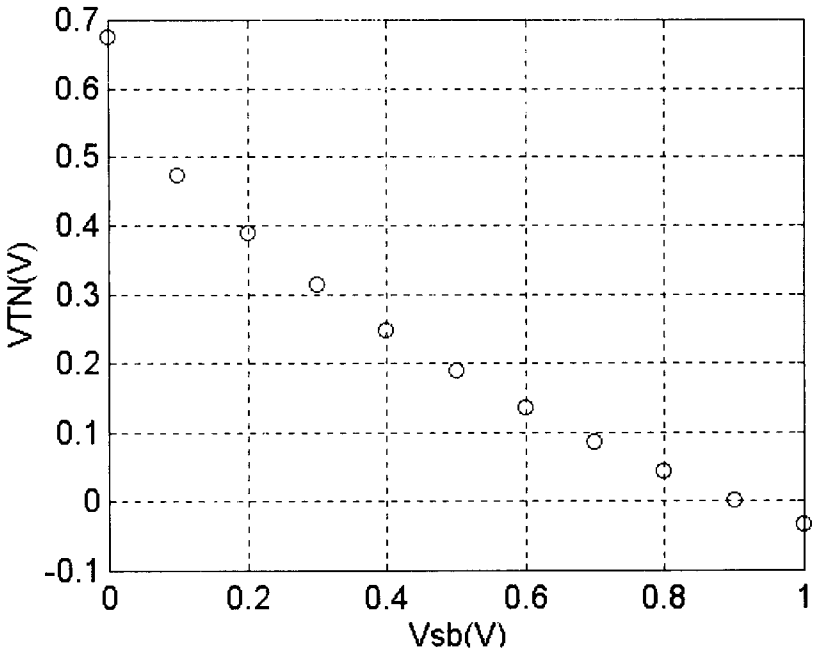


Fig. 2.1 VTN vs. forward bias Vsb

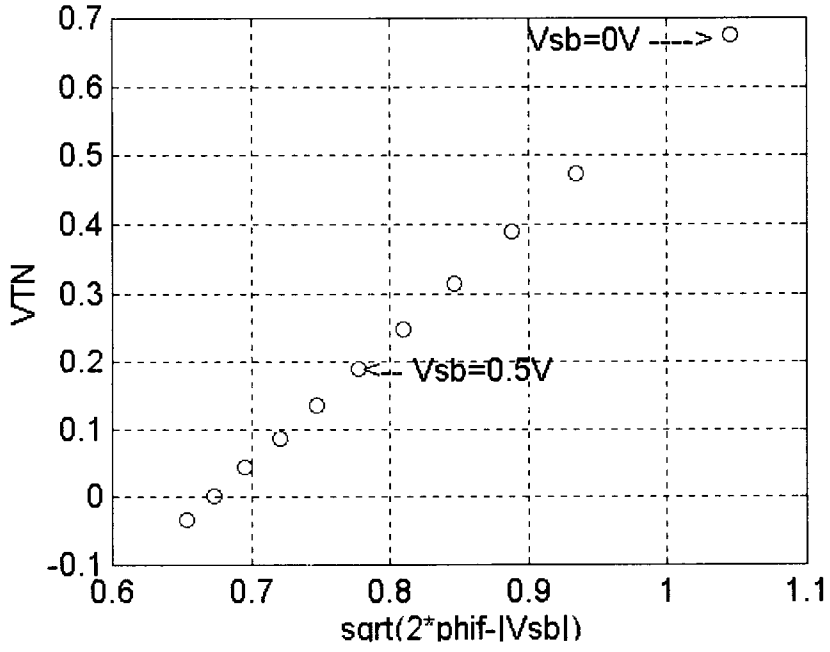


Fig. 2.2 VTN vs. $\sqrt{2 \cdot \phi_F - |V_{SB}|}$

3. DEVICE MODEL

We have used the MOSFET LEVEL 3 model parameters from the n-well $0.6\mu m$, Vdd=5V technology of MOSIS. Table 1a and 1b represent the original values and we have scaled these down to $0.2\mu m$ as shown in Table 2a and 2b. The $0.2\mu m$ is consistent with 64 Mega bit DRAM technology and $f_T = 5GH_Z$ can be obtained with that technology. When scaling, a modified scaling was used with both the constant field and the constant voltage scaling [31] employed together to manipulate the V_T to an appropriate level. For example, the value of NSUB of NMOS was determined based on the γ (body coefficient)=1.8 set by circuit requirements. It did not follow the full scaling rule because the sub-micron scaling has very complicated characteristics. The scaled down model for $0.2\mu m$ is dependent on the physical, electrical, and process characteristics. For example, to find a value of CJ with zero bias potential, x_d, was calculated as follows:

$$x_d = \sqrt{\frac{2\varepsilon_{Si}(N_A + N_D)}{qN_A N_D} \cdot \phi_0} \qquad (3.1)$$

Then

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A} \cdot \phi_0} \qquad (3.2)$$

$$= \sqrt{\frac{2 \cdot 11.7 \cdot 8.85x10^{-12}}{1.6x10^{-19} \cdot 7.62x10^{18}} \cdot 0.99} = 12.3x10^{-9}m \qquad (3.3)$$

therefore $\mathrm{CJ} = \frac{\varepsilon_{Si}}{x_d} = 80 \times 10^{-4} F/m^2$. (3.4)

To find CJSW value, the sidewall parameters such as $\phi_{0,SW}$, $N_{A,SW}$ are not given in this model parameters, thus an approximation is used:

$$\text{CJSW} = \text{CJ} * \text{XJ} = 80\times10^{-4}\cdot 6.67\times10^{-8} \tag{3.5}$$

$$= 80\times10^{-4}\cdot 6.67\times10^{-8} = 5.33\times10^{-10}\ F/m\,. \tag{3.6}$$

Notice that these are enough level 3 model parameters for design by hand calculations. Table 2a and 2b show the $0.2\mu m$ parameters which have been scaled down. Notice that KP= μC_{OX} is one of the level 3 HSPICE parameters and the CJ value for $0.2\mu m$ is increased by 8.6 times the original $0.6\mu m$ value because of the decreased junction depletion width. If the parameter is not specified in the model, HSPICE calculates the value automatically. An ideal model was used for bipolar junction transistor in Table. 3. A more accurate model will be made later including the parasitic vertical BJT's [1] and described in chapter 6.

PB=0.99	PHI=0.700000	TOX=9.4000E-09	XJ=0.2E-06
TPG=1	VTO=0.6746	DELTA=1.148	LD=3.4510E-08
KP=1.8217E-04	UO=495.9	THETA=1.7960E-01	RSH=3.2470E+01
GAMMA=0.5383	NSUB=1.178E+17	NFS=7.1500E+11	VMAX=2.50E+05
ETA=2.1880E-02	KAPPA=4.239E-01	CGDO=9.00E-11	CGSO=9.00E-11
CGBO=3.744E-10	CJ=5.79E-04	MJ=0.611	CJSW=2.00E-11
MJSW=0.621			

Table. 1a N-well 0.6u NMOS with Vdd=5V model parameters

PB=0.89	PHI=0.700000	TOX=9.4000E-09	XJ=0.2E-06
TPG= -1	VTO= - 0.8887	DELTA=1.006	LD=1.0920E-08
KP=4.5773E-05	UO=124.6	THETA=6.902E-02	RSH=1.9550E-01
GAMMA=0.4097	NSUB=6.8230E+16	NFS=6.5000E+11	VMAX=1.00E+06
ETA=4.2420E-02	KAPPA=8.613E+00	CGDO=9.0000E-11	CGSO=9.0000E-11
CGBO=3.5362E-10	CJ=9.30E-04	MJ=0.485	CJSW=2.32E-10
MJSW=0.213			

Table. 1b N-well 0.6u PMOS with Vdd=5V model parameters

PB=0.99	PHI=0.700000	TOX=40E-10	XJ=6.667E-8
TPG=1	VTO=0.6746	DELTA=0.3827	LD=1.1503E-08
KP=428.1E-06	UO=495.9	THETA=0.0599	RSH=10.8233
NSUB=7.62E+18	NFS=2.3833E+11	VMAX=8.3333E+04	ETA=0.0073
KAPPA=0.1413	CGDO=3.0E-11	CGSO=3.0E-11	CGBO=1.2480E-10
CJ=80E-04	MJ=0.611	CJSW=5.33E-10	MJSW=0.621
IS=1E-18			

Table. 2a N-well 0.2u NMOS with Vdd=0.5V model parameters

PB=0.89	PHI=0.700000	TOX=40E-10	XJ=6.667E-8
TPG=-1	VTO=-0.6746	DELTA=0.3353	LD=0.3640E-08

KP=1.3660E-04	UO=124.6	THETA=0.0230	RSH=0.0652
NSUB=7.62E+18	NFS=2.1667E+11	VMAX=3.3333E+05	ETA=0.0141
KAPPA=2.8710	CGDO=3.0E-11	CGSO=3.0E-11	CGBO=1.1787E-10
CJ=80E-04	MJ=0.485	CJSW=5.33E-10	MJSW=0.213
IS=1E-18			

Table. 2b N-well 0.2u PMOS with Vdd=0.5V model parameters

IS=1E-18	BF=100	BR=100	VAF=90V
RB=100	TF=0.03E-9	TR=0.03E-9	

Table. 3 Ideal BJT model parameters

4. GATE-BODY CONNECTED MOSFET

Fig.4.1 and Fig.4.2 represent the I-V characteristic for the gate-body connected NMOS(GB-NMOS) and PMOS(GB-PMOS). For GB-NMOS, the minimum size W/L=0.4 μ /0.2 μ was used, while the GB-PMOS had W/L=1.6μ/0.2μ.

It shows good I-V characteristics like a conventional gate and body MOSFET with separated.

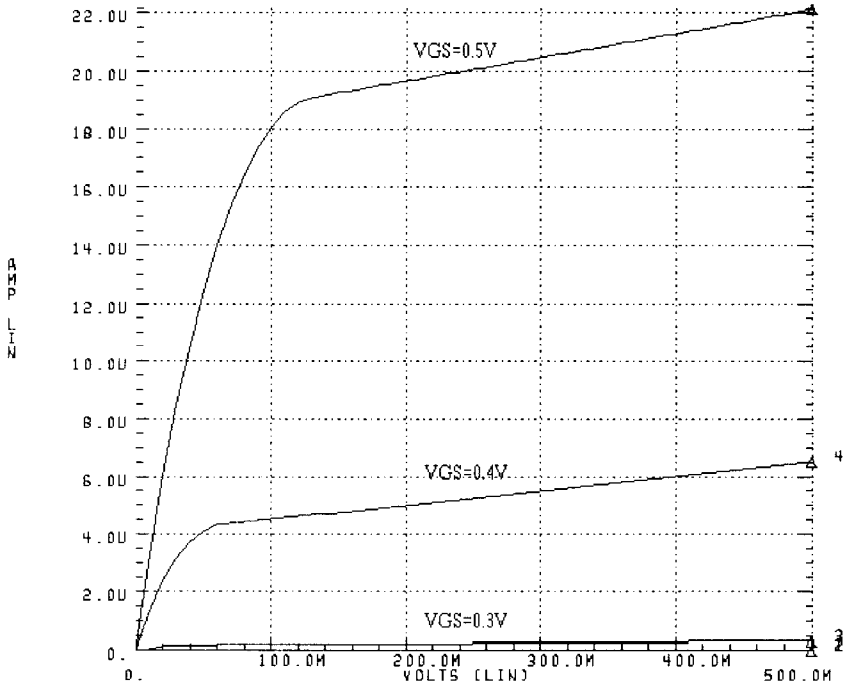


Fig. 4.1 I-V curve of gate body connected NMOS(W/L=0.4μ/0.2μ)

As shown in Fig. 4.1 the curve for Vgs=0.5V has a good characteristic even though VTN=0.6746 as shown in Table2a.

As illustrated in Fig. 2.1, VTN for Vgb=Vsb(gate to body forward bias) = 0.5V shows 0.2V while VTN for Vgb=0.4V represents 0.25V. These VTN values are good threshold voltages for the ultra low power supply voltages like Vdd=0.5V. The following Fig. 4.2 shows the good performance for the VTO=-0.6746 as shown in Table. 2b.

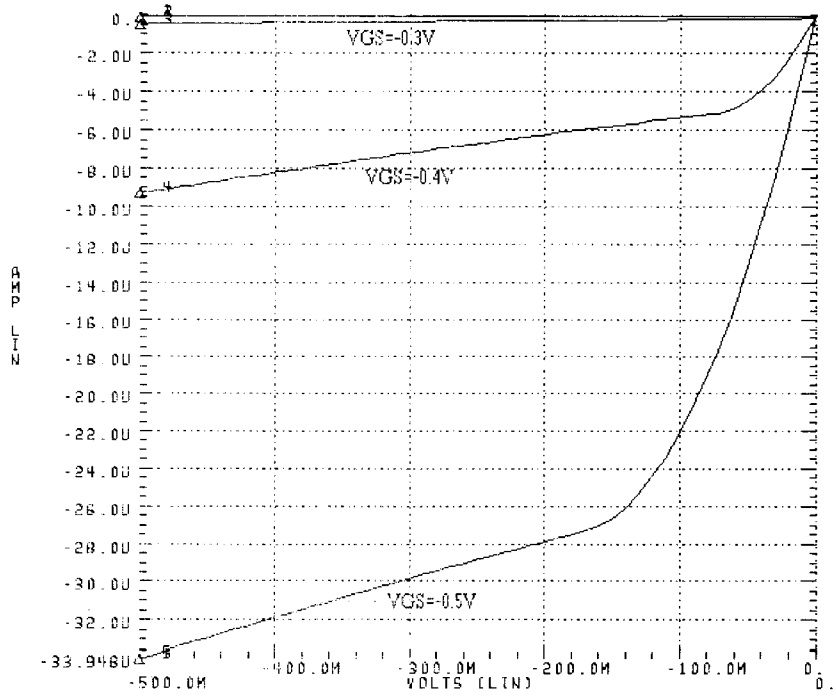


Fig.4.2 I-V curve of gate body connected PMOS(W/L=1.6μ / 0.2μ)

5. MAJOR SENSE AMPLIFIER STRUCTURE

5.1 MEMORY CELL

5.1.1 PLANAR MEMORY CELL

Fig. 5.1.1 shows the planar type memory cell in which a silicide is formed on the top of the wordline polysilicon. A metal bitline is formed on the active drain of the transistor. One plate of the capacitor is made by the n+ active and the other side of it is poly-I. This planar type is an easier process but occupies a large area in order to have a high capacitance. Poly-II acts as a wordline and on the top of it, a silicide is deposited to reduce the poly resistance. The present technology that utilizes the advanced triple well for the high density Giga DRAM has a four levels of poly and two levels of metal used for Vdd and active contact.

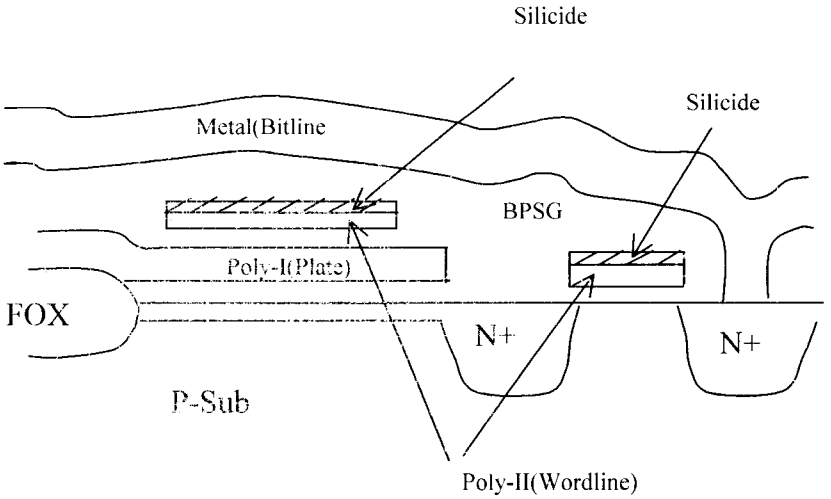


Fig. 5.1.1 Planar memory cell

5.1.2 STACKED MEMORY CELL

The following Fig. 5.1.2 illustrates a stacked memory cell. In Fig. 5.1.2, a wordline consists of the first polysilicon or polycide(poly+silicide). The second level polysilicon is a storage node and the third polysilicon is a Vcc/2 plate. Most of stacked memory cells have fin type capacitors to make a wide plate area resulting in a large capacitance within the limited dimensions. The storage node and bitline contact are done by SAC(**S**elf **A**ligned **C**ontact) polysilicon methods. A LTO(**L**ow **T**emperature **O**xide) is used as isolation between the gate polysilicon and nitride where the nitride is deposited for protection against a etch back of the plate poly.

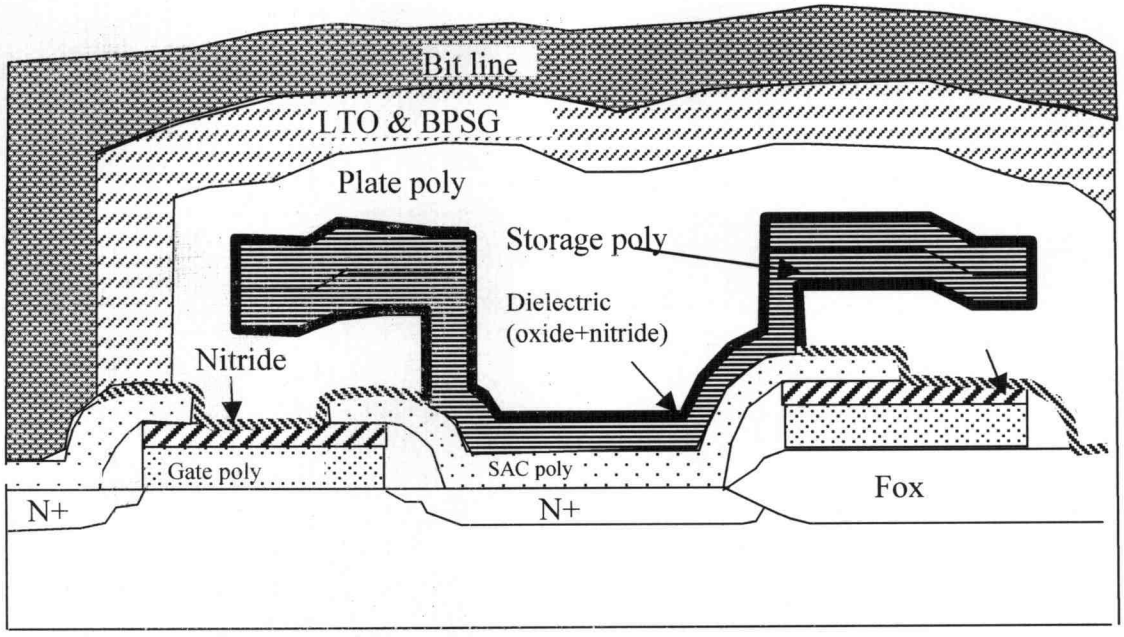


Fig. 5.1.2 Stacked memory cell

5.1.3 TRENCH MEMORY CELL

Fig. 5.1.3 illustrates an electrical memory cell representation and the other type of memory cell which uses trench capacitors, as shown in Fig. 5.1.4. Trench capacitors are formed in the silicon substrate after deep holes are etched into the wafer. The storage node is created by a doped polysilicon plug that is formed in the hole after deposition of the capacitor dielectric. Contact between the storage node plug and the transistor drain is usually made through a poly strap. With most trench capacitor designs, the substrate serves as the common node connection to the capacitor,

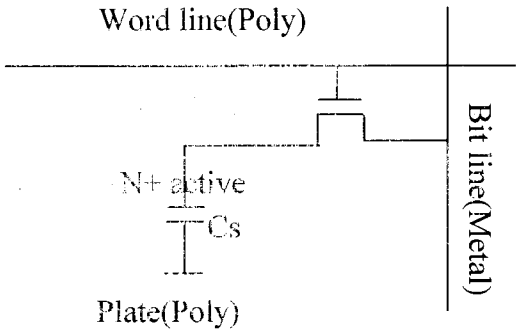


Fig. 5.1.3 Memory bit

preventing the use of +Vcc/2 bias and thinner dielectric. The substrate is heavily doped around the capacitor to reduce resistance and improve the capacitor's CV characteristics. An advantage to trench designs is that capacitance can be increased by merely etching a

deeper hole into the substrate. Furthermore, the capacitor does not add stack height to the design, an attribute that greatly simplifies contact technology. The disadvantage to trench capacitor technology is the difficulty associated with reliably building capacitors in deep silicon holes and contacting trench capacitors to transistor drain terminals. Also it may be suffered from random bit fails coming from the large area of ONO (**O**xide-**N**itride-**O**xide) as the dielectric area.

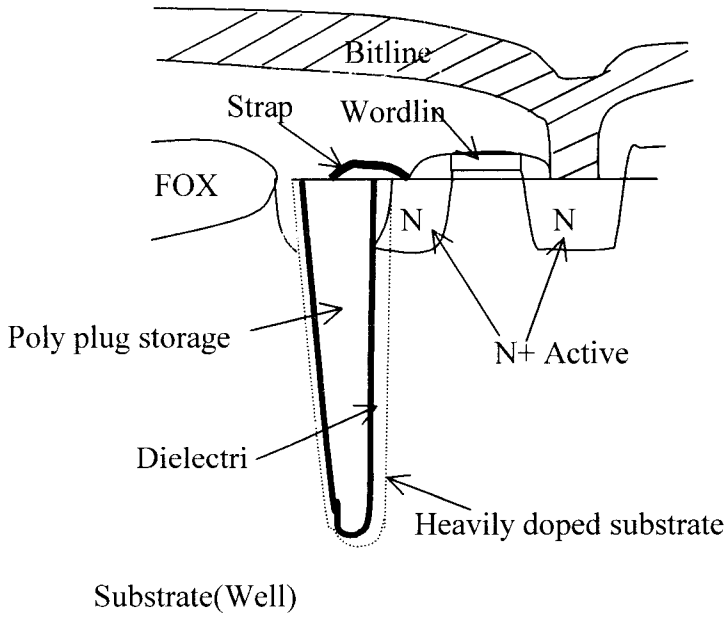


Fig. 5.1.4 Trench memory cell

5.2 FEATURE SIZE

The memory bit shown in Fig. 5.2 is by definition an eight-square feature $(8F^2)$ cell [32]. Feature size in this case should refer to the minimum realizable process dimension, but in fact refers to a dimension that is half of the wordline or bitline pitch. A $0.25\,\mu m$ process having wordline and bitline pitches of $0.6\ \mu m$ yields an memory bit size that is $8 \cdot (0.3\mu m)^2 = 0.72\,\mu m^2$. The $(8F^2)$ cell can be understood with the help of Fig. 5.2.1. A box is drawn around the memory cell to show the cell's outer boundary. Along the x-axis, this box includes one-half bitline contact feature, one wordline feature, one capacitor feature, one field poly feature, and one-half field poly space feature, totaling four features. Along the y-axis, the box contains two one-half field oxide features and one active area feature, totaling two features. Therefore, the area of the memory bit is $4F \cdot 2F = 8F^2$. The folded bit line array architecture shown in Fig. 5.3 always produces an $(8F^2)$ memory bit. This results from the fact that each wordline connects crosspoints with an memory bit transistor on every other bitline and must pass around memory bit transistors as field poly on the remaining bitlines. The field poly in each memory bit cell adds two square features to what would have otherwise been a $(6F^2)$cell. Although the folded array yields a cell that is 25% larger than other array architectures, it produces superior signal-to-noise performance, especially when combined with some form of bit line twisting.

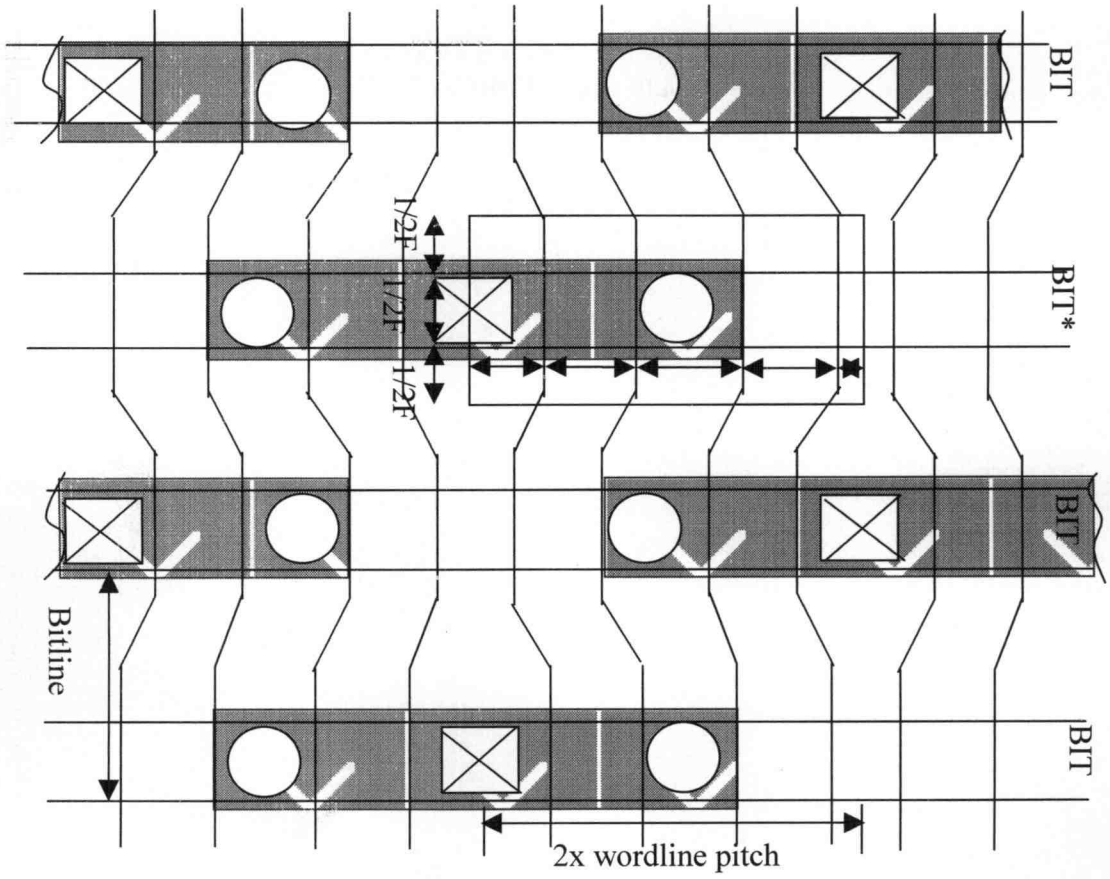


Fig. 5.2.1 Layout to show a $8F^2$ memory

5.3 CONVENTIONAL VOLTAGE SENSE AMPLIFIER

5.3.1 EQUILIBRATION AND BIAS CIRCUITS

The sense amplifier actually consists of two inverters cross-coupled together, isolation transistors, devices for bitline equilibration and bias, one or more NMOS sense amplifiers, one or more PMOS sense amplifiers, and devices connecting selected bitlines to I/O signal lines. The following Fig. 5.3.1 consists of two inverters cross-coupled together. Before the sensing the difference, PRE clock is maintained high to make both

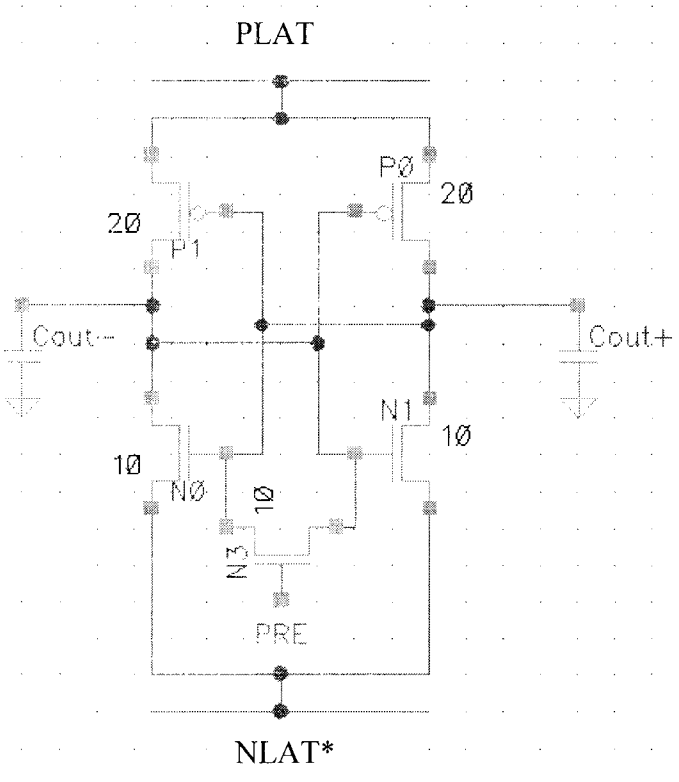


Fig. 5.3.1 Conventional voltage sense amplifier

outputs the same level(usually Vcc/2) before the sensing operation. PRE becomes low and one output goes up while the other output is coming down at the same time depending on the initial voltage difference.

All of the circuits along with the wordline driver circuits are called pitch cells. This designation comes from the requirement that the physical layout for these circuits is constrained by the bitline and wordline pitches of an array of memory bits. For example, the sense amplifiers for a specific bitline pair are generally laid out within the space of four bitlines. With one sense amplifier for every four bitlines, this is commonly referred to as quarter pitch or four pitch.

The first elements of sense amplifier are the equilibration and bias circuits. The bitlines precharge at Vcc/2 volts prior to cell access and sensing. It is vitally important to the sensing operation that both bitlines, which form a column pair, are at the same voltage before the wordline is fired. Any offset voltage appearing between the pair directly reduces the effective signal produced during the access operation. Equilibration of the bitlines is accomplished with one or more NMOS transistors connected between the bitline conductors; NMOS is used because of its higher drive capability and the resulting faster equilibration. An equilibration transistor, together with bias transistors, is shown in Fig. 5.3.2. The gate terminal is connected to a signal called EQ (Equilibrate). EQ is held to Vcc whenever the external row address strobe signal /RAS is high which indicates an inactive or precharge state for the DRAM. After /RAS has fallen, EQ transitions low,

turning the equilibration transistor off just prior to any wordline firing. EQ will again transition high at the end of a /RAS cycle to force equilibration of the bitlines.

The equilibration transistor is sized large enough to ensure rapid equilibration of the bitlines to prepare the part for a subsequent access.

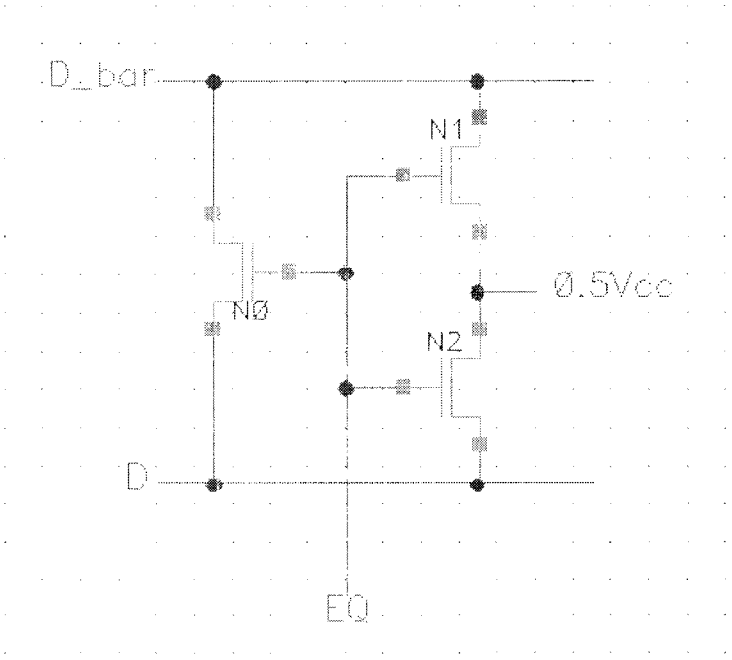


Fig. 5.3.2 Equilibration and bias circuit

As shown in Fig. 5.3.2, two more NMOS transistors accompany the EQ transistor to provide a bias level to Vcc/2 volts. These devices operate in conjunction with equilibration to ensure that the bitline pair remains at the prescribed voltage for sensing.

Normally, bitlines that are at Vcc and ground equilibrate to Vcc/2 volts during the precharge cycle. The bias devices ensure that this occurs and also guarantee that the bitlines remain at Vcc/2, despite leakage paths that would otherwise discharge them. Again, for the same reasons as for the equilibration transistor, NMOS transistors are used. Most often, the bias and equilibration transistors are integrated to reduce their overall size. Vcc/2 volt precharge is used on most modern DRAMs, because it reduces power consumption and read-write times and improves sensing speed. Power consumption is reduced, because Vcc/2 precharge voltage can be obtained by equilibrating the bitlines which are at Vcc and ground, respectively at the end of each cycle. The charge-sharing between the bitlines produces Vcc/2 without additional Icc current. A layout for the equilibration and bias circuits is shown in Fig. 5.3.3.

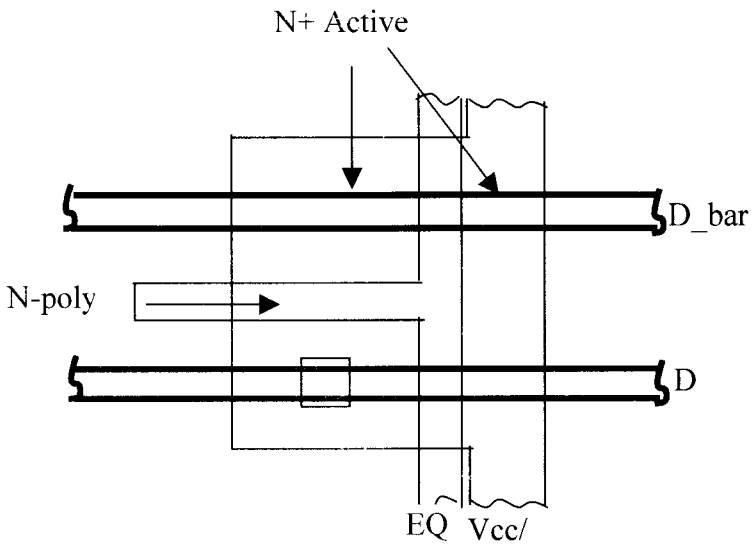


Fig. 5.3.3 Equilibration and bias circuit layout

5.3.2 ISOLATION DEVICES

Isolation devices are important to the sense amplifier circuits. These devices are NMOS transistors placed between the array bitlines and certain sense amplifier components because a multitude of variations are possible for the sense amplifier block. Isolation transistors are physically located on both ends of the sense amplifier layout. In quarter-pitch sense amplifier designs, there is one isolation transistor for every two bitlines. Although this is twice the active area width and space of an array, it nevertheless sets the limit for isolation processing in the pitch cells. The isolation devices provide two functions. First if the sense amps are positioned between and connected to two arrays, they electrically isolate one of the two arrays. This is necessary whenever a wordline fires in one array, because isolation of the second array reduces the bitline capacitance driven by the sense amplifiers, thus speeding read-write times, reducing power consumption, and extending refresh for the isolated array. Second, the isolation devices provide resistance between the sense amplifier and the bitlines. This resistance stabilizes the sense amplifiers and speeds up the sensing operation by somewhat isolating the highly capacitive bitlines from the low capacitance sense nodes. Capacitance of the sense nodes between isolation transistors is generally less than 15fF, permitting the sense amplifier to latch much faster than if it were solidly connected to the bitlines. The isolation transistors slow write back to the memory cell, but this is far less of a problem than initial sensing.

5.3.3 INPUT/OUTPUT TRANSISTORS

The input/output transistors allow data to be read from and written to specific bitline pairs. A single I/O transistor is connected to each sense node as shown in Fig. 5.3.3. The outputs of each I/O transistor are connected to I/O signal pairs. Commonly, there are two pairs of I/O signal lines, which permit four I/O transistors to share a single column select (CSEL) control signal. DRAM designs employing two or more metal layers run the column select lines across the arrays in either metal2 or metal3. Each column select can activate four I/O transistors on each side of an array, permitting the connection of four bitline pairs (columns) to peripheral data path circuits. The I/O transistors must be sized carefully to ensure that instability is not introduced into the sense amplifiers by the I/O bias voltage or remnant voltages on the I/O lines. Although designs vary significantly as to the numerical ratio, I/O transistors are designed to be two to eight times smaller than the Nsense-amplifier transistors. This is sometimes referred to as beta ratio. A beta ratio between five and eight is considered standard, although it can only be verified with silicon. Simulations fail to adequately predict sense amplifier instability, although theory would predict better stability with higher beta ratio and better write times with lower beta ratio.

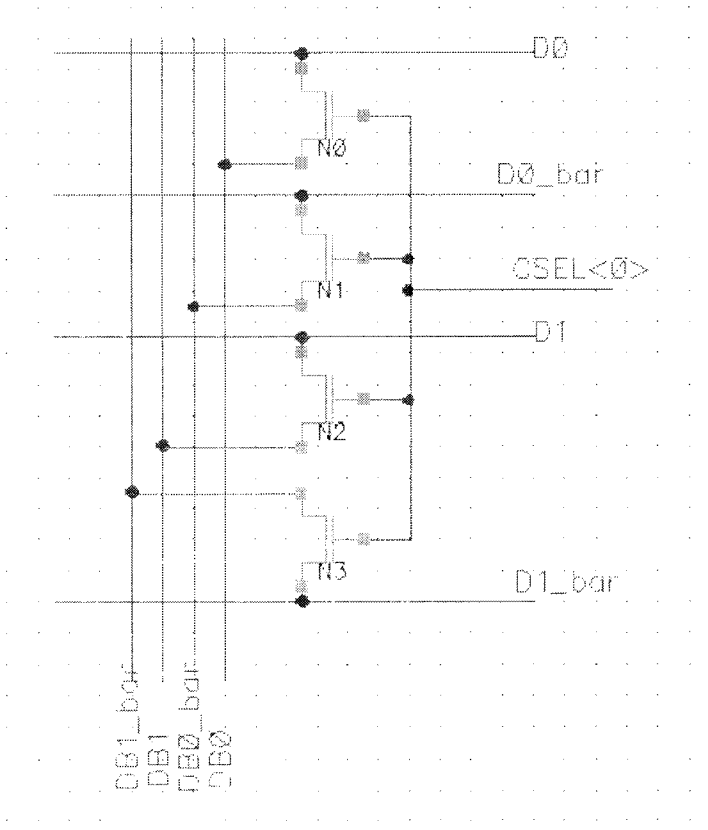


Fig. 5.3.4 I/O transistors

5.3.4 N-LATCH AND P-LATCH SENSE AMPLIFIERS

The two remaining elements to be discussed are the N-latch and the P-latch sense amplifier. These amplifiers, as previously mentioned, work together to detect the access differential signal voltage and drive the bitlines, accordingly to Vcc and ground. As shown in Fig. 5.3.1, the N-latch amplifier consists of cross-coupled NMOS transistors and drives the low potential bitline to ground. Similarly, the P-latch amplifier consists of cross-coupled PMOS transistors and drives the high potential bitline to Vcc. The layout of sense amplifier circuits requires much effort and precision. Because the signal voltage from the cell access is small typically less than 200mV, the sense amplifiers must be designed for correct detection and amplification. Transistor threshold Vth, transconductance, and junction capacitance must be matched within close tolerances for reliable sense amplifier operation. The elements of the design must be symmetrical with one another and duplicated precisely. Coupling to all sources of noise, such as I/O lines and latch signals (NLAT* and PLAT), must be balanced. This is especially true for layout residing inside the isolation transistors.

While the majority of DRAM designs latch the bitlines to Vcc and ground, a growing number are reducing these levels. At first, this may appear contradictory, since writing a smaller charge into the memory cell should produce shorter refresh. Because the bitlines

are never driven to Vcc and ground, however, the benefit is derived from maintaining a negative gate-to-source voltage across non-accessed memory cell transistors. Negative gate-to-source voltages translate to significantly lower subthreshold leakage and longer refresh, despite the smaller stored charge. Designs that implement reduced latch voltages most generally limit only the ground potential. Designated as boosted sense ground designs, they write full Vcc or boosted ground levels into each memory cell. The sense ground level is generally several hundred millivolts above true ground. Whereas junction leakage depletes charge from a stored one level, it tends to increase charge of a stored zero level. Subthreshold leakage on the other hand tends to be slightly worse for a zero level than for a one level due to the higher Vth caused by body effect. This remains true until enough zero charge leaks away to produce a negative Vgs, dramatically reducing subthreshold leakage for zero levels. The net result, though, is that stored one levels leak away faster than stored zero levels. The level retention of "ones" therefore establishes the maximum refresh interval for most DRAM designs. Boosted sense ground helps to extend refresh by reducing subthreshold leakage for stored ones. This is accomplished by ensuring a negative gate-to-source voltage and by reducing the drain-to-source voltage across non-accessed memory cell transistors during active cycles when the bitlines are latched. The benefit of extended refresh from these designs is somewhat diminished by the added complexity of generating the boosted ground level and the fact that the bitlines no longer equilibrate at Vcc/2 volts.

5.3.5 RESPONSE TIME OF VOLTAGE SENSE AMPLIFIER

The following Fig. 5.3.5 represents the response time of a typical voltage sense amplifier. When PRE signal is high the both Vout's are equalized to a half Vdd of same level with the PMOS and NMOS off maintaining the metastability. After PRE goes low the latch is activated and one side is up the other side is down depending on the initial voltage difference between two outputs. The NLAT* signal is activated a little faster than PLAT to reduce the transient current resulting in Ldi/dt inductance noise.

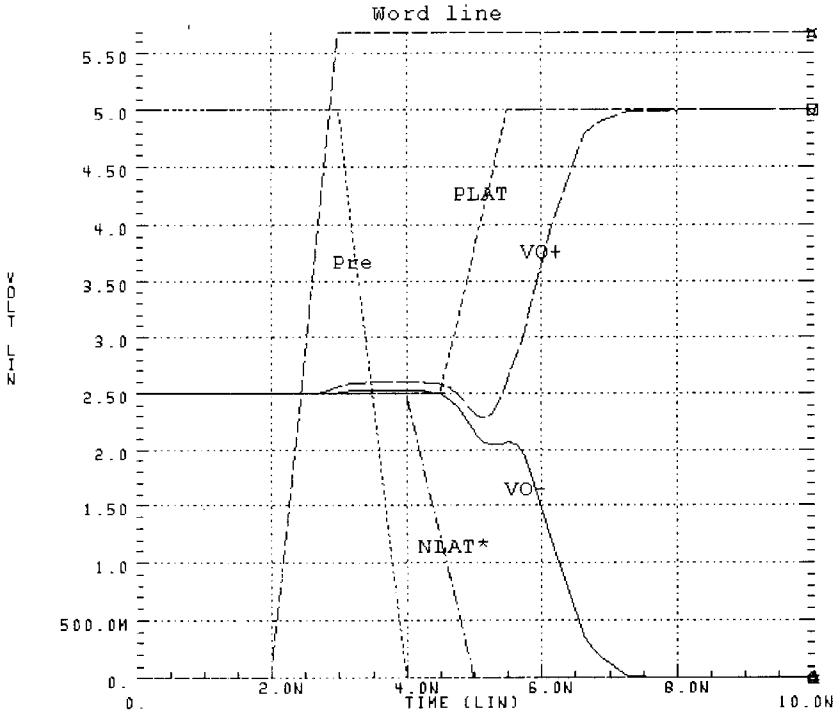


Fig. 5.3.5 Response time of the voltage sense amplifier

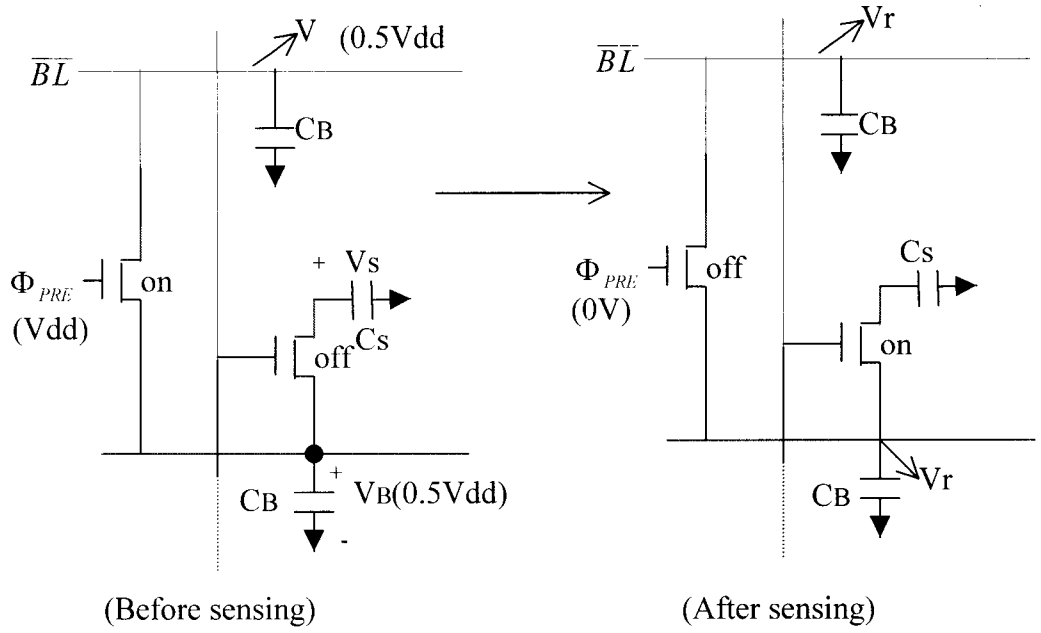


Fig. 5.3.6 Charge sharing when sensing when Vdd=5V

$$C_T = C_B + C_S$$
$$Q_T = 0.5V_{dd} \cdot C_B + V_S \cdot C_S \qquad (5.1)$$
$$V_R = \frac{Q_T}{C_T} = \frac{0.5V_{dd} \cdot C_B + V_S \cdot C_S}{C_B + C_S}$$

Ex) $C_B = 0.6pF$
$C_S = 40fF \qquad V_{dd} = 5V$
$When\ Data = 1(V_S = V_{dd}) \Rightarrow V_R(1) = 2.656V \Rightarrow \Delta V_R(1) = 2.656V - 2.5V = +0.156V$
$When\ Data = 0(V_S = 0V) \Rightarrow V_R(0) = 0.234V \Rightarrow \Delta V_R(0) = 2.344V - 2.5V = -0.156V$

Fig. 5.3.6 shows the charge sharing before and after sensing operation under Vdd=5V. Before sensing, as illustrated in the left figure, total capacitance

$$C_T = C_B + C_S \tag{5.2}$$

where $_B$ is the bitline capacitance and C_S is the cell capacitance.

Total capacitance $Q_T = C_B \cdot 0.5 V_{dd} + C_S \cdot V_S$ (5.3)

Hence the resultant voltage $_R = \frac{Q_T}{C_T} = \frac{C_B \cdot 0.5 V_{dd} + C_S \cdot V_S}{C_B + C_S}$ (5.4)

The example for this calculation is shown in the Eq. (5.1).

5.3.6 SMALL SIGNAL MODELS OF VOLTAGE SENSE AMPLIFIER

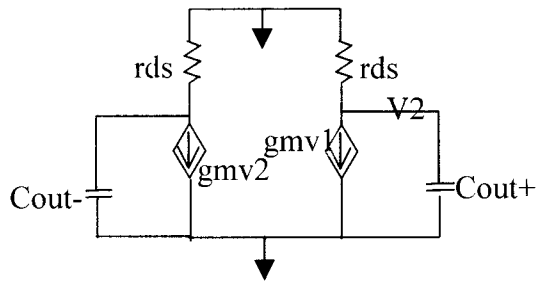


Fig. 5.3.7 Small signal model of the voltage sense amplifier

Fig. 5.3.1 can be represented by small signal models as shown in Fig. 5.3.7. If we assume nMOS is in the saturation region then PMOS should be in the linear region as a latch function. Therefore rds represents the impedance of PMOS as load. In Fig. 5.3.7, Cout consists of Miller cap of Cgd, Cdiffusion and Cbl where Cbl is dominant. Hence, Cout $\approx$ Cbl and the loop gain of the conventional sense amplifier is

$$A_{loop} = \left(\frac{g_m r_{ds}}{1 + s r_{ds} C_{bl}} \right)^2 \tag{5.5}$$

The gain bandwidth is

$$\text{GB} = g_m r_{ds} \cdot \frac{1}{r_{ds} C_{bl}} = \frac{g_m}{C_{bl}} \tag{5.6}$$

Therefore the gain bandwidth mainly depends on the bit line capacitance (C_{bl}).

The larger gain band width product means a faster response time.

5.4 CLAMPED BIT LINE CURRENT SENSE AMPLIFIER

5.4.1 RESPONSE TIME

The clamped bit line current sense amplifier is described in reference [27]. As illustrated in Fig. 5.4.1, Cout includes Miller capacitances of Cgd and Cdiffusion of M1 through M4 while the drains have M6 and M5 are connected to the bit line capacitance. M5 and M6 which are in linear mode act as resistors and drain voltage of the M5 and M6 are clamped to the SAN level. At the end of cycle, M1 through M4 act as a high gain positive feedback amplifier like a conventional sense amplifier. The impedance looking into the source terminal of either M1 or M2 is

$$g_S = g_m + g_{ds} + g_{mbs} \approx g_m$$

In ideal case, $g_{m1,2} = \infty$ then $g_S = \infty$.

Hence, impedance $r_S = 0$.

Therefore this low source impedance causes the current from the bit lines to flow into the sources of M1 and M2 rather than into M5 and M6 and subsequently add to the charge at the drains of M1 and M2.

As shown in Fig. 5.4.2, the response time from the 50 % point of the precharge clock to a 3V difference of Vout is 8ns(18.5ns-10.5ns). For this simulations W/L=5 with L=0.6 μm was used for all transistors by using MOSIS CMOS n-well model parameters. This scheme needs more transistors than the conventional voltage sense amplifier; two transistors for refresh operations and two transistors for the bitline clamping operation.

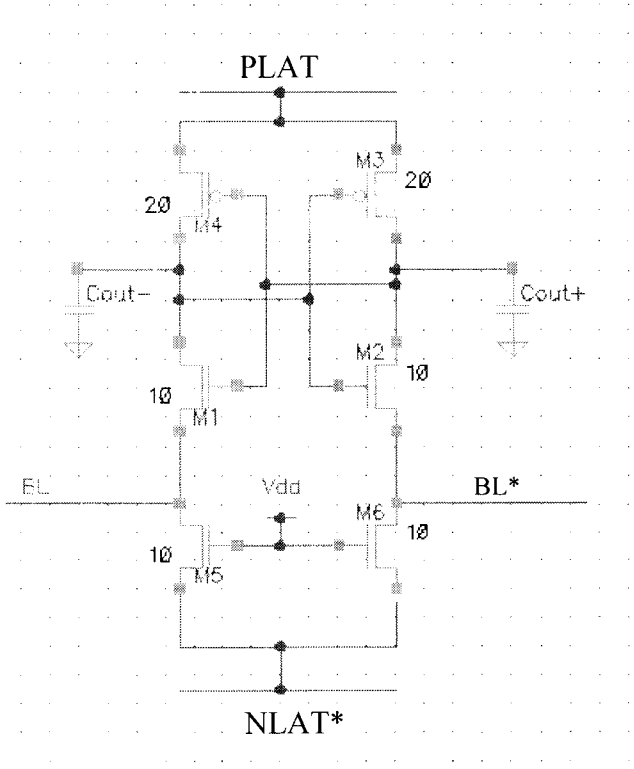


Fig. 5.4.1 Clamped bit line current sense amplifier

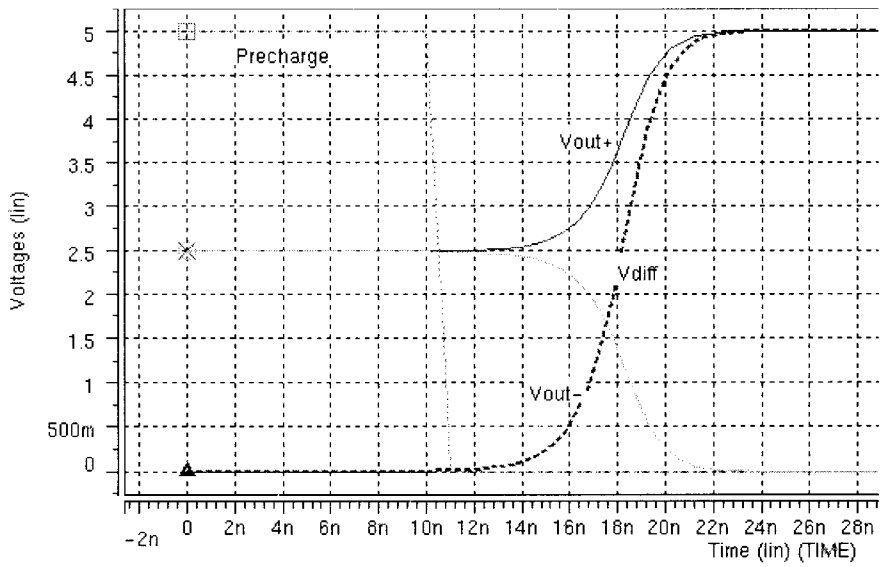


Fig. 5.4.2 Response time of clamped bit line sense amplifier

5.4.2 CIRCUIT DIAGRAM FOR A CLAMPED BIT LINE SENSE AMPLIFIER

Fig. 5.4.3 represents the clamped bit line circuit diagram. Notice that the bit line capacitance is connected to the drains of the M5 and M6 because the bitlines are coming to these points.

Fig. 5.4.4 shows the small signal model to analyze rout , low frequency gain(dc), and frequency domain analysis(ac) model.

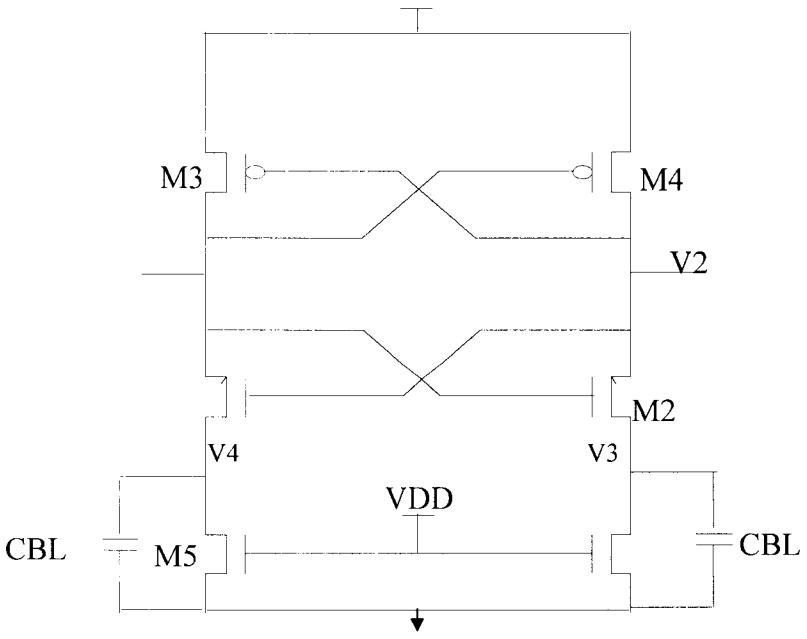


Fig. 5.4.3 Circuit diagram of clamped bitline sense amplifier

5.4.3 SMALL SIGNAL MODEL

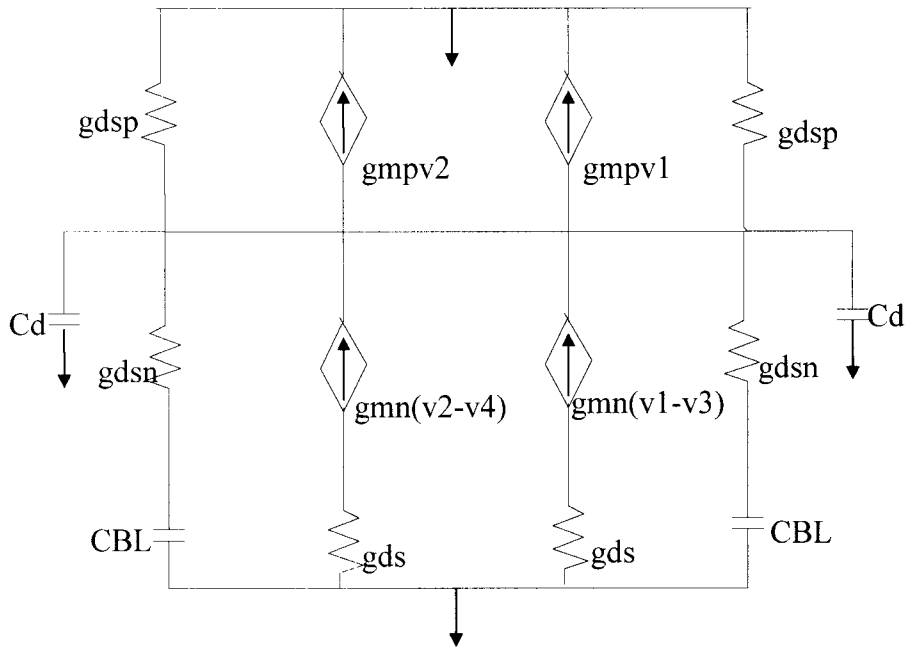
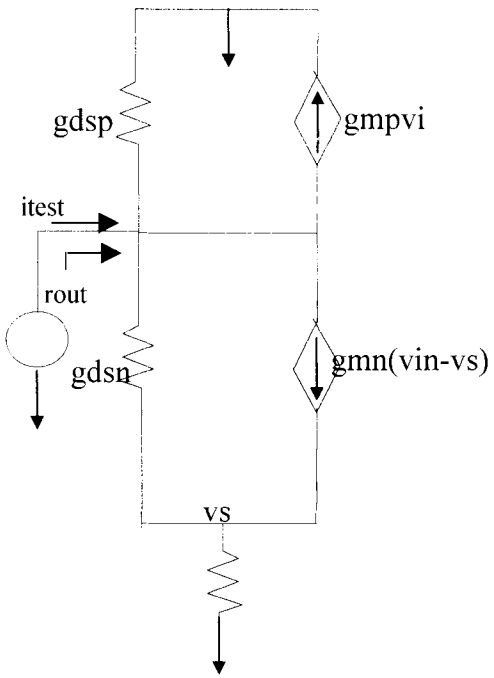
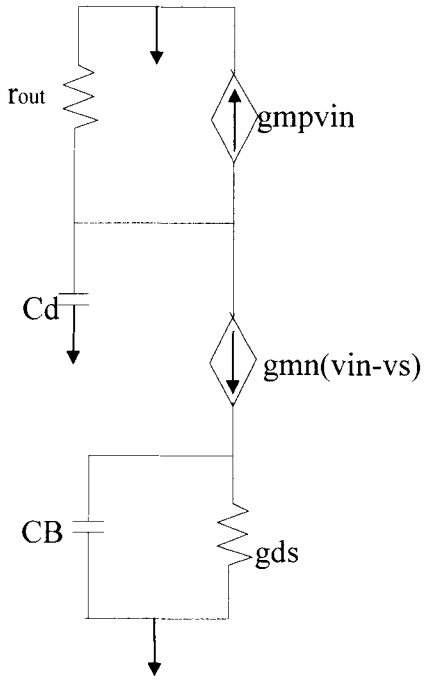


Fig. 5.4.4 Small signal models of clamped bitline sense amplifier

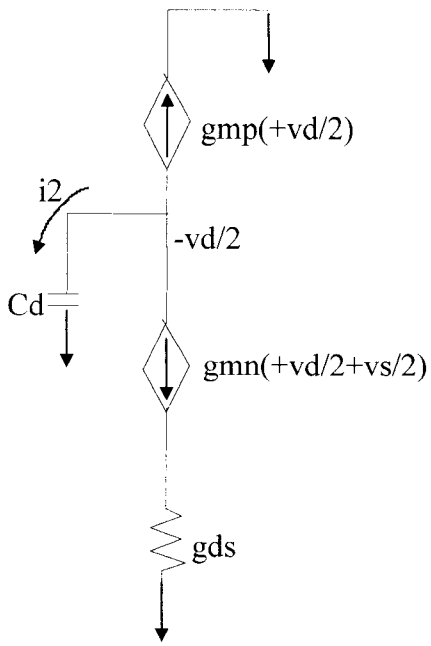
In Fig. 5.4.4, Cd includes Cgdp, Cdbp, Cgsn, Cdbn, and Cwire while CBL represents the bitline capacitance.

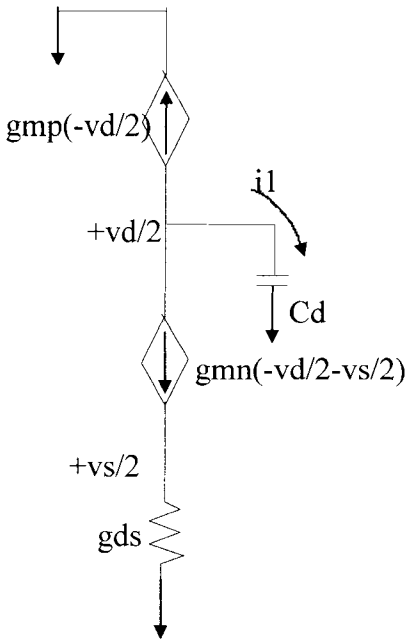


(a) Model for r_{out}



(b) Model for AC





(c) Model for response time

Fig. 5.4.5 Ro, ac, and time model

5.4.4 DC ANALYSIS

Fig. 5.4.3 represents the clamped bit line sense amplifier and the small signal models shown in Fig. 5.4.4. Fig. 5.4.5 is used to calculate the low frequency gain, ac frequency, and response time analysis. r_{out} is calculated in the following analysis.

To find r_{out}, by KCL in Fig. 5.4.5(a)

$$i_{test} = g_{dsp}v_{test} + g_{dsn}(v_{test} - v_s) + g_{mn}(-v_s) = 0 \tag{5.7}$$

$$g_{ds}v_s + g_{dsn}(v_s - v_{test}) + g_{mn}v_s = 0 \tag{5.8}$$

From Eq. (5.8) $v_s = \dfrac{g_{dsn}v_{test}}{g_{mn} + g_{ds} + g_{dsn}}$ (5.9)

By substituting Eq. (5.9) into (5.7),

$$i_{test} = (g_{dsp} + g_{dsn})v_{test} - (g_{dsn} + g_{mn})\left(\frac{g_{dsn}v_{test}}{g_{mn} + g_{ds} + g_{dsn}}\right) \tag{5.10}$$

$$r_{out} = \frac{v_{test}}{i_{test}} = \frac{g_{mn} + g_{ds} + g_{dsn}}{g_{dsp}g_{mn} + g_{dsp}g_{dsn} + g_{ds}g_{dsp} + g_{ds}g_{dsn}} \tag{5.11}$$

$$r_{out} \approx \left(g_{dsp} + \frac{g_{ds}g_{dsn}}{g_{mn} + g_{ds} + g_{dsn}}\right)^{-1} \approx \left(g_{dsp} + \frac{g_{ds}g_{dsn}}{g_{mn} + g_{ds}}\right)^{-1} \quad \Theta\ g_{dsn} << g_{ds} \tag{5.12}$$

5.4.5 AC ANALYSIS

After putting r_{out} to Fig. 5.4.5(b) to find the frequency response(AC), by KCL at Vout and Vs node

$$g_{mp}v_{in} + \frac{v_{out}}{r_{out}} + sC_d v_{out} + g_{mn}(v_{in} - v_s) = 0 \tag{5.13}$$

$$-g_{mn}(v_{in} - v_2) + sC_{bl}v_2 + g_{ds}v_2 = 0 \tag{5.14}$$

From Eq. (5.13), $v_2 = \dfrac{g_{mn}v_{in}}{g_{mn} + sC_{bl} + g_{ds}}$ (5.15)

Substituting Eq.(5.15) into Eq. (5.13),

$$g_{mp}v_{in} + \frac{v_{out}}{r_{out}} + sC_d v_{out} + g_{mn}v_{in} - g_{mn}v_2 = 0 \tag{5.16}$$

$$\frac{v_{out}}{v_{in}} = \frac{\left[\left(g_{mn} + g_{mp}\right) - \dfrac{g_{mn}^{\,2}}{g_{mn} + g_{ds} + sC_{bl}}\right]}{\left(\dfrac{1}{r_{out}} + sC_d\right)} \tag{5.17}$$

$$= \frac{(g_{mn} + g_{mp})(g_{mn} + g_{ds} + sC_{bl}) - g_{mn}^{\,2}}{(g_{mn} + g_{ds} + sC_{bl})(\dfrac{1}{r_{out}} + sC_d)} \tag{5.18}$$

$$= \frac{r_{out}(g_{mn} + g_{mp})(g_{mn} + g_{ds} + sC_{bl}) - g_{mn}^{\,2}}{(g_{mn} + g_{ds})\left(1 + \dfrac{sC_{bl}}{g_{mn} + g_{ds}}\right)(1 + sC_d R_d)} \tag{5.19}$$

If we specify $A(s) = \dfrac{r_{out}(g_{mn} + g_{mp})(g_{mn} + g_{ds} + sC_{bl}) - g_{mn}^{\,2}}{(g_{mn} + g_{ds})}$ from Eq. (5.19) then

$$A(s) = r_{out}\left(g_{mp} + \frac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} + \frac{sC_{bl}(g_{mn}+g_{mp})}{g_{mn}+g_{ds}} \right) \tag{5.20}$$

$$= r_{out}\left(g_{mp} + \frac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} \right)\left(1 + \frac{(g_{mn}+g_{mp})\cdot sC_{bl}}{g_{mp}(g_{mn}+g_{ds}) + g_{mn}g_{ds}} \right) \tag{5.21}$$

$$= r_{out}\left(g_{mp} + \frac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} \right)\left(1 + \frac{sC_{bl}}{\dfrac{g_{mp}g_{mn}+g_{mp}g_{ds}+g_{mn}g_{ds}}{g_{mn}+g_{mp}}} \right) \tag{5.22}$$

$$= r_{out}\left(g_{mp} + \frac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} \right)\left(1 + \frac{sC_{bl}}{g_{ds} + \dfrac{g_{mn}g_{mp}}{g_{mn}+g_{mp}}} \right) \tag{5.23}$$

$$= r_{out}\left(g_{mp} + \frac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} \right)\left(1 + \frac{sC_{bl}}{g_{ds}} \right) \qquad \Theta \frac{g_{mn}g_{mp}}{g_{mn}+g_{mp}} \approx 0 \tag{5.24}$$

Now we replace this simplified form into Eq. (5.19) then

$$r_{out} = \frac{r_{out}\left(g_{mp} + \dfrac{g_{mn}g_{ds}}{g_{mn}+g_{ds}} \right)\left(1 + \dfrac{sC_{bl}}{g_{ds}} \right)}{\left(1 + \dfrac{sC_{bl}}{g_{mn}+g_{ds}} \right)(1 + sC_d R_d)} \tag{5.25}$$

$$r_{out} = \frac{g_m^{*} \cdot r_{out}\left(1 + \dfrac{sC_{bl}}{g_{ds}} \right)}{\left(1 + \dfrac{sC_{bl}}{g_{mn}+g_{ds}} \right)(1 + sC_d R_d)} \tag{5.26}$$

where $g_m^* = g_{mp} + \frac{g_{mn} g_{ds}}{g_{mn} + g_{ds}}$ $\qquad r_{out} = \left(g_{dsp} + \frac{g_{dsn}}{1 + \frac{g_{mn}}{g_{ds}}} \right)^{-1}$ (5.27)

therefore, the loop gain for two inverters is the gain of a single inverter squared or raised to the power of 2.

$$T(s) = \left(\frac{g_m^* r_o^* \left(1 + \frac{sC_{bl}}{g_{ds}} \right)}{\left(1 + \frac{sC_{bl}}{g_{mn} + g_{ds}} \right)(1 + sC_d R_d)} \right)^2 \tag{5.28}$$

From this transfer function, the spacing of the pole-zero pair will be

$$\frac{\frac{g_{mn} + g_{ds}}{C_{bl}}}{\frac{g_{ds}}{C_{bl}}} = \frac{g_{mn} + g_{ds}}{g_{ds}}. \tag{5.29}$$

The drain conductance g_{ds} tends to be large since the clamp device is in the linear region so that they cancel each other in equation (5.29).

Then the gain is $g_m^* r_{out}$ and the bandwidth is $\frac{1}{r_{out} C_d}$.

Eventually the gain bandwidth product GBW=$\frac{g_m^*}{C_d}$ which doesn't have any C_{bl} term while GBW of the conventional amplifier is $\frac{g_m}{C_{bl}}$.

5.4.6 RESPONSE TIME

As shown in the Fig. 5.4.5(c), if we assume that the output resistance is infinite then, by KCL at node 1and 2

$$i_2 + g_{mp}\left(\frac{v_d}{2}\right) + g_{mn}\left(\frac{v_d}{2} + \frac{v_d}{2}\right) = 0 \tag{5.30}$$

$$-g_{mn}\left(\frac{v_d}{2} + \frac{v_s}{2}\right) - \frac{v_s}{2R} = 0 \tag{5.31}$$

From Eq. (5.31), $v_s = \dfrac{g_m v_d}{g_{mn} + \dfrac{1}{R_s}}$ (5.32)

Substituting Eq. (5.32) into Eq. (5.30)

$$-i_2 = \frac{v_d}{2}\left(g_{mp} + g_{mn}\left(1 - \frac{g_{mn}}{g_{mn} + \dfrac{1}{R_s}}\right)\right) \tag{5.33}$$

$$= \frac{v_d}{2}\left(g_{mp} + \frac{g_{mn}}{1 + g_{mn}R_s}\right) \tag{5.34}$$

Therefore $i_2 = \dfrac{v_d}{2}\left(g_{mp} + g_{mn}^{*}\right)$ where $g_{mn}^{*} = \dfrac{g_{mn}}{1 + g_{mn}R_s}$ (5.35)

For the right side of Fig. 14 if we assume the output resistance is infinite then, by KCL at node 1 and 2

$$i_1 - g_{mp}\left(\frac{v_d}{2}\right) - g_{mn}\left(\frac{v_d}{2} + \frac{v_s}{2}\right) = 0 \tag{5.36}$$

$$g_{mn}v_d + g_{mn}v_s + \frac{v_s}{R_s} = 0 \tag{5.37}$$

From Eq. (5.37) $v_s = \dfrac{g_m v_d}{g_{mn} + \dfrac{1}{R_s}}$ (5.38)

Substituting Eq. (5.38) into Eq. (5.36)

$$i_1 = \frac{v_d}{2}\left(g_{mp} + g_{mn}\left(1 - \frac{g_{mn}}{g_{mn} + \dfrac{1}{R_s}} \right) \right) \tag{5.39}$$

$$= \frac{v_d}{2}\left(g_{mp} + \frac{g_{mn}}{1 + g_{mn}R_s} \right) \tag{5.40}$$

Therefore $i_2 = \dfrac{v_d}{2}(g_{mp} + g_{mn}^{*})$ where $g_{mn}^{*} = \dfrac{g_{mn}}{1 + g_{mn}R_s}$ (5.41)

$$i_1 - i_2 = v_d(g_{mp} + g_{mn}^{*}) \tag{5.42}$$

$$\frac{dv_d}{dt} = \left(g_{mp} + g_{mn}^{*}\right)\frac{v_d}{C_d} \text{ where } g_{mn}^{*} = \frac{g_{mn}}{1 + g_{mn}R_s} \tag{5.43}$$

Since C_d is very small in the current sense amplifier, the output voltage difference develops very rapidly.

5.5 MAJOR BIT LINE STRUCTURE FOR A SENSE AMPLIFIER

5.5.1 OPEN BIT LINE STRUCTURE

The following Fig. 5.5.1 shows the open bit line structure in which bit line(BL) and bit line bar(BL*) are located at both ends. The bit line consists of a conductive line connected to a multitude of transfer transistors. The transfer transistor gate terminals are connected to a wordline. The wordline is physically orthogonal to bit line. A memory array is formed by tiling a selected quantity of memory bits together such that memory bits do not share a common wordline and memory cells along a common word line do not share a common bitline. An example of this is shown in Fig. 5.5.2. In this layout memory cells are paired to share a common contact to the bit lines, which reduces the array size by eliminating duplication.

Fig. 5.5.2 illustrates several memory cell features. One memory cell is located at the every wordline and bit line cross point. When a word line is selected, the bitline(BL) voltage increases a little because of a coupling capacitance between the wordline and bitline. However the bitline bar(BL*) doesn't increase because the wordline is not active. This noise imbalance between BL and BL* makes the sense amplifier sensitivity worse. Therefore we need a dummy word line to imitate the wordline selection. In the open bit line architecture, a sense amplifier should exist at each bitline pitch. Hence a good layout technique is needed to lay two PMOS's and two NMOS's within the pitch.

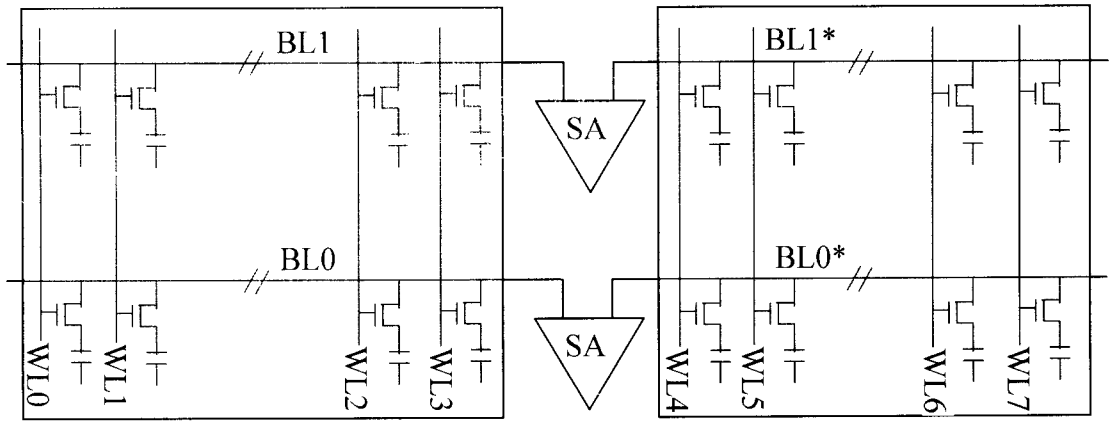


Fig. 5.5.1 Open bit line architecture

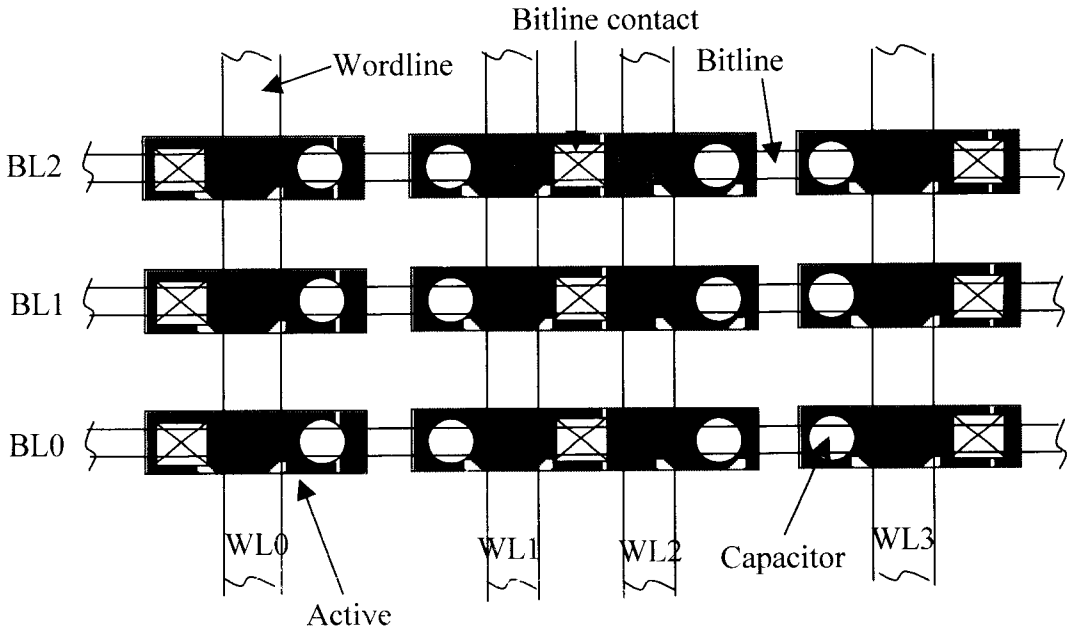


Fig. 5.5.2 Open bit line array layout

5.5.2 FOLDED BIT LINE STRUCTURE

The folded array is schematically depicted in Fig. 5.5.3. Sense amplifier circuits are placed at the edge of the each array with both true bitline (BL) and complement bitline (BL*) coming from a single array.

In other words, one pair of BL and BL* is tied to one side of a sense amplifier and another pair of BL and BL* is connected the other side of it. The space for the sense amplifier occupies the two bit line pitch and this looks like a folded open bit line structure.

The coupling noise to a wordline occurs at both BL and BL* and is in the same direction and this kind of common mode noise is cancelled by a differential sense amplifier.

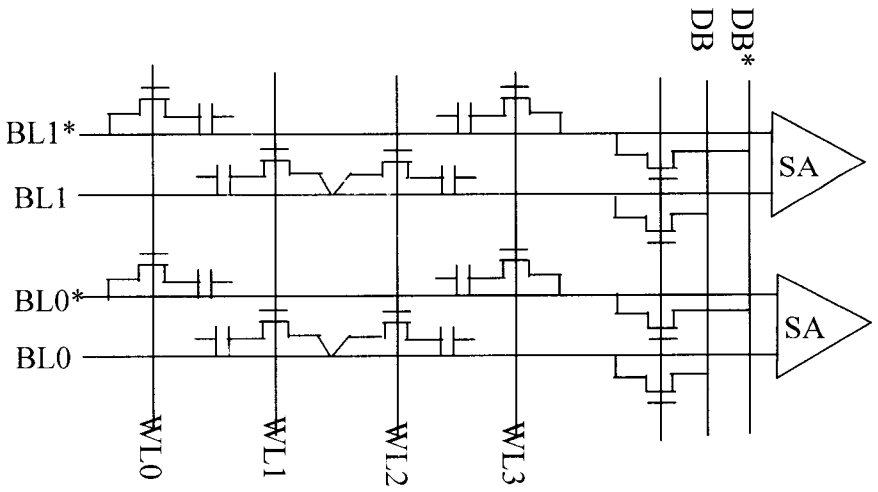


Fig. 5.5.3 Folded bit line architecture

6. GATE-BASE-BODY CONNECTED MOSFET(GBB-MOS)

6.1 TWO TYPES OF GBB-NMOS AND GBB-PMOS

Fig. 6.1.1 shows the schematic of the gated-base-body connected NMOS and PMOS to improve current drive capability. The physical structure for a GBB-NMOS is shown in Fig. 6.1.2. The BJT is inherently formed below the MOS transistor.

Fig. 6.1.3 describes the collector current of the BJT and the drain current of GB-NMOS as well GBB-MOS as VGS varies along x-axis with the various Vdd values.

If VGS is less than 0.63 V, the GB-NMOS dominates the total current and then after that point the collector current of BJT starts to be added to it. If the VGS is increased to about 0.63V, the Ic of BJT starts surpassing the drain current of GB-MOS and the total current is $I_{TOTAL} = 100\mu A$ with Vdd=0.7 V. Ref [1] and [2] describe the modeling of lateral bipolar devices in a CMOS process and discuss the bipolar action in a MOS structure.

Notice that the base width of BJT is the channel length of NMOS transistor. Also a maximum limit of a collector current Ic can be described by a current density per unit area. $J = \frac{qD_n n_p}{W_B}$ Hence $I_C = J \cdot A$ where A is the area of emitter-base junction as shown in Fig. 6.1.2. This is described and derived in detail in Section 6.2.

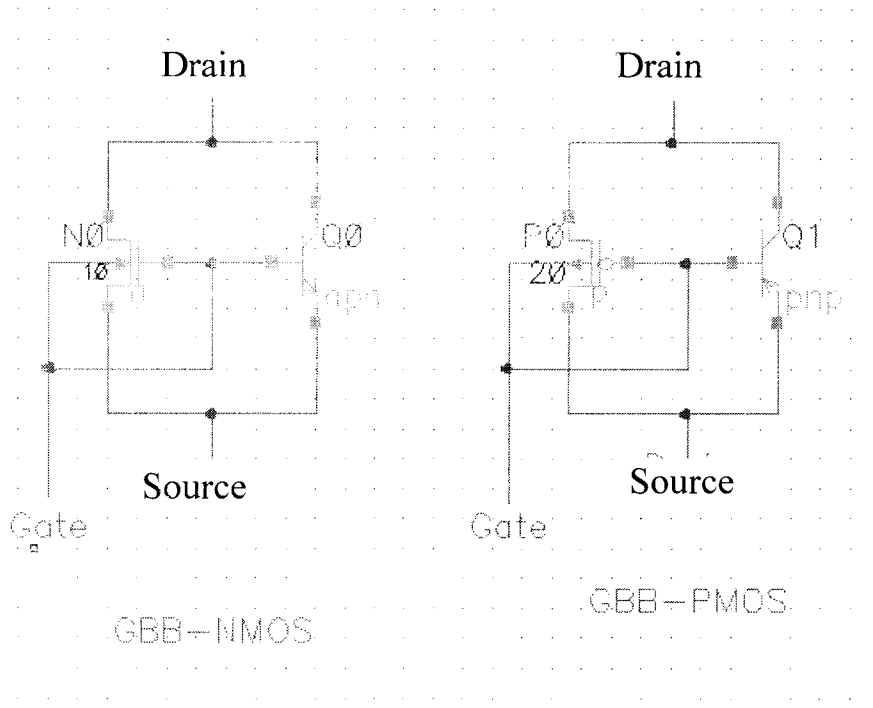


Fig. 6.1.1 Two types of GBB-NMOS and GBB-PMOS

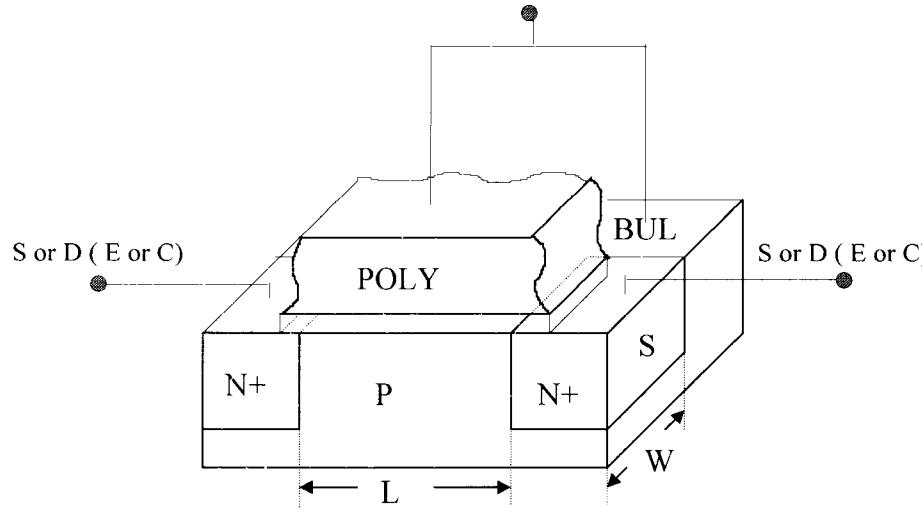


Fig. 6.1.2 Three dimensional shape of GBB-NMOS cell

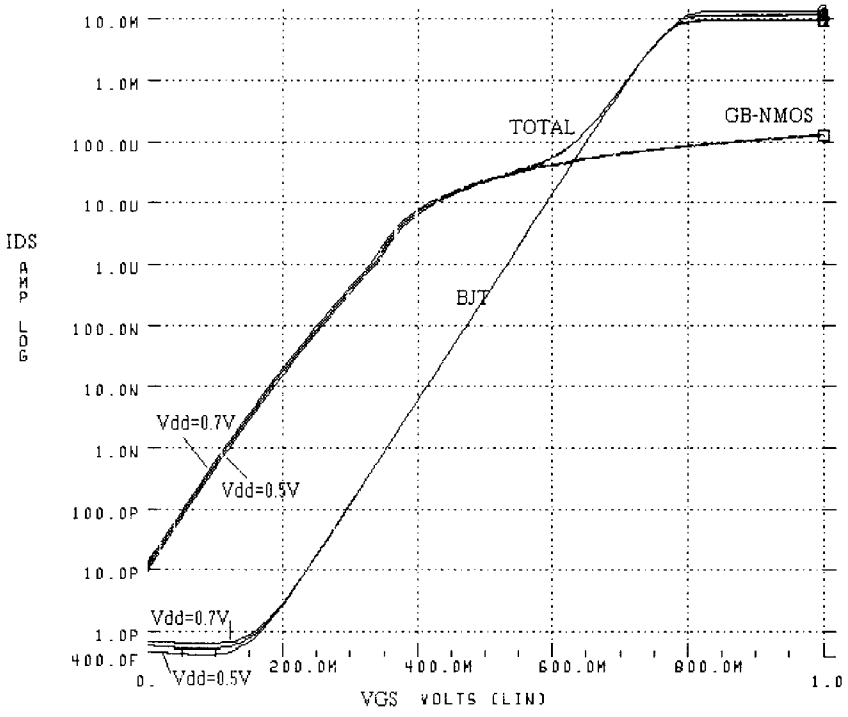


Fig. 6.1.3 I-V characteristic of GBB-NMOS cell

6.2 FLOW OF CARRIERS IN BIPOLAR MODE

The following Fig. 6.2.1 shows the cross-section of the triple well technology used in a modern high density DRAM and shows the carrier flow of lateral bipolar transistor mode.

In the Fig. 6.2.1 the base area of P-Well2 is 420u x 1370u because three different size of transistors are formed in it. The source/drain diffusion depth is about 0.11um and the depth of P-Well2 is around 1.0 um. Emitter current I_E (I_S) is spilit into a base current I_B and lateral collector current I_C (I_D) and substrate collector current is I_{NWELL}. Therefore, either of the common base current gain $\alpha = \frac{-I_C}{I_E}$ and $\alpha_S = \frac{-I_S}{I_E}$ = one. However due to the very small rate of recombination inside the lightly doped p-base region and high emitter efficiency, both common emitter gains $\beta = \frac{I_C}{I_B}$ and $\beta_S = \frac{I_S}{I_B}$ can be large. To optimize the lateral BJT action, the ratio $\frac{I_C}{I_S}$ must be as large as possible. This can be achieved without any change in the standard CMOS technology by minimizing the emitter area and the lateral base width(Length of MOS).

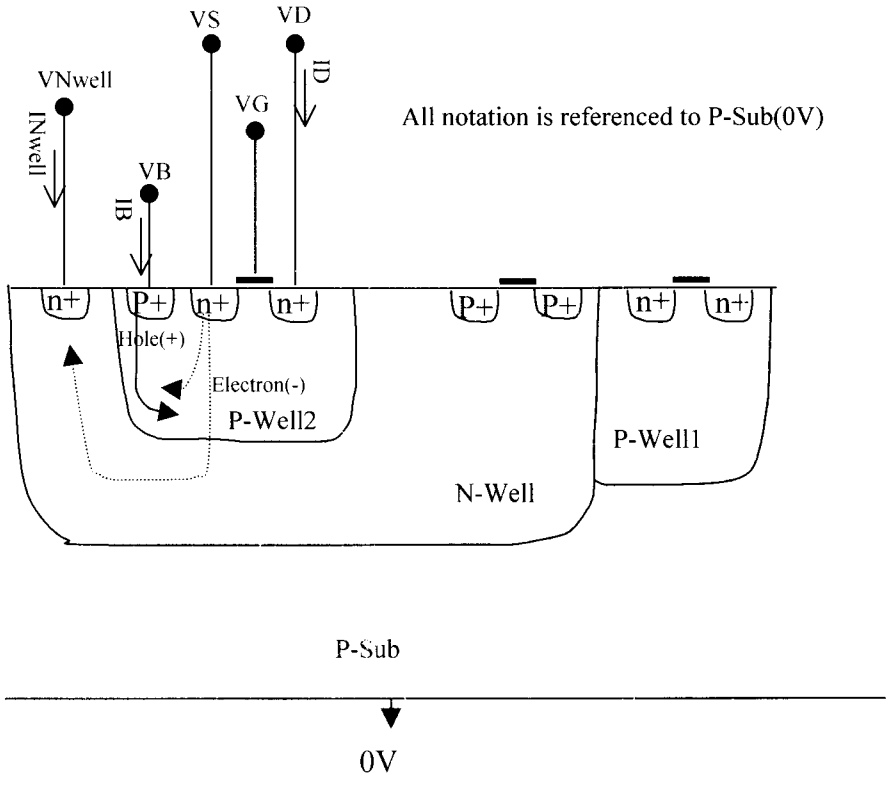


Fig. 6.2.1 Cross section of a triple well

6.3 COLLECTOR CURRENT OF A GATED LATERAL BJT

We need to derive an expression for the collector current of a lateral transistor , β_L, which is parallel to the NMOS transistor.

The collector current is produced by minority-carrier in the base diffusing in the direction of the concentration gradient and being swept across the collector-base depletion region by the field existing there.

The diffusion current density due to electrons in the base is

$$J_n = qD_n \frac{dn_p(x)}{dx} = qD_n \frac{n_p(0)}{W_B} \tag{6.1}$$

$$I_C = qAD_n \frac{n_p(0)}{W_B} \tag{6.2}$$

where A is the cross-section area of the emitter-base junction, W_B is the base width, D_p is the effective diffusion constant.

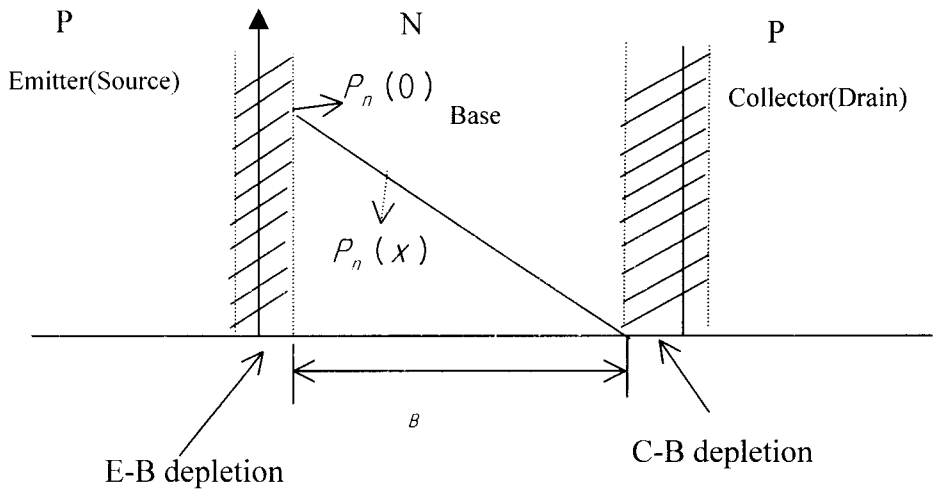


Fig. 6.3.1 Minority carrier in the base of a lateral PNP in the forward-active

$$n_p(0) = n_{po} e^{V_{BE}/V_T} \tag{6.3}$$

$$n_p(W_B) = n_{po} e^{V_{BE}/V_T} \approx 0 \tag{6.4}$$

$$\text{Therefore } I_C = \frac{qAD_n n_{po}}{W_B} e^{V_{BE}/V_T} = I_S e^{V_{BE}/V_T} \text{ where } I_S = \frac{qAD_n n_{po}}{W_B}. \tag{6.5}$$

For low level injection into the base, the base minority-carrier life time remains constant. However, when the minority-carrier density becomes comparable with the majority carrier density, the majority carrier density must increase to maintain charge neutrality in the base. This causes a decrease in the lateral β because the base transport factor and effective life time decrease due to recombinations in the base and the emitter injection

efficiency decreases due to the higher doping density in the base. That is, at the onset of high level of injection,

$$J_n = qD_n \frac{n_p(0)}{W_B} \quad \text{then } n_p(0) = p_p \approx N_A \tag{6.6}$$

Thus $$I_C = I_D = \frac{qAD_nN_A}{W_B} \tag{6.7}$$

where A is the area of emitter-base junction.

Eq. (6.7) gives the limit of the collector current and Eq. (6.8) and (6.9) show the factors affecting the lateral β.

One factor is α_T (base transport factor) and another one is γ (emitter injection efficiency). In ideal case, α_T=1 and γ=1 [33].

$$\alpha_T = \frac{1}{1 + \frac{W_B^{\,2}}{2\tau_b D_n}} \tag{6.8}$$

$$\gamma = \frac{1}{1 + \left(\frac{D_P}{D_n}\right)\left(\frac{W_B}{L_p}\right)\left(\frac{N_A}{N_D}\right)} \quad \text{for NPN} \tag{6.9}$$

From Eq. (6.8) we know that making W_B (Channel length) small will improve α_T which increases the current gain of BJT.

6.4 MEASUREMENTS OF A GATED LATERAL BJT

The following Fig. 6.4.1 shows the transfer I-V characteristics of a fabricated NMOS transistor with W/L=10 μm / 0.25 μm measured by a HP4156 parameter analyzer. This graph was obtained by disabling the lateral bipolar transistor. The size of P-well which acts as the base region of a lateral BJT is 420 μm x 1370 μm and is large because two other different size of transistors are made in the same well. Notice that this transfer curve does not show the reduced threshold voltage characteristics because the positive voltage is not applied to the bulk of NMOS transistor.

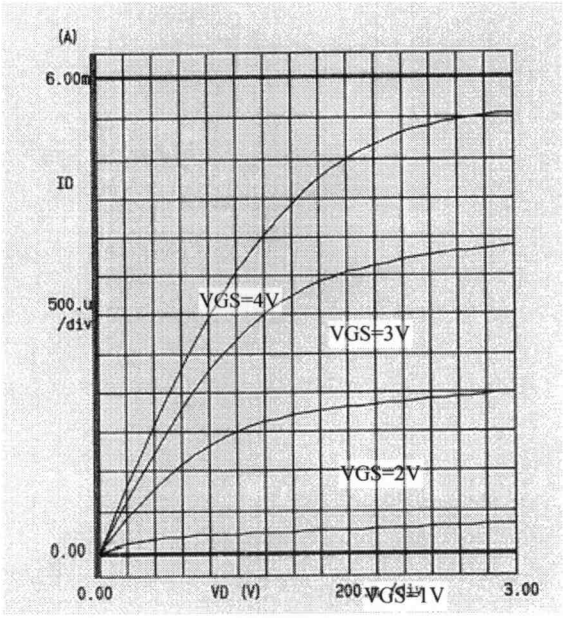


Fig. 6.4.1 Transfer I-V characteristic for W/L=10μm/0.25μm

The comparison between BSIM2(Level 39) simulations and actual measurements are shown in Fig. 6.4.2. This graph shows a good correlation except for the curve for VGS=4V. The curve for VGS=4V shows a deviation from simulations because VGS=4V places the NMOS in the linear region when VDS=3V. In other words, VGS=4V is is given only for reference because it's not a reasonable gate voltage with a VDS=3V power supply.

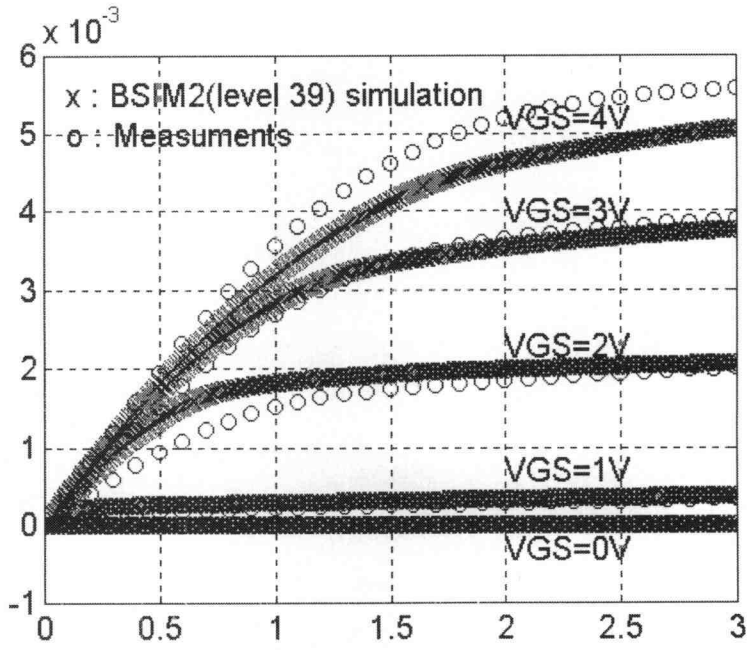


Fig. 6.4.2 Comparison between actual measurements and BSIM2

Fig. 6.4.3 represents the drain current ID as a function of a source voltage VS with VB=0V. As VG increases, in the channel region, holes are depleted away from the surface and equilibrium potential barrier between the source and well is reduced. This makes a dramatic increase in the electron injection into the well(base) for a given well-source forward bias. Therefore the drain current varies significantly with VG. For large enough negative values of VG(VG≤ -0.8V in this case), all curves merge into the last one represented by the thicker line. At this bias condition, the ID-VS relationship becomes independent of VG, stays exponential with a slope of kT/q, the source to drain current has been pushed below the surface of the device and eventually only bipolar action is achieved.

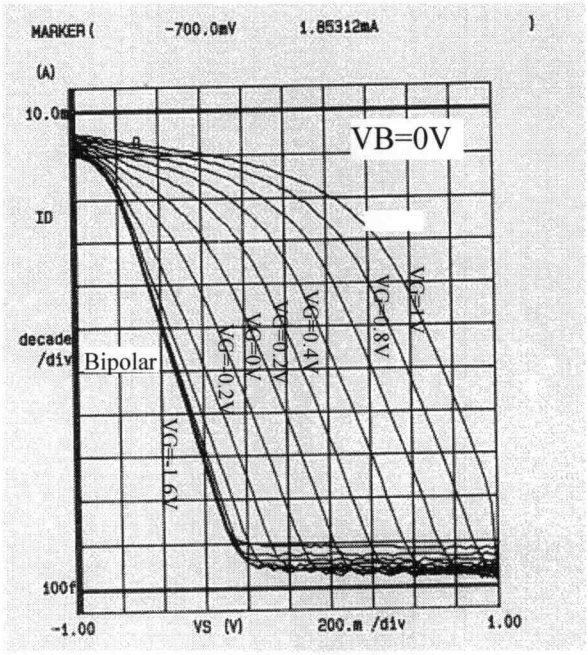


Fig. 6.4.3 ID vs. VS with various VG's

Fig. 6.4.4 represents the conventional ID vs. VD transfer characteristic with various base currents IB, in which one can see the current amplification factor β_L is around 10.

The bipolar mode is set by applying VGS= -2V and a small current is forced to flow into the base as I_B as shown in Fig. 6.4.4. The collector currents are shown based on $I_D = \beta I_B$. But a voltage form is more realistic than the current because a certain voltage is applied in the gated lateral BJT structure.

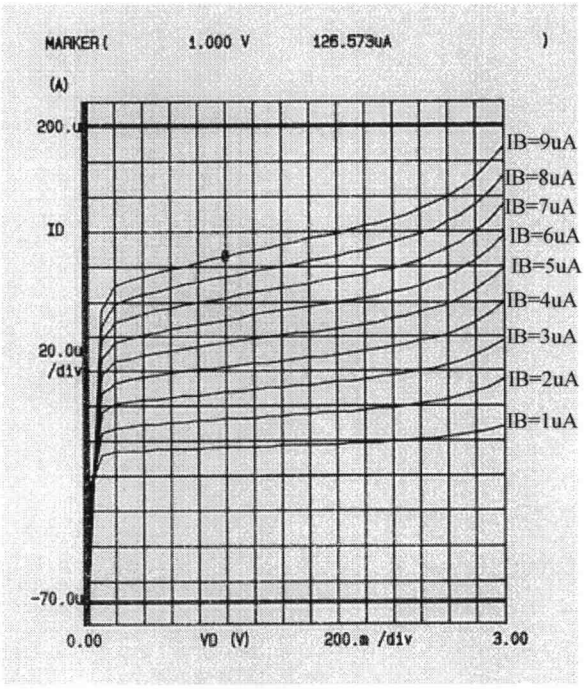


Fig. 6.4.4 ID vs. VD with various IB's

Fig. 6.4.5 shows the Gummel plot ID as a function of VBS while changing the VG from 1V to –2V. As is expected around VG=1V, NMOS action is dominant and there is a lot of drain current ID even though VBS=0 (VBE=0, voltage between base and emitter). However as VG decreases to VG= - 2V, it shows the pure BJT action is dominant and we can see the typical collector currents at points in excess of VBS=0.6V. Notice that base currents IB are almost shown as a single thicker line for various VG values.

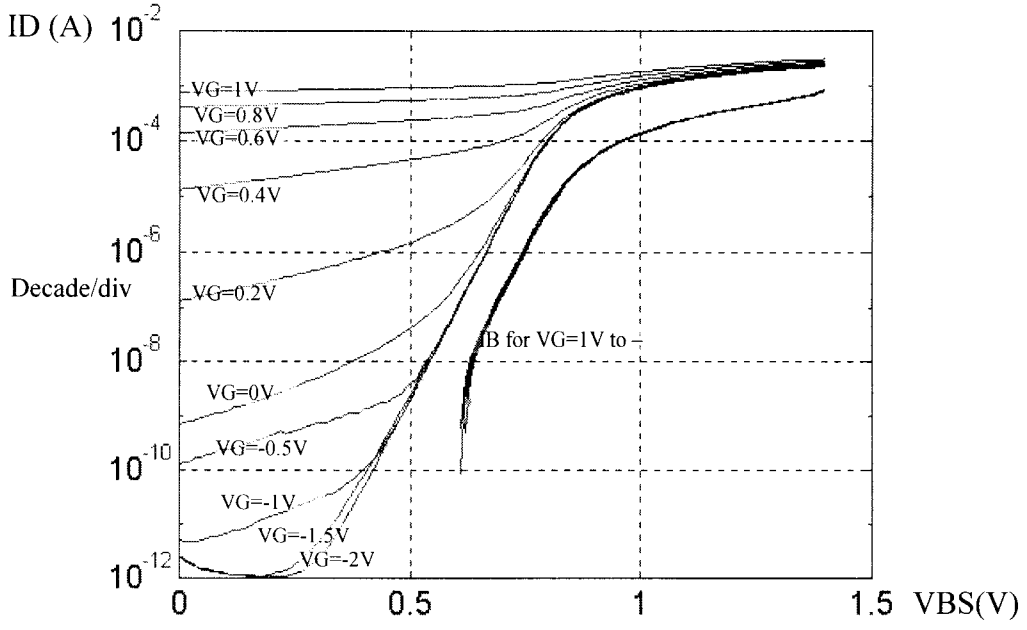


Fig. 6.4.5 Gummel plot with VG values

In Fig. 6.4.6, the base current of the gated lateral BJT can be obtained by connecting the points for which gates voltage VG equals the well voltage VB.

The curves shown in Fig. 6.4.6 are subthreshold behavior of the NMOS with various VB values. When the source-well junction is forward-biased enough, it becomes impossible to turn the device off. The drain current ID remains constant beyond a certain negative voltage VB and pure BJT action is obtained.

The larger reverse bias between source and well results in a larger threshold voltage, that is, V_T is shifted to the higher values. The dotted line represents ID and IB of the hybrid(gated) mode in which the gate and base are tied together.

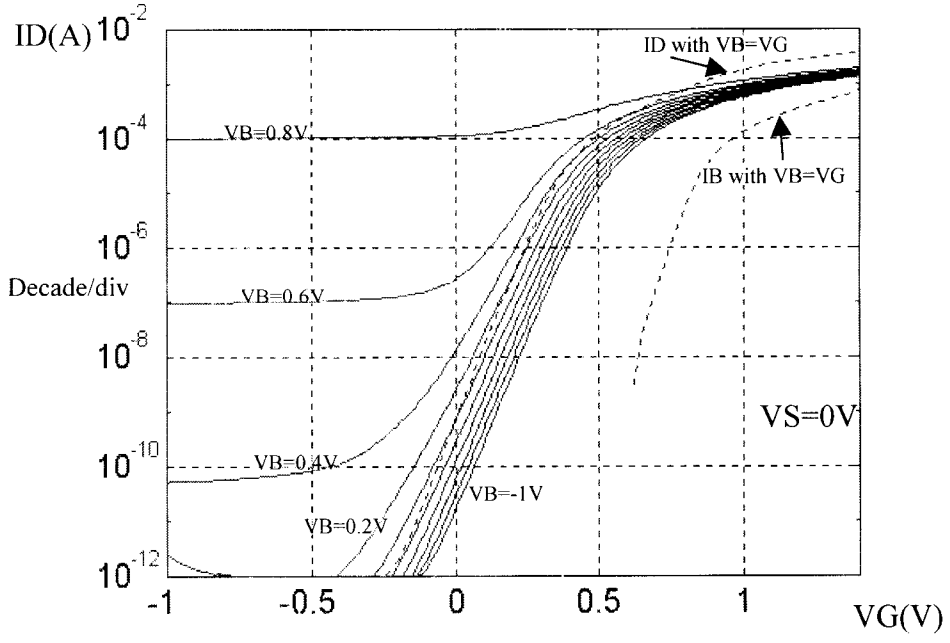


Fig. 6.4.6 ID current as a function of VG with increments of 0.2V.

Fig. 6.4.7 was obtained from the gated lateral bipolar mode in which the gate and base are tied together and the base and collector current measured. This graph is same as the dotted line in Fig. 6.5.6. The collector current was divided by base current and plotted in Fig. 6.4.7.

One can see the gated lateral bipolar current gain, β=100, at around VG=0.8V. This condition will be used in actual simulations because Vdd=1.5V and a half Vdd precharge is used in the simulations.

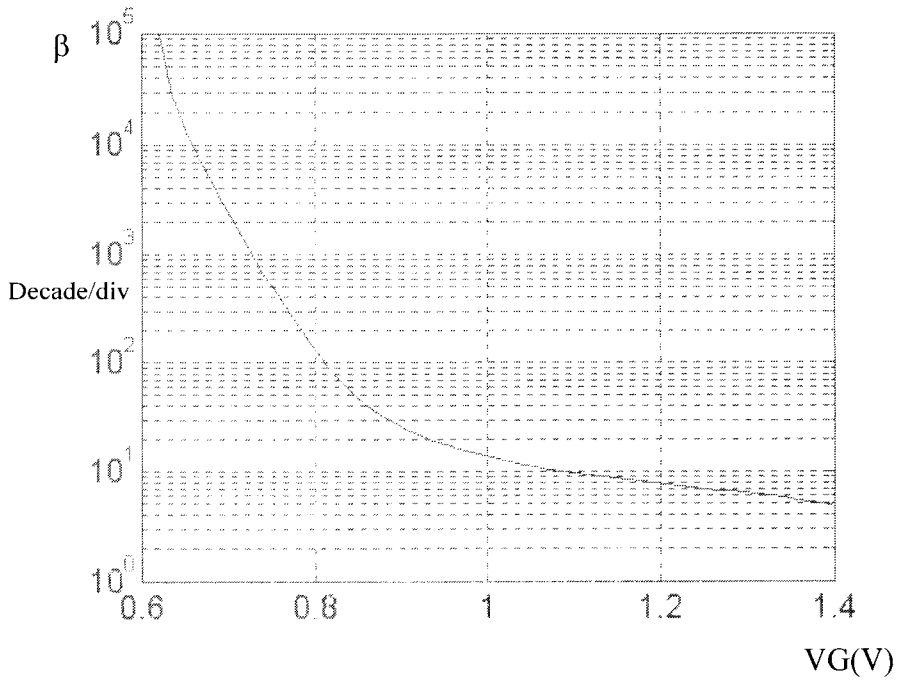


Fig. 6.4.7 Gated lateral bipolar gain, β, as a function of VG

6.5 SIMULATION RESULTS FOR A CURRENT SENSE AMPLIFIER WITH VDD=0.5V

Fig. 6.5.1 represents the circuit diagram for the current sense amplifier with the GBB-MOS structure. Fig. 6.5.2 shows the simulation output with Vdd=0.5V an ultra low voltage power supply in which the BJT part is not working yet. The PRE1, PRE2, and SENSE clocks are maintained high to equate the bit and bit* line(BL, BL*) and then the word line fires up to the $V_{dd} + V_T$ = 0.7V to write the V_d level on the plate of the capacitor. During this time the data in the cell is dumped onto the bit line and sensed by disabling PRE1, PRE2, and SENSE with low voltage levels.

This illustrates the access and sense cycle. After this time, the current from the cell yielded by the SENSE signal flows via the bit line into the low input impedance, the sources of transistors, M1 and M2 as shown in Fig. 6.5.1. Then PRE2 is disabled to detect the current difference. Right after this, the signal at the output node is rapidly amplified by the positive feedback of the latch.

Fig. 6.5.2 shows the write cycle and restore to write the original data back to the original cell. Fig. 6.5.3 shows the simulation results and the access time differences between the GB-MOS structure and GBB-MOS. The GBB has the lateral BJT action added.

As shown in Fig. 6.5.3, when the PRE1 is disabled and the word line is activated, TAWL(the access time from word line) for lateral BJT dominated sense amplifier is 2.75 ns at 0.1 V differential output voltage while that of GB-MOS dominated sense amplifier

is 5.9 ns at the same differential output voltage. Thus there is 3.15 NS difference of access times. Notice that $V_{dd} = 0.7V$ is used for the GBB-MOS to activate the lateral BJT but the GB-MOS has $V_{dd} = 0.6V$ and only MOS transistor action.

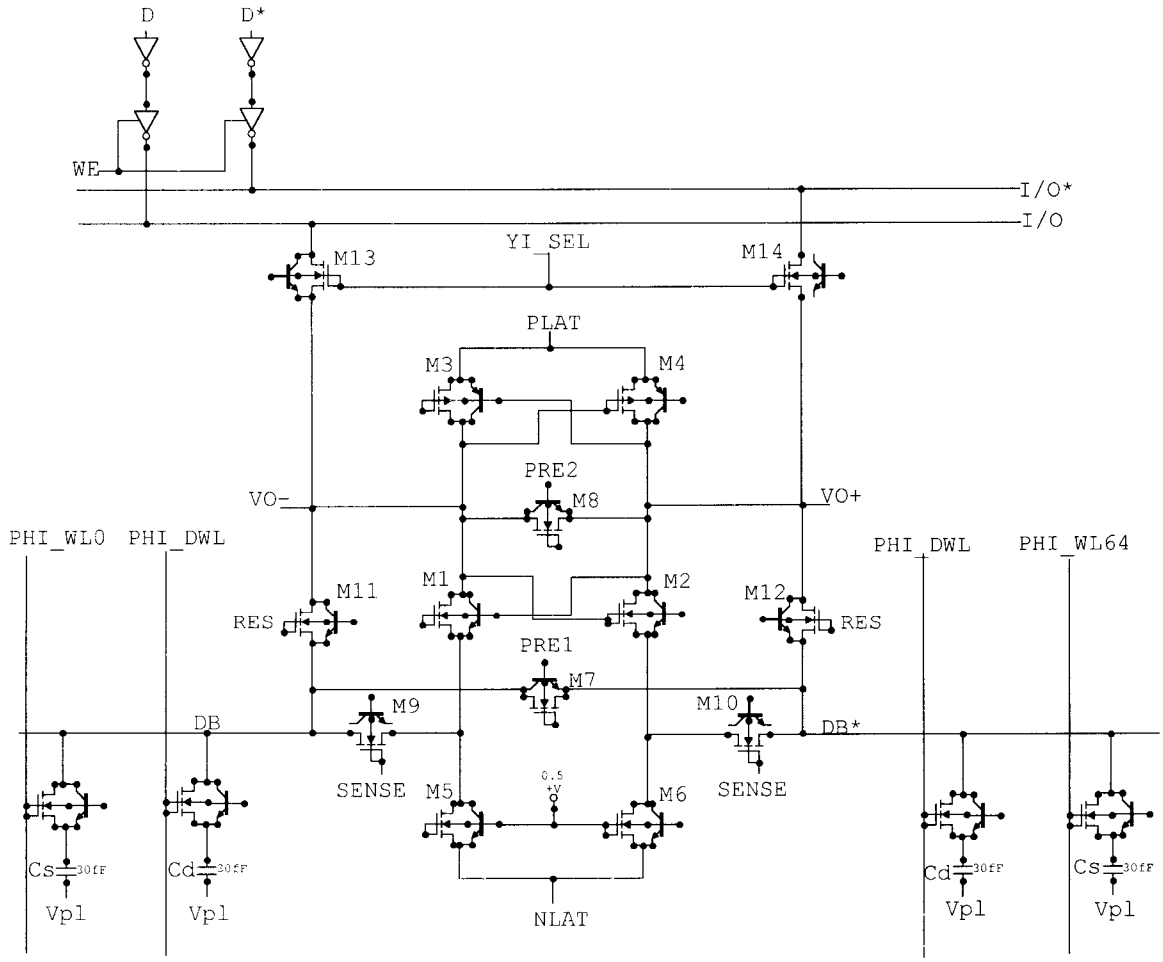


Fig. 6.5.1 Current sense amplifier with the GBB-NMOS and GBB-PMOS

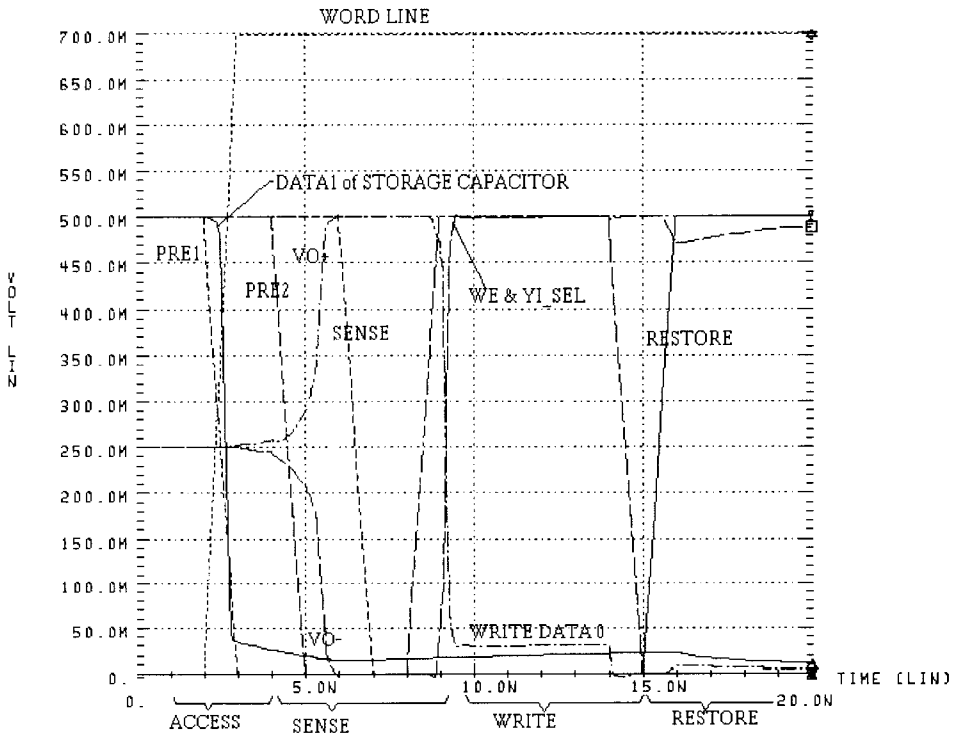


Fig. 6.5.2 Output wave forms for the current sense amplifier

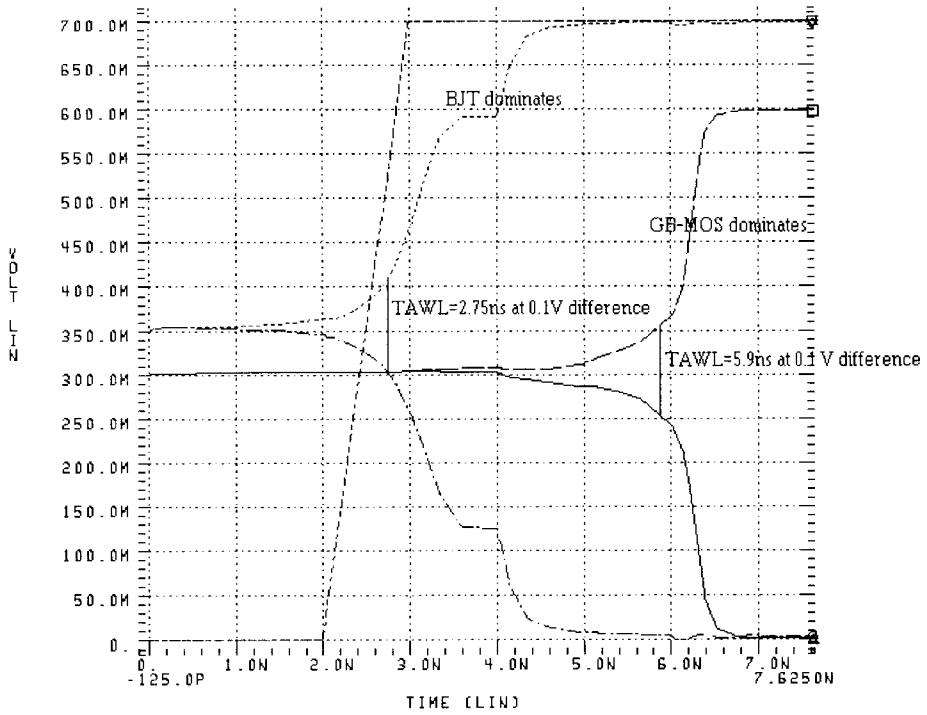


Fig. 6.5.3 Word line access comparison between GB-MOS and GBB-MOS

6.6 PROPOSED CURRENT SENSE AMPLIFIER WITH A GATED LATERAL BJT

6.6.1 MODELING OF A GATED BJT CURRENT SENSE AMPLIFIER

Fig.6.6.1 shows the gated lateral BJT current sense amplifier triggered by a gated BJT. The charge of the bit line is amplified as a huge collector current. If the gated BJT is considered to be only a bipolar transistor like a discrete device then the small signal

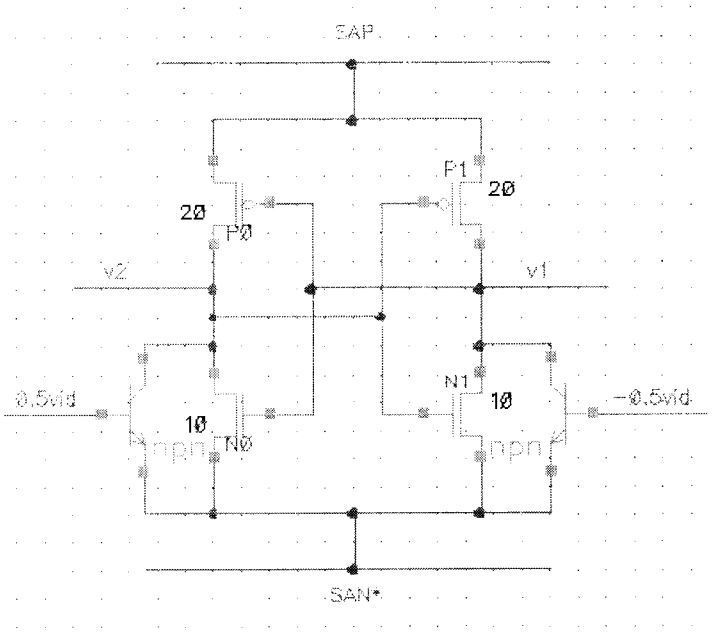


Fig.6.6.1 Gated BJT current sense amplifier

model is shown in Fig.6.6.2. The DC gain is calculated as follows by using a half circuit analysis because the left and right portions are symmetrical topology. The Fig. 6.6.2 can be used to analyze the DC gain of the gated BJT current sense amplifier. By using the half circuit analysis,

$$_2 = \frac{V_{od}}{2} \quad V_2' = \frac{V_{id}}{2} \tag{6.8}$$

$$-\frac{V_{od}}{2} = -(g_m V_2 + g_m' V_2') r_{dsp} \tag{6.9}$$

$$+\frac{V_{od}}{2} = \frac{g_m V_{od} r_{dsp}}{2} + g_m' (+\frac{V_{id}}{2}) r_{dsp} \tag{6.10}$$

$$_{od} - g_m r_{dsp} V_{od} = +g_m' r_{dsp} V_{id} \tag{6.11}$$

$$_{od} (1 - g_m r_{dsp}) = +g_m' r_{dsp} V_{id} \tag{6.12}$$

$$A_{dm} = \frac{V_{od}}{V_{id}} = \frac{+g_m' r_{dsp}}{1 - g_m r_{dsp}} \tag{6.13}$$

If the MOS transistor is in the saturation region, $g_m r_{dsp} >> 1$ then

$A_{dm} \approx \frac{g_m'}{g_m}$ where the transconductance of BJT $g_m' = \frac{I_C}{V_T}$

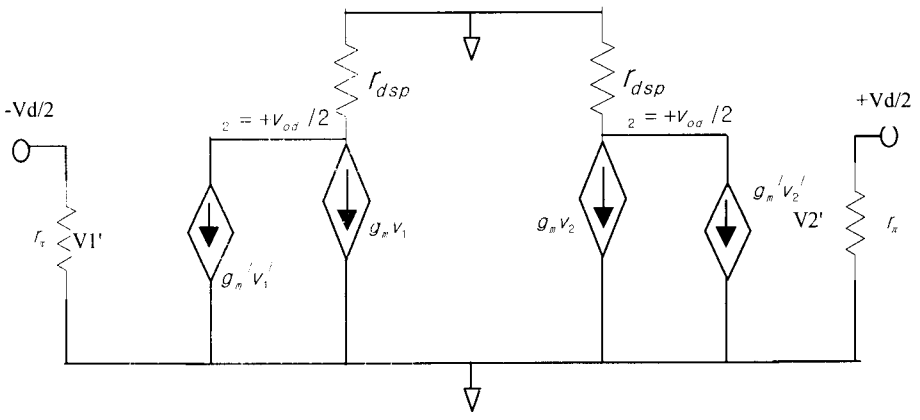


Fig. 6.6.2 Small signal model for DC analysis

The overall operation for this structure is shown in Fig. 6.6.3. In the gated structure, the minority carrier concentration (electrons in P-type base) depends on the gate voltage. As the gate voltage increases positively, the channel region is depleted away from the surface and equilibrium barrier between the well and source is reduced. This dramatically increases the amount of electron injection into the well for a given well-source forward bias, resulting in a strong increase in the current density near the surface.

If the lateral BJT is treated only as a BJT then the gated BJT model can be drawn as shown in Fig. 6.6.3. This model is discussed in [1].

But the devices measured here employ a retrograde N-well to suppress the current gain of the vertical BJT. Hence the model for the gated BJT used here is the simple BJT in the circuit simulations. The gated lateral β was already measured in Fig. 6.4.7.

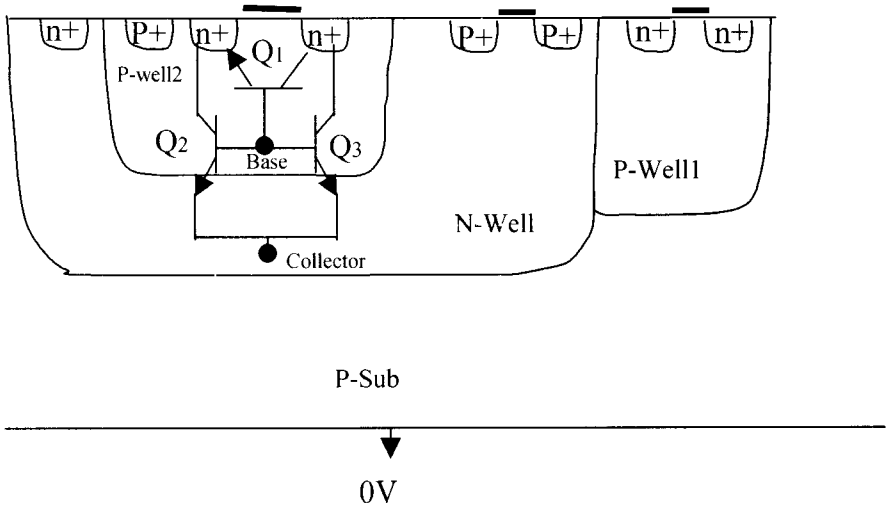


Fig. 6.6.3 Cross section of a triple well

The operation of the model in the forward active region is illustrated in Fig. 6.6.4. It consists of four active devices. They are an NMOS, one lateral (Q1) and two parasitic vertical bipolar transistors(Q2, Q3). In the forward active region of operation, Q1 and Q3 are in the forward active region and Q2 is off because the MOSFET gate has been tied to drain.

Notice that gate is negative or tied to the source to place the NMOS in the off state. If we measure Ie, Ic, Is, and Ib then we can find β of the lateral Q1 by the following relationship.

β of Q1 = Ic1/Ib1

where Ib1=Ib/2, Ic1=Ic-Ic3

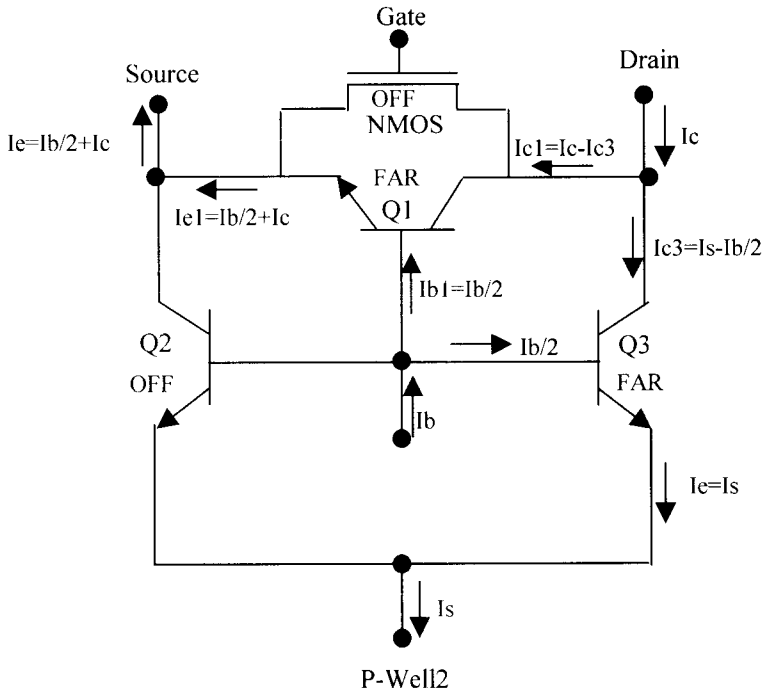


Fig. 6.6.4 Model operation in the forward active region

As shown in Fig. 6.6.5, the simulation of drain currents is very accurate when compared to the measured values. It does not show the degradation effect after the log conformity(square law region) while the measured curves do. This is from the fact that the ideal BJT model was used in this simulations.

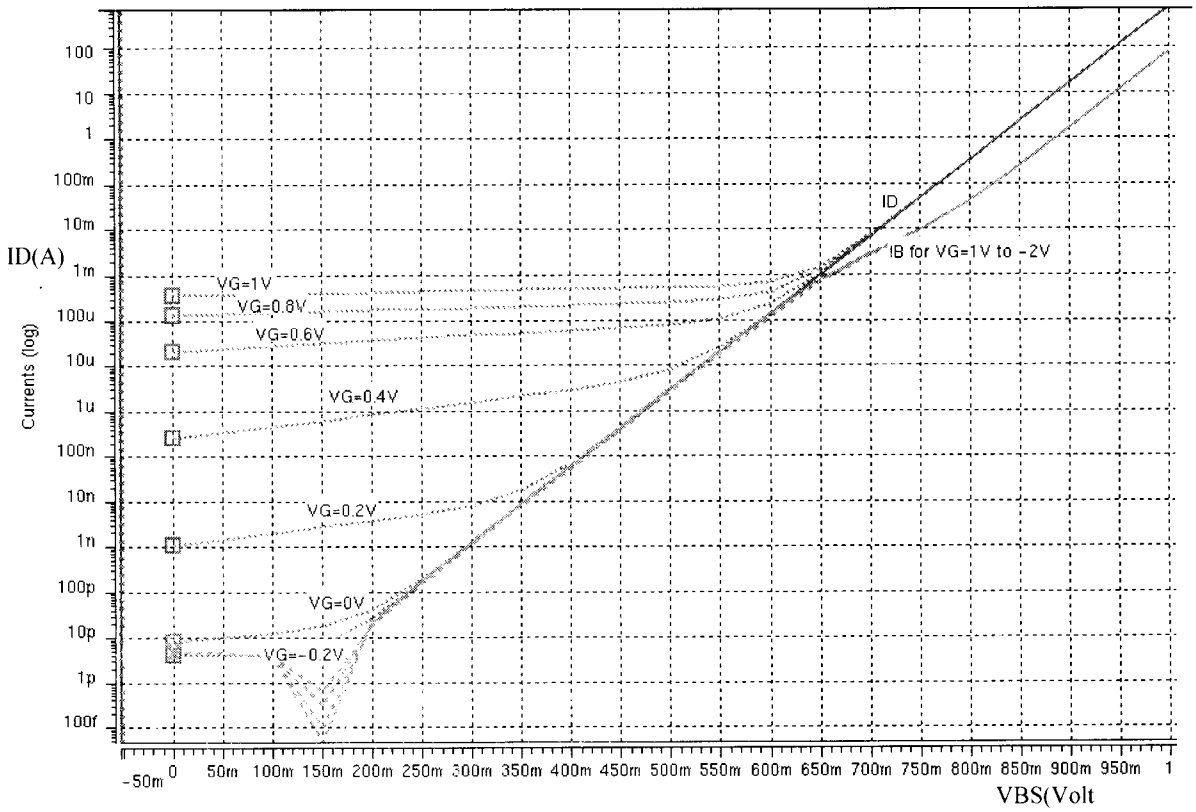


Fig. 6.6.5 Simulations for Fig. 6.4.5

Fig. 6.6.6 shows the simulation for drain currents ID as a function of VG with different VB values. The region of BJT action starts at VG=-2V while Fig. 6.4.6 gives the measurements in which VG= -1V is used to attain the pure BJT action. This deviation is also from the ideal BJT model used.

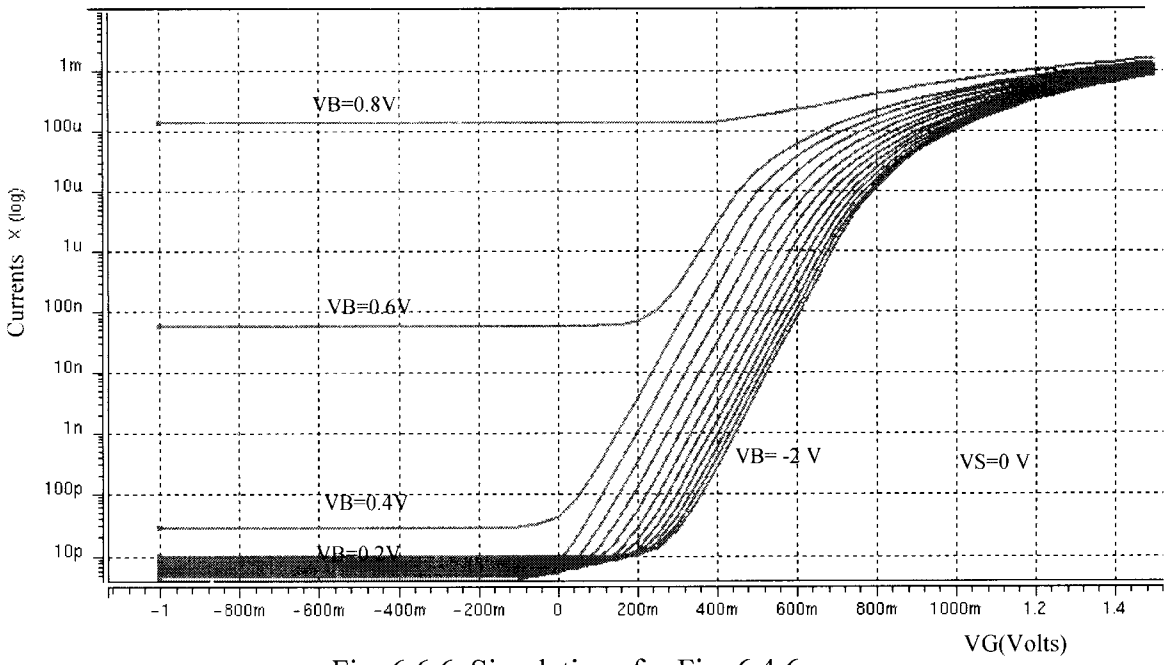


Fig. 6.6.6 Simulations for Fig. 6.4.6

Fig. 6.6.7 shows the gummel plot with different β values in which β=20 was used for all BJT's in the first simulation and 100 used in the second simulations in a BSIM2 model. Fig. 6.6.8 represents the gated β with VB=VG as in the Fig. 6.4.7.

Notice that the gated β is more than 1000 as obtained by using hybrid mode and after VG=0.75V it goes back to the original β value. This is the same results as in Fig. 6.4.7 even if there is a deviation between measurement and simulation.

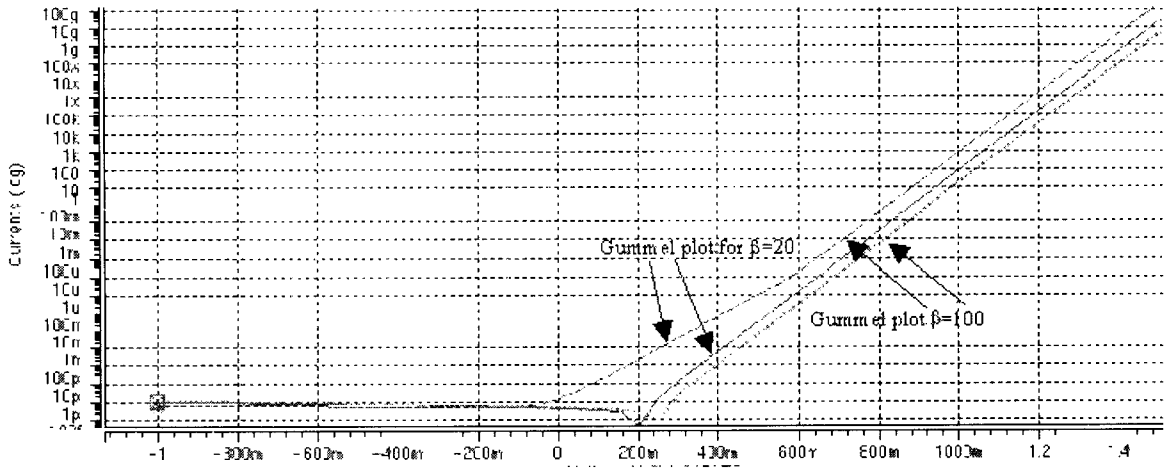


Fig. 6.6.7 Simulations for Gummel plot with different β

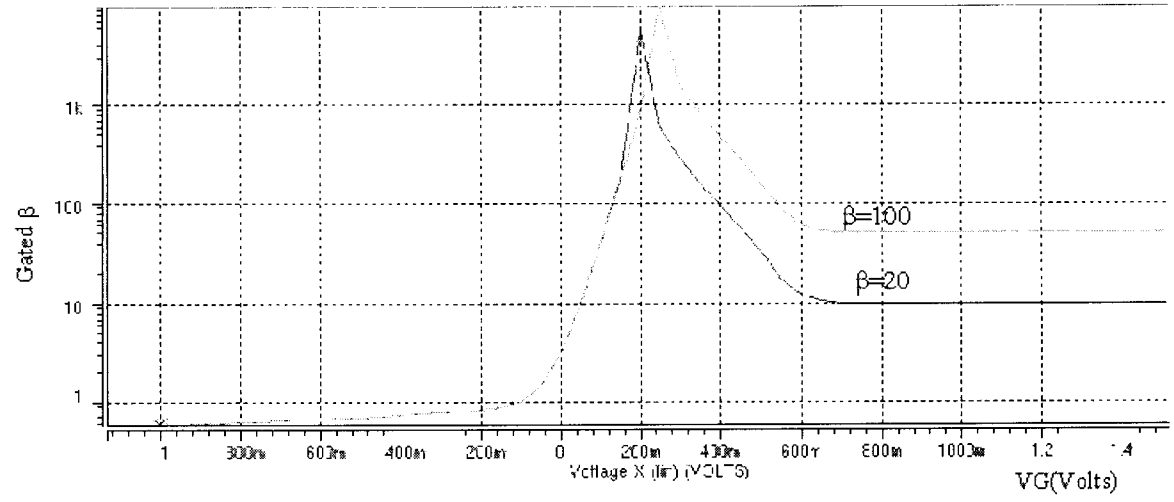


Fig. 6.6.8 Simulations for Fig. 6.4.7

6.6.2 CIRCUIT FOR A PROPOSED GATED BJT CURRENT SENSE AMPLIFIER

The proposed current sense amplifier is shown in Fig. 6.6.2.1. During the precharge time, bleq(**bit**line **eq**ualization), bish(**bit**line **i**solation **h**igher block), and bisl(**bit**line **i**solation **l**ower block) are high. N-latch signal, sz, and restore, rto, are maintained half Vdd during this precharge time to disable the n-latch and p-latch. The res(restore for cell) comes up high to make bitline(sa) and bitline*(saz) maintain a value of half Vdd provided by Vblp. The bases of the gated BJT's are grounded by N31 and N32 NMOS transistors during this precharge time. At the end of precharge, a wordline fires and then restore, res, comes low (0V) for a short time period turning PMOS transistors (P11 and P12) on.

This PMOS actions cause Ib to flow from the storage node of cell capacitor into the base of Q0 or Q1. The collector current is amplified β times and triggers the cross coupled latch. This operation is shown in Fig. 6.7.4 and Fig. 6.7.5. Notice that the proposed sense amplifier employs Vdd=1.5 and the precharge voltage is 0.75V

In Fig. 6.6.2.1, a collector current of P21, I_{21}, ($I_{21}=I_5+Ic$) is becomes huge because Ic is very large. This makes a drain resistance, rds, of NMOS(N5) low so that the drain voltage of N5 comes down and the other side (drain voltage of N28) goes up rapidly. Eventually this operation enables latch action (rto=high, sz=low).

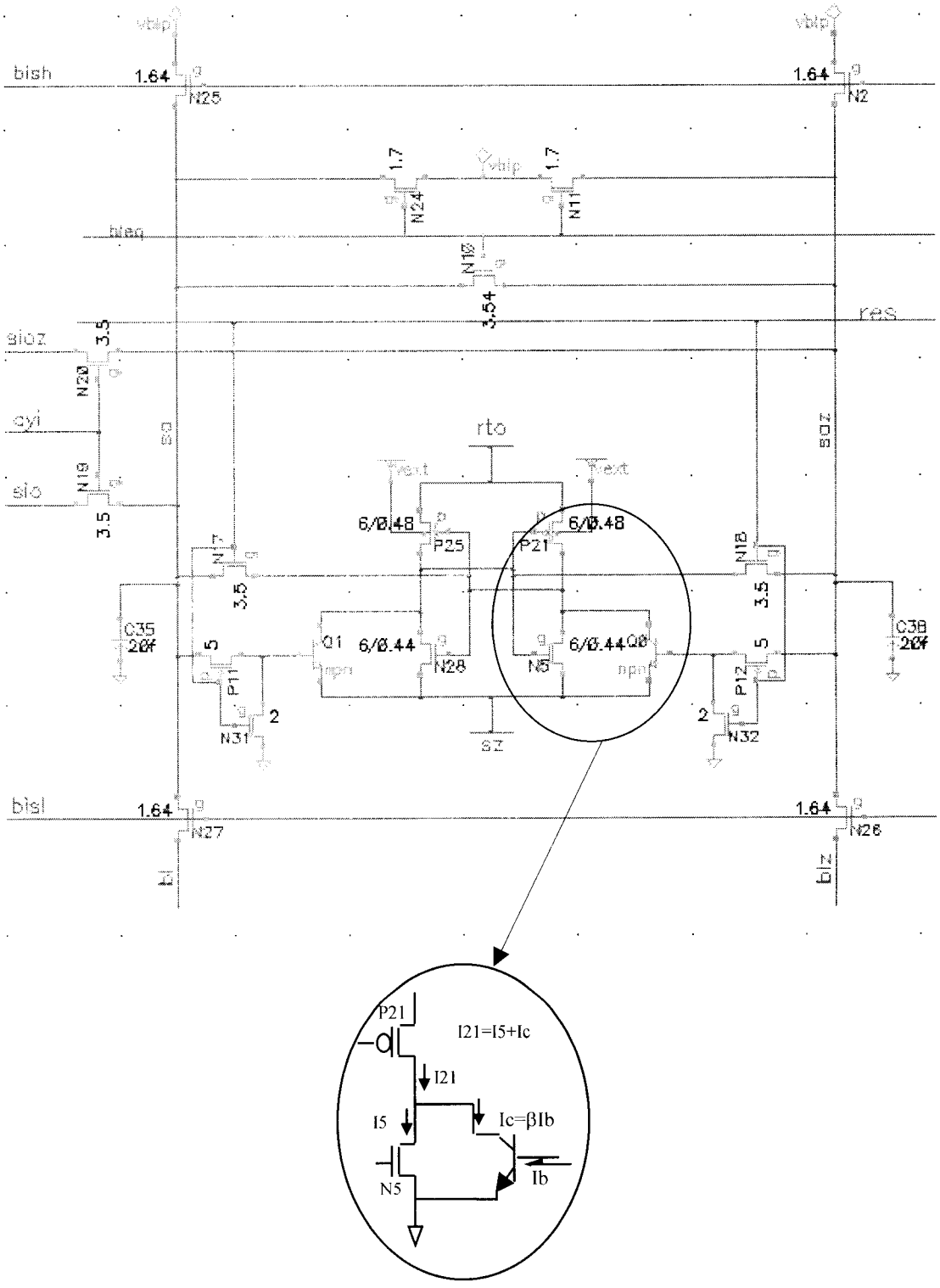


Fig. 6.6.2.1 Gated BJT current sense amplifier

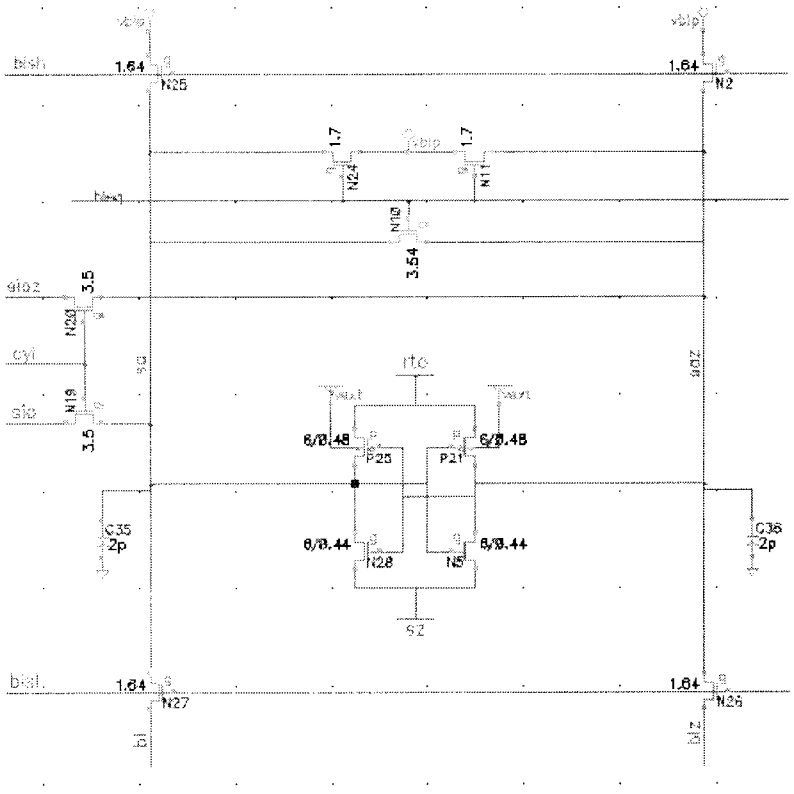


Fig. 6.6.2.2 Conventional voltage sense amplifier

6.6.3 LAYOUT BETWEEN A CONVENTIONAL AND CURRENT SENSE AMPLIFIER

Fig. 6.6.3.1 shows the layout for the conventional voltage sense amplifier as shown in Fig. 6.6.6.2 by using 0.44 μm twin-well CMOS process and the size is $33.72\,\mu m$ x $12.11\,\mu m$ $= 408.35\,\mu m^2$.

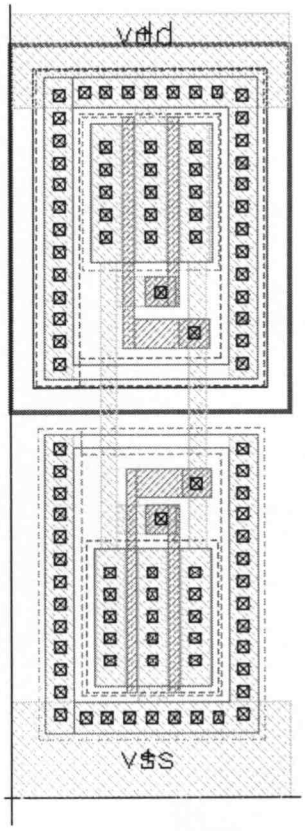


Fig. 6.6.3.1 Layout of a conventional voltage sense amplifier

Fig. 6.6.3.2 represents the gated BJT current sense amplifier for Fig. 6.6.6.1 which has the additional eight transistors. The size is 24.05 μm x 17.88 μm for PMOS parts and 33.72 μm x 15.93 μm for NMOS. The total is 967.1 μm^2 which is 2.4 times bigger than the conventional sense amplifier.

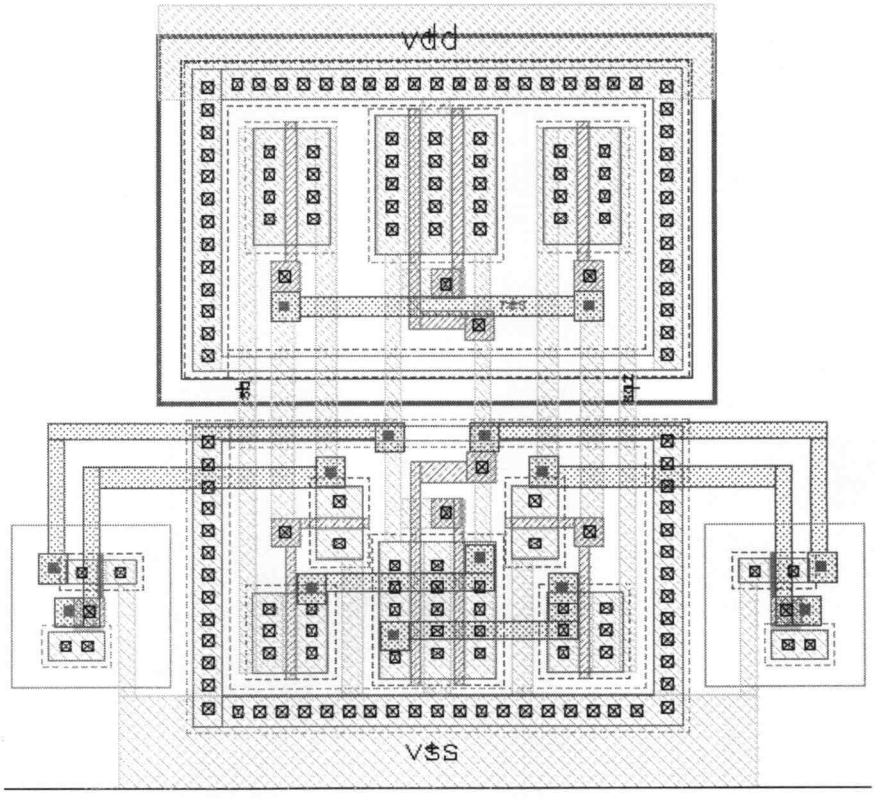


Fig. 6.6.3.2 Layout of a gated BJT current sense amplifier

6.6.4 RESPONSE TIME DEPENDENCE ON BITLINE CAPACITANCE

Fig. 6.6.4.1 illustrates the response time as a function of capacitances for both the conventional and the proposed gated lateral BJT current sense amplifer.

As shown in Fig. 6.6.4.1 the proposed current sense amplifier has much faster response time than that of the conventional amplifier for higher values of bitline capacitances.

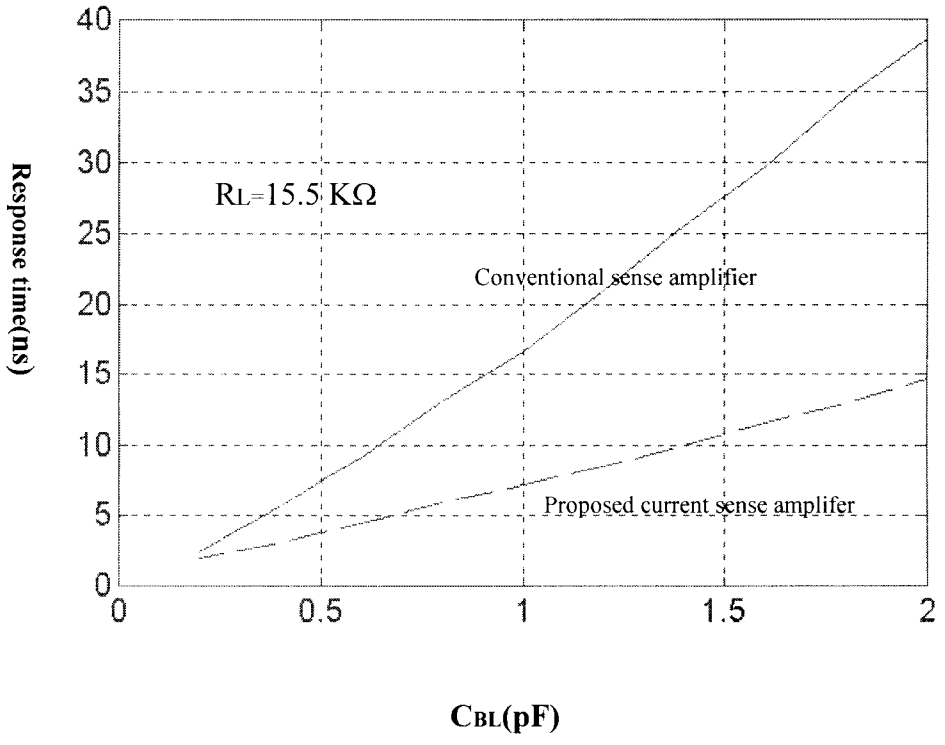


Fig. 6.6.4.1 Simulated response time versus bitline capacitance(R_L=15.5KΩ)

6.7 CIRCUIT SIMULATIONS

Fig. 6.7.2 represents a simulation modeling for four cells with bitlines. In Fig. 6.7.2 , "3p" means a 3π transmission line of a polysilicon bitline for Hyundai 128 Mega Synchronous DRAM. Notice that this device employs Poly-I for wordlines, Poly-II for bitlines, Poly-III for storage nodes, and Poly-IV for cell plates including two level of metals.

A transmission line model for the polysilicon bitline can be represented by the 3π model as shown in Fig. 6.7.3 because it has less than 3 % error than a lumped 1π model. The layout length of polysilicon bit line for the one wordline is 0.55μm and width is 0.24μm, then 520 x 0.55μm = 286 μm. Total number of squares to calculate a sheet resistance Rs = 286 μm/0.24μm=1192 squares. If Rs for the polysilicon is 13 ohms/square then Rbit=1192 x 13 = 15.5 kohms.

The justification we use for the gated current sense amplifier is the fact we can save area by adding an increased number of wordlines attached to the proposed current sense amplifier. This can reduce a lot of area because we do not have to separate the wordline as usual every 520 wordlines to maintain a limited capacitance.

For example of Hyundai 64MDRAM, the number of rows is 8192(8k). The conventional sense amplifier has a limitation in not having more than 520 wordlines on one side of sense amplifier. There should be less than 150fF of bitline capacitance for an acceptable sense amplifier sensitivity.

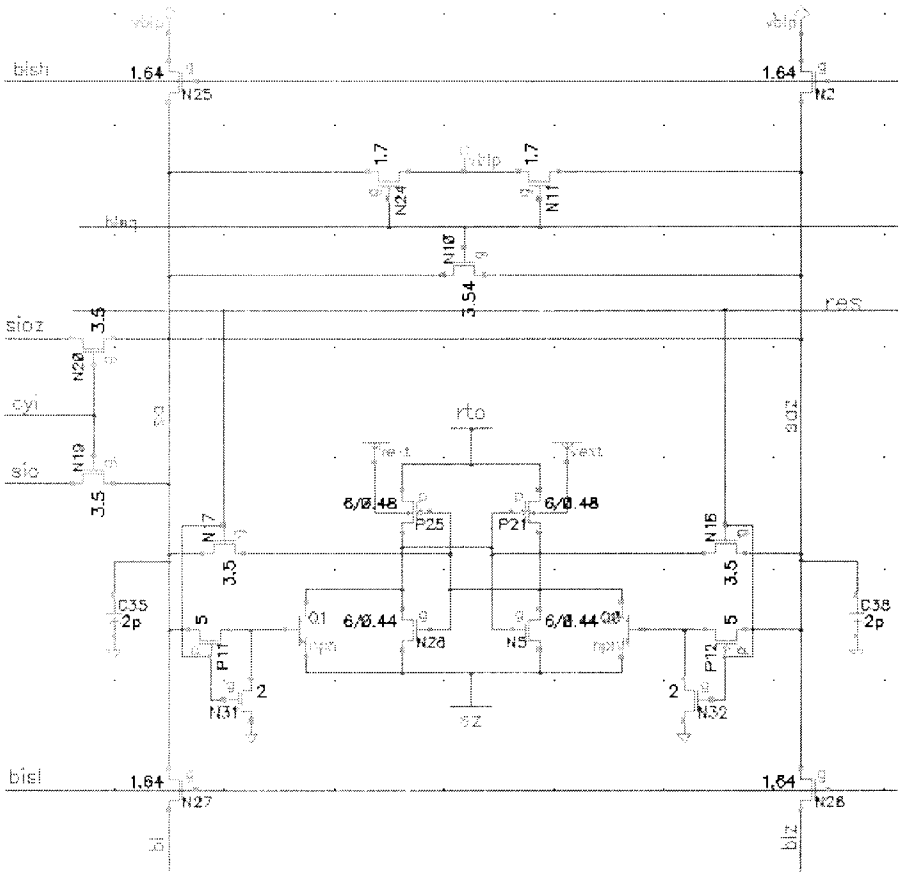


Fig. 6.7.1 Proposed gated BJT current sense amplifier

Hence the conventional sense amplifier has the 1040 wordlines at both ends. Therefore we need at least eight conventional sense amplifiers for the bit lines. However if the

proposed current sense amplifier is used, just one current sense amplifier is enough because the bitline capacitance is 1.2pF(150fF x 8 =1.2pF for one side) which is tolerable.

The bit line capacitance can be calculated by Cdb, Miller capacitance Cgd for each, transistor and the layout bitline stray capacitance.

For 0.24 μm polysilicon for 520 rows, we can estimate the bitline capacitance as Cbit=150fF. This Rbit· Cbit (Rbit·Cbit=15.5 KΩ· 150fF) product can be represented by 3π model as shown in Fig. 6.7.3.

Fig. 6.7.4 shows the bit line waveforms when a data zero was read by the proposed current sense amplifier while Fig. 6.7.5 shows the bit line waveforms when a data one was read. As shown in Fig. 6.7.4 the wordline fires(comes up high) during the precharge time and then restore, res, comes down for a short time doing which the gated lateral BJT triggers. Then sz for the n-latch* becomes low and, rto for the p-latch becomes high to enable cross-coupled latch.

Fig. 6.7.6 shows the gated BJT current sense amplifier(**b**) with an equlibration circuit(**a**) and 4 cells connected to wordlines and bitlines(**c**) and Fig. 6.7.7 illustrates the restore (rto) and n-latch*(sz) generation circuits. Fig. 6.7.8 shows each waveform for Fig. 6.7.7 and Fig. 6.7.8. In Fig. 6.7.8, if bsg(**b**itline **s**ensing **g**eneration) is low and bleq is high during the precharge then rtoextz= high, rtoez= high, and sze= low are the outcome. After precharge, the wordline fires and then the sensing action starts. When bsg(**b**itline **s**ensing **g**enerator) is low, Vg of N52 is high and Vg of N53 is low in Fig. 6.7.7. Then bsg changes to high(after wordline fires) in which case Vg of N53 jumps up to high rapidly.

However Vg of N52 comes up to high after a short pulse delay like a glitch which corresponds to five inverter's delays(I27, I21, I23, I0, I28) at net366 node as shown in Fig. 6.7.8. This short pulse makes rtoextz and rto have the pulses as shown in Fig. 6.7.8. This rto output is applied to one input of the differential sense amplifier(N48, N49, N50, P53, p54). This rto(3.3V) and Vg(Vint=1.5V) of N49 are compared by this amplifier and net366 outputs high(Vext=3.3V) during the glitch time and this output is held due to a disabled Vg of N50. Notice that the differential amplifer is enabled only for the glitch period. Therefore rto is boosted to Vext(3.3V) and then changed to the internal level(Vint=1.5V) by rtoez in Fig. 6.7.6(a). This is a technique to speed up charging a big capacitive load rapidly like the rto node loaded by over 100 sense amplifiers. All timing waveforms are plotted in Fig. 6.7.8.

Fig. 6.7.9 represents the response time comparison between the conventional and gated BJT current sense amplifier output. Before the wordline is fired, the bitlines(bl, blz) are maintained at half Vdd. After the wordline fires the sz is coming down from half Vdd to 0V and at the same time or a little bit later rto goes up from one half Vdd to Vdd level to enable the cross coupled latch. For the conventional voltage sense amplifier, the response time is 38.6ns which represents the time at 1V differential output of sense amplifier minus the rto enable time. The gated BJT current sense amplifier has a timing of 14.7ns. The gated BJT current sense amplifier is 23.9 ns faster than conventional voltage sense amplifier. That output was measured under Cbit=2pF worst case.

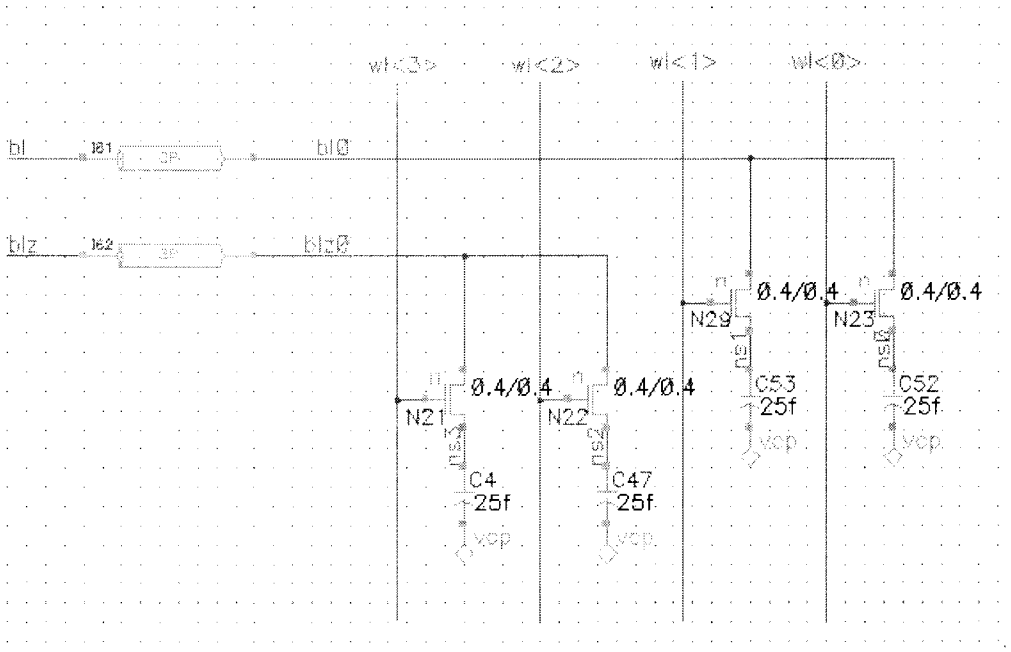


Fig. 6.7.2 Four cells with bit line modelings

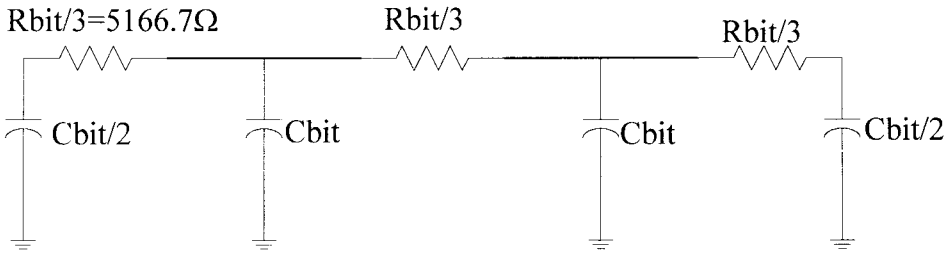


Fig. 6.7.3 Bitline TL modeling by 3π model

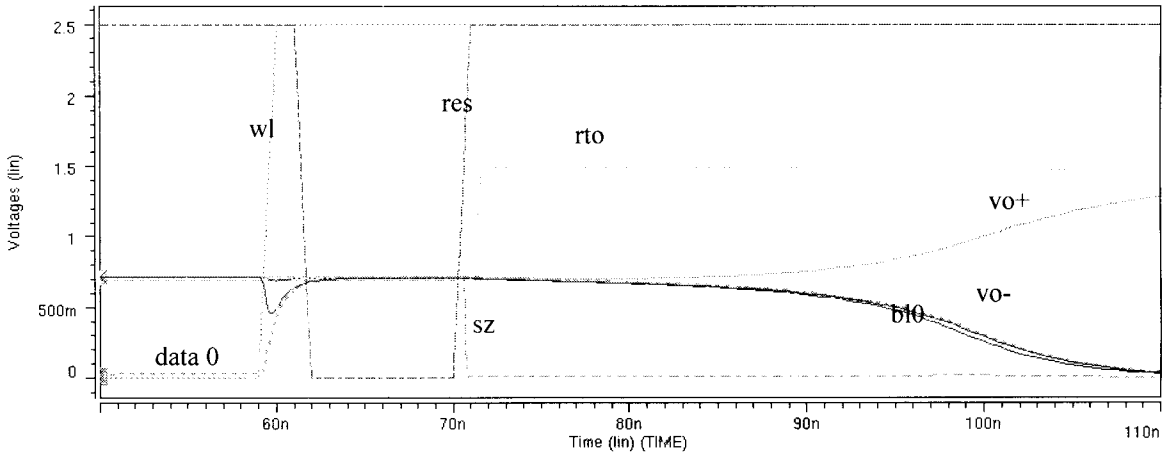


Fig. 6.7.4 Waveforms for read data zero (data 0 = 0V)

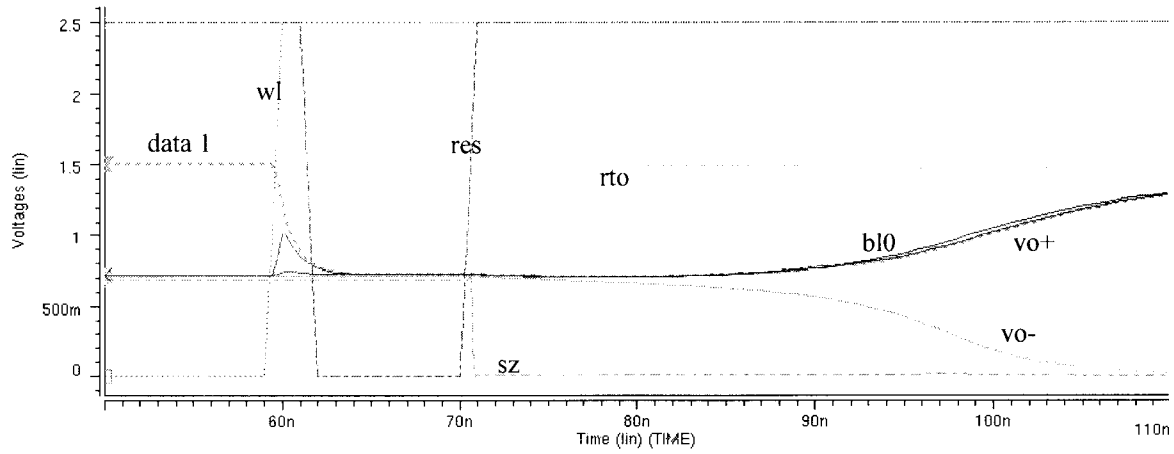


Fig. 6.7.5 Waveforms for read data one (data 1 = 1.5V)

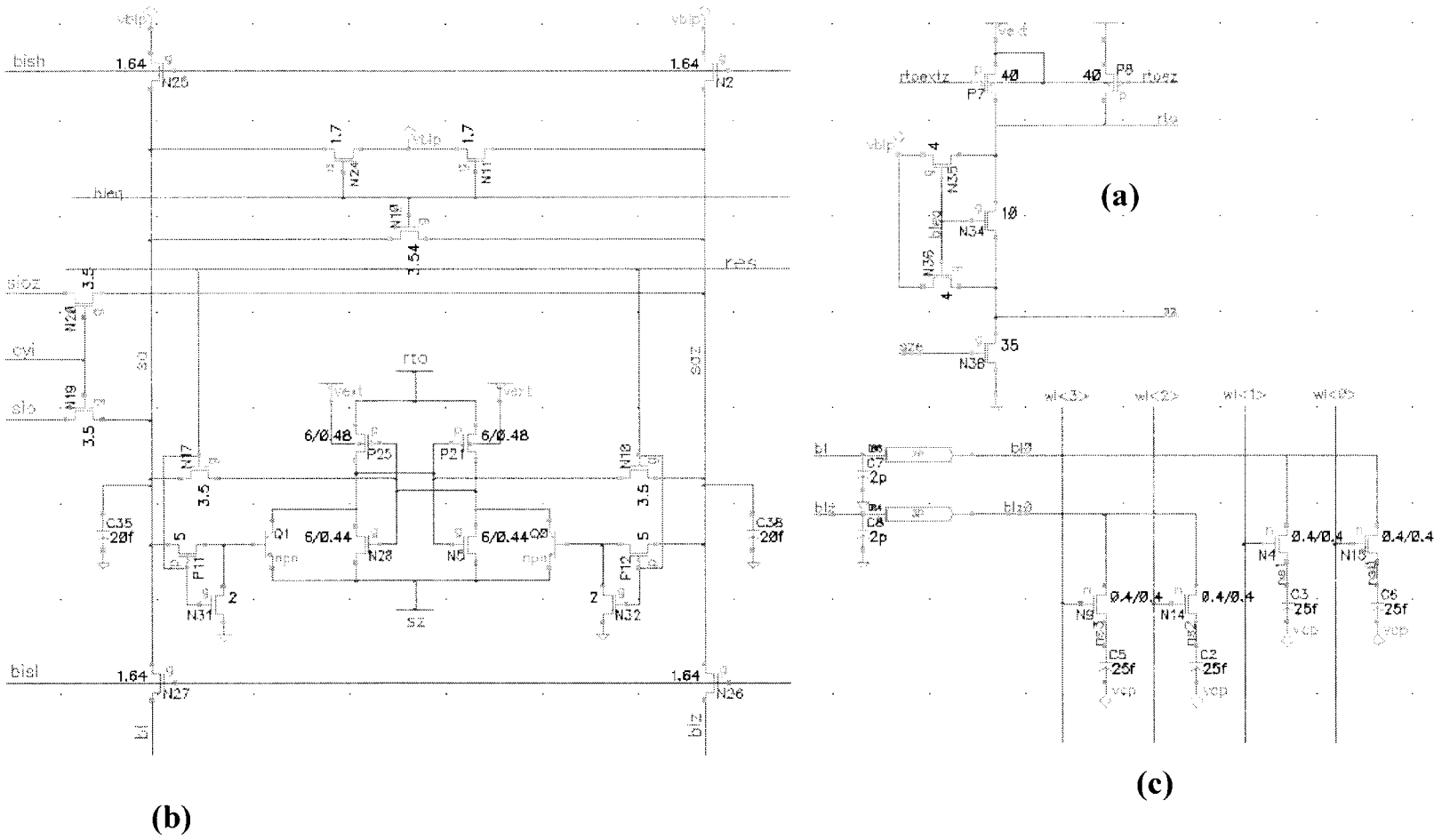


Fig 6.7.6 Gated current sense amplifier with four rows

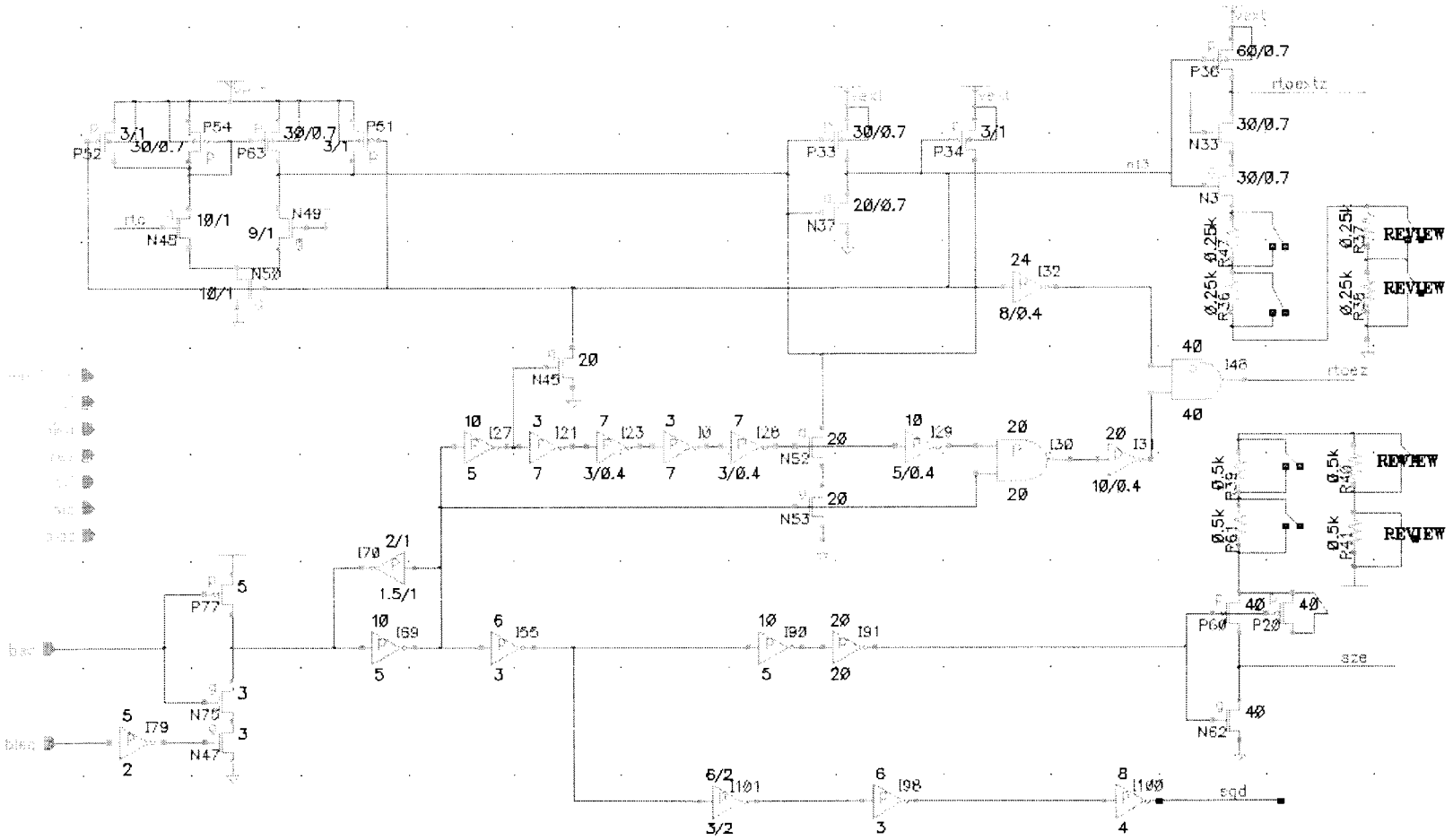


Fig 6.7.7 rto and sz signal path

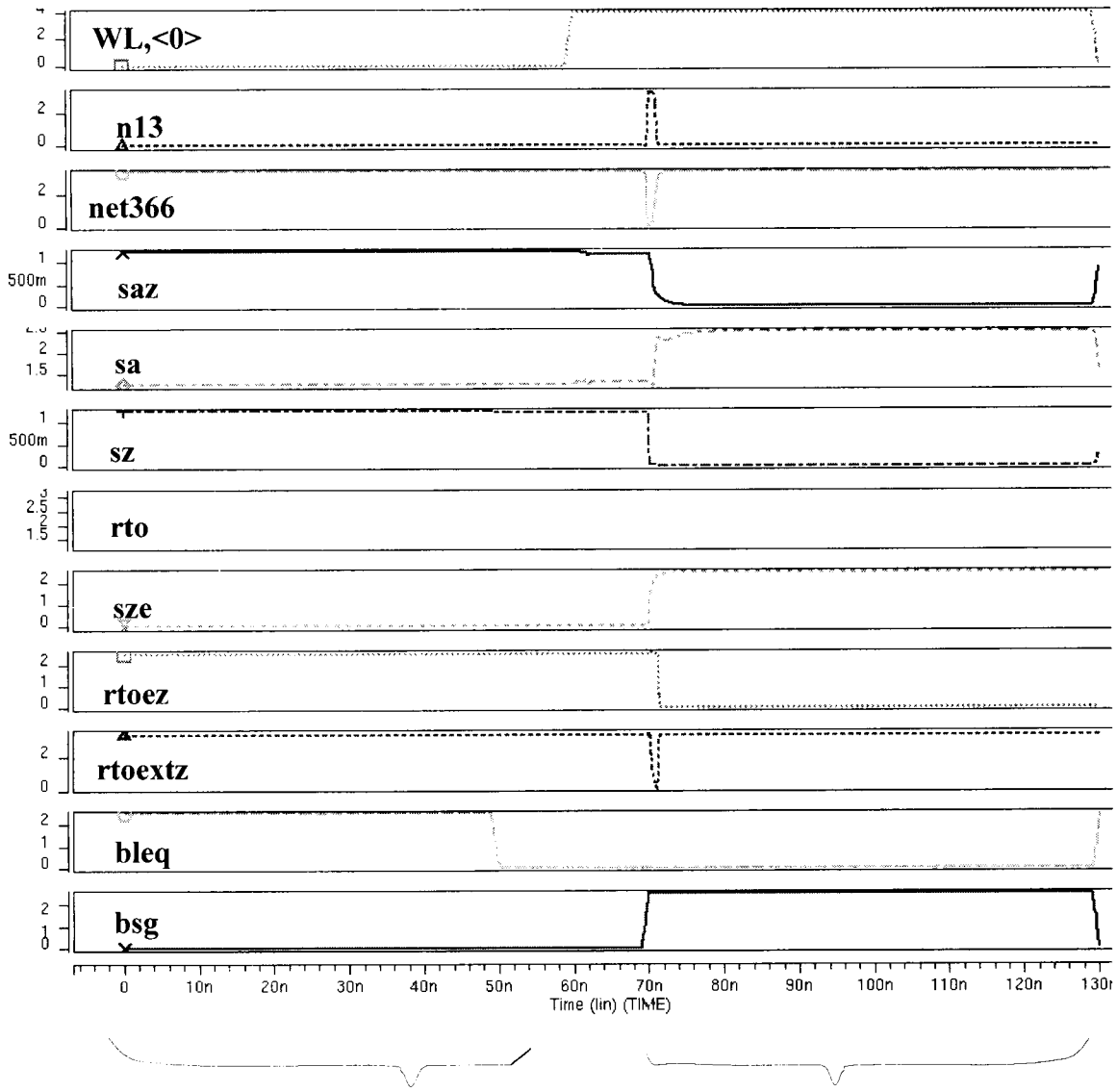


Fig. 6.7.8 Waveforms for precharging and sensing

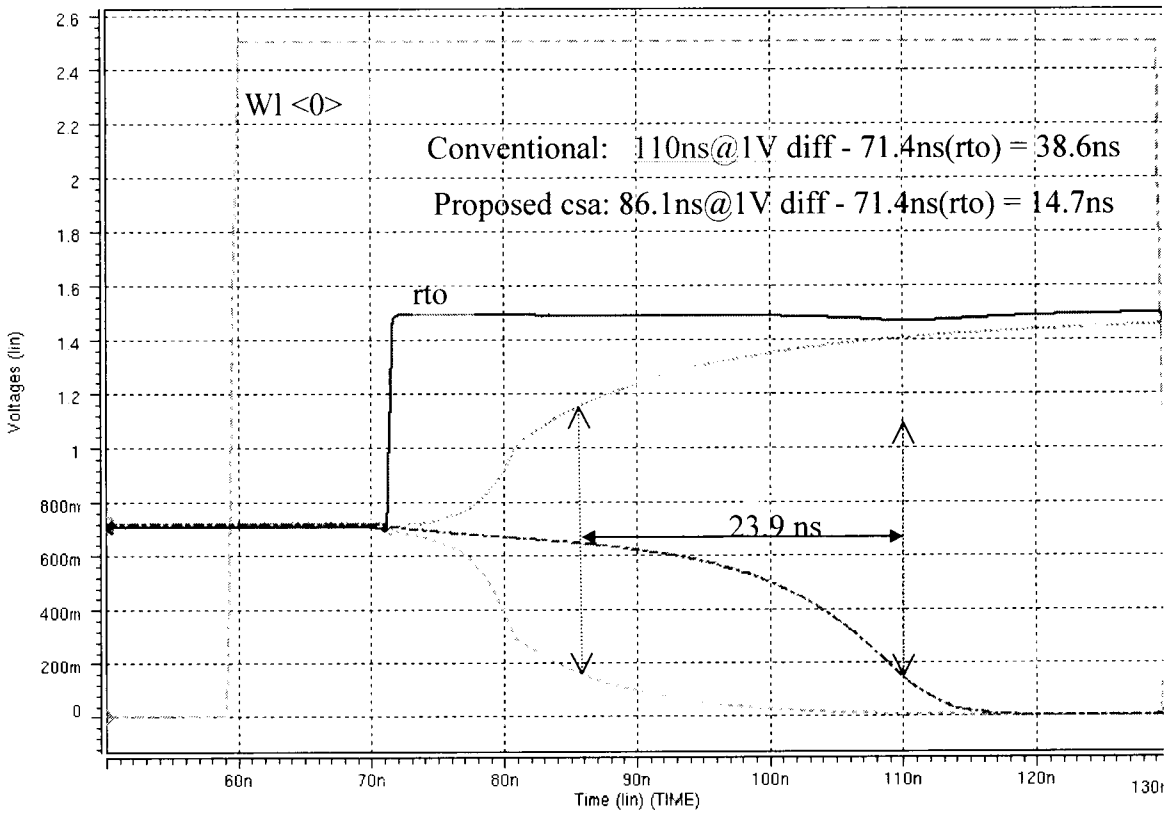


Fig. 6.7.9 Response time between a conventional and gated BJT current sense amplifier

7. CONCLUSIONS

	Conventional MOS	GBB-MOS	GB-MOS
Area	Normal	Big	Big
Current drivability	Normal	Big	Normal
Function	MOS	MOS + BJT + Bulk effect	MOS + Bulk effect
VT (Threshold voltage)	Big	Small for GB-MOS Big for BJT	Small

Table 7a Relative comparison between different transistors

	Conventional sense amplifier	Proposed gated BJT current sense amplifier
Operating voltage	Can't work under Vdd=1.5V	Easily done down to Vdd=0.5V
Response time @VDD=1.5V	38.6 ns	14.7 ns (62 % faster in this proposal)
CBL dependency	High	Less
Sensing method	Voltage	Current
Number of transistors connected	Limited(~500fF) (512 word lines)	Unlimited(several pF)
Sense amplifier area	1	~2 times

Table 7b Sense amplifier comparison

The GBB-MOS(gate-to-base body connected MOS) has an excellent possibility for ultra low voltage and fast operation because the forward body bias reduces the threshold voltage. The gated BJT current sense amplifier is proposed and the response time is compared to conventional voltage sense amplifiers. The response time of the proposed current sense amplifier is 14.7 ns while the conventional voltage sense amplifier is 38.6ns. If a β(current amplification factor) = 100 for a simple BJT is used, the resulting response time is 23.9 ns faster.

The proposed current sense amplifier is at least 62 % faster than the conventional voltage sense amplifier when a β(current amplification factor) = 100 is used. However when it used as a gated lateral BJT we can expect the performance to be much faster than the conventional sense amplifier because β is much larger than 1000 if the design is well optimized. The gated current sense amplifier is a good possibility in ultra low power supply circuits with fast speed. It requires more chip space as a result of the contact between the gate and body for each peripheral transistor and six extra transistors.

REFERENCES

1. D. MacSweeney, K. McCarthy, A. Mathewson, and B. Mason, "Modeling of lateral bipolar devices in a CMOS process," IEEE Proc. of Bipolar Circuits and Technology Meeting, Minneapolis, MN, Sept. 1996, pp. 27-30.

2. S. Verdonckt-Vandebroek, S. S. Wong, J. C. S. Woo, and P. K. Ko, "High-gain lateral bipolar action in a MOSFET structure," IEEE Trans. Electron Devices, vol. 38, no. 11, pp. 2487-96, Nov. 1991.

3. K. Joardar and J. Ford, "Modeling anomalous collector current behavior in gated lateral bipolar transistor," IEEE Proc. of Bipolar Circuits and Technology Meeting, 1993, pp. 193-196.

4. K. Joardar, "An analytical model for collector currents in gated lateral bipolar transistors," IEEE Proc. of Bipolar Circuits and Technology Meeting, 1992, pp. 221-224.

5. S. A. Parke and C. Hu, "A high-performance lateral bipolar transistor fabricated on SIMOX," IEEE Electron Device Letter, vol. 14, no. 1, pp. 33-35, Jan. 1993.

6. K. Joardar, "An improved analytic model for collector currents in lateral bipolar transistors," IEEE Trans. Electron Devices, vol. 41, no. 3, Mar. 1994.

7. M. J. Chen, J. S. Ho, and D. Y. Chang, "Optimizing the match in weakly inverted MOSFET's by gated lateral bipolar action," IEEE Trans. Electron Devices, vol. 43, no. 5, pp. 766-773, May. 1996.

8. W. T. Holman and J. A. Connelly, "A compact low noise operational amplifier for a 1.2um digital CMOS technology," IEEE J. Solid -State Circuits, vol. 30, no. 6, pp. 710-14, 1995.

9. T. Kirihata, S. H. Dhong, L. M. Terman, T. Sunage, and Y. Taira, "A variable precharge voltage sensing," IEEE J. Solid -State Circuits, vol. 30, no. 1, pp. 25-28, 1995.

10. P.G.Y. Tsui, P. V. Gilbert, and S. W. Sun "A versatile half-micron complementary BiCMOS technology for microprocessor-based smart power applications," IEEE Trans. Electron Devices, vol. 42 no. 3, pp. 564-570, Mar. 1995.

REFERENCES(Continued)

11. T. Fuse, Y. Oowaki, M. Terauchi, S. Watanabe, M. Yoshimi, K. Ohuchi, and J. Matsunaga, "0.5V SOI CMOS pass-gate logic," IEEE Int. Solid State Circuits Conf., Dig. Tech. Papers, pp. 88-89, 1996.

12. Y. Puri, "Substrate voltage bounce in NMOS self-biased substrate," IEEE J. Solid - State Circuits, vol. Sc-13, no. 4, pp. 515-519, 1978.

13. W. L. M. Huang, K. M. Klein, M Grimaldi, M. Racanelli, S. Ramaswami, J Tsao, J. Foerstner, B. Y. C. Hwang, "TFSOI complementary BiCMOS technology for low power applications, "IEEE Trans. Electron Devices, vol. 42, pp. 506-512, Mar. 1995.

14. K. Suma, T. Tsuruda, H. Hideto, T. Eimori, T. Oashi, Y. Yamaguchi, T. Iwamatsu, M. Hirose, F. Morishita, K Arimoto, K. Fujishima, Y. Inoue, T. Nishimura, and T. Yoshihara, "An SOI-DRAM with wide operating voltage range by CMOS/SIMOX technology," IEEE J. Solid-State Circuits, Vol. 29, no. 11, pp. 1323-1329, Nov. 1994.

15. S. Kuge, F. Morishita, T. Tsuruda, S. Tomishima, M. Tsukude, T. Yamagata, and K. Arimoto, "SOI-DRAM circuit technologies for low power high speed multigiga scale memories," IEEE J. Solid-State Circuits, vol. 31, no. 4, pp. 586-591, Apr. 1996.

16. K. Shimomura, H. Shimano, F. Okuda, N. Sakashita, T. Oashi, Y. Yamaguchi, T. Eimori, M. Inushi, K. Arimoto, S. Maegawa, Y. Inoue, T. Nishimura, S. Komori, K. Kyuma, A. Yasuoka, H. Abe, "A 1 v 46ns 16Mb SOI-DRAM with body control technique," IEEE Int. Solid State Circuits Conf., Dig. pp. 68-69, 1997.

17. B. Stellwag, J.A. Cooper, Jr., and M. R. Melloch, "A vertically integrated GaAs bipolar DRAM cell," IEEE Trans. Electron Devices, vol. 38, no. 12, pp. 2704, Dec. 1991.

18. T. Fuse, Y. Oowaki, T. Yamada, M. Kamoshida, M. Ohta, T. Shino, S. Kawanaka, M. Terauchi, T. Yoshida, G. Matsubara, S. Yoshioka, S. Watanabe, M. Yoshimi, K. Ohuchi, S. Manabe, "A 0.5V 200MHz 1-stage 32b ALU using body bias controlled SOI pass-gate logic," Dig. IEEE Int. Solid-State Circuits Conf., Dig. San Francisco," pp. 286-287, 1997.

19. M. Harada, T. Douseki, and T. Tsuchiya, "Suppression of threshold voltage variation in MTCMOS/SIMOX circuit operating below 0.5 V," IEEE Symp. VLSI Technology Digest of Technical Papers, pp. 96-97, 1996.

REFERENCES(Continued)

20. M-J. Chen, J-S. Ho, T-H. Huang, C-H. Yang, Y-N. Jou, and T. Wu, "Back-gate forward bias method for low-voltage CMOS digital circuits," IEEE Trans. Electron Devices, vol. 43, no. 6, Jun. 1996.

21. M. Saito, J. Ogawa, K. Gotoh, S. Kawashima, and H. Tamura, "Technique for controlling effective Vth in multi-gbit DRAM sense amplifier," IEEE Symp. VLSI Technology Digest of Technical Papers, pp. 106-107, 1996.

22. K. Gotoh, J. Ogawa, M. Saito, H. Tamura, and M. Taguchi, "A 0.9 v sense amplifier driver for high-speed Gb-scale DRAMs," IEEE Symp. VLSI Technology Digest of Technical Papers, pp. 108-109, 1996.

23. K-C. Lee, C-H. Kim, D-Y. Yoo, J-H. Sim, S-B. Lee, B-S. Moon, K-Y. Kim, N-J. Kim, S-M. Yoo, J-H. Yoo, and S-I. Cho, Low voltage high speed design for Giga-bit DRAMs," IEEE Symp. VLSI Technology Digest of Technical Papers, pp. 104-105, 1996.

24. Seevinck, P. J. V. Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAMs, "IEEE J. Solid-State Circuitss, vol. 26, no. 4, pp. 525-535, Apr. 1991.

25. G. Roientan and A. M. Sodagar, "High-speed current-mode sense amplifier," Electronics Letter, vol. 30, no. 17, Aug. 1994.

26. I. Y. Chung et al., "A new SOI inverter for low power applications," Proc. Int. SOI Conference, Saibei island, Florida, pp. 20-21, 30 Sep.-3 Oct. 1996.

27. R.C. Jaeger et al.,"A high-speed sensing scheme for 1T dynamic RAMs utilizing the clamped bit-line sense amplifier," IEEE J. Solid-State Circuits, vol. 27, pp. 618-25, 1992.

28. C.G. Splain et al., "Ultra low voltage complementary metal oxide semiconductor(ULV-MOS) circuits:bulk CMOS operation below threshold(VTO),"Proc. IEEE Southeast con, pp.670-3,1996.

29. Masaki Tsukude and Kazutami Arimoto., "Sense Amplifier including MOS Transistor Having Threshold Voltage Controlled Dynamically in A Semiconductor Device," United State Patent no. 5646900, Jul. 8, 1997.

30. Meta-Software, "HSPICE user's manual," Dec. 1992

REFERENCES(Continued)

31. S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits Analysis and Design," McGRAW-Hill, 1996

32. Brent Keeth, "A DRAM Circuit Design Tutorial," Micron Technology, Inc., 12/95

33. P. R. Gray and R. G. Meyer "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons, 1992 Third Edition