The purpose of this work is to develop a new model for LDD n-MOSFET degradation in drain current under long-term AC use conditions for lifetime projection which includes a self-limiting effect in the hot-electron induced device degradation. Experimental results on LDD n-channel MOSFETs shows that the maximum drain current degradation is a function of the AC average substrate current under the various AC stress conditions but not a function of frequency or waveforms or different measurement configurations. An empirical model is constructed for circuit applications. It is verified that the self-limiting in drain current is due to the thermal re-emission of a trapped-hot-electron in the oxide. Results show that self-heating during AC stress releases trapped electrons, which in turn limits the maximum amount of drain current degradation. Moreover, tunneling to and from traps model is employed to visualize the internal mechanism of thermal recovery of electrons under different bias conditions. Although the LDD device structure can reduce the hot electron effect, various processing technologies can also affect the device reliability. A carbon doped LDD device with the first and the second level metal and passivation layer but without any final anneal shows that a significant reduction in the shifts of the threshold voltage of MOSFETs with time can be
achieved. However, the long-term reliability projection of n-MOSFETs based on DC stress tests alone is shown to be overly pessimistic.

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Hot Electron Effects in N-Channel MOSFET's

By

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1. Introduction

The degradation of lightly doped drain (LDD) structure MOSFET's has been studied. In Part 2, hot electron effects under DC and AC stress with degradation mechanisms has been observed. The combination of hot electron injection under AC stress—when the gate voltage is one half or one third of the drain voltage, and then recovery when the gate voltage is zero—results in a saturation or self-limiting of the change in drain current with time under AC stress conditions. Also, the effects of gate-leads-drain and drain-leads-gate configurations, the voltage acceleration factors, frequency, and the AC substrate current have been determined and an empirical model is proposed to describe the drain current degradation under long-term AC use conditions. In the process of attempting to define a relationship between DC stress results and AC stress conditions we have identified and quantified the self-limiting or saturation mechanism to be in part thermal re-emission of trapped electrons which is extensively studied in Part 3.

In Part 3, the thermal re-emission of trapped hot electrons in n-channel LDD MOSFET's has been studied more carefully. Results show that self-heating during AC stress releases trapped electrons which then limits the maximum amount of drain current degradation. The Price-Sah model and DC test results are employed in order to quantify the induced self-limiting thermal re-emission model and locate the oxide trap energy level. A thermal activation energy of about 1.5 eV has been found for the oxide traps for electrons. Energy band diagrams are used to explain the recovery phase. The combination of electron trapping and self-heating tunneling re-emission of electrons causes drain current saturation during long term AC stress.
Part 4 covers the effects of different processes which can reduce the hot electron effects. The annealing effect of carbon in N-channel LDD MOSFET's has been studied. A carbon doped LDD device with first and second level metal and passivation layer but without any final anneal shows that a significant reduction in the shifts of threshold voltage of MOSFET's with time can be achieved.
2 Hot electron effects in MOSFETs under AC stress

2.1 Literature review

Recently, there has been extensive work on the hot electron induced degradation of short channel MOSFET's [1]. As the dimensions of the MOS device are scaled down to increase speed or density, hot-carrier degradation has become a major concern in the optimum design for VLSI reliability. The injection of hot electrons into the oxide under stress degrades the device characteristic as shown in Fig. 1. However, the hot carrier effects are closely related to the trapping/detrapping of the hot carriers in SiO₂ from the inversion layer [2], the interface and/or oxide trap generation by the injected carriers [3], and the electron-hole pair generation due to impact ionization [4]. The primary dominant degradation mechanisms in MOSFET's are discussed in the next section. Furthermore, the effects of change in device characteristics have troublesome effects on circuit operations such as access, precharge, and refresh time degradations in Megabit-level RAMs [5]. Two typical approaches to reduce the hot-carrier induced degradation are device structure changes [6] and ion implantation techniques for doping with C, F, and Ge [7]-[9]. The devices to be investigated for hot carrier degradation in Parts 2 and 3 are the well-known lightly doped drain (LDD) MOSFET while part 4 deals with the Carbon doped devices which can significantly reduce the device degradation.

Most of the degradation in n-channel MOSFET's due to hot electron effects after stress are a drain-to-source current reduction, a transconductance reduction, a substrate current increase due to impact ionization, and a lower drain-to-source breakdown. These characteristics have been studied and in particular, the LDD MOSFET shows a stronger self-limiting effect. W. Weber [10] proposes that this effect might come from a series resistance increase after long-term AC stress. However, we have
$V_D = 7.0 \text{ Volts}$  $V_G = 2.5 \text{ Volts}$

Aging Time = 1445 min

Figure 1. Threshold voltage shift under DC stress for device with different drawn gate length
identified and quantified the self-limiting or saturation to be thermal re-emission of trapped electrons in the n-channel LDD MOSFET's which is explored in Part 3. Moreover, we have characterized the drain-to-source current degradation is due to long-term AC stress, which is self-limiting in terms of the average substrate current, the ambient temperature, frequency, the gate and drain waveforms, and the different applied voltages. A simple degradation model with empirical results is also proposed in this work.

2.2 Dominant degradation mechanisms in MOSFET's

Generation, injection and tunneling to and from traps of electrons are three dominant degradation mechanisms in the device reliability. For generation and injection, the primary reasons are due to impact ionization and avalanche multiplication of the electron-hole pairs by high electric fields in the pinch-off region near the drain [4]. In the pinch-off region near the drain, the electrons and holes in the channel have experienced a large acceleration by the high drain voltage (Vds) and gate voltage with a value of about Vds/2. The distributions of the negative oxide charges by the trapping of hot electrons and the positive oxide charges by the trapping of hot holes near the drain will shift the threshold voltage. In addition, avalanche electron injection occurs when there is a voltage drop in the silicon surface layer at the SiO₂/Si interface to accelerate an avalanche injected electrons into the oxide over the SiO₂/Si barrier, where the injected electrons may break hydrogen bonds and strained bonds [3]. As a result of the avalanche carrier multiplication, a corresponding substrate current develops by diffusion of most of the holes generated due to impact ionization toward the substrate.

Recently, we have quantified another aspect of the injection of electrons into the oxide which is the tunneling to and from traps in the oxide [11] as described in section 3.3.
2.3 Self-limiting degradation model

To account for the hot-carrier generation and self-limiting effects in the long-term AC stress of n-channel LDD MOSFETs, a model for trapping/detrapping was undertaken. Fig. 2 and 3 illustrate schematic and energy band diagrams for a substrate current generated by hole diffusion after impact ionization close to the substrate. Since the substrate current has been a good monitor of device drain current degradation, the AC stress degradation is estimated by the average substrate current (\( I_{\text{Sub}} \)) which is calculated by the integration of the quasi-static DC substrate current over a period of AC stress waveforms. Hot electrons are assumed to be uniformly injected along the channel into the oxide in which there are a large number of electron trapping sites. The first-order kinetic rate equations of the trapped electrons are described in [12]. The electron injection rate (\( \gamma_{\text{inj}} \)) and emission rate (\( \gamma_{\text{emi}} \)) are indicated as follows:

\[
\gamma_{\text{inj}} = \alpha |I_{\text{Sub}}| \quad (1)
\]

\[
\gamma_{\text{emi}} = e_n n_t(t) \quad (2)
\]

where \( \alpha \) is an injection and trapping probability which is a constant independent on device gate length and applied voltages. \( n_t(t) \) is the number of the trapped electrons and \( e_n \) is the electron emission rate defined by:

\[
e_n \propto A(T) \exp(-E_t/kT) \quad (3)
\]

where \( A(T) \) is a fitting parameter of the measurements. \( E_t \) is the thermal activation energy which causes an electron to escape from the trap. Therefore, the trapped electron rate equation can be expressed as:
Figure 2. A schematic diagram for hot-carrier mechanisms on LDD MOSFET's.
Figure 3. An energy band diagram for hot-carrier mechanisms.
\[
\frac{\partial n_t}{\partial t} = \alpha \|I_{\text{sub}}\| - n_t(t) e_n
\]  

(4)

Assuming \( n_t(t) = 0 \) at \( t=0 \) and the reliability time constant \( \tau \) is defined as \( 1/e_n \), equation (4) can be solved to yield \( n_t(t) \) as:

\[
n_t(t) = \frac{\alpha \|I_{\text{sub}}\|}{e_n} (1-e^{-t/\tau})
\]  

(5)

under AC stress conditions. The amount of drain current degradation is then proposed as:

\[
\left| \frac{\Delta I_{d_s}}{I_{d_s}} \right| = C I_{\text{sub}} e^{E_t/kT}(1-e^{-t/\tau})
\]  

(6)

where \( C \) depends on the processing technology and bias condition under AC stress.

Equation (6) implies that there is a self-limiting effect in the long-term (\( t = \infty \)) AC stress and predicts a small \( I_{d_s} \) variation limited by the electron emission rate at high device temperatures. By setting \( t = \infty \), the self-limiting effects in drain current degradation is:

\[
\left| \frac{\Delta I_{d_s}}{I_{d_s}} \right| = C \|I_{\text{sub}}\| e^{E_t/kT}
\]  

(7)

2.4 Experimental setup and measurement

The devices used in this study were n-channel MOSFET's with a LDD structure and with a drawn gate length of 1.0 \( \mu \)m and a width of 50 \( \mu \)m. We also have results on two different gate lengths of \( L=0.8 \) \( \mu \)m and \( L= 1.5 \) \( \mu \)m in Part 2. The gate oxide thickness is 200 \( \text{Å} \) grown at 900\(^\circ\)C by oxidation. Fig. 4 shows the typical measurement set-up for AC stress. After reviewing recent publications [13], we placed our primary reliance on bonded
Figure 4. Typical measurement setup including 50 ohm cables for AC stress.
devices, taking special care to reduce ringing in the circuits by using a 50 ohm matching termination on all coaxial cables and a source follower configuration. The DC bias is used to adjust the pulse offset voltage and a digital voltmeter is used to measure the average substrate current which is only generated during the gate voltage transition with high drain voltage [3,4]. In this set-up, drain saturation current and average substrate current are monitored.

In the thermal recovery phase, an oven is employed with the AC set-up in order to set and maintain the device at a constant ambient temperature.

For DC tests, an HP4145 semiconductor parameter analyzer is used to bias the device and monitor the threshold voltage. An HP9836 desk-top computer controls the HP4145 and switching between the "stress" and "threshold voltage measurement" modes at predefined time intervals. Threshold voltage degradations were induced by hot electron injection at a gate voltage of 2.5 V, a drain voltage of 7.0 V, a source voltage of 0 V, and a substrate bias of 0 V. Under stress, the changes in threshold voltage, $V_T$, as measured with a drain to source voltage of 0.1 V, were monitored. At each monitoring time, we also exchanged the source and the drain to measure $V_T$ in the reverse direction. The transconductance, $g_m$, and drain current at $V_{ds} = V_{gs} = 5$ V were also monitored.

2.5 Review of DC stress results

In the present work, some devices were subjected to DC stress to confirm Haddad's previous DC results [7]. There was a small change in degradation with time if the gate and drain voltages were both at 7 volts, but an extremely rapid and large change if $V_{ds} = 7.0$ V and $V_{gs} = 2.5$ V, which are due to the conditions of the maximum substrate current as shown in Fig. 5. In Fig. 6, the one micron gate length n-channel device is in the linear region with small drain-to-source voltage. The transconductance degrades in the low gate voltage
Figure 5. The DC stress conditions for maximum substrate current for bonded devices.
Figure 6. Hot electron effects on drain current and transconductance after DC stress.

STRESS TIME

(1) \( t = 0 \text{ min} \)
(2) \( t = 128.2 \text{ min} \)
(3) \( t = 256.35 \text{ min} \)
(4) \( t = 1441.76 \text{ min} \)

W#15 No Carbon, 1.0 \( \mu \text{m} \) After Annealing
and there is a higher shift in threshold voltage after long periods of stress. In fact, if one considers only the initial part of the results of AC stress in section 2.6.1 over the first 1000 minutes before there is any self-limiting effect, then this might be related in a general way to the DC stress results with $V_{gs}=2.5 \text{ V}$ by a simple duty factor consideration.

However, since MOSFET's operate in dynamic stress in an actual VLSI circuit, a full AC stress is more important to characterize hot-carrier effects than a DC stress. Correlation between DC stress results in reliability tests and AC use condition has, at best, in the past been a projection. However, the projections of DC test results to AC use conditions is probably pessimistic.

2.6 AC stress results

2.6.1 Voltage acceleration factor

The self-limiting changes in drain current under AC stress conditions are shown in Fig. 7 and Fig. 8 for 1.0 micrometer and 0.8 micrometer drawn gate length devices. These figures show the self-limiting effect in drain current after different bias conditions and a long-term stress with measurement conditions of $V_{gs}=V_{ds}=5\text{V}$. The change in drain current tends to saturate in the order of 5,000 to 10,000 minutes and with a higher stress voltage suggests a smaller self-limiting change than with a lower voltage. This aspect is described by the exponential time dependence in (6) and the constant C has been determined from these experimental results to construct an empirical model in the section 2.7.

2.6.2 Effect of gate and drain waveform

Figure 9 shows the results for the drain-leads-gate configuration as opposed to gate-leads-drain and gives the substrate current for both 1.0 and 0.8 $\mu\text{ms}$ drawn gate lengths.
Figure 7. The self-limiting effects of stress voltage on drain current degradation for a 1 μm drawn gate length device.
Figure 8. The self-limiting effects of stress voltage on drain current degradation for 0.8 \( \mu \text{m} \) drawn gate length device.
Figure 9. Substrate current for configurations of (a) a drain leads gate and gate leads drain, and (b) a gate leads drain with additional 1.5 \( \mu m \) drawn gate lengths device under AC stress conditions.
From [14], only the variation of a leading or trailing gate voltage at high drain voltage can influence the degradation results. Contrary to some reports in the literature [14], we observe that there is no basic differences between gate leads drain and drain leads gate and the value of substrate current and the maximum amount of degradation are similar. Therefore, it is concluded that reports in the literature on the differences between the gate-leads-drain and drain-leads-gate configurations are probably due to the different waveforms or by not exercising sufficient care with experimental set-ups as is mentioned in section 2.4 and not a fundamental difference in the physics of the device.

2.6.3 AC substrate current

The substrate current has become a major parameter to monitor the amount of the device degradation [15]. The maximum value of this change is simply related to the maximum average substrate current which develops under AC stress conditions as shown in Fig. 10 in which the values are shown in the empirical model for 0.8 and 1.0 micrometer drawn gate length devices. This dependence is again consistent with the type of linear relationship given by (6). As a result, in Fig 10, there is a linear relationship between maximum drain current degradation and maximum average substrate current. However, the particular devices being used here are lightly doped drain devices. Any technique which will further serve to reduce substrate current will certainly tend to reduce degradation due to hot electron injections.

2.6.4 Frequency dependent

In Fig. 11, the relationship between LDD n-MOSFET's degradation and frequency is shown for 0.8 μm gate length devices. Since the substrate current, in general, increases with frequency,
Gate-Leads-Drain

$W = 50 \ \mu m, \ L = 1 \ \mu m$

$tr = tf = 80 \ \text{nsec}$

$td = 50 \ \text{nsec}$

Freq $= 4 \ \text{MHz}$

---

Figure 10. The linear relationship between maximum drain current degradation and maximum AC average substrate current for 0.8 $\mu m$ and 1.0 $\mu m$ devices.
Figure 11. The linear relationship between maximum drain current and maximum average substrate current for 0.8 µm devices under different frequencies.
the drain current degradation is also found to increase with frequency. The dashed line in Fig. 11 in which the slope is 0.3%/μA shows that our empirical self-limiting model is consistent with different frequencies for 0.8 μm devices. It has then been determined that the degradation results are based on the average substrate current for each of the different configurations and at each frequency. In short, it is possible to relate the degradation to the substrate current in DC tests as measured by Haddad [7], the results of which are shown in the following section. Moreover, it is anticipated that one of the important variables in the empirical model is the average substrate current, not frequency or other parameters such as waveforms, and particular measurement configurations (gate-leads-drain versus drain-leads-gate).

2.7 Empirical model for circuit applications

From an engineering point of view, these results suggest fitting the data to a working equation for engineering applications of the same form as (7) A more empirical form is given below:

\[ \frac{\Delta I_{ds}}{I_{ds}} = \alpha(L) \beta(T) I_{sub}(V_{ds},L)(1 - \exp(-e_n(Td,V_{ds},L)t)) \]

Eqn. (8) gives explicitly the dependence of the maximum degradation on substrate current after long time periods. The time constant is allowed to be a function of ambient temperatures, maximum operating voltage or power dissipation and thus device temperature, \( T_d \), and gate length. \( \beta(T) \), is a relative coefficient to account for deviations of ambient temperature of 25°C and is an exponential function of ambient temperature. Much smaller values of maximum amounts of degradation are observed at higher ambient. \( \alpha(L) \), is a proportionality constant. Figure 12 gives the dependence of substrate current on maximum drain voltage and
Figure 12. (a) The dependence of substrate current and time constant on maximum drain voltage and gate length. (b) The relative coefficient $\beta(T)$ versus ambient temperature.
gate length, the dependence of the time constant on gate length and voltage for an ambient temperature of \(25^\circ\text{C}\), and the relative correction given by \(\beta(T)\), to be applied to the maximum change or degradation for higher ambient temperatures.

The coefficient \(\alpha(L)\) which fits the data reasonably well is found to be \(0.2\%/\mu\text{A}\) of substrate current and \(0.3\%/\mu\text{A}\) for 1.0 and 0.8 micron devices with a gate width of 50 microns respectively. This describes the maximum change or degradation which can be anticipated at an ambient temperature of \(25^\circ\text{C}\). At higher ambient temperatures, Fig. 16 in section 3.2 can be used to estimate the magnitude of the smaller amount of degradation.

These results have also been checked against other configurations and for other gate lengths. Figure 9 and 12 show our results which follows (8) except that the value of \(\alpha(L)\) is smaller, around \(0.15\%/\mu\text{A}\) of substrate current for \(W=50\mu\text{m}\). However, since the maximum amounts of degradation are smaller, it is difficult to determine \(\alpha(L)\) accurately. A simple estimate of the substrate current degradation under AC use conditions can be made from waveform rise times and duty cycle considerations. The appropriate value of \(|I_{\text{Sub}}|\) to use in (8) under AC use conditions can be calculated from DC values of substrate current versus voltage if the waveforms are known.

Figure 13 shows the calculated degradation or changes in drain current at an ambient temperature of \(25^\circ\text{C}\) for both 1.0 \(\mu\text{m}\) and 0.8 \(\mu\text{m}\) gate length devices using (8) and the parameters in Fig. 12 and values for \(\alpha(L)\) given previously. A good correlation is seen between the empirical results from (8) and the experimental data in Fig. 7 and Fig. 8.
Figure 13. Calculated degradation of drain current for (a) 1.0 \mu m and (b) 0.8 \mu m drawn gate length devices at 25°C ambient temperature.
3 Thermal self-limiting mechanism under AC stress

3.1 Literature review

It has been recognized that the hot-electron degradation is an obstacle to further device miniaturization. As covered in section 2.2, since the hot electrons are injected and trapped, there are all sorts of effects on the device characteristics. Some of the main effects are a threshold voltage shift and the reduction of drain to source current [16], and consequently a reduction of switching time in the circuits. Peter Cuevas [17] supports the idea that the major cause of the hot electron effects is a shift in the temperature due to heat dissipation from the stress, not any real change in the device. Another finding [18] suggests that there is an annealing of some of the traps created by stressing and that the hot-electron effects are not permanent. However, our results are significantly different from the results based on DC stress alone or other models [17,18]. In this part, a simple model of injection and thermal re-emission is shown to be adequate for predicting the hot electron injection induced degradation on sub-micron n-MOS technology under AC stress. Hot carrier stressing has been carried out on LDD n-MOS transistors under various AC use conditions. During AC stressing, the devices are subjected to electron injection when the drain voltage is high and gate voltage moderate [3], and self-heating during stress induces thermal re-emission of trapped electrons in the SiO2 when the gate voltage is low. This limits the maximum amount of drain current degradation. Furthermore, the saturation and change in drain to source current is temperature dependent. Devices were tested under various temperatures for recovery to show the thermal re-emission mechanism. We have investigated the recovery after stress and found that the device do not recover with positive voltage bias and in particular when a very high DC
gate voltage and drain voltage is used to generate a large power dissipation and high temperatures in these small devices. They only recover with low gate voltages and in particular zero gate bias. An empirical model with design equations and design curves is presented in section 2.7 for the prediction of drain current degradation under long term AC stress for n-MOSFET's. The field and temperature dependencies allow for a self-heating and field-assisted re-emission of trapped electrons in the oxide. A trap energy level [19] can be extract from the Price-Sah model and the detrapping conditions are explained in detail.

3.2 Thermal re-emission results

To quantify this thermal re-emission mechanism, devices which have been degraded by hot electron injection were tested at various temperatures for recovery. Fig. 14 shows that the long term drain current degradation under AC stress is self-limiting and saturates to a value of 14% which is then fully recovered after 3500 minutes at 70°C with the conditions of zero volts on the gate and drain. Re-emission, however, occurs only when the gate voltage is zero, or grounded, and will not occur with positive gate voltage. From the Arrhenius plot of the recovery phase in Fig. 15, a 1.5 eV activation energy of the trapped electrons in SiO2 has been extracted. In addition, Fig. 15 shows that the time constant of recovery at room-temperature is around $10^5$ minutes, while at 70°C it is around 600 minutes. Fig. 16 shows the temperature dependence of the change in the drain-to-source current under AC stress over long periods of time for different ambient temperatures with conditions of a pulse of 8.3 volts gate-leads-drain and a frequency of 4 MHz. The degradation is reduced at higher temperatures. At about 70°C, there is no degradation in drain to source current. Under AC stress with a condition of gate leads drain, we have found that there was nearly no degradation in a temperature range of 65°C to 75°C with $V_{gs}=V_{ds}=7.65V$. 
Figure 14. The effect of AC stress and recovery on drain-to-source current for one micron devices.
Figure 15. The Arrhenius plot of the drain to source current recovery mechanism, electron re-emission.
Figure 16. The temperature dependence of the change in drain-to-source current under AC stress.
Under stress, there is a high peak temperature near the drain in these small devices. First order estimates based on the calculations from GaAs FET's, yield a temperature difference of about $150 ^\circ C / mW / \mu m$. The devices have up to $4 \text{ mW}$ power dissipation per micron. Therefore, the combination of stress (electrons injection) and the self-heating (thermal re-emission of electrons) limits the amount of change and causes the self-limiting in drain to source current.

3.3 Tunneling to and from trap model

The energy band diagram is an indispensable aid in visualizing the internal mechanism of the thermal recovery of electrons under different bias conditions. Fig. 17a shows that a trapped electron can thermally recover with zero or negative gate voltage which is characterized by the $1.5 \text{ eV}$ activation energy for the electron to escape from the trap. We have also observed that the optical detrapping energies are greater than $2 \text{ eV}$ for electrons, from which it is concluded that the trap involves some lattice relaxation (Jahn-Teller-Effect), or excited states. The dynamic Jahn-Teller-effect is thought to be the origin of the differences in the observed thermal activation energy and the photoionization or photoemission energy of an electron bound to a trap. It is clear that the trapped electron first makes a transition to the excited state and then tunnels out to the semiconductor. It has also been observed that the devices do not recover with positive gate voltage as shown in Fig. 17b. Therefore, the recovery and self-limiting mechanism can only be observed under AC stress conditions but never under DC stress conditions. Based on the Price-Sah model, Fig. 18 can describe the tunneling to and from the trap upon applying a large negative gate voltage on the device. The recovery in threshold voltage over long periods of time is observed in Fig. 19 with a gate bias of $-13 \text{V}$ and zero volts on the drain, the $230 \text{ mV}$ shift in threshold voltage is fully recovered after 8 days. This
Figure 17. Tunneling model for recovery at different gate bias conditions.
PRICE - SAH TUNNELING EMISSION MODEL

\[ N_{\text{ot}}(t) = \int (1 - e^{-\omega t}) D_0 t(E_T) \, dE_T \]

\[
\omega = \left( \frac{\pi^2}{\hbar^3} \right) \left( \frac{\mu m_z}{m} \right)^{1/2} \left( \frac{E_{ox}}{E_T} \right) W^2 \exp(-2\vartheta) \\
\vartheta = \left( \frac{4\pi}{3} \right) \left( \frac{2m_x}{m} \right)^{1/2} E_T^{3/2} / (\hbar E_{ox})
\]

Figure 18. Tunneling from ground state at large negative gate voltages at room temperature, and Price-Sah emission equations.
Figure 19. The effect of the recovery on threshold voltage under negative gate voltages.
simple measurement characterizes the tunneling of the trapped electron from the ground state.

In order to obtain the energy spectrum of oxide traps, a new electric-field-induced emission technique was employed [20]. This technique involves the following steps: (a) The oxide electron traps in the n-channel device are first created at a room temperature by applying a gate voltage of 2.5 volts and drain voltage of 7.0 volts, (b) for recovery, a negative gate voltage is increased in 0.2 volts steps and maintained constant for 840 minutes at each step, (c) at the end of each step, the threshold voltage and gate voltage at constant drain current are monitored. Fig. 20 shows the threshold voltage shifts versus detrapping oxide electric field by increased the negative gate voltage in 0.2 volts steps, where the oxide thickness is 200 Å. As the oxide electric field steps up, the threshold voltage recovers gradually. It is clear that the large number of electrons are detrapped at an oxide field of approximately 5.8 MV/cm.

Using the Price-Sah tunneling emission model [20] with a tunneling emission rate of:

$$\omega = \frac{\pi^2}{h^3}\left(m_ym_z\right)^{1/2}(E_{ox}/E_t)W^2e^{-2\phi}$$  \hspace{1cm} (1)

where

$$\phi = \frac{4\pi}{3}(2m_x)^{1/2}E_t^{3/2}/q*h*E_{ox}$$  \hspace{1cm} (2)

and

- $E_{ox}$ is the oxide electric field [V/cm].
- $E_t$ is the energy level of the oxide electron trap measured from the oxide conduction band [eV].
- $W^2$ is the square of the tunneling transition matrix element [$V^2cm^3$].
Figure 20. Threshold voltage versus discharge oxide electric field for 1 μm devices with 200 Å oxide thicknesses. Substrate injection was at a gate voltage of 2.5 volts and a drain voltage of 7.0 volts to fill the traps.
The density of oxide traps after a time t at an oxide field $E_{ox}$ is:

$$n_t(t) = \int_{E_v}^{E_c} (1-e^{-\omega t}) D_{ot}(E_t) \, dE_t$$  \hspace{1cm} (3)

Based on the same technique and calculation introduced by T. Nishida [20], the mass $[m_{ox}=0.5m_0]$ reported by Weinberg [21], and the value of $W^2$ [22].

$$\omega = 39.16 \times 10^{-9} m_{ox}(E_{ox}/E_t) \exp[15.55(m_{ox})E_t^{3/2}/E_{ox}]$$  \hspace{1cm} (4)

The density of state ($D_{ot}(E_t)$) of oxide electron trap at energy, $E_t$ is then:

$$D_{ot}(E_t) = \frac{(C_0/q)[\Delta V_{gi-1}-\Delta V_{gi}]/[E_{ti}-E_{ti-1}]}$$  \hspace{1cm} (5)

where $E_{ti}$ in (5) and (4) is computed from $\omega t=1$ at each experimental $E_{ox}$.

Fig. 21 shows the energy spectrum for the oxide traps, or the density of states of electron traps versus energy with oxide electric field as a parameter which is shown in (4) and (5). The maximum oxide electron trap density appears at an energy of 2.45 eV. However, this trap depth from tunneling is larger than the thermal activation energy of 1.5 eV. As mentioned before, the difference is due to the lattice relaxation during thermal activation. The theoretical Mott ratio [23] is about 1.9 in SiO$_2$, while Nishida's Mott ratio is 2.2. Our data shows a Mott ratio of 1.6.
Figure 21. The density of charged oxide electron traps versus energy for 1 µm devices with 200 Å oxide thicknesses. Substrate injection was at a gate voltage of 2.5 volts and a drain voltage of 7.0 volts to fill the traps.
4 Anneling effects of Carbon in NMOSFET's

4.1. Literature review

Channel-hot-electron effects have become a serious fundamental limit on sub-micron MOSFET technology and applications [1]. Several methods have been proposed to improve the SiO₂/Si interface degradation due to hot electron injection [24]-[26]. Recently, it has been reported that, by introducing carbon impurities into the SiO₂/Si interface, the reliability of MOS transistor devices can be significantly improved [7]. This part presents new results based on sequential process steps with and without carbon doping. It is demonstrated that threshold voltage degradation has been reduced, but final anneal has not improved the hot-electron degradation. During the course of previous work on techniques to reduce hot electron trapping and models of degradation under AC use conditions, it became clear that process steps following first and second level metal are introducing large numbers of electron traps in the gate oxides of MOSFET's [27]. It is evident that the annealing process involves a chemical reaction which decreases the dangling bonds at the SiO₂/Si interface. However, carbon doping results in a better lattice match at the surface and stronger bond strengths at the interface [7].

4.2 Experimental

The n-channel MOSFET's (drawn gate length = 1.0 μm; channel width = 50 μm) used in this study have a LDD structure. A carbon doping of 5.6*10¹⁴ cm⁻² has been achieved by ion implantation of carbon. In order to examine the behavior of the device, wafers were removed at various process steps and the
threshold voltage variation of n-channel MOS transistor devices at various points in the process was measured. These process steps included the second level metal, passivation layer and pad etch, and final anneal with or without carbon doping. The DC test is described in section 2.4.

4.3 Results and discussion

Fig. 22 shows the results of the threshold voltage measurements of MOSFET's as a function of process steps prior to hot electron stressing. It is evident that \( V_T \) starts with a positive value around 0.9 V in the carbon doped device following the second level metal, passivation and pad etch. Fig. 23 illustrates that final anneal does not reduce degradation but rather enhances the shifts of threshold voltage. The results in Fig. 22 suggest that carbon doping at SiO2/Si interface may help to terminate interface bonds which are not terminated by the usual annealing. This may be due to the fact that the binding energy between carbon and Si is much higher than that between hydrogen and Si. Fig. 22 also shows what the damage caused by process techniques is an important consideration.

In addition to the process effects on the MOSFET's, threshold voltage stability with time under DC stress is also of great interest. Fig. 23 curve (a) shows a carbon doped device without final anneal and the small shift in \( V_T \) under DC stress. In terms of the resistance to hot electron injection and degradation, final anneal has not improved the characteristics of these devices. Clearly, there are many complex process considerations affecting the subsequent resistance of devices to hot electron degradation. Fig. 23 curve (b) and (c) show the threshold voltage degradation under DC stress of both normal devices and carbon doped devices after second level metal, passivation, and anneal. The shifts of \( V_T \) are relatively large, around 300 mV. However, the sequence of carbon doping and final anneal illustrate only slightly improved \( V_T \) shifts. Curve (d) is for a normal device without carbon after the second level metal, no passivation, and no anneal, not only is the threshold
Figure 22. Threshold voltage variation of n-channel MOSFET devices at various points in the process.
Figure 23. Second level metal and passivation for the cases investigated:

(a) with carbon, no anneal.
(b) with carbon, anneal.
(c) no carbon, anneal.

curve (d) is without carbon, after metal 2, without passivation, and without anneal.
voltage below or much more negative than the nominal value (as shown in Fig. 22) but also even large shifts around 800 mV are observed under DC stress. Final anneal has obviously improved the degradation of this device, but clearly carbon doped devices without final anneal show $V_T$ shifts which are the smallest.

The peak value of the transconductance, $g_m$, as measured in the linear region for a non-carbon doped device is larger than that for the one with carbon doping. In contrast, however, they are only slightly different in the saturation region. Analysis of the I-V data of carbon doped devices indicates that there exists a saturation in the degradation of $g_m$ after a long period of DC stress.

M. Walters and A. Reisman [28] suggest that various oxidation temperatures affect the concentration of neutral electron traps. Consequently, the results of Fig.22 and Fig. 23, may be explained by the fact that the gate oxides may possess neutral electron traps. These traps are difficult to remove by annealing and become filled during device operation, or are formed by the passivation process. Furthermore, Fig. 23 also shows that annealing can not effectively remove the neutral electron trap when the process sequence consists of second level metal, passivation and pad etch.
5 Summary

The aging behavior of lightly doped drain (LDD) structure MOSFET's and some carbon doping devices under various process steps has been studied. The maximum value of drain current degradation after AC stress can be monitored by the maximum average AC substrate current. It is demonstrated that gate leads drain does not enhance AC degradation more than drain leads gate and that they have same changes in drain current. Moreover, it is also concluded that the degradation based on our empirical model gives a good prediction of the drain current degradation phenomena for LDD n-MOSFET's under long term AC use conditions.

The mechanism for the self-limiting or saturation in drain current degradation appears to be the thermal re-emission of the trapped electrons in the gate oxide. High ambient temperatures in AC stress can significantly reduce the degradation. In fact, self-heating during AC stress causes a detrapping of electrons which leads to the self-limiting or saturation in the drain to source current. However, re-emission appears only under AC stress. The difference between the thermal activation energy and the photoemission energy is due to a lattice relaxation of the traps. This simple thermal re-emission model is adequate for predicting the hot-electron injection induced degradation on submicron n-MOSFET's.

Electron traps in MOSFET's gate oxides can be introduced by various fabrication sequences. Carbon doped devices with passivation and pad etch, but without any annealing process show the smallest concentrations of electron traps which is demonstrated by a shifts in threshold voltages of only 45 mV under DC stress. Clearly, a combination of carbon doping, annealing and/or particular passivation process steps can probably be chosen to further improve n-channel MOS transistor reliability.
6 References


