AN ABSTRACT OF THE DISSERTATION OF

Abhijith Arakali for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on January 29, 2010.

Title: Low-Power Techniques for Supply-Noise Mitigation in Phase-Locked Loops.

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Pavan Kumar Hanumolu

Modern day digital systems employ frequency synthesizers to provide a common clock to the system. They are undergoing large scale integration due to which, mitigation of the effect of noise on power supply has become a major design consideration in clocking circuits. Rapid scaling of CMOS technology mandates the design of frequency synthesizers in a low supply voltage environment. Maintaining the supply noise immunity of clocking circuits in low-voltage processes is particularly challenging.

In this thesis, techniques to mitigate the effect of supply-noise in frequency synthesizers are explored. The ring-oscillator based frequency synthesizer is an important part of many clocking circuits. They are used in various digital communication systems and as a building block in high speed signalling systems. They suffer from high sensitivity to power supply noise thereby requiring careful design considerations to improve its supply noise immunity. In light of the above, an attempt has been made to improve the immunity of the ring-oscillator based frequency synthesizer to noise on the supply voltage. The effect of noise on the sup-

plies of other building blocks of a frequency synthesizer, though not as pronounced as that of noise on the ring-oscillator supply, is quite significant. Analysis of effect of power supply noise on various building blocks of the frequency synthesizer are presented. Also, techniques to effectively reduce the effect of power supply noise on the performance of the frequency synthesizer are presented. Measured results from proof-of-concept ICs are presented to illustrate the effectiveness of the proposed techniques.

Clock and data recovery (CDR) circuits which utilize ring-oscillators are also highly sensitive to power supply noise. Measurement of CDR jitter tolerance without the use of expensive equipment is another challenge involved in the design of CDRs. An on-chip jitter tolerance measurement technique is presented wherein, a phase averaging dual loop CDR architecture is used which comprises of a phase-locked loop (PLL) inside the CDR loop. Previously proposed idea of using oversampling in this architecture has proven to considerably reduce power consumption in this CDR architecture. In this thesis, an attempt has been made to further reduce the power consumption. The PLL in this CDR architecture utilizes the proposed supply regulated PLL architecture in order to minimize the bit-error rate (BER) of the CDR due to power supply noise.

Low-Power Techniques for Supply-Noise Mitigation in Phase-Locked Loops

by

Abhijith Arakali

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Abhijith Arakali, Author

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To Amma and Anna.

LOW-POWER TECHNIQUES FOR SUPPLY-NOISE MITIGATION IN PHASE-LOCKED LOOPS

CHAPTER 1. INTRODUCTION

The building blocks in clocking systems, of many, include phase-locked loops (PLLs), delay-locked loops (DLLs) and clock and data recovery circuits (CDRs). In particular, PLLs are commonly used clock generators in all large digital systems. The quality of the clock that is generated is measured by the amount of phase noise present in the clock signal that is generated. Apart from the device noise, noise on power supply is a major source of degradation of the phase of the clock signal that is generated by the PLL. The focus of this work is to mitigate the effect of power supply noise on the output phase of the PLL. In the rest of this Chapter, this issue is further elaborated.

1.1 Noise on VCO Supply

Phase-locked loops are used to multiply a low-frequency reference clock to generate a low-jitter high frequency clock. The main performance goals in the design of PLLs are the following: 1) low-jitter, 2) low-power, 3) small-area, 4) wide operating range, and 5) immunity to extrinsic interference mechanisms such as supply- and substrate-noise coupling. Depending on the target application, one or more of these performance metrics will determine the available design choices of the PLL architecture and its circuit implementation. While charge-pump based

architectures are almost universally used, the circuit realization of such PLLs can be broadly classified into two main categories: a) LC-based voltage controlled oscillator (LC-VCO); and b) ring-based voltage controlled oscillator (ring-VCO). Many of the design trade-offs arise from the choice of the type of oscillator employed in the PLL.

A differential LC-VCO improves the jitter performance of the PLL for three reasons. Firstly, the oscillation frequency of a LC-VCO is determined by passive components and therefore have less noise [2]. Secondly, the differential nature of the LC-VCO makes them relatively immune to power supply noise. Lastly, their low gain reduces the impact of charge-pump and the loop filter resistor noise. The low gain also minimizes PLL sensitivity to the VCO supply noise; however, LC-VCOs occupy large area and have narrow tuning range, thus limiting their usage predominately to narrow frequency-range applications. Ring-VCOs, unlike LC-VCOs, offer wide tuning range and occupy small area, but have inferior noise performance. Due to large VCO gain, ring-VCOs are very sensitive to supply noise. If the noise and supply-sensitivity issues of ring-VCOs are addressed, these VCOs would be ideally suited for applications such as serial links.

A PLL comprises many blocks and hence, supply noise has many paths to affect the output phase of the PLL. Figure 1.1 depicts all the important supply noise coupling paths that cause jitter on the PLL output clock. For simplicity, various clock buffers such as the reference buffer and the VCO buffer are not shown in the figure. In the presence of a tone on the power supply, the cumulative jitter, when plotted as a function of time, will also be sinusoidal as shown in Fig. 1.2. The impact of supply noise in each of the individual building blocks can be quantified

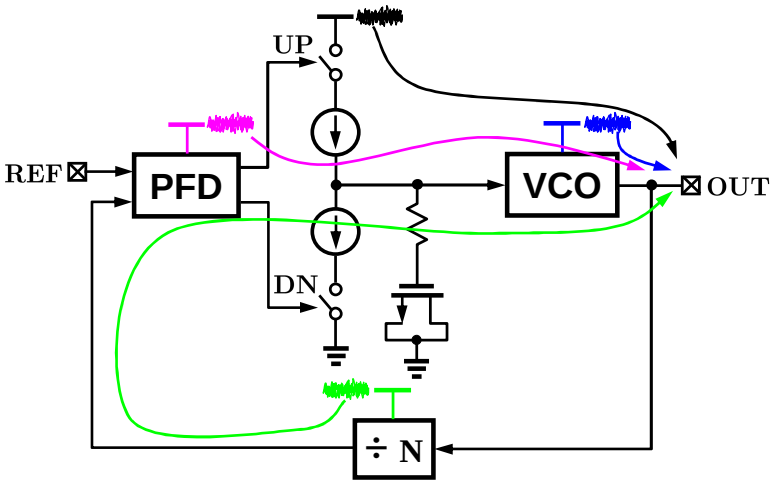

Figure 1.1: Illustration of supply noise coupling paths in a PLL.

by power-supply noise rejection (PSNR) defined as,

$$\text{PSNR[dB]} = 20\text{log10}\left(\frac{\text{T}_\text{j}/\text{T}}{\Delta\text{V}_\text{DD}}\right), \tag{1.1}$$

where, T_j represents the peak jitter of the output clock having a period T, resulting from the sinusoidal perturbation of amplitude ΔV_DD on the supply voltage. To provide a better feel for the relationship between PSNR and jitter, the peak-to-peak jitter of a 2GHz PLL output due to a supply-noise tone of amplitude 100mV for various PSNRs is summarized in Table 1.1. Depending on the application, the requirement on jitter degradation varies from 1% to 0.1% of the output clock period for a supply noise amplitude of 1%. This translates to a PSNR requirement of 0dB down to -20dB. It can be seen from Fig. 1.3, which is obtained through Spectre PAC simulations [3], that the worst-case PSNR for the PLL due to noise on unregulated VCO supply is about 30dB. At 2GHz operating frequency, this is equivalent to about 1500ps of peak-to-peak jitter with a supply noise amplitude of 100mV! Hence careful design considerations are required to avoid the corruption of the output phase of the PLL due to noise on the VCO supply.

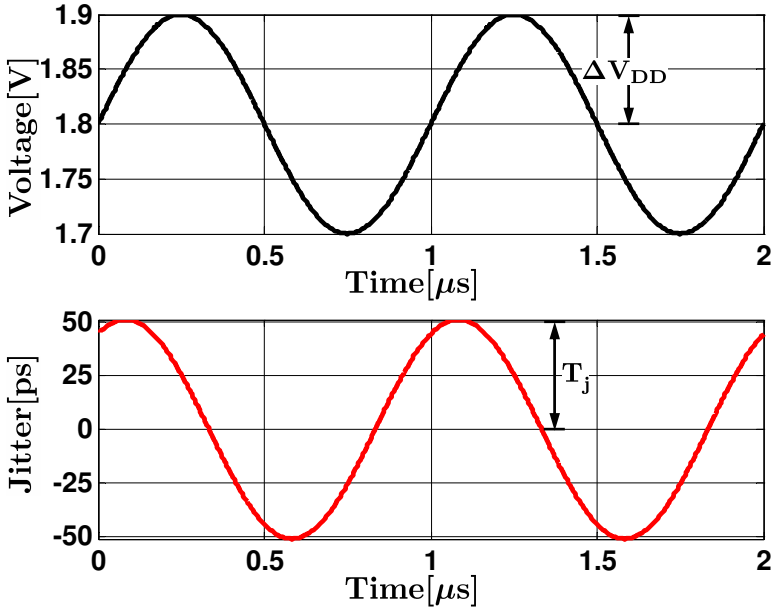

Figure 1.2: Supply noise and jitter waveforms.

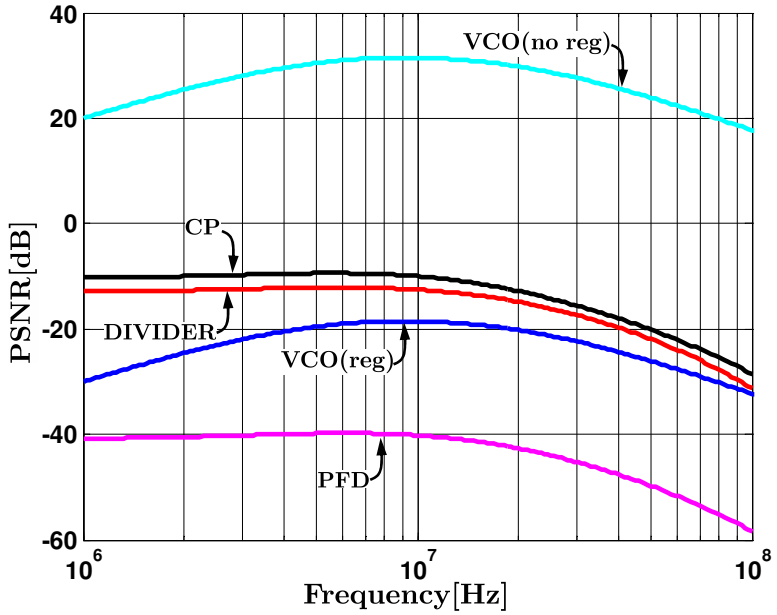

Figure 1.3: Simulated PSNR curves of each of the building blocks of a PLL operating at 2GHz.

Table 1.1: Relation between PSNR and peak-to-peak jitter

PSNR	Peak-to-peak jitter
10dB	316ps
0dB	100ps
-10dB	31.6ps
-20dB	10ps
-30dB	3.16psV
-40dB	1ps

1.2 Supply Noise in Rest of the PLL Building Blocks

While it is true that VCO is most sensitive to supply noise, it is very important to realize that other building blocks of a PLL such as the phase-frequency detector (PFD), charge pump (CP), frequency divider, and clock buffers are also susceptible to supply noise and hence can contribute significant amount of output jitter due to supply noise. To the author's knowledge, there has been little published literature on this aspect of the PLL design. For most of the practical applications, an overall PLL PSNR of -20dB is necessary. Since each building block contributes to the PLL output jitter, a target PSNR of better than -35dB for each of the blocks has to be set. In time domain, this translates to about 1.8ps peak-to-peak jitter degradation with injection of a supply-noise tone of amplitude 100mV.

The PSNR curves shown in Fig. 1.3 reveal many aspects of supply-noise coupling in PLLs that are very useful to implementing noise mitigation techniques. First, as mentioned previously, the VCO supply noise, when its supply is unregu-

lated, is by far the dominant source of output jitter. Consequently, much of the effort has been focussed on suppressing the detrimental effect of supply noise in VCOs [1, 4–7]. Second, when the VCO supply is regulated, charge pump and divider become the dominant sources of output jitter due to supply noise. It can be shown that the reference clock buffer and the VCO buffer exhibit similar sensitivity as the divider and therefore also contribute significantly to output jitter. Note that such supply-noise induced degradation of output jitter is larger at higher PLL output frequencies, thus making it all the more significant to address the issue with frequencies of ring-VCO based clock generators approaching 10GHz [8]. In order to substantiate this, a plot of worst-case PSNR for the entire PLL is plotted in Figure 1.4 as a function of output frequency. It is clear that PSNR of the PLL degrades significantly with increase in the output frequency. Since the modern day ring-VCO based clock generators are required to produce output clock frequencies as high as 10GHz, it becomes mandatory to address the issue of degraded PSNR of the PLL building blocks in such applications.

1.3 A Data Recovery Circuit with High Supply Noise Immunity

Clock and data recovery (CDR) circuits are used in communication systems where digital data needs to be recovered which mainly involves retiming of the received data using a clock signal. The bit-error rate (BER) is one of the measures used to quantify the performance of the CDR which increases in the presence of supply noise. Hence effective techniques to reduce the effect of supply noise on performance of a CDR are required. In many applications, clock is not transmitted with the data which mandates recovery of clock signal from the received data. Of

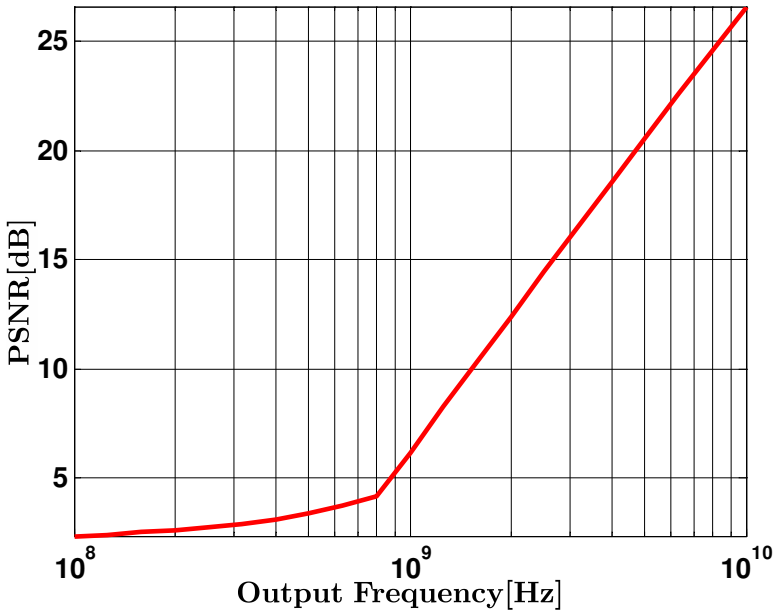

Figure 1.4: Simulated worst-case PSNR as a function of the output frequency.

the many useful CDR architectures, the phase averaging dual loop CDR architecture [9] is very suitable for low voltage applications. The use of a $\Delta\Sigma$ modulator in this CDR [10] helps in relaxing the low bandwidth requirement of the PLL used in the phase averaging CDR which minimizes power consumption in the CDR significantly; however, a practical aspect of the design of a phase averaging CDR is that multiple phases of the VCO are to be routed across the chip. This in turn results in increase of the power consumption in the CDR since the phases have to be routed in such a way that the phase relationship between different phases has to be maintained. Also, the registers used in the digital loop filter of the CDR can consume significant power if operated at high frequencies. Hence there is a scope for improvement in the power efficiency of this CDR architecture.

1.4 Thesis Organization

Since the ring oscillator is the most sensitive block in the ring-VCO based PLL, Chapter 2 is dedicated to analysis of the effect of noise on ring-VCO supply as well as a ring-VCO based PLL architecture that has superior supply-noise immunity with low-jitter, small-area and minimal power consumption is presented [6]. Measured results from the proof-of-concept IC are presented which validates the effectiveness of the proposed techniques.

In view of the observations made in Section 1.2, qualitative as well as quantitative analysis of the impact of supply noise on PLL performance and mitigation techniques to combat supply noise in the PLL building blocks [11] are given in Chapter 3. A PLL architecture that facilitates the use of simple low-dropout regulators to shield the entire PLL from supply noise is presented. Measured results from the prototype PLL are presented which supports the effectiveness of the proposed techniques.

In addition to the detrimental effect of power supply noise of charge pump on the jitter performance of the PLL, it causes intermodulation of the input phase of the PLL with the noise on the charge pump supply. Analysis of this phenomena is presented in Chapter 4.

In Chapter 5, certain techniques to reduce the power consumption in the CDR architecture of [12] are presented. On-chip measurement of the jitter tolerance of a CDR is a desirable feature since that would obviate expensive equipment to measure the jitter tolerance of the CDR. A scheme to measure the jitter tolerance on-chip is also presented in Chapter 5.

CHAPTER 2. POWER-EFFICIENT SUPPLY REGULATION OF VCO SUPPLY IN RING-OSCILLATOR BASED PLLS

Wide tuning range is a desirable feature of a PLL in many applications. Ring-oscillator based PLLs offer this feature at the expense of increased sensitivity to supply noise. In this Chapter, analysis of the effect of noise on the ring-VCO supply is presented. Also, a ring-oscillator based PLL architecture with good supply-noise immunity is presented. The Chapter is organized as follows. A conceptual supply-regulated PLL architecture and the design goals are described in Section 2.1. A detailed analysis of the VCO power supply-noise rejection and the design trade-offs in the regulator design are discussed in Section 2.2. The proposed PLL architecture is presented in Section 2.3 and the regulator design details are given in Section 2.4. The circuit details of important building blocks are described in Section 2.5 and measured results obtained from the prototype integrated circuit are presented in Section 2.6. Finally, the key contributions of this work are summarized in Section 2.7.

2.1 Conventional Supply-Regulated PLL

Power-supply noise is a major performance limiting factor in ring oscillator-based PLLs used for clock generation in large digital integrated circuits [1]. Specifically, supply noise has the most detrimental effect on the jitter performance of voltage-controlled oscillator (VCO). Process scaling dictates increasing VCO

gain, further exacerbating the detrimental effect of supply noise on the oscillator performance. Considering supply noise, various supply-regulation techniques primarily focussing on suppressing the supply noise in the VCO have been employed [1, 4, 5, 13]. Figure 2.1 shows a general representation of a supply-regulated PLL, wherein the control voltage for the VCO is applied to its supply through a low drop-out regulator. Ideally, the regulator behaves as a unity gain buffer

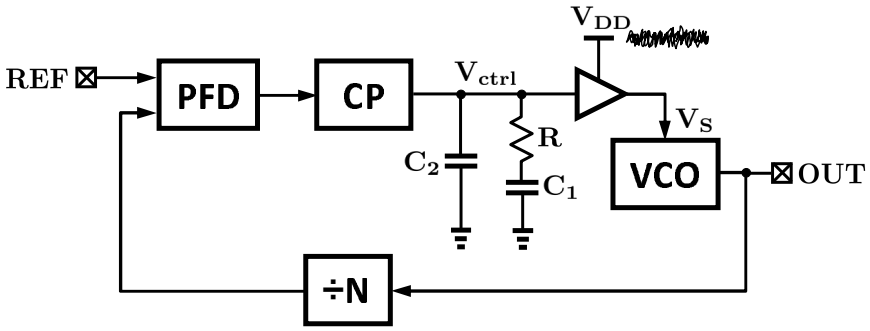

Figure 2.1: Conventional supply-regulated PLL.

completely shielding its output from the supply noise. In practice, the regulator fails to completely isolate supply noise from the output due to various circuit non-idealities such as the finite transistor output impedance and so on. Furthermore, the regulator also limits the maximum control voltage range of the VCO due to intrinsic voltage drop, referred to as drop-out voltage, across its output pass transistor. A common practice is to minimize the drop-out voltage to maximize the available supply and hence improve the frequency range of the VCO.

Conventional supply regulation techniques used in [1, 4, 5, 13], all suffer from one fundamental limitation − since the regulator is inside the PLL loop, the poles in the regulator degrade the stability of the loop dictating the use of a much wider regulator bandwidth (compared to the PLL bandwidth), hence leading to excessive power consumption [5]. Additionally, regulators used in [1, 4] also suffer from poor

supply-noise rejection performance.

2.2 Design Considerations for Supply-Regulation in PLLs

The regulator which is used to regulate the VCO supply must be designed in conjunction with the supply-noise characteristic of the PLL. Before examining the design procedure for a regulator in a supply-regulated PLL, it is necessary to understand the sensitivity of the PLL output phase, Φ_{out}, to noise on the VCO control node, V_S (refer to Fig. 2.1). The small-signal block diagram of the PLL along with supply noise as an input (denoted as $V_{DD}(s)$) is shown in Fig. 2.2. We have denoted the transfer function of the regulator from its supply V_{DD} to its output V_S (as shown in Fig. 2.2) by $H_{V_{DD}}(s)$. Since the regulator is used as a voltage buffer between the loop filter and the VCO control node, we assume that the gain of the buffer is unity. We also assume that its bandwidth is much wider than the PLL bandwidth and hence, does not impact the PLL loop dynamics.

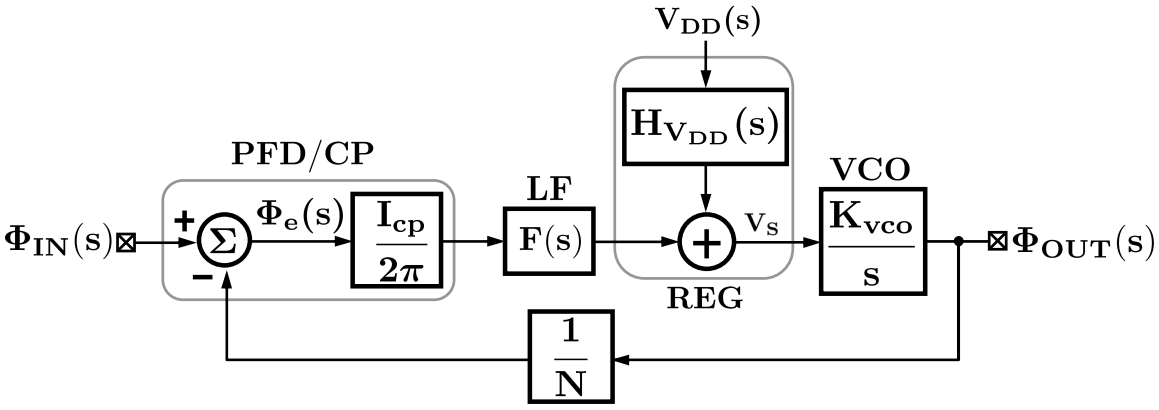

Figure 2.2: Conventional supply-regulated PLL's small-signal model.

The VCO sensitivity to supply noise can be evaluated by analyzing the transfer function between the VCO control voltage, V_S, and the output phase, Φ_{out}, given

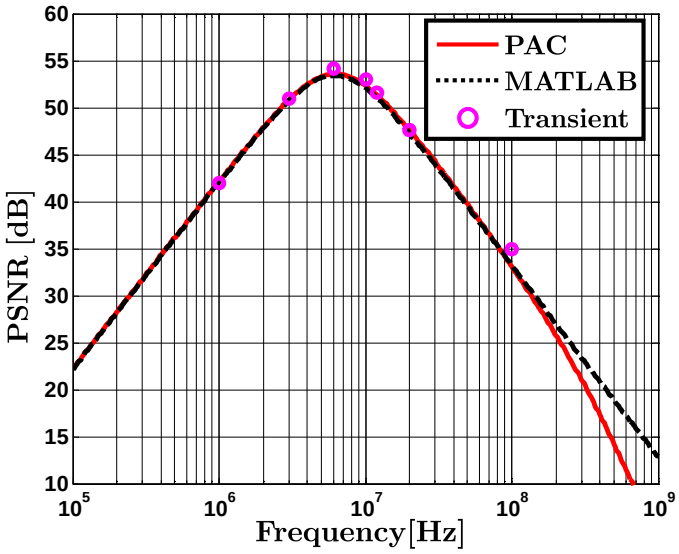

Figure 2.3: PSNR of a PLL plotted using PAC simulation, transient simulation and small-signal analysis.

as,

$$\frac{\Phi_{out}(s)}{v_S(s)} = \frac{K_{VCO}/s}{1 + LG(s)} \tag{2.1}$$

where,

$$LG(s) = \frac{I_{cp}K_{VCO}}{2\pi N(C_1 + C_2)} \frac{1 + RC_1 s}{s^2(1 + s\frac{RC_1C_2}{(C_1+C_2)})}. \tag{2.2}$$

The small-signal model of the PLL can be used to derive the noise transfer functions as long as the PLL bandwidth is lower than the reference frequency by a factor of about twenty [12]. To validate the small-signal operation approximation, the PSNR profile of the PLL is plotted in Fig. 2.3 using three methods: 1) with a circuit-level transient simulation of the PLL, by applying a sinusoidal supply-noise amplitude of 200mV peak-peak, and evaluating the PSNR (as described previously) from the resulting jitter; 2) by using the periodic-AC analysis in SPECTRE [3]; and 3) by using the small-signal analysis. The PLL was designed for a bandwidth of 20MHz

using a reference frequency of 500MHz with a divide ratio of 4. Figure 2.3 shows the profiles obtained by the three methods, clearly indicating that the small-signal analysis provides a good estimate of the PSNR.

2.2.1 Regulator Design Methodology

The issues involved in the design of linear-regulators for supply-regulated PLLs have been studied in [13] but we have included similar analysis in this Chapter for the sake of notational consistency and completeness. A commonly used low-dropout regulator schematic is shown in Fig. 2.4(a). The regulator consists of an error amplifier, compensation capacitor, C_c, pass transistor, M_P, and the bypass capacitor, C_d. The open-loop poles associated with the amplifier and the output node are denoted as ω_a and ω_o, respectively. The regulator provides oscillation-frequency dependent current through the pass transistor while maintaining the virtual supply of the VCO, V_S, at the loop control voltage, V_{ctrl}. Alternatively, it is also possible to drive the VCO directly with the error amplifier configured as a voltage follower, as illustrated in Fig. 2.4(b) [5]. In this case, the low-output impedance provides superior supply-noise rejection, but has been discarded in this design for two reasons: 1) in order for the amplifier to operate in the *linear* region, the bias current in its output stage needs to be 2-to-5 times larger than the VCO current resulting in large power dissipation; and 2) the unity-gain configuration forces useful output voltage range to be limited by the output swing of the error amplifier, reducing the VCO operating range. For these reasons, the focus of our work is on improving the performance of the regulator shown in Fig. 2.4(a). We seek to improve the supply-noise rejection of the regulator while minimizing both power consumption and operating range penalty. To this end, we shall discuss the

inherent limitations of conventional regulators, thus providing the framework for the proposed solutions in Sections 2.3 and 2.4.

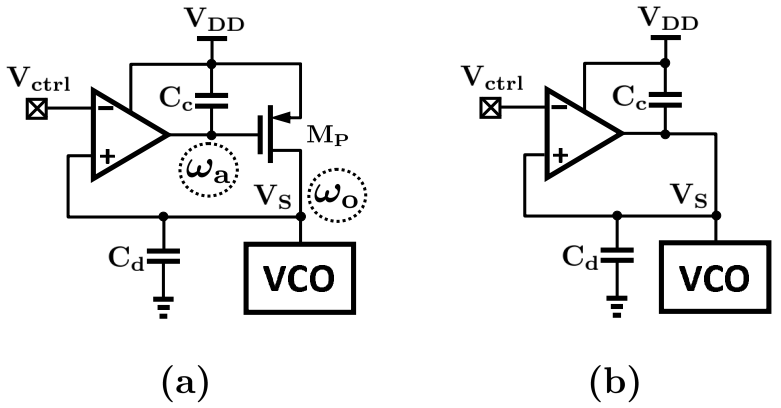

Figure 2.4: Conventional regulators used in a supply-regulated PLL: (a) using a pass transistor. (b) without using the pass transistor.

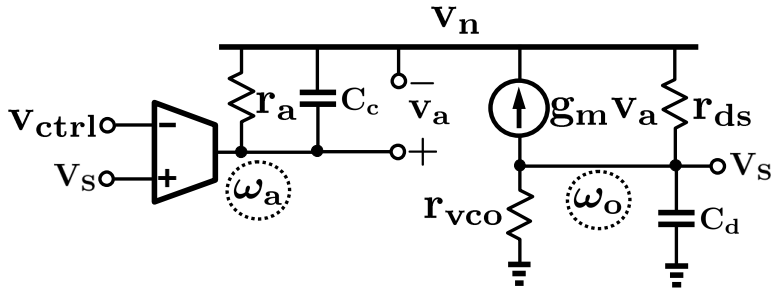

Figure 2.5: Small-signal model for the conventional regulator.

Figure 2.5 shows the small-signal model of the conventional regulator. This regulator is a two pole system and, hence, needs to be frequency compensated to avoid poor transient response. A straightforward approach for improving the transient response is to use Miller compensation; however, this technique, when applied to two-stage regulators, results in poor high-frequency power-supply-rejection-ratio (PSRR[1]) performance [14]. Alternatively, the two-stage regulator can have a ca-

[1]In this work, we use the terms PSRR and PSNR to represent the supply-noise rejection

pacitor C_c at the output of the amplifier, which is coupled to the supply as shown in Fig. 2.4(a). Either of the two poles can be made dominant and the regulator loop dynamics will be the same in each case, if designed to have the same phase margin; however, each choice leads to a vastly different PSRR performance in the regulator- the subject of discussion for the remainder of this section.

We first consider the case where the amplifier pole ω_a (i.e $\omega_a \ll \omega_o$) is made dominant. The PSRR performance of the stand-alone regulator is characterized by the transfer function from the supply to the regulator output, $\frac{v_S(s)}{v_n(s)}$, and is given by

$$\frac{v_S(s)}{v_n(s)} = \frac{S_{V_{DD}}\,(1 + s/\omega_a)}{(1 + s/\omega_a)\,(1 + s/\omega_o) + A_a A_o} \tag{2.3}$$

which can be rearranged as,

$$\frac{v_S(s)}{v_n(s)} = \frac{S_{V_{DD}}}{\left(1 + \dfrac{s}{\omega_o}\right)(1 + LG(s))} \tag{2.4}$$

where,

$$S_{V_{DD}} = \frac{r_{vco}}{r_{vco} + r_{ds}} \tag{2.5}$$

$$\omega_a = \frac{1}{r_a C_c} \tag{2.6}$$

$$\omega_o = \frac{1}{(r_{ds} \parallel r_{vco})\, C_d} \tag{2.7}$$

$$A_a = g_a r_a \tag{2.8}$$

$$A_o = g_m\,(r_{ds} \parallel r_{vco})\,. \tag{2.9}$$

The terms $S_{V_{DD}}$, ω_a, ω_o, A_a, and A_o represent the PSRR in an open-loop regulator at DC, the amplifier output pole, the pole at the regulator output, the

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performance of the regulator and the whole PLL, respectively.

amplifier DC gain, and the output stage gain, respectively. The corresponding PSRR plot is shown in Fig. 2.6[2]. Intuitively, in the absence of the regulator feed-

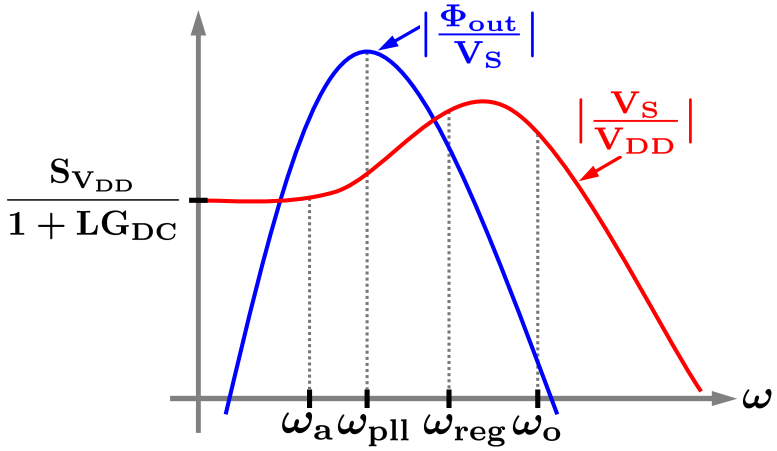

Figure 2.6: Conventional pass transistor-based regulator supply-noise rejection profile when ω_a is made dominant (LG_{DC}: regulator DC loop gain).

back, low-frequency supply-noise sensitivity is determined by the resistive division of the pass transistor, r_{ds}, and the VCO's supply impedance, r_{vco}, and is equal to $\frac{r_{vco}}{r_{vco}+r_{ds}}$. In the presence of the regulator feedback, for frequencies below the regulator dominant pole, ω_a, the open loop sensitivity is reduced by the DC loop gain, LG_{DC}. Consequently, excellent noise immunity at DC can be achieved by employing an error amplifier with a large DC gain. For frequencies above the dominant pole, ω_a, the loop gain rolls-off with a -20dB/decade slope, thus degrading the supply-noise immunity. At the regulator bandwidth, ω_{reg}, the loop gain equals unity and the closed-loop sensitivity equals open-loop sensitivity. Beyond the regulator bandwidth, the loop gain falls below unity and the supply-noise sensitivity peaks to its worst value, equal to the open loop DC sensitivity. Beyond the reg-

[2]The figure also includes the closed response of the PLL to supply-noise on the VCO, which will be alluded to in Section III.B .

ulator output pole frequency, ω_o, the bypass capacitor, C_d, suppresses the supply noise and the supply-noise sensitivity improves at 20dB/decade rate.

Let us now consider the second scenario where the output pole ω_o is made dominant, and the corresponding PSRR response is shown in Fig. 2.7. Here,

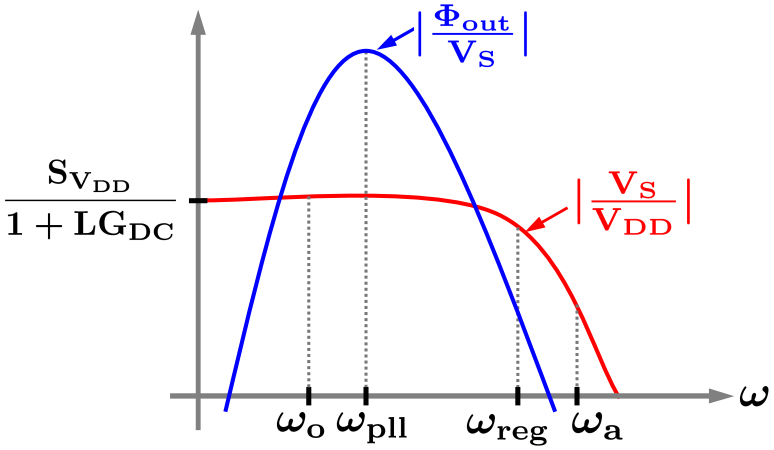

Figure 2.7: Conventional pass transistor-based regulator supply-noise rejection profile when ω_o is made dominant (LG_{DC}: regulator DC loop gain).

the loop gain reduces beyond ω_o at -20dB per decade, while the capacitor C_d, provides improved suppression at the rate of 20dB/decade, thus enabling a flat PSRR response beyond ω_o. Beyond the regulator's unity-gain bandwidth (UGB), the magnitude of the loop gain reduces to a value less than unity and the supply-noise sensitivity is same as the open-loop supply-noise sensitivity. The open-loop PSRR keeps improving at -20dB per decade beyond the UGB of the regulator. Hence, the overall PSRR improves at that rate beyond the regulator UGB. While good PSRR is achieved over the entire frequency range by making the output pole ω_o dominant, this approach entails prohibitively large area and power penalty. Due to this reason, the output pole is seldom made dominant even though excellent supply rejection is obtained. Therefore, for the rest of this section, we consider the case where the amplifier output pole ω_a is dominant.

2.2.2 PLL's Supply-Noise Rejection Properties

Having presented the supply-noise transfer function analysis of the stand-alone regulator, we will now discuss the impact of supply noise on the PLL output jitter with the regulator placed in the PLL feedback loop (Fig. 2). Considering the negative feedback action of the PLL loop, the transfer function from the VCO's supply to its output phase has a bandpass transfer characteristic, with its center frequency approximately at the PLL bandwidth, ω_{pll}. The product of the two transfer functions, $|\frac{V_S}{V_{DD}}|$ and $|\frac{\Phi_{out}}{V_S}|$, shown in Fig. 2.6, will effectively determine the complete PLL sensitivity to VCO supply noise. In other words, regulator supply-noise transfer function, $|\frac{V_S}{V_{DD}}|$, determines the amount of noise on V_{DD} that appears on the VCO virtual supply node V_S, while the VCO supply-noise transfer function, $|\frac{\Phi_{out}}{V_S}|$, quantifies the amount of jitter on the VCO output due to noise on its supply voltage, V_S. It is evident, from Fig. 2.6, that the worst-case supply-noise sensitivity of the PLL occurs in the vicinity of the PLL bandwidth ω_{pll}. This is because the regulator bandwidth needs to be at least 2-3 times larger than the PLL bandwidth to ensure overall PLL stability and hence the product of the regulator and VCO supply-noise transfer functions always peaks near the PLL bandwidth (refer to Fig. 2.6). Ideally, a regulator with large DC gain and large bandwidth, as compared to the PLL bandwidth ($\omega_{\text{reg}} \gg \omega_{\text{pll}}$), will guarantee excellent supply-noise immunity over the full spectrum of frequencies. To illustrate this fact, the simulated PLL supply-noise sensitivity for different regulator bandwidths is shown in Fig. 2.8. The regulator is designed for a phase margin of 70^{o} with the amplifier output pole, ω_{a}, being made dominant. These simulation results indicate that even for a modest -8dB of worst-case PSNR, a regulator bandwidth equal to fifty times the PLL bandwidth is needed. Such a large regulator bandwidth will incur signif-

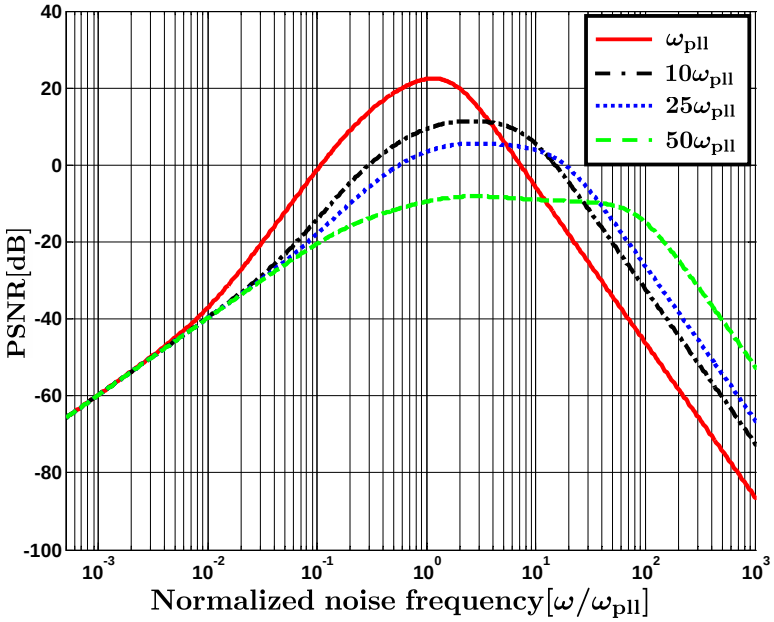

Figure 2.8: Overall PSNR of the regulator plotted for various regulator bandwidths.

icant power penalty. Alternatively, it is possible to reduce the PLL bandwidth to ease the bandwidth requirement of the regulator to achieve the same supply-noise sensitivity; however, such a design choice will result in an inadequate suppression of the VCO phase noise, thereby increasing the PLL output jitter.

In summary, conventional regulation schemes suffer from the power-supply noise rejection performance versus power dissipation trade-offs. This is due to the conflicting PLL loop bandwidth requirements imposed by the VCO and the regulator. The proposed solutions in Section IV and V completely decouple the PLL bandwidth from regulator bandwidth, thereby alleviating the above trade-offs.

2.3 Proposed Supply-Regulated PLL Architecture

Conventional supply-regulation techniques must contend with the regulator in the main loop of the PLL resulting in unfavorable trade-offs between supply-rejection and power dissipation. This trade-off can be decoupled if the supply regulator is not included in the main loop of the PLL. Following this line of thought, Fig. 2.9 shows the proposed split-tuned supply-regulated PLL. This architecture enables wide operating range with low VCO gain, a highly desirable feature in the design of low-noise PLLs. More importantly, this PLL allows the regulator to be placed in the low-bandwidth coarse loop.

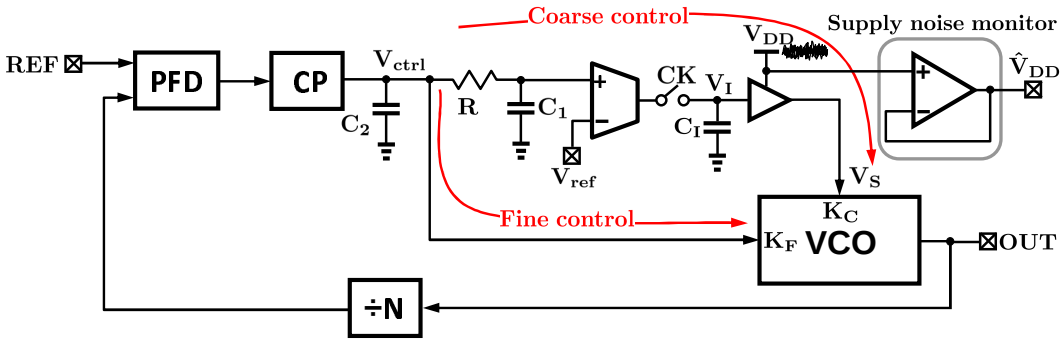

Figure 2.9: Proposed supply-regulated PLL.

The PLL consists of a phase frequency detector (PFD), a charge-pump (CP), a low-pass loop filter realized using passive components R, C_1, and C_2, a switched $G_M - C_I$ filter, a supply regulator, a split-tuned VCO controlled by a separate high-gain, V_S, and low-gain, V_{ctrl}, inputs, and a frequency divider. Supply-noise monitor shown in Fig. 2.9, as discussed later in Section 2.6, is used to directly measure noise on the on-chip supply node, V_{DD}.

The PFD compares the phase and frequency of the reference clock input

(REF) to the output of the frequency divider and produces a signal proportional to the phase error. The charge-pump converts this error signal to an equivalent charge and transfers it to the loop filter. The loop filter output voltage, V_{ctrl}, serves as the fine control voltage to the VCO. In addition to the conventional fine control path, a coarse control loop is also utilized in this PLL [10, 15, 16]. In the coarse control path, a switched $G_M - C_I$ filter integrates the voltage across the loop filter capacitor, C_1, and generates an output voltage V_I. A 0.1% duty cycle clock, CK, is used to effectively increase the integrator time constant. A regulator buffers this voltage and generates the coarse control voltage, V_S, to the VCO. The coarse and fine control voltages tune the oscillator frequency by varying the VCO's supply voltage and the delay cell's load capacitance, respectively. In locked state, the coarse control loop also biases the charge-pump to a known voltage, V_{REF}, irrespective of the PLL output frequency. This reduces the dynamic current mismatch in the charge-pump and results in superior deterministic jitter performance. Having briefly presented the operation principle of the PLL, we shall now discuss the supply regulation properties of the PLL.

The coarse control voltage generated by the switched $G_M - C_I$ integrator is buffered through a low-dropout regulator to produce the supply voltage of the VCO much like the conventional supply-regulated PLL shown in Fig. 2.1; however, placement of the regulator in the low-bandwidth coarse control path eliminates the trade-off between regulator bandwidth (thereby lowering the power consumption in the regulator) and supply-noise rejection present in conventional supply-regulated PLLs, a fundamental advantage over existing solutions [1, 4, 5, 13]. In other words, since the loop dynamics are primarily dictated by the wide-bandwidth fine control path, the bandwidth of the regulator in the coarse control is decoupled from the PLL bandwidth. By designing the regulator bandwidth to be much lower than

the PLL bandwidth, a vastly superior supply-noise rejection performance can be achieved. To further illustrate this point, the simulated PSNR curves of the conventional supply-regulated PLL in [1] and the proposed split-tuned supply-regulated PLL are compared in Fig. 2.10. In this comparison, the traditional regulator circuit shown in Fig. 2.4(a), is used in both architectures with similar overall power dissipation. The proposed architecture shows a 12dB improvement in supply-noise rejection performance over conventional solutions, confirming that the proposed architecture is inherently well suited for supply-regulated PLLs. Even though conventional regulators shown in Fig. 2.4 can be readily used in the proposed PLL, it is possible to further improve the supply-noise rejection by designing the regulator that specifically exploits the benefits offered by the proposed split-tuned PLL architecture. In the next section, we shall first discuss various trade-offs in regulator design and will then present a regulator architecture that uses a replica branch and a very low-frequency dominant pole in the supply-noise transfer function to further improve the PSRR by nearly 25dB over the PSRR of a conventional regulator.

2.4 Regulator Design

The design of the regulator requires considerations that specifically exploit the benefits offered by the proposed PLL architecture. It is important to note that even though the regulator is placed in the coarse control path, which has minimal impact on the dynamics of the PLL, its supply-noise rejection performance depends on the loop dynamics. Consequently, the regulator should be designed in conjunction with the PLL loop response to supply noise. We will first describe the limitations to further improving the PLL PSNR using a conventional regulator in the proposed split-tuned PLL. We will then present a regulator architecture that

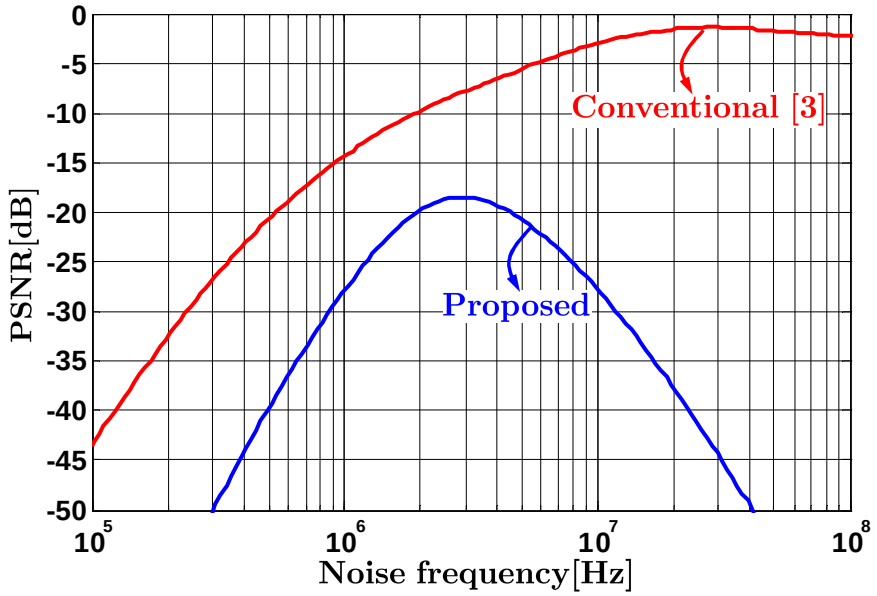

Figure 2.10: Simulated PLL's power-supply noise rejection (PSNR) performance for conventional [1] and proposed PLL.

circumvents these limitations.

Consider the conventional regulator schematic shown in Fig. 2.4(a) and the power supply noise sensitivity curves of the regulator and the VCO depicted in Fig. 2.6. The PLL supply-noise rejection performance can be improved by misaligning the peaks of the two transfer curves so as to obtain a lower overall peak of the product of the two curves. This can be achieved by having a regulator bandwidth that is either much higher or much lower compared to the PLL bandwidth. Note that in both cases a large DC loop gain is needed to achieve good supply-noise rejection. Misaligning the peaks by having a very wide regulator bandwidth, as done in conventional supply-regulated PLLs, increases the power dissipation of the error amplifier. On the other hand, reducing the regulator bandwidth, a design choice allowed only in the proposed architecture, incurs a severe area penalty due to large capacitors (of the order of nF), C_c and C_d.

It should be mentioned here that, alternatively, the regulator can also be frequency compensated by making the regulator output pole dominant ($\omega_a \gg \omega_o$) as opposed to the case described above, where ω_a was the dominant pole. This design choice leads to reduced peaking in the supply noise transfer curve, thereby resulting in a superior PLL supply noise immunity. However, this compensation scheme leads to: 1) increased power dissipation due to large ω_a, and 2) large chip area required to implement the bypass capacitor, C_d. To quantify these drawbacks, the total capacitance needed is plotted as a function of the worst case PLL PSNR in Fig. 2.11. This plot reveals that for a desired PSNR of -24dB, the regulator requires 6.5nF total capacitance. Compared to this, a conventional regulator with ω_a as the dominant pole requires 300nF of total capacitance (see Fig. 2.12). It is also possible to use a simple current source to control the VCO frequency but a large bypass capacitor (of the order of nF) will be required to obtain a reasonably good worst-case PSNR. For most applications, the requirement for large capacitance precludes the use of such architectures. Another class of regulators commonly referred to as replica-based regulators are also used to improve the supply-noise rejection [13, 17]. In particular, [13] uses a replica branch to introduce a fast path in parallel to the slow VCO path. This results in a zero in the open-loop transfer function of the regulator which makes it possible to have the output pole very close to the amplifier pole, thereby reducing the peaking in the supply-noise transfer function of the regulator. We will now present a low-power regulator architecture that obviates a large capacitor while achieving excellent supply-noise rejection performance by completely eliminating the peaking in the supply-noise transfer function.

As discussed in Section 2.3, there is no restriction on the bandwidth of the regulator if it is used in the coarse path of the PLL. Exploiting this new-found

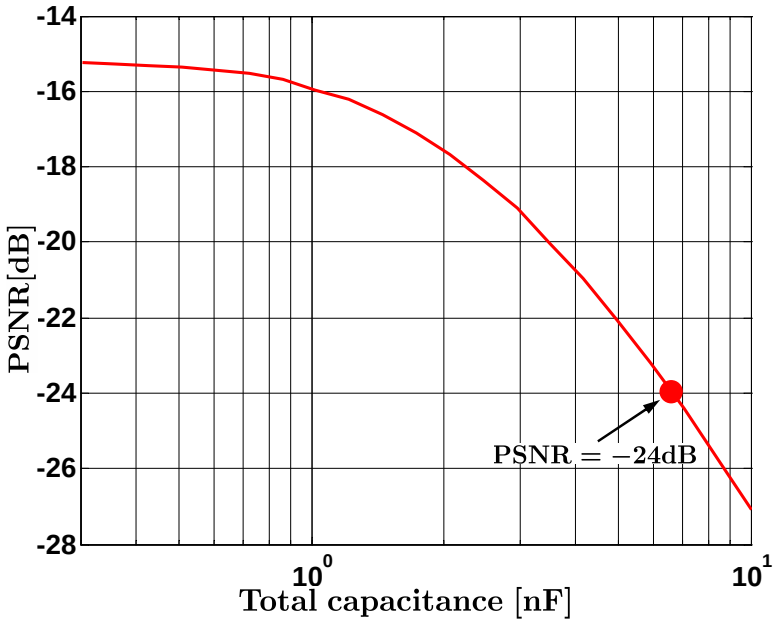

Figure 2.11: Worst case PLL PSNR using a conventional regulator for various values of total regulator capacitance when output pole ω_o is dominant.

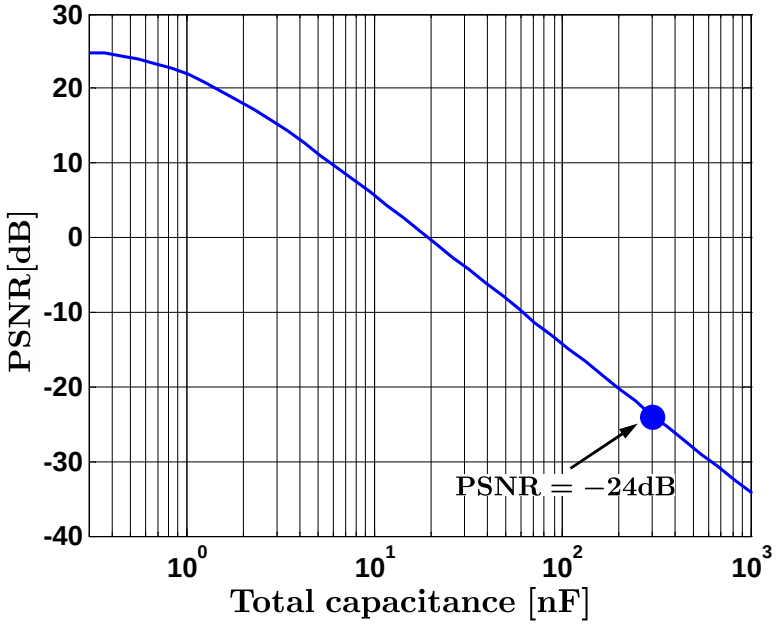

Figure 2.12: Worst case PLL PSNR of the conventional regulator for various values of total regulator capacitance when amplifier pole ω_a is dominant.

design freedom, the peaking present in the PSRR curve of a conventional regulator can be removed if an additional low-frequency pole, ω_d where $\omega_d < \omega_a$, is introduced in the PSRR curve. Following this line of thought, the regulator architecture employed in this design, shown in Fig. 2.13, introduces a low-frequency pole, ω_d, using a replica branch. A similar regulator topology was first introduced in [17] and

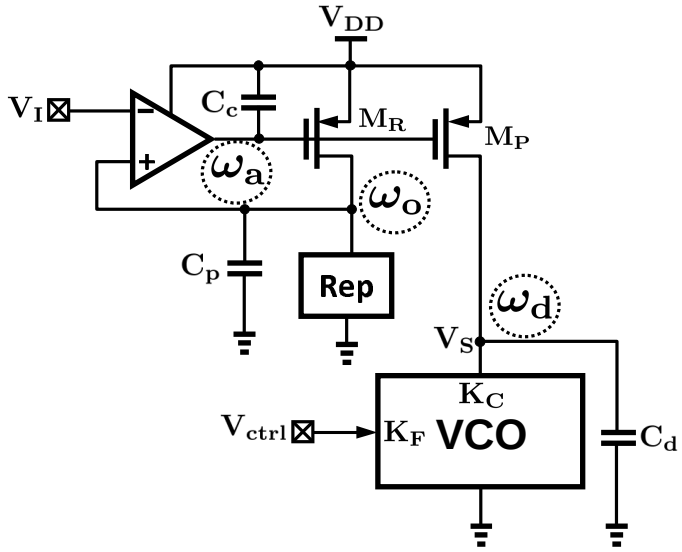

Figure 2.13: Regulator architecture employed in the proposed split-tuned PLL.

later adopted in [18]; however the conventional PLL architecture employed in [13] prohibits the use of such regulators. In this work, we optimize this regulator for our proposed PLL architecture. The replica branch consisting of a replica pass transistor (M_R) and a VCO replica (Rep) is used to mimic the supply noise on the main branch (M_P + VCO). The replica load used in this design is similar to the one used in [13]. With the feedback eliminated in the main branch, a reasonably small (of the order of tens of pF as against few nF) bypass capacitor C_d can be used to introduce a low frequency pole at ω_d in the supply noise transfer function. By making ω_d the dominant pole ($\omega_d < \omega_a$), the peaking in the supply noise transfer curve can be completely eliminated. Having presented the regulator architecture

and its operation principle, we will now derive the supply noise transfer curve of the regulator using its small-signal model and discuss the regulator's supply noise rejection properties in detail.

The small signal model of the regulator is shown in Fig. 2.14. Using the small-signal model and assuming that the transistors M_R and M_P are perfectly matched, the supply noise transfer function can be derived to be

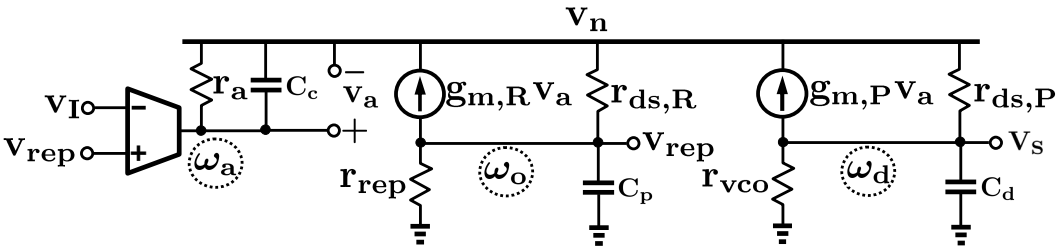

Figure 2.14: Small-signal model of the regulator.

$$\frac{v_s(s)}{v_n(s)} = \frac{S_{V_{DD}}\,(1+s/\omega_a)\,(1+s/\omega_o)}{((1+s/\omega_a)\,(1+s/\omega_o)+A_aA_o)\,(1+s/\omega_d)} \tag{2.10}$$

$$= \frac{S_{V_{DD}}}{\left(1+\dfrac{s}{\omega_d}\right)(1+LG(s))} \tag{2.11}$$

where,

$$S_{V_{DD}} = \frac{r_{vco}}{r_{vco}+r_{ds,P}} \tag{2.12}$$

$$\omega_a = \frac{1}{r_aC_c} \tag{2.13}$$

$$\omega_o = \frac{1}{(r_{ds,R} \parallel r_{rep})\,C_p} \tag{2.14}$$

$$\omega_d = \frac{1}{(r_{ds,P} \parallel r_{vco})\,C_d} \tag{2.15}$$

$$A_a = g_ar_a \tag{2.16}$$

$$A_o = g_{m,R}\,(r_{ds,R} \parallel r_{rep})\,. \tag{2.17}$$

As expected, Eq. 2.11 shows that the regulator supply noise transfer function has an additional pole ω_{d}. Comparing the supply-noise transfer functions of the conventional regulator (Eq. 2.3) and the replica-based regulator (Eq. 2.11), an additional degree of design freedom to avoid degradation of supply noise rejection beyond the loop-gain dominant pole (ω_{a}) can be observed. Recall that in the conventional regulator ω_{o} must be made much larger than ω_{a} to ensure stability.

A typical PSRR plot of the regulator is shown in Fig. 2.15 which assumes the pole frequency ω_o is much higher than the UGB of the regulator. Intuitively, the

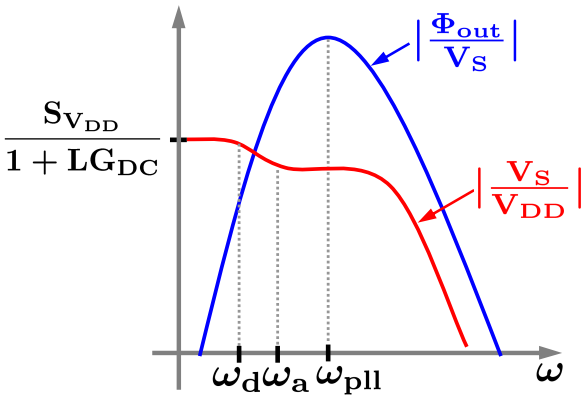

Figure 2.15: The regulator's supply-noise rejection profile.

regulator's loop gain provides low-frequency rejection, while the bypass capacitor, $\mathrm{C_d}$, further suppresses noise at frequencies beyond ω_{d} leading to a 20dB/decade roll-off of the sensitivity profile. The loop gain degrades beyond ω_{a}, resulting in a flattened power-supply rejection response. In other words, the pole of the amplifier contributes a zero to the overall transfer function and this degrades the suppression around ω_{a}. Beyond the regulator bandwidth, the supply-noise rejection curve starts to roll-off again. Note that the DC rejection is inversely proportional to the DC replica-loop gain and any variation in the amplifier gain, transconductance of $\mathrm{M_R}$ or the replica load resistance results in a change of DC rejection of the regulator.

Figure 2.16 compares the simulated performance of the regulator employed in our PLL with the conventional [1] and replica-based regulators [13], indicating that our regulator provides greatly improved supply-noise rejection performance. The power consumption in each of these regulators was maintained the same for fair comparison. The output pole was made dominant for the conventional regulator as we are now considering the possible regulator architectures for the proposed PLL where the bandwidth of the regulator is not required to be higher than the PLL bandwidth. This way, the conventional regulator design would be optimized with respect to the supply-noise rejection performance enabling a fair comparison between the PSRR of our regulator and that of the conventional regulator architectures; however, recall that making output pole of the conventional regulator dominant, as has been shown earlier, requires very large capacitance of 760pF while the other two regulators employ only 200pF bypass capacitance.

As the PSRR of the proposed regulator is a strong function of the ratio of ω_d to ω_a, better rejection can be obtained by increasing the value of the bypass capacitor C_d. This point is quantified in Fig. 2.17 where-in worst-case PSNR of the PLL is plotted versus the regulator bypass capacitor C_d. The worst case PSNR is constant for values of C_d less than 10.5pF because ω_d is greater than ω_{reg} for these values of C_d. On the other hand, for larger values of C_d, ω_d is less than ω_{reg} and the PSNR improves proportionally with C_d. Note that to achieve a PSNR of -24dB, a total bypass capacitance of only 200pF is required as opposed to using a much larger capacitance in a conventional regulator (6.5nF for the case when ω_o is dominant or 300nF when ω_a is dominant).

In the regulator PSRR discussion thus far, we have assumed that the replica transistor M_R and the main pass transistor, M_P are perfectly matched; however, in practice, random variation in both transistor dimensions and process parameters

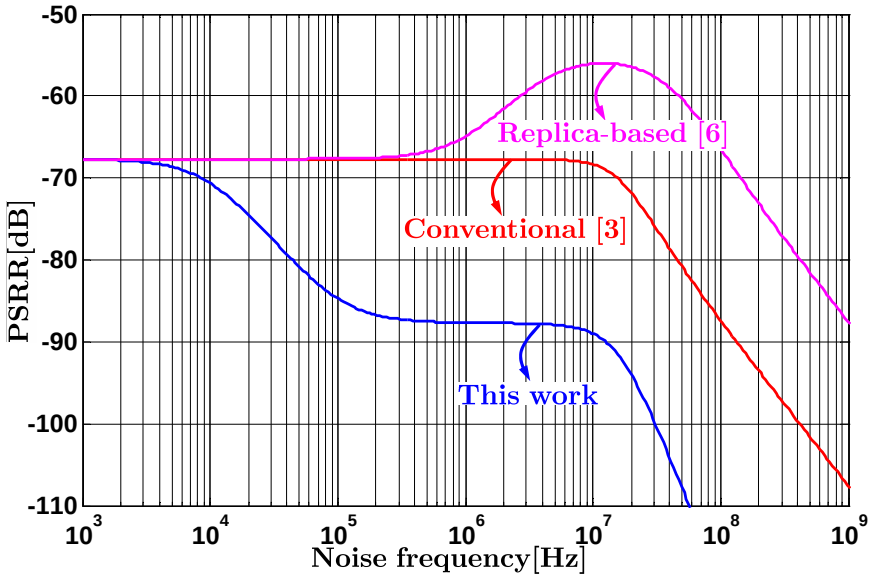

Figure 2.16: Simulated PSRR performance of different regulators. A 760pF capacitor is used in the conventional regulator while others use 200pF capacitors and all regulators consume same power.

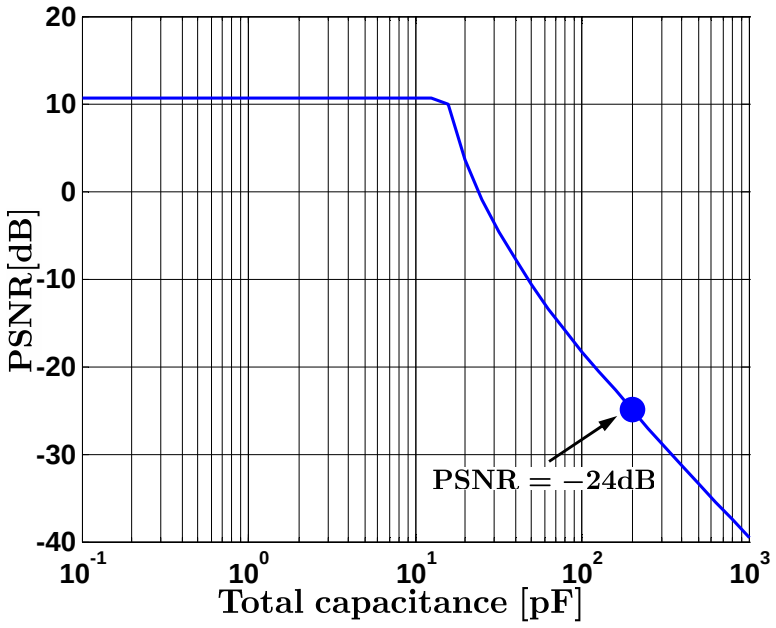

Figure 2.17: Worst case PSNR of our regulator for various values of the total capacitance ($C_{tot} = C_p + C_d + C_c$).

introduce mismatch between the two transistors. Next, we will consider the effect of such mismatch on the PSRR of the regulator. The supply noise has two paths to appear at the output node V_S: 1) through the gate to source voltage of M_P and 2) through the resistive division between VCO supply impedance, r_{vco}, and the pass transistor output impedance, $r_{ds,P}$ (Figs. 2.13 and 2.14). In the presence of mismatch a small portion of the supply noise appears at node V_S due to imperfect cancellation by the replica branch. In other words, the amplifier output voltage v_a (refer to Fig. 2.14), generated by the regulator to suppress supply noise component in the replica branch, does not completely suppress supply noise in the main branch. Mathematically, using small-signal analysis, the regulator supply noise transfer function can be derived to be,

$$\frac{v_S(s)}{v_n(s)} = \frac{S_{V_{DD},P}}{1 + sC_d\left(r_{vco} \parallel r_{ds,P}\right)} - \frac{g_{m,P}S_{V_{DD},R}A_a\dfrac{r_{vco} \parallel r_{ds,P}}{1 + sC_d\left(r_{vco} \parallel r_{ds,P}\right)}}{A_aA_o + \left(1 + \frac{s}{\omega_a}\right)\left(1 + \frac{s}{\omega_o}\right)}. \tag{2.18}$$

This can be rearranged to get

$$\frac{v_S(s)}{v_n(s)} = \frac{S_{V_{DD,P}}\left(1 + mLG(s)\right)}{\left(1 + \dfrac{s}{\omega_d}\right)\left(1 + LG(s)\right)} \tag{2.19}$$

where the factor m represents the mismatch in the $g_m r_{ds}$ values of transistors M_R and M_P and is equal to

$$m = 1 - \frac{g_{m,P}r_{ds,P}}{g_{m,R}r_{ds,R}}. \tag{2.20}$$

Note that Eq. (2.19) reduces to Eq. (2.11) when m is equal to zero. The simulated regulator PSRR curves for various values of mismatch factor m are shown in Fig. 2.18. The value of m for a particular design depends on various factors such as the mismatch in the I-V characteristics of the replica load and the VCO

along with the statistical mismatch between the transistors M_R and M_P. Here, we estimate the degradation in the DC rejection of the regulator for various values of m without assuming a particular source for the mismatch. The mismatch factor is normalized by the DC loop gain in these simulations as the effect of mismatch is proportional to the product of the mismatch factor and the loop gain. It can be seen that the DC rejection of the regulator is nearly unaffected for values of m less than 1/LG(0). On the other hand, for values of m greater than 1/LG(0), the DC rejection is severely limited by mismatch. Therefore, it is important to match transistors M_R and M_P by careful device sizing and good layout techniques.

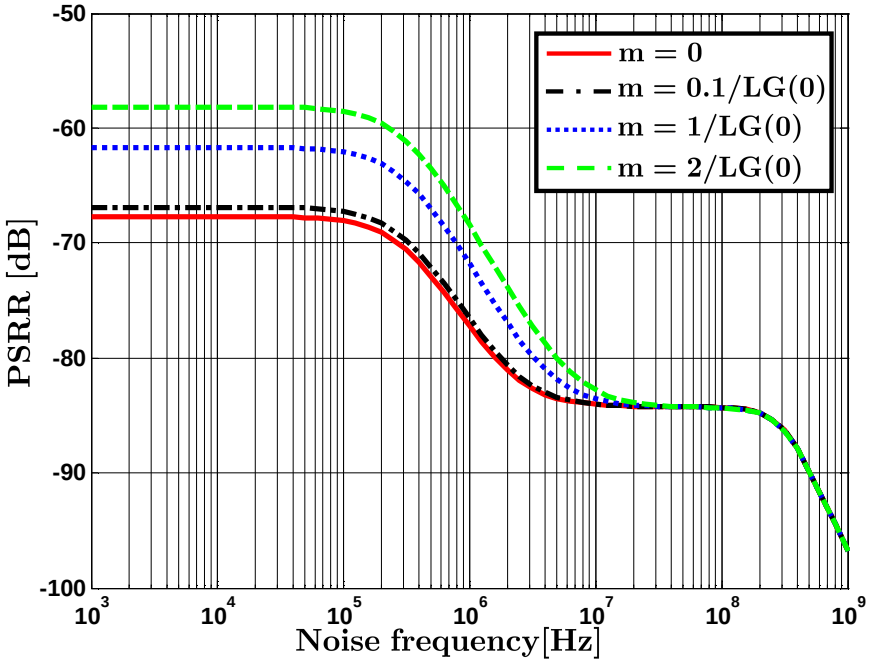

Figure 2.18: Simulated PSRR for different values of the mismatch parameter m.

To get a more realistic estimate of the impact of mismatch on the regulator DC PSRR, a Monte Carlo simulation was carried out on the transistor-level schematic of the regulator. Using mismatch parameters of A_{V_T} = 6mV-μm and A_β = 5% [19], hundred thousand PSRR simulations were performed. This accounts

for statistical mismatch in transistors M_R and M_P as well as the mismatch in the I-V characteristics of the replica and the VCO. The simulation results, as depicted in Fig. 2.19, are plotted as a histogram of the DC PSRR. These simulation results indicate that the regulator is relatively immune to a reasonable amount of mismatch between the critical transistors of the regulator circuit. Also, proposals [20] to improve the PSRR of the regulator have been made recently wherein the effect of mismatch of the PMOS transistors on the PSRR has been considerably reduced.

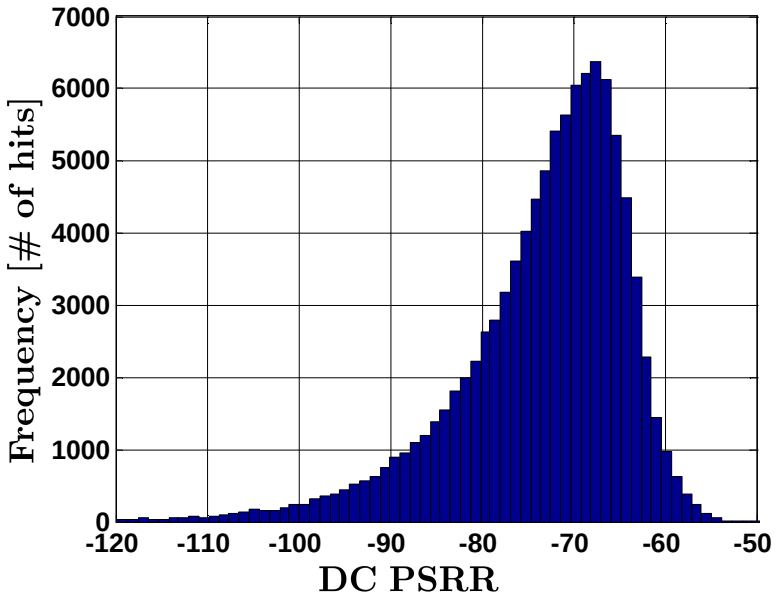

Figure 2.19: Histogram of the regulator DC PSRR obtained from a Monte Carlo simulation of the transistor-level regulator circuit for 100K trials.

2.5 Building Blocks

In this section, we will present the circuit implementation details of the pertinent building blocks of the proposed supply-regulated PLL (refer to Fig. 2.9). The PFD employs the well-known 3-state state-machine architecture and is imple-

mented using the pass-transistor structure [21]. The schematic of the charge-pump circuit is shown in Fig. 2.20. It utilizes a single-ended source-switched architecture for high-speed operation. A reference current, I_{Ref}, is mirrored to the output current source transistors M_P and M_N with a mirror ratio of 10 to minimize power consumption in the bias branches. The output currents are turned ON or OFF by controlling switches S_1 and S_3 with PFD outputs, $\overline{UP}$ and DN, respectively. Switches S_2 and S_4, controlled by the complimentary PFD outputs UP and $\overline{DN}$, are included to minimize the current mismatch due to charge-sharing [9]. To account for the drop across switches S_1 and S_3, and to improve the current-mirroring accuracy; dummy switches S_5, S_6, and S_7 are used in the bias branches.

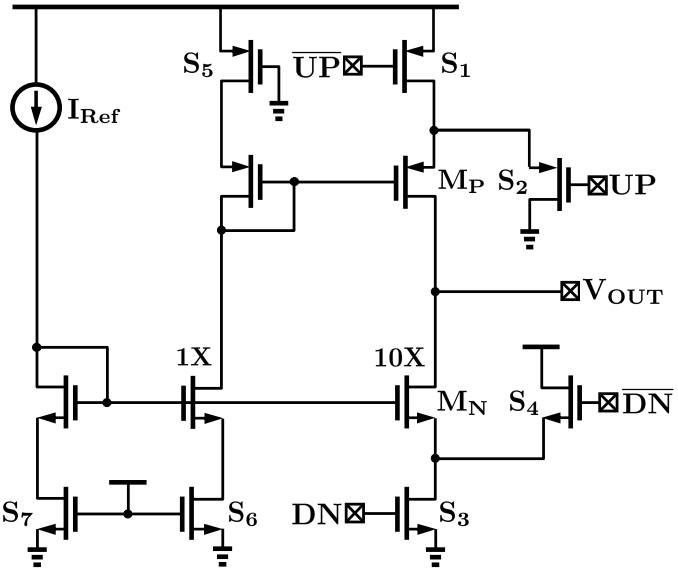

Figure 2.20: Schematic of the Charge Pump circuit used in the proposed design.

A three stage split-tuned pseudo-differential VCO shown in Fig. 2.21 is employed in our design [22]. The delay cell consists of two inverters whose outputs are coupled in a feed-forward manner through the NMOS/PMOS pass transistor pair. This coupling ensures differential operation of the oscillator. Coarse tuning is achieved by controlling the supply voltage, V_S, of the inverters. A tunable NMOS

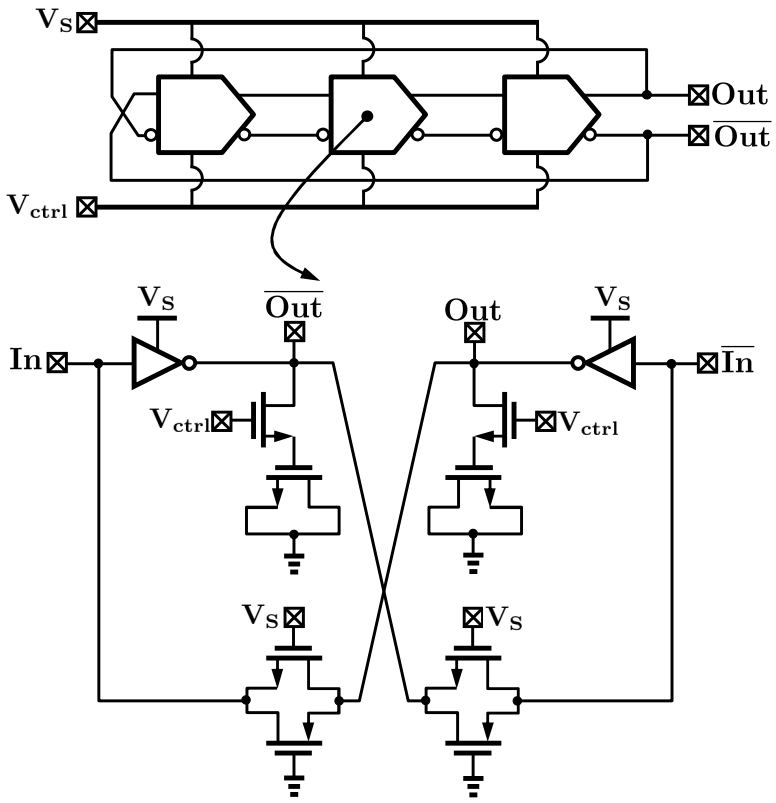

Figure 2.21: Schematic of the VCO circuit used in the proposed design.

transistor-based RC branch is employed in each delay cell for fine tuning the VCO frequency. The individual cell delay is modulated by changing the gate voltage of the NMOS resistor. In order to have fine control gain much lower than the coarse control gain, sizes of the NMOS resistor and the capacitor in the fine-tuning path are chosen to be much smaller than the size of transistors in the inverter. The fine control scheme of the VCO, employed in this design, is not suitable for implementation of conventional self-biasing techniques; however, due to the change in delay associated with the NMOS RC branch with the reference frequency, the fine-control gain scales with the reference frequency. This leads to scaling of PLL bandwidth with reference frequency in a non-linear way. As shown in Fig. 2.22,

circuit simulations indicate that bandwidth to reference frequency ratio varies by 25% with reference frequency in the typical corner. This ratio varies by 25% with process for the reference frequency of 500MHz. The peaking in the jitter transfer function under all conditions is less than 3dB.

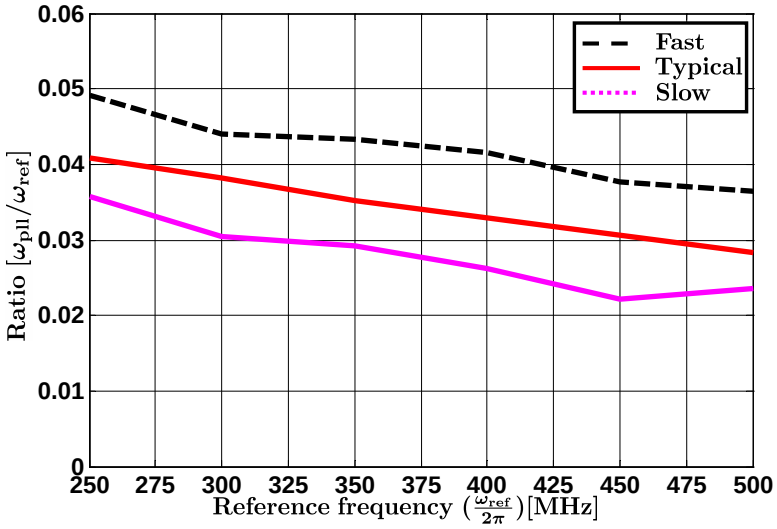

Figure 2.22: Ratio of bandwidth to reference frequency.

The output swing of the VCO depends on the size of the pass transistor MOSFETs relative to that of the inverters. If the pass-transistor device size is made comparable to the transistor device size of the inverter, the resulting swing will be lower than the inverter supply voltage, V_S. On the other hand, if the pass transistor size is made smaller than that of the inverter, the coupling between the inverter outputs will be weaker, resulting in limited attenuation of the common-mode gain. Hence the size of the pass transistors must be chosen carefully to meet both the requirements– wide-swing and maximum attenuation of the common-mode signal. In our design, pass transistors were sized ten times smaller than the devices of the inverters. Simulated coarse and fine voltage-to-frequency transfer curves of the VCO are depicted in Fig. 2.23. When the VCO is operating at 1.5GHz

with the reference voltage V_{REF} set to 1V, the coarse and fine control gains are approximately 4.5GHz/V and 70MHz/V, respectively. A level-shifting VCO buffer

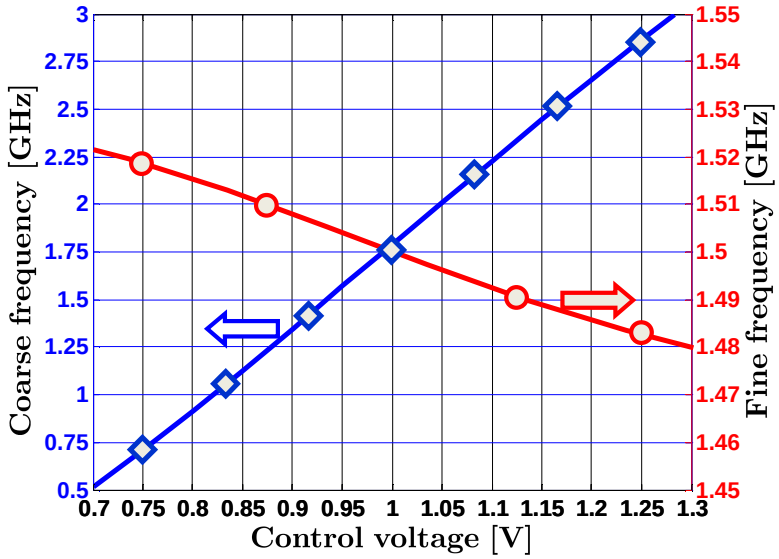

Figure 2.23: VCO output frequency plotted against fine control voltage.

similar to the one employed in [10] is used at the output of the VCO as the swing of the VCO is not rail-to-rail.

The transconductor used in the $G_M - C_I$ integrator of the coarse-tuning control loop is shown in Fig. 2.24. The input common-mode is fixed as the coarse-control loop biases the input of the transconductor to the reference voltage, V_{REF} and hence, a relatively simple input stage is employed. A wide-swing folded output stage is employed to maximize the VCO operating range. The output stage is switched in a way similar to the current switching in the charge-pump. By having a low duty-cycle clock control these switches, the effective value of the transconductance is greatly reduced thereby obviating a large capacitor to realize a very large time constant. The clock used in this design has a duty cycle ratio of 1 : 1024 and is generated on-chip using digital logic.

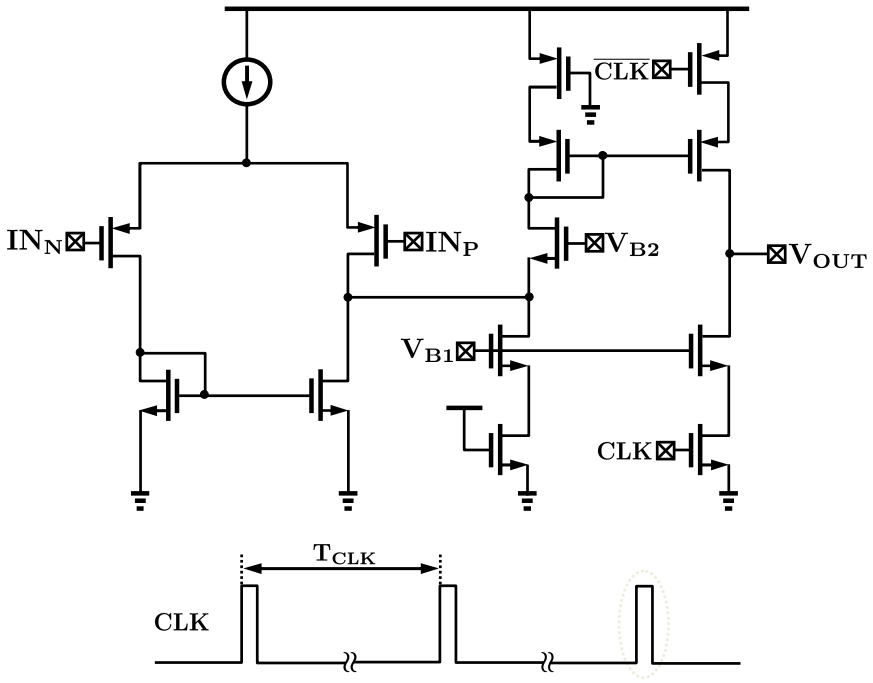

Figure 2.24: Schematic of the switched-transconductor circuit used in the G_M-C integrator.

2.6 Experimental Results

A prototype IC was developed using the proposed split-tuned PLL and was fabricated in a 0.18μm digital CMOS process. Figure 2.25 shows the die photograph of the prototype and occupies an active area of 0.093mm^2 (300μm$\times$310μm). The supply-regulation test was performed by modulating the regulator supply with a sinusoidal tone. Package parasitics along with the bypass capacitance and other stray parasitics dampen the injected noise on-chip. To ensure the reliability of the test, the actual noise level reaching the regulator is measured by a wide-bandwidth voltage follower circuit that operates from a clean supply, shown as supply-noise monitor in Fig. 2.9.

A sinusoidal signal imposed on the supply voltage introduces tones in the

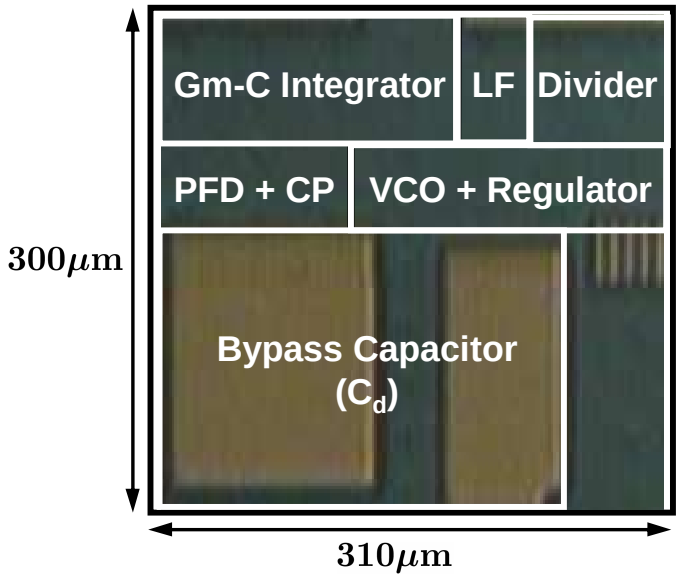

Figure 2.25: Die photograph.

spectrum of the output clock of the PLL. For example, if the PLL output frequency is 1.5GHz, a supply-noise tone at 50MHz introduces tones at 1.55GHz and 1.45GHz in the the output clock spectrum. If the difference between the magnitudes of the tones at 1.5GHz (the oscillation frequency) and at 1.55GHz (or 1.45GHz) is M dB, then the peak-to-peak deterministic jitter (T_j) due to the supply noise can be calculated using the following equation:

$$T_j = \frac{2T}{\pi} 10^{(M/20)} \tag{2.21}$$

where T is the period of the output clock. Figure 2.26 shows the measured PLL output spectrum when a 200mV peak-to-peak, 8.85MHz sinusoidal tone is superimposed on the supply. As shown later, this measurement represents the worst-case condition in terms of PLL's sensitivity to supply noise. Substituting M = −32dB and T = 1/1.5GHz in Eq. (2.21), we calculate the worst-case peak-to-peak jitter of 10.6ps resulting from the 200mV peak-to-peak supply noise tone. Using

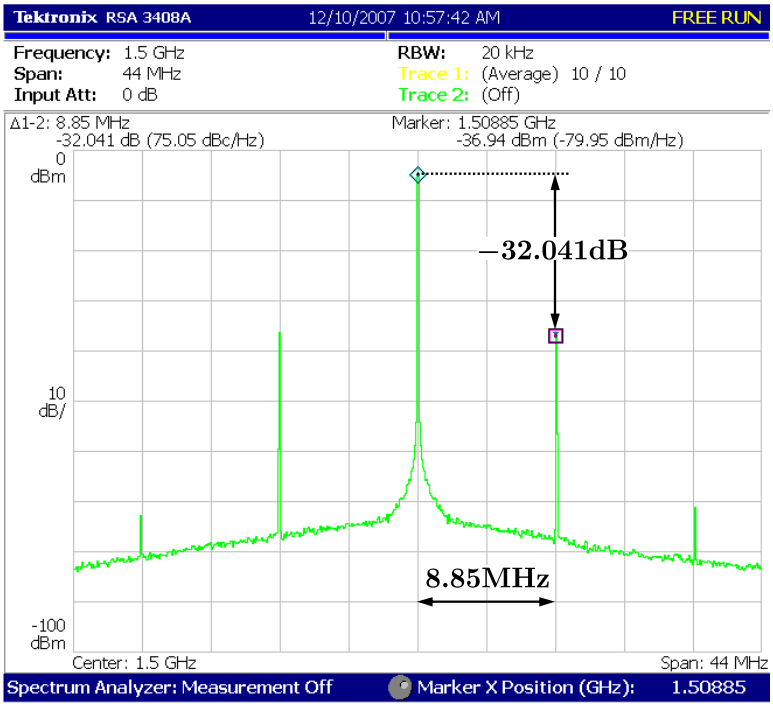

Figure 2.26: Spectrum of output clock with a supply-noise amplitude of $200\text{mV}_{\text{pk-pk}}$ at 8.85MHz.

Eq. (1.1), this corresponds to a worst-case PSNR of -28dB. Figure 2.27 shows the measured PSNR of the PLL along with the equivalent time-domain peak-to-peak supply-noise induced jitter. The worst-case PSNR of -28dB represents an improvement of at least 20dB over the conventional supply-regulated PLL and 15dB over the PLL employing a replica-based regulator [13]. Alternatively, in time domain a worst case peak-to-peak jitter of only 10.6ps translates to a sensitivity of 50fs/mV (0.5rad/V). To validate frequency-domain measurement results presented thus far, the measured jitter histograms without and with supply noise are shown in Fig. 2.28 and Fig. 2.29, respectively. Figure 2.29 was obtained when the PLL was operating under the worst-case supply noise condition ($200\text{mV}_{\text{pk-pk}}$, 8.85MHz sinusoidal supply-noise voltage). These histograms also indicate, as expected, that

the peak-to-peak jitter is degraded by only about 10ps under the worst-case supply noise condition.

The performance summary of the prototype is summarized in Table I. The power consumption of the PLL operating at 1.5GHz is 3.9mW from a 1.8V supply, of which 1.2mW is consumed in the VCO and only 0.27mW in the regulator. The VCO power consumption was minimized by choosing a large PLL bandwidth without compromising its noise performance. This is only possible in the proposed PLL because the regulator bandwidth is completely decoupled from the PLL bandwidth. The design of a regulator in conjunction with the proposed supply-regulated PLL

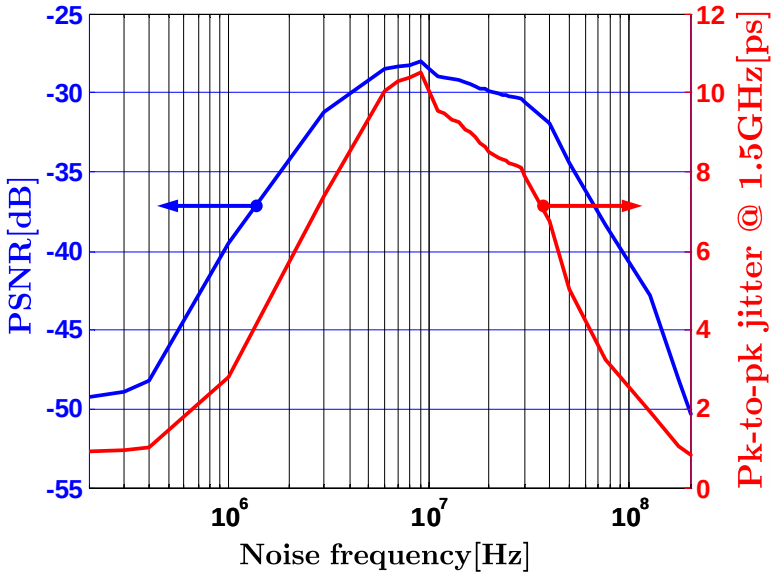

Figure 2.27: Measured power-supply noise rejection (PSNR) performance and jitter with a supply-noise amplitude of $200\text{mV}_{\text{pk-pk}}$.

offers the advantage of the regulator being designed independent of the PLL loop, giving tremendous flexibility in the design and leading to a low-power solution with significantly improved power-supply noise rejection properties.

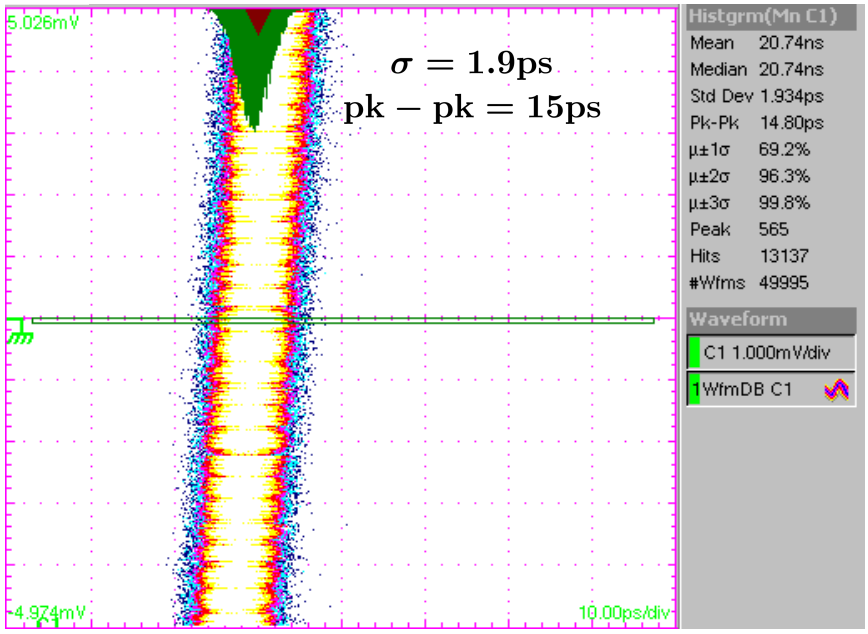

Figure 2.28: Jitter histogram without supply noise.

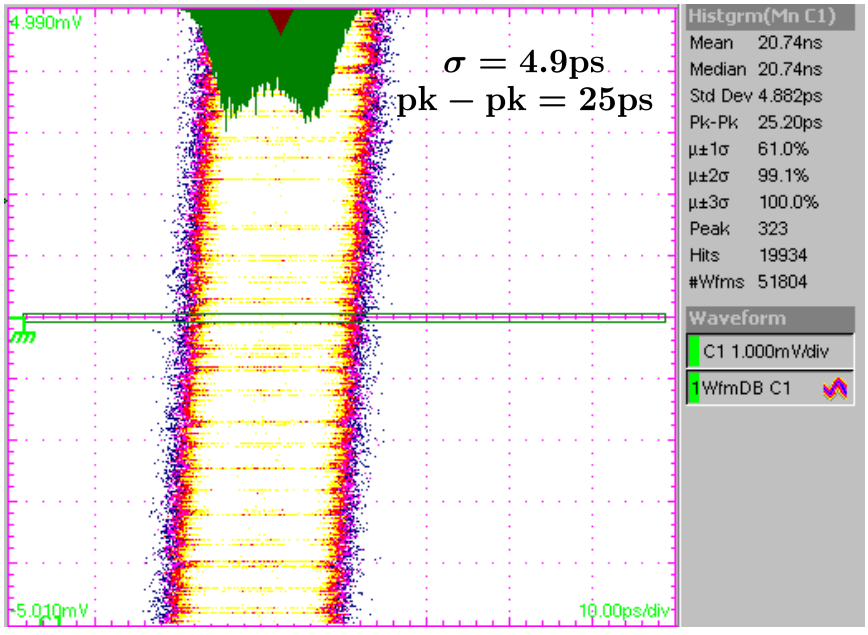

Figure 2.29: Jitter histogram with supply-noise amplitude of 200mV$_{\mathrm{pk-pk}}$ at 8.85MHz.

Table 2.1: Performance Summary

Technology	0.18μm CMOS
Supply Voltage	1.8V
Operating Frequency	0.5-2.5GHz
Jitter(r.m.s/pk-pk) @ 1.5GHz	1.9ps/15ps (no noise)
	4.9ps/25ps (200mV noise)
Power Consumption @ 1.5GHz	VCO: 1.2mW
	Regulator : 0.27mW
	Remainder of PLL : 2.5mW
	Total : 3.9mW
Active Die Area	0.093mm^2

2.7 Summary

In this Chapter, analysis of the effect of supply noise on the jitter performance of the PLL has been provided. Also, a split-tuned supply-regulated PLL architecture that achieves excellent supply-noise rejection while operating with low power is presented. By placing the regulator in the low-bandwidth coarse control loop of the PLL, the proposed PLL allows the regulator and the PLL bandwidth to be chosen independently. Hence, the proposed PLL overcomes a severe limitation present in all conventional supply-regulated PLLs namely, the regulator bandwidth be more than 2-3 times the PLL bandwidth. In the proposed architecture, the PLL bandwidth can be maximized to suppress the VCO phase noise without incurring any power penalty in the regulator. A regulator architecture that specifically exploits the benefits offered by the supply-regulated split-tuned PLL is presented.

This regulator introduces a low-frequency pole in its supply-noise transfer function using a replica branch in order to avoid supply-noise degradation beyond the regulator-loop's dominant pole frequency. Measured results obtained from a prototype PLL test chip fabricated in a standard digital CMOS process validate the effectiveness of the proposed techniques. Specifically, the prototype PLL chip operating at 1.5GHz achieves better than -28dB power-supply noise rejection while consuming only 3.9mW from a 1.8V power supply. The achieved PSNR represents better than 15dB improvement over the state-of-the art supply-regulated PLL.

CHAPTER 3. SUPPLY REGULATION OF PLL BUILDING BLOCKS

From Chapter 2, it is evident that effect of noise on the VCO supply is the most pronounced in ring-oscillator based PLLs. As discussed in Chapter 1, the effect of noise on the other building blocks of the PLL becomes pronounced once the VCO supply is well regulated. In this Chapter, we will provide analytical, simulation, and design techniques to address supply noise in the other building blocks of ring-oscillator based PLL. This Chapter is organized as follows. Brief analysis of supply noise in PLL building blocks is presented in Section 3.1, Section 3.2 describes the proposed architecture while Section 3.3 discusses the issues with regulator design and the experimental results are presented in Section 3.4.

3.1 Supply Noise in PLL Building Blocks

The impact of supply noise on all PLL building blocks will be analyzed using the small-signal block diagram shown in Fig. 3.1. By adding supply-noise coupling paths into the conventional small-signal model of the PLL, this model allows transfer function based analysis to quantify the impact of supply noise. Much like the conventional noise analysis, the contribution of each of the building blocks to the supply-noise induced output jitter is calculated using the supply-noise transfer functions derived from Fig. 3.1. This analysis relies on the assumption that PLL supply-noise response is linear, a claim validated by measured results for reasonable amplitudes of supply noise (see Fig. 3.16). Supply-noise sensitivities, transfer

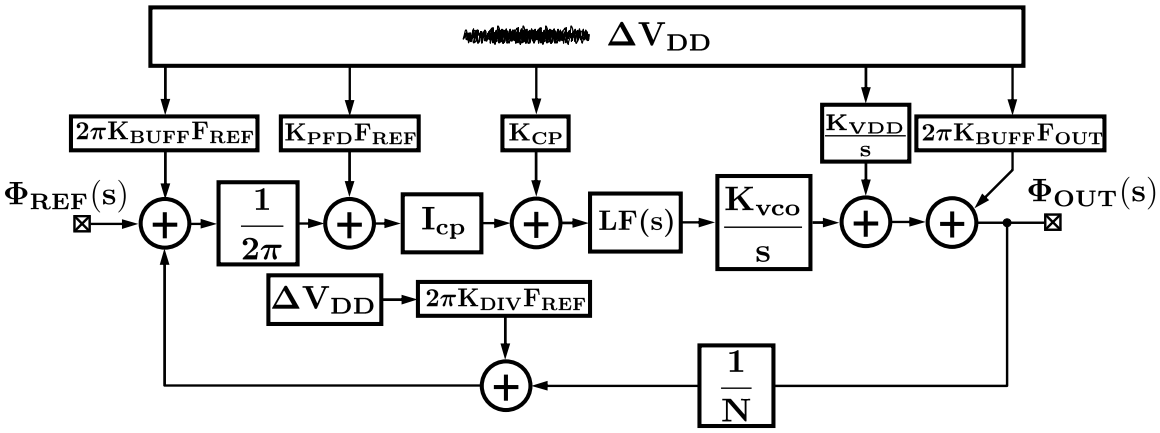

Figure 3.1: Small-signal block diagram of the PLL.

functions, and jitter contribution of each of the building blocks are evaluated in the rest of this section. Effect of supply noise in ring-VCOs was dealt with in Chapter 2. Hence we begin by considering the effect of charge pump power supply noise on the PLL.

3.1.1 Supply noise in charge pump

Single-ended source-switched charge-pumps such as the one shown in Fig. 3.2 are most commonly employed because of their fast-switching characteristics. Unfortunately, these charge-pumps are very sensitive to supply noise as illustrated by the simulated charge-pump PSNR curve in Fig. 1.3. This susceptibility arises from UP/DN current mismatch induced by: (i) finite output impedance of the current sources and (ii) asymmetric noise coupling into the UP and DN current sources through the bias circuitry. The supply-noise induced current mismatch causes the charge

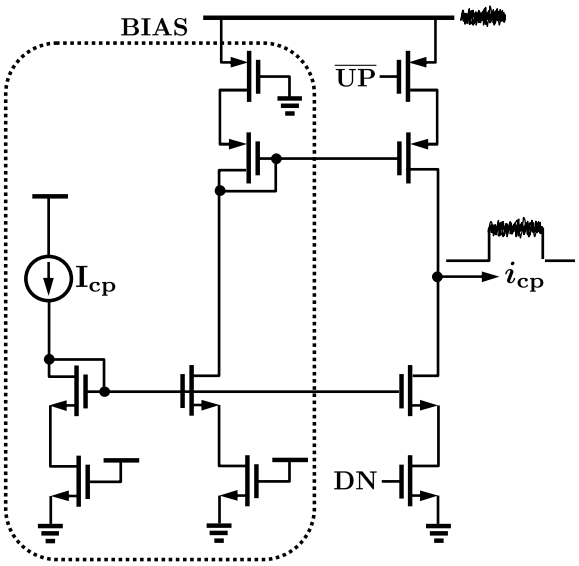

Figure 3.2: Supply noise in source-switched charge-pump.

pump to output an additional charge equal to

$$\Delta Q_{CP} = I_{UP} t_{UP} - I_{DN} t_{DN} \tag{3.1}$$

where, t_{UP} and t_{DN} denote the pulse widths of UP and DN signals at the PFD output, respectively. Note that the PLL feedback forces t_{UP} and t_{DN} to be unequal in the presence supply-noise induced current mismatch. The sensitivity of charge pump to supply noise is equivalent to the sensitivity of ΔQ_{CP} to supply noise. We define the charge pump sensitivity, K_{CP}, to its supply as the average change in the output current of the charge pump due to change in supply. Mathematically,

$$K_{CP} = \frac{1}{T_{ref}} \frac{d\Delta Q_{CP}}{dV_{DD}}. \tag{3.2}$$

Using the expression for ΔQ_{CP}, we can derive K_{CP} as a function of UP/DN currents and UP/DN pulse widths as,

$$K_{CP} = \frac{1}{T_{ref}} \left(t_{UP} \frac{dI_{UP}}{dV_{DD}} - t_{DN} \frac{dI_{DN}}{dV_{DD}} \right). \tag{3.3}$$

Having determined the supply-noise sensitivity, the PSNR of the charge pump can be derived as,

$$\mathrm{PSNR_{CP}(s)} = \frac{\mathrm{K_{CP}}}{\mathrm{I_{CP}}} \frac{\mathrm{NLG(s)}}{1 + \mathrm{LG(s)}}. \tag{3.4}$$

In the above equation, $\mathrm{I_{CP}}$ is the average of the UP and DN currents and the PLL loop gain LG(s) is given by,

$$\mathrm{LG(s)} = \frac{\mathrm{I_{CP}K_{VCO}}(1 + \mathrm{RC_1 s})}{2\pi \mathrm{N}(\mathrm{C_1} + \mathrm{C_2})\mathrm{s}^2(1 + \mathrm{sRC_1C_2}/(\mathrm{C_1} + \mathrm{C2}))}, \tag{3.5}$$

where, $\mathrm{K_{VCO}}$, R, $\mathrm{C_1}$, $\mathrm{C_2}$, and N denote the VCO gain in rad/sec/V, loop filter resistance, loop filter capacitance, the loop filter ripple-pole capacitance, and the feedback divider ratio, respectively. A plot of the PSNR curve shown in Fig. 3.3,

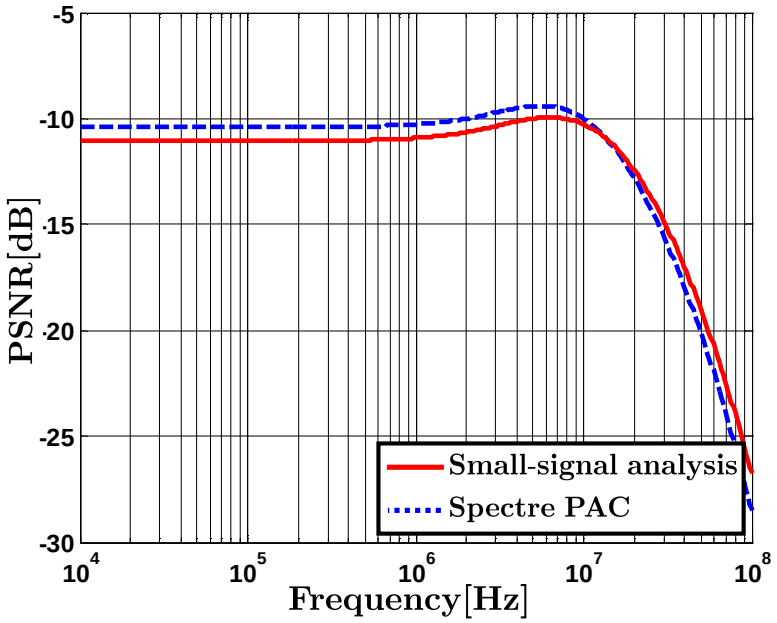

Figure 3.3: Charge pump PSNR curves generated using small-signal transfer function and transistor-level Spectre PAC simulation.

indicates that the charge pump PSNR follows a low-pass response and closely matches the PSNR curve generated using Spectre PAC simulations, thus illustrating the validity of the presented analysis. Figure 6 also reveals that the worst-case

PSNR is about -10dB, thus mandating the need for a charge pump supply regulator to meet the design target of -35dB. It should also be pointed out that the above analysis, while accurate for most practical cases, is valid only for small variations in charge pump current ($< 10\%$). For larger variations, time varying behavior of the PLL loop gain due to the gain variation of the charge pump can not be neglected and a more thorough analysis using harmonic transfer functions is needed [23, 24]. This will be dealt with in Chapter 4.

3.1.2 Supply noise in divider and clock buffers

Supply noise in *digital* circuit elements of the PLL such as the divider and clock buffers also contribute significantly to the output jitter. A vast majority of the clock buffers and the dividers in the PLL are implemented either directly by CMOS inverters or structures derived from them (for e.g. true single phase clock flip-flop). Hence, supply-noise sensitivity of the *digital* building blocks can be understood simply by examining the CMOS inverter shown in Fig. 3.4. The

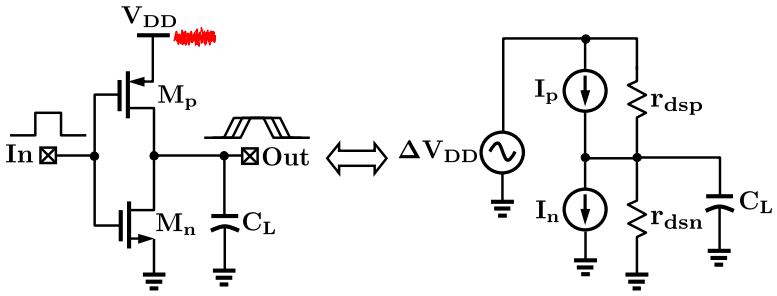

Figure 3.4: Supply noise in a CMOS inverter.

delay of a CMOS inverter is a strong function of the supply voltage as the charging and discharging currents, I_p and I_n, increase/decrease with the supply voltage. The

low-to-high transition delay t_{dLH} of a CMOS inverter is given by [25, 26],

$$t_{dLH} = \left\{ \frac{1}{2} - \frac{1 - V_{Tp}/V_{DD}}{3} \right\} t_{HL} + \frac{C_L V_{DD}}{2 I_p} \tag{3.6}$$

where $I_p = \beta_p (V_{DD} - V_{Tp})^2$ is the PMOS charging current when operating in the saturation region and t_{HL} is the input fall time. Hence, the supply voltage sensitivity of the inverter delay for a low-to-high transition is given by,

$$\begin{aligned} K_{INV} &= \frac{dt_{dLH}}{dV_{DD}} \\ &= -\left(\frac{V_{Tp}}{3V_{DD}^2} t_{HL} + \frac{C_L}{2\beta_p} \left\{ \frac{V_{DD} + V_{Tp}}{(V_{DD} - V_{Tp})^3} \right\} \right) \end{aligned} \tag{3.7}$$

which suggests that the inverter supply-noise sensitivity is inversely proportional to the square of the supply voltage. Since digital circuits such as the clock buffer and the divider are typically implemented using CMOS logic style, they also exhibit very similar supply sensitivity as the inverter. As a consequence, denoting the supply sensitivities of the divider and the clock buffers as K_{DIV} and K_{BUF}, respectively, the PSNR of these building blocks can be derived to be,

$$PSNR_{DIV}(s) = K_{DIV} F_{ref} \frac{NLG(s)}{1 + LG(s)}, \tag{3.8}$$

$$PSNR_{BUFF,IN}(s) = K_{BUFF,IN} F_{ref} \frac{NLG(s)}{1 + LG(s)}, \tag{3.9}$$

$$PSNR_{BUFF,VCO}(s) = K_{BUFF,VCO} F_{ref} \frac{N}{1 + LG(s)}, \tag{3.10}$$

where, F_{ref} is the reference clock frequency. A plot of the PSNR curves shown in Fig. 3.5 reveal, as expected, that the divider and the input buffer exhibit a low-pass transfer response and the PSNR of the output buffer takes a high-pass shape. More importantly, digital blocks suffer from much worse PSNR compared to that of a supply-regulated VCO (see Fig. 1.3). Consequently, an efficient supply-regulation scheme that improves the PSNR to meet the design target of -35dB is needed.

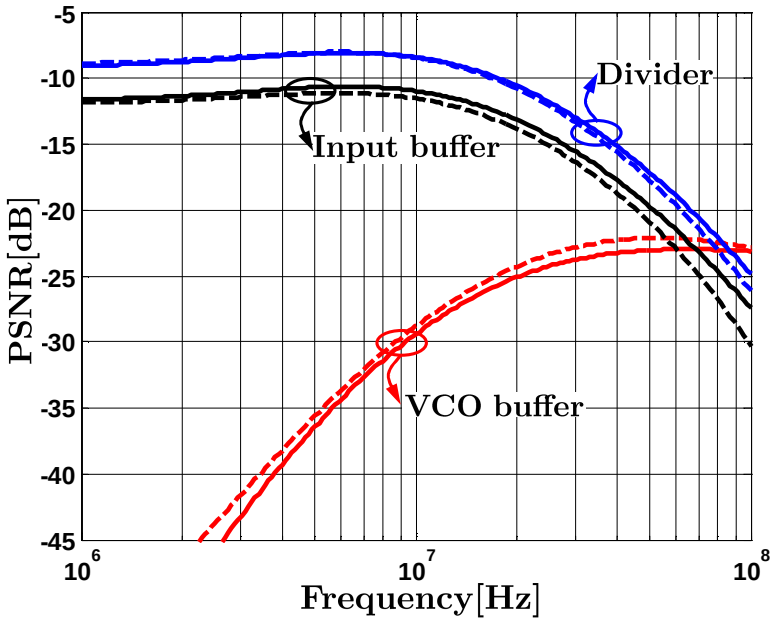

Figure 3.5: PSNR of divider and clock buffer. PSNR obtained from small-signal analysis and Spectre PAC simulations are indicated by solid and dotted lines, respectively.

3.1.3 Supply noise in PFD

The conceptual schematic of a commonly used phase frequency detector is shown in Fig. 3.6. Ideally, up (UP) and down (DN) paths are fully symmetric since they are made out of identical flip-flops and a symmetric AND gate. In practice, careful attention is paid to minimize the mismatch between the UP and DN paths to suppress reference spurs or equivalently, in time domain, to minimize deterministic jitter. Under these conditions of symmetry and perfectly matched UP/DN current sources in the charge pump, the supply-noise induced jitter in the UP and DN signals is cancelled resulting in excellent supply-noise immunity of the PFD. However, any systematic mismatch between UP/DN paths in the PFD or UP/DN current sources in the charge pump causes imperfect cancellation,

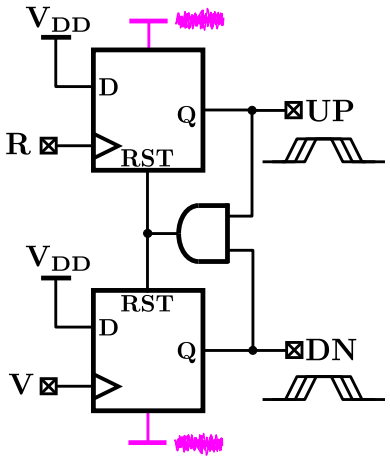

Figure 3.6: Conceptual PFD schematic illustrating the effect of supply noise.

resulting in leakage of the PFD supply noise to the output of the PLL.

To quantify the effect of PFD supply noise due to UP/DN path mismatches, denoting the reset pulse duration of UP/DN signals as $t_{rst,UP}$ and $t_{rst,DN}$, respectively, consider the case when the time difference between the inputs of the PFD is equal to ΔT, as shown in Fig. 3.7. Under this condition, the charge pump outputs

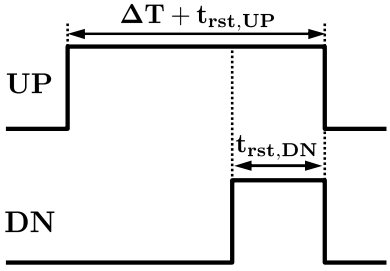

Figure 3.7: UP and DN pulses of a PFD for a nominal time difference of ΔT.

a charge given by,

$$\begin{aligned} Q_{CP} &= I_{CP}\Delta T + I_{CP}(t_{rst,UP} - t_{rst,DN}) \\ &= Q_{DESIRED} + \Delta Q, \end{aligned} \tag{3.11}$$

where, ΔQ denotes the additional charge due to the PFD supply noise. Noting that UP/DN reset pulse mismatch (Δt_{rst}) is the only supply-dependent component of ΔQ, the PFD supply-noise sensitivity, K_{PFD}, can be defined as,

$$K_{PFD} = \frac{d(\Delta t_{rst})}{d\Delta V_{DD}}. \tag{3.12}$$

Having defined the PFD supply-noise sensitivity, the PSNR of the PFD derived using the small-signal model shown in Fig. 3.1 is given by,

$$PSNR_{PFD}(s) = NK_{PFD}F_{REF}\frac{LG(s)}{1+LG(s)}. \tag{3.13}$$

The validity of the PFD PSNR expression is evaluated by plotting the magnitude of Eq. 3.13 along with the transistor-level Spectre PAC simulation in Fig. 3.8. Good matching between the two PSNR curves illustrate the accuracy of the derived analytical expression.

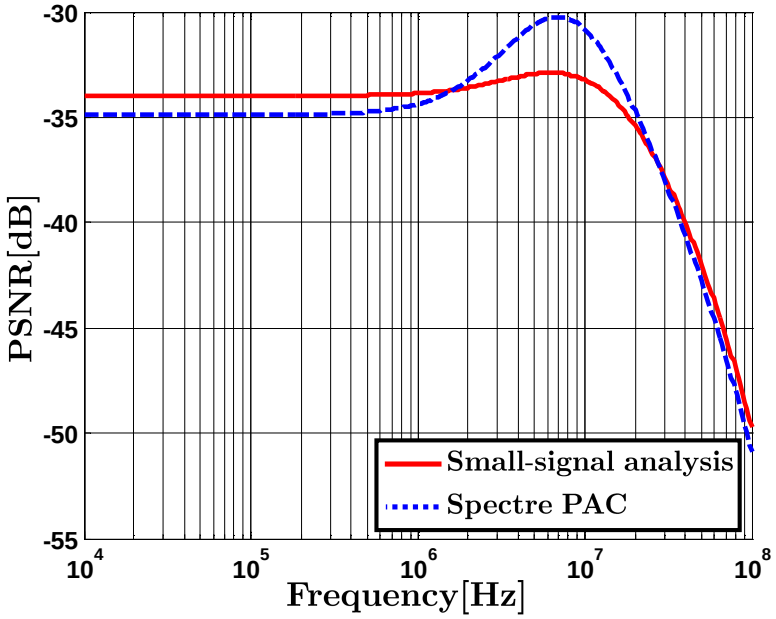

Figure 3.8: Power-Supply Noise Rejection of PFD obtained through small-signal analysis and through Spectre PAC simulations.

From the above analysis, it can be concluded that the PFD exhibits excellent immunity to supply noise under the zero static phase offset condition. However, PFD supply-noise sensitivity, K_{PFD}, increases drastically in the presence of a static phase offset in the PLL. In applications such as fractional frequency synthesizers, a known static phase offset in often introduced to operate the PFD, charge pump combination in a more linear region [27]. The asymmetry in the UP/DN paths due to the static phase offset increases the value of K_{PFD}, thus degrading the PFD PSNR. Simulations show that a static phase offset of 180° increases K_{PFD} to as high as 30ps/V from its nominal value of 10ps/V at smaller phase offsets. Note that sensitivity of 30ps/V translates to a reset pulse width mismatch of 300fs for a 10mV change in supply voltage. Changes in the reset pulse mismatch of this order can be easily caused by the asymmetric delays in the UP/DN paths. For instance, the input capacitance of the AND gate depends on its input state causing a difference in the loading of UP/DN D-flip flops. To verify this, simulations were performed on the PFD which indicated that K_{PFD} decreases to 15ps/V from 30ps/V when a transistor-level AND gate is replaced by an ideal gate. Such a change in K_{PFD} translates to a degradation of the PSNR from -34dB to about -25dB. Consequently, in almost all practical cases, a PFD supply regulator is needed to achieve the target PSNR of -35dB in the presence of large static phase offsets. In the following section, a PLL architecture wherein regulators are used to shield the digital building blocks from supply noise is presented.

3.2 Supply-Regulated PLL Architecture

The PLL architecture which strives to minimize supply-noise induced output jitter is shown in Fig. 3.9. The PLL employs a split-tuned VCO that is

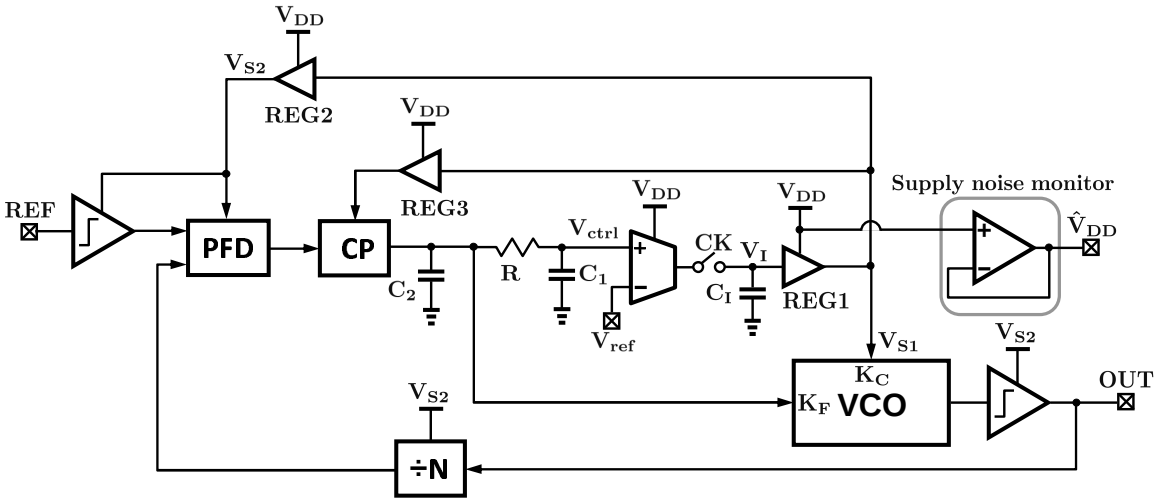

Figure 3.9: Proposed supply-regulated PLL architecture.

controlled through a high-gain low-bandwidth coarse control path and a low-gain wide-bandwidth fine control path [28]. The frequency-tracking coarse control loop integrates the voltage across the loop-filter capacitor C_1 and produces an output voltage V_I. This voltage serves as an input to a low-dropout regulator (REG1) whose output serves as the supply (coarse control) voltage V_{s1} to the VCO. A regulator architecture that provides better than -40dB power supply noise rejection is employed to effectively shield the VCO from supply perturbations [6].

In addition to the many benefits offered by the split-tuned PLL architecture [15], it also has superior low-frequency immunity to VCO supply noise. It is well known that the VCO PSNR of a conventional single-loop PLL exhibits a bandpass shape with an ideal DC rejection of infinity. However, in practice, finite output impedance of the charge pump current sources severely limit the low-frequency VCO PSNR as illustrated in Fig. 3.10. Because in a split-tuned PLL, the low-frequency PSNR is boosted by the loop gain of the coarse control path, PSNR at 1kHz supply-noise frequency improves nearly by 40dB (see Fig. 3.10).

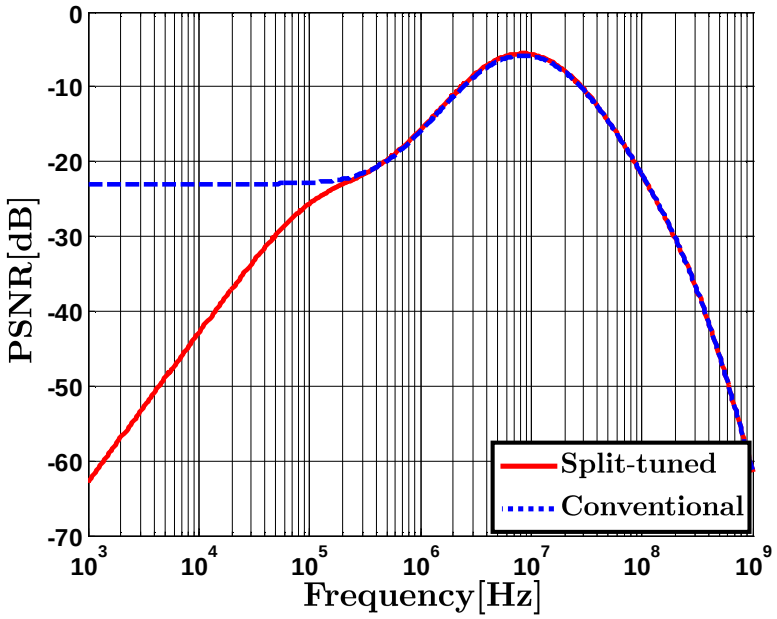

Figure 3.10: Simulated VCO PSNR with and without split-tuning in the PLL.

The supply-noise sensitivity of charge-pump, divider, and reference/VCO clock buffers is reduced by employing specially designed low-dropout regulators (REG2 and REG3). The VCO supply voltage V_{s1} serves as the input to both the regulators, thereby obviating the need for a bandgap reference circuit. This is advantageous because of the considerable difficulties in designing a low-voltage bandgap reference circuit with a good wide-band power supply rejection ratio [29]. Note that the coarse-control loop biases the charge-pump to a known voltage V_{ref} in steady-state, thereby circumventing any voltage headroom issues even in the presence of few hundred milli-volt drop in the regulator (REG3). Any potential start-up problems in this self-regulating architecture are avoided by a simple start-up circuitry that connects the inputs of regulators, REG2, REG3, to a known voltage at power-up. The design details of these regulators are discussed in the next section.

Supply-noise coupling through the coarse path of the split-tuned PLL must be considered to prevent any PSNR degradation of the PLL. Fortunately, narrow bandwidth of the coarse loop suppresses much of the supply noise and minimizes its impact on the overall PLL PSNR. In the prototype, coarse-loop bandwidth is made arbitrarily low by using a switched G_m-C integrator [6]. To suppress the coupling through the reference voltage derived from a noisy supply, additional filtering is provided by a low-pass filter composed of a 200kΩ resistor and a 25pF capacitor. The noise rejection curves shown in Fig. 3.11, obtained through transistor-level simulations of the PLL, indicate better than -60dB and -55dB rejection from V_{ref} and the supply of the G_m-C integrator, respectively. Because of this excellent inherent PSNR, the supply of the G_m-C integrator was left unregulated in the prototype.

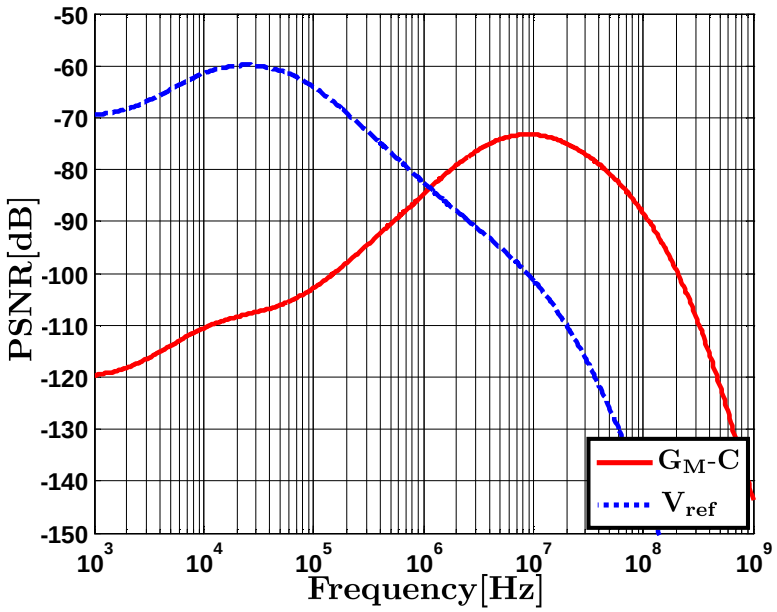

Figure 3.11: Simulated PSNR curves of the Gm-C integrator and the V_{ref} generation.

3.3 Regulator Design

Regulators used in the proposed architecture are co-designed with the PLL by accounting for the intrinsic supply-noise suppression provided by the PLL feedback itself. It has been shown that the PLL feedback suppresses (1) the high-frequency noise introduced into the PFD, charge-pump, and the divider supplies and (2) the low-frequency noise introduced into the VCO buffer supply. Consequently, in order to improve the wide-band supply noise immunity of the PLL, the regulators should provide excellent noise rejection for a broad range of frequencies.

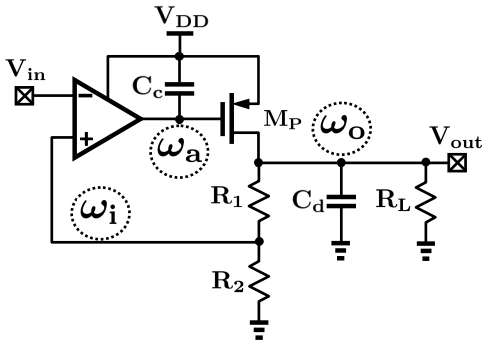

Figure 3.12: Low-dropout regulator.

A commonly used low dropout regulator is shown in Fig. 3.12, where, $\omega_{\rm i}$, $\omega_{\rm a}$, and $\omega_{\rm o}$ represent the pole frequencies at the amplifier input, amplifier output, and the regulator output nodes, respectively. The amplifier input capacitance is relatively small in regulators designed for light loads, and hence is not considered as a design parameter. The location of $\omega_{\rm a}$ and $\omega_{\rm o}$ plays a crucial role in determining the power-supply rejection properties of the regulator. Consider the power-supply noise rejection curves shown for the two frequency compensation cases ($\omega_{\rm a} < \omega_{\rm o}$ and $\omega_{\rm a} > \omega_{\rm o}$) in Fig. 3.13. The regulator provides good low-frequency rejection in both cases. However, for the case when $\omega_{\rm a} < \omega_{\rm o}$, the noise rejection degrades

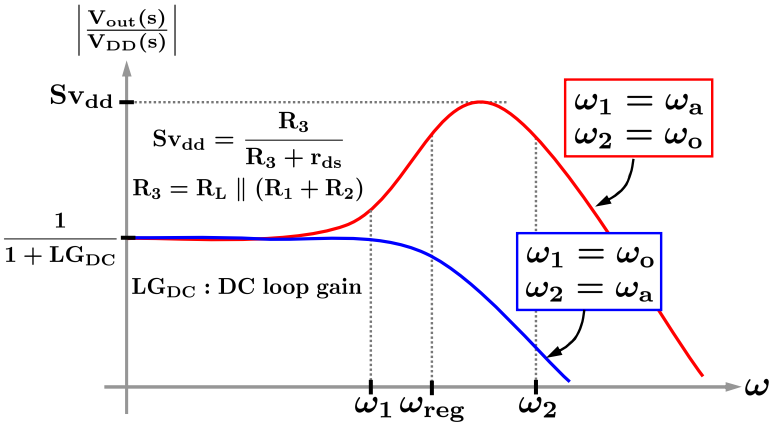

Figure 3.13: Regulator power supply noise rejection curves.

beyond the amplifier pole at the same rate as the loop gain would reduce. Consequently, in order to achieve good supply rejection in the vicinity of the PLL bandwidth, the amplifier pole, ω_a, should be moved to high frequency, a design requirement that incurs severe power penalty. On the other hand, when $\omega_a > \omega_o$, the regulator provides excellent wide band supply noise rejection as illustrated in Fig. 3.13. This condition ($\omega_o < \omega_a$) is, however, difficult to meet in practice for two reasons: First, a low load resistance R_L, defined as the ratio of regulator output voltage to the average load current pushes the output pole, ω_o, to high frequencies. Second, the large gate capacitance of the pass transistor reduces the amplifier pole frequency. While it is possible to increase the size of the capacitor C_d, to make ω_o dominant, it incurs a large area penalty. Fortunately, in the case of a PLL wherein the regulator needs to drive only low-power building blocks, it is possible to make ω_o dominant with reasonably small area penalty.

A replica-biased architecture that achieves better than -40dB worst-case power supply noise rejection is employed in the VCO regulator, REG1(see Fig. 3.9) [6]. Two regulators REG2, REG3 with output pole dominant compensation are

used to drive rest of the building blocks. The separation of regulators prevent the switching currents in the digital blocks (like divider, VCO buffer) from interacting with the charge pump. In both REG1 and REG2 a total bypass capacitor of 80pF was sufficient to make the output pole dominant and achieve about -40dB worst-case supply noise rejection. Simulated supply-noise sensitivities shown for unregulated and regulated cases in Table 3.1, illustrate that regulation improves the supply-noise immunity by about -30dB. With a regulator of -40dB supply-

Table 3.1: Supply Noise Sensitivities with and without regulation

Parameter	With Regulation	W/o Regulation
K_{PFD}	0.25 ps/V	10 ps/V
K_{CP}	0.16 μA/V	17 μA/V
K_{DIV}	2.7 ps/V	145 ps/V
$K_{BUFF,IN}$	4.2 ps/V	155 ps/V
$K_{BUFF,VCO}$	1.1 ps/V	31.65 ps/V

noise rejection, one would expect that the supply-noise immunity of the regulated blocks improves by a factor of 1/100. However, supply sensitivity of digital circuits increases at a lower supply voltages leading to a somewhat reduced improvement in the net supply-noise immunity. For instance, the input buffer supply-sensitivity plotted as a function of its supply voltage in Fig. 3.14 reveals that the immunity degrades from 155ps/V at 1.8V to about 420ps/V at 1.4V. Consequently, a regulator providing -40dB rejection with a dropout voltage of 0.4V improves the input buffer supply sensitivity from 155ps/V to only 4.2ps/V, instead of reducing it to 1.55ps/V.

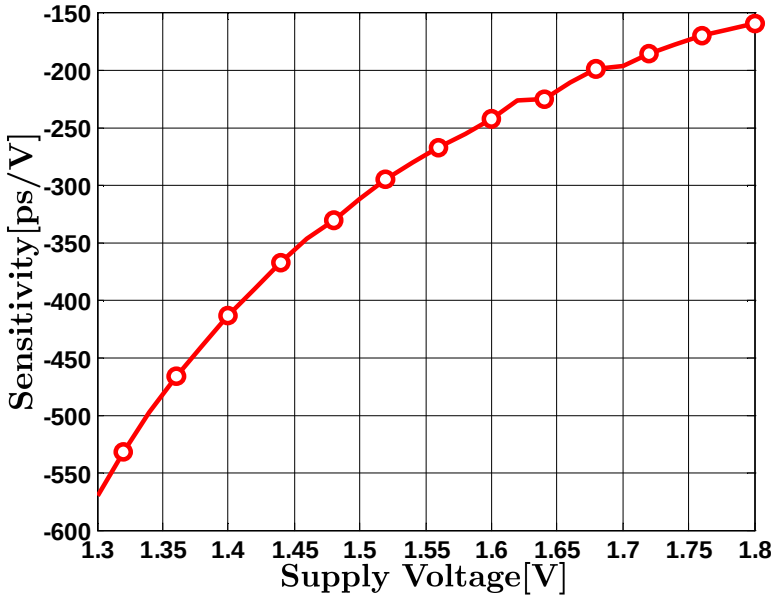

Figure 3.14: Variation of input buffer supply sensitivity.

3.4 Experimental Results

A prototype IC was fabricated in a 0.18μm digital CMOS process operates to evaluate the validity of the presented analysis and effectiveness of the proposed mitigation techniques. The die photograph is shown in Fig. 3.15. The PLL operates from 0.8GHz to 3GHz with a fixed feedback divide ratio of 4. All the ensuing measured results are presented at an operating frequency of 1.5GHz. In order to estimate the amount of noise on the internal supply voltages, the on-chip supply-noise monitor (see Fig.3.9) was first characterized for its DC gain and bandwidth. By sweeping the DC supply voltage and measuring the supply-noise monitor output, the gain was determined to be about 0.9. Hence, the input supply-noise amplitudes were scaled down by about 10% to account for less than unity gain of the monitor. Using an AC measurement the bandwidth of the supply-noise moni-

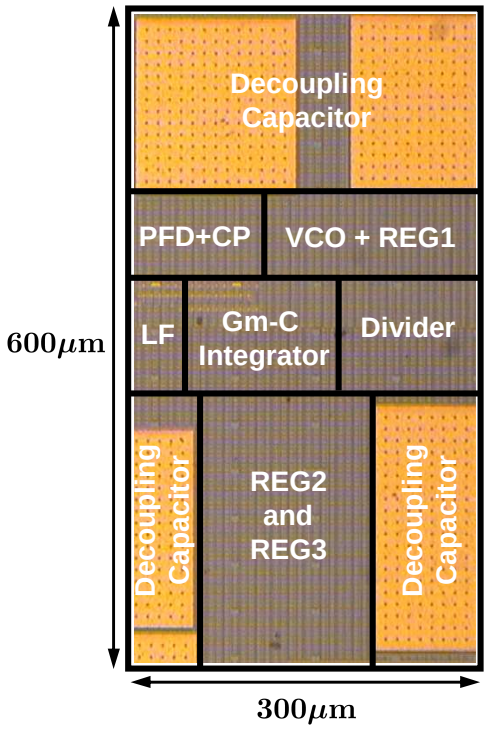

Figure 3.15: Die-photograph.

tor was determined to be about 200MHz, which is well beyond the frequencies of interest and thus has minimal impact on the measurement results presented later in the section. The availability of thick-oxide devices in our process allowed to operate the supply-noise monitor at 2.5V and measure the on-chip supply voltages directly. Alternate monitoring techniques based on sub-sampling can obviate the need for thick-oxide devices [30].

The PSNR analysis presented in Section 3.1 relies on linear response of the PLL to supply perturbations and hence, it is important to verify this assumption experimentally. The peak-to-peak jitter plotted as a function of supply-noise amplitude in Fig. 3.16 shows that the PLL response to supply noise is fairly linear for amplitudes of about 50mV. For higher amplitudes, the supply-noise induced jitter

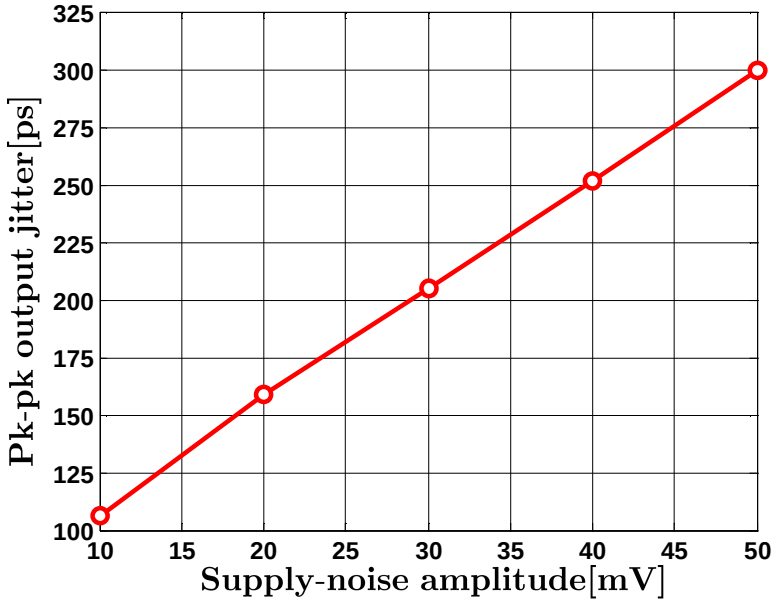

Figure 3.16: Measured peak-to-peak jitter of an unregulated PLL for various supply noise amplitudes.

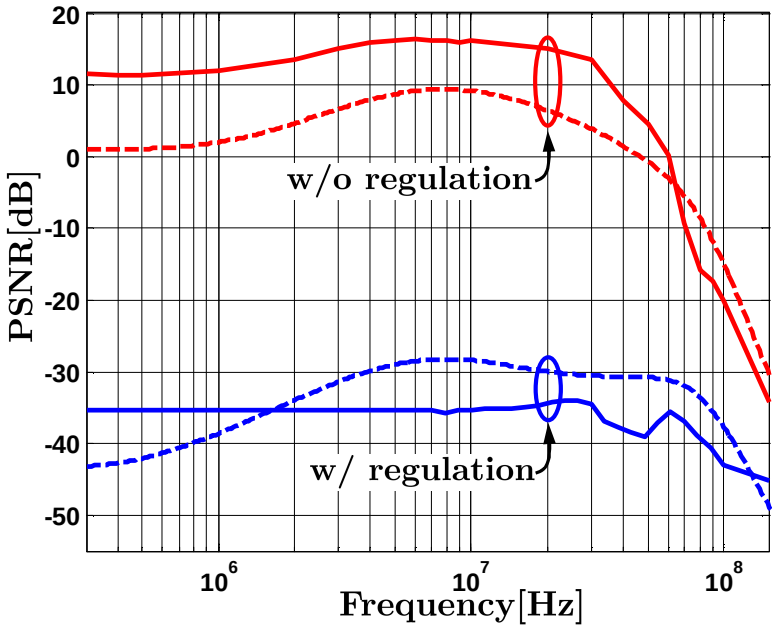

Figure 3.17: Measured and simulated PLL PSNR with noise on all the building blocks except VCO. Solid lines and dotted lines indicate measured and simulated PSNR curves, respectively.

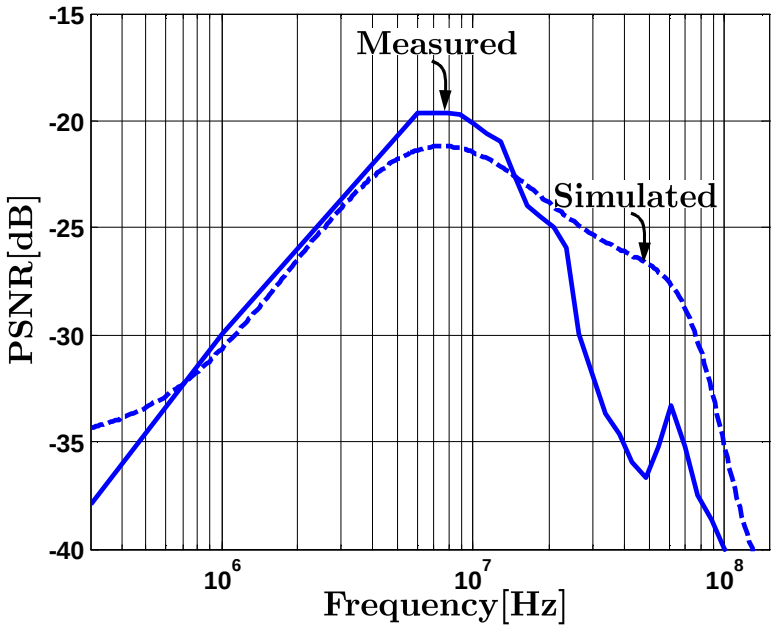

Figure 3.18: Measured and simulated overall PLL PSNR with noise on all the building blocks.

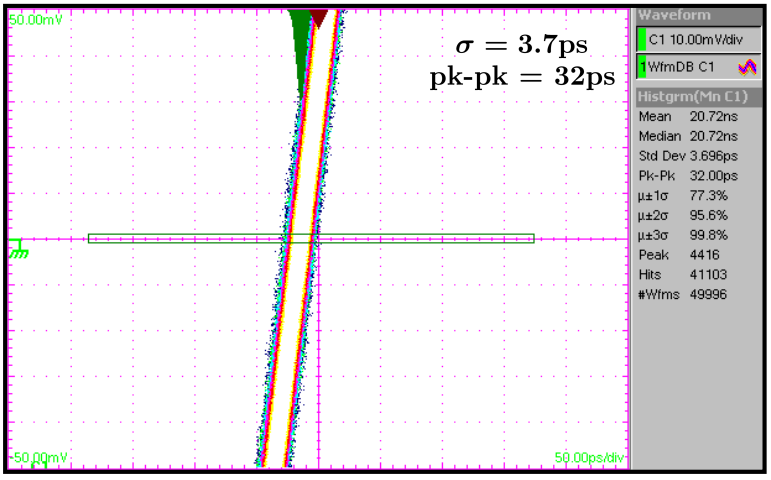

Figure 3.19: Output jitter without any supply noise.

approaches the time period of the PLL output and makes the response of the PLL progressively nonlinear. The measured PSNR curves shown in Fig. 3.17 illustrate an improvement of 50dB is achieved by the proposed regulation scheme for the

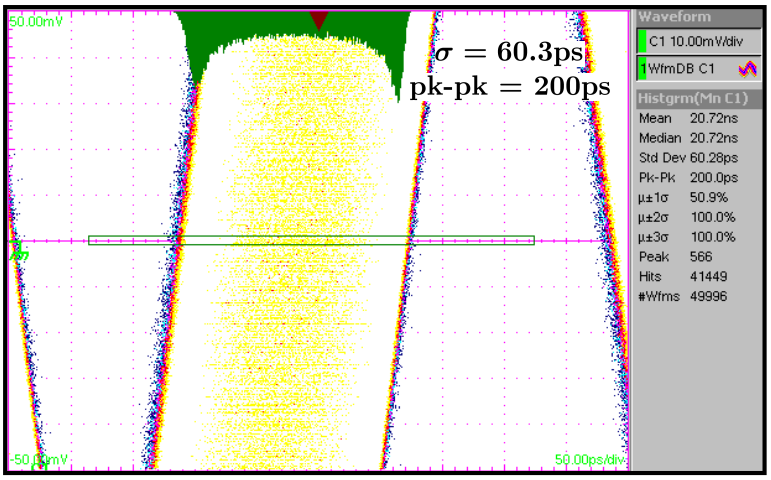

Figure 3.20: Unregulated PLL output jitter with a 20mV amplitude supply noise tone at 9MHz.

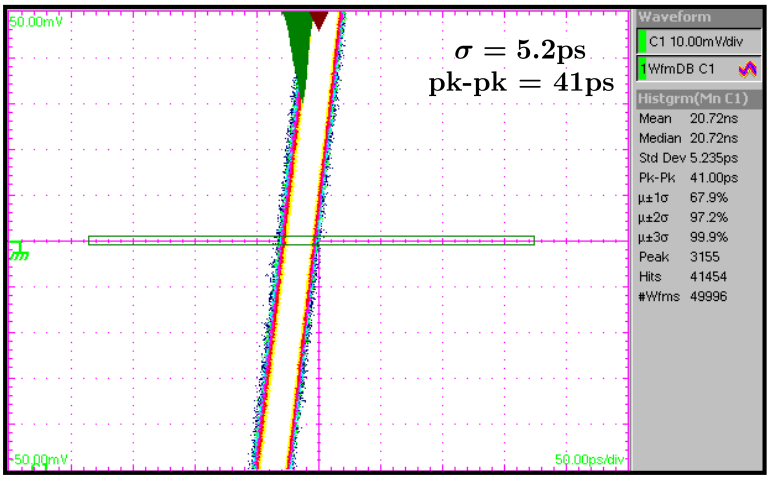

Figure 3.21: Supply-regulated PLL output jitter with a 100mV amplitude supply noise tone at 9MHz.

building blocks in the PLL. For both the regulated and the unregulated cases, no noise is injected into the VCO supply. The complete PSNR of the PLL obtained by injecting a 100mV sinusoidal noise into supplies of all the building blocks (including VCO) is shown in Fig. 3.18. A worst-case PSNR of about -20dB is achieved, which in time domain translates to an increase of 7ps in peak-to-peak jitter.

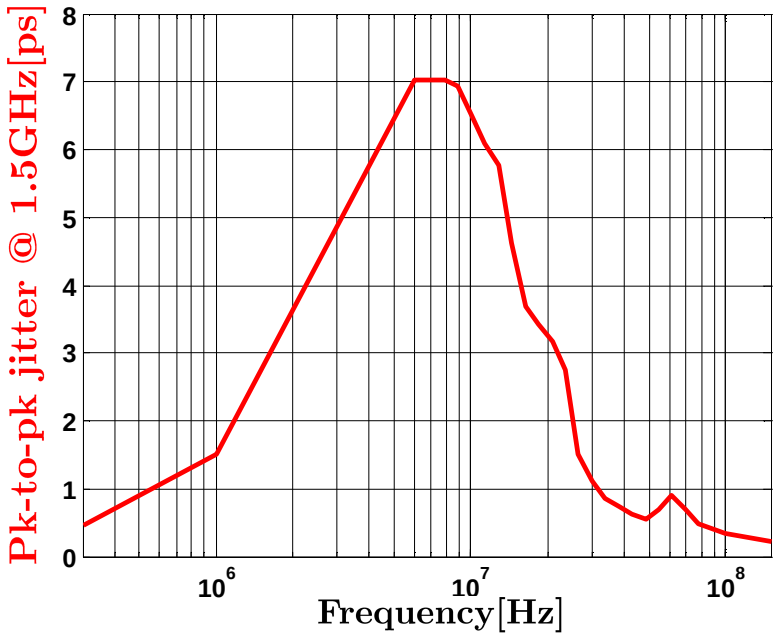

Figure 3.22: Measured peak-to-peak jitter at 1.5GHz with 100mV amplitude noise tone injected into the supply of all the building blocks.

In the absence of any external supply noise, as depicted in Fig. 3.19, the measured r.m.s and peak-to-peak output jitter of the prototype PLL operating at 1.5GHz are 3.7ps and 32ps, respectively. With a supply-noise tone of 20mV amplitude, the peak-to-peak output jitter for the unregulated case degrades to 200ps (see Fig. 3.20). With regulation, this jitter increases to about 41ps (see Fig. 3.21) even with a rather large supply-noise of 100mV amplitude. A complete profile of the jitter as a function of supply noise frequency is depicted in Fig. 3.22.

The power consumption of the PLL operating at 1.5GHz is 3.3mW of which 1.2mW is consumed in the VCO and only 540μW in the regulators. Placing the VCO regulator in the low-bandwidth coarse path allows to maximize the PLL bandwidth and achieve good jitter performance with such low power consumption. In other words, because the regulator power dissipation is independent of the PLL

Table 3.2: Performance Summary

Technology	0.18μm CMOS
Supply voltage	1.8V
Operating frequency	0.8-3.0GHz
Jitter(r.m.s/pk-pk) @ 1.5GHz	3.7ps/33ps (no noise)
	60ps/200ps (20mV noise, w/o reg)
	5.2ps/41ps (100mV noise, w/ reg)
Power consumption @ 1.5GHz	VCO: 1.2mW
	Regulators : 0.54mW
	Total : 3.3mW
Active die area	Regulators: 0.15mm^2
	Total: 0.18mm^2

bandwidth, the supply rejection and intrinsic noise-induced jitter performance can be optimized independently. A detailed measured performance summary of the prototype PLL is presented in Table 3.2.

3.5 Summary

In this Chapter, a comprehensive design-oriented analysis of the impact of supply noise in all the building blocks of the PLL has been presented. The key conclusions of the analysis are:

1. Asymmetric coupling of the supply noise in the UP and DN current paths due to finite output impedance of the current sources introduces current mismatch in the charge pump. Such a supply-noise induced current mismatch

manifests itself as jitter at the PLL output.

2. Digital circuits such as clock buffers and the feedback divider are extremely sensitive to supply noise as their delay is a strong function of the supply voltage.

3. Owing to the symmetric nature of its UP and DN paths, a conventional 3-state PFD exhibits reasonably good intrinsic supply-noise immunity. Any residual leakage of the supply noise to the PLL output is largely due to the modulation of the PFD reset time by the supply noise.

Based on the analytical results, robust mitigation techniques that combine a split-tuned PLL architecture with novel circuit techniques are developed and are shown to greatly improve the PLL supply-noise immunity with minimal power penalty. The employed PLL architecture allows efficient use of low bandwidth large supply noise rejection replica-biased regulator in the VCO. Output pole dominant regulators use the virtual VCO supply voltage as the reference and generate the regulated supply voltage to all the other building blocks of the PLL. This approach obviates voltage references that have good supply rejection. Measured results obtained from a test chip show the effectiveness of the proposed architecture in mitigating supply noise. Operating at 1.5GHz, the prototype PLL achieves a worst-case overall PSNR of -22dB while consuming only 3.3mW of power from a 1.8V supply. In time domain, the achieved PSNR translates to about 7ps of peak-to-peak jitter degradation with a 100mV amplitude sinusoidal tone at the worst-case noise frequency.

CHAPTER 4. INTERMODULATION EFFECTS DUE TO NOISE ON CHARGE PUMP SUPPLY

In Chapter 3, the effect of noise on charge pump supply on the jitter performance of the PLL was studied. A PLL can be considered as a linear time-invariant (LTI) system in order to design it for a target application. Small signal analysis of a PLL is carried out in order to evaluate the supply noise sensitivity of the PLL to various building blocks [6, 12] as the PLL is approximately linear in phase domain. The small signal block diagram of a PLL with the VCO phase noise indicated is shown in Fig. 4.1. The VCO phase noise gets *added* to the PLL at the output and

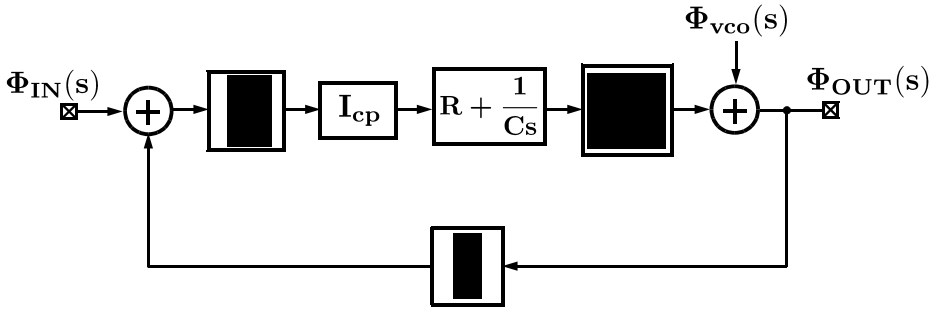

Figure 4.1: Small-signal block diagram of a charge-pump PLL.

using the small signal analysis, it can be shown, as is well known, that the phase noise gets highpass shaped with the transfer function given by

$$\frac{\Phi_{OUT}(s)}{\Phi_{VCO}(s)} = \frac{1}{1 + LG(s)} \tag{4.1}$$

where

$$LG(s) = \frac{I_{cp}K_{vco}(1 + RCs)}{2\pi Cs^2} \tag{4.2}$$

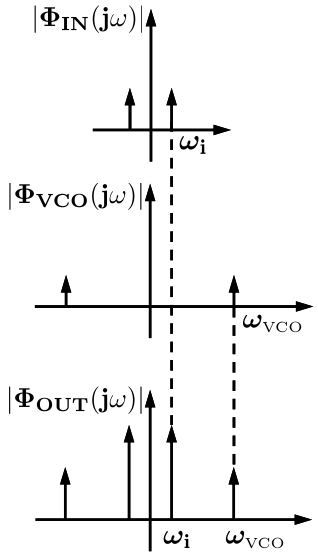

Figure 4.2: Spectra of input and output phases of a PLL.

Hence if the spectrum of the PLL input phase and the VCO phase have tones at ω_i and ω_{VCO}, then the output will contain tones at those frequencies as shown in Fig. 4.2. Similarly all the building blocks of the PLL add noise to the PLL loop with the exception of the charge pump which affects the performance of the PLL in a different way. As an example, a simulation was carried out where the input phase had a tone at 1MHz while the charge pump had a tone of frequency 4MHz, and the spectrum of the output phase is shown in Fig. 4.3. It can be seen that, the output has tones at 1MHz as well as at 3MHz, 5MHz, 7Mhz and 9Mhz. The charge pump in a PLL is a gain block and presence of noise in the charge pump current results in the modulation of the PLL loop-gain resulting in a linear time-variant (LTV) system. Figure 4.4 shows the block diagram of a PLL where the charge pump current has been labelled as $I_{cp}(s)$ to indicate that the charge pump current is not a constant but time varying. If, in the presence of noise on charge pump supply, the input phase has a tone, then the output phase will have a tone

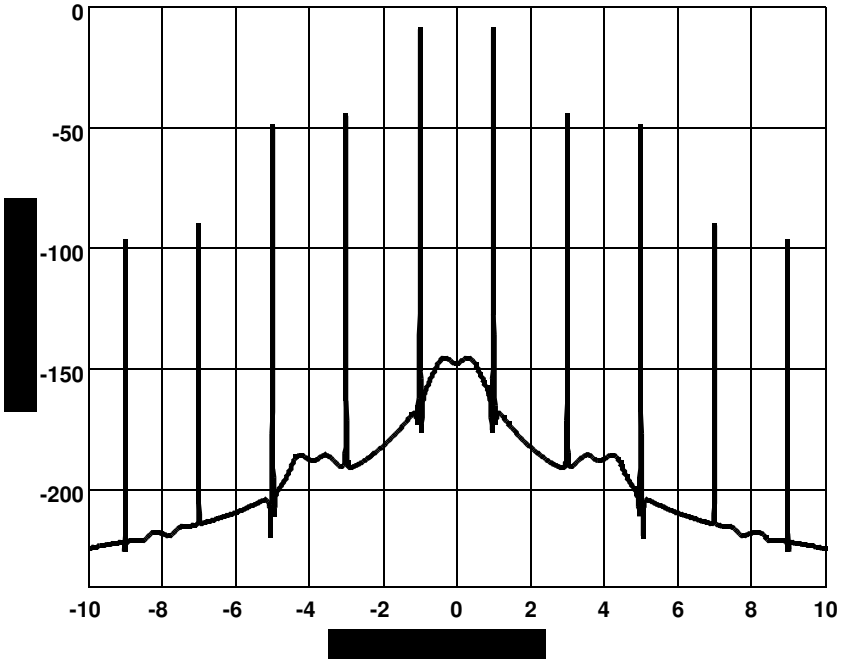

Figure 4.3: Spectrum of PLL output phase in the presence of noise on charge pump current.

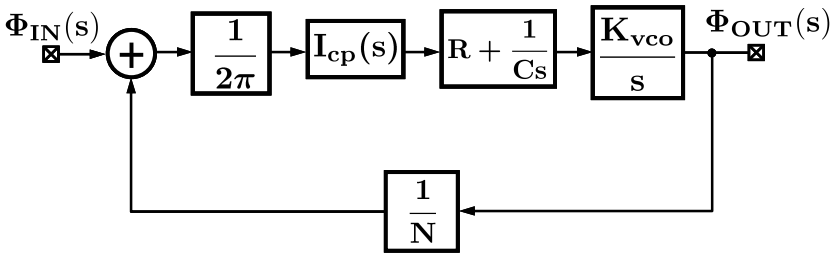

Figure 4.4: Block diagram of a PLL with time varying charge pump current.

corresponding to that at the input as well as higher order harmonics. This effect is due to the fact that the PLL is a LTV system in the presence of noise on charge pump supply. Analysis of the effect of noise on charge pump supply therefore requires us to analyse the PLL as a LTV system. As pointed out in [23], analysis of negative feedback LTV systems can be quite involved and derivation of accurate closed form expressions may not be possible. In this Chapter, an attempt has been made to analyze a second order negative feedback system whose structure is very similar to that of a charge pump PLL and whose loop is modulated by a secondary signal which represents the modulation of the PLL loop by noise in charge pump supply. Certain simplifying assumptions makes the analysis easier and simulation results that are provided later agree with the proposed analysis quite closely.

4.1 Description of the Problem

Without loss of generality, we can reduce the system shown in Fig. 4.4 to that shown in Fig. 4.5. The equivalence holds good as we can identify the parameters in Fig. 4.5 using the ones in Fig. 4.4. Mathematically,

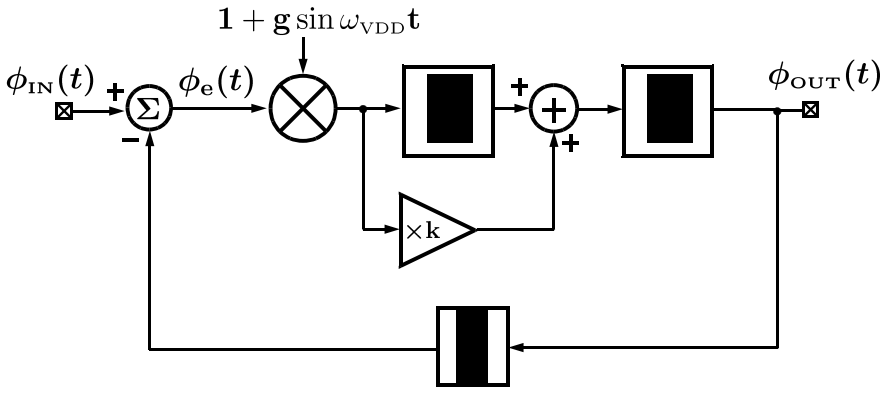

Figure 4.5: Block diagram of a second order PLL with noise on Charge-Pump current.

$$\frac{\omega_o}{Ns}\left(k+\frac{\omega_o}{s}\right) \longrightarrow \frac{I_{cp}}{2\pi}\left(R+\frac{1}{Cs}\right)\frac{K_{vco}}{Ns} \tag{4.3}$$

where the effect of the modulation of the loop gain is assumed to be absent. The second order LTI has a damping factor of 0.75 for N = 4 and k = 3. In this work, we will demostrate the intermodulation effects of the LTV system for N = 4 and k = 3. We can model the effect of noise on charge pump supply as modulation of the error signal $\phi_{\mathrm{e}}(\mathrm{t})$ by the term $1+\mathrm{g}\sin\omega_{\mathrm{VDD}}$ where g represents the fractional change in the charge pump current due to noise on the supply and ω_{VDD} is the frequency of the supply noise expressed in rad/s. As discussed before, if the input is a tone at ω_{i}, we can expect a tone at the output at ω_{i} and additional tones at $\mathrm{k}\omega_{\mathrm{VDD}} \pm \omega_{\mathrm{i}}$. In many applications (for example data communication using fractional-N frequency synthesizers), the phase of the PLL carries information. The presence of noise on charge-pump supply will corrupt the information. In order to minimize this effect, it is necessary to understand the effect of noise on charge-pump supply. As has been pointed out earlier, analysis of negative feedback LTV systems is highly involved and obtaining closed form expressions for the output in terms of input and the supply noise signals through rigorous analysis is very hard. In this work, we will derive the relevant equations for a second order system. We will derive closed form expressions for the output, making certain simplifying assumptions, and then, we will present guidelines to minimize the effect of noise on charge pump supply.

4.2 Analysis of the LTV System

Consider the second order PLL whose block diagram is shown in Fig. 4.5. The difference of the input phase and the divided output phase gets modulated and filtered by the forward path of the system. In the absence of supply noise, the s domain equations governing the input-output relationship is given by

$$\Phi_{OUT}(s) = LG(s)\Phi_e(s) \tag{4.4}$$

$$\Phi e(s) = \Phi_{IN}(s) - \frac{\Phi_{OUT}(s)}{N} \tag{4.5}$$

where

$$LG(s) = \frac{3\omega_o\left(s + \frac{\omega_o}{3}\right)}{s^2}, \tag{4.6}$$

where the proportional gain k in Fig. 4.5 has been assumed to be 3. In the presence of supply noise, additional terms will appear due to the modulation of the phase error $\phi_{\mathrm{e}}(\mathrm{t})$ by noise on charge pump supply. The relationship between $\Phi_{\mathrm{OUT}}(\mathrm{s})$ and $\Phi_{\mathrm{e}}(\mathrm{s})$ changes to

$$\Phi_{OUT}(s) = \Phi_e(s) + a\left(\Phi_e(s - j\omega_{VDD}) - \Phi_e(s + j\omega_{VDD})\right) \tag{4.7}$$

where $\mathrm{a} = \mathrm{g}/(2\mathrm{j})$. The modulation of the error signal due to the presence of noise on charge pump supply results in tones at the output of the PLL. For a given phase input $\Phi_{\mathrm{IN}}(\mathrm{s})$, the output will consist of terms of the form $\mathrm{H_k(s)}\Phi_{\mathrm{IN}}(\mathrm{s} + \mathrm{jk}\omega_{\mathrm{VDD}})$ for $\mathrm{k} = 0, \pm 1, \pm 2, \ldots$. The transfer functions $\mathrm{H_k(s)}$ are known as harmonic transfer functions (HTFs) [23] and they represent the magnitude of tones at frequencies $\omega_{\mathrm{i}} + \mathrm{k}\omega_{\mathrm{VDD}}$. Eliminating $\Phi_{\mathrm{e}}(\mathrm{s})$, the input-output relationship can be derived to

$$\{1 + LG(s)\}\,\Phi_{OUT}(s) + aLG(s)\,\{\Phi_{OUT}\,(s - j\omega_{VDD}) - \Phi_{OUT}\,(s + j\omega_{VDD})\}$$
$$= NLG(s)\,[\Phi_{IN}(s) + a\,\{\Phi_{IN}\,(s - j\omega_{VDD}) - \Phi_{IN}\,(s + j\omega_{VDD})\}]\,. \quad (4.8)$$

be the one given in Eq. 4.8. By substituting s by $s + jk\omega_{VDD}$ for integer values of k, recurring equations can be derived to obtain relationships between various harmonics of the input and output. Finally, the HTFs can be numerically obtained by truncating the number of harmonics to a finite value. For the system shown in Fig. 4.5, the HTFs were derived numerically with N = 4, ω_{VDD} = 4MHz and ω_o = 1MHz while truncating number of harmonics to 21. Figure 4.6 shows the magnitude of $H_1(s)$ plotted using the above method, Spectre PAC analysis and by plotting the FFT of the output signal in the transient analysis. It can be seen that the three curves match very closely validating our approach. An important observation to be made is that the transfer function of input to the fundamental component of the output (i.e. $H_0(s)$) is found to be unaffected by the modulation by charge pump current (as shown in Figure 4.7) when the fractional change in the charge pump current g = 0.1. Hence, it can be approximated to be

$$H_0(s) = \frac{NLG(s)}{1 + LG(s)}. \quad (4.9)$$

In the next section, we will present the simulation results of the higher HTFs and we will also provide intuition into the shapes of the HTFs.

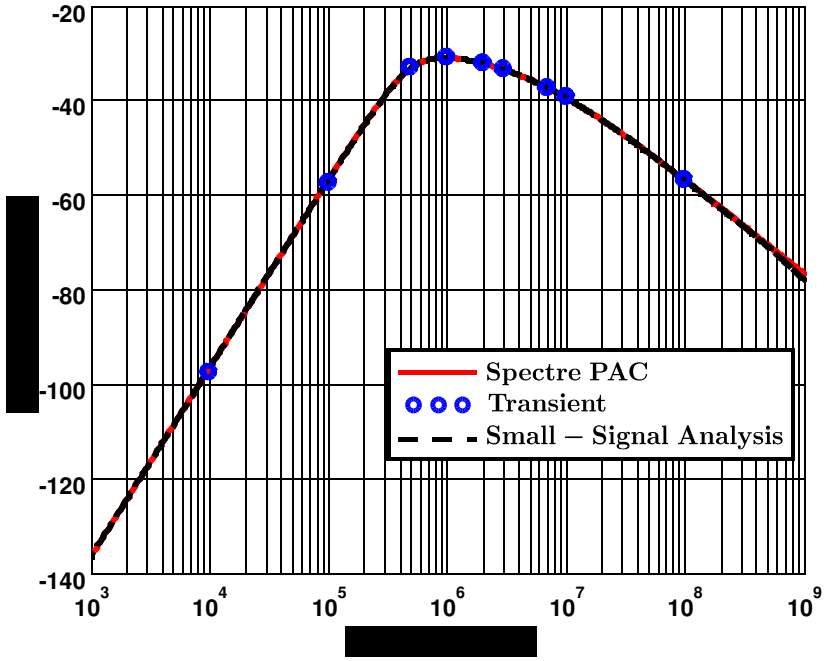

Figure 4.6: Plot of $|H_1(j\omega)|$.

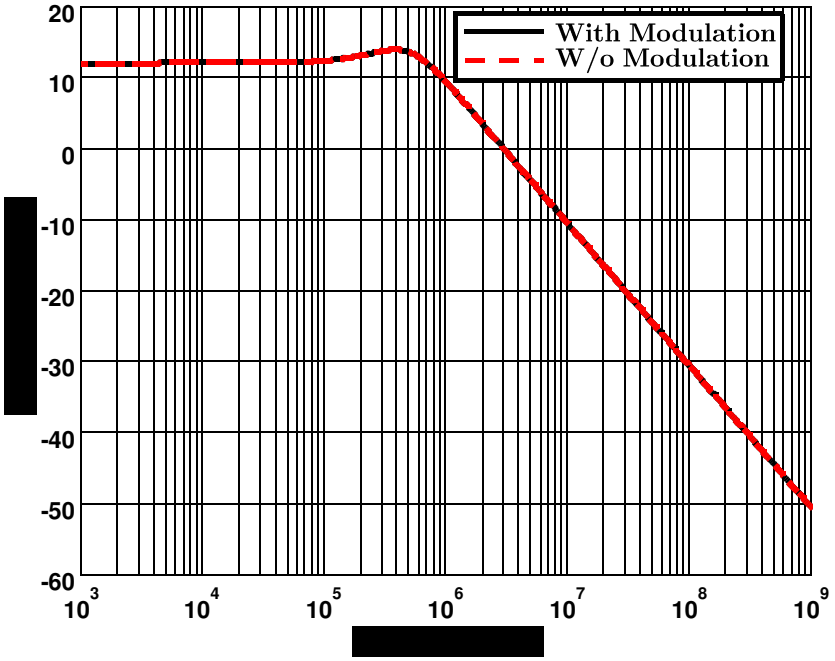

Figure 4.7: Plot of $|H_0(j\omega)|$.

$$\Phi_{mod,e}\left(j\left(\omega_{VDD}-\omega_i\right)\right)=\Phi_e\left(j\left(\omega_{VDD}-\omega_i\right)\right)+a\left\{\Phi_e\left(j\omega_i\right)-\Phi_e\left(j\left(2\omega_{VDD}-\omega_i\right)\right)\right\}. \tag{4.10}$$

4.3 Harmonic Transfer Functions: Intuition and Simulation Results

In order to gain insight into the shape of the HTFs, we will have to derive the approximate closed form expressions for the HTFs. We will make the assumption that the input to output transfer function is unaffected by the modulation due to charge pump current (which is also apparent from the plots shown in Fig. 4.7). In this discussion, we will look at $H_1(s)$ and $H_{-1}(s)$ as the behaviour of the higher HTFs is similar and can be easily deduced using the techniques that will be discussed below. The presence of harmonics is mainly due to the modulation of the phase error $\phi_e(t)$ by the charge pump noise. The phase error, after modulation, will have a spectrum given by $\Phi_e(s)+g\left\{\Phi_e\left(s-j\omega_{VDD}\right)-\Phi_e\left(s+j\omega_{VDD}\right)\right\}$. The modulated phase error $\Phi_{mod,e}(s)$ will have a tone at $\omega_{VDD}-\omega_i$ which is given by Eq. 4.10, where we have assumed that $\Phi_e\left(j\omega_i\right)=\Phi_e\left(-j\omega_i\right)$.

The mechanism of the phase modulation can be better understood by looking at the spectrum of various signals shown in Fig. 4.8 (the various tones here are not drawn to scale). Note that the input phase $\Phi_{IN}(s)$ has tones only at $\pm\omega_i$. Therefore, the tone in the phase error $\Phi_e(s)$ at $j\left(\omega_{VDD}-\omega_i\right)$ will be equal to $-\Phi_{OUT}\left(j\left(\omega_{VDD}-\omega_i\right)\right)$. As the higher harmonics have lower strength when compared to the lower ones, we can neglect the $\Phi_e\left(j\left(2\omega_{VDD}-\omega_i\right)\right)$ term in Eq. 4.10 to

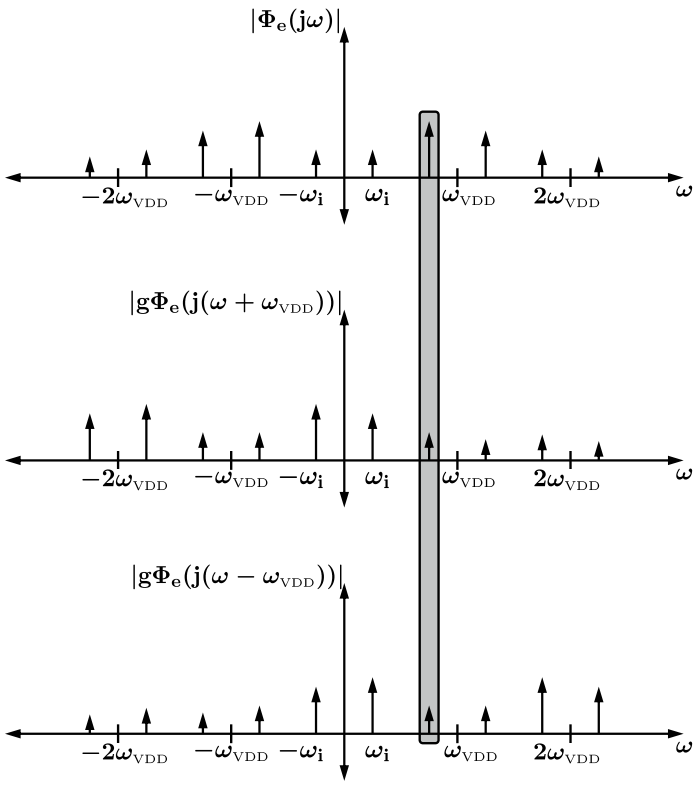

Figure 4.8: Spectrum of various components of modulated phase error $\phi_e(t)$.

obtain the approximation to $H_{-1}(s)$ as

$$H_{-1}(s) \approxeq \frac{NLG(s - j\omega_{VDD})}{1 + LG(s - j\omega_{VDD})} \frac{a}{1 + LG(s)}. \tag{4.11}$$

Similarly the expression for $H_1(s)$ can be derived as

$$H_1(s) \approxeq \frac{NLG(s + j\omega_{VDD})}{1 + LG(s + j\omega_{VDD})} \frac{a}{1 + LG(s)}. \tag{4.12}$$

Note that these are single side-band transfer functions and hence, are complex. Figure 4.9 shows the plots for $H_{-1}(s)$ obtained using the approximate expression and using the small signal model assuming $\omega_{VDD} = 2\pi \times 4$Mrad/s. The approximation is seen to match the transfer function very closely. Let us consider $H_1(s)$ first. The ex-

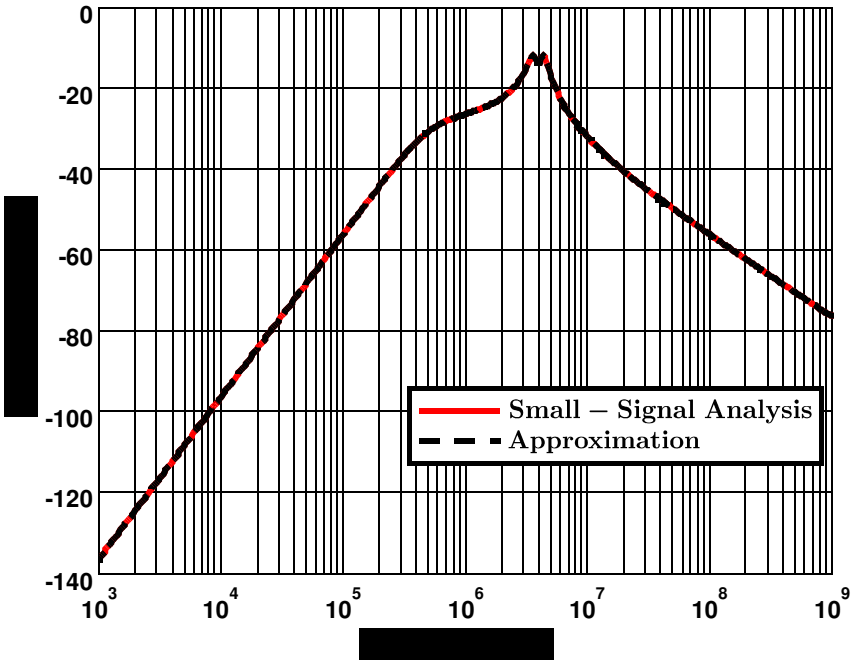

Figure 4.9: Plot of $|H_{-1}(j\omega)|$ using the approximation and using the small-signal model.

pression for $H_1(s)$ has two parts to it. The term $NLG(s+j\omega_{VDD})/(1+LG(s+j\omega_{VDD}))$ is nothing but the input to output transfer function with the frequency transformation of s to $s + j\omega_{VDD}$. The second term is the highpass transfer function scaled

by the factor a = g/2j. If the fundamental component is absent in the $\Phi_e(j\omega)$, then modulation of the phase error will not have any term corresponding to the harmonic at $\omega_i + \omega_{VDD}$. The output corresponding to the harmonic at $\omega + \omega_{VDD}$ is the magnitude of the fundamental in $\Phi_e(j\omega)$ times the magnitude of input to output transfer function at frequency $\omega + \omega_{VDD}$ with a scaling factor of a. A plot of $NLG(s + j\omega_{VDD})/(1 + LG(s + j\omega_{VDD}))$ for various values of ω_{VDD} is shown in Fig. 4.10. A plot of $a/(1 + LG(j\omega))$ is also included in the same Figure. We know from elementary frequency transformation that the DC gain decreases with increasing ω_{VDD} while the bandwidth progressively increases and this can be observed in Fig. 4.10 as well. The highpass transfer function $a/(1+LG(s))$ reaches its

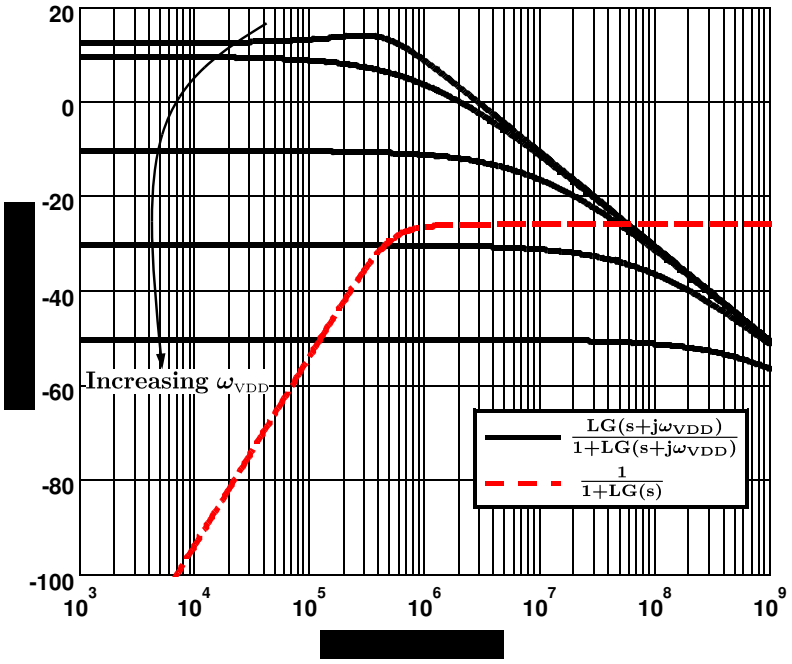

Figure 4.10: Plot of the two parts of $|H_1(j\omega)|$.

maximum at around the UGB of the feedback system. Hence the overall transfer function $H_1(s)$ reaches the maximum value at around the UGB of the loop and the

peak value can be approximated to be

$$|H_1(j\omega)|_{max} = 20\log\frac{Na\omega_{UGB}}{\omega_{UGB}+\omega_{VDD}} \tag{4.13}$$

where ω_{UGB} is the UGB of the loop. The plots in Fig. 4.11 reflects the observations made above. Most importantly, the effect of supply noise is most detrimental for

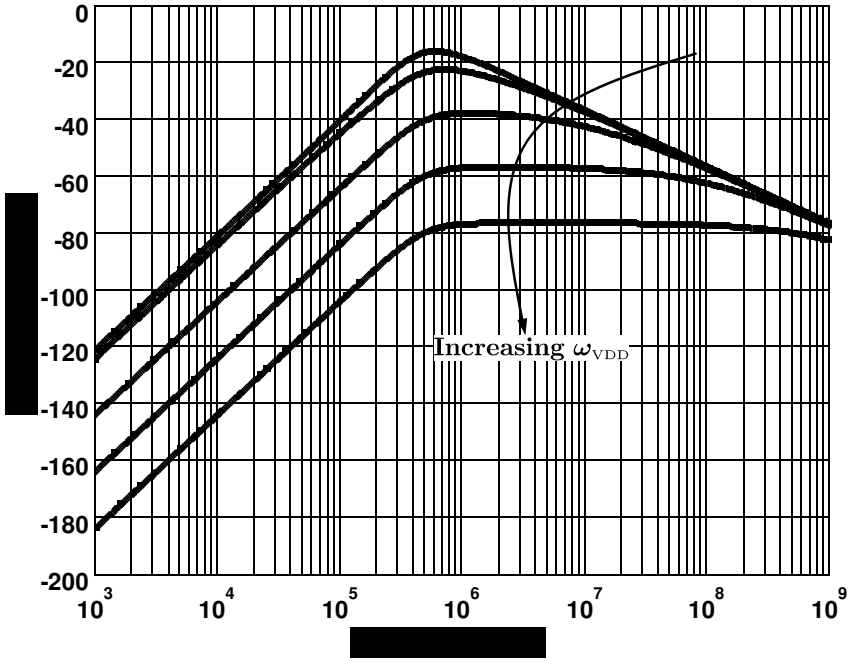

Figure 4.11: Plot of $|\mathrm{H_1(j\omega)}|$ for increasing values of ω_{VDD}.

low frequencies and the worst case value of $|\mathrm{H_1(j\omega)}|$ occurs roughly at the UGB of the loop. Unlike $|\mathrm{H_1(j\omega)}|$, $|\mathrm{H_{-1}(j\omega)}|$ has its worst case value at around ω_{VDD} if ω_{VDD} lies well beyond the UGB of the loop. Figure 4.12 shows the two parts of $|\mathrm{H_{-1}(j\omega)}|$. The value of $|\mathrm{a}/(1+\mathrm{LG(j\omega)})|$ reaches its maximum value of $|\mathrm{a}|$ beyond the UGB of the loop. Since this component of $|\mathrm{H_{-1}(j\omega)}|$ peaks at ω_{VDD}, the overall transfer function peaks at ω_{VDD} and its value is equal to $20\log\mathrm{Na}$ which is independent of ω_{VDD} and ω_{UGB}. The overall transfer function is plotted for progressively increasing values of ω_{VDD} in Fig. 4.13. The peak value is seen to

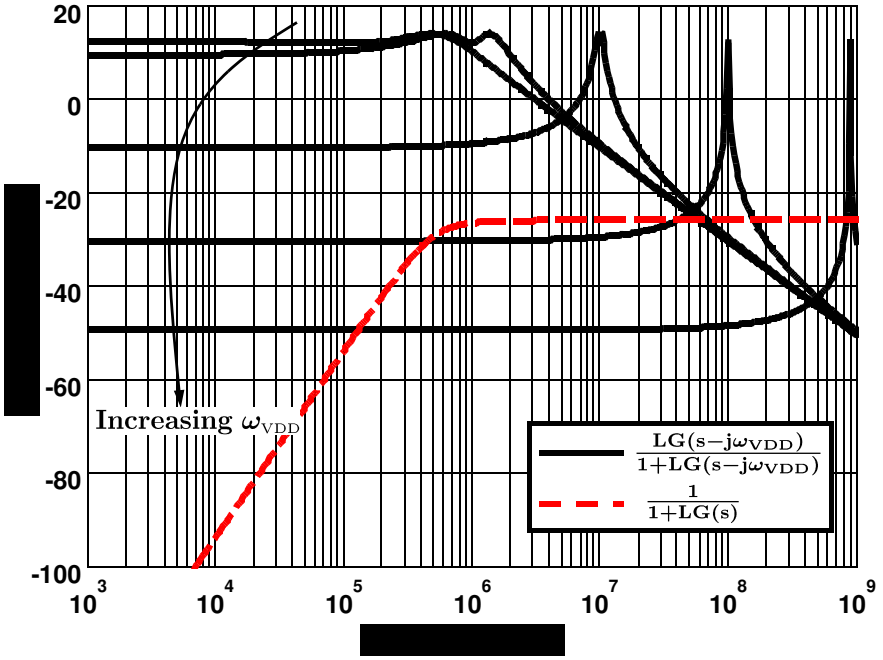

Figure 4.12: Plot of the two parts of $|H_{-1}(j\omega)|$.

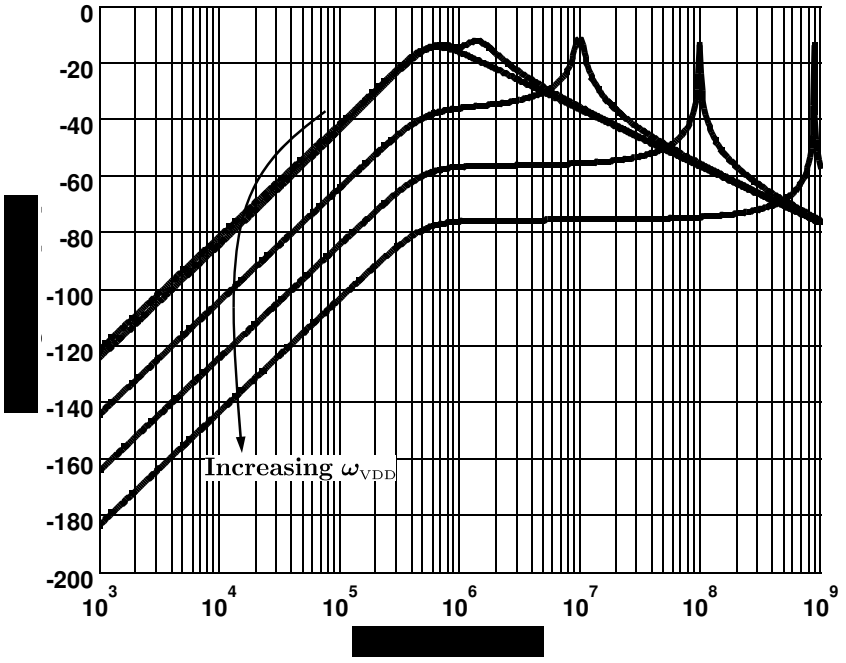

Figure 4.13: Plot of $|H_{-1}(j\omega)|$ for increasing values of ω_{VDD}.

be constant and equal to $20\log \mathrm{Na}$ unlike the case with $|\mathrm{H}_1(\mathrm{j}\omega)|$ where the peak value decreases with increase in ω_{VDD}. Intuitively, the phase error $\Phi_{\mathrm{e}}(\mathrm{s})$, will have a gain of unity for noise on the input phase $\Phi_{\mathrm{IN}}(\mathrm{s})$ at frequencies near ω_{VDD}. This will then be modulated by the noise on charge pump current $1 + \mathrm{g}\sin\omega_{\mathrm{VDD}}\mathrm{t}$ which will introduce harmonics near the zero frequency. If the input noise frequency is very close to ω_{VDD}, then the harmonic in the baseband frequency will appear at the output with a gain of N as it lies well within the PLL bandwidth. This statement holds good even if ω_{VDD} is much less than the UGB. The only difference is that for very low values of ω_{VDDD}, the transfer function reaches the peak value near the PLL UGB. Hence any correlation between the noise on the input phase and the charge pump current will show up in the output even if the band of noise frequency falls well beyond the UGB of the loop. The only way to mitigate the effect of noise is to reduce the value of the parameter a which can be accomplished by having a good regulator on the charge pump supply as well as by designing the charge pump circuit to minimize the effect of noise on its supply as discussed in Chapter 3.

4.4 Summary

In this Chapter, analysis of a second order LTV system, to model the intermodulation effects of the noise on charge pump supply in a PLL, has been presented. The analysis shows that the primary positive sideband HTF ($\mathrm{H}_1(\mathrm{j}\omega)$) peaks roughly at the UGB of the PLL. The value of the peak decreases progressively with increasing supply noise frequency indicating that the in-band noise (noise within PLL UGB) is more problematic than the out of band noise. The primary negative sideband HTF ($\mathrm{H}_{-1}(\mathrm{j}\omega)$) peaks at the supply noise frequency for

supply noise frequencies higher than the PLL UGB. The peak value remains as a constant (equal to $20\log|\mathrm{Na}|$) and it occurs at the supply noise frequency ω_{VDD} which indicates that the PLL loop does not offer any filtering on the harmonics if a noise component on the supply exists whose frequency, ω_{VDD} lies very close to the input frequency, ω_{i}. Therefore, in applications where the input phase carries certain information, it is necessary to maintain the charge pump current to be constant as any noise on the charge pump current will essentially corrupt the output phase of the PLL.

CHAPTER 5. A SUPPLY NOISE INSENSITIVE CDR WITH ON-CHIP JITTER TOLERANCE MEASUREMENT

So far, analysis of the effect of supply noise on the jitter performance of PLLs as well as techniques to mitigate supply noise have been presented. As discussed in Chapter 1, clock and data recovery circuits are used to retime digital data and recover clock signal from the data stream. The phase averaging CDR architecture [9] which is commonly used in low voltage applications utilizes a PLL inside the CDR loop. Oversampling is used in this architecture [10] in order to reduce the power consumption in the PLL. Since the PLL uses a ring-VCO, the effect of supply noise on the bit-error rate (BER) of the CDR is an important design consideration. In this Chapter, we present techniques to further reduce power consumption of the phase averaging CDR proposed in [9, 10], achieve low BER introduced by VCO supply noise and incorporate on-chip jitter tolerance measurement in the CDR.

5.1 Problem Description

The simplified block diagram of the phase averaging CDR is shown in Fig. 5.1. It consists of a PLL loop embedded in a CDR loop. The reference frequency to the PLL is such that the PLL output frequency is nominally equal to the data rate. The CDR loop corrects for any mismatch in the frequencies.

The PLL generates eight phases in this quarter rate CDR and that is used by

the bang-bang phase detector (BBPD) to slice the data. The output of the BBPD is then filtered by the DLF and the $\Delta\Sigma$ modulator re-quantizes the DLF output to a two bit signal. The phase rotator accumulates this over a modulus of eight. The output of the phase rotator controls a multiplexer which selects one out of the eight phases of the VCO. This CDR has good jitter performance as the PLL loop filters the phase steps of the phase rotator. The DSM further reduces the jitter by reducing the effective phase jumps in at the phase rotator output. This CDR architecture achieves lower power in multiphase CDRs as compared to the previous architectures. The effect of supply noise on the BER can be minimized by using the proposed supply regulation scheme for the PLL portion of the CDR.

In-spite of being a low-power architecture, there is still some room for improvement (refer to Fig. 5.2). In this example of a quarter rate CDR, there are eight VCO phases which need to be routed to the samplers of the BBPD as well as the multiplexers. Even though the VCO output frequency is four times lower, the routing of eight phases still consumes power as it is necessary to maintain the right phase relationship between all the eight phases. The multiplexer has eight inputs and this also results in increase in power consumption. The digital loop filter has flip flops to provide delay for the accumulators. These flip flops consume a lot of power inspite of operating at one-eigth of the VCO output frequency.

5.2 Proposed Solution

Using a full rate architecture greatly simplifies the layout as only two lines have to be routed to the samplers. As shown in Fig. 5.3, a four-phase divider is used to generate four phases at half the VCO frequency using the two output phases of the VCO. The phase rotator output can now be used to select one of

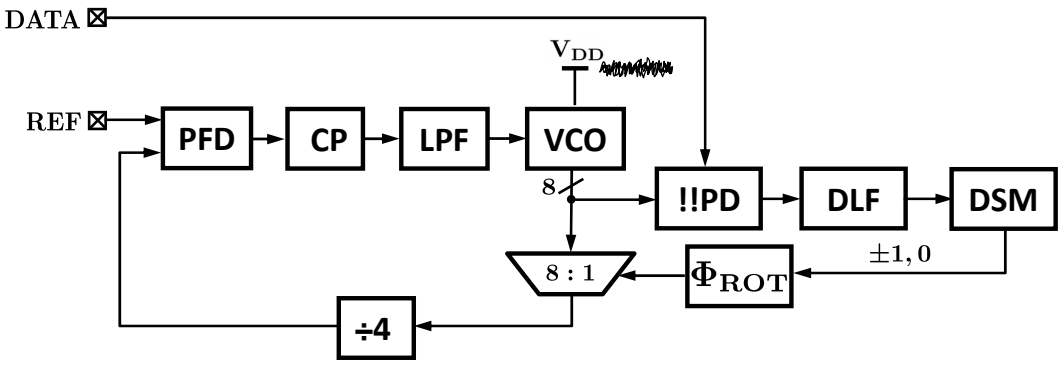

Figure 5.1: Simplified block diagram of a phase averaging CDR.

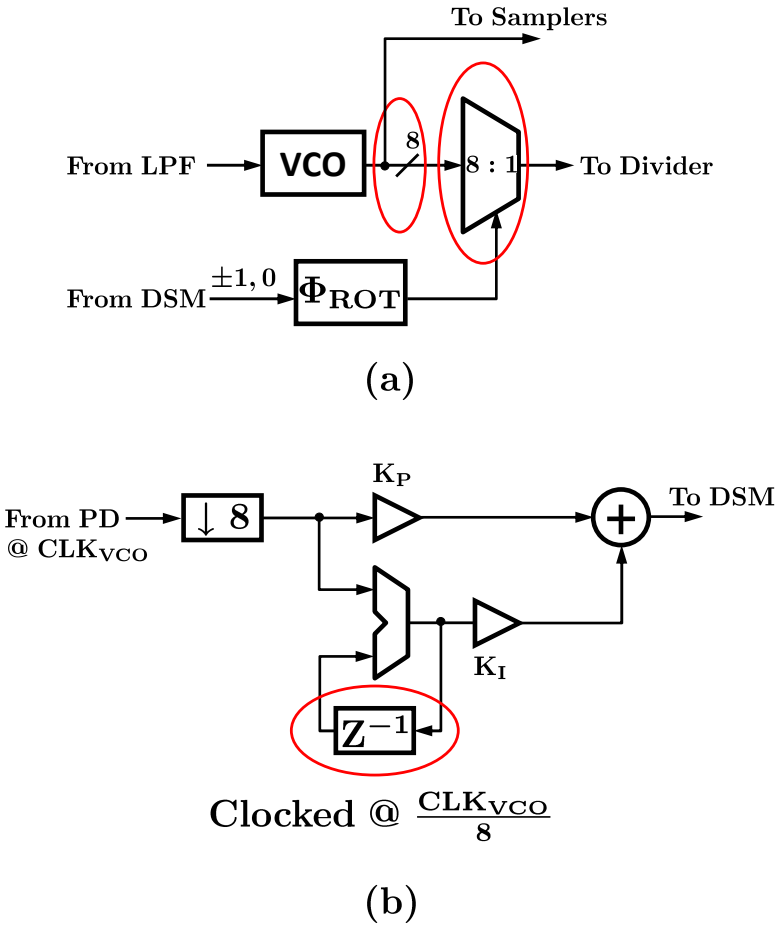

Figure 5.2: Power consuming blocks of a phase averaging CDR.

the four phases. The accumulator can be made to operate at a lower clock by

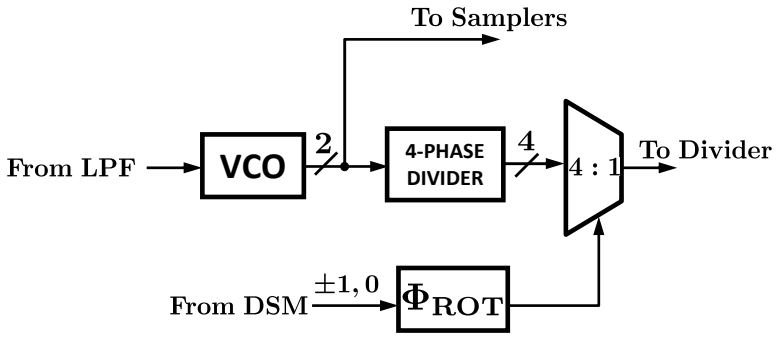

Figure 5.3: Phase interpolator block diagram.

further decimating the output of the BBPD as shown in Fig. 5.4. This will result in reduction of power consumption with minimal impact on jitter performance.

Apart from good PSNR and power efficiency, on-chip jitter tolerance is another feature which is added to this design. In the next Section, the jitter tolerance metric of a CDR will be defined first after which, the proposed on-chip jitter tolerance measurement scheme will be presented.

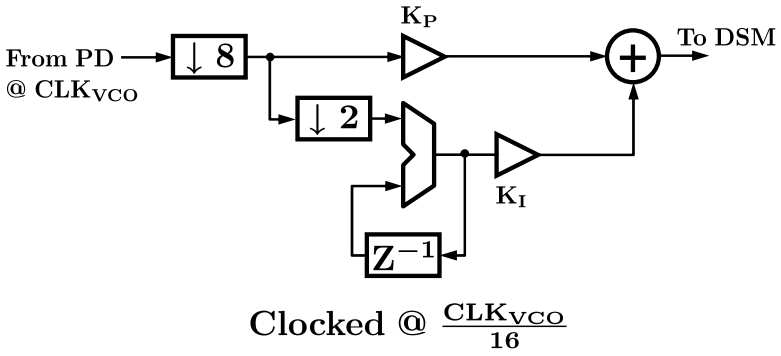

Figure 5.4: Digital loop filter block diagram.

5.3 On-chip Jitter Tolerance Measurement

A simple small-signal model of the CDR is shown in Fig. 5.5. Ideally, the output clock is supposed to track the jitter on the input data. That way, the sampler that uses the clock to retime the data doesn't make bit errors. A metric defined to quantify the ability of a CDR to track jitter on the input data is called jitter tolerance. For a sinusoidal input phase as shown in Fig. 5.6, the output clock phase will be sinusoidal as well. The amplitude of the input jitter in Unit Intervals for which, the BER is less than a target BER is defined as the jitter tolerance of the CDR. Figure 5.7 shows a jitter tolerance curve for a BER of 10^{-12}. Typically, each application has a *jitter tolerance mask* to be satisfied by the CDR as shown in the Fig. 5.7.

To test for the jitter tolerance of the CDR, the input data is modulated to have some jitter and BER is measured. The same BER can be obtained by introducing the disturbance at other points in the CDR loop as indicated in Fig. 5.5. The only restriction is to inject a known excitation at another point in the CDR loop which will cause the same change (in small-signal sense) in the output of the BBPD as it would when the phase of the data is modulated. Off-chip jitter tolerance measurement requires use of expensive equipment while on-chip jitter tolerance measurement obviates expensive equipment. In the current design, jitter is introduced at the digital loop filter output. Figure 5.8 shows the way in which the digital loop filter output is added to the output of a digital sine-wave generator (DSG). The DSG generates a sinusoid which has five levels between the extreme values, in its digital output code, of A and -A. It can be shown that the digital sinusoid has no third and fifth harmonics if generated this way.

The hardware implementation of DSG will consist of a look-up table and a

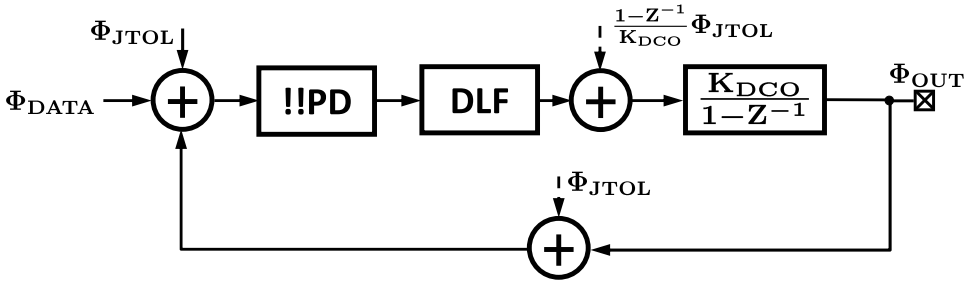

Figure 5.5: Small-signal block diagram of a digital CDR.

multiplexer which reads the values from the look-up table at each clock edge. The complete block diagram of the CDR is shown in Fig. 5.9. Table 5.1 shows the summary of target performance of this CDR and the layout of the designed CDR is shown in Fig. 5.10. The design has been carried out in a 90nm CMOS process and the CDR is designed to be tuned from 0.5 to 5 Gbps. The target BER is 10^{-12} while consuming a power of 10mW and occupying an area of $800\mu\text{m} \times 1\text{mm}$. The target jitter is 20ps pk-pk due to VCO phase noise and the target for the worst case PSNR of the PLL is -28dB.

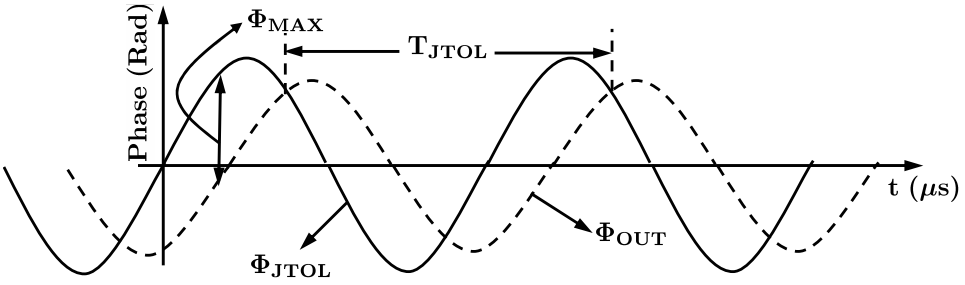

Figure 5.6: Plot of input and output phases.

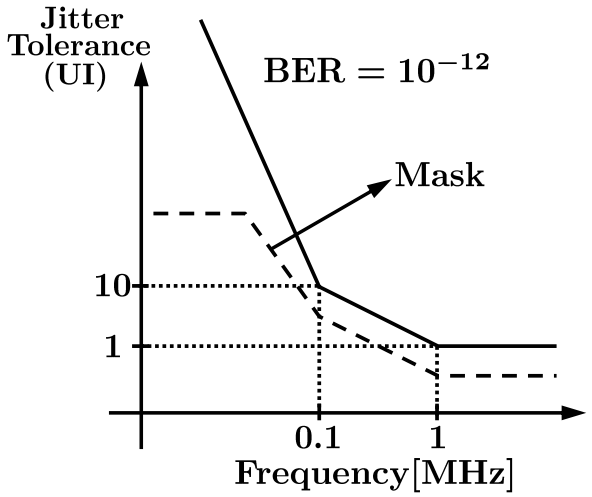

Figure 5.7: Plot of jitter tolerance curve.

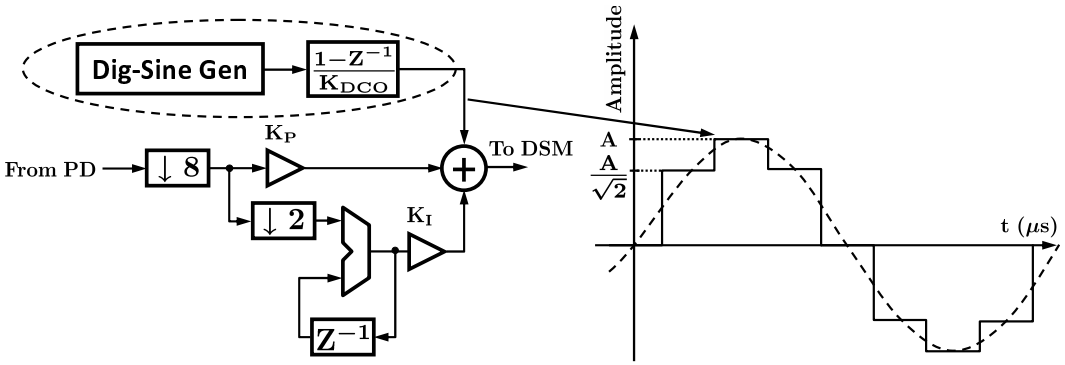

Figure 5.8: Addition of a digital sine-wave to the output of the digital loop filter of the CDR.

5.4 Summary

In this Chapter, certain techniques to improve the power efficiency of the phase averaging CDR have been presented along with the technique to measure the jitter tolerance on-chip. By employing a full rate CDR architecture, the necessity to route multiple phases was eliminated. The registers used in the digital loop filter were operated at a lower clock frequency resulting in more power saving. The CDR

Table 5.1: Performance Summary

Technology	90 nm CMOS
Supply Voltage	1.2V
Target data rates	0.5-5Gbps
Target lock-in range	200ppm
Target tracking-range	2000ppm
Target PLL PSNR @ 5Gbps	-28dB
Target jitter @ 5Gbps	R. M. S. 3.6ps
	Pk-pk: 20ps
BER @ 5Gbps	$< 10^{-12}$
Power consumption @ 5Gbps	10mW
Die Area	0.8 mm^2

uses the PLL architecture proposed in Chapter 2 and hence, has a low BER in the presence of power supply noise. The digital nature of the phase averaging CDR architecture was exploited to excite the CDR output clock with a known phase amplitude. This enables us to measure the jitter tolerance of the CDR on-chip.

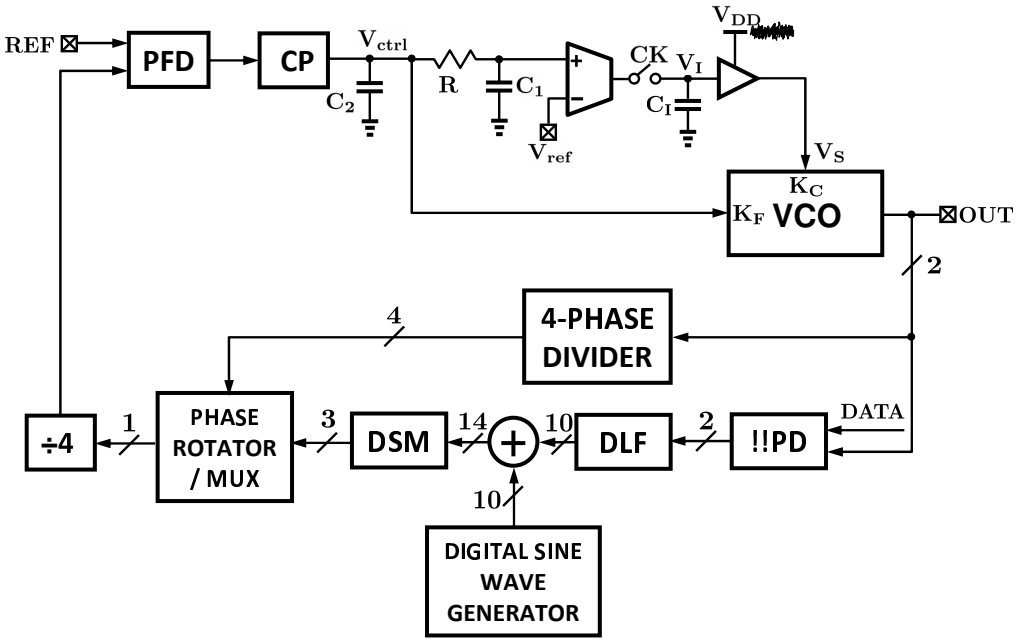

Figure 5.9: Complete block diagram of the proposed architecture.

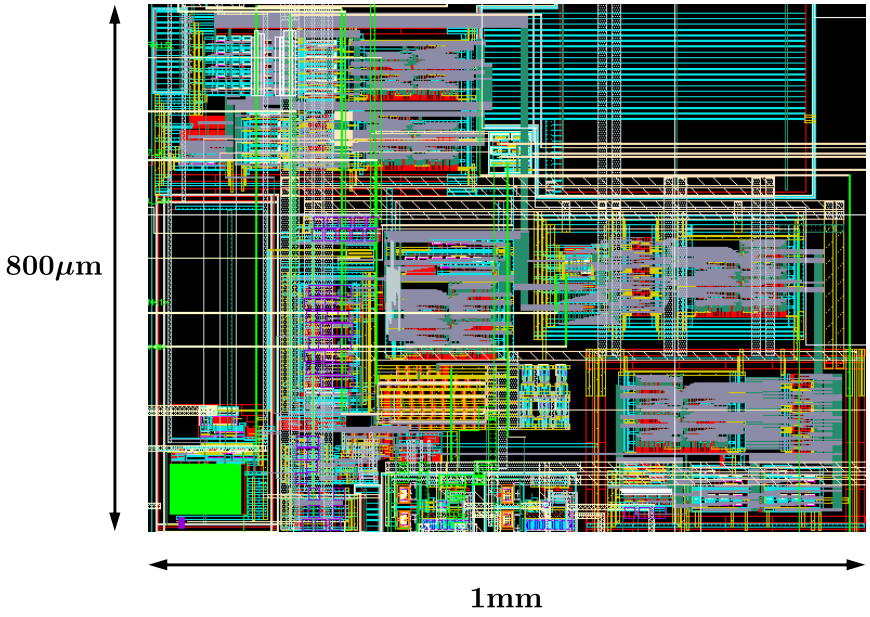

Figure 5.10: Layout of the CDR.

CHAPTER 6. CONCLUSIONS

Frequency synthesizers form an essential part in digital communication systems and high purity in the output phase spectrum of frequency synthesizers is necessary in high performance systems. Among others, effect of supply noise is one of the primary factors which determines the purity of the output phase spectrum of frequency synthesizers. In this thesis, techniques to improve the supply noise immunity of frequency synthesizers has been explored.

In Chapter 2, the effect of supply noise on ring-oscillator based frequency synthesizers was analysed. In particular, owing to the wide tuning range offered by a ring-VCO, the sensitivity of the output phase to noise on ring-VCO supply is very high and is the most dominant among all the building blocks of the frequency synthesizer. Techniques to effectively isolate the ring VCO supply from the supply noise is proposed. The use of a replica-load based regulator in a split-tuned PLL architecture is shown to provide excellent immunity to noise on ring-VCO power supply.

In Chapter 3, the effect of noise on the other building blocks of the PLL is considered. If the ring-VCO supply is provided with good regulation, then the effect of noise due to the other building blocks of the PLL becomes dominant. Analysis of the effect of noise on the supply of the other building blocks of the PLL is presented. Using the well regulated ring-VCO supply, the supplies of the other building blocks of the PLL can be effectively regulated to provide an excellent overall supply noise rejection.

Chapter 4, the intermodulation effects of the noise on charge pump supply

is analysed. The PLL behaves as a linear time-varying system in the presence of noise on charge pump supply. Analysis shows that the strength of higher order harmonics depend linearly on the amplitude of the noise on charge pump current. In applications where the frequency synthesizer output phase carries information, careful design is necessary to prevent the information from getting corrupted by the charge pump supply noise.

Finally, in Chapter 5, a full rate phase averaging CDR architecture with built in jitter tolerance measurement circuit is presented. The CDR employs the proposed split-tuned supply regulated PLL which results in a low BER resulting from power supply noise. The full rate CDR needs only two phases to be routed and hence, the power spent in routing the clocks is reduced. A digital sine wave generator is used to excite the CDR output clock with a known value of jitter. This enables on-chip jitter tolerance measurement of the CDR.

BIBLIOGRAPHY

[1] V. von Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra, "A 320 MHz, 1.5 mW@1.35 V CMOS PLL for microprocessor clock generation," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1715–1722, Nov 1996.

[2] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, Mar 2000.

[3] J. Kim, K. D. Jones, and M. A. Horowitz, "Variable domain transformation for linear PAC analysis of mixed-signal systems," in *IEEE/ACM Int. Conf. on Computer-Aided Design*.

[4] K. Y. K. Chang, J. Wei, C. Huang, S. Li, K. Donnelly, M. Horowitz, Yingxuan Li, and S. Sidiropoulos, "A 0.4-4-Gb/s CMOS quad transceiver cell using on-chip regulated dual-loop PLLs," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 747–754, May 2003.

[5] S. Sidiropoulos, D. Liu, J. Kim, G. Y. Wei, and M. Horowitz, "Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers," in *Symp. VLSI Circuits Dig. Tech. Papers*.

[6] A. Arakali, S. Gondi, and P. K. Hanumolu, "Low-power supply-regulation techniques for ring oscillators in phase-locked loops using a split-tuned architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2169–2181, Aug. 2009.

[7] C. H. Lee, K. McClellan, and Jr. Choma, J., "A supply-noise-insensitive CMOS PLL with a voltage regulator using DC-DC capacitive converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1453–1463, Oct 2001.

[8] T. Toifl, C. Menolfi, P. Buchmann, C. Hagleitner, M. Kossel, T. Morf, J. Weiss, and M. Schmatz, "A 72mW 0.03mm^2 inductorless 40Gb/s CDR in 65nm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*.

[9] P. Larsson, "A 2-1600-MHz CMOS clock recovery PLL with low-Vdd capability," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1951–1960, Dec 1999.

[10] P. K. Hanumolu, G. Y Wei, and U. K Moon, "A wide-tracking range clock and data recovery circuit," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 425–439, Feb. 2008.

[11] A. Arakali, N. Talebbeydokthi, S. Gondi, and P. K. Hanumolu, "Supply-noise mitigation techniques in phase-locked loops," in *Proc. European Solid-State Circuits Conference*, Sept. 2008, pp. 374–377.

[12] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U. K Moon, "Analysis of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 9, pp. 1665–1674, Sept. 2004.

[13] E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, "Replica compensated linear regulators for supply-regulated phase-locked loops," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 413–424, Feb. 2006.

[14] M. S. J. Steyaert and W. M. C. Sansen, "Power supply rejection ratio in operational transconductance amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, no. 9, pp. 1077–1084, Sep 1990.

[15] S. Williams, H. Thompson, M. Hufford, and E. Naviasky, "An improved CMOS ring oscillator PLL with less than 4ps RMS accumulated jitter," in *Proc. IEEE Custom Integrated Circuits Conf.*

[16] W. B. Wilson, U. K Moon, K. R. Lakshmikumar, and L. Dai, "A CMOS self-calibrating frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1437–1444, Oct 2000.

[17] G. W. den Besten and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 956–962, Jul 1998.

[18] E. Alon, *Measurement and regulation of on-chip power supply noise*, Ph.D. thesis, Stanford University, Stanford, CA, Dec 2006.

[19] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct 1989.

[20] T. Toifl, C. Menolfi, P. Buchmann, M. Kossel, T. Morf, and M. L. Schmatz, "A 1.255 GHz clock generator with high-bandwidth supply-rejection using a regulated-replica regulator in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2901–2910, Nov. 2009.

[21] M. Mansuri, D. Liu, and C.-K. K. Yang, "Fast frequency acquisition phase-frequency detectors for Gsamples/s phase-locked loops," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1331–1334, Oct 2002.

[22] J. F. Parker, D. Weinlader, and J. L. Sonntag, "A 15mW 3.125GHz PLL for serial backplane transceivers in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers.*

[23] P. Vanassche, G. Gielen, and W. Sansen, "Symbolic modeling of periodically time-varying systems using harmonic transfer matrices," *IEEE Trans. Computer-Aided Design*, vol. 21, no. 9, pp. 1011–1024, Sep. 2002.

[24] A. Arakali and P. K. Hanumolu, "On the intermodulation effects of charge pump supply noise in phase locked loops," *submitted to IEEE Trans. Circuits Syst. II*, 2010.

[25] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.

[26] P. R. Karlsson and K. O. Jeppson, "An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors," *IEEE Transactions on Semiconductor Manufacturing*, vol. 9, no. 2, pp. 215–222, May 1996.

[27] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700-kHz bandwidth $\Sigma\Delta$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sept. 2004.

[28] G. Wei, J. Stonick, D. Weinlader, J. Sonntag, and S. Searles, "A 500MHz MP/DLL clock generator for a 5Gb/s backplane transceiver in 0.25μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*.

[29] G. Giustolisi and G. Palumbo, "A detailed analysis of power-supply noise attenuation in bandgap voltage references," *IEEE Trans. Circuits Syst. I*, vol. 50, no. 2, pp. 185–197, Feb. 2003.

[30] M. Takamiya, M. Mizuno, and K. Nakamura, "An on-chip 100 GHz-sampling rate 8-channel sampling oscilloscope with embedded sampling clock generator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*.