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S. J. T. Owen

In microwave network analysis, proper matching of the measurement system is necessary to prevent measurement errors and provide a proper terminating impedance for the device-under-test. To obtain this matching, a buffer amplifier is often used in the first stage of the network analyzer.

This study describes the design and analysis of one such amplifier for use in a future generation of Hewlett-Packard network analyzers. Design goals, specifically for return loss, were set. The amplifier was to operate in the 100 kHz to 3 GHz range. A common base amplifier was chosen, and an analysis performed to determine problem areas. Methods of correcting the problem areas were presented, and a breadboard was constructed for measurement purposes. The measurements presented indicate that the final circuit met all specifications.

The Analysis and Design of a Broadband Microwave Buffer Amplifier

by

Joel P. Dunsmore

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THE ANALYSIS AND DESIGN OF A BROADBAND MICROWAVE AMPLIFIER

This thesis describes the design and analysis of a microwave buffer amplifier. The amplifier has to meet specific design goals for ultimate use in a microwave network analyzer. The goals were set to meet or exceed current state-of-the-art performance of circuits of similar cost and complexity. The input of the circuit will interface directly with the outside world. The output will go to a sampling-mixer circuit; to prevent reflections from interfering with the device under test, the amplifier should have high reverse isolation.

This design task was assigned as a summer project during a co-operative summer intern program at Hewlett-Packard's Network Measurement Division in Santa Rosa, California, and continued at Oregon State University.

Current with modern microwave practices, most measurements are made in scattering parameters or S-parameters. S-parameters fully describe the operation of a two port circuit. The definition of S-parameters, and the relationship between S-parameters and the more familiar Z-parameters are given in appendix A. S-parameter design techniques were used extensively during the development of this circuit.

This thesis details the design process from initial design specifications, through experimental and analytical work, to the final design and working prototype.

CHAPTER 1

SPECIFICATIONS

The amplifier described here is to be used as the input stage for a new generation of network analyzers being developed at Hewlett Packard. The performance and frequency range of this new generation of network analyzer will surpass that of two previous network analyzers: the 8407 network analyzer, with frequency range from 0.1 to 110 MHz; and the 8754 network analyzer, with frequency analyzer, with frequency range from 10 MHz to 2.6 GHz. This new network analyzer will operate oever the range of 0.1 MHz to 3.0 GHz.

An important specification in network measurement instruments is the input match of the instrument. The error introduced in a measurement can be directly related to the mismatch at the input port. Also, a mismatch at the input port may cause the device under test to operate improperly. Another important input characteristic is the input power saturation, or the 1 dB gain compression. These are the major specifications to be met.

Other considerations include amplifier gain, cost, and noise figure. In addition, the design must meet standard engineering quality with respect to reliability and producibility.

The complete specifications are:

Input match:
- >28 dB Return Loss from .5 MHz to 1. GHz
- >22 dB Return Loss from .1 MHz to .5 MHz
- >22 dB Return Loss from 1. GHz to 3. GHz

Frequency response:
- 300 kHz to 3 GHz -1 dB down
- 100 kHz to 300 kHz -2 dB down

1 dB gain compression:
- >5 dBm required
- >10 dBm desired

Midband gain:
0 to -4 dB acceptable

Noise figure:
<10 dB to 3 GHz

Cost:
Similar to the input amplifier in the HP 8754 NA

It is appropriate to evaluate these specifications with respect to what is currently available to perform network analysis.

At this time, there is no network analyzer available from Hewlett-Packard which extends over the frequency range of 0.1 MHz to 3.0 GHz. Market analysis indicates a need for an instrument covering this range. Most network analyzers specify an input return loss on the order of 23-26 dB, and a maximum input power of 10 dBm. The above goals surpass the former, and equal the latter. The rest of the specifications correspond to those found in instruments currently in use. In order to meet the objective of cost, it is necessary to use a circuit of similar complexity to that used in the HP 8754. This eliminates costly alternative solutions such as band-switching or multi-device circuits, which might include multi-stage amplifiers. These solutions are inherently costly because of the expense of microwave components.

CHAPTER 2

OPNODE MODELING

In the field of microwave circuit design, the difficulty of evaluating the operation of a circuit analytically dictates the need for computer aided techniques. One program available for this purpose is the Hewlett-Packard OPNODE computer-aided linear circuit design program. OPNODE (a mnemonic for OPtimization of NOdal networks) is a collection of programs and subroutines which allow, among other things, analysis, optimization, and filter or matching network synthesis. For this project, the analysis portion was used extensively for confirming models, and checking new designs for specified performance.

The OPNODE program is a nodal analysis program much like SPICE or other simulation programs. An important difference is that OPNODE is specifically tailored to be used with microwave circuits. Outputs of the analysis are in scattering parameters, in rectangular or polar form. Another feature is the flexibility in entering device and circuit structures. Since the 2-port scattering parameters fully describe a network, all that is needed to describe a component, or circuit, is measured S-parameters at desired frequencies. The S-parameters can be easily converted to transfer or T-parameters, whose properties allow cascading of networks by matrix multiplication of these T-parameters (1). The relationship between transfer and scattering parameters is given in appendix A. This gives a simple way to find the overall network function. OPNODE uses this to provide the overall S-matrix of a complex circuit. The OPNODE program allows entering device characteristics by several methods:

a) by giving the S-parameters at specified frequencies (OPNODE interpolates between given frequency points), such as the measured S-parameters of a transistor;

b) by giving the device in terms of a small signal model composed of inductors, capacitors, resistors, transmission lines, dependent and independent sources, etc., such as a hybrid π model of a transistor;

c) by creating S-parameters by using some kind of defining equation.

The third method can be used to compare a hand analysis of a circuit with the network function derived by OPNODE analysis of the small signal model.

EXAMPLES OF OPNODE

Frequency Response of an RC Circuit

As an example of the use of OPNODE, consider the simple circuit shown in Figure 1. This circuit has a pole at $f=1/2\pi(R_1+R_2)C$, and a zero at $f=1/2\pi R_2C$. For R_1=30 ohms, R_2=20 ohms and C=100pF, the pole and zero frequencies are fp=31.8 MHz, and fz=79.6 MHz. Using the VDBPLOT program in OPNODE, the gain of the circuit is plotted in Figure 2. This example shows how OPNODE can solve problems for a nodal network.

Often in microwave design, the specifications are set in S-parameters, such as return loss (equivalent to S11) or power gain equivalent to (S21). In Figure 2, the signal reflected from the input, referenced to a fifty ohm system represents S11. Figure 3 shows a plot of S11 versus frequency for the simple RC circuit. At low frequencies the input impedance looks like an open circuit; the reflection of an open circuit has unit magnitude and zero phase change. At high frequencies, the capacitor looks like a short circuit, and the reflection looks like that of 50 ohm resistor in a

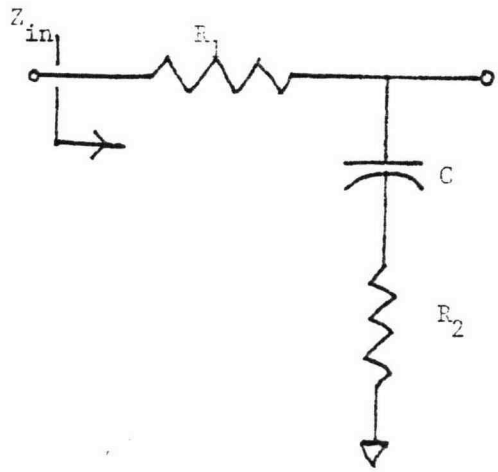


Figure 1. RC Circuit

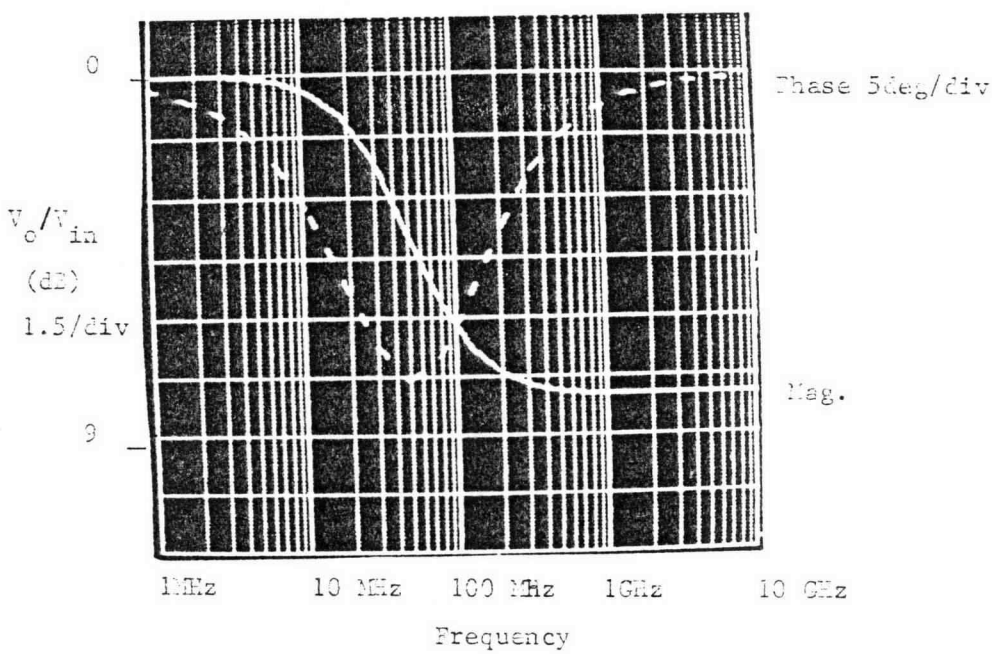


Figure 2. Transfer function of RC circuit

50 ohm system; this should have a zero magnitude and phase. The locus of points in between follows a curve of constant resistance on the Smith chart. The characteristics of a Smith chart are shown in appendix B.

S11 of Simple Impedances

The representation of a reflection parameter (S11 or S22) as a locus, with respect to frequency, of points on a Smith chart is very useful in microwave engineering. From this representation, the impedance of a device can be read directly from the resistive and reactive curves of the Smith chart. It is helpful if the frequency is marked in some way; OPNODE allows the user to move a curser along the locus of S11 while displaying frequency, magnitude, and phase information.

In Figure 3, the locus of reflection follows a constant resistive circle; this is to be expected since the real part of the input impedance of the circuit is a constant 50 ohms, but the reactive part varies from near infinite at low frequencies, to near zero at high frequencies.

It may be helpful to look at the representation of the impedance of other simple circuits as an S11 locus on a Smith chart to become familiar with the shape and region of occurence of these loci. Figure 4 shows an RL series circuit, and its associated S11 locus. It is similar to plot of the RC combination, following a constant resistive circle, but with the imaginary part being in the upper or positive reactance portion of the Smith chart. These two simple examples demonstrate that, in general, when the S11 locus lies in the upper half of the Smith chart, the impedance has some inductive

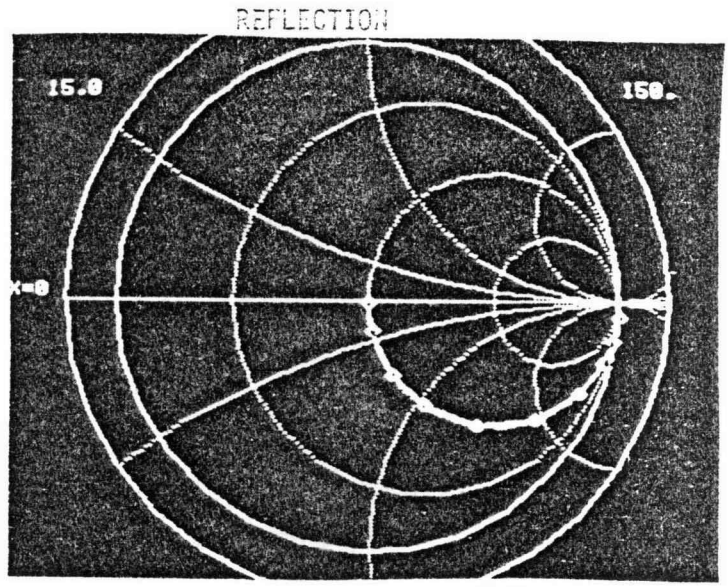


Figure 3. S11 locus of RC circuit, R=50 ohms

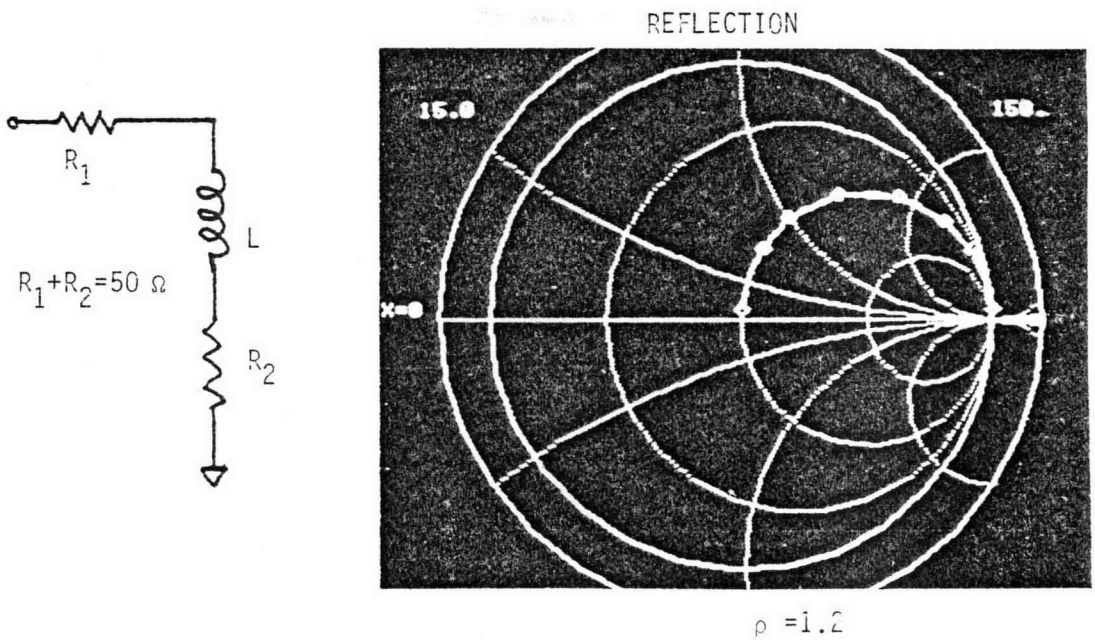


Figure 4. S11 locus of LC circuit

element associated with it. Similarly, S11 in the lower half of the Smith chart implies a capacitive component in the impedance.

However, an input impedance can have a negative imaginary part without being capacitive, or have a positive imaginary part without being inductive. Active devices, and feedback mechanisms can cause impedance transformations that make resistors look inductive, or inductors look capacitive, etc. Transmission lines can also cause impedance transformations. At low frequencies, the lengths of connections are very small compared to wavelength, but in microwave circuits, almost all interconnections must be treated as transmission lines.

To demonstrate the effect of a transmission line, consider the circuit shown in Figure 5. Here, a 50 ohm system is terminated with a 40 ohm lead, separated from the system by a finite legnth 50 ohm transmission line. Notice, in Figure 6, the impedance of this termination looks resistive at low frequencies, but as frequency is increased, begins to look more inductive. At the frequency which the length of the line corresponds to a quarter wavelength, the impedance looks real and has a value of 62.5 ohms. As the frequency is increased, the impedance looks more capacitive, until the length of the line corresponds to a half wavelength, when the impedance as before is 40 ohms. This cycle will be repeated if the frequency continues to increase. In Figure 6, the maximum frequency shown corresponds to the line being approximately .45 wavelength.

To see the effect of a transmission line on an S11 locus, consider the circuit in Figure 1 with the total resistance $R_1+R_2=40$ ohms. If a transmission line whose length corresponds to about one full wavelength at the highest frequency is added, it has the effect

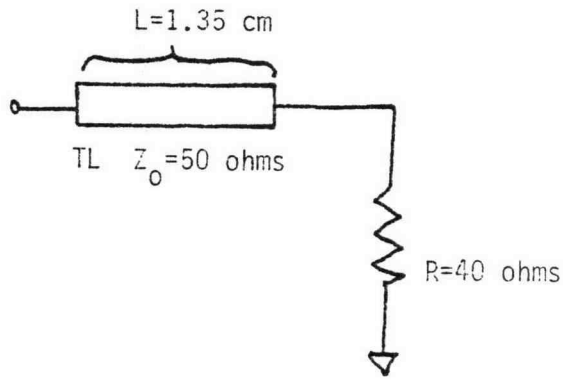


Figure 5. Transmission line, 40 ohm term

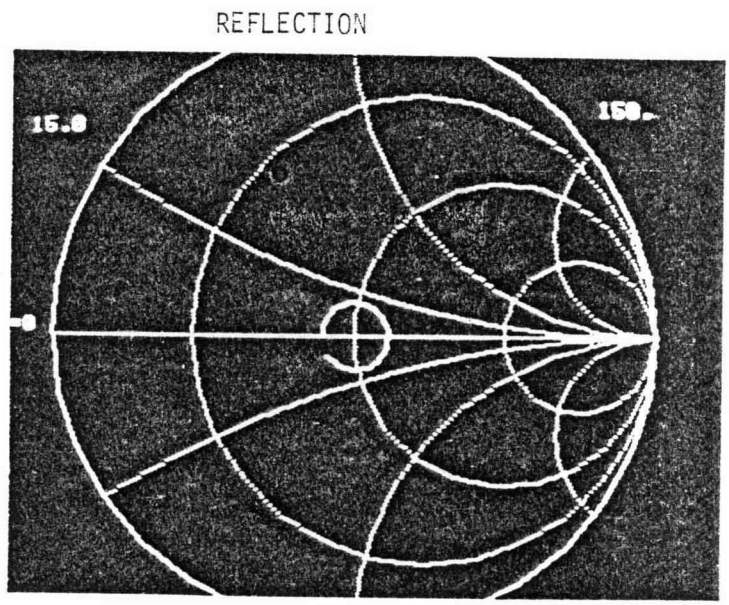


Figure 6. S11 of Figure 5

of changing the plane of reference of the calculation. Figure 7 shows the S11 plot of the same circuit used in Figure 1, with just the resistance changed; it follows a constant 40 ohm resistive circle. Figure 8 shows the S11 locus for the same circuit as above, with a transmission line added. Here it is much more difficult to see that the termination is simply an RC circuit. The transmission line has transformed the phase of the S11 locus, with the amount of phase change proportional to the frequency. At low frequency, little phase change is noted; at high frequency, nearly 360° of phase change has occurred.

These simple examples serve a dual purpose. The concept of expressing impedance as a reflection coefficient, and the relationship between the impedance and reflection coefficient is presented. Also the use of OPNODE to analyze small signal circuits is shown. All the figures in this section were generated by OPNODE.

OPTIMIZATION

In addition to analysis, OPNODE will optimize a circuit component, or components to elicit a desired reflection coefficient over the frequency range of interest. This is done by specifying an adjustable component, and letting OPNODE change the value, analyzing the result until a successful configuration is achieved. Of course, the optimization requires an accurate model of the circuit to be analyzed. Finding such a model can often be very difficult, and may be the most time consuming part of a circuit design.

The OPNODE program can be used to optimize an S-parameter of any circuit. There are special routines which are tailored to optimizing amplifier performance for magnitude and phase response. More

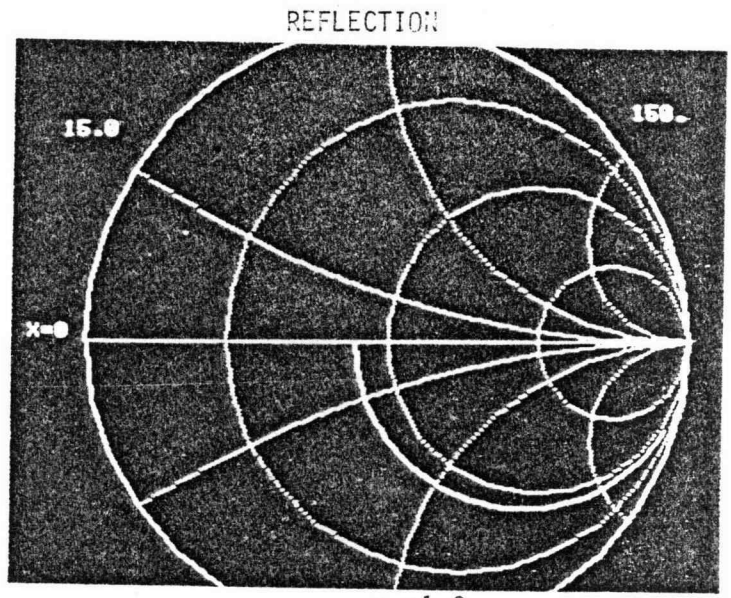


Figure 7. S11 of RC circuit, R=40 ohms

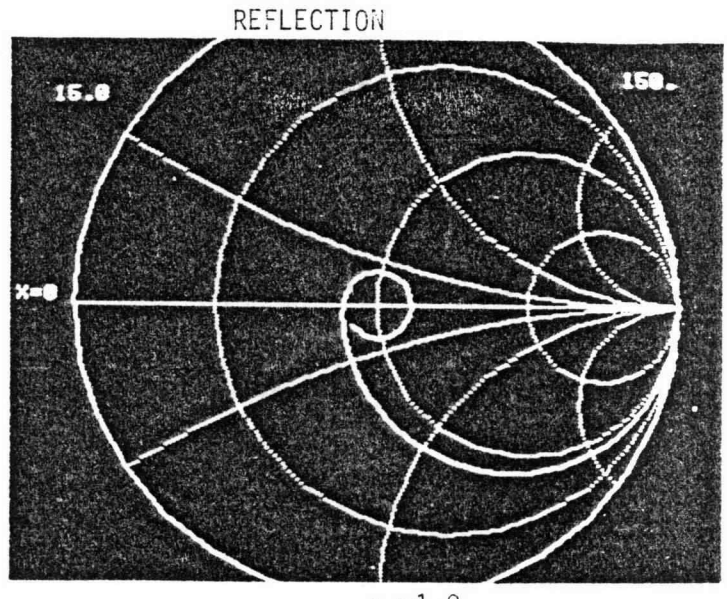


Figure 8. S11 of transmission line with 40 ohm termination

information on this can be found in the OPNODE manual (2).

Throughout this thesis, OPNODE will be used to analyze circuits, and confirm models obtained by hand calculations, as well as optimize circuits. Source files used to create OPNODE plots can be found in the appendix.

CHAPTER 3

EVALUATING DESIGNS

DESIGN CHOICES

In any design task, a starting point must be chosen. In this design, an amplifier currently in use was chosen as starting point. The HP 8754 Network Analyzer operates over a range of 10 MHz to 2.6 GHz, and its input amplifier is used as benchmark and a basis for this design. This circuit, shown in Figure 9, is typical for a wide-band amplifier. It consists of a single stage common base amplifier. A characteristic of such amplifiers is wide bandwidth and high reverse isolation, as will be shown in detail later.

Other choices were possible, for example, common emitter or multi-stage Bipolar Junction Transistor (BJT), and Field Effect Transistor (FET) amplifiers in common source or common gate configurations. The common emitter BJT circuit, while having high gain, was rejected because of its comparatively low bandwidth. High cost eliminated the multi-stage amplifier concept.

Both common source and common gate amplifiers were rejected because of the high 1/f noise of FET's causes concern in the area of noise floor reduction in the low frequency region of operation.

At attempt to extend further the range of the common base circuit used in the HP 8754 requires careful study of the circuit. The actual limitations of the circuit must be found, and, if the design goals are not within these limitations, then improvements or modifications must be made.

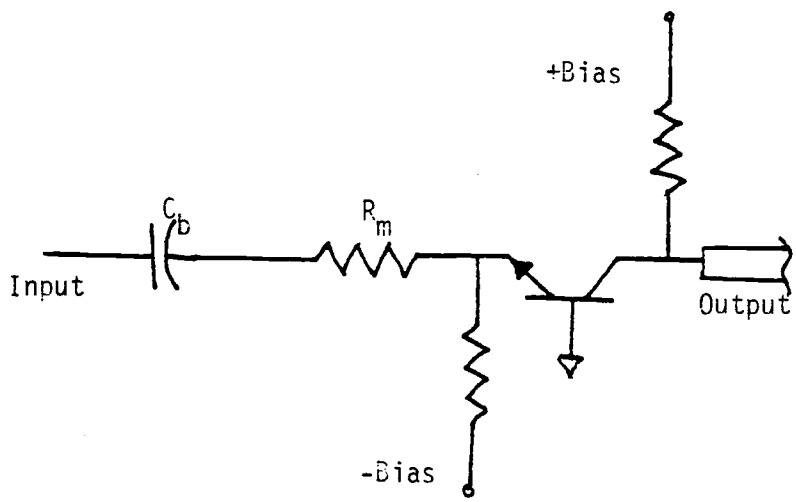


Figure 9. HP 8754 common base circuit

EVALUATING CURRENT DESIGN

An evaluation of the HP 8754 amplifier will serve two purposes: first, it will identify the shortcomings of the design, and second, it will help establish benchmarks and testing routines to be used throughout the design and evaluation process.

Figure 10 shows the initial measurement of S11, the input return loss of the amplifier. Note that this measurement displays the magnitude of the return loss as a function of frequency in the high frequency region of operation. The specification is shown as a line above which the trace of S11 must remain. It is clear that the return loss specification will not be met by the existing ciruict in the high frequency range. A low frequency measurement of the return loss, shown in Figure 11, also indicates unacceptable performance.

A measurement of power gain saturation is shown in Figure 12; the 20.6 mA case exceeds the safe operation range of the device. The 10 dBm input power specification desired cannot be achieved with normal bias.

Noise figure measurements show greater than 10 dBm noise floor above 1 GHz. The noise figure measurement, as measured on an HP 8970 noise figure meter, from 10 MHz to 1.5 GHz, was just under 10 dB. At higher frequencies, no accurate noise figures could be measured.

The midband gain, S21, was measured to be -2 dB, within acceptable limits. The measurement of S21 versus frequency is shown in Figure 13.

Equipment Used

With the exception of midband gain, the amplifier tested failed

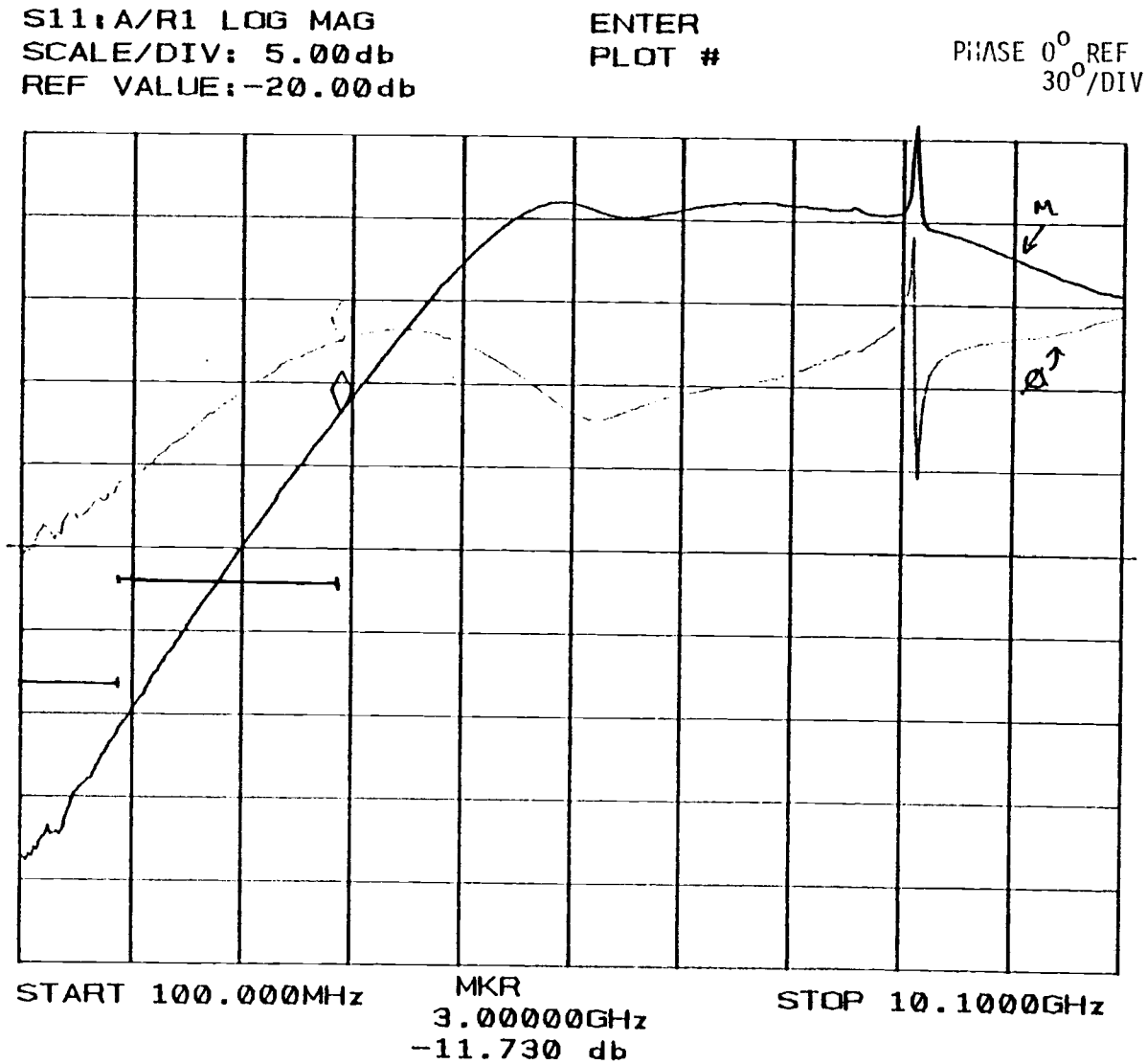


Figure 10. S11 of HP 8754 amp. (rect)

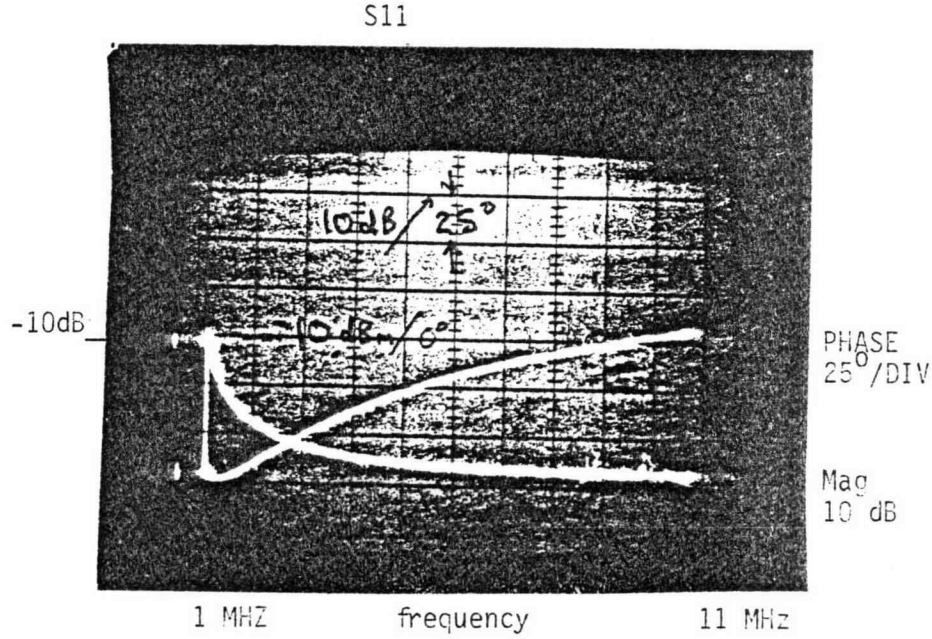


Figure 11. S11 of HP 8754 amp. (low freq.)

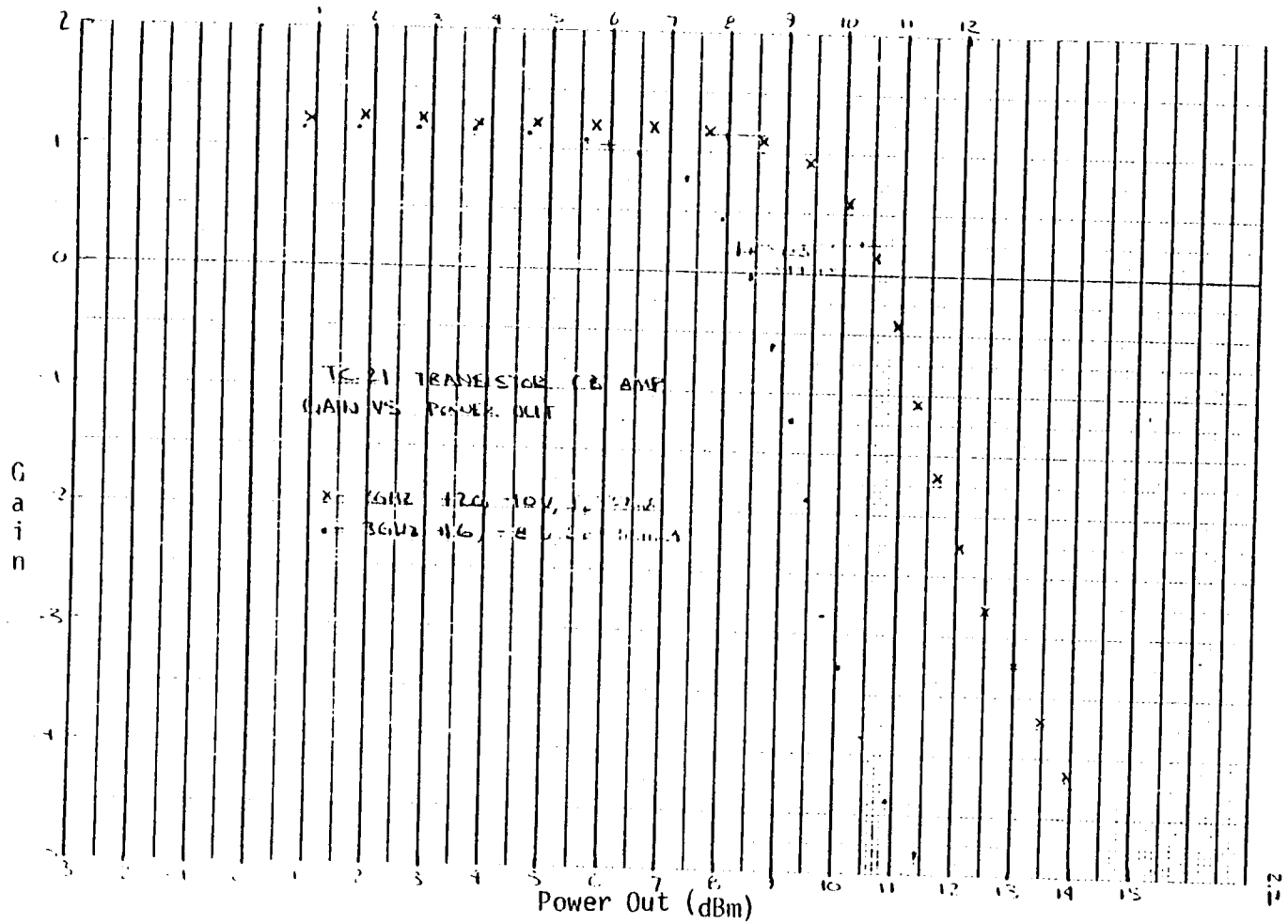


Figure 12. Power gain saturation of TC 21

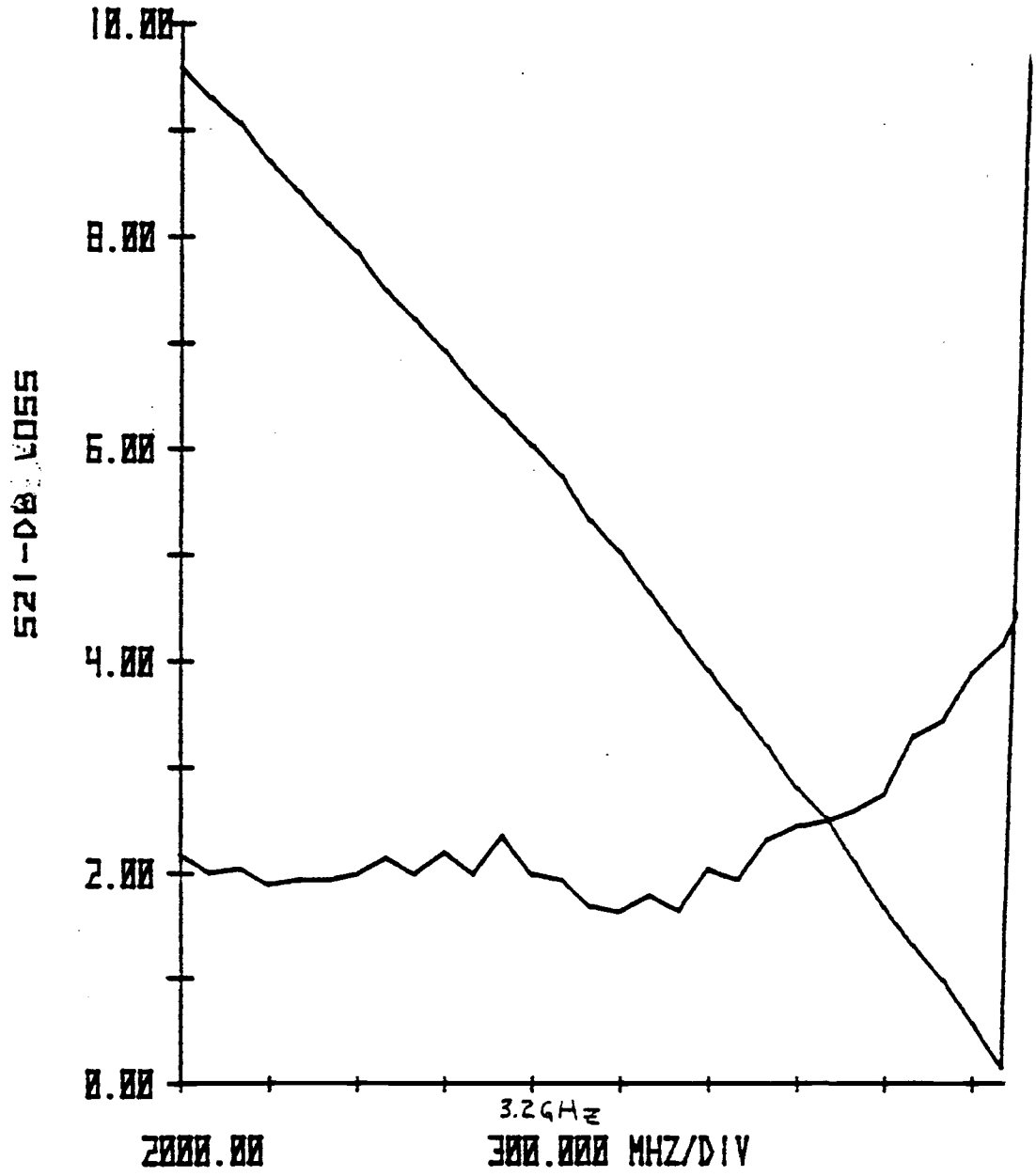


Figure 13. S21 of HP 8754 amp.

to meet the desired goals. To redesign this circuit to meet the desired specifications, it is necessary to identify the causes of the limitations which were measured. This requires accurate data to be taken, and a detailed analysis of this data. The tools at hand to take data are limited to network analyzers (or S-Parameter test sets) and time domain reflectometers (TDR).

The network analyzer used gives both magnitude and phase information at the frequency measured. These can be plotted as a polar plot over a Smith chart. In this way, the input impedance seen at the measurement port can be directly related to the plot, referenced to 50 ohms. In this persepctive, the goals set can be represented as circles about the origin inside of which the S11 trace must remain. For the specifications, the low frequency goal is shown as a circle of radius .1 (22 dB), the high frequency goal is shown as a circle of radius .05 (28 dB). The Smith chart representation, if properly interpreted, can reveal a great deal about the nature of the reflection.

In addition to frequency domain analysis, the use of the time domain reflectometer allows a time domain analysis of the circuit. This type of analysis provides a means to locate, in a physical manner, the position of a discontinuity. This will be very useful in the analysis of packaging for the amplifier.

Measurement Methods

The initial measurements were made on test structures using the substrate assembly from the HP 8754. The substrate carries all the micro-circuit components as well as the signal and bias lines. The structure used an SMA input connector, and a machined, gold plated

package. A package which must be custom machined is quite expensive. This package will be replaced by a readily available commercial package. The SMA input connector (SMA stands for subminiature type A) is a coaxial through-the-wall type connector which transmits the signal to the inside of a hermetically sealed package. Output was obtained by modifying the substrate; the substrate was cut just past the amplifier section and the transmission line which had gone to the sampling mixer section was bonded to another SMA connector. A drawing of this modified circuit substrate is shown in Figure 14.

Figure 15 shows the performance of the amplifier, plotted on a Smith chart. Measurements were taken from 2 GHz to 10 GHz in .5 GHz steps. Figure 16 shows the same measurement from 2 GHz to 5 GHz in .1 GHz steps. It is easy to identify the point at which this amplifier fails to meet the high frequency return loss specification; the reason for this is not so obvious. It is important to note that the plane of reference for this measurement is at the SMA input connector. To associate the measurement with the impedance looking into the transistor, the effect of the transmission line from the SMA connector to the circuit must be accounted for.

The complete schematic diagram, with possible parasitic elements included, is shown in Figure 17. The high frequency degradation is due in some part to both the input line section, and the section containing transistor with its associated bias components.

Finding a solution to eliminate the unwanted effects of these sections, will be easier if these effects can be separated. The input transmission line structure can be easily studied by appropriatly terminating the input line, rather than connecting it to the transistor. In order to operate the transistor section, however, the

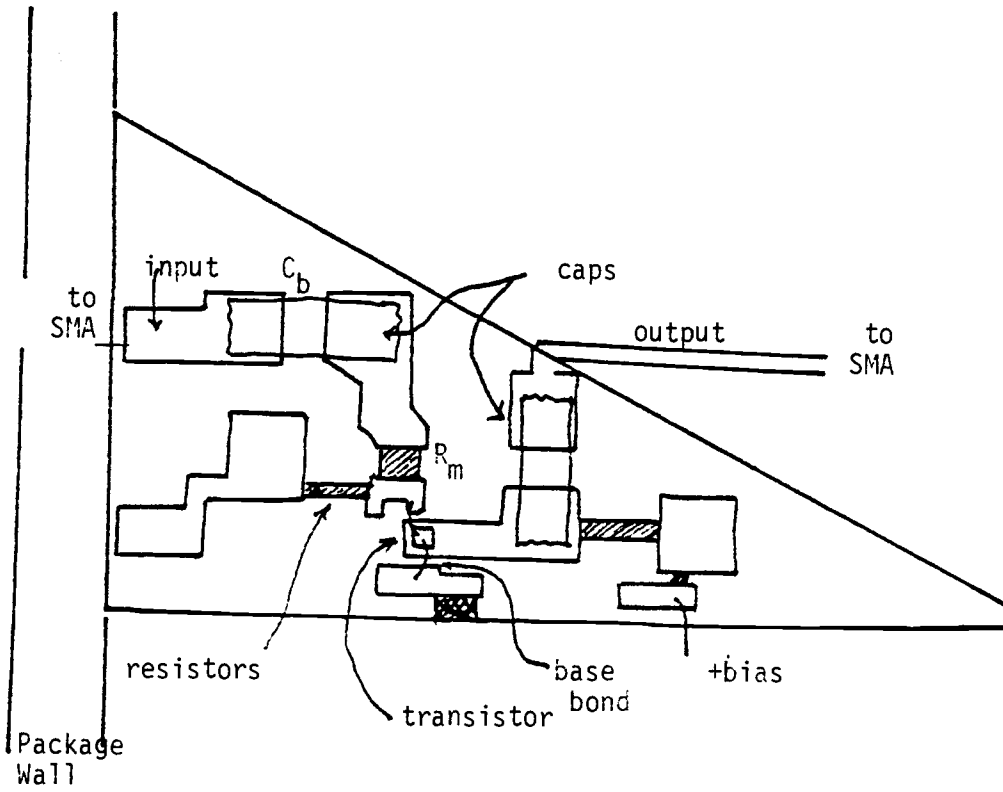


Figure 14. Circuit layout of HP 8754 amp.

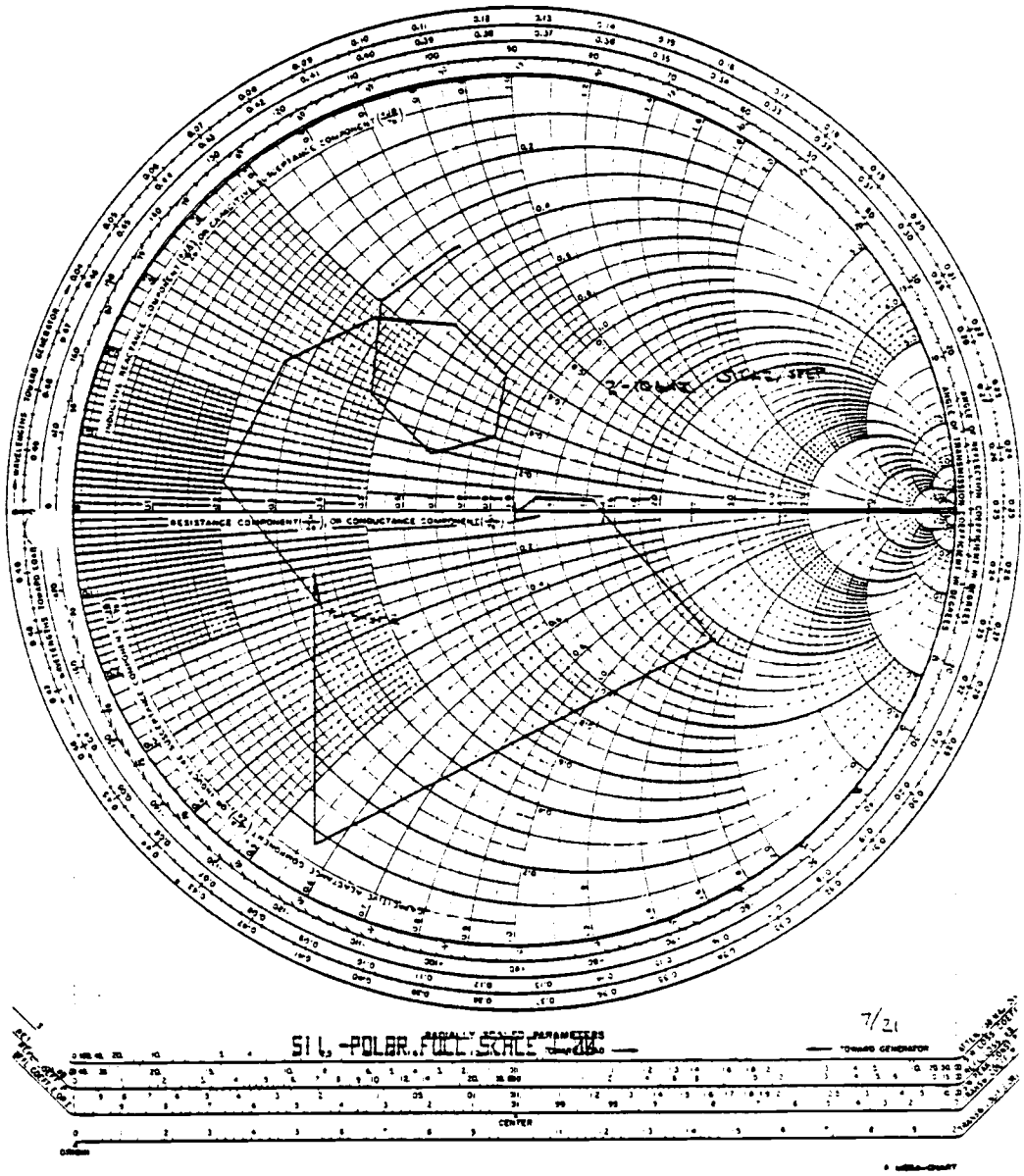


Figure 15. S11 of HP 8754 (polar 2-10 GHz)

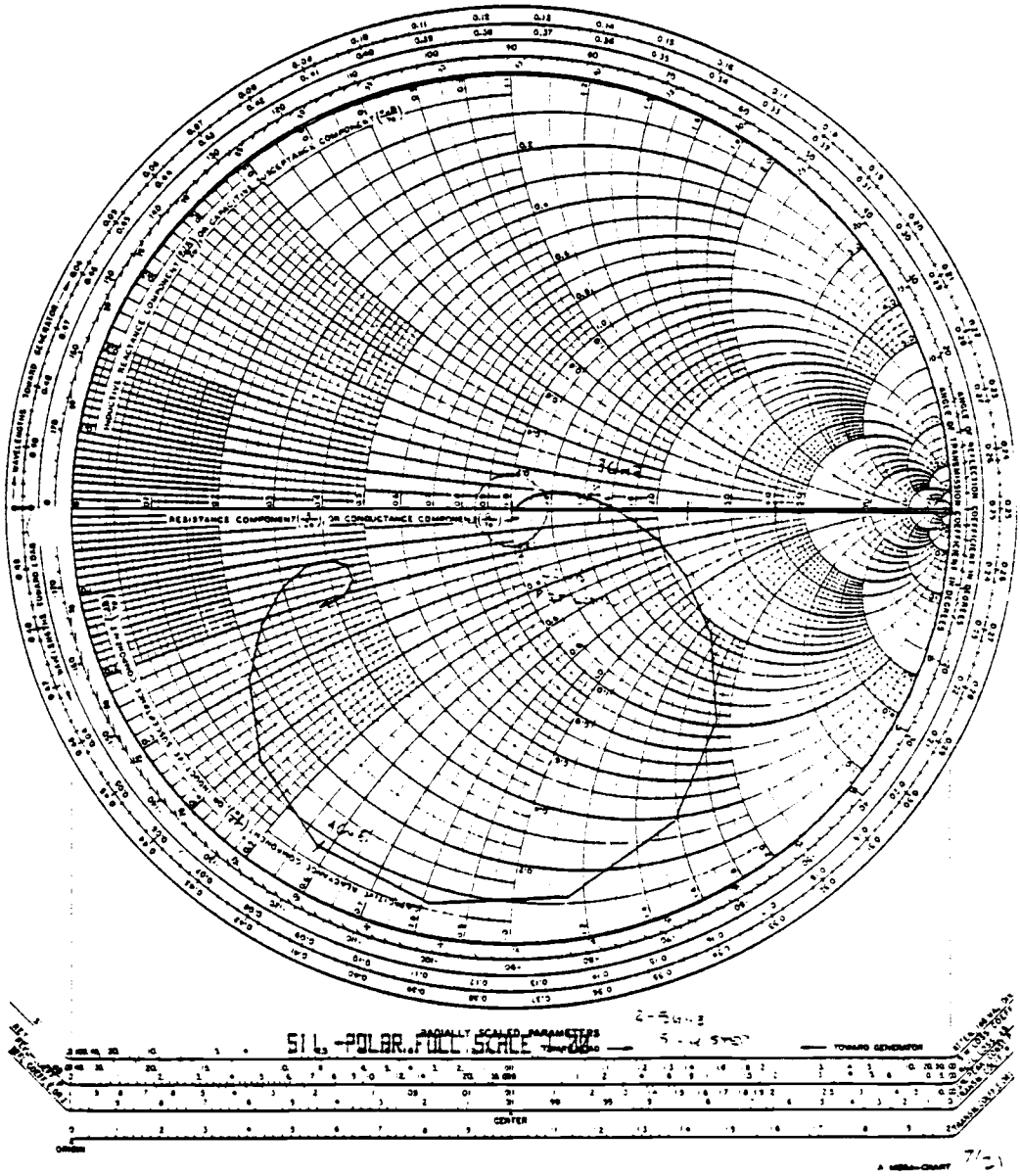


Figure 16. S11 of HP 8754 (polar 2-5 GHz)

TL - Transmission Line

C_p - Parasitic Capacitor

L_p - Parasitic Inductor

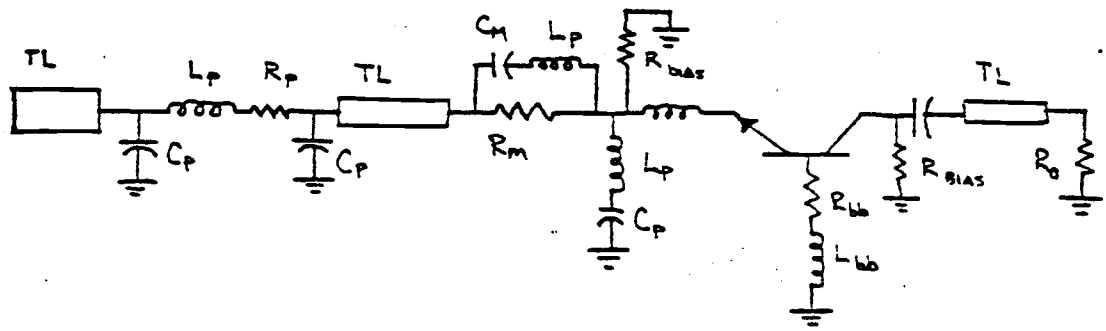


Figure 17. Common base circuit with parasitics

input line section is required. The effect of the input line section can be eliminated, though, through using the calibration and error correcting feature of the network analyzer.

The high performance automatic network analyzer used allows calibration using standard open circuits, short circuits, and loads. These define the reference plane and reference levels for all future measurements. Any losses or reflections in the instrument can be calibrated out of the measurements. By using an open, short and load at the end of an equivalent transmission line, the effect of the transmission line section will also be calibrated out. In addition, by measuring the equivalent transmission line at its input, the effect of the transmission line (reflections, radiation, loss, etc.) can be found.

Test Structures

Transmission line test structures with open, short and 50 ohm terminations were constructed, as shown in Figure 18, and measured, as shown in Figure 19. Note that the short has nearly 0 dB return loss.

The open has about 3 dB of return loss in the band of interest, but at 8.17 GHz, has a very sharp and large return loss. This can be shown to be a radiation effect at that frequency; the line being approximately ¼ wavelength at 8 GHz.

To demonstrate this, a TDR measurement of the open circuit line and a reference open circuit was made, Figure 20. The difference in time corresponds to twice the length of the transmission line divided by the speed of light in the medium. Since the transmission line is on saphire, the velocity of propogation is approximately

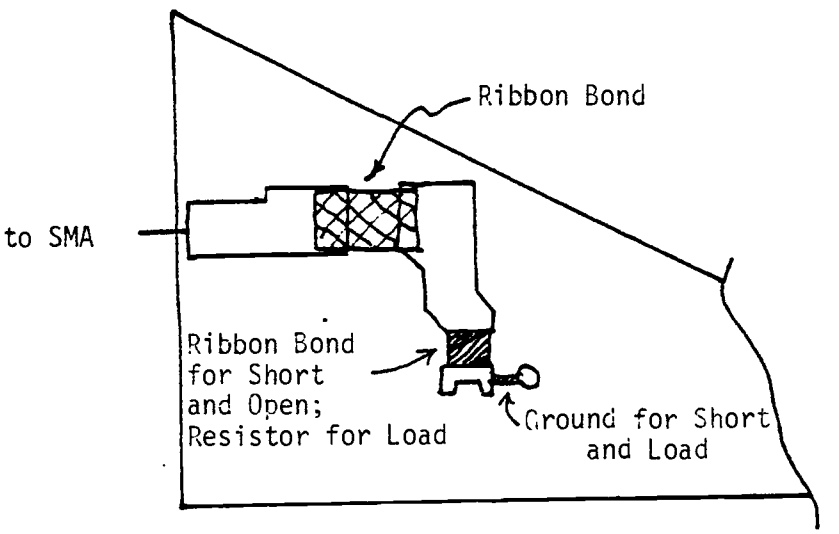


Figure 18. Transmission line structures

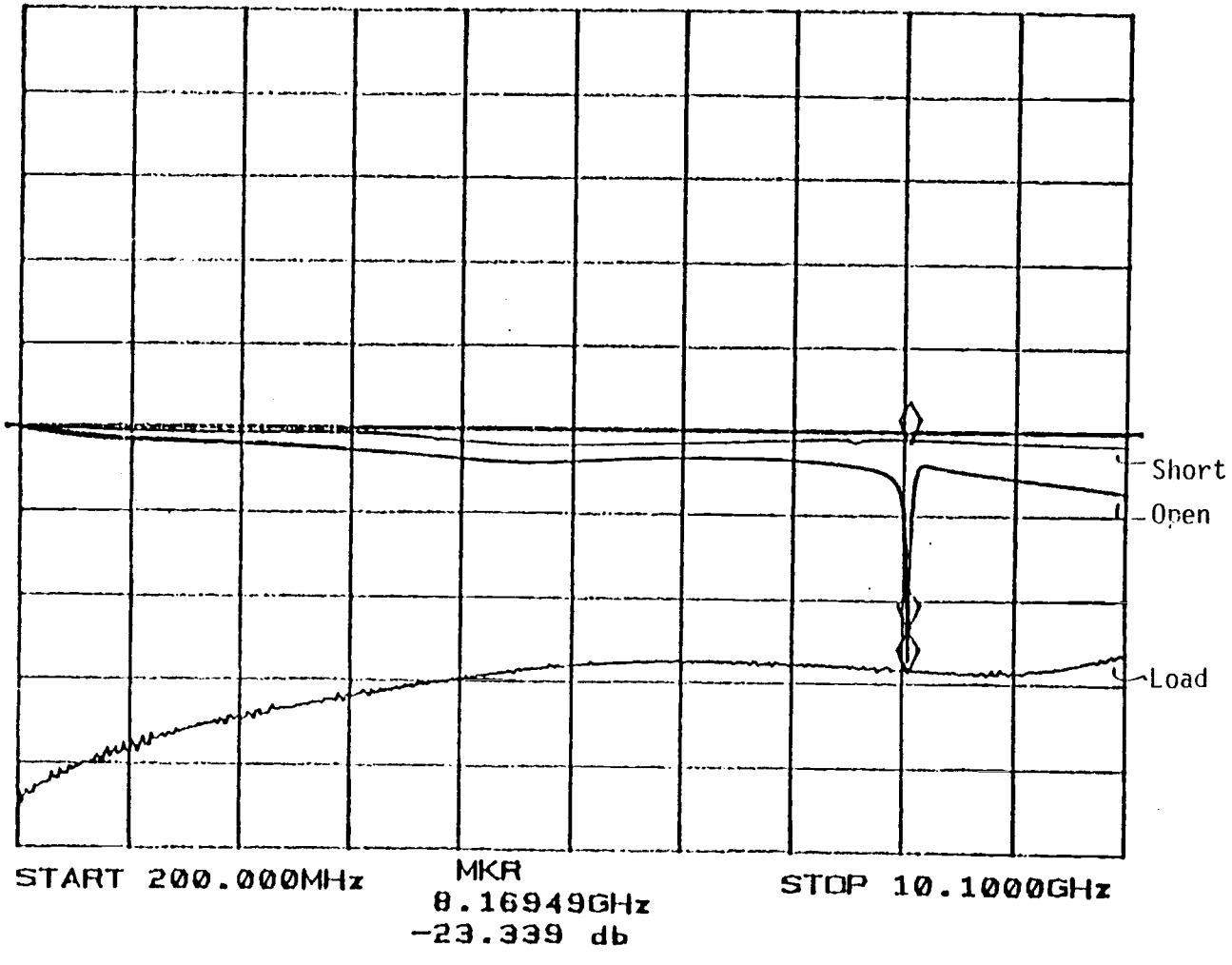


Figure 19. S11 of transmission line structures

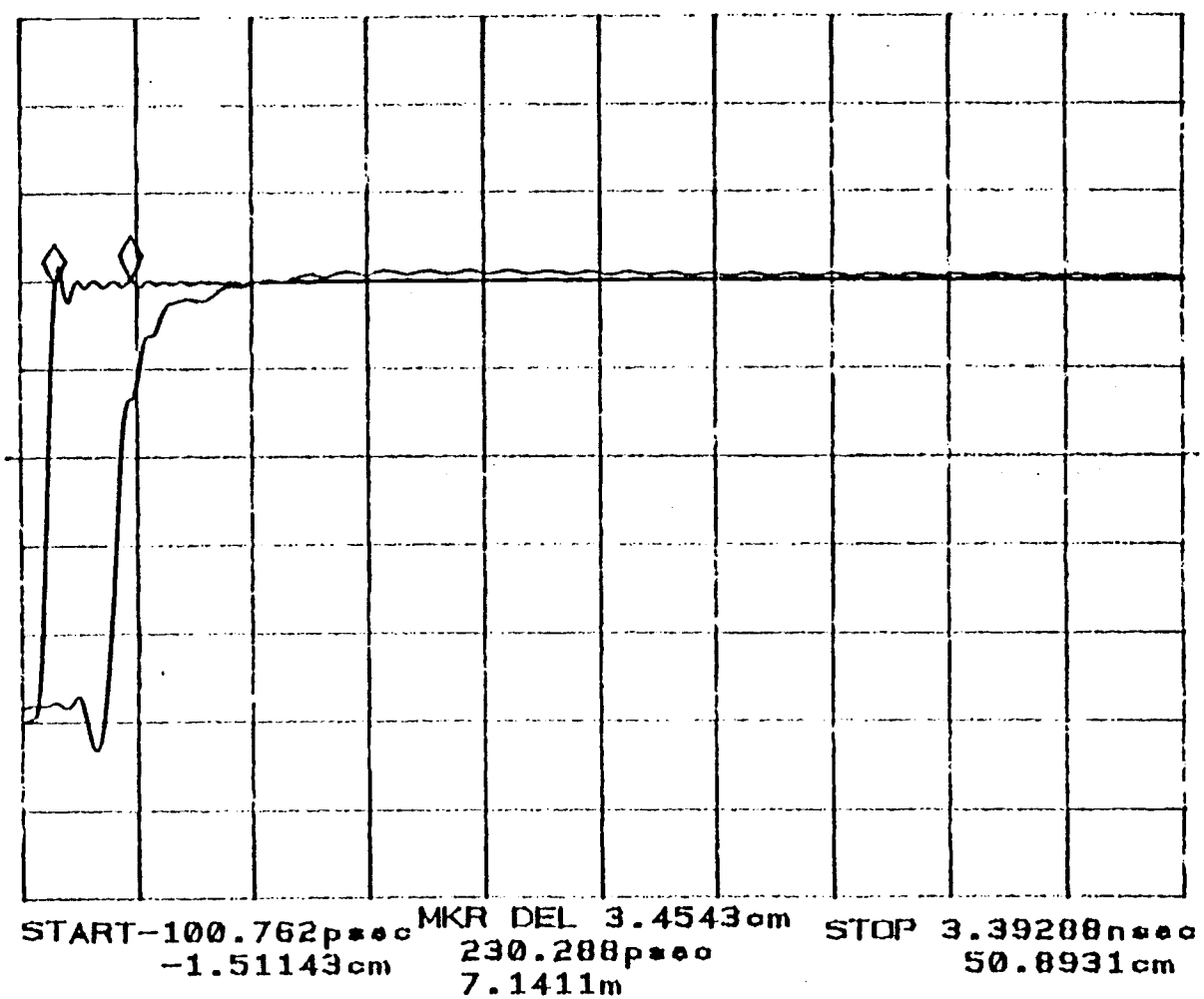


Figure 20. TDR of open circuit line

c/2.5, c being the velocity of light in a vacuum, due to the higher dielectric constant of the saphire substrate. This gives an effective length of

$$l=(c/2.5)*t = (c/2.5)*(115\ ps) = 1.38\ cm$$

This is a full wavelength at

$$f= (c/2.5)/l = 8.6\ GHz$$

which is close to the measured radiation frequency. Furthermore, an isolation test between the open line and a pickup loop showed maximum coupling at the expected radiation frequency, as shown in Figure 21.

Due to this radiation, when using the transmission line to calibrate the network analyzer for measurement of the transistor section, data taken at 8 GHz will be invalid. However, this is far outside the frequency range of interest.

As Figure 19 shows, the load has very low return loss (greater than 30 dB) to 4 GHz. This indicates that it will make a good reference load for the purpose of measuring the return loss of the transistor.

Effects of the Transmission Line Section

With these structures, a major effect of the transmission line can be identified. Figure 22 shows the S11 of the microstrip transmission line open with the input blocking capacitor, C1, in place. A measurement of the same structure, with C1 removed, and a ribbon conductor of the same width as the transmission line placed across the connection pads, is shown in Figure 23. Note that the line looks like it is less lossy, i.e., a better transmission line. The study of the effect of the input blocking capacitor, and the elimination of

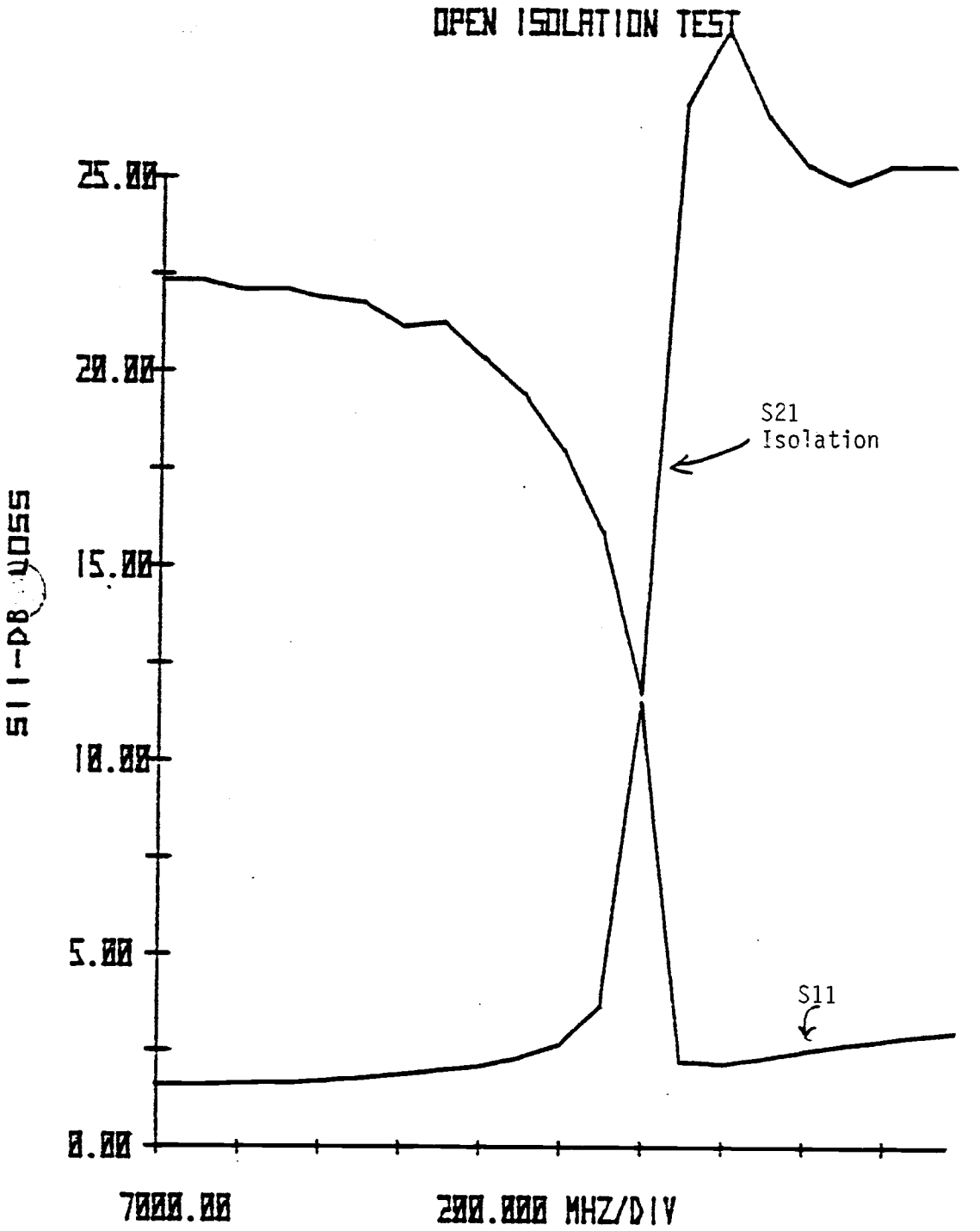


Figure 21. Isolation test of open circuit

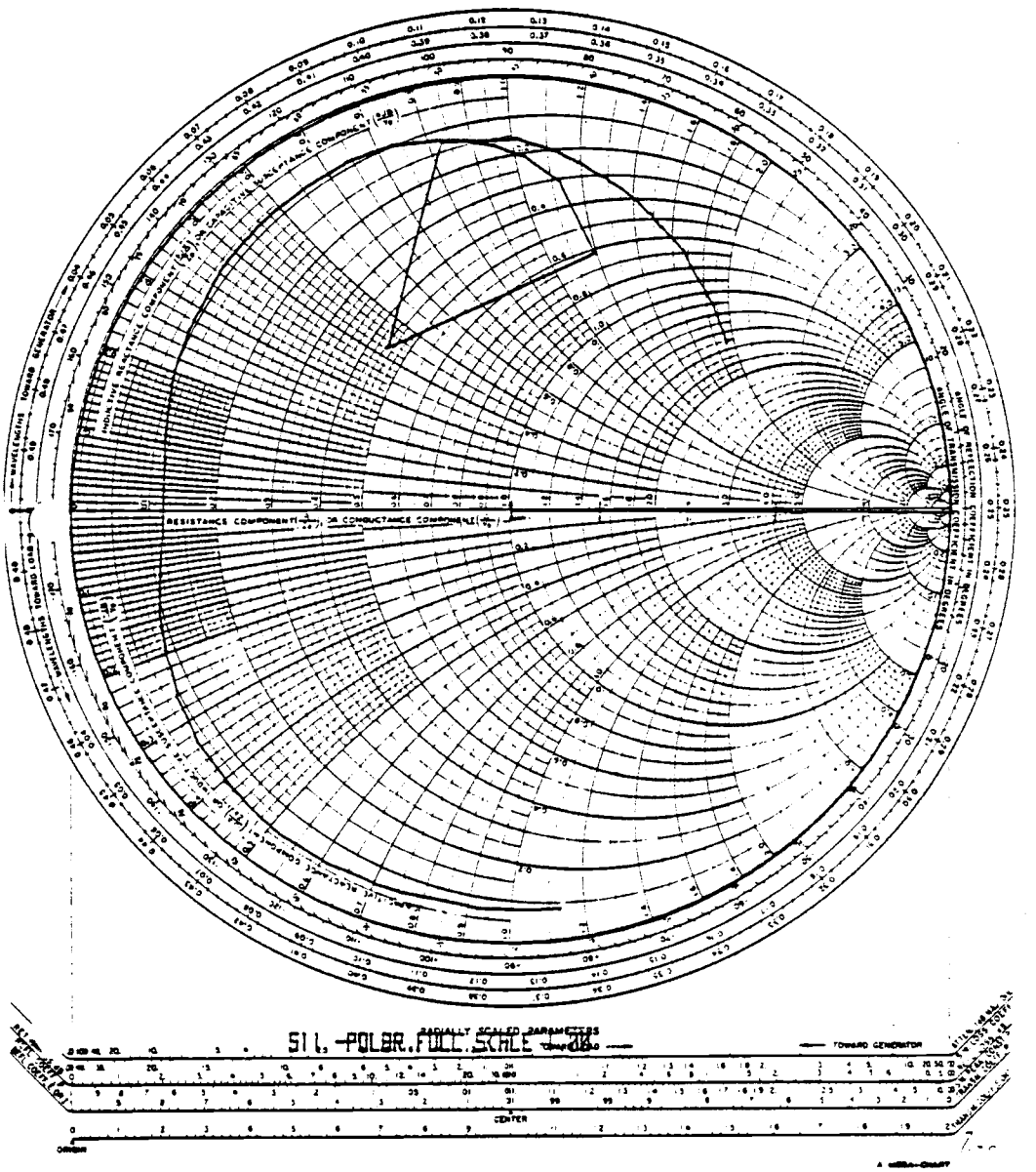


Figure 22. S11 of open line with capacitor

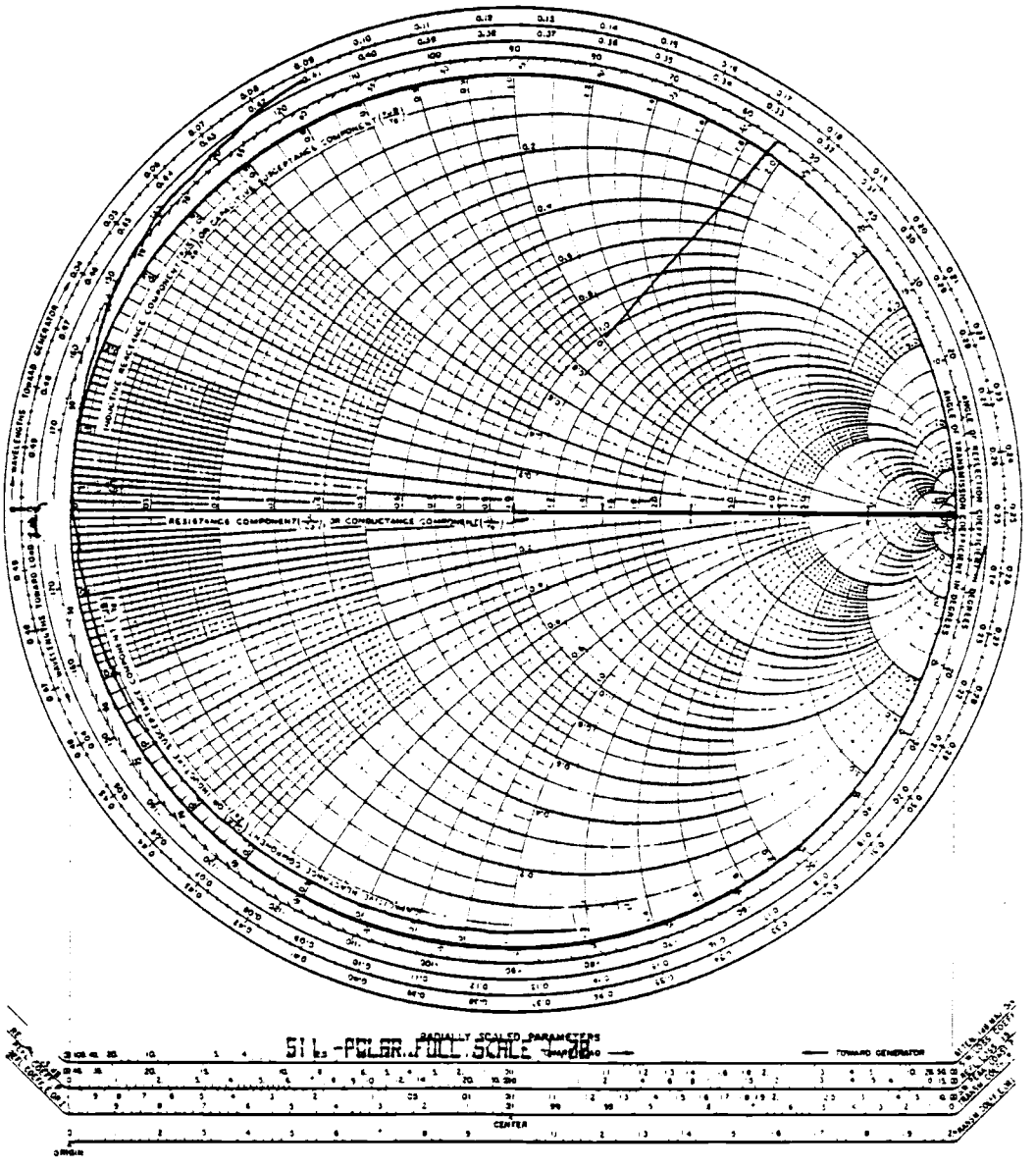


Figure 23. S11 of open line without capacitor

that effect, will be discussed in detail later.

Also note the rotation of the S11 plot. The fact that it rotates just over halfway around the Smith chart confirms that the length of the transmission line is just over ½ wavelength at 10 GHz.

MEASUREMENT OF THE TRANSISTOR SECTION

With the micro strip open, short, and load in hand, the automatic network analyzer is calibrated with the reference plane nearer the actual input of the common base amplifier. The initial measurement, Figures 15 and 16, showed a swinging about the center of the Smith chart, with much of the trace in the lower or "capacitive" section of the chart. At first glance, this might seem reasonable, as parasitic capacitance is often the source of high frequency circuit degradation. With the reference plane of measurement nearer the transistor, the impedance transforming effect of the input transmission line is eliminated, along with the error due to the input blocking capacitor. The input blocking capacitor and other discontinuities associated with the SMA to micro strip bond, etc., are calibrated out when the micro strip open, short, and load are used for calibration. This gives a truer picture of what is happening in the transistor section of the amplifier. The S11 measurement of the amplifier, "calibrated at the transistor," is shown in Figure 24. Notice that the magnitude at various frequencies is about the same, but the phase angle has changed, indicating the elimination of the transmission line effect.

With this new picture of the input impedance, the return loss indicates the impedance following a locus of decreasing real part and increasing imaginary part, implying the existence of a real part which

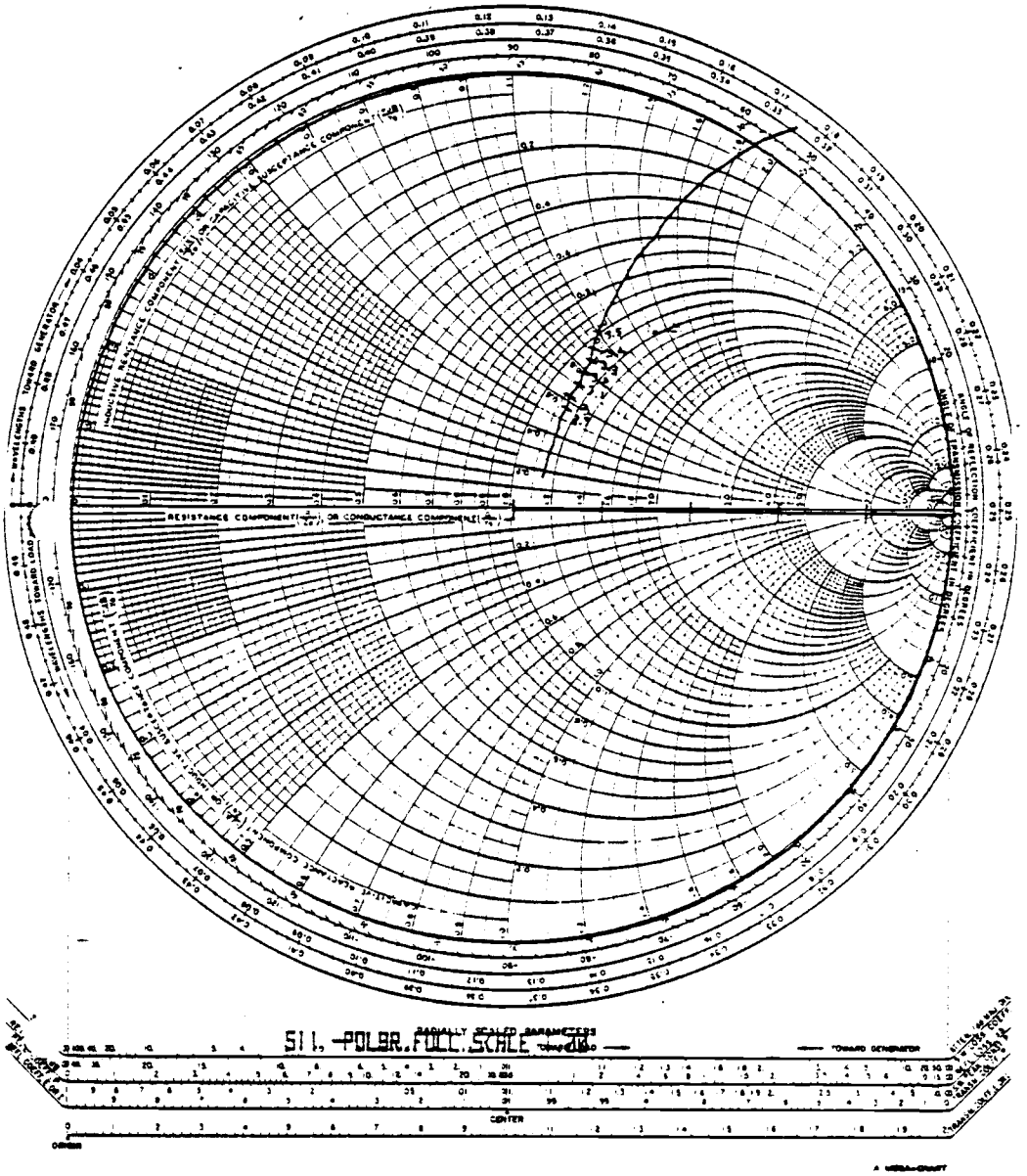
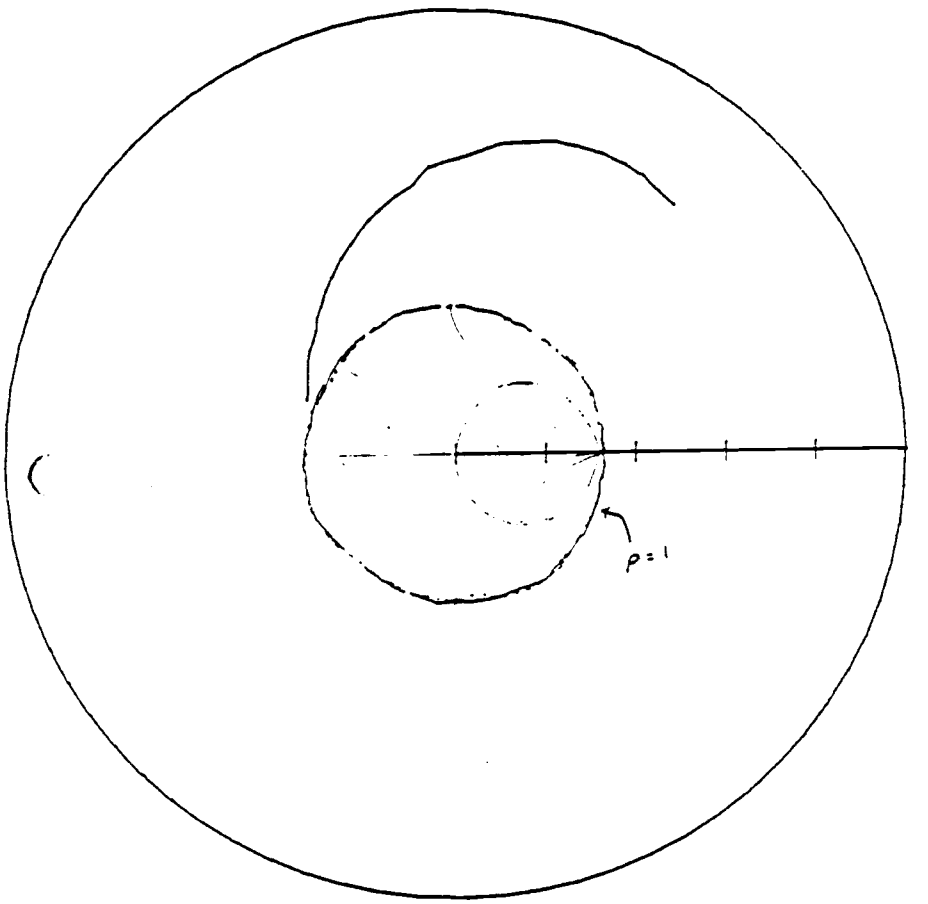


Figure 24. S11 of amplifier calibrated at transistor

becomes smaller with increasing frequency (in fact, going negative where S11 goes outside the unit circle), and an inductance term which is fairly constant. The input resistive term of the transistor (around 1 or 2 ohms), may be masked by the large 49 ohm resistor in series with the emitter of the transistor. This resistor is a thin film resistor on the saphire substrate. Strapping the resistor with a conductive ribbon of the same width as the transmission line, as was done for the reference open and short (the load used the 49 ohm resistor strapped to ground), eliminates the effect of the resistor in measuring the input impedance of the common base transistor.

A measurement of S11 for the transistor without the input matching resistor is shown in Figure 25; note that S11 goes outside the unit circle over the entire range of frequencies tested. The negative real part observed indicates that with improper matching, oscillation may take place. In fact, this common base configuration is the basis of many microwave oscillator circuits.



S11 -POLAR FULL SCALE 3.00

Figure 25. S11 of amp calib. at xstr w/o 50 ohms

CHAPTER 4

ANALYSIS OF THE COMMON BASE CIRCUIT

INPUT IMPEDANCE OF THE COMMON BASE AMPLIFIER

To evaluate properly what parasitics are affecting the amplifier operation, a detailed knowledge of the common base circuit is necessary. The analysis of the common base configuration requires a small circuit model of the transistor. Starting with the hybrid π model, and following Gray (3), the hybrid T circuit shown in Figure 26 is obtained.

In this configuration, r_e is α/gm, C_π has its usual meaning and the product r_eC_π has the value $\alpha/2\pi F_T$. F_T is an easily measured quantity, and is found by measuring β as a function of frequency for a common emitter circuit; the frequency at which $\beta(jw)$ equals 1 is defined as F_T. The collecter to emitter resistance, r_o is Va/V_Tgm where Va is the early voltage and $V_T=kT/q$; r_o is usually quite large (>50 k ohm). The collector to base resistance, r_μ, is greater than βr_o. The parasitic capacitance Cce is very small and is almost always neglected. The collector to base capacitance, C_μ, is not as small, but in common base circuits, it not multiplied by the Miller effect and has little effect on the input impedance.

In addition to the usual hybrid π elements, the parasitic elements in the base are added. These elements are shown as R_{bb} and L_{bb}. R_{bb} is predominantly internal to the device, and is the effective resistance of the silicon along the base. L_{bb} is primarily due to the inductance of the base lead to ground. The emitter contact inductance and resistance can simply be added in series with the Zin found.

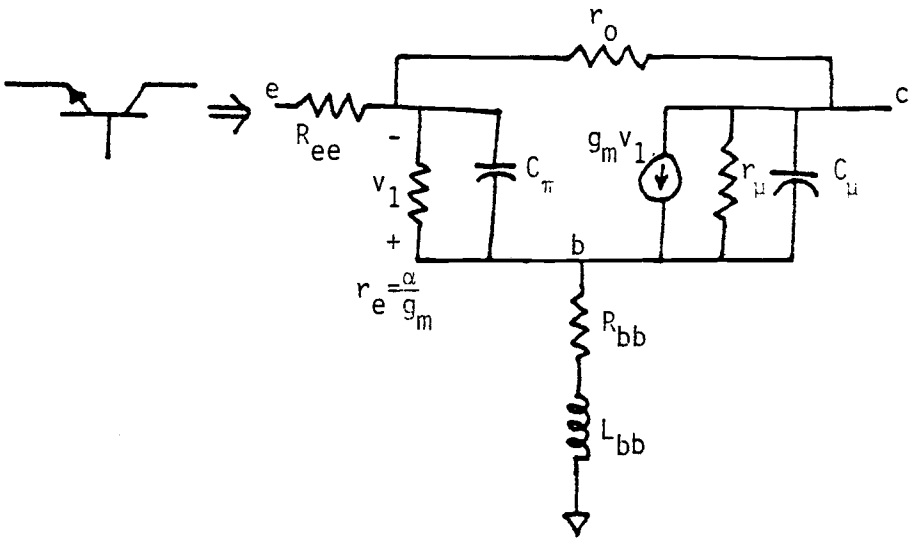


Figure 26. Hybrid T common base circuit

The circuit could be analyzed for input impedance on a computer, but this would not give an insight into the effects of various elements. For simplicity, in the hand analysis, the effects of r_o, Cce, r_μ and C_μ are neglected. These can be added in the computer model to see if significant once the hand analysis is complete.

The input impedance is

$$Zin = Z_\pi + Z_{bb} - g_m \cdot Z_\pi \cdot Z_{bb} \qquad \text{(eqn 1)}$$

where $Z_\pi = r_e \quad 1/jwC_\pi$ and $Z_{bb} = R_{bb} + jwL_{bb}$

evaluating this gives

$$Z_{IN} = \left\{R_{bb}\left[1 - \frac{\alpha}{1+(\alpha F/F_T)^2}\right] - L_{bb}\left[\alpha^2(F/F_T)/(1+(\alpha F/F_T)^2\right] + \frac{\alpha/g_m}{1+(\alpha F/F_T)^2}\right\} + j\left\{\omega L_{bb}\left[1 - \frac{\alpha}{1+(\alpha F/F_T)^2}\right] + R_{bb}\left[\frac{\alpha^2(F/F_T)}{1+(\alpha F/F_T)^2}\right] - \frac{\alpha/g_m(F/F_T)}{1+(\alpha F/F_T)^2}\right\} \qquad \text{(eqn 2)}$$

which can be simplified by defining $D=\alpha/(1+(\alpha F/F_T)^2)$, where α is the low frequence collector to emitter current gain, and F_T is as defined earlier to get

$$Z_{IN} = [R_{bb}(1-D) + (1/g_m)D - \omega L_{bb}(\alpha F/F_T)D] + j[\omega L_{bb}(1-D) + R_{bb}(\alpha F/F_T) - 1/g_m(\alpha F/F_T)D] \qquad \text{(eqn 3)}$$

If α is about 1, the value of D is about α at low frequency and $\alpha/2$ at F_T.

From equation 3 the effects of the parasitic elements as a function of frequency can be identified. At low frequency, $1-D=1/\beta$ so R_{bb} in the real part and jwL_{bb} in the imaginary part are reduced by β, as one might expect. The equivalent input impedance is approx-

imately $(1/g_m)D$.

As frequency is increased, R_{bb} and wL_{bb} become more significant. At F_T, the real and imaginary parts become

$$Re[Zin(wt)] = R_{bb}/2 + (1/g_m - wtL_{bb})/2$$

$$Im[Zin(wt)] = R_{bb}/2 - (1/g_m - wtL_{bb})/2$$

Here R_{bb} and wtL_{bb} (X_{bb} at $w = w_T$) are as significant as $1/g_m$.

Another way to write the input impedance is

$$Z_{IN} = [(1/g_m)D + f^2 \cdot D(R_{bb} - \omega_T L_{bb})] + j[\omega_T L_{bb} \cdot f^3 \cdot D + (R_{bb} - 1/g_m) f \cdot D] \qquad \text{(eqn 4)}$$

where f is the normalized frequency F/F_T; D is, as before, 1/1+f ; and wtL_{bb} is the reactance of L_{bb} at frequency wt. Note here that α is assumed to be unity. The method for finding values for R_{bb}, L_{bb} and $1/g_m$ is to measure S11 of the common base transistor, then at some choice of frequency, initial values may be calculated. By plotting curves of Zin against the measured device, best fit values for R_{bb} and L_{bb} for all frequencies may be found.

SMALL SIGNAL MODEL FOR THE TC 21 TRANSISTOR

Measurements were obtained from the HP Technology Center for the TC 21 transistor; the transistor used in the 8754 input amplifier. The measurements were made at bias conditions of Vce = 15 volts and Ic = 15 mA. This gives $1/g_m$ = Vt/15mA = 1.7 ohms. At the lowest frequency measured, the real part of Zin is 2.688 ohms; calculated as an average of the three wafers. The difference between Re[Zin] and $1/g_m$ might be associated with a contact resistance, Ree, in the emitter; a value of Ree = (Re[Zin] - $1/g_m$) = 1 ohm is reasonable. At a high frequency, $F = F_T$, then f = 1 and Zin becomes

$$R_{bb}/2 - wtL_{bb}/2 = Re[Zin]-Ree-(1/g_m)/2 \qquad \text{(eqn 5)}$$

$$R_{bb}/2 + wtL_{bb}/2 = Im[Zin] + (1/g_m)/2 \qquad \text{(eqn 6)}$$

Averaged over the three wafers measured, Zin = 5.921 + j 6.054. Adding equation 5 and equation 6 gives R_{bb} = 12.0 ohms. Subtracting equation 6 from equation 5 gives wtL_{bb} = 2.453 ohms, or L_{bb} = 0.88 nH. Figure 27 shows a plot of the average of the three measurements, and the curve generated by equation 4. The values of Zin given by equation 3 follow closely with the measurements.

To confirm that the analysis was done correctly, the small signal model is analyzed by OPNODE, and plotted along with the values obtained by equation 3. Figure 28 shows that, indeed, the values obtained by euqation 3 fall exactly on the S11 locus generated by OPNODE.

The analysis assumes that the effects of r_o, C_{ce}, R_μ, and C_μ were negligible. These elements can be added to the small signal model used by OPNODE, and their effects seen. The small signal analysis is repeated using r_o = 100 k ohms, C_{ce} = .09pF, r_μ = 10 M ohms, and C_μ = .18pF (these are typical values), and is shown in Figure 29, along with the curve in which the effects of the above parasitics were neglected. The overall S11 was changed very little, less than 2 percent change for frequencies below the F_T of the device; from the figure, it is difficult to see any change.

COMPARISON IN CIRCUIT

The transistor can be placed in the circuit in which it will be used, and the effects of that circuit on its input impedance can be determined. The measured S11 looking directly into the emitter of the transistor, shown in figure 25, is completely outside the unit

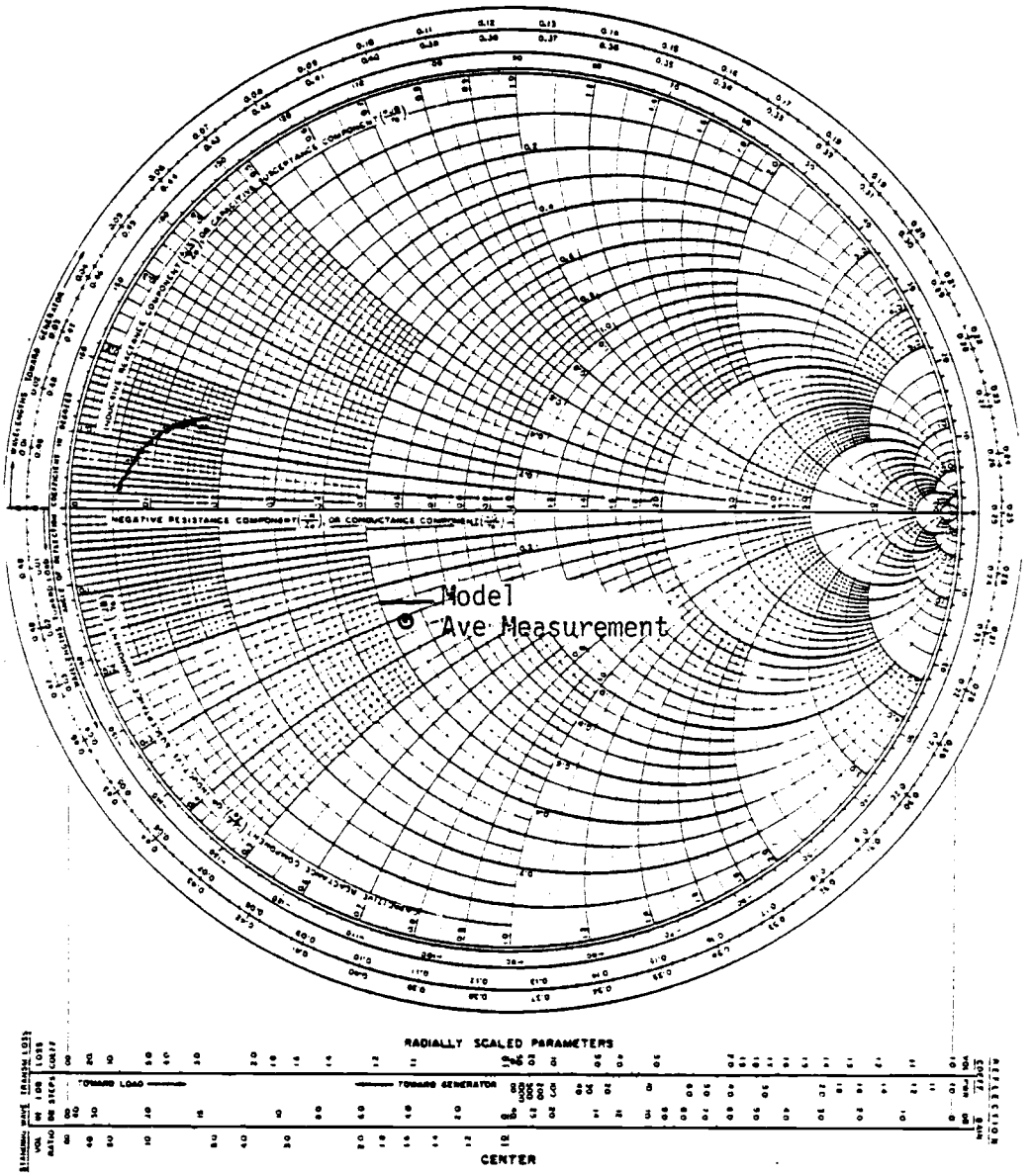


Figure 27. Hand analysis of TC 21 vs. meas.

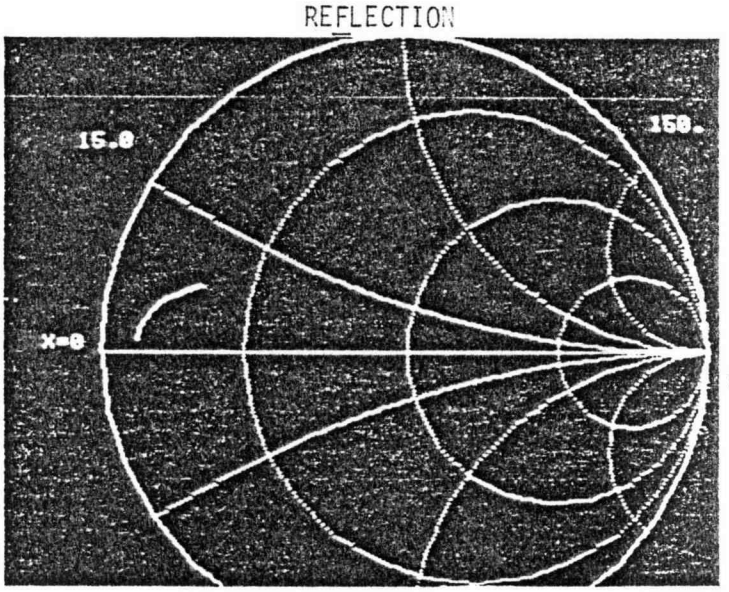


Figure 28. Simulation of TC 21

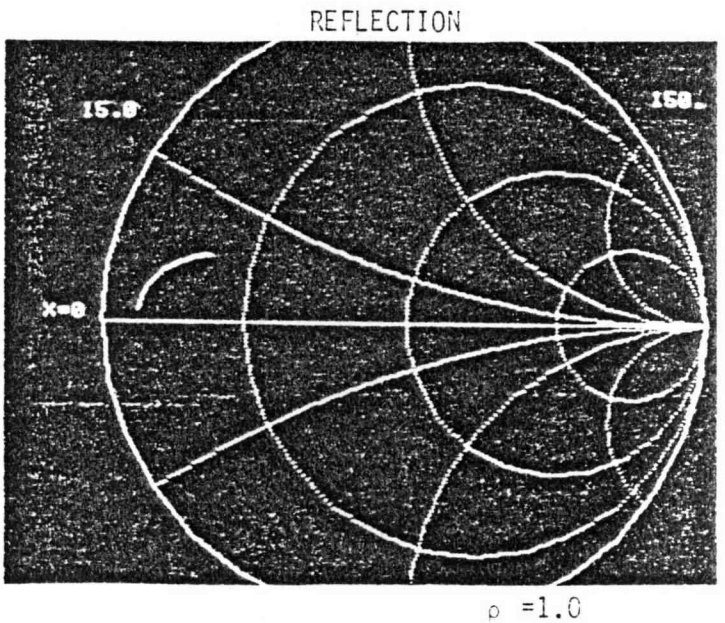


Figure 29. Simulation of TC 21 with parasitics

circle. This implies the input impedance has a negative real part. With the analysis of the common base transistor available from equations 1 through 4, the input reflection measured can be explained.

In equation 3, the only negative real term is associated with the base inductance L_{bb}. Also, the reactive part of S11 extends farther around the unit circle which indicates a larger positive or "inductive" reactance. This increase can be associated with the inductance of the base connection. Using the techniques of the last section, a value of input inductance in this configuration of 3.65 nH was obtained. Some of this can be associated with the emitter inductance. By using computer modeling, about .7 nH of inductance was associated with the emitter, and about .9 nH inductance is associated with the base.

The measurement of the transistors, taken at HP Technology Center, utilized special test structures that were calibrated in such a way that L_{bb} and any emitter inductance were very small. When placed in the circuit to be used, L_{bb} (the inductance of the base to ground connection) is much larger. Figure 30 shows the physical connection of the transistor to the rest of the circuit.

MATCHING COMPONENTS

To match the low impedance of the common base amplifier to a 50 ohm system, a 49 ohm matching resistor was used. This tends to mask the real part of the input impedance, but will have no effect on the imaginary part. This is shown in Figure 24. Note that at low frequencies, the curve is inside the 50 ohm constant resistance circle, indicating a low frequency real part greater than 50 ohms since the 49 ohm resistor is too large for a perfect match. As fre-

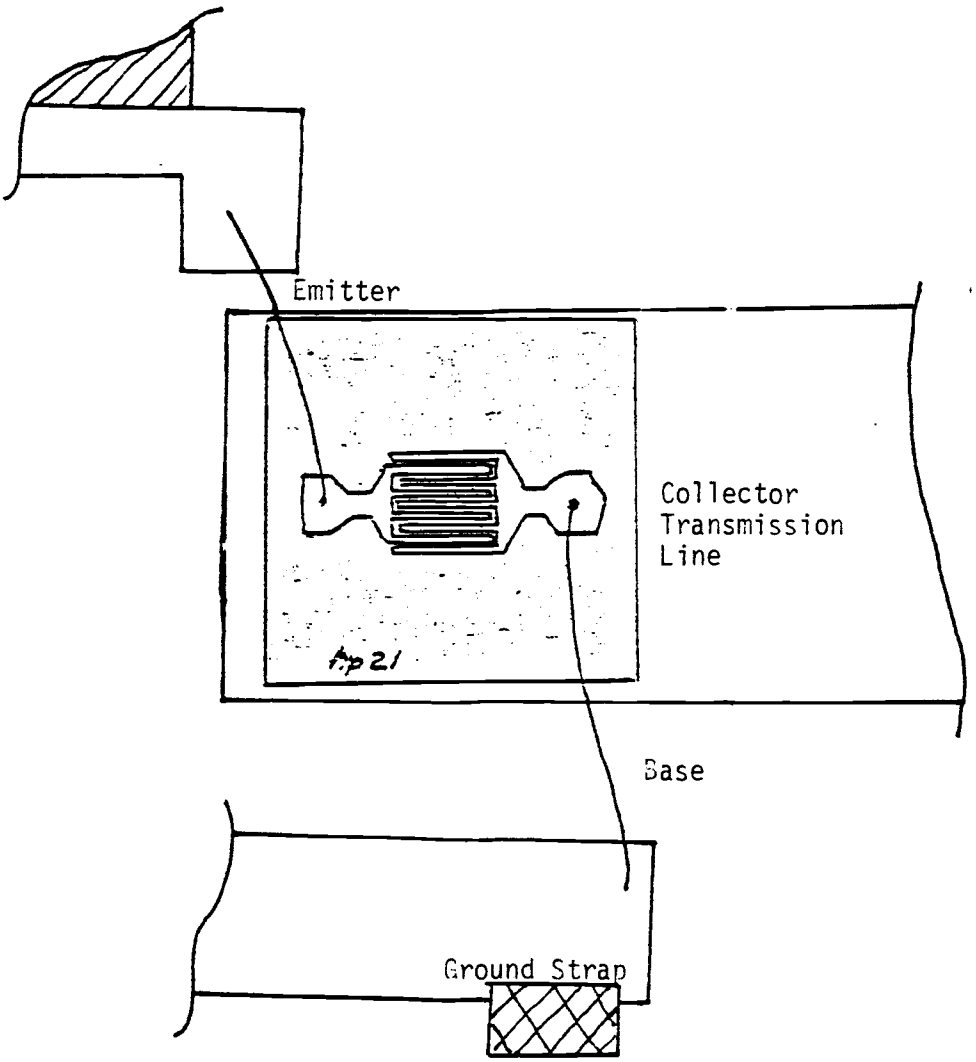


Figure 30. Physical connection of TC 21

increases, the real part becomes less, as expected.

The real part does not vary much; it is about 55 ohms at 3 GHz, and the imaginary part is about 30 ohms. At 3.5 GHz, the real part has decreased to just 50 ohms, but the imaginary part has increased by 20 ohms to 50 ohms. It is clear that to improve the return loss, the effect of the imaginary part of the input impedance will need to be reduced.

Compensating Capacitor

If a negative imaginary term could be added to the input impedance, then it might be possible to correct for some of the positive (inductive) reactance. In a special version of the 8754 amplifier, a capacitor was added in parallel with the 49 ohm matching resistor. This gives an effective matching impedance of

$$Zm = R/[1 + (wRC)2] - jwR2C/[1 + (wRC)2]$$

Note that this will reduce Rm (the effective matching resistance), but will also give a negative imaginary term. The value of the negative imaginary term can be manipulated to best correct for the positive term.

Figure 31 shows S11 for the circuit with a .22pf compensating capacitor added; a 3 GHz the imaginary part is 10.6 ohms.

This method of compensation can cause the imaginary part of Zin to go negative at low frequencies, degrading the low end response. In addition, the circuit does not meet the specifications, even with the compensating capacitor.

The problems in the transistor section have been identified. The final design, which will account for these problems, will be discussed later.

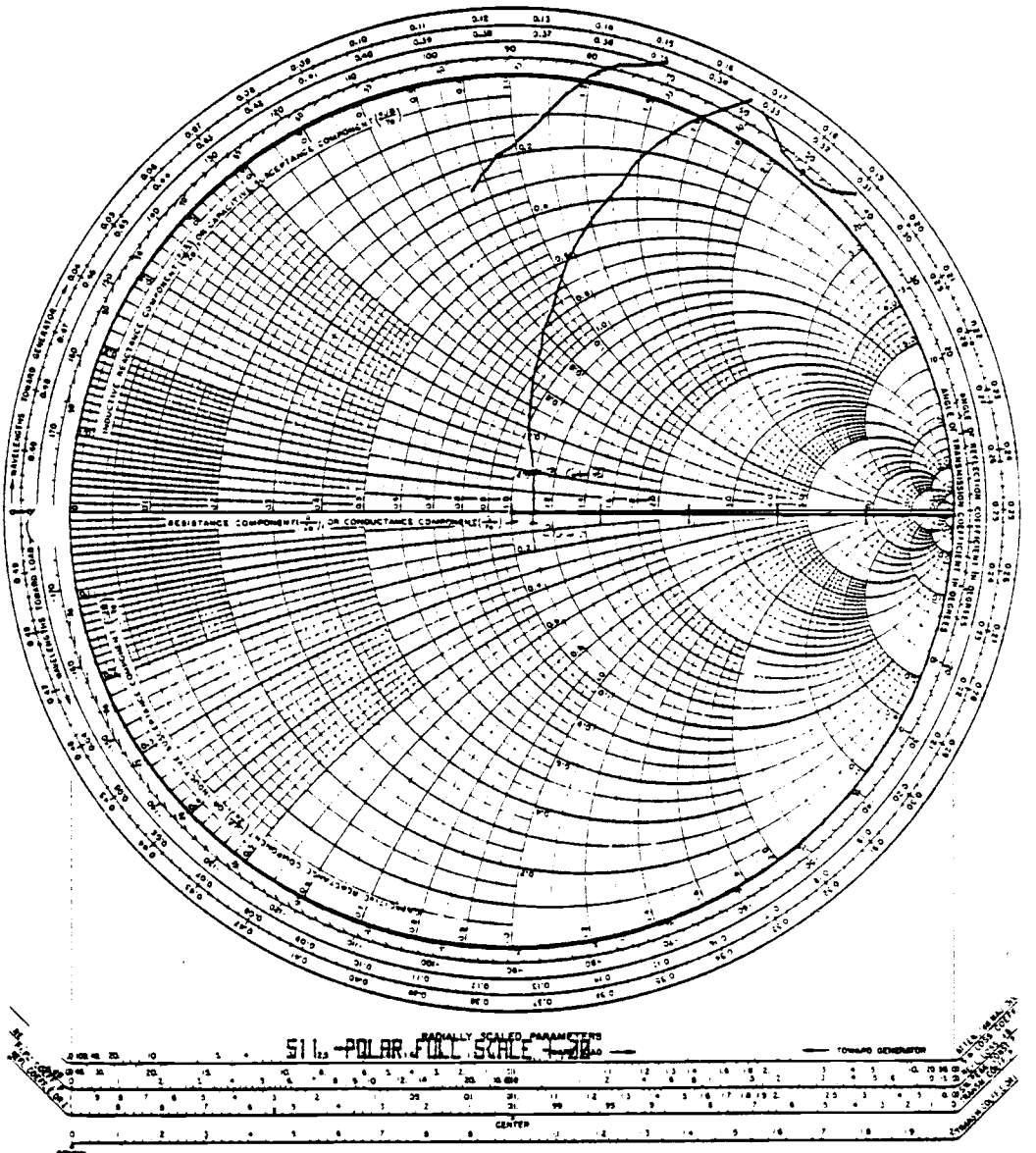


Figure 31. S11 of TC 21 amplifier with .22 pF compensating capacitor

CHAPTER 5

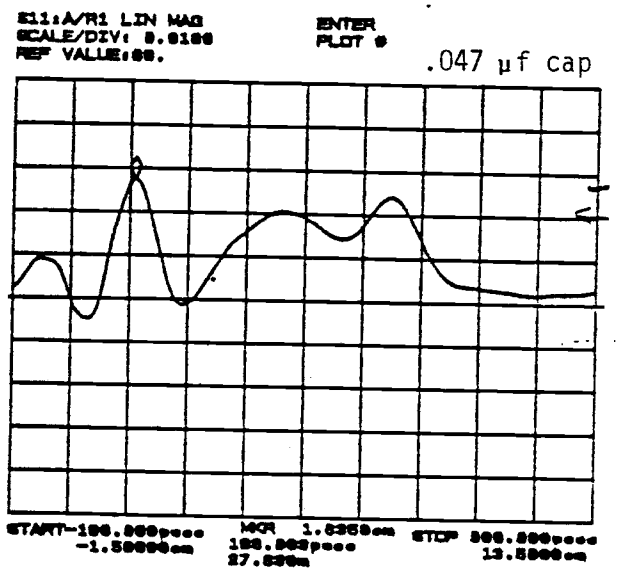
ANALYSIS OF INPUT LINE & PACKAGING

Besides reflections due to a mismatch at the transistor, reflections due to mismatched packaging and transmission line structures may result in a degradation of return loss.

INPUT BLOCKING CAPACITOR

One primary area of mismatch may occur at the input blocking capacitor. This capacitor is necessary to prevent a DC input signal from interfering with the bias of the common base circuit. The capacitor must have a minimum value based on the low frequency return loss. The low frequency return loss is $1/(j100\omega C + 1)$, which must be greater than 22 dB at 100 kHz, and greater 28 dB above 500 kHz. This puts a minimum value on C, the blocking capacitor of .200 μF.

The parasitics involved with the blocking capacitor are stray capacitance to ground, and series inductance. These will cause a degradation at high frequencies. If the capacitor is simply placed on the saphire micro-strip transmission line, as is done in the 8754 amplifier, it can be modeled as a transmission line whose impedance is determined by the series inductance and stray capacitance. Several capacitors were measured on test structures; for capacitors of width similar to the transmission line, the impedance could be varied by changing the stray capacitance to ground. This is done by removing the saphire substrate beneath the capacitor, thus lowering the dielectric constant between the capacitor and ground. A .047 μF mono-block capacitor of the same dimension as the micro-strip line (25 mil) was tested. Figure 32 shows a TDR of the line with the cap-

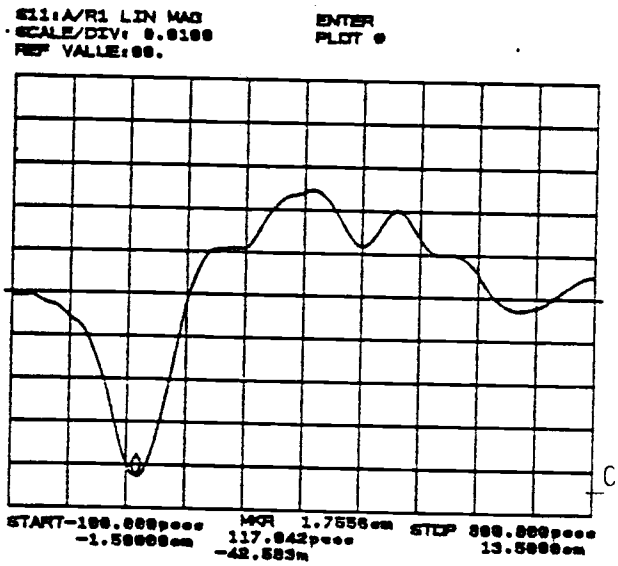


.047 µf cap

≃ 53 Ω

Inductive

Microstrip with holes



≃ 46 Ω

Capacitive

Microstrip without holes

Figure 32. TDR of micro-strip line with cap

acitor placed on it, with and without a hole under the capacitor. With a hole, the line is about 53 ohms, too inductive; without the hole, the line is about 46 ohms, too capacitive. For larger value capacitors (i.e., bigger bodies), the line is always too capacitive. It is clear that a different approach is necessary to accomodate the .200 μF capacitor needed for low frequency return loss.

PACKAGING

The desired package is a low cost Tekform package. This package can be purchased for approximately 15 dollars, much cheaper than a manufactured package, which runs about 80 dollars. The package is shown in Figure 33, with its connections. The problem here is to make the PC board-to-Tekform pin-to-saphire transmission line as good a match as possible. The input connector for the instrument is an SMA connector. This is a coaxial connector. Making the transition to the PC stripline is another source of mismatch. Figure 34 shows the return loss and a TDR of the SMA to PC stripline and the Tekform pin connections. The return loss is greater than 30 dB to 3.5 gHz. The sources of mismatch are an inductive connection at the SMA, and an inductive connection at the Tekform pin. By removing these mismatches, the overall S11 of the circuit will be improved.

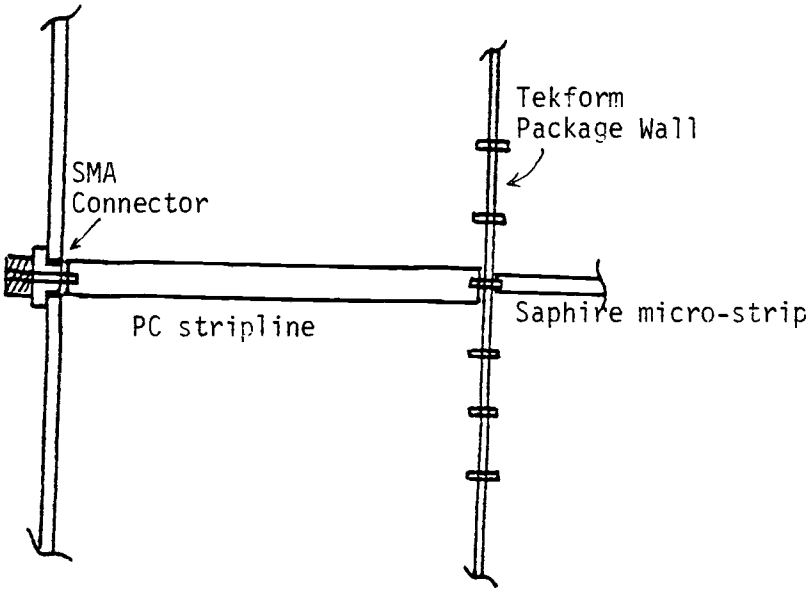


Figure 33. Tekform connections

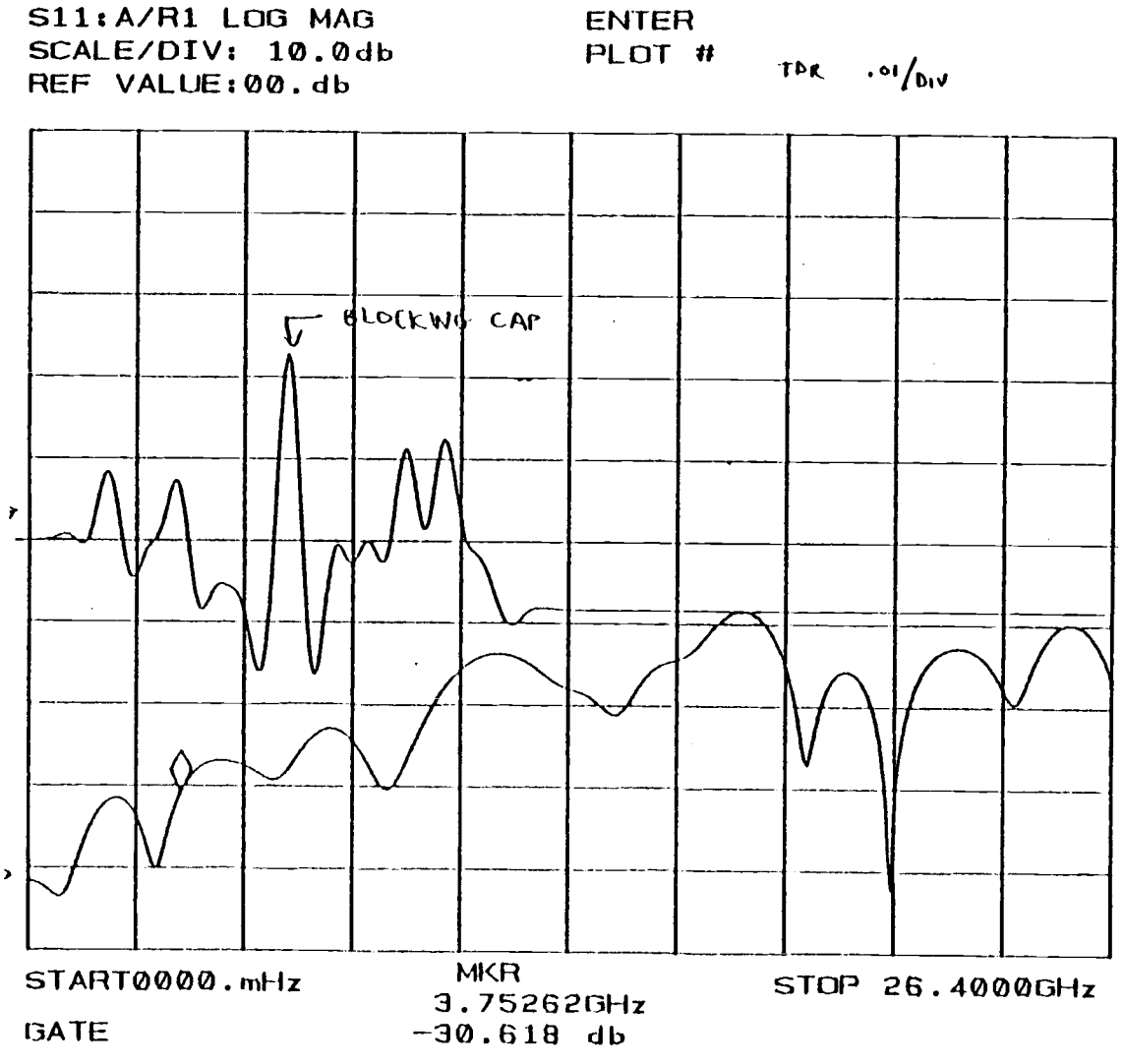


Figure 34. S11 and TDR of Tekform (initial ckt)

CHAPTER 6

DESIGNING INPUT LINE & PACKAGING

THE INPUT BLOCKING CAPACITOR

The main concern in the input section is to provide a large enough input blocking capacitor to meet the low end return loss. As noted in a previous section, a 50 ohm impedance cannot be maintained if a capacitor as large as required is placed on the saphire microstrip. To solve this problem, the input blocking capacitor is placed outside the package in the PC stripline. Since the PC board material is thicker, and has a lower dielectric constant than saphire, parasitic capacitance to ground is reduced. This allows a much larger capacitor to be used, while still maintaining a 50 ohm impedance. In this circuit, a .28 μF capacitor is used; this large value will allow the low frequency return loss specification to be met.

SMA TO PC STRIPLINE

To improve the input SMA concector to PC stripline transition, the parasitic inductive effect will need to be removed. This is done by reducing the diameter of the hole through with the connectors' center conductor passes. This increases its capacitance to ground, compensating for the large parasitic inductance.

TEKFORM PIN TRANSITION

Experimentation with this connection shows that the best match is obtained if the PC stripline is maintained at constant width throughout its length. In the past, it had been tapered at the end

near the Tekform pin, but this makes the transition inductive.

The transition from the Tekform pin to the saphire micro-strip was initially made by a .7 mil diameter wire bond. Such a transition is very inductive. The wire bond was replaced with a 15 mil ribbon, which improved the match. However, the transition was still inductive. To compensate for this, small pads were placed on the saphire, under the Tekform pin to increase the capacitance to ground. By making these pads' area total about 200 square mils, the best match was obtained.

FINAL PACKAGE DESIGN

The final design for the packaging is shown in Figure 35. The improvements led to a return loss better than 30 dB for the terminated line out past 3.5 GHz. Placing the blocking capacitor outside to the Tekform package allowed the use of a larger capacitor; this improved the low end return loss, shown in Figure 36, bringing it within specification.

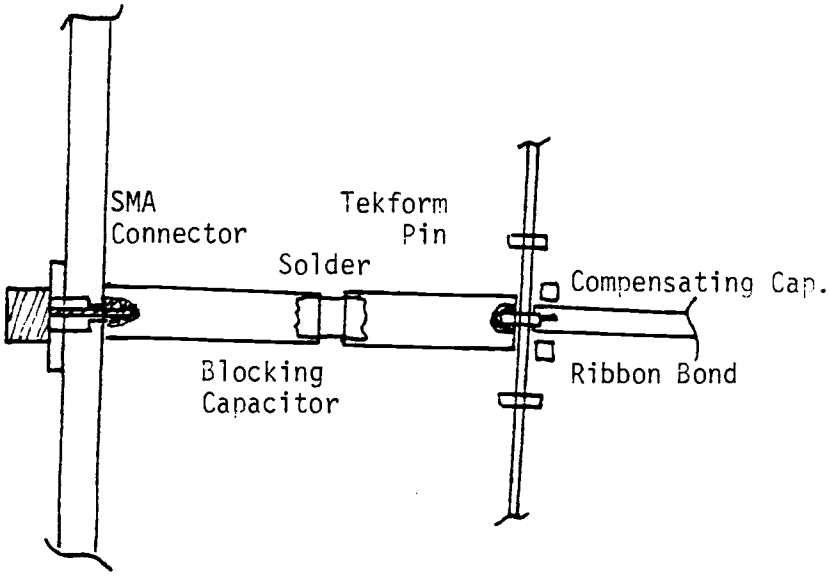


Figure 35. New package design layout

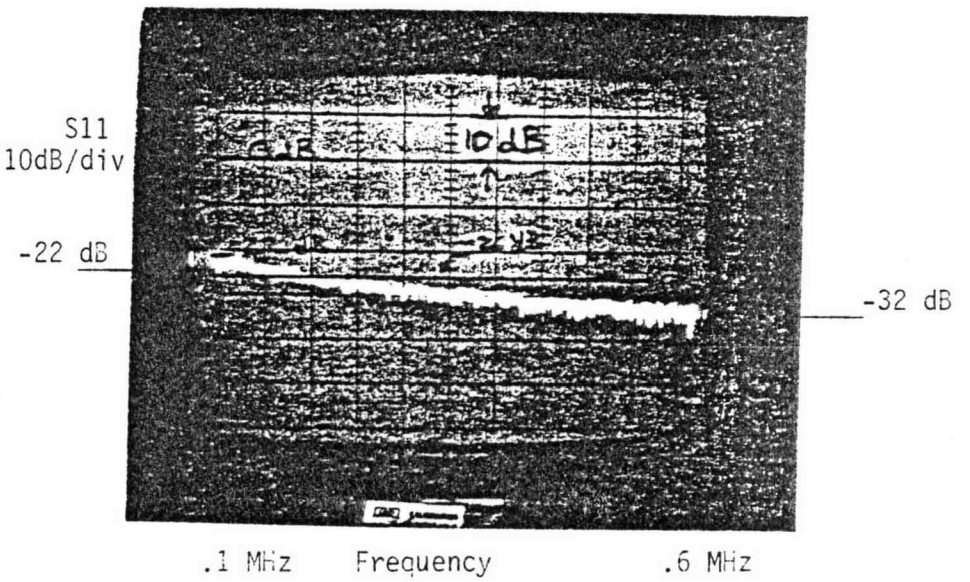


Figure 36. New package design return loss

CHAPTER 7

DESIGNING THE TRANSISTOR SECTION

To meet the high end return loss goal, the input match of the transistor section must be improved. Many of the problem areas were presented in the analysis section; the improvements of those areas are now presented.

CHOICE OF TRANSISTOR

Since the transistor is the main component in this amplifier, the choice of the transistor is important. The TC 21, which was used in the 8754 amplifier, does not meet the power gain saturation goal. A higher power alternative is the TC 16. The power gain saturation is shown in Figure 37; for 31 mA bias, the 10 dBm power gain saturation goal is achieved. The ability to bias this circuit at high power is due to balancing resistors in the emitter fingers which keep them from "hogging" current when hot. This resistance is typically about 3-5 ohms. The F_T of this device is about 4.5 GHz. The S-parameters of the TC 16 were provided by HP Technology Center. Using these in an OPNODE model, the values of base inductance, matching resistor, and matching capacitor can be manipulated to provide the best return loss response.

REDUCING THE BASE INDUCTANCE

A concentrated effort to reduce base inductance was made, as this appears to be a major source of mismatch. From the analysis, the value of base inductance was found to be .9 nH. Using this, with the 49 ohm resistor, gives the return loss shown in Figure 38. At

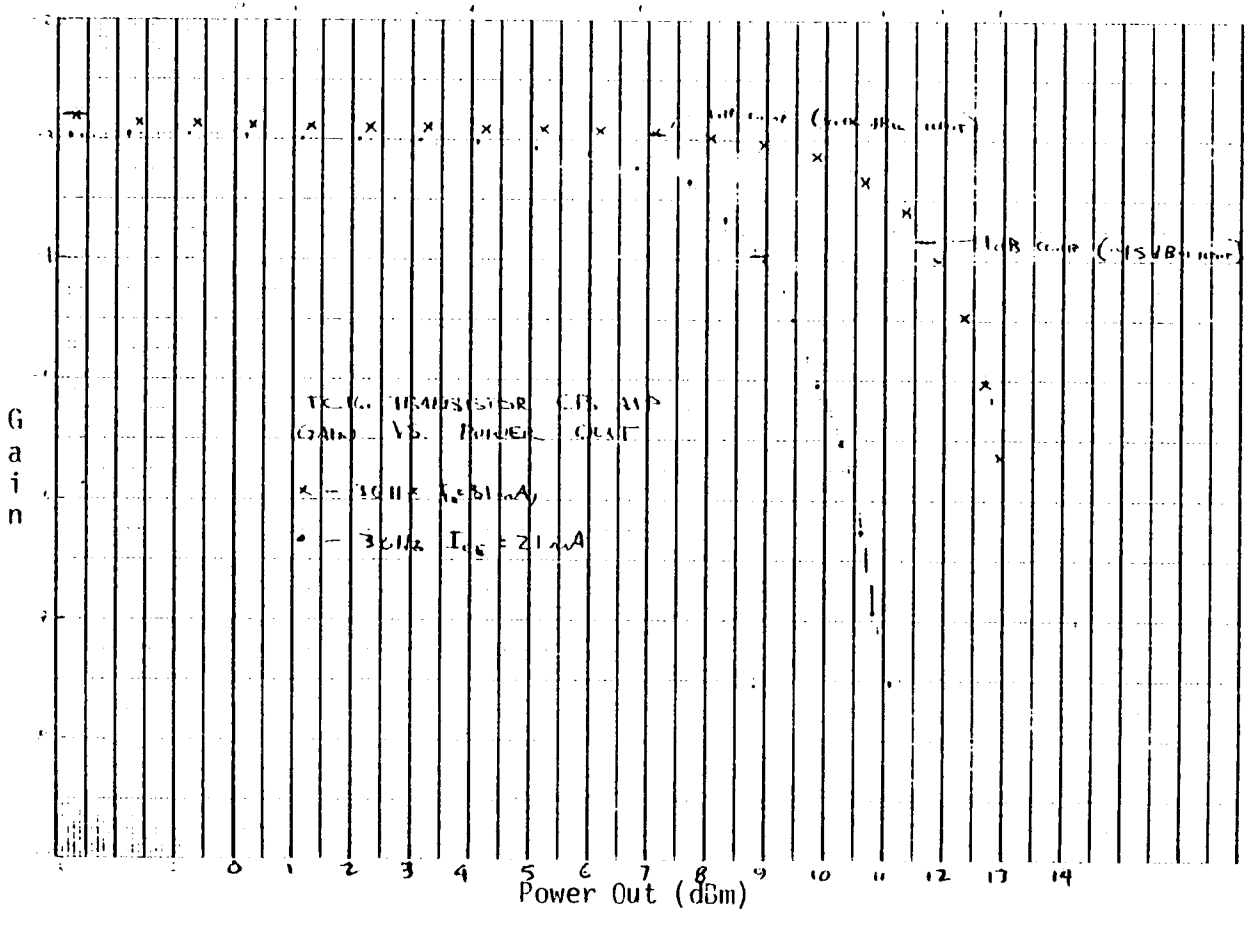


Figure 37. Power gain saturation of TC 16

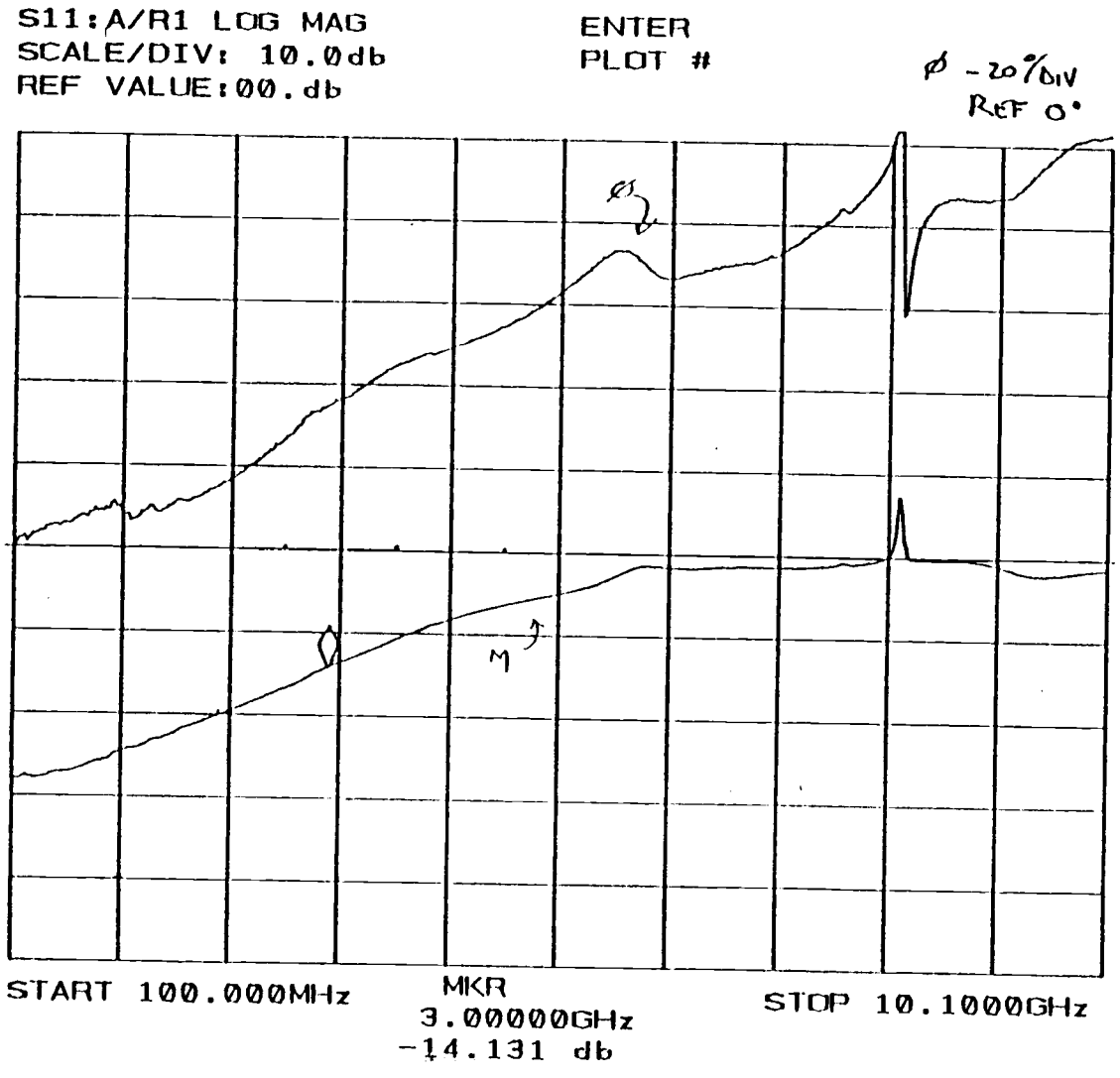


Figure 38. S11 of TC 16 amp (49 ohms, rect)

3 GHZ, the return loss is only 14 dB.

Both the matching resistor and the base inductance must be reduced. The matching resistor is something that is easily controlled, but since the base inductance is parasitic, it is much more difficult to reduce.

Initially, the base connection was altered by replacing the .7 mil bond wire with a wire mesh. This reduced the inductance some, but the primary cause of the large inductance is the length of the bond to the back side ground. To reduce this length, a conductive via is placed next to the transistor. A conductive via provides a signal path through the substrate. For the prototype it is a 25 mil hole with a ribbon bond through it to ground; in the final circuits, it will be plated through hole to the conductive ground plane. A second conductive via is placed on the other side of the transistor, and a wire mesh is stitch bonded from one conductive via, to the transistor base, then to the other conductive via.

This type of bonding configuration, done with .7 mil bond wire on thick film alumna circuits, has been measured to have as low as .2 nH inductance (4). Since the breadboard uses ribbon bond rather than plated through holes, the inductance might be expected to be higher.

From the data gathered, the inductance in the original circuit was about .9 nH. In this new configuration, the base inductance is much lower, on the order of .4 nH.

VALUES FOR MATCHING COMPONENTS

To give the best return loss response, the matching resistor and capacitor, (if needed), can be set to an optimum value. A 49 ohm

resistor was available on the substrate. If this is used, the resistance will be too high. The low frequency input resistance is found to be 5.4 ohms from a measurement of Zin with the low inductive base and no matching resistor. Adding the 49 ohm resistor makes the real part too large.

In previous measurements, the real part would tend to go negative because the real part depends on R_{bb}-wtL_{bb} and this is negative for large L_{bb}. As equation 4 shows, the R_{bb}-wtL_{bb} is multiplied by f^2, f being the normalized frequency F/F_T. By making L_{bb} smaller (so that R_{bb}-wtL_{bb} is a positive quantity) for frequencies below F_T, the real part will increase with frequency. This can be seen in Figure 39; both real and imaginary parts are increasing with frequency. At low frequency, the input impedance is 54.4 ohms, exactly 49 ohms more than the 5.4 ohms measured without the matching resistor.

Another reason why the real part may look like it is increasing is that the circuit with the matching resistor has a shorter effective transmission line (shorter even than the reference), thus rotating the measurement clockwise from the true impedance.

Values Used on Breadboard

For 50 ohm at low frequency, the matching resistor should be 44.6 ohms. The only way to reduce the value of the thin film resistor for the breadboard is to place a chip resistor in parallel with the thin film resistor. Using a 390 ohm resistor, the value the matching resistor becomes is 43.5 ohms. The total low frequency input resistance becomes 48.9 ohms. This is shown in a rectangular plot in Figure 40, and in polar form in Figure 41. Note that the resistance starts too small (viewing Figure 41), then gets larger,

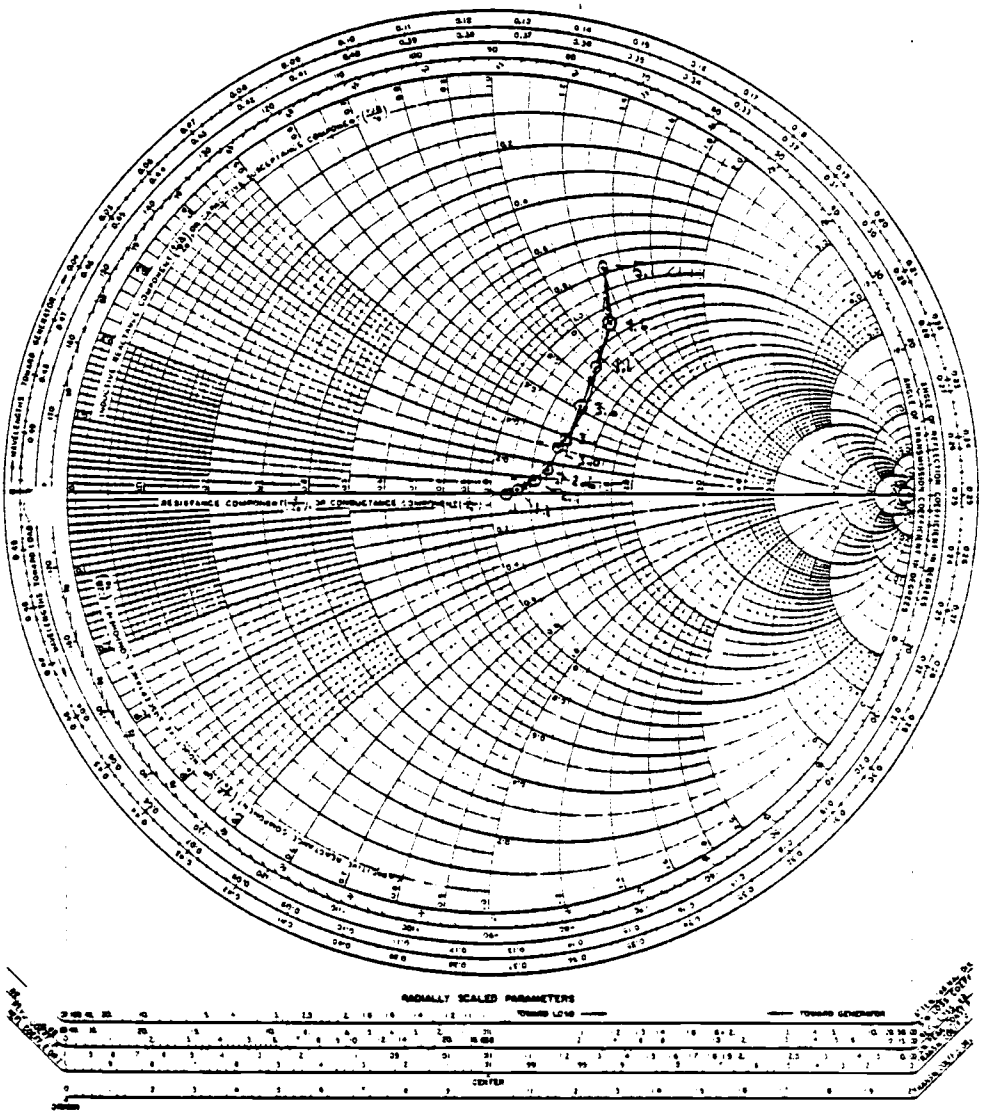


Figure 39. S11 of TC 16 amp (49 ohms, low L_{bb})

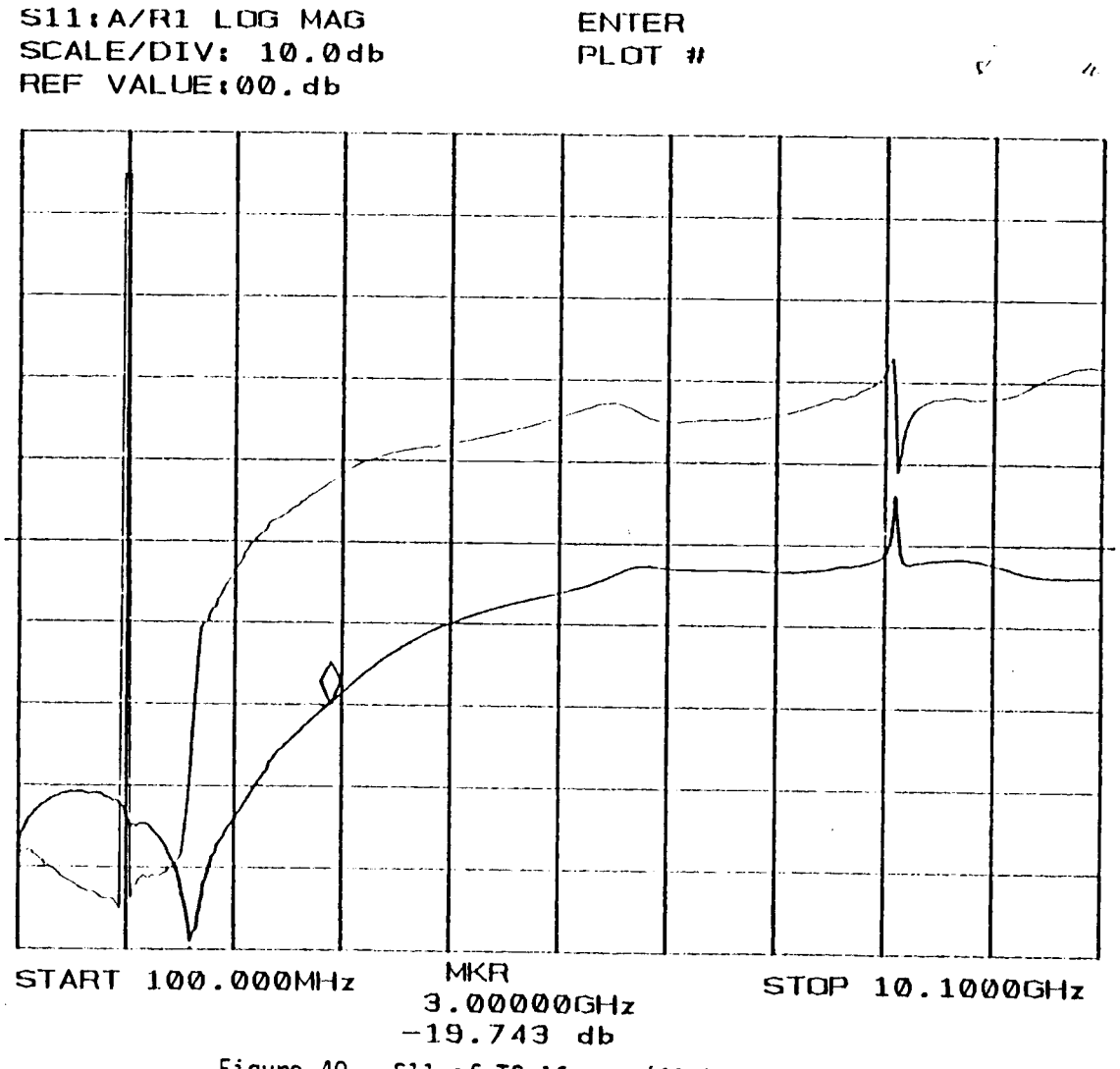


Figure 40. S11 of TC 16 amp (43.5 ohms, rect)

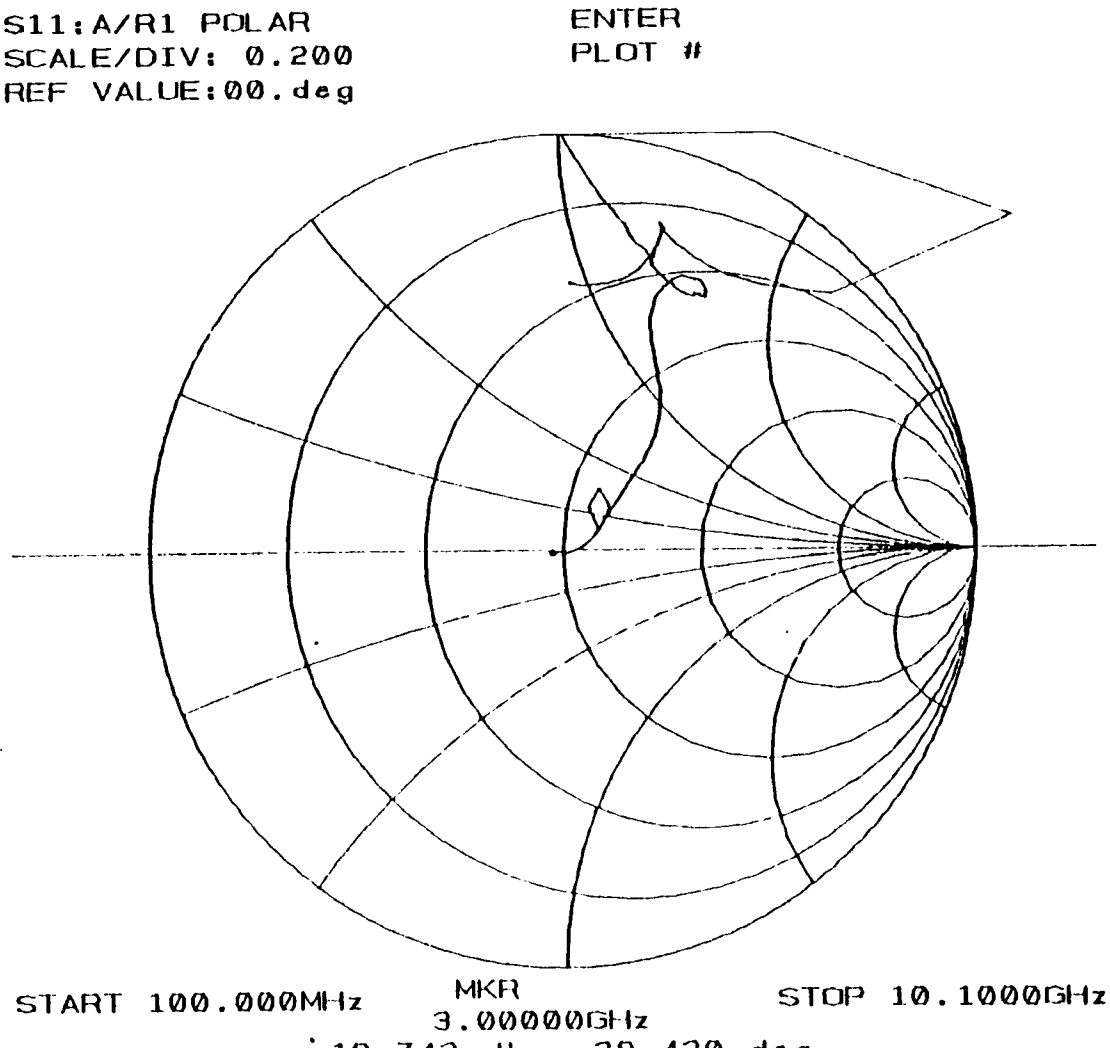


Figure 41. S11 of TC 16 amp (43.5 ohms, polar)

passing through exactly 50 ohms at (from Figure 40) about 1.76 GHz. This gives a circuit that nearly meets the desired specifications; at 3 GHz it is only 2.3 dB out of specification. This is a nine dB improvement from the 8754 amplifier measured.

Adding the proper value of compensating capacitor improves the return loss to meet specification. Currently, the compensating capacitor is a chip type capacitor which is connected across the matching resistor. In the original circuit in the 8754 amplifier, a .22 pF capacitor was used. In this subpicofarad range, the available values are .15 pF, .22 pF, and .33 pF.

The best response is when a .15 pF compensating capacitor is used. In Figure 42, the return loss is shown in rectangular form, and in Figure 43, the polar form is shown. This indicates that the return loss is about .7 dB better than specified in both the low and high frequency range. Note that the compensating capacitor causes the S11 locus to become capacitive at low frequencies, before the effects of the base inductance make S11 become inductive, this rotates the locus around the 50 ohm center.

Matching Values from OPNODE

For the new design, the value of the matching resistor and capacitor, which in a new thin film layout may be an interdigitated capacitor, can be set to an optimum value. One way to obtain these values is to use a computer analysis and optimization.

First, the model is obtained by using the information on the base and emitter inductances, and by adding parasitic capacitors and transmission lines to account for the effects of the connecting pads and input lines. Using a 43.5 ohm resistor for an initial value for

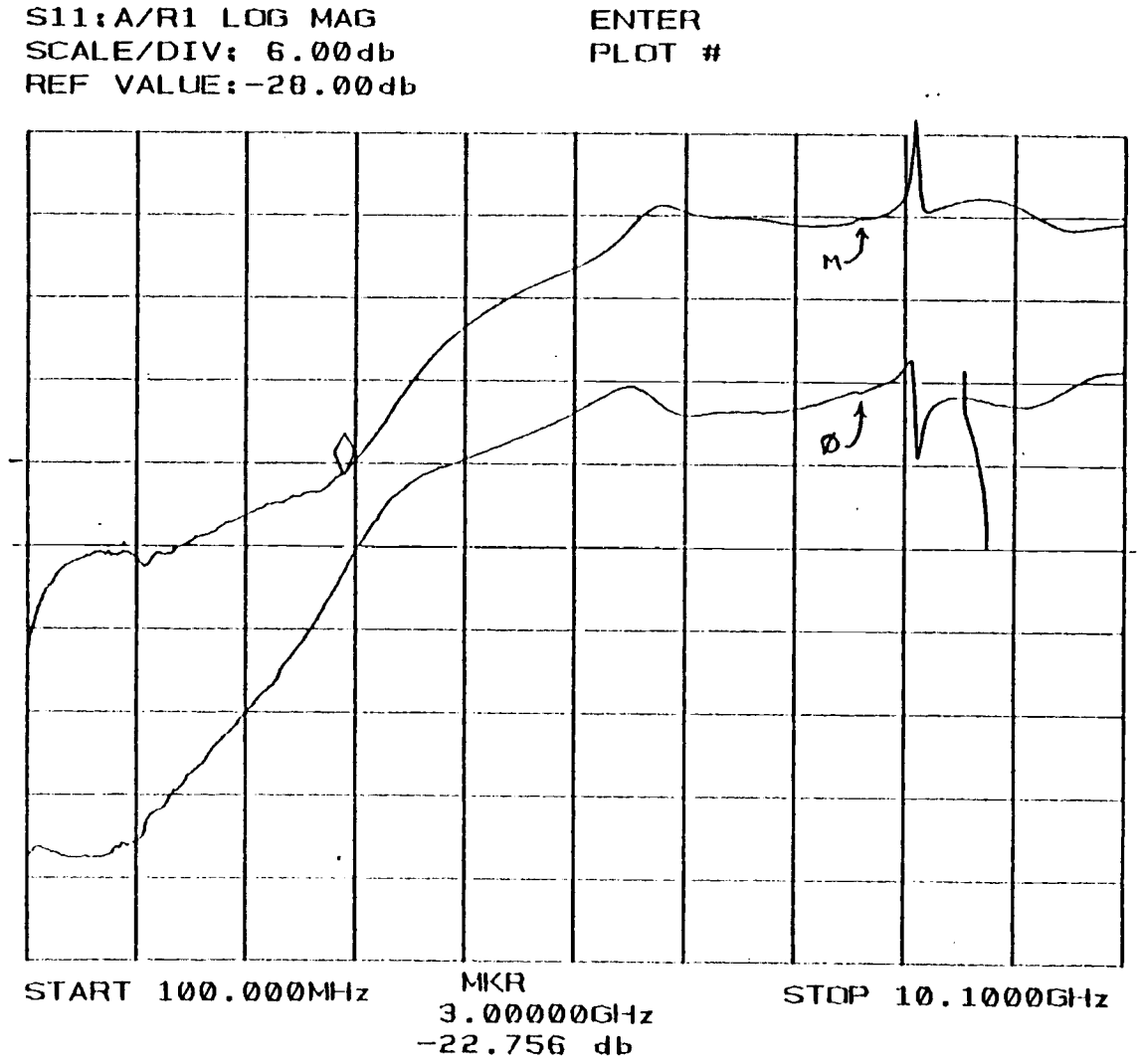


Figure 42. S11 of TC 16 (43.5 ohm, .15 pF, rect)

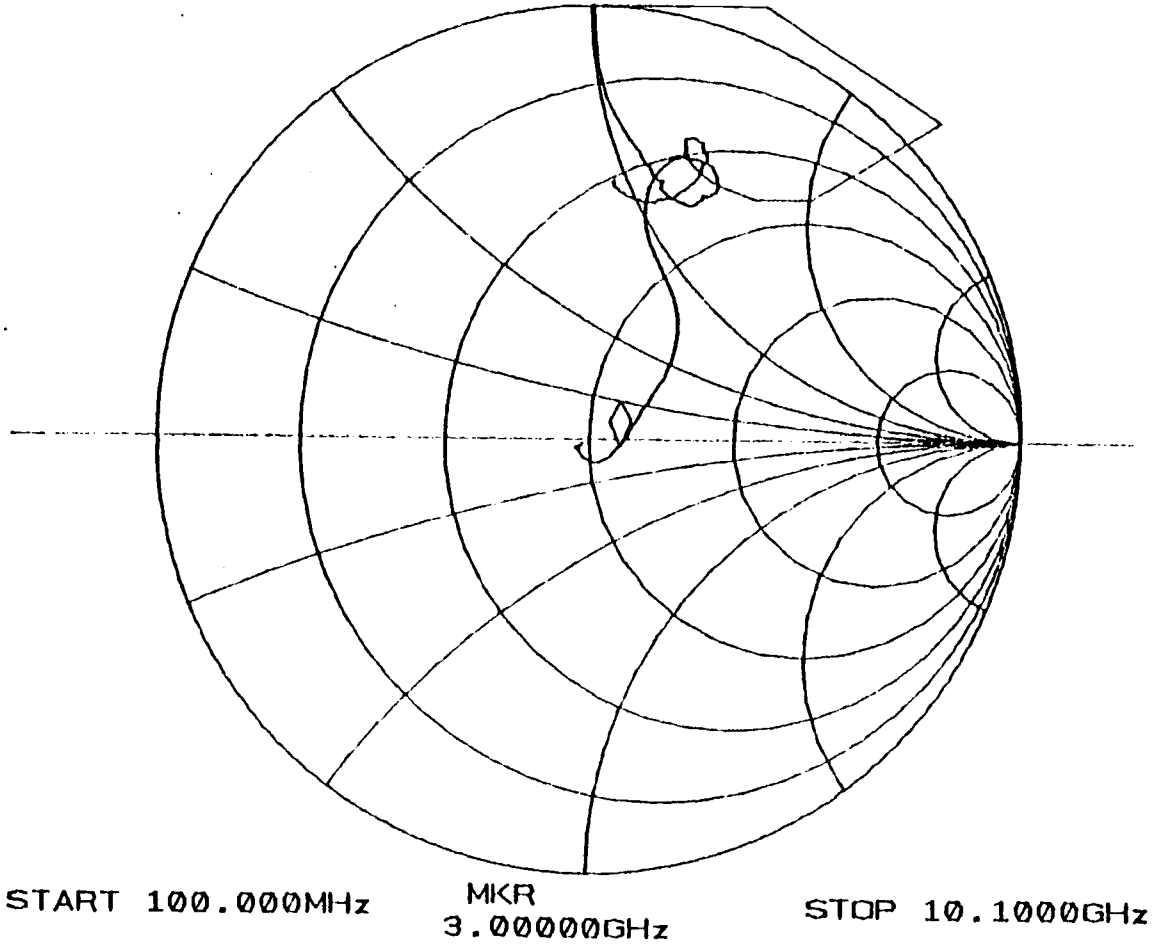


Figure 43. S11 of TC 16 (43.5 ohm, .15 pF, polar)

the matching resistor, the values for the parasitics are "tweaked" until the analysis fits the measurements. For this analysis, the measurement of the TC 16 at various frequencies is used for the transistor model, rather than using a small signal model.

After a suitable model is obtained, the values of matching resistor and compensating capacitor are varied and optimized using the MATCH routine in OPNODE. For this optimization, the goal was set at 29 dB return loss below 1 GHz, and 23 dB return loss between 1 and 3 GHz. The optimization results, shown in Figure 44 gave values for Rm and Cm as

Rm = 40 ohms

Cm = .35 pF

In practice, for a first prototype, the resistive value used would be smaller, since it is possible to raise the value of a thin film resistor once it is created, but not to lower it. If thin film interdigitated capacitors are used, they would be set to a larger value, since it is possible to reduce the capacitance, by removing interdigitated fingers, once it is made.

FINAL BREADBOARD

The measurement in Figure 42 was made with the poor input blocking capacitor configuration. The final breadboard is made by placing the amplifier circuit in the improved Tekform package, as discussed in a previous section. The input reflection of the circuit was measured, shown in Figure 45, and is at least 4 dB better than the desired return loss at all frequencies. The circuit is now in nearly final form; the only thing that needs to be added is a protection diode to prevent any static charge from reverse biasing the

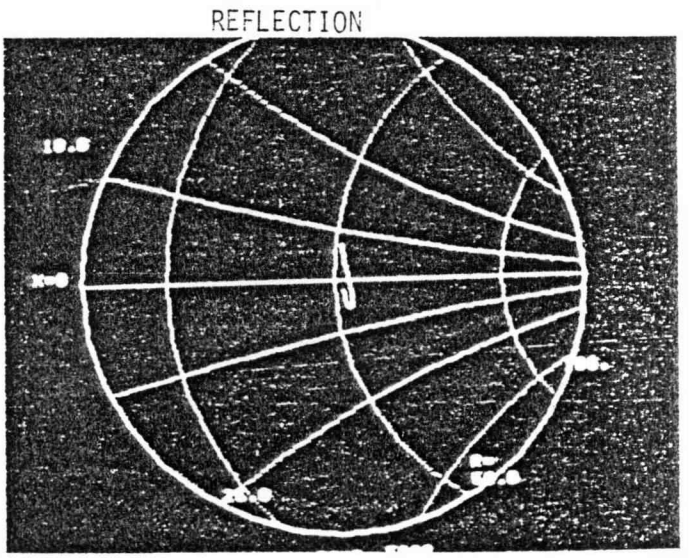


Figure 44. S11 of optimized matching elements

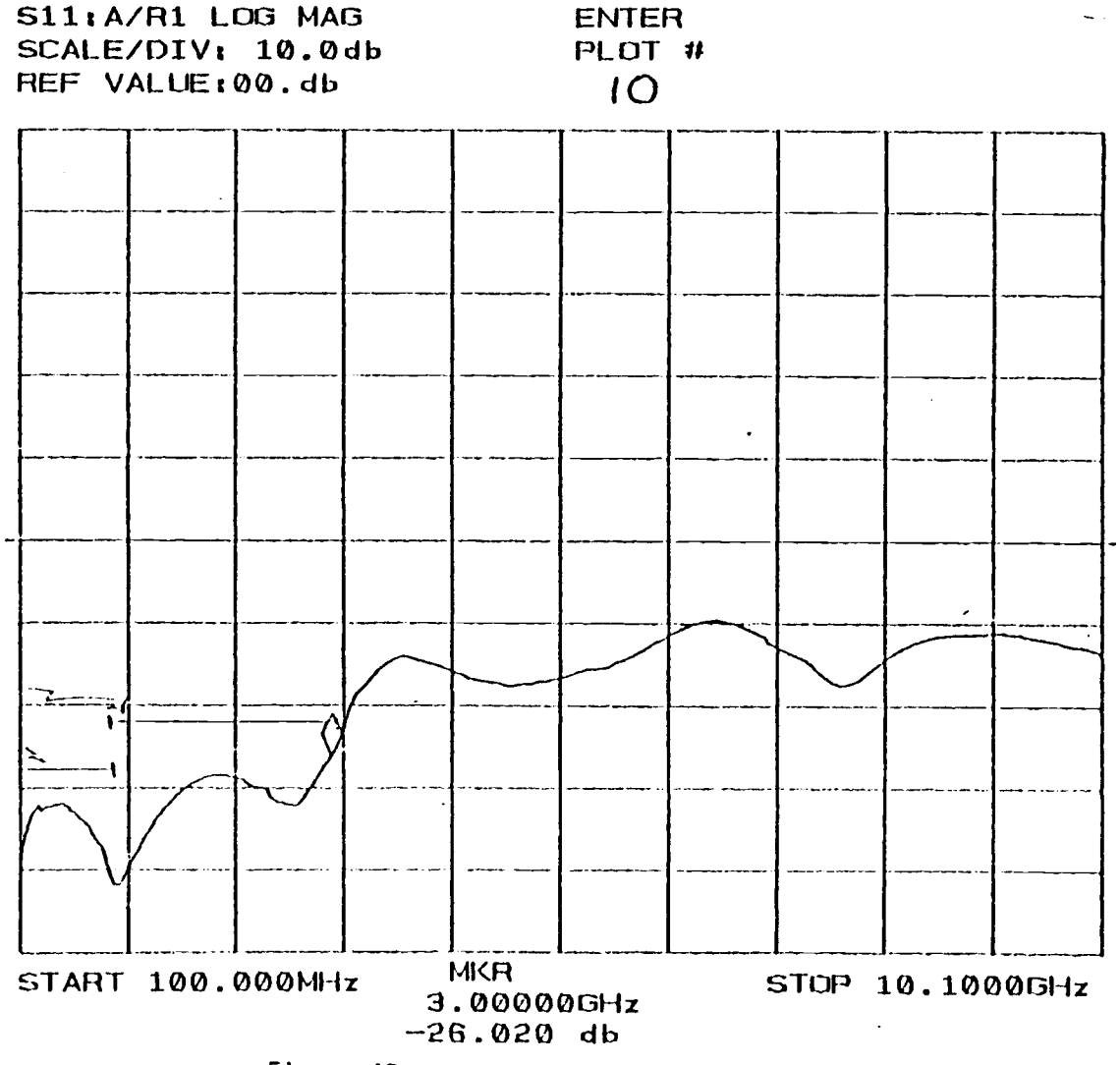


Figure 45. S11 of final breadboard

transistor. This will be a reverse biased diode and will add a capacitance to ground at the emitter. A diode with a very small reverse bias capacitance can be used, so this will likely have little effect.

The return loss might be expected to be even better, since the matching resistor used and the input transmission line will be improved in a new thin film layout. Also, the conductive vias will be of lower inductance than in the breadboard.

FINAL CIRCUIT LAYOUT

The final design is shown in Figure 46. It has the input transmission line and packaging described previously, but the amplifier will require a new thin film layout. This new layout is shown in Figure 46. Note that the input line has no bends in it. The compensating capacitor may be placed on the line, if a chip is used; or an interdigitated capacitor may be used instead.

For biasing, a changeable connection is used to change from 21 mA to 31 mA biasing. The 31 mA bias is required for adequate power gain saturation. Increasing the bias to 31 mA has less than a 1 dB effect on the return loss.

The output has a 200 ohm bias resistor, and is outputted to the sampler through a 66 ohm transmission line, providing a 50 ohm termination to the amplifier. This completes the design stage of the input buffer amplifier.

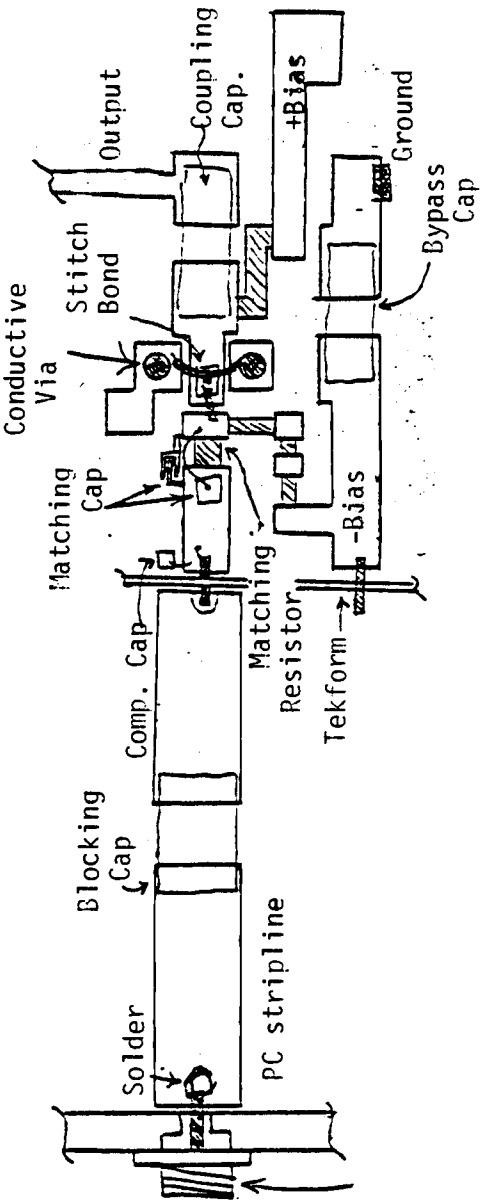


Figure 46. Final circuit layout

CHAPTER 8

CONCLUSION

The design of a state-of-the-art amplifier has been presented in this thesis. The breadboard has met all the measured specifications. Before the amplifier is ready for manufacture, a prototype using the new thin film layout should be tested for return loss and power gain saturation. Also to be tested are the noise figure and gain characteristics. Though a prototype has not yet been made, the breadboard shows the feasibility of the design, especially in the most critical design goal: input power reflection.

The circuit used in the HP 8754 amplifier failed to meet either low frequency or high frequency return loss specifications, as well as power gain saturation. By careful study of the cause of the problems, these problem areas were identified. Once identified, a solution was formulated, sometimes with the help of computer analysis and optimization, and was implemented on a breadboard circuit. The proof that a correct solution was not only a theoretical model which met the goals, but a breadboard circuit that exceeded all return loss goals.

BIBLIOGRAPHY

(1) Hewlett-Packard Co., Application Note 154, S-Parameter Design, May 1973.

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(3) Gray, P., Meyer, R., Analysis and Design of Analog Integrated Circuits, Wiley, New York. Pg. 140.

(4) Oldfield, D., Hewlett-Packard Colorado Springs Div., private correspondence, 1983.

(5) Anderson, Richard, Application Note 95-1, S-Parameter Techniques for Faster, More Accurate Network Design, reprinted from Hewlett-Packard Journal, Vol. 18, No. 6. Feb. 1967.

APPENDIX A

To define scattering parameters, consider Figure 47. Scattering parameters are ratios of incident and reflected voltages, referenced to a system impedance. The input incident and output incident voltages, normalized by $1/\sqrt{Zo}$ are a_1 and a_2, respectively. The input and output reflected voltages are b_1 and b_2, respectively. These can be mathematically defined as

$$a_1=(V_1+I_1Zo)/2\sqrt{Zo}=Vi_1/Zo \qquad a_2=(V_2+I_2Zo)/2\sqrt{Zo}=Vi_2/Zo$$

$$b_1=(V_1-I_1Zo)/2\sqrt{Zi}=V_{r1}/Zo \qquad B_2=(V_2-I_2Zo)/2\sqrt{Zo}=V_{r2}/Zo$$

where Vi = incident voltage, and V_r = reflected voltage.

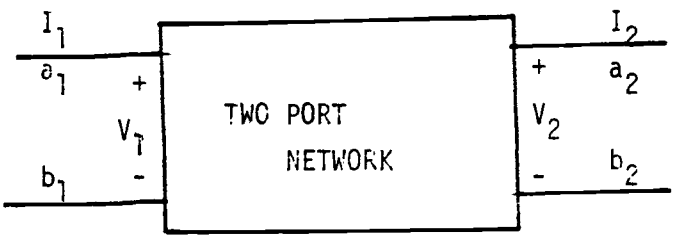

Figure 47. Two port network

The S-parameters can now be defined by

$$b_1 = (S11)a_1 + (S12)a_2$$

$$b_2 = (S21)a_1 + (S22)a_2$$

By terminating the source or load in the system impedance, Zo, and measuring B and a, any S-parameter can be found. For example, by making the load Z_1 = Zo, the a_2 = 0 and

$$S11 = b_1/a_1 = \text{input reflection coefficient}$$

The S-parameters can be related to the familiar Z-parameters by (5)

$$S_{11} = \frac{(Z_{11} - 1)(Z_{22} + 1) - Z_{12}Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}}$$

$$S_{12} = \frac{2Z_{12}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}}$$

$$S_{21} = \frac{2Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}}$$

$$S_{22} = \frac{(Z_{11} + 1)(Z_{22} - 1) - Z_{12}Z_{21}}{(Z_{11} + 1)(Z_{22} + 1) - Z_{12}Z_{21}}$$

Transfer parameters can be defined by the matrix relation

$$\begin{bmatrix} T11 & T12 \\ T21 & T22 \end{bmatrix} = \begin{bmatrix} \frac{-S11\ S22 - S12\ S21}{S21} & S11 \\ \frac{-S22}{S21} & \frac{1}{S21} \end{bmatrix}$$

The transfer parameters of cascaded networks are simply the matrix multiplication of the transfer parameters of the individual networks.

APPENDIX B

The Smith chart is very useful for relating reflection coefficient to imput impedance. It is simply a bilinear transformation of the form

$$\rho = (Zin - Zo) / (Zin + Zo)$$

where ρ, Zin, and Zo can all be complex. Typically, Zo is real and in most circuits Zo = 50 ohms.

The locus of constant resistance form circles, indicated in Figure 48. Constant reactance forms arcs of circles as shown in Figure 48. The upper half of the chart corresponds to inductive reactance; the lower half of the chart corresponds to capacitive reactance. A full circle around the center of the Smith chart corresponds to a movement of one half wavelength from the impedance being measured, by, for example, adding a half wavelength of transmission line between the measurement port and the impedance being measured.

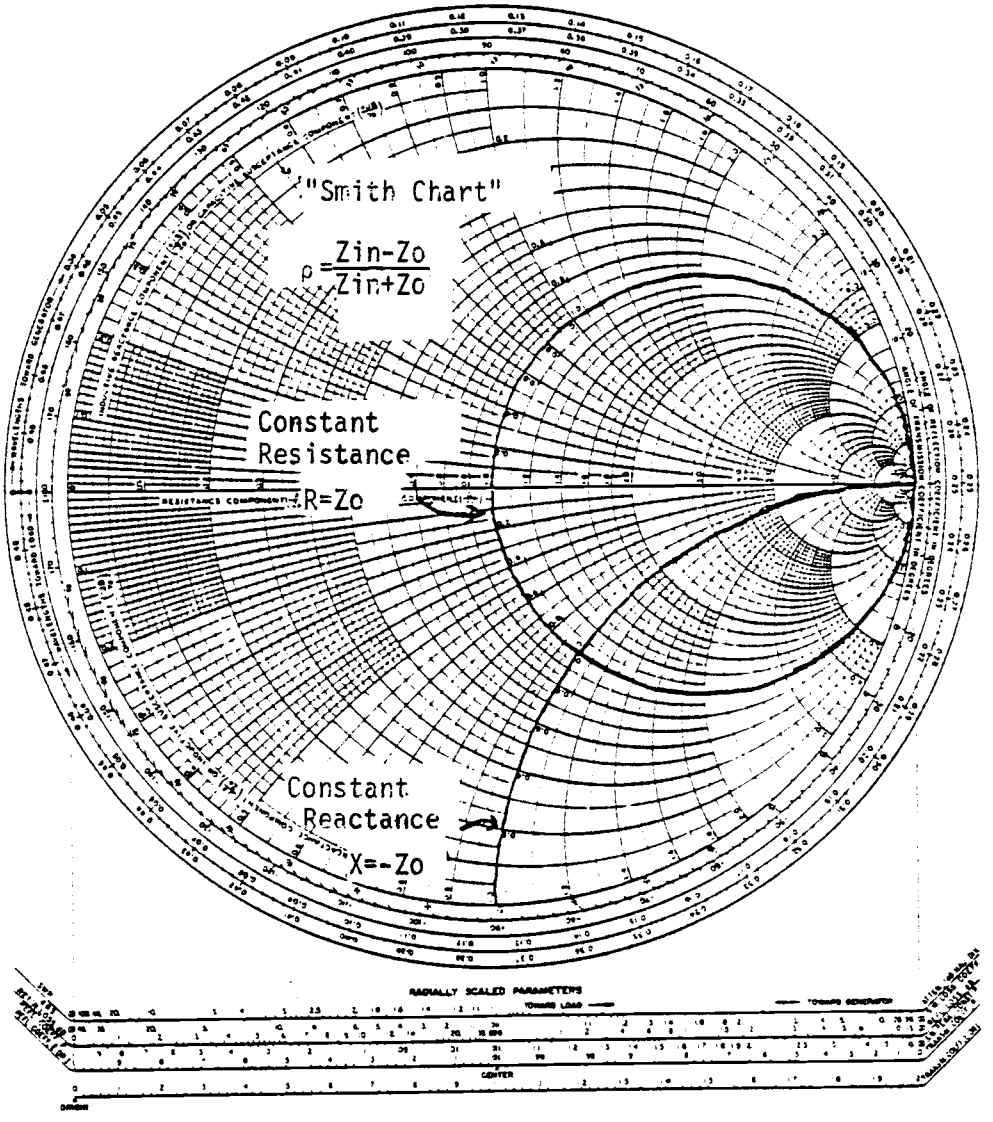

Figure 48. Smith chart

APPENDIX C

The source programs used by OPNODE to create some of the figures are given here. The figures generated by OPNODE are Figures 2, 3, 4, 6, 7, 8, 28, 29, 30, and 45. Each source program is identified by the figure number in the first line. Finally, there is the source program which contains the data library for the TC21 transistor.

```
10REM PROGRAM FOR FIGURE 2
1000CALLMWRST
1010CALLINCH
2000CALLR(1,2,30)
2010CALLC(2,3,100)
2020CALLR(3,0,20)
2030CALLIVS(1,0,1,0)
3000CALLPUT1(2,0,.001,10,-20,0,0)
```

```
10REM PROGRAM FOR FIGURE 3
1000CALLMWRST
1010CALLINCH
2000CALLR(1,2,30)
2010CALLC(2,3,100)
2020CALLR(3,0,20)
3000CALLPUT1(1,0,.001,10,-20,0,0)
3010GOSUB 9000
8999STOP
```

```
10REM PROGRAM FOR FIGURE 4
1000CALLMWRST
1010CALLINCH
2000CALLR(1,2,30)
2010CALLL(2,3,100)
2020CALLR(3,0,20)
3000CALLPUT1(1,0,.001,10,-20,0,0)
3010GOSUB 9000
8999STOP
```

```
10REM PROGRAM FOR FIGURE 6
1000CALLMWRST
2000CALLR(4,0,40)
2030CALLTL(1,0,4,0,50,1.35,1)
3000CALLPUT1(1,0,.001,10,-40,0,0)
3010GOSUB 9000
8999STOP
```

```
10REM PROGRAM FOR FIGURE 7
1000CALLMWRST
2000CALLR(1,2,20)
2010CALLC(2,3,100)
2020CALLR(3,0,20)
3000CALLPUT1(1,0,.005,10,-100,0,0)
3010GOSUB 9000
8999STOP
```

```
10REM PROGRAM FOR FIGURE 8
1000CALLMWRST
2000CALLR(4,2,20)
2010CALLC(2,3,100)
2020CALLR(3,0,20)
2030CALLTL(1,0,4,0,50,1.35,1)
3000CALLPUT1(1,0,.1,10,-40,0,0)
3010GOSUB 9000
8999STOP
```

```
5 REM PROGRAM FOR FIGURE 27
10REM THIS PROGRAM IS USED TO CALCULATE S11 FROM HAND ANALYS??
20REM OF THE COMMON BASE AMPLIFER
25CALLDLRST
26CALLMWRST
30DIM F[20],S[20,8]
40LET A=1
41LET G=.5656
42LET F1=4.5
43 R3=1.023
50PRINT "INPUT R   AND L  "
60INPUT R1,L2
61LET L1=L2*1.00000E-09
100FOR I=1TO 20STEP 1
110LET F[I]=.5*I
120LET N=I
200LET D=A/(1+(A*F[I]/F1)*(A*F[I]/F1))
201PRINT "D=",D
210LET Z1=R1*(1-D)+(1/G)*D-6.28000E+09*F[I]*L1*(A*F[I]/F1)*D??
220LET Z2=6.28000E+09*F[I]*L1*(1-D)+ R1*(A*F[I]/F1)*D- (1/G)??
230LET M=SQR(((Z1-50)*(Z1-50)+Z2*Z2)/((Z1+50)*(Z1+50)+Z2*Z2)??
240LET P1=ATN(Z2/(Z1-50))
250LET P2=ATN(Z2/(Z1+50))
260LET P=(P1-P2)*180/3.1415926
261PRINT "Z1=",Z1,"Z2=",Z2
265IF (Z1-50)<0THEN 267
266GOTO 270
267LET P=P+180
270LET S[I,1]=M
280LET S[I,2]=P
281PRINT "FREQ=",F[I],"MAG= ",M," ,PHASE= ",P
290FOR J=3TO 8STEP 1
300LET S[I,J]=0
310NEXT J
320NEXT I
330CALLNWDEV("HYBRIDTMOD",N,F[1],"SMP",S[1,1])
340STOP
3210LET S[I,J]=0
9999END
```

```
5 REM PROGRAM FOR FIGURE 28
10CALLDLRST
20LET L1=.088
1000CALLMWRST
1010CALLNWMOD("HMOD",100,4.5,.01,12,5.00000E+12,5.00000E+13)
2000CALLMODEL(2,3,4,"HMOD",17,.015)
2010CALLR(2,0,50)
2020CALLL(3,0,L1)
2030CALLR(1,4,1.023)
3000CALLPUT1(1,0,.5,7.5,15,0,0)
3010GOSUB 9000
8999STOP
```

```
5 REM PROGRAM FOR FIGURE 29
10CALLDLRST
20LET L1=.088
1000CALLMWRST
1010CALLNWMOD("HMOD",100,4.5,.18,12,50000.,500000.)
2000CALLMODEL(2,3,4,"HMOD",17,.015)
2010CALLR(2,0,50)
2020CALLL(3,0,L1)
2030CALLR(1,4,1.023)
3000CALLPUT1(1,0,.5,7.5,15,0,0)
3010GOSUB 9000
8999STOP
```

```
10 REM PROGRAM FOR figure 44
1000CALLMWRST
2000CALLDEV(5,6,7,6,"TC16B15MA")
2010CALLR(7,0,50)
2020CALLL(6,0,.45)
2030CALLL(4,5,.57)
2040CALLC(4,0,.1)
2050CALLTL(2,0,3,0,50,.32,.4)
2060CALLC(2,0,.3)
2070CALLTL(1,0,2,0,50,-.42,.4)
2080CALLR(3,4,49)
2085CALLOPT(1,1,100)
2090CALLC(3,4,.001)
2095CALLOPT(1,.001,1)
3000CALLPUT1(1,0,.5,3.5,15,.079,15)
```

```
1  REM  THIS DATA WAS TAKEN BY TC, ENTERED BY
2  REM  JOEL DUNSMORE, JULY 9,1981
10 DLRST
100  CALL MWRST
110  DIM F[14],S[14,8]
120    FOR I=1 TO 14
130    READ F[I]
140    IF F[I]=0 THEN 200
150      FOR J=1 TO 7 STEP 2
160      READ S[I,J],S[I,J+1]
170      NEXT J
180    LET N=I
190    NEXT I
200  CALL NWDEV("TC21B15MA",N,F[1],"SMP",S[1,1])
210  STOP
220  REM THIS IS THE DATA FOR THE TC21 IN COMMON BASE
230  REM MODE, BIAS VCE=15V, ICE=15MA
1000  DATA .5,.892,177,.004,92,1.867,-10,1.004,-7
1010  DATA 1,.884,175,.009,98,1.854,-19,1.011,-14
1020  DATA 1.5,.873,172,.014,103,1.847,-30,1.021,-21
1030  DATA 2,.86,170,.02,105,1.821,-41,1.037,-28
1040  DATA 2.5,.834,168,.024,101,1.781,-51,1.05,-36
1050  DATA 3,.818,167,.032,104,1.727,-62,1.069,-43
1060  DATA 3.5,.801,165,.041,102,1.663,-74,1.088,-50
1070  DATA 4,.773,165,.043,94,1.563,-85,1.08,-58
1080  DATA 4.5,.75,165,.047,90,1.468,-96,1.094,-65
1090  DATA 5,.734,165,.053,88,1.358,-106,1.085,-71
1100  DATA 5.5,.725,165,.057,85,1.238,-117,1.055,-78
1110  DATA 6,.723,166,.054,85,1.137,-127,1.053,-83
1120  DATA 6.5,.716,166,.061,85,1.029,-137,1.035,-88
9998  DATA 0
9999  END
```