Real-Time Pulse-Shape Discrimination and Beta-Gamma Coincidence Detection in Field-Programmable Gate Array

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Abstract

A real-time FPGA-based algorithm has been developed and tested to discriminate pulse-shapes, identify beta-gamma coincidence events and collect energy spectra from xenon radioisotopes using a phoswich detector. The detector consists of a thin plastic scintillator (BC-400) to detect beta and conversion electrons, a CsI(Tl) crystal for measuring X-rays and gamma-rays, and a BGO crystal, which surrounds the CsI(Tl) layer, to identify scattered photons and ultimately to reduce Compton continuum in the gamma energy spectrum. In this paper, we report on the detail of the FPGA hardware design, the pulse-shape discrimination method, and the system's operational modes. In addition, our initial real-time radioxenon measurement results with the phoswich detector are presented.

Keywords: Digital Signal Processing; Pulse Shape Discrimination; Phoswich Detector; Radioxenon Measurement; FPGA Devices

1. Introduction

Measuring elevated concentrations of the four xenon radioisotopes (^{133m}Xe, ^{131m}Xe, ^{133}Xe and ^{135}Xe) along with their relative concentration ratios in the atmosphere will enable the International Monitoring System (IMS) to monitor nuclear weapon testing around the world. One proved efficient and highly sensitive radioxenon measurement method is the well-known beta-gamma coincidence technique. In this technique, beta particles (or conversion electrons) and gamma-rays (or X-rays) emitted from the xenon radioisotopes are measured simultaneously. Table 1 lists characteristic energies for the decay of ^{131m}Xe, ^{133m}Xe, ^{133}Xe, and ^{135}Xe [1].

Table 1. Half-lives and characteristic energies for the decay of ^{131m}Xe, ^{133m}Xe, ^{133}Xe, and ^{135}Xe [1]

Radionuclide	**^{131m}Xe**	**^{133m}Xe**	**^{133}Xe**	**^{135}Xe**
Half-life	11.93 d	2.19 d	5.25 d	9.14 h
Gamma-rays (keV)	163.9	233.2	81.0	250.0
Gamma-ray abundance (%)	1.96	10.3	37.0	90.0
X-ray, K-shell (keV)	30.	30.	31.	31.
X-ray abundance (%)	54.1	56.3	48.9	5.2
Beta, Max. Energy (keV)	-	-	346.	905.
Beta abundance (%)	-	-	99.	97.
CE, K-shell (keV)	129.	199.	45.	214.
CE abundance (%)	60.7	63.1	54.1	5.7

In a typical detection system, a beta-gamma coincidence spectrum is constructed to locate three regions of interest in which the four xenon radioisotopes can be detected and measured [2]. These regions are located at three X-ray/gamma-ray energy lines: 30, 81 and 250 keV. It has been shown that using beta-gamma coincidence counting provides a 10^3- to 10^4-fold background reduction over standard gamma-ray spectroscopy [3]. The Automated Radioxenon Sampler and Analyzer [4] and the Swedish Automated Unit of Noble gas Acquisition [5] are two radioxenon detection systems designed based on this technique. Both systems employ two separate detection channels, one for measuring beta particles (or conversion electrons) and one for gamma rays (or

X-rays). Employing multiple detection channels in these systems requires separate pulse processing electronics for each channel and, eventually, sophisticates energy calibration and gain matching procedures.

In order to simplify radioxenon measurements, we have developed a novel phoswich detector with Compton suppression capability [6-7]. One important feature of this detector is its capability to identify and reject Compton scattering events in its gamma detection layer. The phoswich detector has been designed with three scintillation layers. Beta-gamma coincidence events from radioxenon isotopes are identified when a coincidence energy absorption is detected in the first (plastic, BC-400) and second (CsI(Tl) crystal) scintillation layers. To identify and reject scattered photons, the CsI(Tl) crystal is surrounded by a BGO scintillation layer. If a photon triggers responses in both layers, the event is rejected.

In the past, we characterized our phoswich detector in measuring xenon radioisotopes using a PC-based digital pulse processing algorithm (offline analysis) [6]. To enhance the detection system's performance and portability in measuring beta-gamma coincidence events, a real-time digital pulse processing firmware was developed and implemented in a Field-Programmable Gate Array (FPGA) device.

In this paper, we describe our FPGA algorithm structure by which the system is triggered, pulse-shapes are discriminated, Compton events are rejected, beta-gamma coincidence events are identified, associated beta-gamma energy releases are measured, and finally the two energy histograms are updated. In addition, our recent real-time test results in measuring coincidence events from ^{133}Xe and ^{135}Xe, produced at the Oregon State University's TRIGA reactor, are presented.

2. Digital processing of detector pulses in FPGA devices

FPGAs are an array of programmable logic cells interconnected by a network of wires and configurable switches. A FPGA has a large number of these cells available to form multipliers, adders, accumulators and so forth in complex digital circuits. FPGAs can be infinitely

reprogrammed in-circuit in only a small fraction of a second. In modern digital pulse processing systems for radiation spectroscopy, the processing of radiation pulses is performed either in a pair of FPGA-DSP system [8-9] or entirely in a single FPGA device [10-11]. In both approaches, after an analog conditioning stage, detector pulses are sampled by a high-speed, free-running Analog-to-Digital Convertor (ADC), and then the stream of digital samples is fed into a FPGA device.

In a typical FPGA-DSP-based pulse processing system, generally only those digital functions that should be performed with ADC's clock speed, such as triggering, pileup detection/rejection, pulse capturing and digital pulse shaping, are implemented in a FPGA device. The rest, including pulse amplitude measurement and histogram construction, are performed in a slower sequential algorithm in a DSP (Digital Signal Processor) device. The DSP processing algorithm must be implemented with much higher clock frequency to maximize the system throughput since the detection system accumulates dead time while the DSP performs the sequential calculations in its algorithm. One other drawback of this approach is the need for code development and troubleshooting for two different devices/platforms which dramatically increases the development time and overall cost.

In a FPGA-based radiation pulse processing system, all the pulse processing functions including energy measurement and histogram construction are realized in a single FPGA device. In addition, new FPGA devices provide integrated memory components. This feature further simplifies the system design in constructing energy histograms inside the FPGA without using external memory. Since all the computation functions are executed in parallel in the hardware, a minimal dead time can be achieved using a single FPGA for real-time measurements. Since only one processing device is employed, developing codes for FPGA-based pulse processors are much easier and less time consuming.

3. Phoswich detector and pulse-shape analysis

The phoswich detector, shown in in Fig. 1, consists of a thin plastic scintillator (BC-400) to detect beta and conversion electrons, a CsI(Tl) crystal for measuring X-rays and gamma-rays,

and a BGO crystal, which surrounds the CsI(Tl) layer, to identify scattered photons and ultimately to reduce Compton continuum in the gamma energy spectrum. Physical properties of the scintillators used in the phoswich detector are summarized in Table 2.

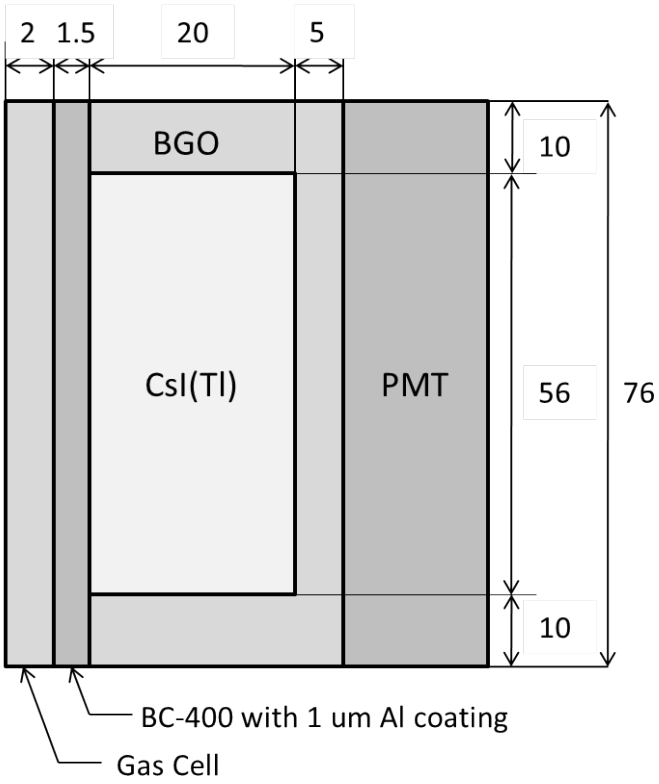

Fig. 1. Schematic diagram of the phoswich detector used in this work. All dimensions are in mm.

Table 2. Physical properties of scintillators used in the phoswich detector.

Scintillator	**BC400**	**CsI(Tl)**	**BGO**
Decay Time (ns)	2.4	~1000	300
Light Output (photon/MeV)	13,000	65,000	8,200
Peak Emission (nm)	423	540	480
Refractive Index	1.58	1.8	2.15
Density (g/cm^3)	1.032	4.51	7.13

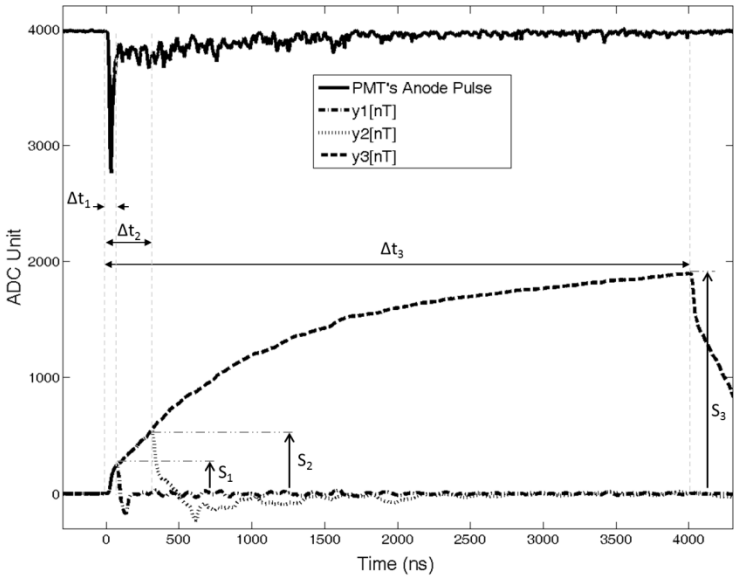

Fig. 2. A typical phoswich pulse and responses of three digital triangular filters (y_1, y_2 and y_3) when a coincidence event occurs in the phoswich detector [6]. The pulse shown in this Fig. was captured with a sampling period (T) of 5 ns.

In the past, for prototyping purposes, we developed an offline algorithm in MATLAB to digitally process pulses from the phoswich detector. In our offline algorithm, to discriminate between different pulse-shapes, each anode pulse was integrated over three time intervals (Δt_1, Δt_2 and Δt_3) using three digital triangular filters with appropriate peaking times. y_1, y_2 and y_3 traces shown in Fig, 2 are the responses of these filters to a typical phoswich signal pulse. The output amplitudes of these filters, S_1, S_2 and S_3, represent the integration or sum of each pulse over the Δt_1, Δt_2 and Δt_3 time intervals, respectively. In Fig. 2, Δt_1, Δt_2 and Δt_3 were set respectively to 60 ns, 300 ns and 4000 ns. Using these sums, two ratios, the Fast Component Ratio (*FCR*) and Slow Component Ratio (*SCR*), were calculated from each captured pulse. The *FCR* and *SCR* were calculated using the following equations:

$$FCR = \frac{S_1}{S_2} \qquad \textbf{(1)}$$

$$SCR = \frac{S_2 - S_1}{S_3 - S_1} \qquad \textbf{(2)}$$

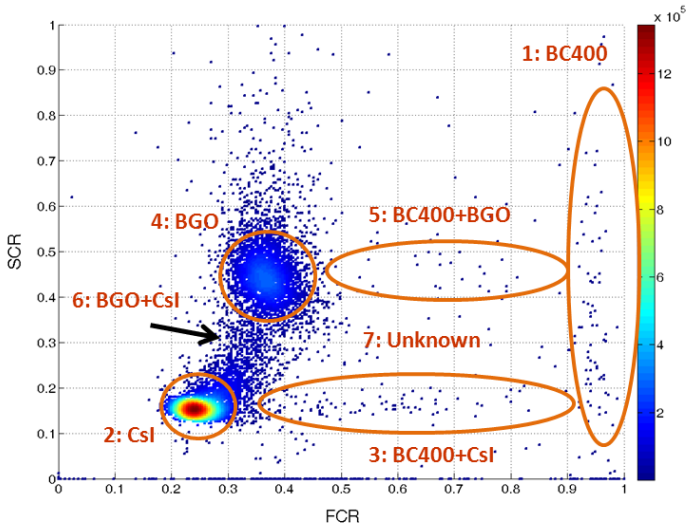

Fig. 3. Scatter of the Fast and Slow Component Ratios from 662 keV of ^{137}Cs calculated using an offline pulse shape-analysis. Seven marked regions correspond to seven pulse shapes, indicating how gamma-rays interact with the three layers of phoswich detector.

Since sum S_1 is a fraction of sum S_2 and sum S_2 is a fractions of sum S_3, the *FCR* and *SCR* defined in Equations 1 and 2 can range from zero to unity. Our previous offline analysis showed that depending on how the incident radiation releases its energy within each layer of the phoswich detector, seven possible regions are populated in the *FCR-SCR* scatter plot. Fig. 3 shows a two-dimensional scatter plot of the *FCR* and *SCR* from our offline analysis when the phoswich detector was exposed to 662 keV of a ^{137}Cs source. In this Figure, regions 1, 2 and 4 represent single events in plastic (BC-400), CsI(Tl) and BGO scintillators, respectively. Regions 3 and 5 show coincidence events of CsI(Tl)-plastic and BGO-plastic, respectively. Region 6 accommodates Compton scattering events between CsI(Tl) and BGO. When either all three timing components appear in the pulse or the shape of pulse is unknown, corresponding event appears in region 7.

The same sum values are used to calculate the corresponding pulse areas A_g and A_b (proportional to the number of scintillation photons generated in the CsI(Tl) and BC400, respectively) and

subsequently to measure coincidence energy deposition in the CsI(Tl) and BC400 layers. The A_g and A_b are calculated using the following equations:

$$A_g = S_3 - S_1 \qquad \textbf{(3)}$$

$$A_b = S_1 - K(S_3 - S_1) \qquad \textbf{(4)}$$

The product term *"K (S_3 – S_1)"* in Eq. 4 is the contribution of CsI(Tl)'s scintillation component in the Δt_1 integration interval. The fraction coefficient *"K"* can be determined experimentally using pulses detected in region 2 (CsI(Tl) single events).

We have employed the same pulse shape analysis approach in our real-time pulse processing algorithm discussed in the following sections.

4. FPGA operational modes

In order to make the FPGA algorithm usable in both prototyping and real-time measurements, the FPGA pulse processing algorithm was developed for operation in four modes: (1) Scope, (2) Pulse-Shape Analysis (PSA), (3) Coincidence Event (CE), and (4) Multichannel Analyzer (MCA) modes. In addition, a MATLAB program was developed to control the digital pulse processor unit, set the pulse processing parameters and display measurement results on the PC's screen. The function of each mode is described below.

In the Scope mode, individual anode pulses are captured in a circular buffer (1,024 samples) and transferred to the PC for either displaying on the screen or for an offline analysis. Using this mode, a user can conveniently monitor the health of anode pulses and set the optimum pulse capture parameters such as amplification gain and offset level by the MATLAB program. This mode provides no pulse processing on the phoswich anode pulses.

The PSA mode is used to plot a *FCR-SCR* scatter graph from individual pulses and to determine the boundaries of the region 3 (BC400+CsI coincidence events shown in Fig. 3). This region is defined by four level values: Fast Ratio Lower Level (*FRLL*), Fast Ratio Upper Level (*FRUL*),

Slow Ratio Lower Level (*SRLL*), and Slow Ratio Upper Level (*SRUL*). These level values should be determined and set before running the pulse processing algorithm in the other two coincidence modes such as the CE and MCA modes.

In the CE mode, for each detected coincidence pulse, two pulse areas (A_g and A_b) are calculated in real-time and transferred to the PC to construct a 3-D beta/gamma coincidence energy spectrum. This type of coincidence spectrum should be constructed from individual coincidence events and cannot be made from histogram data collected in the MCA mode.

The MCA mode is used to collect separate beta particle and gamma-ray histograms in on-board FPGA device. Both histograms are updated only if the measured *FCR* and *SCR* values of the pulse are identified to be in the region 3 (BC400+CsI(Tl) coincidence events). If the gamma-ray undergoes a Compton scattering in the CsI(Tl) and the scattered photon is fully absorbed or re-scattered in the BGO, even if it is in coincidence with beta absorption in the BC400, the event will be outside the region 3 and therefore will be rejected automatically.

5. FPGA hardware design and implementation

To realize the four operational modes, the FPGA hardware design was developed with a hierarchical structure including three main modules: Trigger, Scope, and Histogram modules. The Scope mode is realized in the Scope module including two state machines and a circular buffer to capture and transfer sampled pulses to the PC. Since no digital processing is performed in this module, the detail of its hardware implementation is not discussed here.

5.1. Trigger module

A block diagram of the Trigger module is given in Fig. 4. This module has a simple structure and generates a trigger input to other modules. The Trigger module was realized by employing a fast digital triangular filter (Finite Impulse Response filter). The peaking time of this filter was initially set to 100 nsec. Since the triggering function is based on a differential sum computation

(triangular filtering), detecting a valid radiation pulse above the noise level is independent of the baseline offset. In this module, the ADC samples are fed into the triangular filter then from there to a comparator. A dedicated state machine continually monitors the output of this comparator and issues a one-cycle logic pulse (trigger output) when the filter output is above a predetermined threshold level.

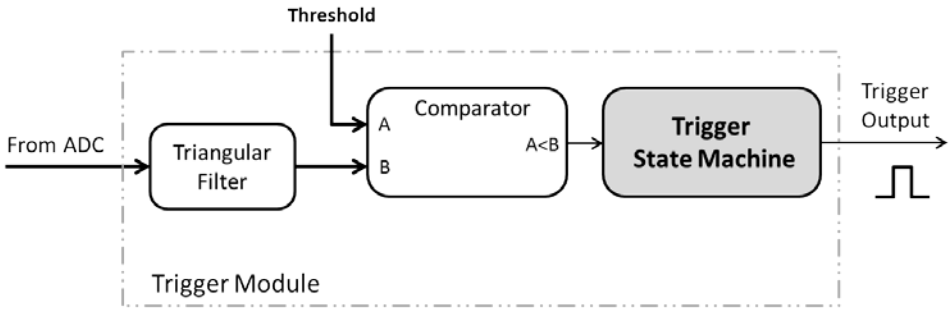

Fig. 4. Block diagram of the Trigger module.

5.2. Histogram module

Except the Scope mode, the other three FPGA operational modes were realized in the Histogram module illustrated in Fig. 5. To enhance timing performance of the Histogram module, all combinational components implemented in this module were registered leading to a fully pipelined hardware design. As depicted in Fig. 5, the Histogram module receives detector sample data directly from the ADC (12 bits). It also receives a trigger signal from the Trigger module. Our simulations using the Xilinx ISE Design Suite software shows that there is a 12-cycle latency for the trigger signal when a step function is applied to the Trigger module. To compensate for this latency, the ADC data are delayed by a variable delay unit made by RAM-based shift registers (a Xilinx IP core).

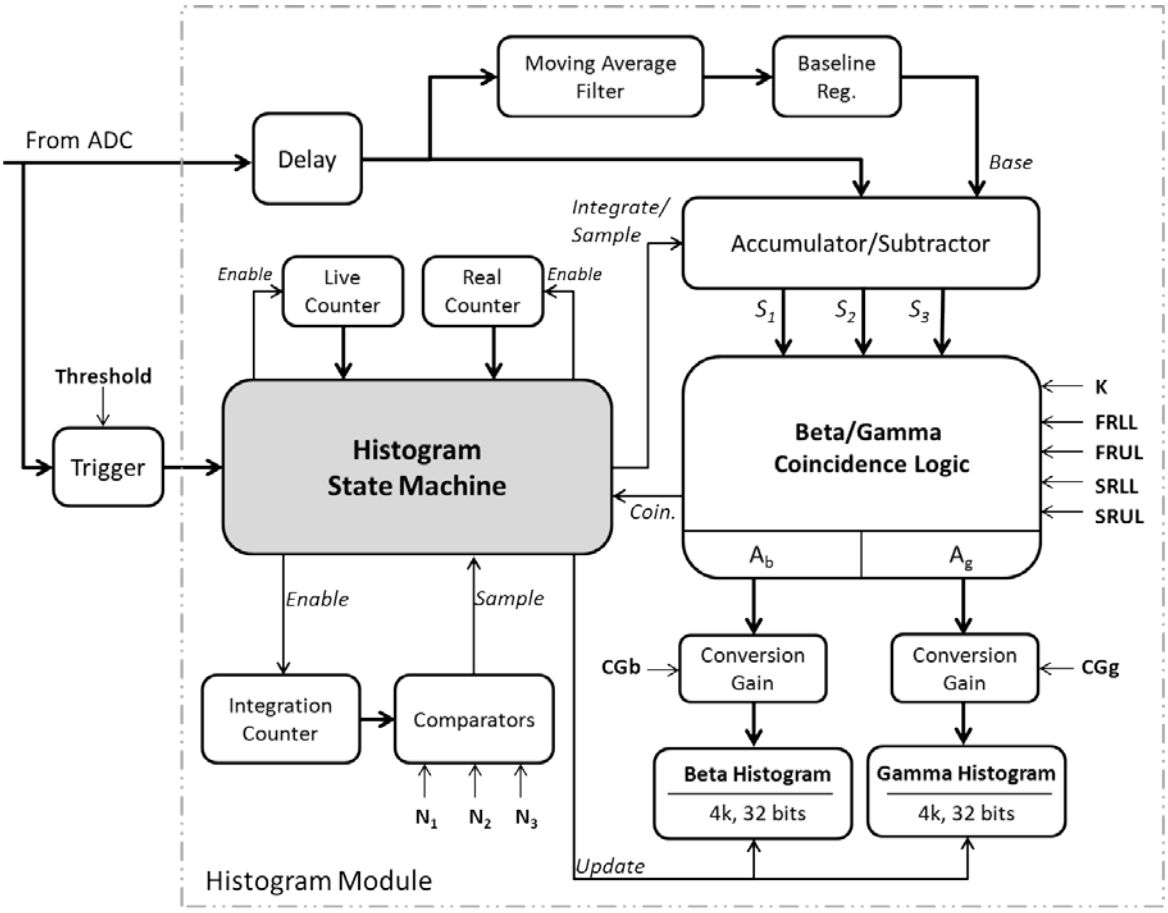

Figure 5. A simplified block diagram of the Histogram module implemented in the FPGA device for real-time pulse-shape discrimination and beta/gamma coincidence measurements. To simplify the diagram, only data processing path for the MCA mode is shown.

In order to estimate the areas under each phoswich pulse, an average of the pulse baseline, right before the trigger point, needs to be taken. The average *Base* is computed using a simple moving average filter. In the current design, the *Base* is an average of the pulse baseline over eight ADC samples before a radiation pulse arrives. A register is used at the output of this filter to sample the average baseline Base. The average baseline and delayed ADC samples are fed into the Accumulator/Subtractor unit. A single counter (Integration Counter) and three comparators schedule the integration process in the Accumulator/Subtractor unit to estimate the three sums, S_1, S_2 and S_3, defined mathematically by Eqs. 5-9:

$$y[n] = y[n-1] + x[n] \qquad \textbf{(5)}$$

$$b[n] = b[n-1] + Base \qquad \textbf{(6)}$$

$$S_1 = b[N_1] - y[N_1] \qquad \textbf{(7)}$$

$$S_2 = b[N_2] - y[N_2] \qquad \textbf{(8)}$$

$$S_3 = b[N_3] - y[N_3] \qquad \textbf{(9)}$$

where *n* is the sample index, *x[n]* is the delayed ADC sample, *y[n]* and *b[n]* are the outputs from two accumulators, *Base* is the averaged baseline, and N_1, N_2 and N_3 are the number of ADC clock cycles within the three integration intervals Δt_1, Δt_2 and Δt_3, respectively.

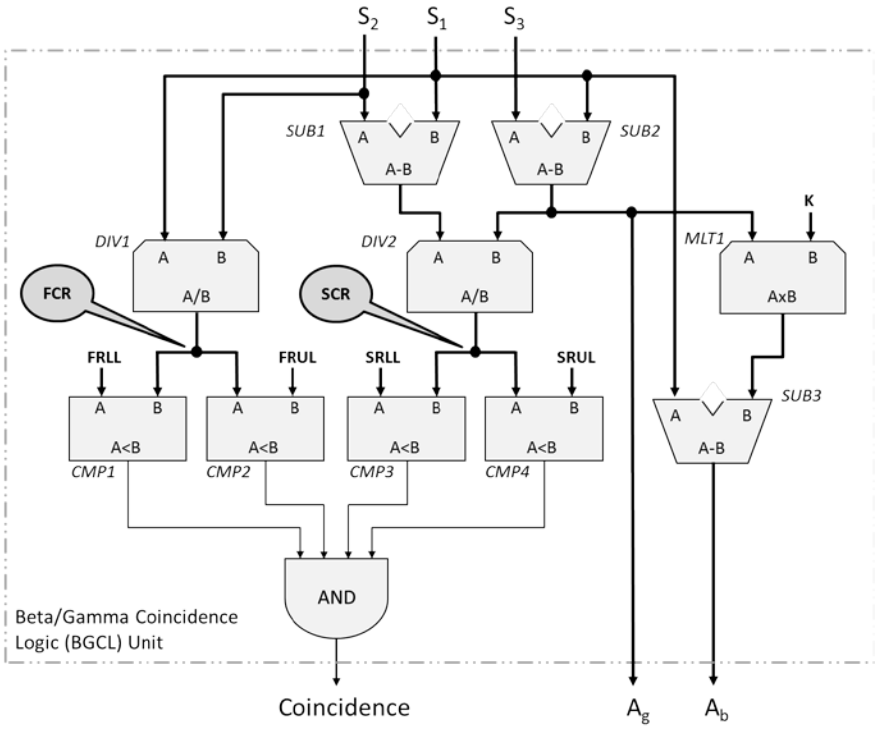

Fig. 6. Block diagram of the Beta/Gamma Coincidence Logic (BGCL) unit.

As depicted in Fig, 6, the three calculated sums (S_1, S_2 and S_3) are fed into the Beta/Gamma Coincidence Logic (BGCL) unit in which (1) coincidence pulses are identified through a real-time pulse-shape analysis (defined by Eqs 1 and 2) and (2) the corresponding pulse areas A_g and

A_b are calculated (defined by Eqs 3 and 4). The BGCL unit was realized using three substractors, two dividers, one multiplier, four comparators, and one four-input AND gate. The *Coincidence* signal output in BGCL unit (Fig. 6) goes "*High*" if the measured pulse-shape parameters of the pulse (*FCR* and *SCR*) are identified to be a coincidence event in the region 3 defined by its four predetermined boundaries (*FRLL*, *FRUL*, *SRLL* and *SRUL*).

In order to reconstruct the beta particle (conversion electrons) and gamma-ray (X-ray) energy spectra in real-time, two separate histograms were implemented in the FPGA design. The Gamma and Beta Histograms, shown in Fig. 5, were implemented using dual-port Block RAM memories available in SPARTAN-3 FPGA devices. Sixteen Block RAM's were used to implement these two 4k, 32-bit histograms. Two Conversion Gain units are employed to scale and locate appropriate channel addresses in the two histograms. CG_b and CG_g are gamma and beta conversion gain parameters, respectively. These parameters can horizontally scale the beta and gamma energy histograms in 16 scaling steps (four bits).

As shown in Fig. 5, to measure elapsed real and live times and to perform real-time quantitative measurements, two counters (*Live Counter* and *Real Counter*) were implemented in the Histogram module. They were made of two 49-bit counters. These counters are clocked with the ADC's clock frequency, f_{adc}. Since only 32 most significant bits of these counters are used to measure the time, minimum measurable time is $2^{17}/f_{adc}$.

5.3. Histogram state machine

The histogram state machine, shown in Fig. 5, sequentially controls the pulse processing algorithm in the Histogram module. This state machine is clocked with the ADC's clock frequency (f_{adc}). A simplified state diagram is presented in Fig. 7. To simplify the diagram, some states such as mode selection/directing states are not shown.

The state machine will move from its idle state, the *STOP* state, to the *RESET* state and start processing incoming pulses when it receives a one-cycle signal, *Start*, initiated from the MATLAB program. The *RESET* state resets the two time measuring counters, Real and Live

Time Counters. Then the state machine stays at the *START* state until it receives a *Trigger* signal from the Trigger module. The average baseline, *Base*, is sampled at the next state, the *RD-BASE* state. The Integration Counter is also reset at the same state.

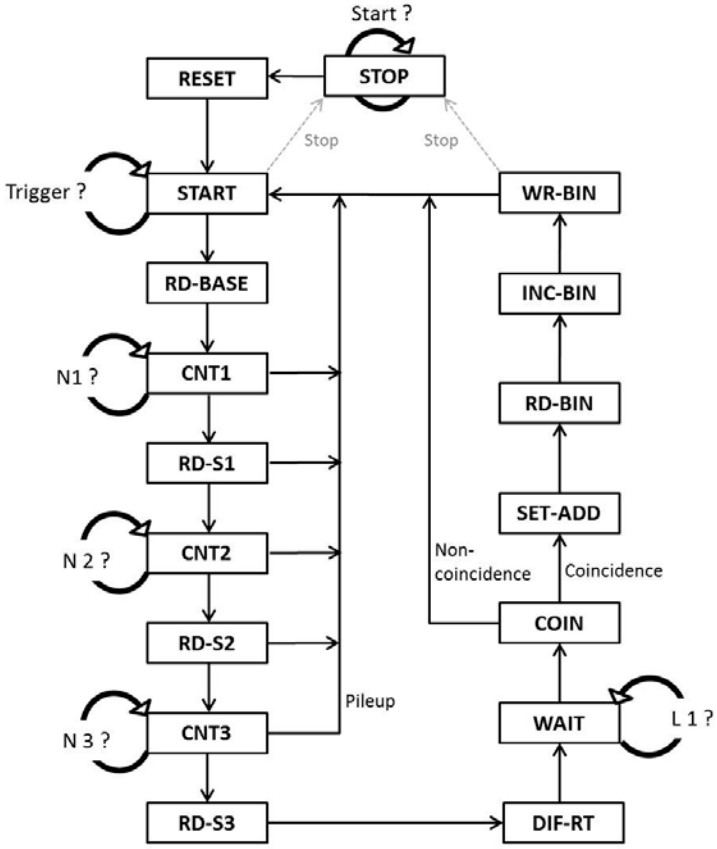

Fig. 7. A simplified state diagram of the histogram state machine implemented in the FPGA device.

The state machine starts integrating incoming pulses by enabling the Integration Counter and Accumulator/Subtractor unit at the *CNT1* state. It moves to the *RD-S1* state when the counter reaches at its first sampling point, N_1. At the *RD-S1* state, the first sum, S_1, is calculated and sampled in the Accumulator/Subtractor unit. The integration process will continue in the next four states (*CNT2*, *RD-S2*, *CNT3* and *RD-S3*) to calculate sums S_2 and S_3. During the integration process, the state machine continually checks the Trigger signal for any pileup event. If a pileup event is detected, the state machine will move to the *START* state without performing any further pulse processing or histogram updating.

Sums S_1, S_2 and S_3 are provided to the BGCL unit at the *DIFF-RT* state. Since divider components implemented in the BGCL unit require 34 clock cycles to complete their division operations, the state machine moves to the WAIT state and stays there for L_1=34 clock cycles. The pulse areas A_g and $A_{b,}$ and the *Coincidence* signal will be valid for further actions at the *COIN* state. In the PSA or CE modes, only calculated data such as *FCR*, *SCR*, A_g and A_b are transmitted to the PC and no additional processing function is performed in the hardware. In the MCA mode, however, the two histograms will be updated in the following states if a coincidence event is identified.

If the *Coincidence* signal level is "*LOW*" indicating a non-coincidence event has occurred, the state machine will reject the event and will move to the *START* state. Otherwise, it will move to the *SET-ADD* state where the A_g and A_b values locate and set bin addresses in the two corresponding histograms. At the *RD-BIN* state, current contents of the two histograms at the located addresses (bins) are read. The current contents (counts) are incremented by one in the *INC-BIN* state. At the final histogram's updating process in the *WR-BIN* state, the incremented counts are written into the corresponding histograms. At this point, the state machine will stop processing additional phoswich pulses if a stop request has been received from the PC side. Otherwise, it will move to the *START* state and will wait for the next trigger signal.

The Real and Live Counters, shown in Fig. 5, are handled differently to account for any dead time caused in the pulse processing algorithm. Both counters are disabled at the STOP state. While the Real Counter is enabled in all other states, the Live Counter is only enabled in the "live states" from the *START* to the *CNT3* states. By taking the latency of divider components into account, the dead time in the MCA mode is estimated to be 40 ADC's clock cycles per coincidence event.

5.4. Synthesis and implementation

The real-time pulse processing algorithm, described in the above sections, was synthesized and implemented using Xilinx's ISE WebPack software. The FPGA design was tailored to run in low-cost Xilinx's SPARTAN-3 FPGA (1000k equivalent gate) available in the RX1200 (200

MHz/12-bit digital pulse processor, Avicenna Instruments LLC). With the current FPGA design, we achieved a maximum sampling rate of 157 MHz (f_{adc}).

6. Real-time measurements

The following real-time test results were obtained with the phoswich anode's output directly connected to the RX1200. In all real-time measurements, the ADC's clock frequency (f_{adc}) was set to 150 MHz.

First, the PSA mode was used to test the performance of our real-time algorithm in pulse-shape discrimination and to determine the four boundary levels (*FRLL*, *FRUL*, *SRLL* and *SRUL*) for the region 3. The real-time FPGA-based processing algorithm was then tested with ^{135}Xe and ^{133}Xe through beta-gamma coincidence measurements.

Radioxenon gases were produced by activating small volumes (3 ml) of stable and enriched (>99%) isotopes of xenon, ^{134}Xe and ^{132}Xe, in the thermal column of the TRIGA reactor for two hours. The resulting 3-D beta/gamma coincidence energy spectra from ^{135}Xe and ^{133}Xe are shown in Figures 8 and 9, respectively. The spectral data in these Figures were collected using the CE mode. In this mode, coincidence events in the region 3 (BC400-CsI(Tl) coincidence events) are discriminated then the corresponding calculated pulse areas, A_g and A_b, are transmitted to the PC, event by event. ^{135}Xe emits 250 keV gamma-rays in coincidence with beta particles. Fig. 8 shows a populated area at a fixed gamma energy (250 keV photopeak) extending from zero to the maximum energy of beta particles. In Fig. 9, 30 keV X-rays and 81 keV gamma-rays in coincidence with beta particles from ^{133}Xe are well pronounced. Although both photons are emitted in coincidence with the same beta energy distribution, the beta component of 30 keV X-ray region is extended to higher energies due to conversion electrons (45 keV) from ^{133}Xe.

To test the MCA mode, separate real-time beta and gamma coincidence energy spectra from ^{135}Xe and ^{133}Xe were collected by running the processing algorithm in the MCA mode. The resulting energy spectra are presented in Figs 10 and 11. The energy resolution for the 250 keV, 30 keV and 81 keV photopeaks were measured to be 16.7%, 56.6% and 37.1%, respectively.

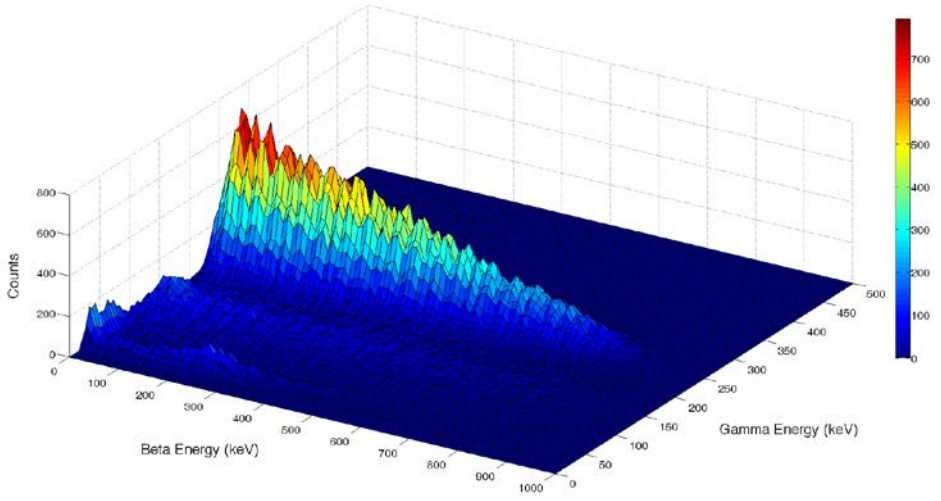

Fig. 8. ^{135}Xe 3-D beta/gamma coincidence energy spectrum. Data were collected in real-time using the "Coincidence Event" mode.

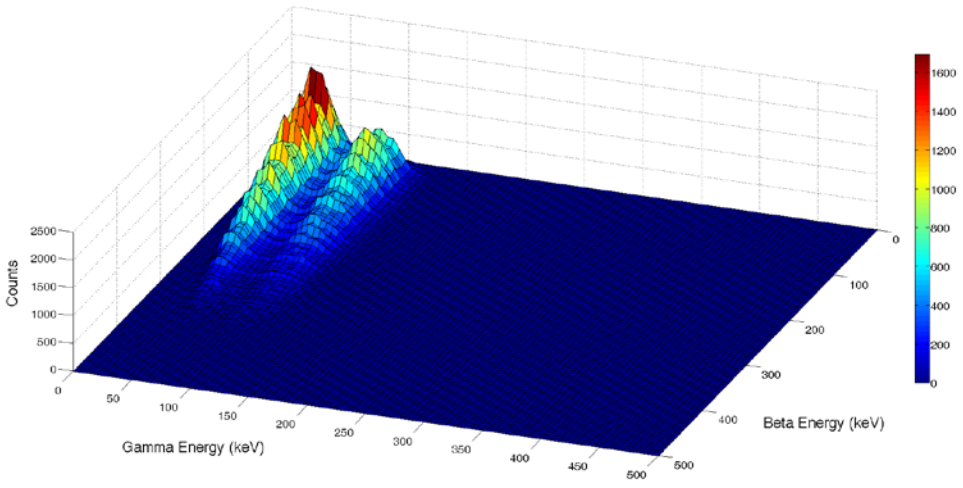

Fig. 9. ^{133}Xe 3-D beta/gamma coincidence energy spectra. Data were collected in real-time using the "Coincidence Event" mode.

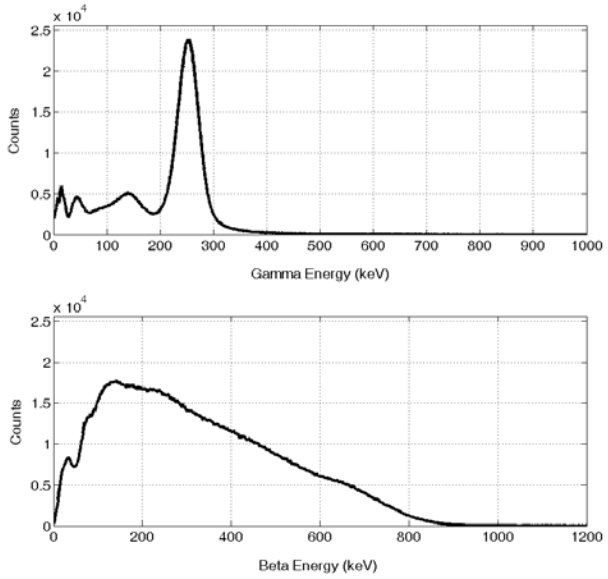

Fig. 10. Gamma (top) and beta (bottom) energy spectra from ^{135}Xe. Data were collected in real-time using the "MCA" mode.

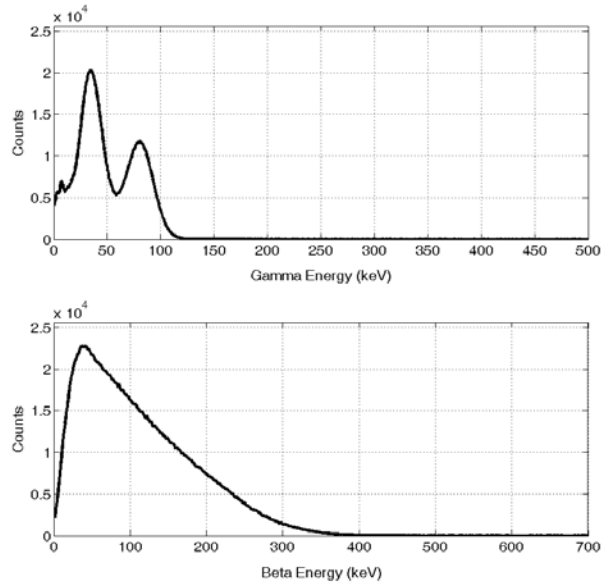

Fig. 11. Gamma (top) and beta (bottom) energy spectra from ^{133}Xe. Data were collected in real-time using the "MCA" mode.

Table 3. Energy resolution (FWHM) from selected energy photons obtained in offline and real-time measurements.

Source	Photon Energy (keV)	Energy Resolution (FWHM %)	
		Offline analysis [6]	Real-time analysis
^{133}Xe	30	46.1	56.6
	81	24.2	37.1
^{135}Xe	250	13.0	16.7
^{137}Cs	662	9.4	10.2

Table 3 shows energy resolutions (FWHM) from selected energy photons obtained in our offline and real-time measurements. As it can be seen in Table 3, the offline measurements show better energy resolutions than our real-time measurements. One possible reason might be the difference in ADC's sampling rate in these two measurements. Pulse-shape mischaracterization can be minimized by increasing the ADC's sampling rate. The ADC's sampling rate in the offline measurements were 200 MHz whereas it was 150 MHz in our real-time measurements.

While the present results for both xenon radioisotopes, shown in Figs 8-11, are in relatively good agreement with their radiological characteristics, some abnormal events are seen in low-energy parts of the energy spectra. These might be due to mischaracterization of BGO events in the region 3 in which coincidence events are identified and processed. Our pulse-shape analysis shows that events possessing a BGO component are less localized than other events and as a result they are more susceptible to be mischaracterized. Discrimination of BGO events becomes even more difficult when low-energy radiation is absorbed in the BGO. Using high-gain PMT's or improving light collection efficiency are two solutions that potentially can improve overall discrimination performance of the phoswich system.

7. Conclusion

In this paper we described the principles and development of a real-time FPGA-based digital pulse processing algorithm for our previously developed phoswich detector to discriminate pulse shapes and measure xenon radioisotopes via a beta/gamma coincidence technique. All the digital pulse processing functions including system triggering, pulse-shape discrimination, beta/gamma coincidence event detection, pileup rejection, energy measurements, and updating beta/gamma histograms were entirely realized in a single low-cost FPGA device. To be useful in both real-time measurements and prototyping stages, the pulse processing algorithm was developed for operation in four modes: (1) Scope, (2) Pulse-Shape Analysis, (3) Coincidence Event, and (4) Multichannel Analyzer modes. The performance of our digital pulse processing algorithm was tested through real-time measurements of ^{135}Xe and ^{133}Xe produced in the Oregon State University's TRIGA reactor.

Implementation of sophisticated digital processing tasks in Field-Programmable Gate Array has brought significant advantages to analyzing pulses from our phoswich detector. These include: pulse processing performed in real-time with minimal dead time; no external memory needed to construct energy histograms; a processing algorithm that is easily changed without changing hardware; accurate quantitative measurements are possible since the live time is measured in hardware; and code development made easier and less time consuming by employing only one processing device.

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