AN ABSTRACT OF THE DISSERTATION OF

Mahmoud Sadollahi for the degree of Doctor of Philosophy in Electrical and Computer Engineering, presented on February 5, 2018.

Title: Power Efficient Architectures for Medium-high Resolution Analog-to-Digital Converters.

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Gabor C. Temes

Analog-to-digital converters are essential components to the portable devices that we are using today. Wireless sensors, body implanted devices, communication devices and so forth require low power ADCs. Therefore achieving higher resolution and bandwidth with lower power consumption is targeted in ADCs design. In this work power efficient ADCs for medium-high resolution is presented.

In this dissertation first an ultra-low power successive approximation register SAR ADC is presented. The ADC is an 11-bit single-ended, low power, area efficient one with small loading effect, targeted for biomedical applications. The design features an energy-efficient switching technique to cover an input range twice the reference voltage. The ADC's loading effect to previous stage is reduced by using single-ended structure and eliminating the largest capacitor (MSB capacitor) in the switching network. All building blocks were designed in subthreshold for power efficiency, with asynchronous self-controlled SAR logic. The ADC was fabricated in 0.18 µm CMOS 2P4M process. The measured peak SNDR was 60.5 dB, the SFDR was 72 dB, the DNL +0.6/-0.37 LSB and the INL +0.94/-0.89 LSB. The total power consumption was 250 nW from a 0.75V supply voltage. This gives a Walden FoM of 28.8 fJ/Conv-step.

In addition, a noise-coupled VCO-based quantizer is presented. By applying the noise-coupling technique a second order noise-shaped quantizer is achieved, which gets one order from VCO-quantizer and another order from noise-coupling technique.

This quantizer is employed as the second stage in a 2-2 MASH delta-sigma modulator with 4rd order noise-shaping. Thus the input signal range of the VCO is the quantization error of the first stage and it is in the linear range of the VCO. OPAMP sharing technique is used between the first and second stage to save power. Proposed architecture was designed and implemented in 0.18 µm CMOS 2P6M process at sampling frequency of 160 MHz with 8 MHz bandwidth. The achieved peak SNDR is 80.54 dB and SFDR is 94 dB.

Finally a 3rd order passive delta-sigma modulator employing a VCO-based quantizer is presented. A conventional passive delta-sigma modulator and proposed passive delta-sigma modulator has been designed and simulated for comparison. The results show power efficiency for the proposed structure.

Power Efficient Architectures for Medium-high Resolution Analog-to-Digital Converters

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Mahmoud Sadollahi, Author

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CHAPTER 1. INTRODUCTION

1.1 Motivation

Data converters are bridges between the real world signals and the digital signal processing DSP units. All real word signals are continuous-time continuous-amplitude signals, and they have to be converted to digital domain to be processed by DSP block. Analog-to-digital converter ADC is a block which is used for this purpose. At the end, the digital signal will be converted to analog through digital-to-analog converter DAC to provide the output signal for actuators. Figure 1.1 shows system-level block diagram of general digital-signal processing and its interface between real world signals.

Analog-to-digital converter (ADCs) are essential function to take advantages of digital processing. There are different type of ADCs and they can be categorized as Nyquist-rate and oversampled ADCs [1]. Each of these categories can be implemented in different architectures depending on the application and required specification. They can be very low–bandwidth to very high-bandwidth, low resolution to high resolution for biomedical applications, audio-signal processing, video-signal processing, communication and so on. The power efficiency is a key parameter in recent ADCs, because of increasing demand of portable application to electronic devices.

Biomedical application requires a low-bandwidth, medium resolution but ultra-low power ADC while wireless communications require medium-to-high resolution and very high-speed ADCs. The power efficiency is important for these applications because they are mostly portable devices and for long-time battery life they have to be power efficient.

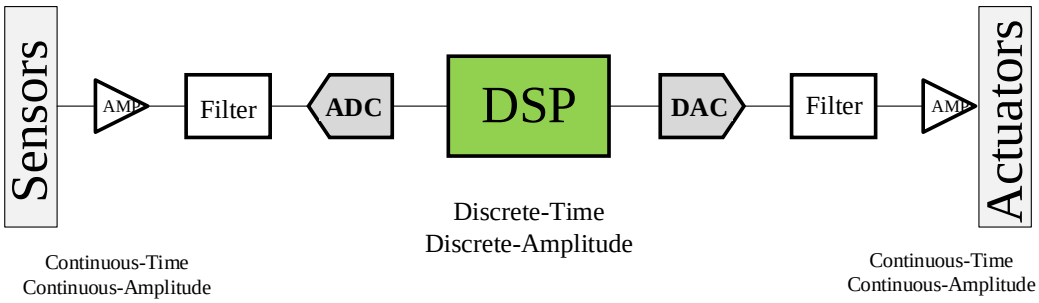


Fig. 1.1 Interface between real world signal and digital signal processing.

In this dissertation, ADCs in both Nyquist and oversampled analog-to-digital converters are designed and analyzed. An improvement in power efficiency is presented in both.

1.2 Contributions

- A switching technique is proposed for successive-approximation register (SAR) analog-to-digital converter. This scheme reduces the switching energy of the ADC.
- A power efficient SAR ADC is proposed and implemented based on the switching scheme. It can cover two-times input range of the reference voltage.
- A noise-coupled VCO-based quantizer is proposed to improve the order of noise-shaping in VCO-based quantizer.
- A 2-2 Multi-stAge noise-SHaping MASH, delta-sigma ADC is designed and implemented based on the noise-coupled VCO-based quantizer.
- To reduce the power dissipation an OPAMP sharing technique is used between the stages of 2-2 MASH.

- A passive delta-sigma ADC is designed and proposed with VCO-based quantizer.

1.3 Organization of Dissertation

Chapter 2 reveiws the Nyquist rate and oversampling ADCs architecture and the required specification for different applications. It focuses on the SAR architecture in Nyquist-rate and discrete-time delta-sigma in oversampling ADC, the two structures of the proposed ADCs are covered in the next Capters.

Chapter 3 describes and presents the proposed SAR ADC. It covers the analysis and circuit design procedure and requirement for the proposed SAR ADC. It presents the simulation and measurement results. It is an asynchronous SAR ADC with 11-bit resolution, 5KHz bandwidth and 250 nW power dissipation. Most of the material in this chapter is published in:

M. Sadollahi, K. Hamashita, K. Sobue and G. C. Temes, "An 11-Bit 250-nW 10-kS/s SAR ADC With Doubled Input Range for Biomedical Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 61-73, Jan. 2018.

In Chater 4, a noise-coupled VCO-based quantizer is presented and a 2-2 MASH delta-sigma ADC is proposed based on that. OPAMP sharing techniques is used between the MASH satges for even more power efficency. The architecture is analyzed and the required building blocks are designed and implemented. It covers the result and disscusion of the ADC. Some part of this is presented at:

M. Sadollahi and G. Temes, "Two-stage ΔΣ ADC with noise-coupled VCO-based quantizer," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 305-308.

Chapter 5 disscusses the passive delta-sigma ADC and presents a passive delta-sigma ADC with VCO-based quantizer. it compares the proposed structure with

conventional passive delta-sigma ADC. It provides the simulation results. Some part of this chater presented at:

M. Sadollahi and G. C. Temes, "Passive 3rd order delta-sigma ADC with VCO-based quantizer," *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, 2017, pp. 743-746.

Finally, Chapter 6 summerizes the contribution of this research and concludes the dissertation.

CHAPTER 2. NYQUIST-RATE AND OVERSAMPLING ADCS

Analog to digital converters ADCs are key building blocks to electronic systems. They are the part of the front-end in radio-frequency RF receivers, sensor circuits and sensor networks, audio and video systems, medical devices and instruments and etc.

There are different architectures to implement an ADC depending on the required resolution and bandwidth. Fiquire 2.1 illustrates the state-of-the-art ADCs with different architectures based on achieved resolution and bandwidth [12]. The ADCs which process and quantize signals at, or slightly above the Nyquist rate are refered as Nyquist rate ADCs. This includes architectures such as flash, folding, two-step, pipeline, or succesive-approximation-register (SAR). This category is mostly low-to-medium resolution and medeium-to-high bandwidth.

The other category is oversampled ADCs, which are delta-sigma modulators. They can achieve very high resolution with employing a low resolution quantizer. The sampling rate at this type of ADC is much higher than the bandwdith, and it can shape the in-band noise and achieve high accuracy by oversampling. Delta-sigma modulator can be implemented in discrete-time or continuous-time structure, where each of them has pros and cons. Recently many techniques have been presented to improve the performance of delata-sigma ADC, including VCO-based quantizer, time domain and etc.

This chapter disscuses and reviewes Nyquist-rate ADC, specifically the SAR architecture, and oversampling ADC, delta-sigma modulator, to provide enough background for next chapters.

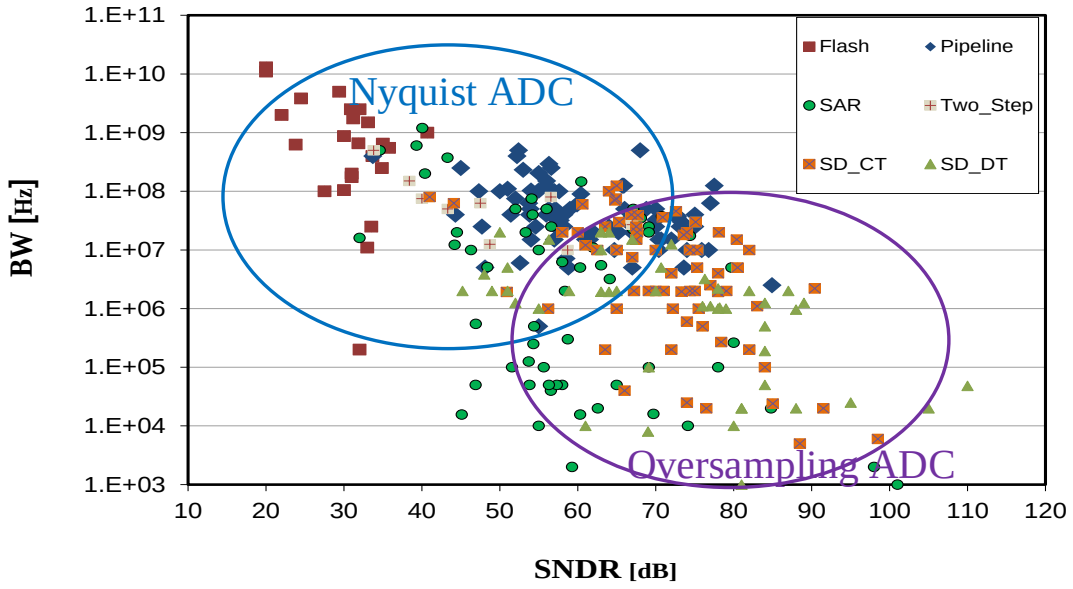


Fig. 2.1 Bandwidth vs resolution for different ADC architectures.

2.1 Nyquist-Rate ADCs

Figure 2.2 shows the general block diagram and power spectrum of Nyquist-rate ADC. Those are suitable for high-speed but low-medium resolution application. There are different Nyquist-rate ADC architectures. The simplest architecture is flash quantizer, which consists of comparators and thermometer-to-binary decoder. The other architecture is a pipeline, which consists of several stages working together. Another architecture which got attention again is successive-approximation register SAR. SAR ADC is the most suitable architecture for low power applications. Biomedical devices is one of the areas where power consumption is very restricted. Specifically for body implanted devices, the long-time battery life, and the power dissipation should be very low.

Figure 2.3 shows different biomedical signals specifications [11]. Those signals frequency range is from DC to few kHz and their magnitude range is from µV to mV. The required ADC's specifications in these applications are 8-12 bit resolution, few kHz bandwidth and µW-nW power dissipation.

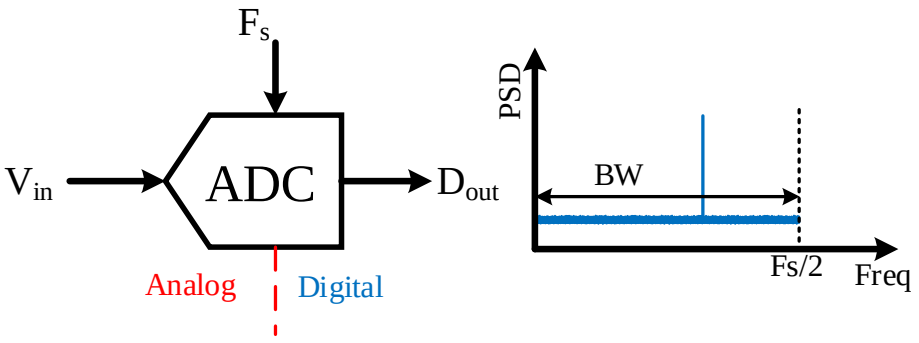


Fig. 2.2 Nyquist-rate ADC's block diagram and power Spectrum density.

SAR ADC consists of a comparator, DAC and digital timing block as shown in Fig. 2.4. Switching energy in capacitive DAC, comparator power and digital power are the three power dissipation parts. To achieve ultra-low power, all of these three blocks should be designed for ultra-low power.

Monotonic switching scheme [15], V_{cm}-based switching scheme [19] and merged-capacitive switching scheme [20] for capacitive DAC are the methods to reduce the switching energy in DAC comparing to conventional switching scheme in SAR ADC.

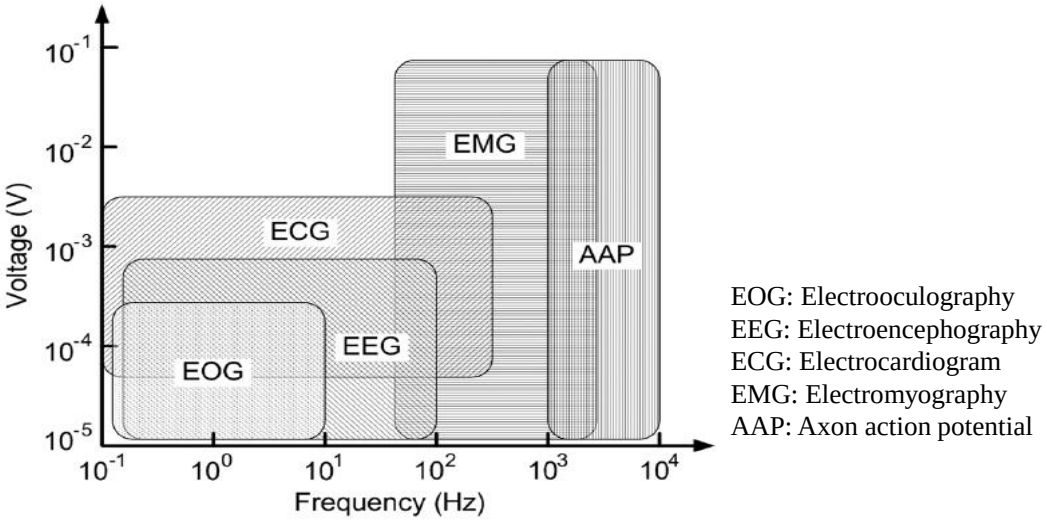


Fig. 2.3 Different biomedical signals specifications.

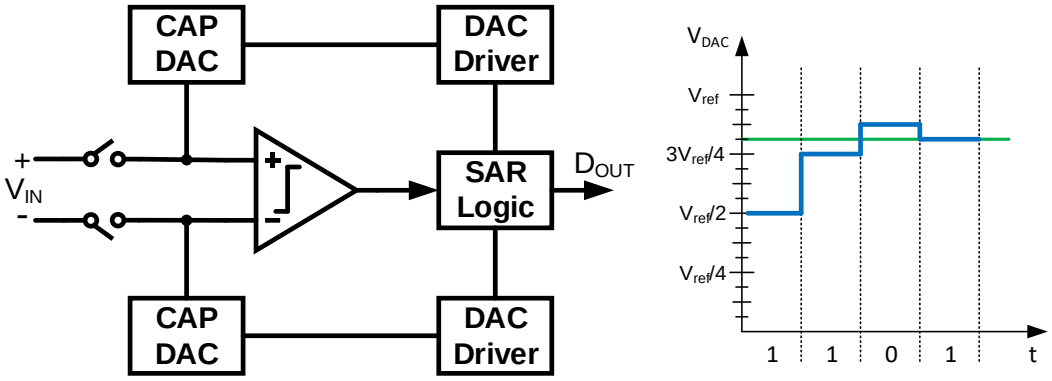


Fig. 2.4 SAR ADC block diagram.

Single-ended implementation is another way to save power in biomedical application, since it reduces total capacitance size. However the mentioned switching schemes are differential and cannot be implemented in single-ended structure. Also if some can use smaller reference voltage to cover same input signal range in SAR ADC, it can save even more power, based on Eq (2.1)

$$E_{sw} = \frac{1}{2} C_{tot} V_{ref}^2 \tag{2.1}$$

In chapter 3, we present an ultra-low power SAR ADC for biomedical applications.

2.2 Oversampling ADCs

Figure 2.5 shows the general block diagram and power spectrum of oversampling ADC. Since the quantization noise are shaped, oversampled and then filtered-out, this architecture is suitable for high-resolution applications.

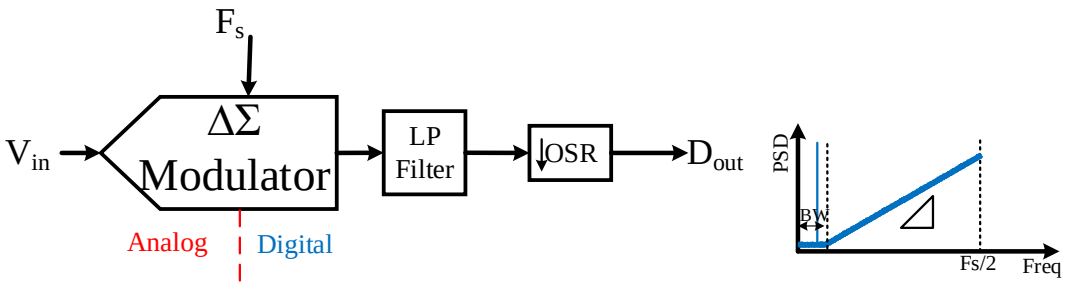


Fig. 2.5 Oversampling ADC block diagram and power spectrum density.

The design of the ΔΣ ADC involves different design challenges and trade-offs to optimize their performances in terms of resolution, bandwidth and power consumption. These issues can be categorized as system level issues (including stability, linearity range, and clock jitter) and circuit level issues (including loop filter, quantizer, and feedback DAC and clock generation). Significant efforts have been made to increase the bandwidth and reduce the power consumption of the ΔΣ ADCs. Figure 2.6 shows a survey on the ΔΣ ADC in terms of energy, number of bits and architecture [2].

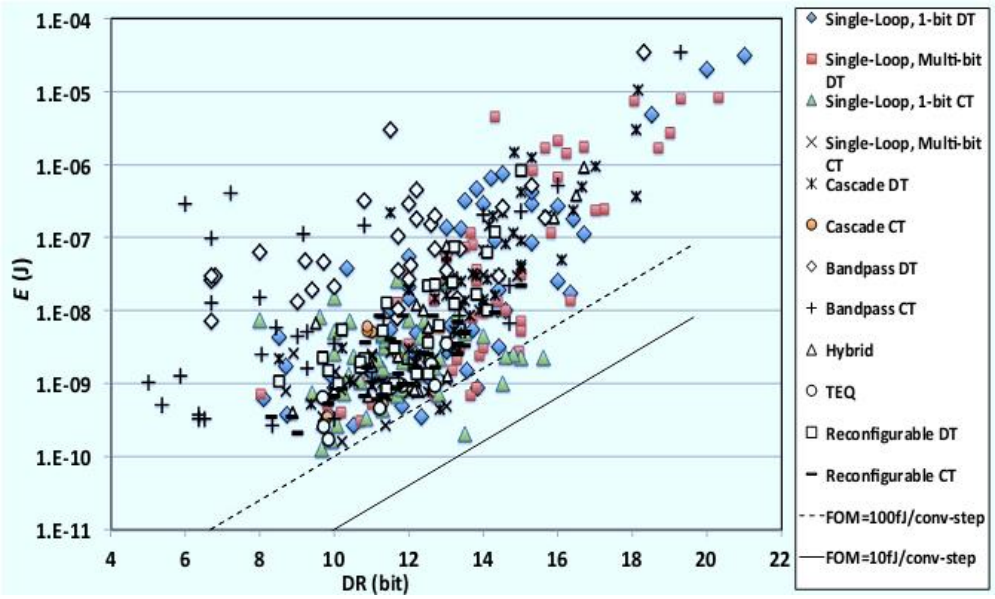


Fig. 2.6 State-of-the-art ΔΣ ADC's energy plot vs. DR [2].

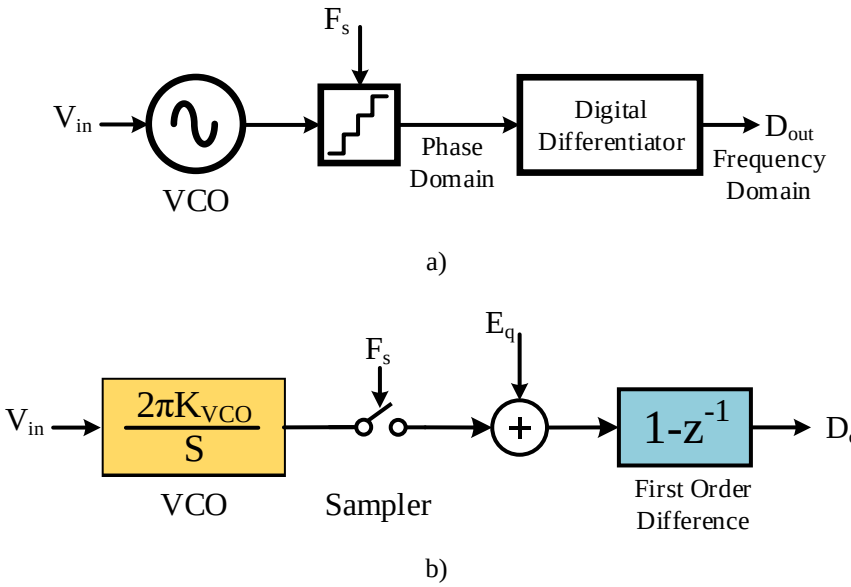


Fig. 2.7 a) Block diagram and b) behavioral model of the VCO-based quantizer.

One way to improve the SNDR in ΔΣ modulator is to increase the loop-filter order. Higher loop-filter order in single-loop can cause stability issue. A solution for this issue is cascading of low-order modulators to achieve high-order loop filter which is known as MASH architecture. Every increase in loop-filter order requires additional OPAMP, which means more power dissipation. Also each stage would require its own quantizer which adds even more power consumption.

Recently the voltage controlled oscillator (VCO)-based ADCs have emerged as an attractive solution due to their highly digital circuit architecture, inherent noise shaping characteristic, as well as anti-aliasing property. Fig. 2.7 shows the block diagram and behavioral model of the VCO-based quantizer [51]. This quantizer can provide first order of noise-shaping besides the quantizing the input signal. The signal transfer function and noise-transfer function is:

$$STF = \frac{D_{out}}{V_{in}} = \frac{2NK_{VCO}z^{-1}}{F_s}$$
$$NTF = 1 - z^{-1} \quad (2.2)$$

Where N is the number of levels, K_{VCO} is the oscillator gain and F_s is the sampling frequency [52]. However, the nonlinear behavior of the VCO, voltage-to-frequency characteristic has severe limitation on the performance of the VCO-based ADC.

In chapter 4, we will present a noise-coupled VCO-based quantizer that acheives second order of noise-shaping. To enhance the dynamic range, the proposed noise-coupled VCO-quantizer is employed at second stage of 2-2 MASH architecture. To improve the power efficency, first and second stage shares the OPAMP. The details of the design and result will be covered as well.

CHAPTER 3. AN 11-BIT 250-nW 10-kS/s SAR ADC WITH DOUBLED INPUT RANGE for BIOMEDICAL APPLICATIONS

Abstract

This chapter presents a low power, area efficient 11-bit single-ended successive-approximation-register (SAR) analog-to-digital converter (ADC) targeted for biomedical applications. The design features an energy-efficient switching technique with an error cancelling capacitor network. The input range is twice the reference voltage. The ADC's loading of the previous stage is reduced by using a single-ended structure, and by eliminating the largest capacitor in the array. The common mode voltage of the input signal can be used as reference voltage. All building blocks were designed in subthreshold for power efficiency, with an asynchronous self-controlled SAR logic. The ADC was fabricated in 0.18 µm CMOS 2P4M process. The measured peak SNDR was 60.5 dB, the SFDR was 72 dB, the DNL +0.6/-0.37 LSB and the INL +0.94/-0.89 LSB. The total power consumption was 250 nW from 0.75V supply voltage [42, 43].

3.1 Introduction

Biomedical wearable sensors or implanted devices, such as defibrillators, retinal prosthesis and pacemakers, require ultra-low power consumption since their longtime operation is restricted by battery life [3-9]. The interface of such biomedical devices consists of several blocks. The analog-to-digital converter ADC is a key block in the interface, and ultra-low power consumption is mandatory for longer operation. Also, it is necessary to minimize the area of the ADC for such

applications. In addition, the loading of the preceding stage, which usually is a sensing amplifier, is another key parameter to consider in the design of the ADC [3, 7, and 8, 44]. Thus, in ADC design low power, small area and small loading effect are the key parameters [10, 11].

Successive approximation register SAR ADCs have recently gained renewed attention because of their low power, simple structure and minimal analog circuitry [12, 65]. In advanced process it is possible to achieve very good performance with SAR ADC [13]. Biomedical signals are usually slow (DC to a few kHz) [14], and for low speed applications SAR ADCs are the best candidates to achieve low power consumption. The power dissipation in SAR ADC consists of the switching power of the capacitive DAC network, comparator power (analog) and SAR control logic power (digital). To achieve ultra-low power operation, it is necessary to reduce the power consumption of all of these three main blocks.

The switching power of the capacitive DAC (digital-to-analog converter) in a SAR ADC is related to the switching activity, capacitor size and reference voltage V_{ref}. There are many research papers on how to reduce this switching power [15-22]. Monotonic or set-and-down switching [15] has been presented recently to reduce the amount of switching activity. It allows up to 81% energy saving comparing to conventional switching scheme. V_{cm}-based switching [22] has been proposed to reduce the effective voltage range of charging and discharging the capacitive DAC, and thus save switching power. This scheme saves up to 87% switching power compared to the conventional switching scheme. Also in [23] a bidirectional switching technique is presented. These schemes use differential structures, and they require two reference voltages (+/-V_{FS}/2) or (0, V_{FS}), where V_{FS} is the full-scale input range. Extra reference voltage generation needs added power. Also, the loading effect of these structures to previous stage is twice that of the single-ended capacitor DAC. Thus, a single-ended structure is preferable for biomedical applications to reduce the area, power consumption, loading effect, and also to avoid the need for a common-mode feedback circuit [24]. However, the trade-off is in the

design complexity for comparator and common-mode variation effects. An estimation based noise reduction presented in [26] to relax the comparator.

Advanced CMOS processes benefit from smaller feature size, lower threshold voltage and higher bandwidth, but they have higher device leakage current [9]. Therefore besides accommodating a small supply voltage, we have to minimize the leakage power to achieve best power efficiency. Since the signals in biomedical applications are slow, larger feature size processes with lower leakage current can be used, if one can optimize the design for smaller power supply and minimum area.

In this paper, a single-ended SAR ADC with a doubled (0 - $2V_{ref}$) input range and an error-and-offset canceling capacitor network is described. In this scheme, first the most significant bit (MSB) is detected directly after sampling without any switching activity. This saves 50% of total capacitance size, and thus of the switching energy. Next, a one-bit DAC is used to choose the comparator's reference voltage V_{ref} as 0 or $V_{FS}/2$ depending on the MSB's value. The capacitors are charged from a voltage source $V_{ref} = V_{FS}/2$ which is half of the reference voltage of the conventional single-ended SAR ADC, and therefore the switching power is reduced by a factor over 4.

The proposed switching scheme gives an 87.5% reduction in switching power loss compared to the conventional single-ended counterpart SAR ADC. Also, this scheme requires $V_{FS}/2$ as the reference voltage. This is the common-mode level of the previous stage's output. Therefore the circuit does not require a dedicated reference voltage generator; the common-mode voltage which is generated in the preceding blocks can be used as reference voltage for this ADC. A single-ended split capacitor DAC with a bridging capacitor is used to allow a small total capacitance. This leads to smaller area and loading effect.

This paper also proposes a novel comparator. It is designed to operate in the subthreshold region to have very low power consumption. An adjustable calibration capacitor array is used to cancel charge error caused by parasitic capacitors, and also the comparator's offset variation when switching comparator's reference voltage

between 0 and V_{ref}. The power supply of the ADC is 0.75V and the process is 0.18 µm CMOS, which allows a significant reduction in the leakage current and power needed in the logic circuits. Also, high threshold-voltage devices are used in the logic circuitry to reduce the leakage current further.

3.2 Proposed SAR ADC Architecture

Figure 3.1 shows the architecture of the proposed 11-bit SAR ADC with $2V_{ref}$ input range. It consists of a single-ended switched capacitor network DAC, a low-power comparator, the asynchronous SAR control logic, comparator reference control, and parasitic capacitor error/comparator offset cancellation network. The DAC uses a 10-bit split scheme with a bridge capacitor. Since the MSB determination does not require DAC switching, a 10-bit DAC can be used for an 11-bit ADC. The DAC is divided into two 5-bit networks (MSB DAC and LSB DAC) to optimize the area and power. The comparator reference control connects the non-inverting input of the comparator to V_{ref} or GND, depending on the MSB value. The comparator uses a preamplifier and latch to meet the noise and accuracy requirements. The SAR control logic controls the DAC switches, based on the comparator decisions and control signals [42, 43].

The operation of the ADC is as follow: As shown in Fig. 3.1 there are three operation phases; sampling phase (samples the input signal), conversion phase (converts the sampled input signal to digital form) and reset phase (resets the ADC to prepare for the next sample). During the sampling phase, the bottom plates of all capacitors are connected to the input signal, and all top plates are connected to the reference voltage (V_{ref}). Therefore, the signal on all capacitors will be $V_{cap} = V_{ref} - V_{in}$. At the same time, the noninverting input of the comparator is connected to V_{ref}, and the parasitic error/comparator offset cancelling capacitor C_c is connected between $2V_{ref}=V_{DD}$ and V_{ref}.

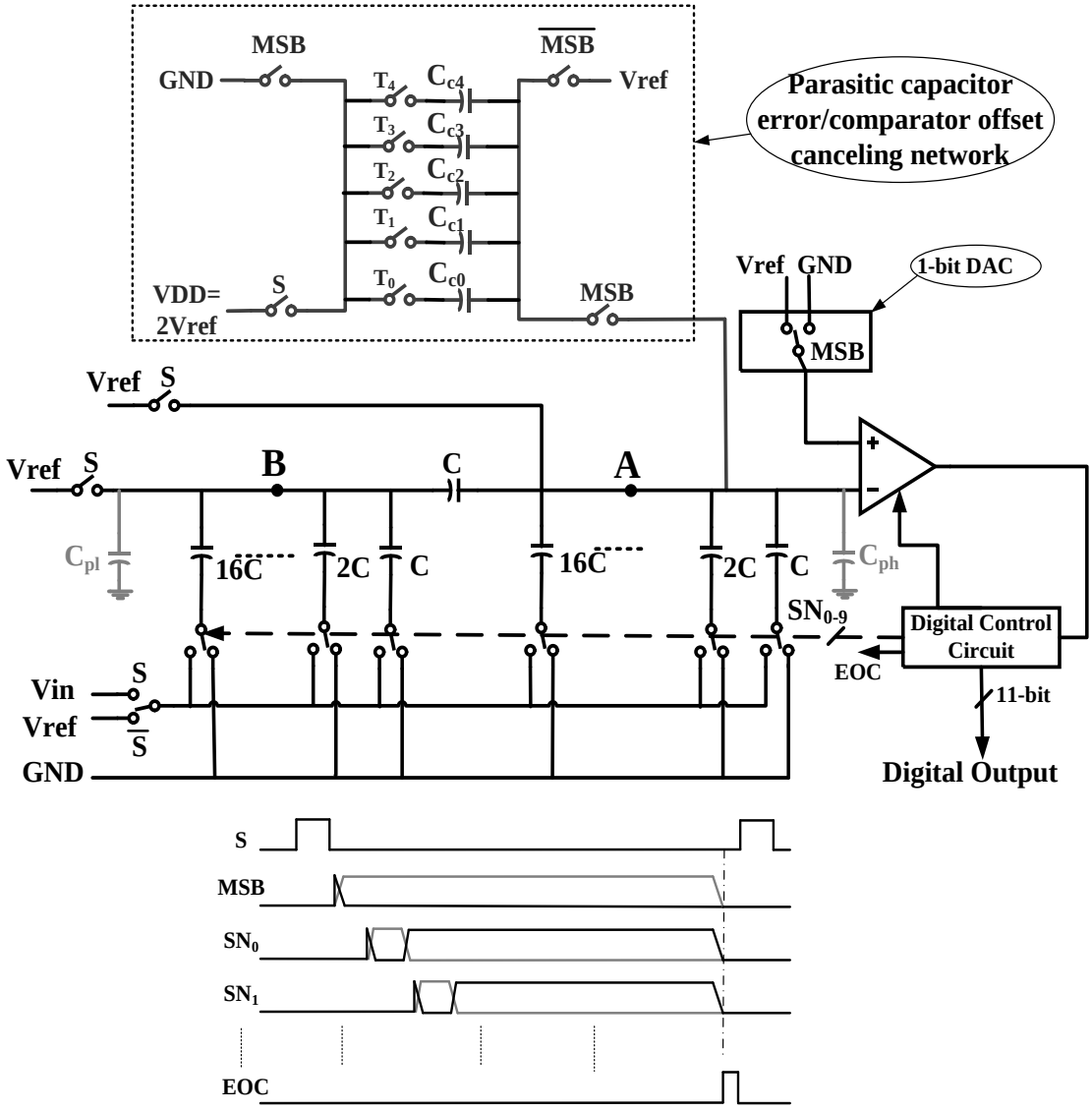


Fig. 3.1 The proposed SAR ADC architecture and timing signals.

When the sampling clock transitions from '1' to '0', the bottom plates of all capacitors will be disconnected from the input signal, and connected to V_{ref}, while the top plates of the capacitors will be disconnected from V_{ref}. Therefore the voltage across the capacitors will move up by V_{ref}, and the voltage at nodes *A* and *B* will be $V_{A,\,B} = 2V_{ref} - V_{in}$. This step does not take charge from reference voltage source to

charge the capacitors, and hence no energy is consumed at this step, except for the very small amount of energy that is taken to charge the parasitic capacitors at node *A* (C_{ph}) and *B* (C_{pl}).

At this time, the most-significant-bit (MSB) is detected by comparing the voltage at node *A* (inverting input of the comparator) with V_{ref} (noninverting input of the comparator). The MSB detection is performed without any switching activity and energy consumption unlike in a traditional SAR ADC. The detected MSB bit will be stored at SAR logic circuit, and sets the reference voltage of the 1-bit DAC to be V_{ref} or GND.

Next, depending on the MSB value, there will be two paths to detect the rest of bits.

If MSB = 0, so that the input signal is smaller than V_{ref} and $0 < V_{in} < V_{ref}$, the positive input of the comparator will stay connected to V_{ref}, and the rest of the comparisons will continue using V_{ref} as reference voltage. To detect the MSB-1 bit, the MSB-1 capacitor switches from V_{ref} to GND. Now the voltage at node *A* will be $V_A = 2V_{ref} - V_{in} - 1/2V_{ref}$. This voltage will be compared to V_{ref}, and based on the result MSB-1 will be detected and stored in the SAR logic circuit. This procedure will continue until the Least-Significant-Bit (LSB) is detected.

If MSB = 1, so the input signal is greater than V_{ref} and $V_{ref} < V_{in} < 2V_{ref}$, the noninverting input of the comparator will be switched from V_{ref} to GND, and rest of the comparisons will continue using GND as reference voltage. To detect the MSB-1 bit, the MSB-1 capacitor switches from V_{ref} to GND, and the voltage at node *A* will be $V_A = 2V_{ref} - V_{in} - 1/2V_{ref}$. This voltage will be compared to GND, and based on that, MSB-1 will be detected and stored in the SAR logic circuit. This procedure will again continue until the least-significant-bit is detected. The flow chart of the proposed SAR ADC is shown in Fig. 3.2. The voltage of node A can vary below GND. Therefore, a PMOS switch was used to connect the C_c to node A (MSB switch) to avoid any possibility of the latch-up.

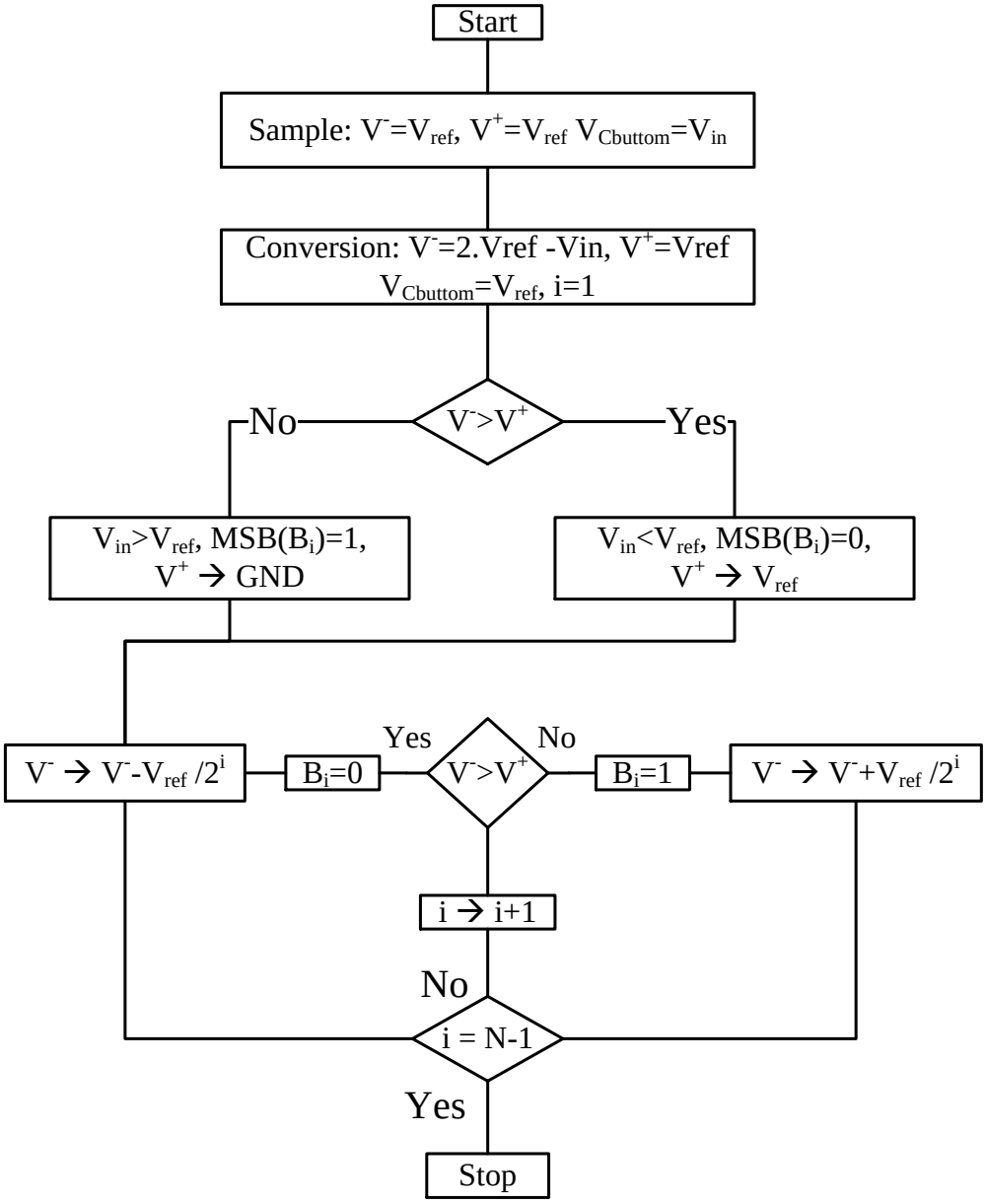


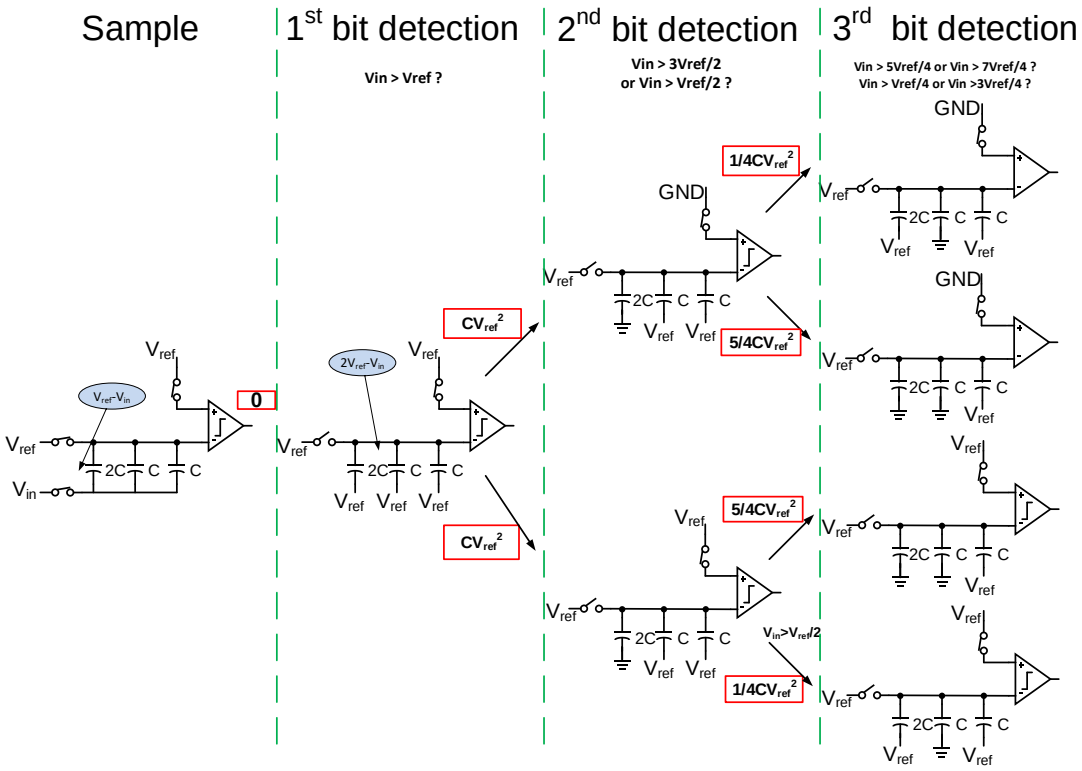
Fig. 3.2 Flow chart of the proposed SAR ADC.

Figure 3.3 shows an example of the operation for a 3-bit ADC, and the possible two cases that can occur for the voltage waveform at the DAC's output signal (inverting input of the comparator).

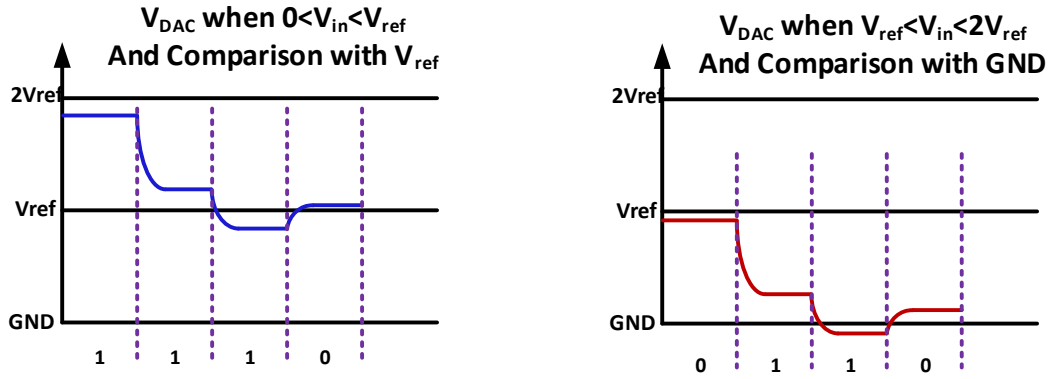
As shown in Fig. 3.3, when MSB = 0, the voltage at node *A* (inverting input of the comparator) goes to V_{ref} eventually, and since the initial voltage at this node was V_{ref} as well, therefore the charge injected by the parasitic capacitor (C_{ph}) will not introduce error at the final digitized output code. But when MSB = 1, the voltage at node *A* goes to GND eventually, and the parasitic capacitor will introduce error, since its initial voltage was V_{ref} and the final voltage is GND. The charge injected by this parasitic capacitor is $C_{ph}V_{ref}/C_{tot}$, and resulting error will be:

$$\Delta V_{A-err} = \frac{C_{ph}V_{ref} - C_{ph}V^{+}}{C_{tot}} \tag{3.1}$$

Here $\Delta V_{A\text{-}err}$ is the voltage error at node *A*, C_{ph} is the parasitic capacitance at node *A*, V^{+} is the voltage at the noninverting input of the comparator, and C_{tot} is total capacitance of the main DAC. Figure 3.4 shows the effect of this error for 50fF and 100 fF parasitic capacitance where the LSB capacitor size is C=100 fF. It causes dead band or undetected range of input signal around the midpoint transition. To cancel this voltage error, caused by switching the reference between V_{ref} and GND, a parasitic error canceling network is introduced. The parasitic capacitance is estimated at node *A* by post-layout extraction, and an adjustable capacitor array $\mathbf{C_c}$ containing series and parallel capacitors with unit size of 2.75 fF is used to provide a matching charge to cancel the voltage error caused by the parasitic capacitor. Capacitor C_c is charged initially to V_{ref} in the sampling phase, and if MSB = 1 it will be connected to node *A* and discharged to this node. This capacitor network C_c also is used to cancel the error due to the comparator's offset difference introduced by reference voltage switching to GND or V_{ref} at the noninverting input of the comparator. This will be explained in the next Sections.



a)



b)

Fig. 3.3 a) Switching procedure and switching energy for 3-bit example of the proposed structure, b) Voltage waveforms at non-inverting node of comparator.

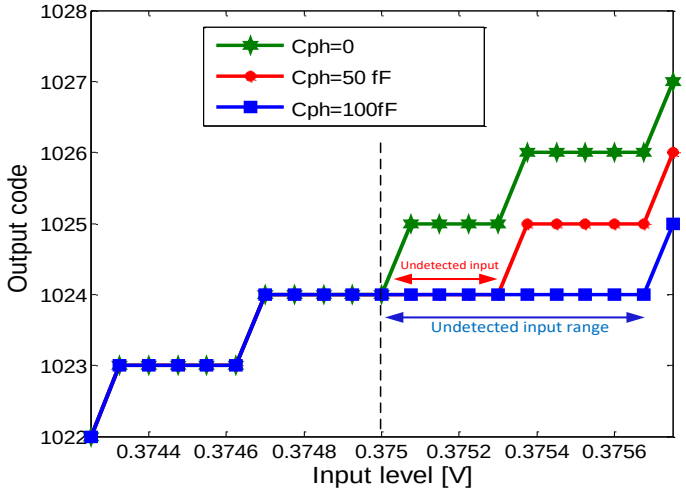


Fig. 3.4 Output code for different C_{ph} around midpoint transition.

Comparison of the proposed SAR ADC with a single-ended conventional SAR ADC shows that the total capacitance is reduced to half, since finding the MSB does not require a capacitor, and the reference voltage is reduced to half for the same input range and therefore the switching energy is reduced. The total switching energy for the proposed SAR ADC is 12.5% of that of the conventional single-ended SAR ADC. Comparing it to the monotonic switching [15] and Vcm-based switching [16], the proposed SAR ADC uses similar technique to detect the MSB without capacitor switching and thus to eliminate the MSB capacitor, but monotonic and Vcm-based switching require differential implementation, while the proposed architecture is implementable by a single-ended structure which saves power and chip area. Therefore, the total capacitor size is half of the monotonic and V_{cm}-based switching, and also the reference voltage is half of the reference voltage for same input range. The switching energy for the different structures was calculated and simulated for the same resolution, same binary weighted capacitor DAC and same input range. The average energy formulas for different switching schemes are given below

$$E_{avg,Conv} = \sum_{i=1}^{n} 2^{n+1-2i}\left(2^{i}-1\right)CV_{ref}^{2} \tag{3.2}$$

$$E_{avg,Monotonic} = \sum_{i=1}^{n-1} 2^{n-2-i}CV_{ref}^{2} \tag{3.3}$$

Figure 3.5 plots the switching energy versus the output code for the proposed structure and for the previously reported structures.

Another important aspect is the common-mode voltage of the comparator. In the monotonic and V_{cm}-based structures, the final voltage of the comparator's input (DAC's output) is code dependent, and varies with input signal, from GND-to-V_{ref}. This introduces a signal dependent dynamic offset for the comparator. But in the proposed structure the final voltage of the comparator's input (DAC's output) will have one of two values: GND if $V_{ref} < V_{in} < 2V_{ref}$ or V_{ref} if GND$< V_{in} <V_{ref}$. This will introduce only an MSB dependent offset difference, which will be cancelled by the error/offset canceling capacitor network C_c.

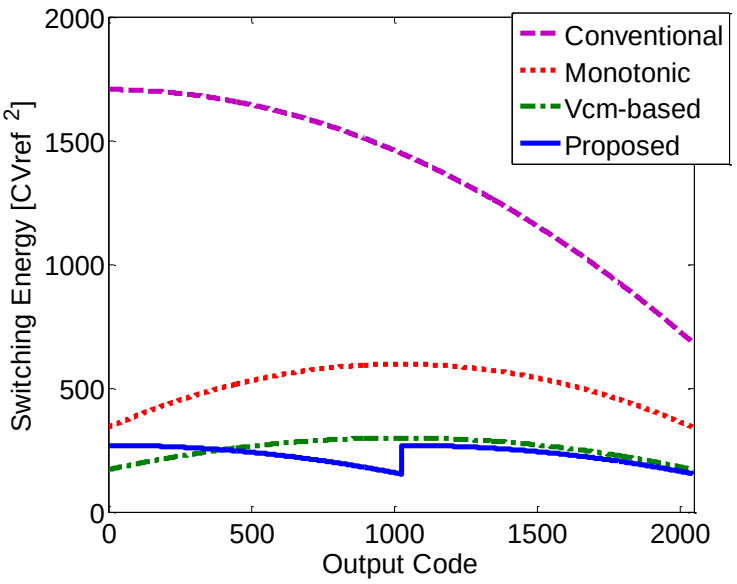


Fig. 3.5 Switching energy versus output code comparison.

3.3 Circuit Realization of the Proposed SAR ADC

This Section describes the circuit design and layout considerations of the capacitive DAC, comparator, and asynchronous SAR control logic.

3.3.1 Capacitive DAC

The capacitive DAC was implemented with a split architecture (MSB DAC and LSB DAC) with a bridge capacitor [27, 28], to reduce the total capacitor size and therefore the power consumption and area (Fig. 3.6). The ratio between MSB DAC (M-bit) and LSB DAC (L-bit) is determined by considering the number of unit capacitors and total area. Since there is $1/2^M$ gain from LSB DAC to MSB DAC, by choosing an equal or higher value for MSB DAC, the MSB DAC dominates the total mismatch error, so we can ignore the mismatch error from the sub DAC.

Table 3.1 shows the total number of unit capacitors for different combinations of the M and L for a 10-bit DAC. In this design L=M=5 has been chosen for power and area efficiency.

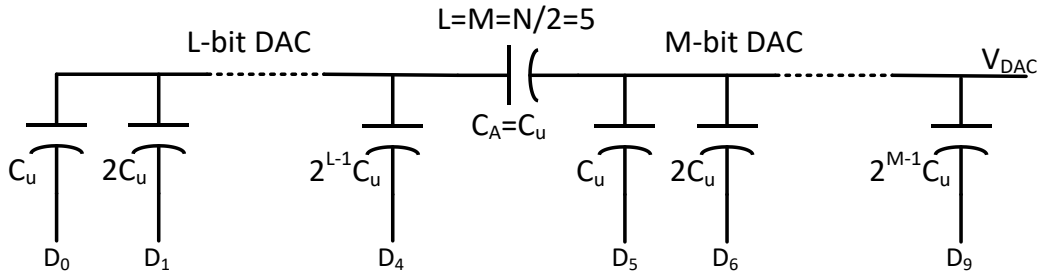


Fig. 3.6 Capacitive DAC with unit bridge capacitor.

TABLE 3.1. TOTAL NO. OF C_U FOR DIFFERENT M AND L COMBINATION

M	1	2	3	4	5	6	7	8	9
L	9	8	7	6	5	4	3	2	1
No. of C_u	513	260	136	80	64	80	136	260	513

The power consumption of a capacitive DAC is directly propositional to the unit capacitor size C_u in the DAC array [31]. The smallest value of the C_u is determined by the minimum value of capacitor which satisfy the following criteria [27, 28]: 1) thermal noise power *kT/C*; 2) the required capacitor matching accuracy (DNL, INL); 3) design rules and parasitic capacitance of the technology. Usually the matching property is the dominant condition in finding the unit capacitance C_u for medium/ high resolution SAR ADCs [32]. The worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) for the used capacitive DAC is calculated as follow.

3.3.1.a Capacitor mismatch and static linearity, DNL/INL

To calculate the static linearity of the binary-weighted capacitor array with bridge capacitor, each of the capacitors can be considered by its nominal value and some error

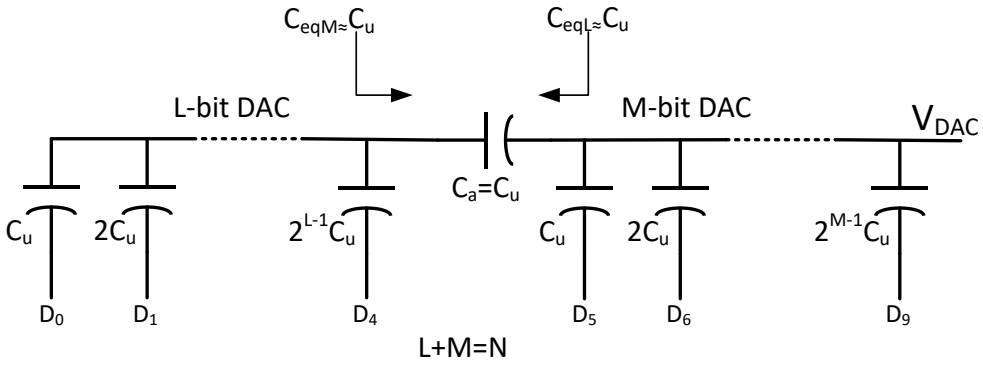


Fig. 3.7 Capacitor DAC array with bridge capacitor.

$$C_n = 2^n \left(C_u + \Delta C_u \right) \tag{3.4}$$

For capacitor mismatch with a σ_0 standard deviation, the mean-square error will be

$$E[\Delta C_n^2] = 2^n \sigma_0^2 \tag{3.5}$$

and the ADC output with b_i digital bits will be

$$V_{out}(n) = \frac{\sum_{i=1}^{n} (C_i + \Delta C_i) b_i}{C_{tot}} V_{ref} = D_{out} V_{ref} \tag{3.6}$$

The DAC error and its variance can be calculated from (17)-(19) as

$$V_{err}(n) = \frac{\sum_{i=1}^{n} \Delta C_i b_i}{2^N C_u} V_{ref} \tag{3.7}$$

$$E[V_{err}^2(n)] = \frac{\sum_{i=1}^{n} 2^{n-1} \sigma_0^2 b_i}{2^{2N} C_u^2} V_{ref}^2, \quad LSB = \frac{V_{ref}}{2^N} \tag{3.8}$$

For ADC we can calculate the DNL and INL by finding the maximum error of

$$\begin{aligned} DNL(n) &= V_{out}(n) - V_{out}(n-1) - (LSB) \\ INL(n) &= V_{out}(n) - V_{ideal}(n) \end{aligned} \tag{3.9}$$

The worst case for nonlinearity is the transition for the MSB, (0111...1) to (1000...0). By calculating the DAC voltage from Fig. 3.7 we can get the error of this transition. The DAC voltage V_{DACi} in Fig. 3.7 is

$$V_{DACi} = \frac{\sum_{i=1}^{M} \frac{D_{Mi}}{2^i} C_{Mi}}{C_{totM} + C_{eqL}} + \frac{\sum_{i=1}^{L} \frac{D_{Li}}{2^i} C_{Li}}{C_{totL} + C_{eqM}} \frac{C_a}{C_{totM} + C_a} \tag{3.10}$$

Here, C_{Li} is for the LSB DAC capacitor and C_{Mi} is for the MSB DAC capacitor. Then by calculating the DNL from (22) for the worst case and finding the variance of this error from (21) we get

$$E[DNL_{MAX}^2] = E\left[\left(\left(\frac{\delta_M}{(2^M - 1)C_u + C_{egL}}\right) - \left(\frac{\sum_{i=1}^{M-1} \delta_M}{(2^M - 1)C_u + C_{egL}}\right) - \left(\frac{\sum_{i=1}^{L} \delta i}{(2^L - 1)C_u + C_{egM}} \frac{C_a}{(2^M - 1)C_u + C_{eqL}}\right)\right)^2\right]$$

$$= E\left[\left(\left(\frac{\delta_M}{2^M C_u}\right) - \left(\frac{\sum_{i=1}^{M-1} \delta_M}{2^M C_u}\right) - \left(\frac{\sum_{i=1}^{L} \delta i}{2^L C_u} \frac{1}{2^M}\right)\right) V_{ref}^2\right] \tag{3.11}$$

By considering the standard deviation for the capacitors from (18) we can get

$$E[DNL_{MAX}^2] = E\left[\left(\left(\frac{2^{M-1}\sigma_0^2}{2^{2M} C_u^2}\right) + \left(\frac{(2^{M-1} - 1)\sigma_0^2}{2^{2M} C_u^2}\right) + \left(\frac{(2^L - 1)\sigma_0^2}{2^L C_u^2} \frac{1}{2^{2M}}\right)\right) V_{ref}^2\right]$$

$$= E\left[\left(\left(\frac{(2^M - 1)\sigma_0^2 \times 2^{2L}}{2^{2M} C_u^2}\right) + \left(\frac{(2^L - 1)\sigma_0^2}{2^{2L} C_u^2} \frac{1}{2^{2M}}\right)\right) V_{ref}^2\right] \tag{3.12}$$

Therefore the standard deviation of the DNL based on capacitor mismatch will be

$$\sigma^2[DNL_{MAX}] = \left[\left(2^M - 1\right)2^{2L} + \left(2^L - 1\right)\right]\left(\frac{\sigma_0}{C_u}\right)^2 LSB^2$$

$$\sigma[DNL_{MAX}] = 2^{N - \frac{M}{2}} \frac{\sigma_0}{C_u} LSB \tag{3.13}$$

By following a similar procedure for INL we can get

$$\sigma[INL_{MAX}] = 2^{N-\frac{M}{2}-1}\frac{\sigma_0}{C_u}LSB \tag{3.14}$$

And based on this DNL and INL equations the minimum capacitor value can be calculated to satisfy the required linearity.

In terms of the LSB, the results are

$$\sigma_{DNL,MAX} \approx 2^{N-\frac{M}{2}}\frac{\sigma_u}{C_u}LSB \tag{3.15}$$

$$\sigma_{INL,MAX} \approx 2^{N-\frac{M}{2}-1}\frac{\sigma_u}{C_u}LSB \tag{3.16}$$

Here, N is the overall resolution in bits, M is the number of bits of the MSB DAC, C_u is the nominal unit capacitor and σ_u is the standard deviation of C_u from nominal value [33].

Metal-insulator-metal (MIM) capacitors which have small parasitic capacitors have been used to implement the capacitive DAC. In the used technology, a MIM capacitor has 1.73 fF/μm^2 density and a matching of 0.3 %.μm. Based on the calculation and simulation results, a unit capacitor size of 90 fF has been chosen, which satisfies all matching requirements. Besides larger size, a careful layout and routing has been done to avoid nonlinearity degradation. Figure 3.8 shows the floor plan and layout of the capacitor DAC. It is divided into the main and low side capacitive DACs. Each side has 32 unit capacitors, and is surrounded by dummy unit capacitors. The bridge capacitor is located in the middle, and connects the two sides together.

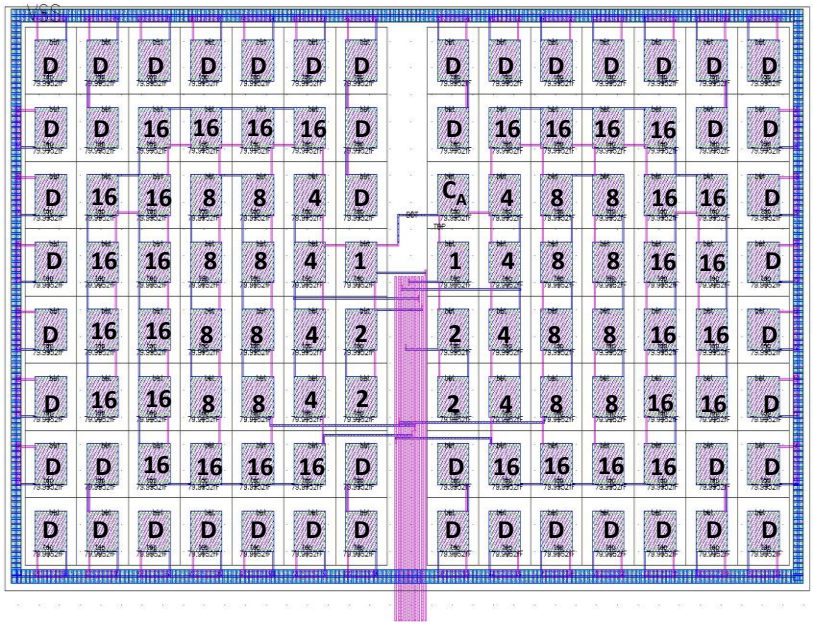


Fig. 3.8 Capacitive DAC array floorplan and layout.

Figure 3.9 shows the schematic of the bootstrap switch, which has been used to sample input signal. It provides a linear on resistance over the full range of the input signal.

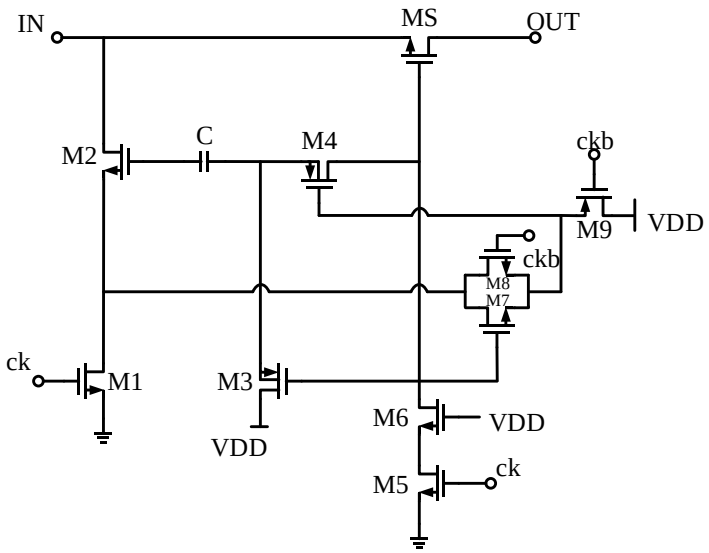


Fig. 3.9 Bootstrap switch schematic.

3.3.1.b DAC and offset error canceling network

Figure 3.10 shows a capacitive array which has been implemented to cancel out the DAC charge error and the comparator's offset difference when switching the reference voltage between GND and V_{ref}. This array is adjustable with 5-bit (T_0 – T_4) external control bits. The resolution of this capacitive array should be small enough to cancel the DAC error due to the parasitic capacitor at the top plate of the main-DAC and also the comparator's offset difference. A minimum capacitor size of 2.86 fF (C_c) which is $1/2^L$ times of C_u has been used in this array, based on the calculation and simulation results. Poly-insulator-poly (PIP) capacitor which has a smaller minimum size has been used to implement this capacitor array. PIP capacitor has larger parasitic capacitance than a MIM one, but the parasitic capacitance and matching are unimportant in the error canceling network.

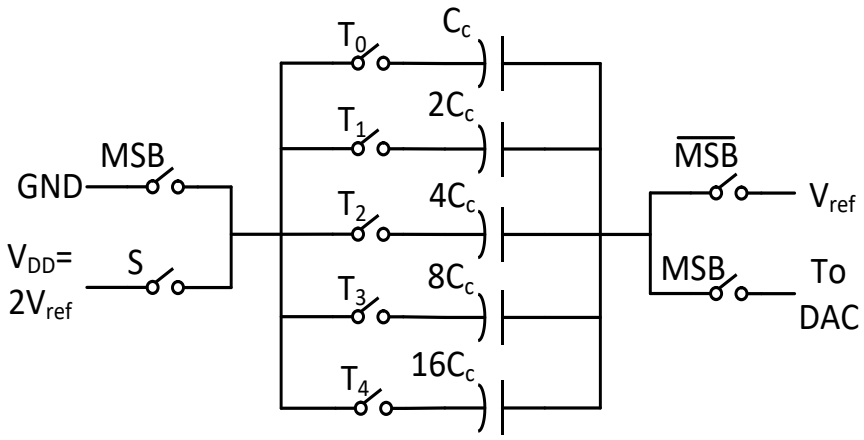


Fig. 3.10 DAC error and comparator offset/error canceling capacitor network.

During the sampling phase these capacitors are connected between $V_{DD}=2V_{ref}$ and V_{ref}, since all output bits are reset during sampling phase and MSB = 0. Then during the conversion phase, if MSB = 1 the capacitor array will be connected to the DAC

output node (the comparator's non-inverting input). The best setting for T_0-T_4 is obtained by applying different DC inputs around the switching point (Vref) and finding the output code. Therefore it is calibrated to cancel out the DAC error and comparator offset error between the two cases of $0 < V_{in} < V_{ref}$ and $V_{ref} < V_{in} < 2V_{ref}$. The power needed by this array is very small, since the capacitor size is very small and it only discharges half of the time when the input is larger than V_{ref}.

3.3.2 Comparator circuit design

Figure 3.11 shows the circuit schematic of the proposed comparator, which is designed in the subthreshold region. It uses a preamplifier (preamp) and a dynamic regeneration latch [34, 35]. The operation of the comparator is divided into a preamp reset phase, amplification and latch enable phase as shown in Fig. 3.11. The control clock phases were generated by a SAR control logic, and they have a controlled duty cycle depending on the comparator's input. Thus, the total time for the 11-bit conversion (100 µsec) is automatically distributed for each bit: for large difference at comparator's input, shorter amplification time is allocated, and for smaller difference, a larger amplification time is allocated. During the preamp reset, the output nodes of the preamp are shorted together to avoid memory effect of the pervious comparison. Then the preamp starts to amplify the voltage difference between the inputs, while the regeneration latch is disabled, and its output is set to V_{dd} by M_{21} and M_{22}. After amplification, the regeneration latch will be enabled to make its decision, and it provides a full-scale output digital signal, which will be stored in the SR-latch. The preamp uses folded-cascode circuitry, with g_m load to avoid the common-mode feedback circuit requirement. To get enough gain, positive feedback has been used in the load branch. The bias current of the input differential pair is 10 times of that of the load branch, which causes the input transconductance g_m to be 10 times larger than the g_m of the load branch, since $g_m = I_d / n.V_T$ in the subthreshold region.

The DC voltage gain of the preamp is

$$Av = -\frac{g_{m_{IN}}}{g_{m_{NEG}} - g_{m_{POS}}} \tag{3.17}$$

Here, g_{mIN} is the transconductance of the input differential pair (M_1, M_2), g_{mNEG} is of M_{NEG}'s (M_{11}, M_{12}), and g_{mPOS} is of M_{POS} (M_9, M_{10}). We have $(W/L)_{POS}=(7/8)(W/L)_{NEG}$ and $g_{mPOS} = (7/8)g_{mNEG} = (1/10)g_{mIN}$. The total DC gain is around 45 dB. In order to achieve high output impedance, the tail current and load branch devices use cascades of low-threshold (LVT) and standard-threshold (SVT) devices. This insures that both devices are in saturation. Based on the current equation (9) in subthreshold [36] we need 100 mV across the devices to be sure that they are in saturation

$$I_D = \mu C_{ox} \frac{W}{L} V_T^2 e^{\frac{Vgs-Vth}{nV_T}} \left(1 - e^{-\frac{Vds}{V_T}}\right) \tag{3.18}$$

Here, V_T is the thermal voltage and n is the subthreshold slope factor (~1.5). Since the reference voltage of the comparator switches between GND and V_{ref}, in order to make sure all transistors are operating in saturation in all process corners, the bulk of input pair is switched between V_{dd} and the source of input pair, based on MSB values. When MSB = 0 and comparison is with V_{ref}, the bulks of the input pair (M_1, M_2) connect to their source and when MSB = 1 and comparison is with GND, the input pair's bulk connect to V_{dd}.

This switching minimizes the voltage variation at the source of the input pair by controlling the bulk voltage and therefore the threshold voltage of the input devices. Larger threshold voltage occurs when reference voltage is GND, and smaller when the reference voltage is V_{ref}. This switching may introduce some offset, which can be cancelled by the charge error and offset cancelling capacitor network. The total input referred offset of the comparator is

$$Vos_{in-tot} = Vos_{preAmp} + \frac{1}{Gain_{preAmp}} Vos_{latch} \tag{3.20}$$

Since the preamp has a large gain, we can ignore the offset caused by the latch, also the input referred offset of the load branch of the preamplifier ($M_{7\text{-}12}$) would be negligible, since the input pair's bias current and therefore its g_m is 10 times larger than load branch's g_m ($g_m = \frac{I_D}{n.V_T}$). However the bias current of the $M_{5,6}$ is in the similar range of the input pair's bias current. Therefore, we can consider only the preamp's input pair $M_{1,2}$ and $M_{5,6}$ as the main source of the offset voltage. Based on the I_D equation in subthreshold region (9), and following the procedure described in [37], the input offset voltage for $M_{1,2}$ can be estimated from (similar approach can be applied for $M_{5,6}$)

$$\begin{cases} Vos_{in} = V_{GS1} - V_{GS2} \\ V_{GS} = V_{th} + nV_T \ln\left[\dfrac{I_D}{\mu C_{ox} \dfrac{W}{L} V_T^2} \right] \end{cases} \tag{3.21}$$

By considering the mismatches in the threshold voltage V_{th}, physical size W/L and load R_{load}, this represent the dynamic effect of the load branch $M_{5\text{-}12}$, after some algebra we can get

$$Vos_{in} = \Delta V_{th1,2} + nV_T \left[\frac{\Delta\left(\frac{W}{L}\right)_{1,2}}{\left(\frac{W}{L}\right)_{1,2}} + \frac{\Delta R_{load}}{R_{load}} \right] \tag{3.22}$$

The first term is static offset. It will be different in the two reference voltage modes, when the comparator's input is switched to GND or V_{ref} based on the MSB value. This offset difference would be canceled by the charge error and offset canceling network (background calibration). The second term is slightly input

dependent because of the changes it can cause in the load impedance (R_{load} is the total impedance at the output node of the preamp, $R_{load} = \frac{1}{g_{m11,12} - g_{m9,10}} \| g_{m7,8} r_{ds7,8} r_{ds5,6}$ and ΔR_{load} represents its variation). But this effect is small compared to conventional comparators which operate in strong inversion [15, 38] with the input offset of

$$Vos_{in} = \Delta V_{th1,2} + \frac{(V_{GS} - V_{th})_{1,2}}{2} \left[\frac{\Delta \left(\frac{W}{L} \right)_{1,2}}{\left(\frac{W}{L} \right)_{1,2}} + \frac{\Delta R_{load}}{R_{load}} \right] \tag{3.23}$$

Here, instead of nV_T as in (12) we have $½(V_{GS}-V_{th})$ and $½(V_{GS}-V_{th}) >> nV_T$. Also, the effect of $\Delta R_{load}/R_{load}$ in (12) is smaller, since the total R_{load} is smaller (only $1/g_m$) and distributed to four devices. Therefore the comparator offset is mostly static and it would not affect the performance of the ADC.

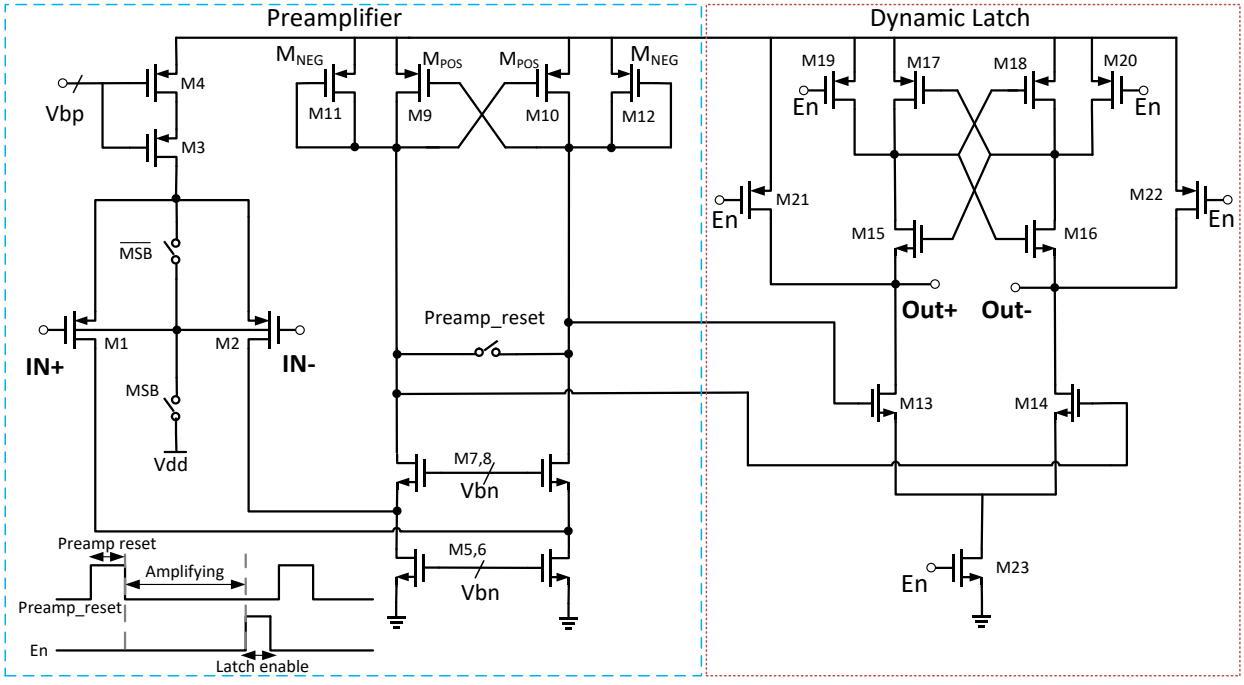


Fig. 3.11 Circuit schematic of the comparator with preamplifier and dynamic latch.

The input referred noise of comparator is mostly coming from the preamp [34]. The input differential pair (M_1, M_2) and current devices in the load branches (M_5, M_6 and $M_{9...12}$) are the dominant noise sources. For operation in the subthreshold region the power spectral density PSD of devices noise is [36]

$$PSD_{\overline{i_{nd}^2}} = 2kTng_m + \frac{K_f g_m^2}{fWLc_{ox}} \tag{3.24}$$

Here, the second term represents flicker noise. The input pair was designed large enough ($\left(\frac{W}{L}\right)_{1,2} = \frac{8\mu}{0.4\mu} \times 4$) to reduce the flicker noise and make it negligible [35]. The power spectral density of the input referred noise is given by

$$PSD_{\overline{Vn_{in}^2}} = 2kTn\frac{1}{g_{m_{IN}}}\left[1 + \frac{g_{m_N}}{g_{m_{IN}}} + \frac{g_{m_P}}{g_{m_{IN}}}\right] \tag{3.25}$$

Here g_{mN} and g_{mP} are for the top PMOS (M_9...M_{12}) and bottom NMOS (M_5, M_6) devices in the load branches of preamp, respectively. The input pair's transconductance g_{mIN} is 10 times larger than the load branch g_m, to reduce the input-referred noise. Also, the transfer function of preamp is second order, and its second pole is designed to be close enough to the first pole to make the transfer function sharper, which helps to reduce the total integrated in-band noise. Total in-band input-referred noise is obtained by integrating this PSD over the preamp's bandwidth. Simulated total in-band input-referred noise is around 63 µV which is small enough compared to the LSB = 366 µV.

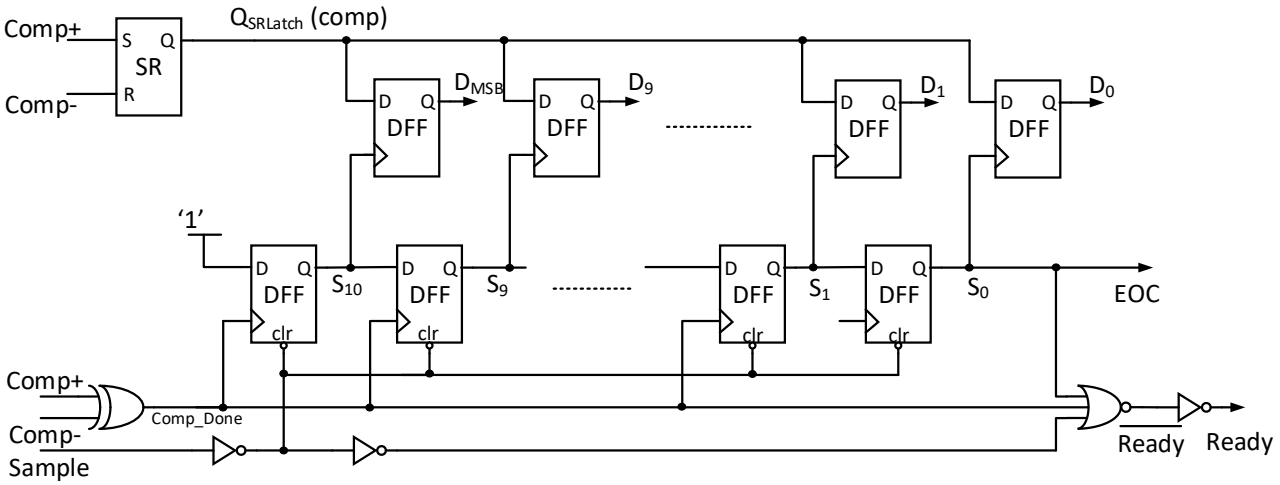
The input common-voltage (CM) to the comparator can vary with different input signals [34]. The CM variation range for MSB generation is $V_{ref}/2$-to-$3V_{ref}/2$. To generate rest of the bits and eventually the LSB, depending on the input signal range, the CM voltage will converge to V_{ref} or GND. This variation can cause the dynamic offset in the single-ended structure. To overcome this issue a high output impedance current source ($M_{3,4}$) was used in the preamplifier circuit, which determines the

current flowing through the $M_{1,\ 2}$ and therefore reduces the overdrive voltage variation and indeed the dynamic offset.

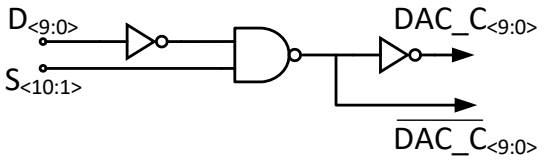
3.3.3 Asynchronous SAR control logic circuit

Asynchronous control logic is used in this ADC. The circuit schematic and timing diagram of the asynchronous controller are illustrated in Fig. 3.12. Low power supply voltage and the use of high threshold devices in the logic circuit reduced the power consumption and the leakage currents. The input signals to this circuit are Sample (external signal with 10% duty cycle), V_{comp} (comparator decision at SR-latch) and Comp_Done (XOR of comparator's positive and negative output). The output signals are DAC control bits, preamp_reset, En and EOC (end of conversion). During the sampling phase, the DFFs are reset and their outputs (S_0 to S_{10}) will be '0', therefore all of controlling signals for DAC (DAC_C) will be '0' and the bottom plates of all capacitors in DAC will be connected to the input. When the sample signal changes from '1' to '0', all capacitors will be switched to V_{ref} from the input signal, and conversion starts. When the first comparison is done, MSB is ready and stored at SR latch, and Comp_Done goes to '1'. This will trigger DFF and S_{10} goes to '1', and it generates trigger clock for the bit FFs. At the rising edge of this clock, the bit DFFs will sample the comparator's output witch was stored in the SR latch. Meanwhile, $\overline{\text{Ready}}$ goes to '0' and resets the En signal in comparator. This will set the comparator's output to '1' and Comp_Done goes to '0' again.

If DAC_C = 1, the bottom plate of the affected capacitor will be connected to GND, and if DAC_C = 0 the bottom plate of the relevant capacitor will be stay connected to V_{ref}. This procedure will continue until the detection of the last bit. Then the EOC signal will go from '0' to '1', and it will reset the capacitors to prepare for the next sampling and conversion. The preamp_reset and En signals will be generated as shown in Fig. 3.12. The Preamp_reset duty cycle is tunable by I_{td1}, and the amplifying time is adjustable by I_{td2}.



a)



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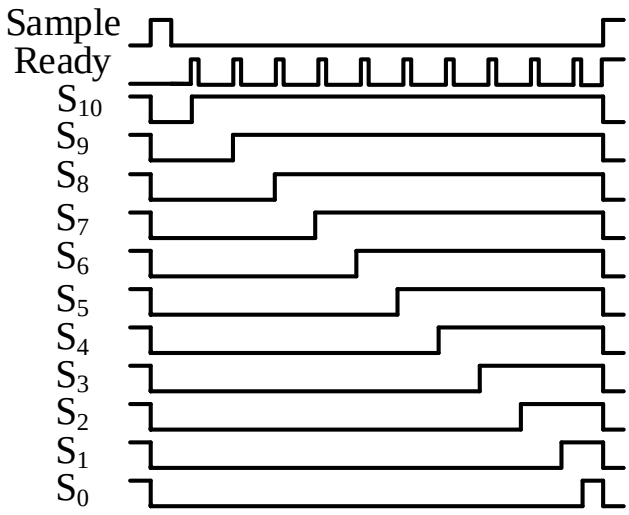


c)

Fig. 3.12 a) Block diagram of the asynchronous SAR control logic and timing diagram b) DAC switches control signal c) Control signals waveform.

When $\overline{\text{Ready}}$ goes low, preamp_reset goes high and after a t_{d1} delay it goes low, and amplification starts. The t_{d2} time is amplifying time, and at the end of this time En signal goes high and enables the latch. When the comparator's output becomes ready, it will be detected by xor of positive and negative output of comparator, and comp_Done goes high.

3.4 Measurements Results

The prototype ADC was fabricated in 0.18 µm CMOS 2P4M process and tested. Figure 3.13 shows a full micrograph and zoomed-in view of the core ADC. The total chip size is 1.9×1.9 mm^2, while the core size is 270×475 μm^2. The sampling frequency is 10 kS/s, and the power supply voltage is 0.75 V. The sampling trigger is a pulse waveform with a 10% duty cycle. It was generated by an arbitrary waveform generator. This trigger pulse controls the sampling switch, and rest of the control clocks are generated internally by the asynchronous control logic inside the chip. The test set-up is shown at Fig. 3.14.

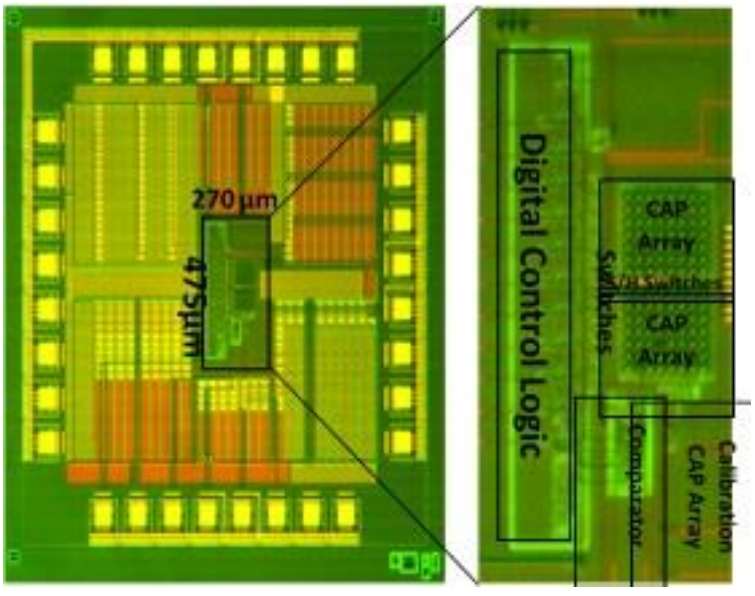


Fig. 3.13 Die micrograph and the zoomed-in core.

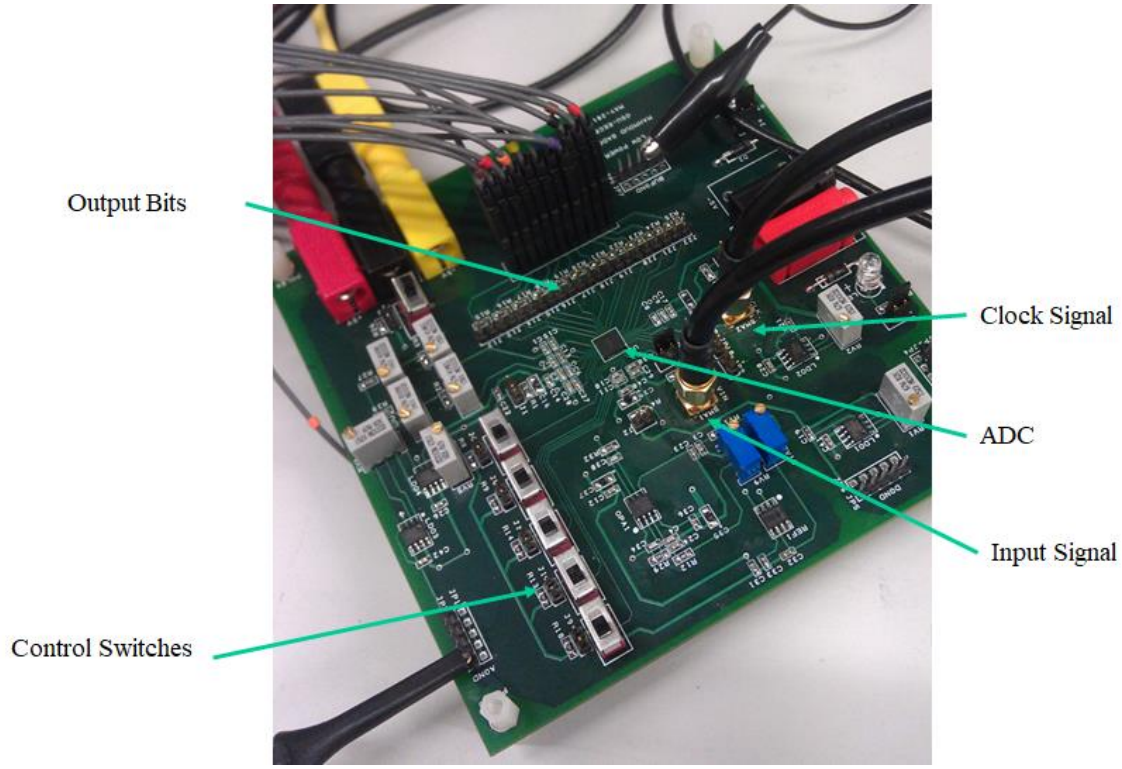


Fig. 3.14 Test Set-up of the ADC.

Figure 3.15 shows the output of the ADC for a sine-wave input signal with and without error/offset cancelling capacitor network. When the input signal is getting larger than V_{ref}, the reference voltage for the comparator switches from GND to V_{ref}. As explained earlier, because of the parasitic capacitor at the comparator's input node, this reference switching creates error in the final code. The reference switching creates a comparator offset change as well. This error and offset change cause nonlinearity at the output when the input signal varies around V_{ref}. This nonlinearity is visible in Fig. 3.15.a, where the error/offset canceling network is turned off. Figure 3.15.b shows the output of the ADC for same input signal with the error/offset canceling network turned on and calibrated to cancel the voltage error. The curve around the V_{ref} (middle of amplitude) point is zoomed in to show the effectiveness of the error/offset canceling network.

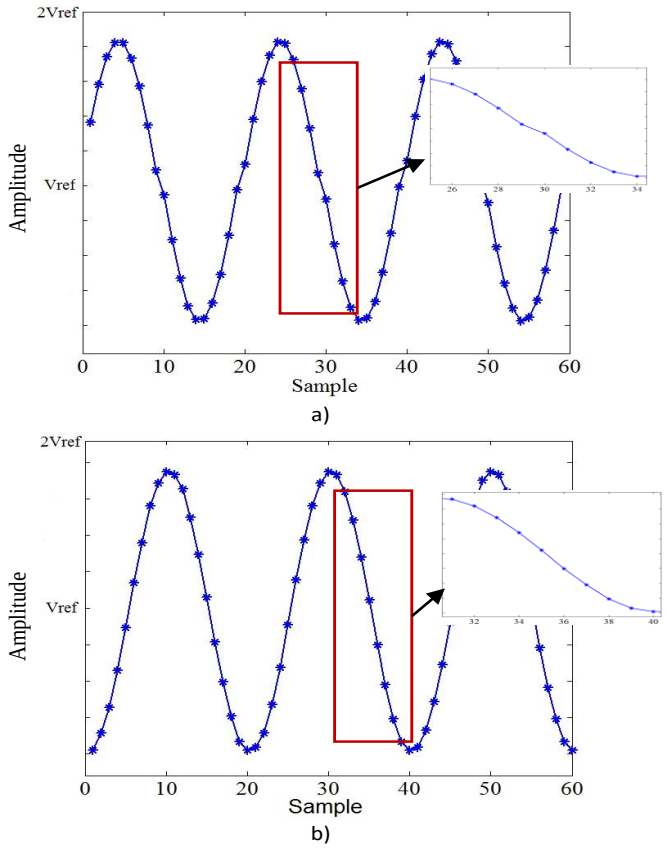
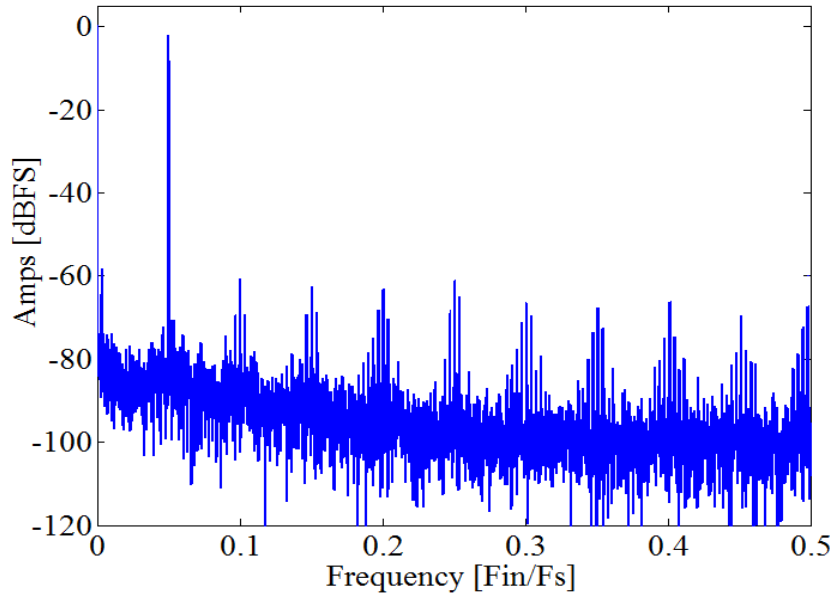
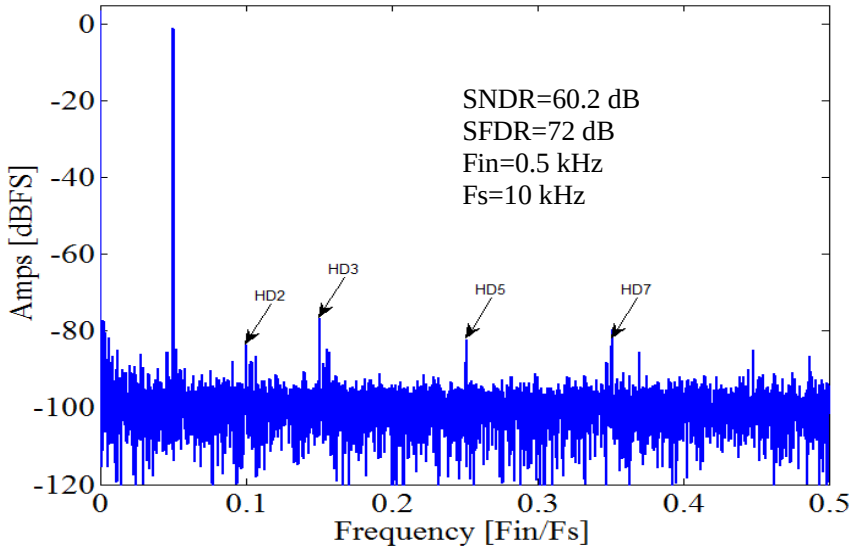


Fig. 3.15 Measured ADC output for 0.5 kHz sinewave input a) without (EOC) error/offset canceling b) with error/offset canceling.

Figure 3.16 shows the ADC output spectrum without and with the error/offset canceling network for a 0.5 kHz input signal. As expected, without error cancellation there are large harmonics (Fig. 16. a,) due to the nonlinearity around the mid-range signal level. Figure 3.17 shows the ADC output spectrum with the input frequency at 3.8 kHz. The possible source of the higher third order harmonic distortion is from the input signal source and the filter that have been used for the measurement. Another possibility is not enough resolution in the parasitic voltage error canceling network.



a)



b)

Fig. 3.16 Measured ADC output spectrum for 0.5 kHz sinewave input a) With error/offset canceling network off b) With error/offset canceling network on.

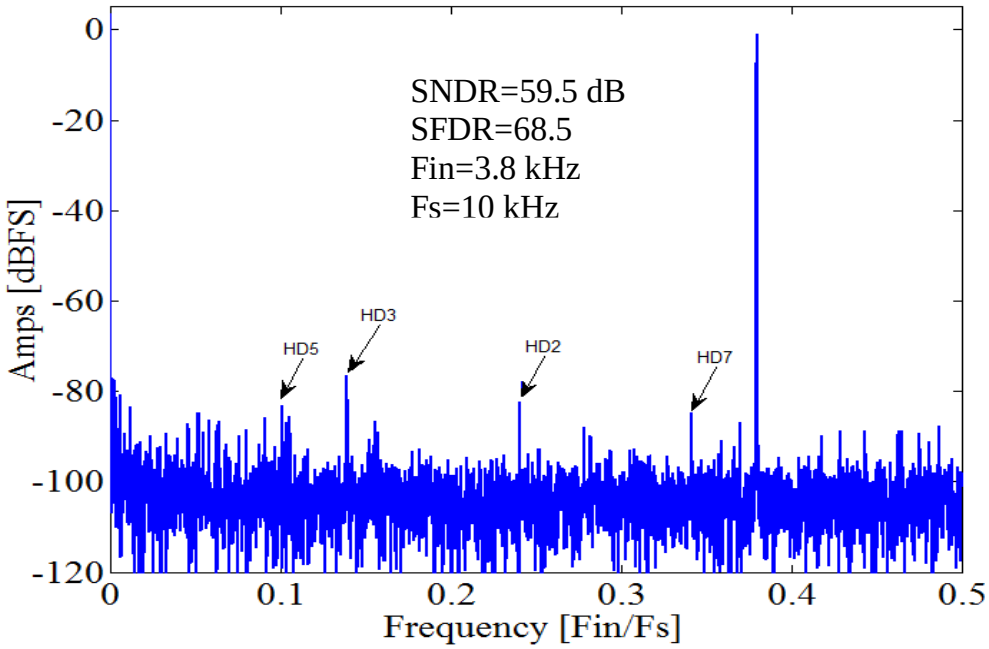


Fig. 3.17 Measured ADC output spectrum for 3.8 kHz sinewave input with error/offset canceling network on.

Figure 3.18 shows the dynamic performance (SNDR/SFDR) of the ADC with the input frequency swept from DC to Nyquist at a 10 kS/s sampling rate. The effective number of bits (ENOB) versus the input frequency is shown in Fig. 3.19. There is no significant drop in the ENOB at higher input frequencies, because of the lower operation frequency and (more importantly) the asynchronous control signal which controls the comparator's pre-amplification and latching time based on the input signal. The ADC can achieve 9.76 ENOB at 0.9 kHz and 9.6 ENOB at 4.8 kHz.

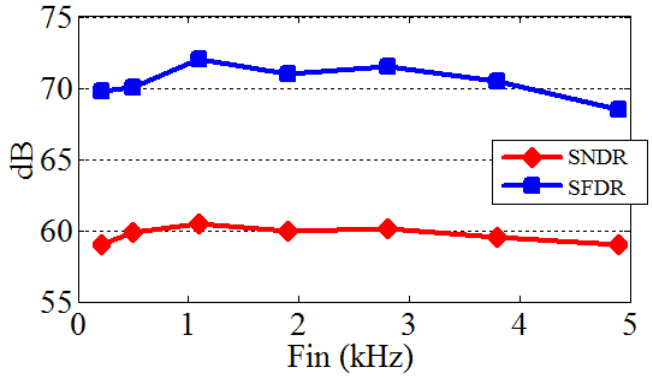


Fig. 3.18 Measured ADC dynamic performance (SNDR/SFDR) versus input frequency.

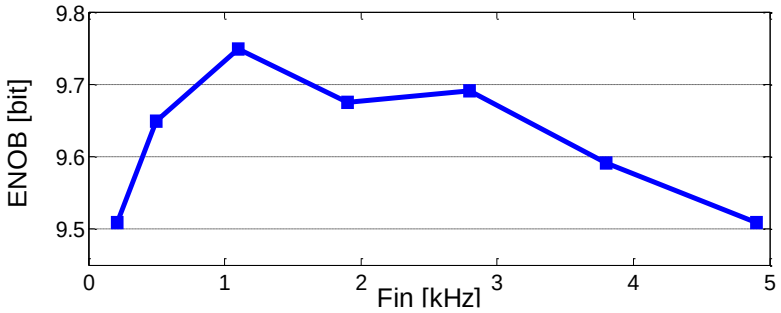


Fig. 3.19 Measured ENOB of the ADC versus input frequency.

The DNL and INL are illustrated in Fig. 3.20. The peak DNL and INL are +0.6/-0.37 and +0.94/-0.89, respectively at a 10 kS/s sampling rate. The power consumption is 250 nW from a 0.75 V supply voltage. The analog power is the main part of the power consumption. It includes the comparator, the capacitive DAC array and the sampling switches. The digital power, including control logic and output buffers, is a small portion of the total power consumption. It is because of the high threshold devices that had been used in digital blocks to reduce the leakage current, and also the lower leakage current of the process compared to more modern technologies.

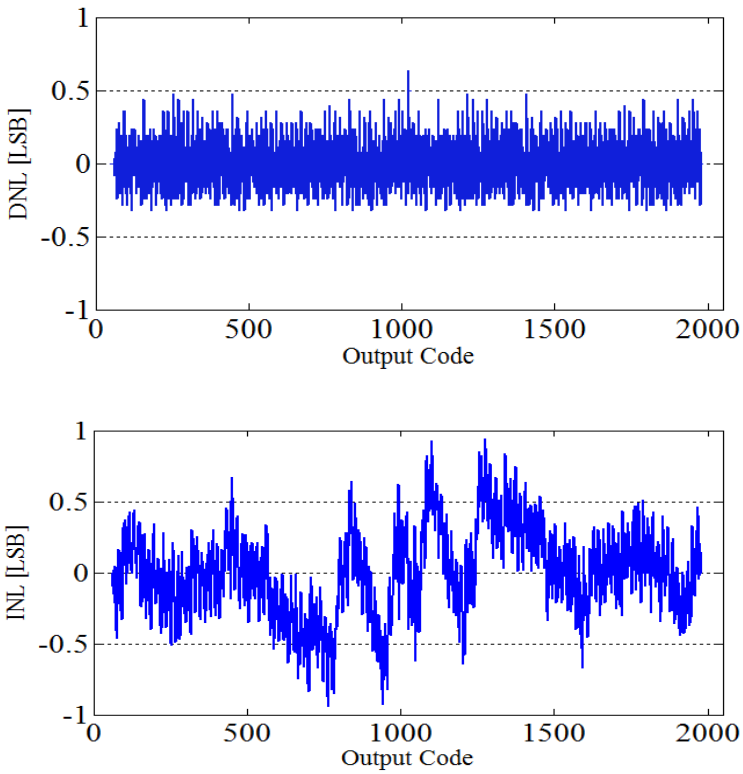


Fig. 3.20 Measured DNL and INL.

The measurement performance of the prototype ADC is summarized in Table 3.2. The prototype ADC is compared with the most relevant state-of-the-art works in Table 3.3.

The figure-of-merit (FOM) used to compare the ADC performance was

$$FOM = \frac{Power}{\min\{fs, 2\times ERBW\}\times 2^{ENOB}} \tag{3.26}$$

Lower power consumption is important factor for biomedical application as well as FoM. Reference [7] is benefiting from the advanced process, and in [23, 24], which used similar process, they achieved slightly better FoM but their power consumption is much higher. In [25] the performance is reported up to 10 kHz input, which is way lower than Nyquist.

TABLE 3.2 Summary of Performance

Technology	0.18 μm CMOS 2P4M
Area [mm^2]	0.12
Resolution [bit]	11
Sampling Rate [kS/s]	10
Supply Voltage [V]	0.75
Input Range (Single Ended) [V]	2×Vref (2×0.375)
SNDR [dB]	60.5
SFDR [dB]	72
ENOB [bit]	9.76
DNL [LSB]	+0.6/-0.37
INL [LSB]	+0.94/-0.89
Total Power Dissipation [nW]	250
FoM [fJ/Conv.]	28.8

TABLE 3.3 COMPARISON TO STATE-OF-ART WORKS

	This Work [42]	**JSSC'13 [7]**	**TBCS'14 [8]**	**JSSC'12 [9]**	**TCASI'15 [10]**	**ISSCC'10 [11]**	**ESSCIRC'14 [23]**	**ASSCC'15 [24]**	**TCASI'16 [25]**	**TCASII'16 [41]**
Architecture	Single-ended	Diff	Single-ended	Diff	Single-ended	Single-ended	Diff	Single-ended	Diff	Diff
Technology [nm]	180	65	180	130	130	350	180	180	180	65
Supply Voltage [V]	0.75	0.6	0.9	1/0.4	1.0	1.0	1.0	0.6	0.8	1.0
Resolution [bit]	11	10	9	10	10	10	11	10	10	14
Sampling Rate [kS/s]	10	20	100	1.0	1000	10	1000	100	200	10
SNDR [dB]	60.5	55	50.1	56.7	54	-	63.4	58.83	57.86	77
SFDR [dB]	72	69	65.1	67.6	-	-	76.6	63.6	72.27	88.8
ENOB [bit]	9.76	8.84	8.02	9.1	8.8	9.06	10.3	9.48	9.3	12.5
DNL [LSB]	+0.6/-0.37	0.58	0.85	+0.54/-0.61	-0.33/+0.56	0.89	+0.53/-0.85	+0.85/-0.47	+0.29/-0.26	-0.9/+2.2
INL [LSB]	+0.94/-0.89	0.57	1.52	+0.45/-0.46	-0.61/+0.55	0.73	+0.68/-0.91	+1.52/-1.26	+0.36/-0.8	-2.2/+2.2
Power [nW]	250	206	1330	53 / 72	9000	22000	24000	1720	2010	1980
FOM [fJ/Conv-Step]	28.8	22.4	51.3	94.5	27	45	19.9	24.1	15.5(10kHz)	34.2
Core Area [μm×μm]	270×475	470×750	478×316	357×536	235×240	-	-	360×380	0.154mm^2	0.28mm^2

3.5 Summary

A single-ended 250 nW SAR ADC with a 0 - $2V_{ref}$ input range using a charge error/offset canceling network is presented. It has a small total capacitance and a reduced loading effect on the previous stage. It is suitable for biomedical applications. A comparator operating in the subthreshold region with low dynamic offset was used, along with a self-controlled SAR logic at a 0.75 V supply voltage. The measurement results verify the power, area and loading efficiency of the ADC.

CHAPTER 4. A NOISE-COUPLED VCO-BASED QUANTIZER AND ΔΣ ADC BASED ON NOISE-COUPLED VCO-BASED QUANTIZER

Abstract

In chapter two, we have discussed the VCO-based quantizer and its different implementation for delta-sigma ADCs. We have described previous works with VCO-based quantizer in both continuous and discrete time applications. In this chapter, we begin by describing the proposed noise-coupled VCO-based quantizer, its implementation and benefits. Then we will present 2-2 MASH delta-sigma ADC architectures in discrete time by employing the proposed noise-coupled VCO-based quantizer. Furthermore OPAMP sharing technique reduces power dissipation. The first stage of the 2-2 MASH is implemented as second order delta-sigma ADC with feedforward technique, which reduces the output swing requirement of the first OPAMP and therefore improves the power efficiency. The second stage is the proposed noise-coupled VCO-based delta-sigma ADC. The OPAMP of the second integrator at first stage and the adder in the second stage are shared to reduce the power dissipation. Therefore 4^{th} order noise-shaping has been achieved with employing only two OPAMP. The implementation details and non-idealities effect are also covered in this chapter. The ADC is designed and implemented at 0.18 um CMOS process technology. It achieves 80.54 dB peak SNDR over 8 MHz signal bandwidth at 160 MHz sampling frequency rate. The results and discussions are provided at the end of this chapter.

4.1 Introduction

With increasing speed in wireless communication and portable electronics, there comes demands in high performance and low power analog and RF building blocks to extend battery life and operation time. Analog-to-digital converter (ADC) is a key building block in these applications. High resolution with higher bandwidth and lower power dissipation is necessary for those ADCs. For medium to high resolution, oversampled delta-sigma ADCs are suitable structures because of the relaxed matching requirements on analog components, and noise shaping capability [1, 12].

Figure 4.1 shows the general block diagram of delta-sigma ADC [1]. Key building blocks are loop filter (integrator), internal quantizer and feedback DAC. The achievable signal to quantization noise is:

$$SQNR \approx \underbrace{(6.02 * B + 1.76)}_{\text{Quantizer: B-bit}} + \underbrace{10\log(OSR)}_{\text{Oversampling}} + \underbrace{N * 20\log\left(\frac{OSR}{\pi}\right)}_{\text{Noise-shaping: N}^{th}\text{-order}} \tag{4.1}$$

There are three ways to improve the SQNR based on Eq (4.1): increase the quantizer resolution, increase the OSR or increase the loop filter order. However there are trade-offs in increasing each of these parameters. Increasing the quantizer resolution demands more power dissipation in quantizer and adds complexity in the DWA or DEM in the feedback DAC. The OSR is limited by available process bandwidth and requires higher OSR to increase the power dissipation of the OPAMP. The last option is to use higher order loop filter, but in a single-loop structure it can cause stability issue and each extra order of loop filter demands an additional active block which leads to more power consumption.

One option to achieve higher loop-order without having stability issue, is Multi-stAge noise-SHaping MASH modulator. Figure 4.2 depicts the block diagram for two-stage MASH modulator [1]. The first stage quantization error extracted and processed by the second stage. The overall order of noise-shaping is multiplication of each stage's order and we have:

$$\begin{aligned} v &= v_1.H_1 + v_2.H_2 \\ &= \left(STF_1.u + NTF_1.e_1\right).H_1 + \left(STF_2.e_1 + NTF_2.e_2\right).H_2 \\ &= STF_1.STF_2.u + NTF_1.NTF_2.e_2 \quad for\ H_1 = STF_2 \,\&\, H_2 = NTF_1 \end{aligned} \tag{4.2}$$

The MASH architecture overcomes the stability issue for higher order noise-shaping modulator, but the perfect matching between analog and digital transfer function in MASH delta-sigma modulator is required to cancel the quantization error of the preceding stage, otherwise the quantization error leakage will degrade the overall performance.

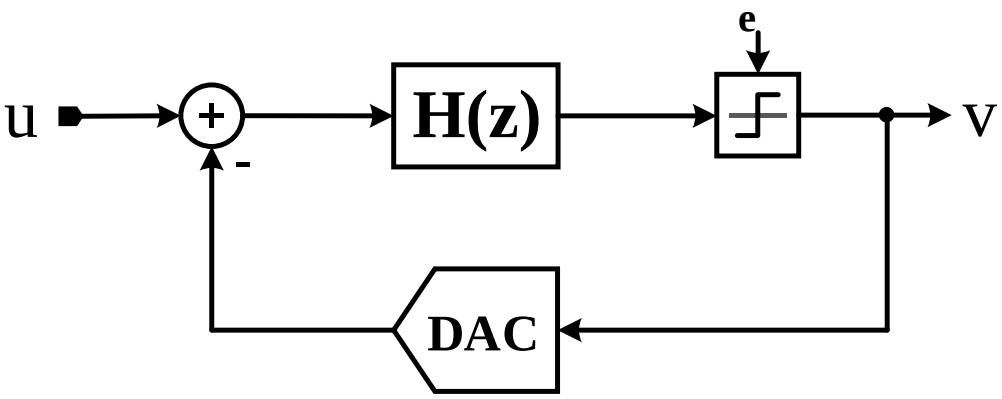


Fig. 4.1 Block diagram of delta-sigma ADC.

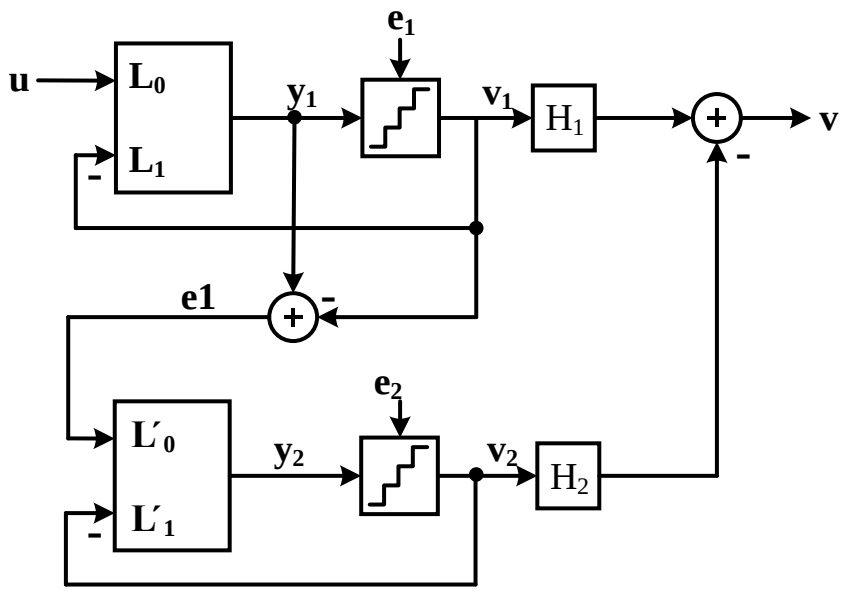


Fig. 4.2 Block diagram of two-stage MASH delta-sigma ADC.

In the MASH structure, each additional stage leads to an additional quantizer and active elements (OPAMP) and therefore increases the power dissipation. Previous research has introduced several techniques to save the power dissipation in MASH, such as OPAMP sharing [45], multirate VCO-based modulator [46], multirate OPAMP sharing [47, 48] and dual-slope quantizer [49]. Most of these works used OPAMP-sharing technique to reduce the required active elements by one, and they also have the additional power dissipation by the quantizer of the further stage.

In this chapter, first a VCO-based modulator with noise-coupling technique is presented [50]. The noise-coupling technique enhances the noise-shaping of the VCO-based modulator and provides a second-order noise-shaping. Also since the VCO-based quantizer has inherent DEM, therefore it doesn't require additional DEM or DWA block. Then the proposed noise-coupled VCO-based quantizer is used as second stage of the 2-2 MASH modulator. To save the power dissipation and reduce the number of active elements, OPAMP sharing technique has been applied between the stages. The OPAMP of the second integrator of first stage is shared with the required adder at second stage. Therefore 4th order modulator has been achieved

with only employing a two OPAMP. The quantizer power of the second stage is reduced by using a VCO-based quantizer as compared to a conventional flash quantizer.

4.2 Noise-Coupled VCO-Based Quantizer

Voltage controlled oscillator VCO based ADCs became popular in oversampling ADCs, due to their highly digital circuit architecture and inherent first-order noise shaping with inherent dynamic element matching DEM [51].

The behavioral model of the VCO-based ADC consists of the integrator block, sampling block and differentiator block, which represents the conversion from voltage to frequency and then the conversion to digital form. For this circuit, the signal transfer function is $STF \approx z^{-1}$ and the noise transfer function is $NTF = (1-z^{-1})$ [51, 52]. Higher signal-to-noise ratio SNR in delta-sigma ADCs can be achieved by higher order of noise-shaping, but this needs more integrators, which increases the power consumption. Closed-loop VCO-based architectures have been presented using an active integrator for each additional noise shaping order [53]. The dynamic range (DR) of VCO-based ADCs is limited by the nonlinearity of the VCO. Previous work tried to improve the DR by using the VCO in second stage, and therefore reducing the input signal to the VCO quantizer. In [46] the VCO quantizer is as a second stage of the multi-stage noise shaping (MASH) structure. This needed a power-hungry first stage and complex digital canceling filter, which should be matched to the analog path of the ADC. In previous research [54], the residue of the first stage is the input to the VCO quantizer, and the first stage is in the loop as well. But the integrator of the loop sees full scale input signal swing and therefore its amplifier needs large power.

A conventional VCO-based quantizer provides first-order noise shaping without using any active integrator. Higher order of noise shaping is achievable by using a loop filter, which means one integrator per order increase. Figure.4.3 shows the

proposed VCO-based quantizer employing the error feedback technique [50]. In this structure, the quantization error of the VCO-based quantizer is extracted, delayed and coupled back to the input of the quantizer. Depending on the delay block, we can achieve second or higher-order noise-shaping. For example, for $D = z^{-1}$, we can get second-order noise-shaping: one from the VCO-quantizer and the other one from noise-coupling. This scheme improves the modulator order without additional active integrator and therefore it saves power. The required adder can be combined with the other adder in the structure, as will be explained in next section. The following equation shows the noise transfer function (NTF) for delay block $D(z) = z^{-1}$:

$$NTF = \left(1 - z^{-1}\right)^2 \quad for \quad D(z) = z^{-1} \tag{4.3}$$

Also for delay block $D(z) = z^{-2} - 2z^{-1}$ we will have:

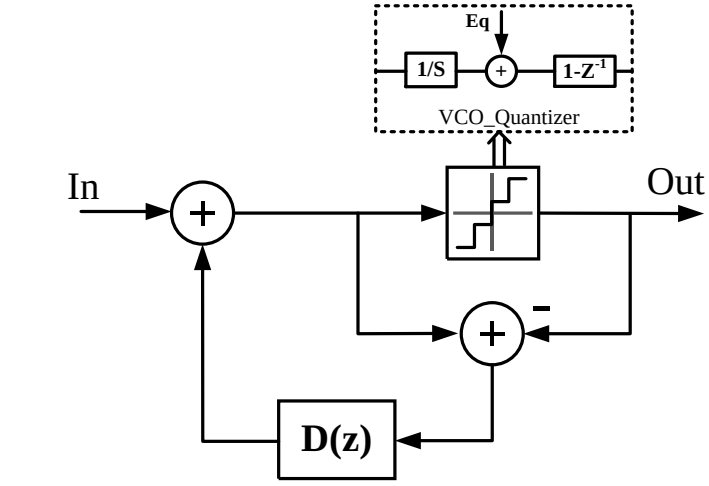
$$NTF = \left(1 - z^{-1}\right)^3 \quad for \quad D(z) = z^{-2} - 2z^{-1} \tag{4.4}$$

This can be generalized for higher orders (L) as follow:

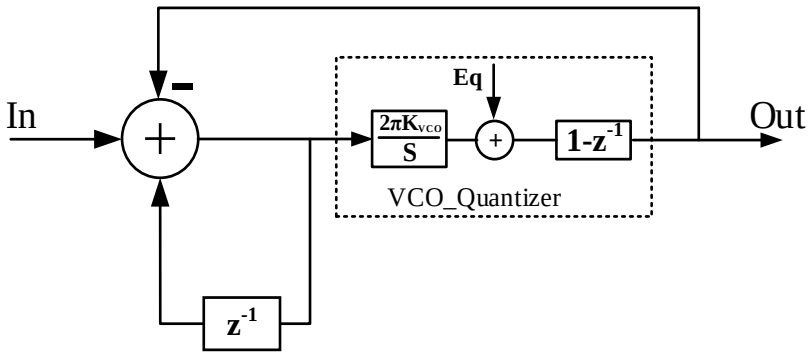
$$NTF = \left(1 - z^{-1}\right)^L \quad for \quad D(z) = \left(1 - z^{-1}\right)^{L-1} - 1 \tag{4.5}$$

Since the signal transfer function (STF) of the VCO quantizer is $STF \approx z^{-1}$, we don't need a delay block in the VCO-quantizer path. The only required delay is from the output of the adder to its input; thus, two adder blocks can be merged, and the final structure can be simplified as shown in Fig 4.3.b. Second- or higher-order noise shaping is achieved without using extra active integrator, so the power consumption will be much less than the conventional ΔΣ ADC. The 15-level (15 stage ring oscillator) conventional VCO-based quantizer and the proposed noise-

coupled VCO-based quantizer has been designed and simulated for comparison. The circuits were implemented in a differential structure, and the linear range of the VCO extracted with simulation. The sampling frequency is Fs = 160 MHz and the VCO designed with Fs/4 free running frequency. As shown in Fig. 4.4 the proposed noise-coupled VCO-based quantizer for D = z^{-1} achieves second order noise shaping in contrast to the first order of the conventional VCO-based quantizer. In this simulation the output is normalized. The actual input signal level is smaller, and it is in the linear range of the VCO's input.



a)



b)

Fig. 4.3 Proposed noise-coupled VCO-based quantizer b) Simplified structure for D=z^{-1}.

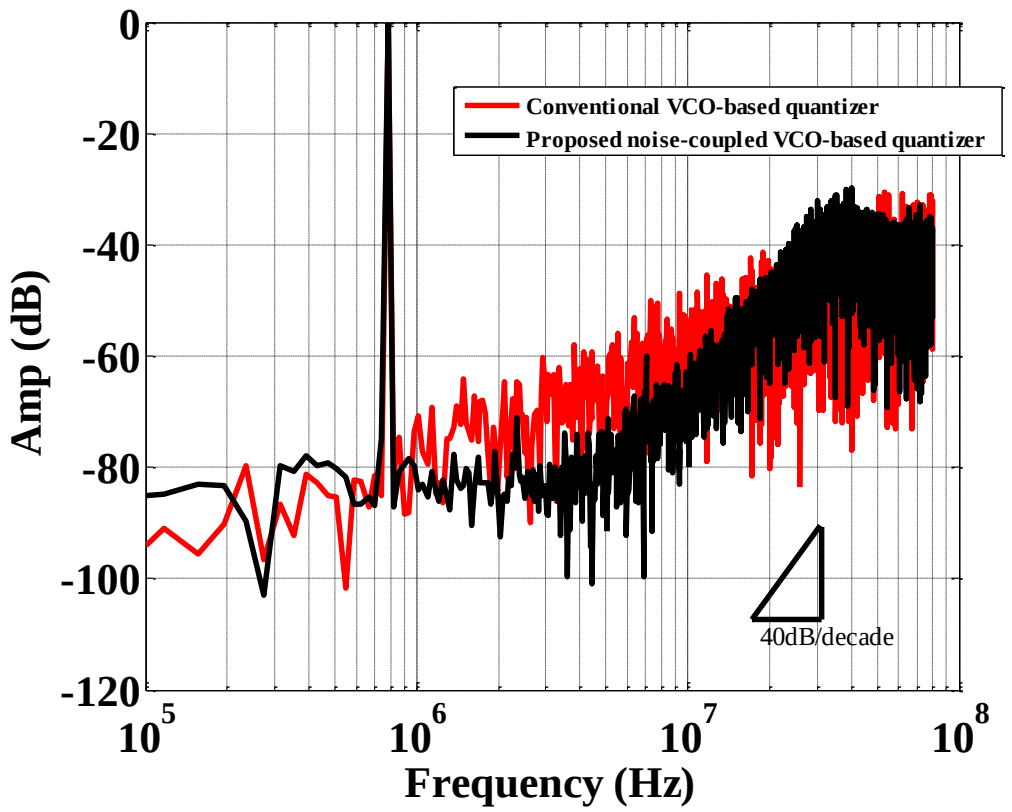


Fig. 4.4 Conventional VCO-based quantizer and the proposed noise-coupled VCO-based quantizer output spectrum comparison.

4.3 Architecture of 2-2 MASH Modulator with Noise-Coupled VCO-Based Quantizer and OPAMP Sharing

4.3.1 Conventional 2-2 MASH ΔΣ ADC structure

MASH modulator can be implemented in discrete-time or continuous-time [55, 56]. However the discrete-time is preferable, since the transfer functions are precisely definable comparing to continuous-time counterpart. This is because the absolute value of the components (resistors and capacitors) defines the coefficients, and thus the large variation of the absolute value of these components cause a huge coefficient variation from designed one. But in the discrete-time the ratio of the

components (capacitors) defines the coefficients value and this can be defined more precisely comparing to absolute values. However this come with cost of power dissipation in OPAMPs of the integrators, since the require unity-gain bandwidth for discrete-time structure is larger than continuous-time counterpart.

Figure 4.5 shows an example of the conventional feed-forward 2-2 MASH modulator. It consists of 4-Integrator, one adder and two quantizer. One option to save the power is to reduce the number of active elements by sharing them. Figure 4.6 shows the prior works where they tried to reduce the number of OPAMPs by applying the OPAMP-sharing technique. One way is to share the OPAMPs in adjacent integrators (horizontally) as marked by green box, another way is to share the OPAMs vertically as marked by red box. This way, a 2-2 MASH modulator implemented with two-OPAMPs as integrator, one adder and two quantizer [45].

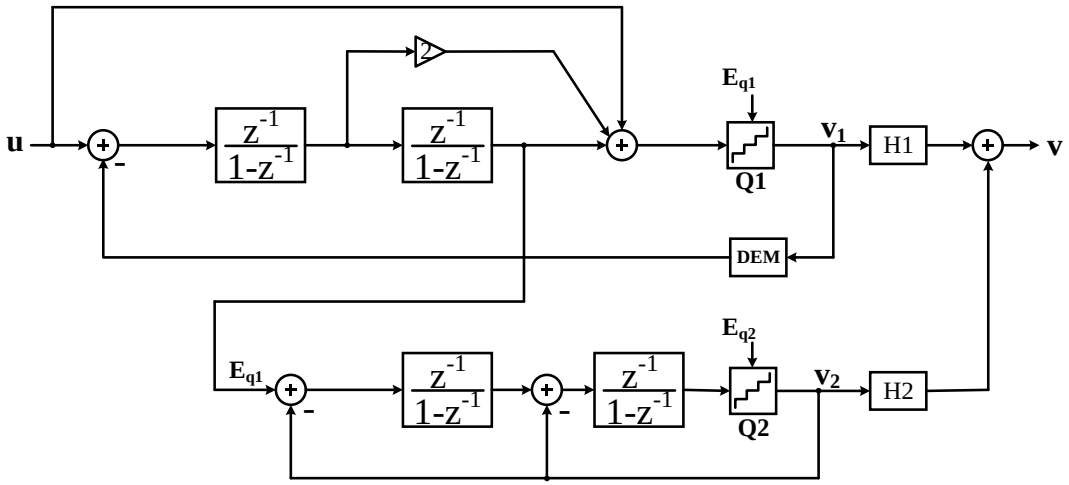


Fig. 4.5 Block diagram of 2-2 MASH ΔΣ ADC.

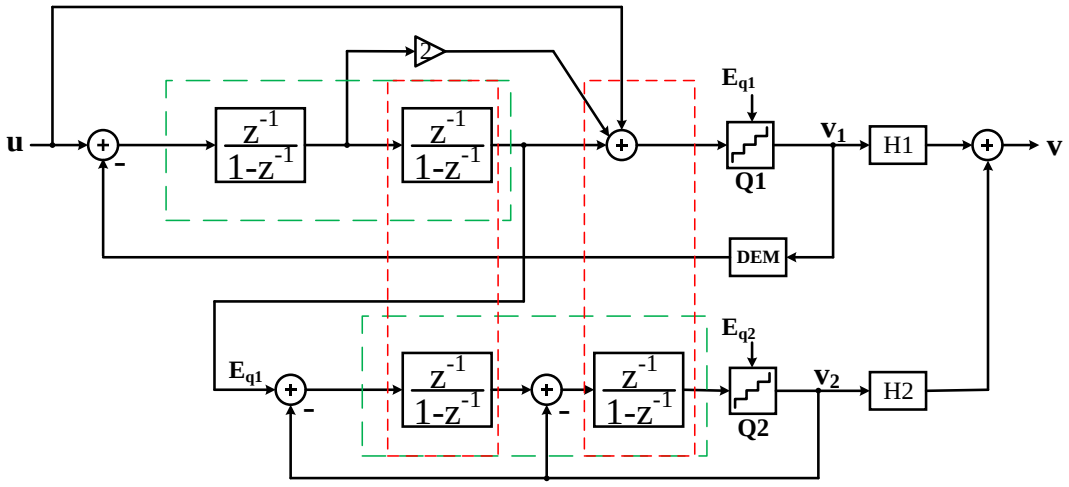


Fig. 4.6 Block diagram of 2-2 MASH ΔΣ ADC with possible OPAMP sharing methods.

4.3.2 MASH ΔΣ ADC with noise-coupled VCO-based quantizer

Figure 4.7 shows the block diagram of the 2-2 MASH delta-sigma ADC by employing the noise-coupled VCO-based quantizer. The first stage is a second order delta-sigma loop with feedforward path from input signal to input of the second integrator [57]. In a delta-sigma modulator the first integrator is most critical/power-consumer block and the required OPAMP specification of that is the highest. Since capacitors of this integrator is largest one, to satisfy thermal noise, therefore its capacitive load is large. The feedforward path reduces the output swing of first integrator and therefore we can achieve the required DC gain with stacking more devices in single stage telescopic OPAMP as will explain later in this section.

The quantization error of first stage extracted and applied to the second stage, which is the noise-coupled VCO-based quantizer. Therefore the input signal swing of second stage and VCO will be just quantization error of first stage which is small and in linear operation range of VCO. Based on the simulation and designed VCO specification, 4-bit quantizer is enough to make sure the input of second stage is in

linear operation range of VCO. Second integrator and adder of second stage shares the OPAMP, but first stage has its own OPAMP. The specification of these two OPAMPs are different. First one has higher DC gain, lower unity-gain bandwidth and smaller output swing. But the second one has lower DC gain, higher unity-gain bandwidth and higher swing. More details about them will be covered later in this section. Gain scaling has been done for second integrator to relax its output swing.

For this purpose as shown in Fig. 4.8 the gain of two, pushed from integrator to the quantizer. This just implemented by scaling down the reference voltage of quantizer by half, which is equivalent to amplifying by two. This makes the quantizer design a little bit difficult but it relaxes the OPAMP and has power efficiency.

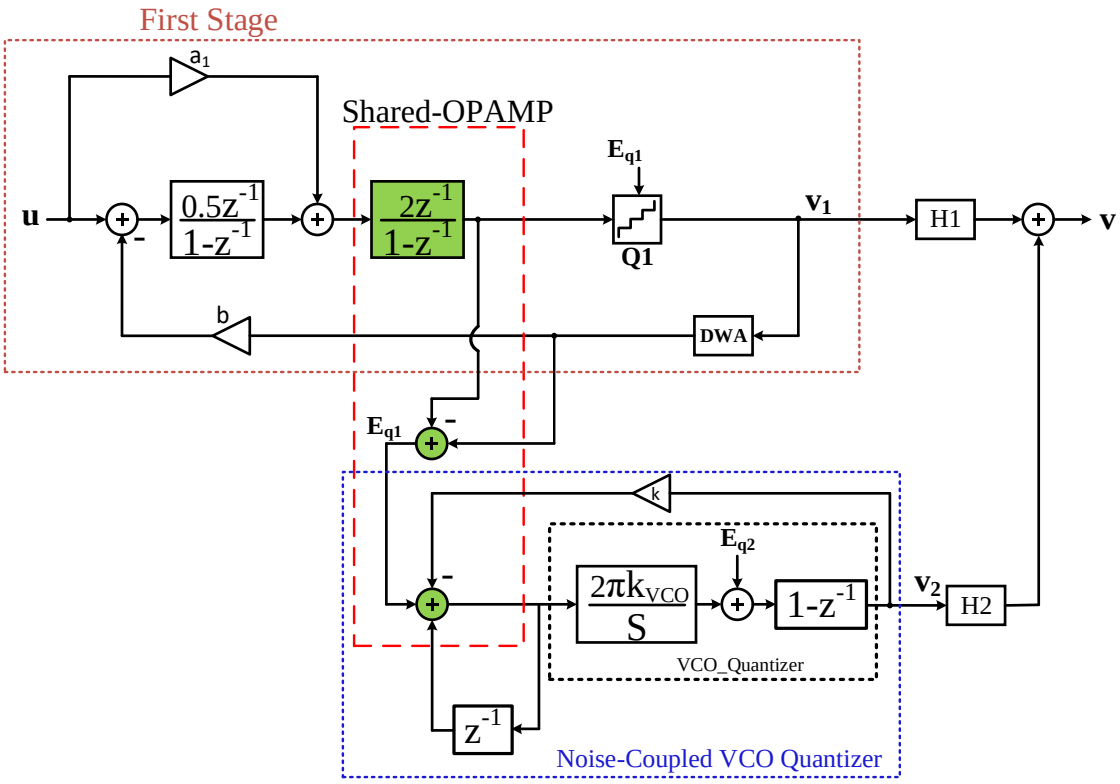


Fig. 4.7 Block diagram of 2-2 MASH ΔΣ ADC with noise-coupled VCO-based quantizer and OPAMP sharing.

The second stage is a 15-level VCO-based quantizer, which is equivalent to 4-bit quantizer. The final output is generated by passing the first and second stage output through the digital filters H_1 and H_2. Where H_1 is the signal-transfer function of second stage, which is z^{-1}, and H_2 is noise-transfer function of first stage, which is $(1-z^{-1})^2$. This architecture achieves 4^{th} order of noise-shaping with employing two OPAMPs, one quantizer, and one VCO-based quantizer, which leads to higher power efficiency.

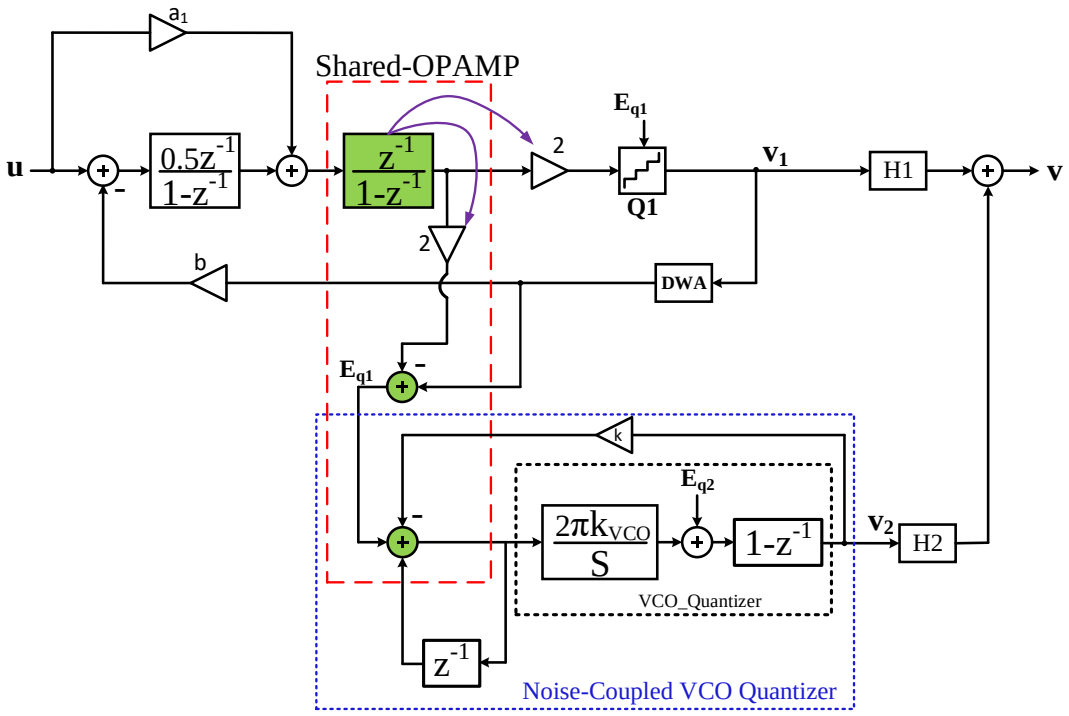


Fig. 4.7 Block diagram of 2-2 MASH ΔΣ ADC with noise-coupled VCO-based quantizer and OPAMP sharing after scaling.

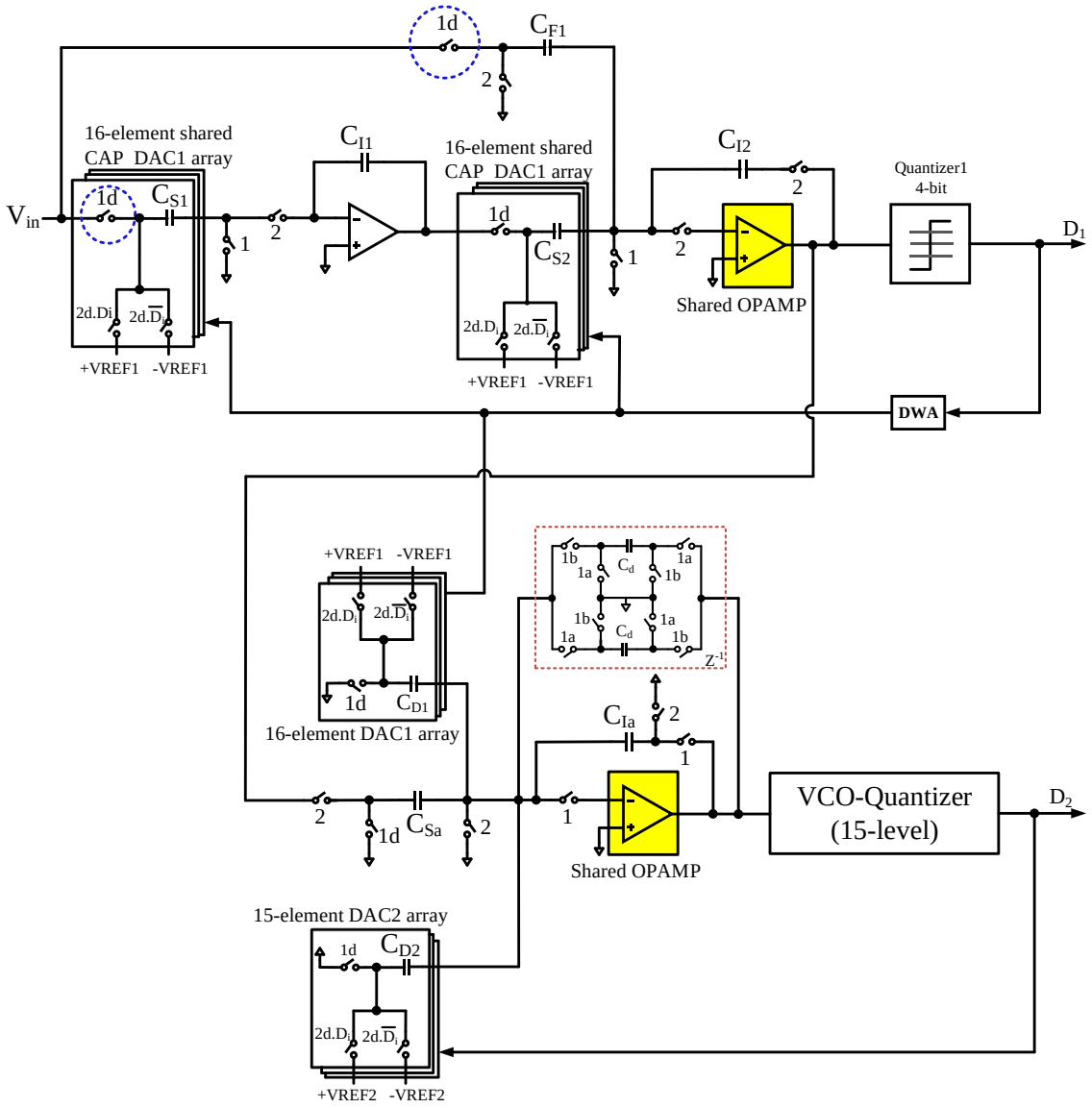
4.4 Circuit Implementation

This section explains the circuit-level implementation of the proposed ADC with more details about each blocks and their design requirements.

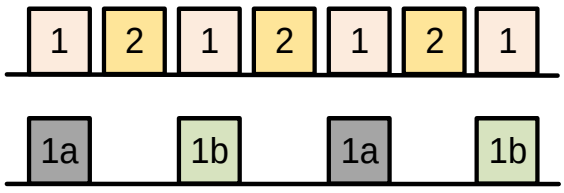
Figure 4.9 shows the circuit-level implementation block diagram of 2-2 MASH ΔΣ ADC with noise-coupled VCO-based quantizer and OPAMP sharing. The single-ended version is shown for simplifying purpose, but the actual implementation is differential. The first stage has 4-bit quantizer which is implemented as flash ADC. And the second stage has VCO-based quantizer which implemented with current starved inverter chain ring oscillator. The second integrator of first stage and adder of second stage are sharing OPAMP. At clock phase 2, shared OPAMP is working as integrator at first stage. And at clock phase 1, it works as adder block for second stage. A Data-weighted averaging DWA block is used to linearize multi-bit feedback DAC elements. To implement a delay block of z^{-1}, a set of switched-capacitor are used as shown in Fig. 4.9. The required timing and timing diagram of the ADC shown in Fig. 4.9.b. Following are more details of VCO quantizer and other blocks.

4.4.1 VCO-Based Quantizer

Figure 4.10 shows the schematic of the VCO quantizer that has been used in this design. The implemented circuit is pseudo differential and only half of the VCO quantizer shown here for simplicity and the other half is exactly the same circuit but with negative input and output signals. The VCO implemented with 15 stage current starving inverter ring oscillator. The inverter-based VCO is very compact with fast switching speed. More bits can be achieved increasing the number of inverters in the oscillator. The cross coupled transmission gates across the positive output to negative input and vice-versa provides the complementary phases at the output and input of each stage of the oscillator. The free running frequency of the oscillator should be FS/4 and it should have linear K_{VCO} for the input range.



a)



b)

Fig. 4.8 a) Circuit-level implementation block diagram of 2-2 MASH ΔΣ ADC with noise-coupled VCO-based quantizer and OPAMP sharing b) timing diagram.

Since the sampling frequency is Fs =160 MHz in this design, it leads to 40 MHz free-running frequency for oscillator. Achieving high K_{VCO} at this low free running frequency is difficult, and therefore it needs sort of amplification in tuning current which is controlled by input signal. As shown in Fig. 4.10 the tuning current is equal to:

$$I_{tune} = K * V_{ctrl} + K_2 * V_{ctrl} + K_1 * V_{ctrl}^{-} \tag{4.6}$$

Which means when the V_{ctrl} increases the current sources I and I_2 sinks more current and I_1 source less current, therefore the current through inverter chain increases more. And when V_{ctrl} decreases the current sources I and I2 sinks less current and I_1 sources more current and therefore the current through inverter chain decreases more. This is equal to amplification of the V_{ctrl} and it helps to achieve higher K_{VCO}. The linearity of the designed VCO is more than 7-bit, based on the simulation result for 150mVp-p input signal. Differential output of each stage of ring oscillator get sampled through sense-amplifier and then delayed one clock period by DFF. Figure 4.11 shows the schematic of the sense-amplifier and DFF. The final output code is provided by XOR of the output of SA-DFF and DFF. To set the free-running frequency to desired value over the process variation, tunable device has been used in tuning current cell which is digitally controlled. The digital output of the VCO quantizer is a thermometer code and it has converted to binary code by thermometer-to-binary decoder.

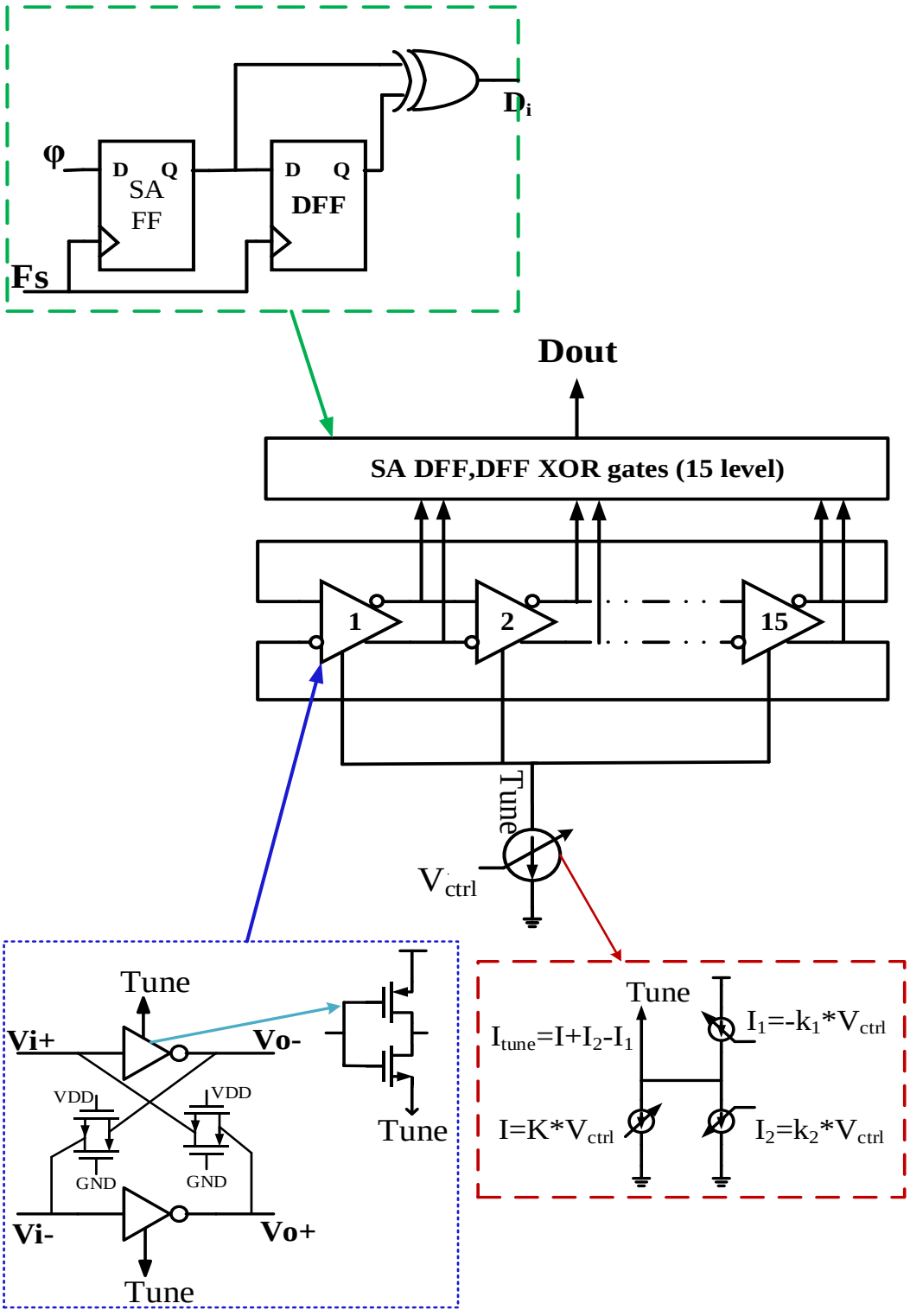
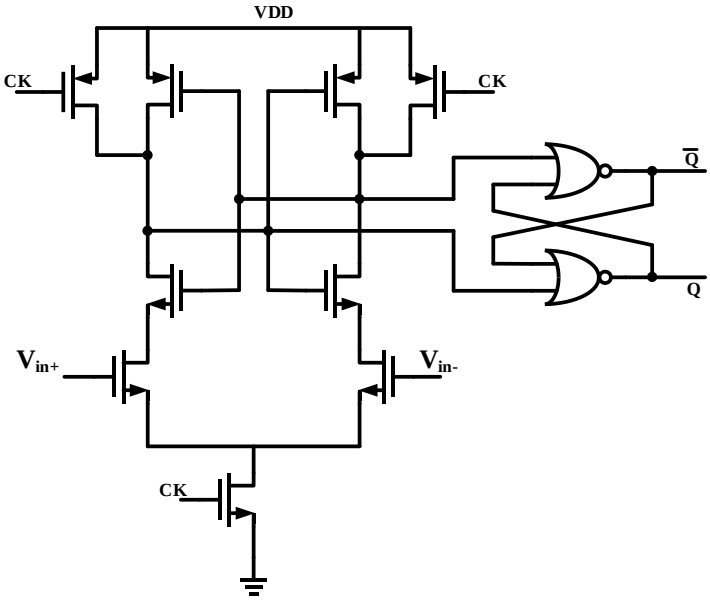
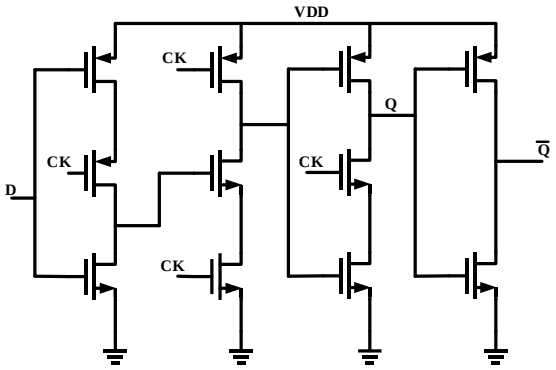


Fig. 4.9 Schematic of the VCO quantizer with 15-stage ring oscillator.



a)



b)

Fig. 4.10 a) Schematic of the sense-amplifier DFF b) True single phase clock DFF.

4.4.2 OPAMP Circuit

Two different OPAMP with different specification were designed to build the switched-capacitor integrators. First integrator has its own individual OPAMP but the second integrator shares the OPAMP with the adder of the second stage. Telescopic structure has been used for the OPAMP, to achieve higher bandwidth. A feed-forward path provided from input signal to the second integrator to bypass the input signal from the first integrator, therefore the output swing of first integrator is relaxed and it processes only quantization error. This let us to use more stacked devices at the telescopic OPAMP to achieve higher DC gain which is required for first OPAMP. The second OPAMP requires less DC gain but it needs higher output swing. Figure 4.12 shows the required DC gain of OPAMP based on system level simulation in Matlab. However higher DC gain would improve the matching between the analog loop filter and digital filter.

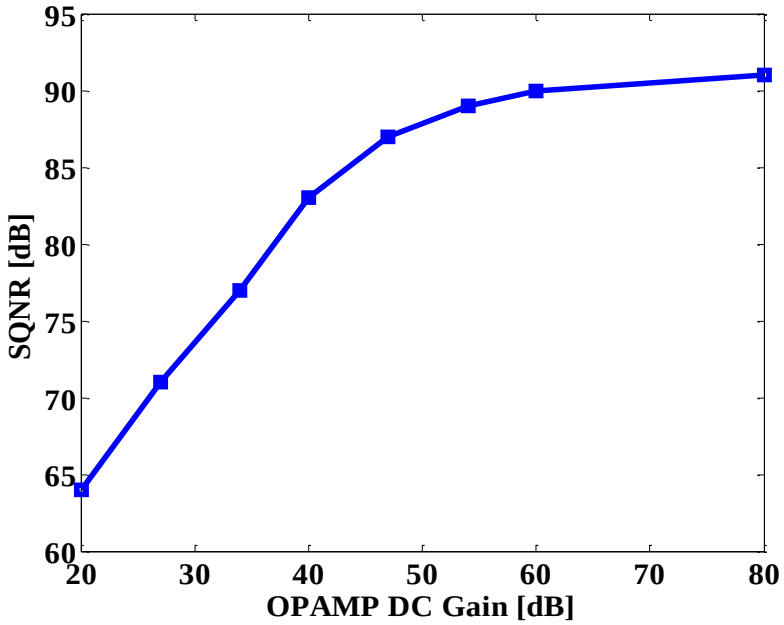


Fig. 4.11 SQNR vs OPAMP DC gain.

Required unity-gain bandwidth estimated based on each integrators configuration at sampling and integrating phases. Figure 4.13 shows first and second integrator including their connected load capacitance. The unity-gain bandwidth can be calculated as:

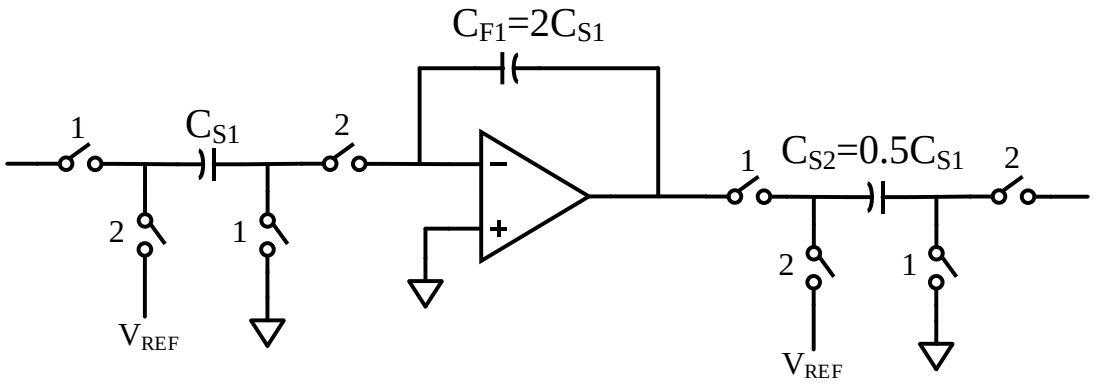
$$UGB \approx \frac{(N+1).\ln(2)}{\pi.\beta.t_{sett}} \tag{4.7}$$

Where N is the settling accuracy, t_{sett} is the settling time and β is feedback factor. Higher feedback factor reduces the required UGB. For first stage the feedback factor is 2/3 and at second stage the initial feedback factor was 1/5, before the gain scaling of second stage. By moving the gain of two from integrator to quantizer and reference voltage, the new feedback factor becomes 1/3, which allows to save power at the OPAMP by reducing the required UGB. Even though the feedback factor is higher for second stage, but we can use smaller capacitor sizes after first stage, and it reduces the effective capacitance load for the OPAMP.

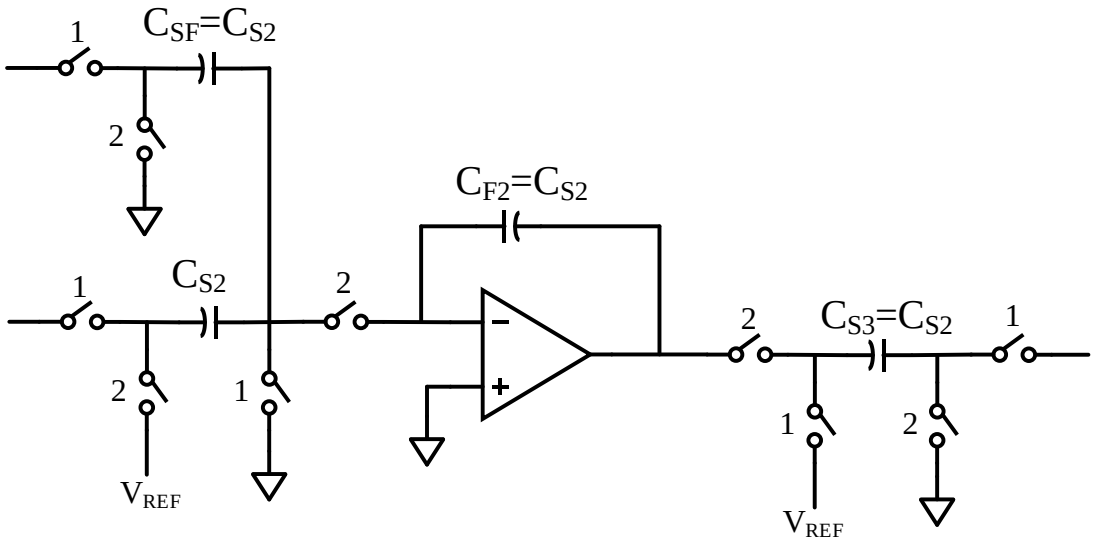
Figure 4.14 illustrates the OPAMP schematic which used in first integrator including its bias circuit and common-mode feedback circuit. It achieves DC gain of 55 dB and UGB of 1.5 GHz with 1.8V supply voltage. Second OPAMP is shown in Fig. 4.15 which is shared between second integrator and adder of the second stage. Common-mode feedback of this OPAMP is active at both phases 1 and 2. This amplifier achieves a UGB of 1.7 GHz with 50 dB DC gain.

Table 4-1Simulated performance of designed OPAMPs.

	DC Gain (dB)	**UGB (GHz)**	**PM (°)**	**I_{tot} (mA)**	**VDD (V)**
OPAMP1	55	1.5	65	2.02	1.8
OPAMP2	50	1.7	63	2.12	1.8

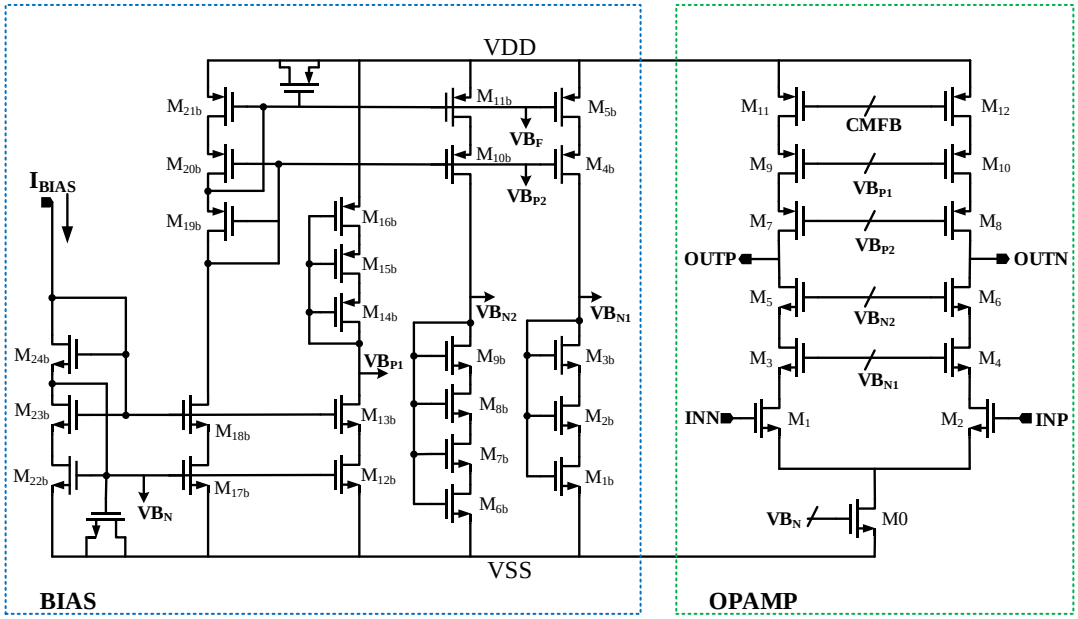


a)

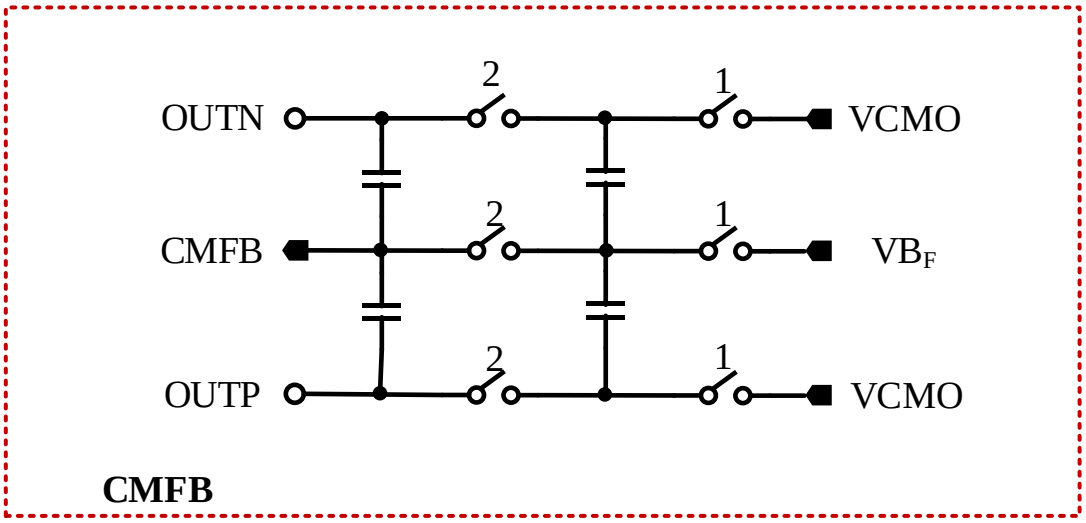


b)

Fig. 4.12 a) First integrator and OPAMP configuration b) Second integrator and OPAMP configuration.

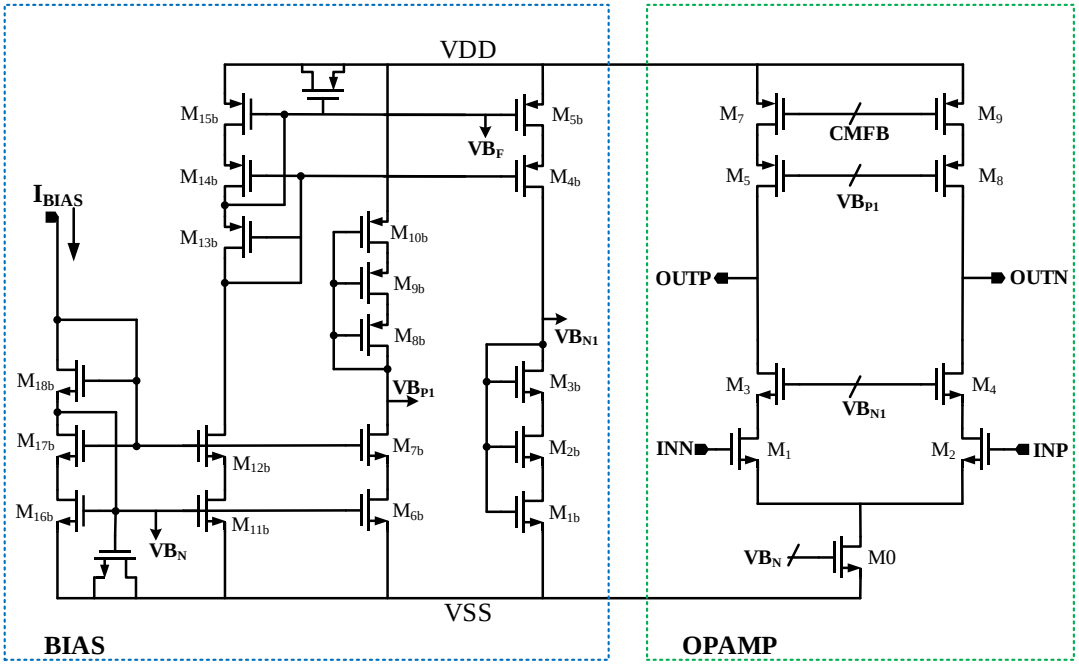


a)

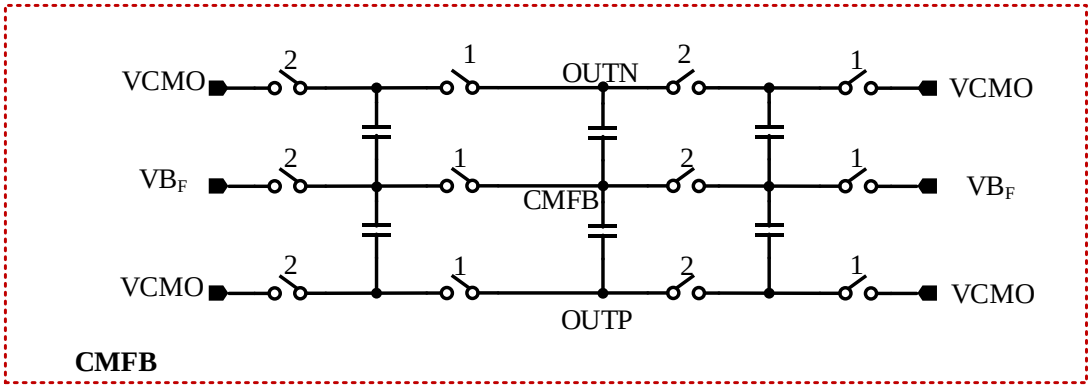


b)

Fig. 4.13 a) OPAMP schematic with bias circuit and b) Switched capacitor common mode feedback.



a)



b)

Fig. 4.14 a) OPAMP schematic with bias circuit and b) Switched capacitor common mode feedback.

4.4.3 First Quantizer

The quantizer in first stage is a 4-bit flash ADC which compromises 16 comparators, reference voltages and thermometer to binary decoder circuit. Each comparator employs a pre-amplifier followed by regeneration latch and set-reset latch. Pre-amplifier is used for auto-zeroing and offset canceling, and it also reduces the kick-back noise and input referred noise from regeneration latch to the comparator's input. In phase-1 input offset along with reference voltage get sampled in C_{AZ} and in comparison phase (phase-2) the sampled reference voltage get compared with input signal. The sampled input offset at phase-1 gets canceled with input offset at phase-2. As shown in Fig. 4.16 pre-amplifier implemented with differential pair with diode-connection and positive-feedback load. Diode-connection devices set the common-mode of the output and the positive-feedback devices improves the DC gain of the pre-amplifier. The main source of the input referred-offset and noise are input differential pair. The auto-zeroing capacitor C_{AZ} size is determined by considering the time-constant of the C_{AZ} and resistor ladder of the reference voltage generator. This capacitor also loads the previous stage which means it should be chosen small. But from the other side the capacitive divider formed by C_{AZ} and parasitic capacitor of the input devices, attenuate the input signal during the comparison. Therefore the larger capacitor leads to lesser attenuation. The dedicated time for the comparator is the non-overlapping time of the clock phase-1 and clock phase-2 which this time should be as small as possible to dedicated more time for simplification and integration. Based on the simulation results the worst-case delay time of the comparator is < 300ps. Also the simulation result shows that the total integrated input referred noise of the comparator is 5-mV, which is very smaller than LSB.

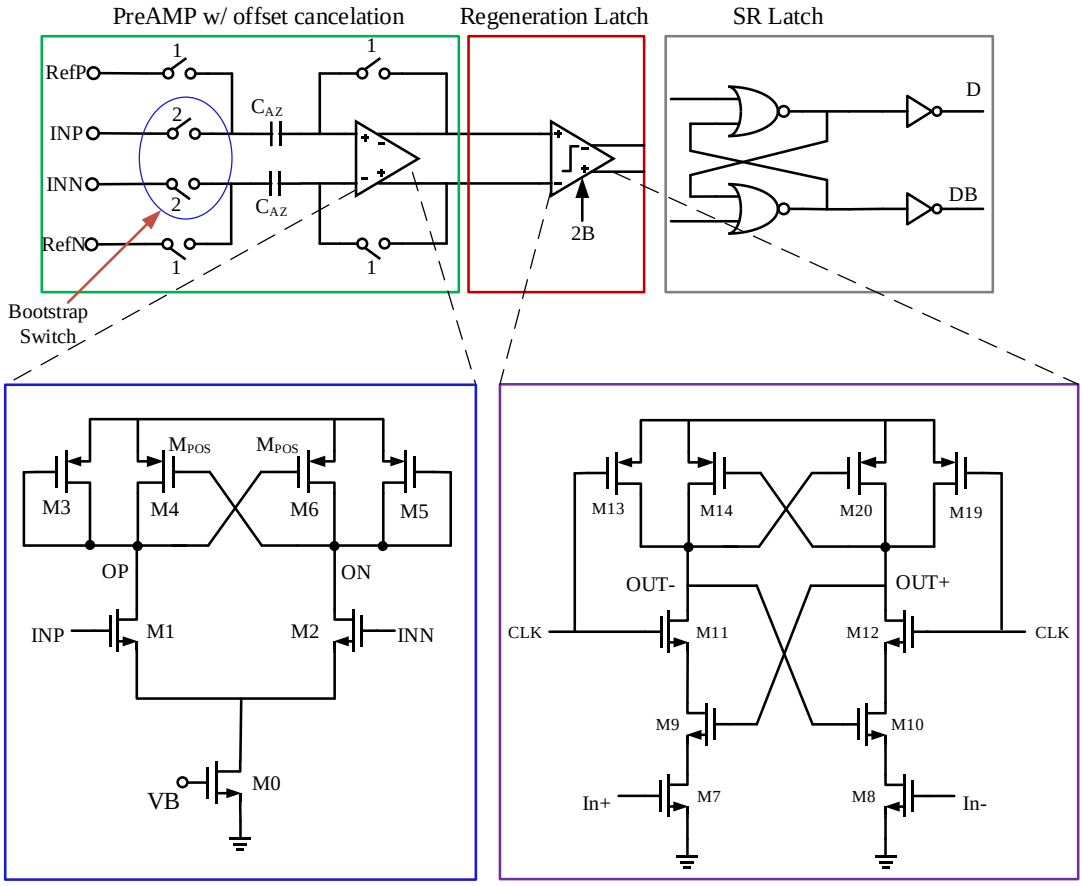


Fig. 4.15 Circuit block diagram of the comparator in first stage flash quantizer.

4.4.4 Clock Generator Circuit

On-chip clock generator (Fig. 4.17) has been designed to create the different clock phases that have been used in the ADC.

There is main non-overlapping clock phase (1 & 2) and also the delayed version of them which is used to reduce the charge injection and clock feedthrough effects. In additional to these clock phases the clock phases (1a & 1b) are generated which have been used in second stage of the ADC. Applied external clock is 2x of the sampling clock and it is divided by two on-chip, to realize 50% duty cycle. Transistor $M_{1a,\,b}$ is used to synchronize the rising edge of the clock phases (1 & 1d, 2

& 2d). Frequency and duty cycle of the clock phases 1_a and 1_b are half of the clock phase 1. And clock phases 1_a and 1_b are synchronized by main clock phase1 through the AND gates and ckq signal from the clock phase 1 path. En signal is to have external control over the activation of the Z^{-1} block on the second stage of the ADC for testing and measurement purpose.

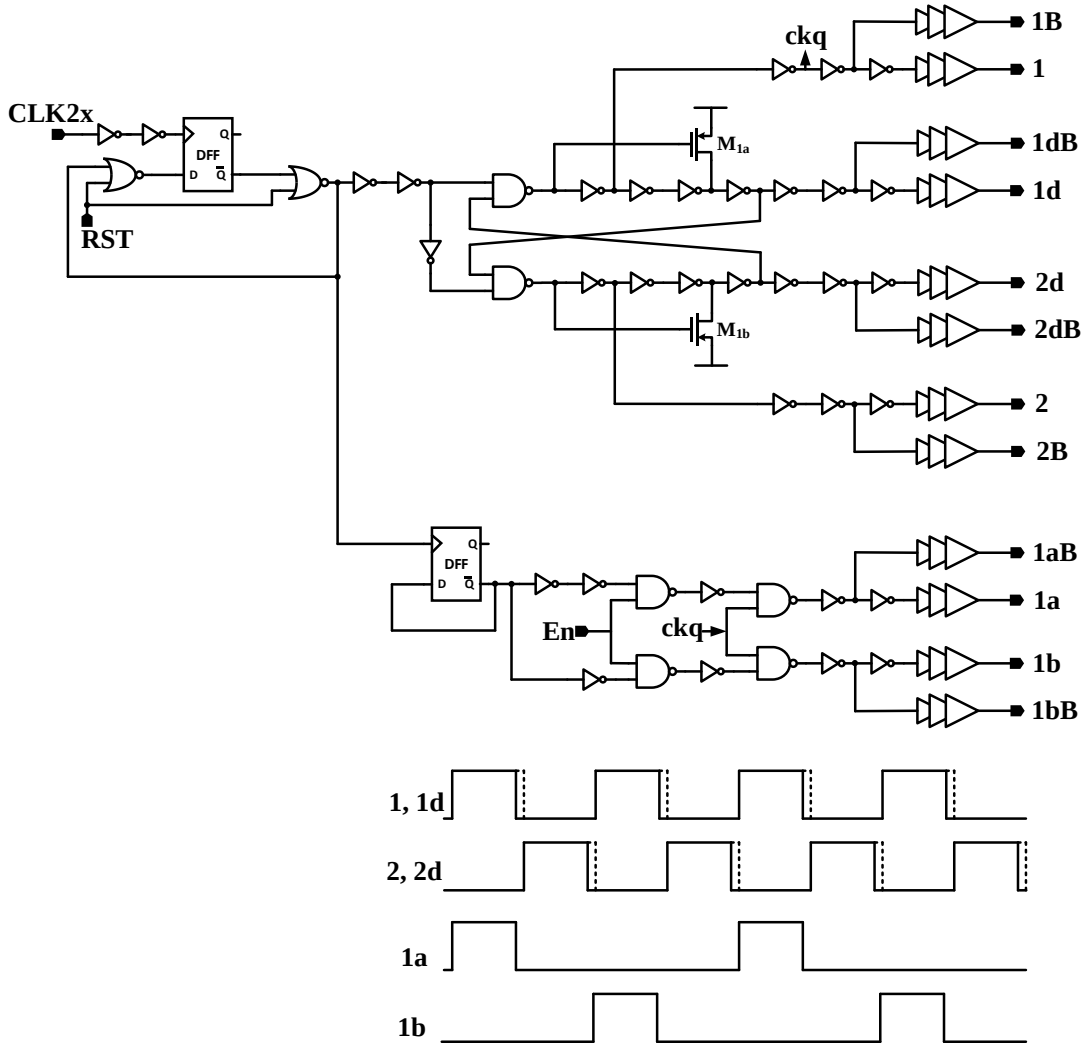


Fig. 4.16 Clock-phases generator diagram.

4.4.5 DWA Circuit

First stage has 4-bit quantizer and the feedback DAC linearity should be enough to satisfy the target resolution. A Data-weighted averaging DWA block is used to increase the linearity of the feedback DAC at first stage [58]. Figure 4.18 shows the block diagram of the DWA block. It consists of thermometer to binary encoder (16-to4), pointer generator (MOD-4), and delay block (DFF) and shifter which is a barrel shifter structure. The 4-bit control signal which is generated by the pointer generator block, based on the input code, controls the shifter. The shifter shift the input code starting from the pointer location. This provides the first of order-noise shaping for the DAC elements and it linearizes the DAC, which is enough for the target resolution. Based on the first stage timing diagram, the quantizer triggers at the falling edge of the clock phase 2, and the DAC gets connected to the integrator at next clock phase 2. Therefore the available time for DWA is more than half clock cycle (2*non-overlapping time + clock phase-1 duty cycle). It relaxes the speed requirement for quantizer and DWA. The critical path's delay for the shifter and DWA control at worst case is extracted and estimated based on simulation to make sure it is less than the allocated time.

The second stage's DAC doesn't require DWA, since the VCO-based quantizer has inherent barrel shifting which provide a dynamic element matching (DEM) for its DAC elements.

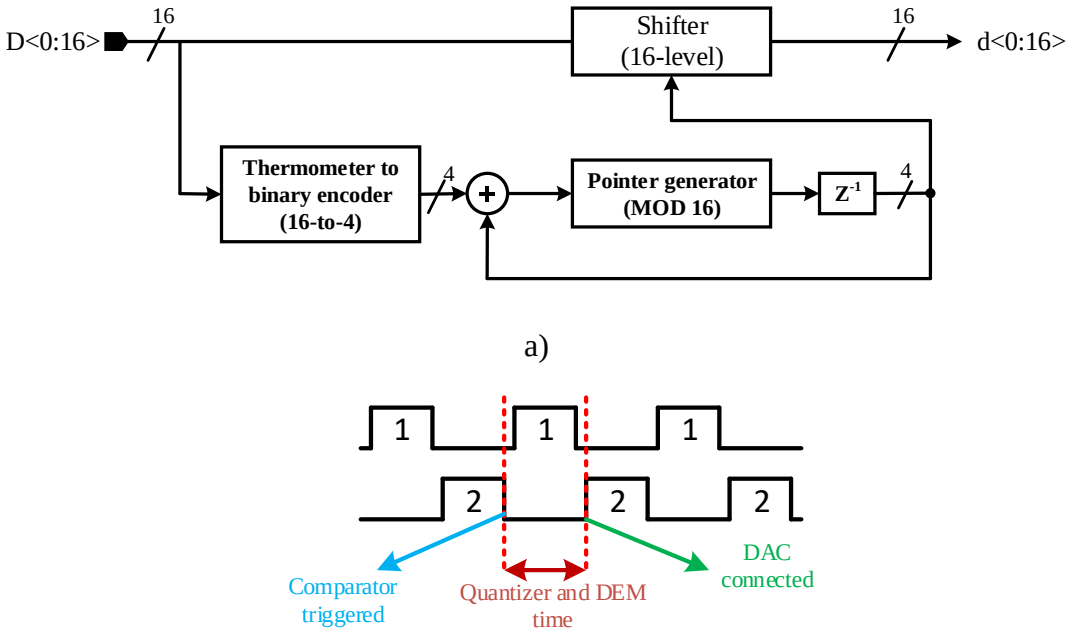


Fig. 4.17 a) DWA block diagram, b) timing diagram of DWA.

4.5 Results

The prototype ADC was designed and implemented in 0.18 µm 2P6M CMOS process technology with MIM and PIP capacitors option. The chip layout is shown in Fig. 4.19. The chip size is 4 mm x 4 mm with core area of 1.7 mm x 0.7 mm. The chip has 80 total PAD, where for input, reference, biasing and supply signals, two or more PADs were used to have parallel wire bonding in order to reduce the total inductance of the wire bonding. Figure 4.20 shows the chip package and its wire binding's connections. A 48-PINs package has been used, where most analog signal PINs has parallel connection to reduce bonding wire inductance.

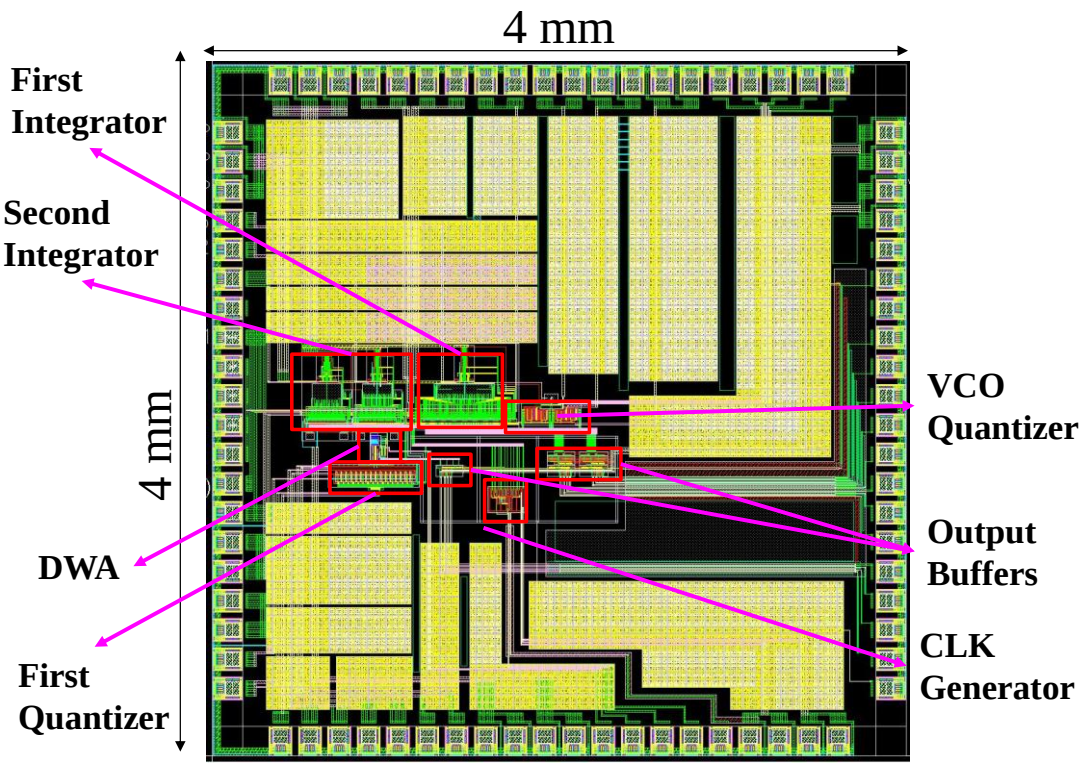


Fig. 4.18 Chip Layout.

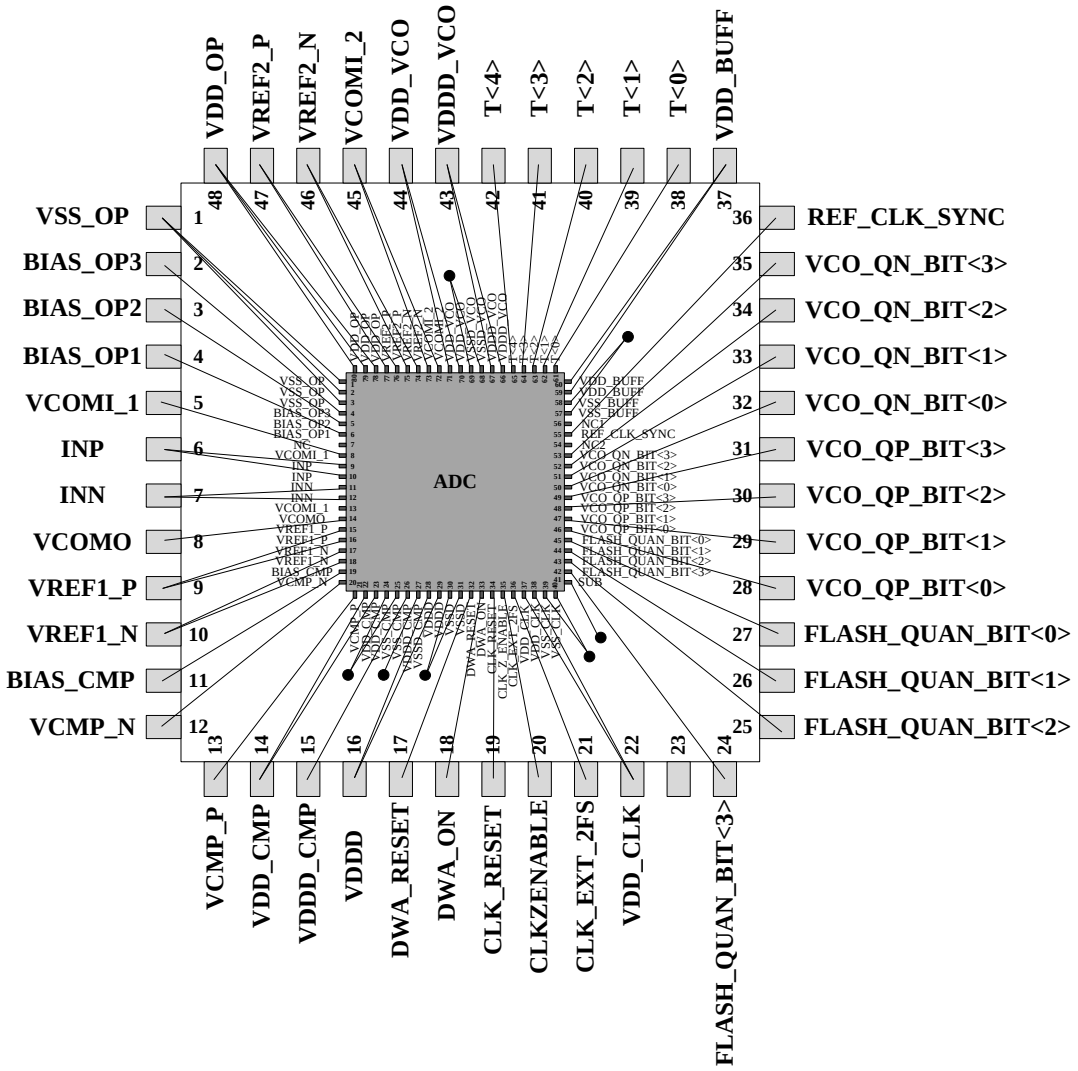


Fig. 4.19 Chip package and PIN connections.

The analog power supply is 1.8 V and the digital power supply/ VCO power supply is 1.6 V. There are 4-bit trimming for VCO to calibrate the process variation and set the free-running frequency of the VCO for designed Fs/4. Also VCO has separate power supply which makes it possible to trim its frequency by adjusting the power supply.

Figure 4.21 shows the power spectrum density of the ADC for input signal frequency of 0.47 MHz at sampling frequency of 160 MHz. The achieved SNDR and SFDR are 80.54 dB and 94.6 dB respectively at 8 MHz input signal bandwidth.

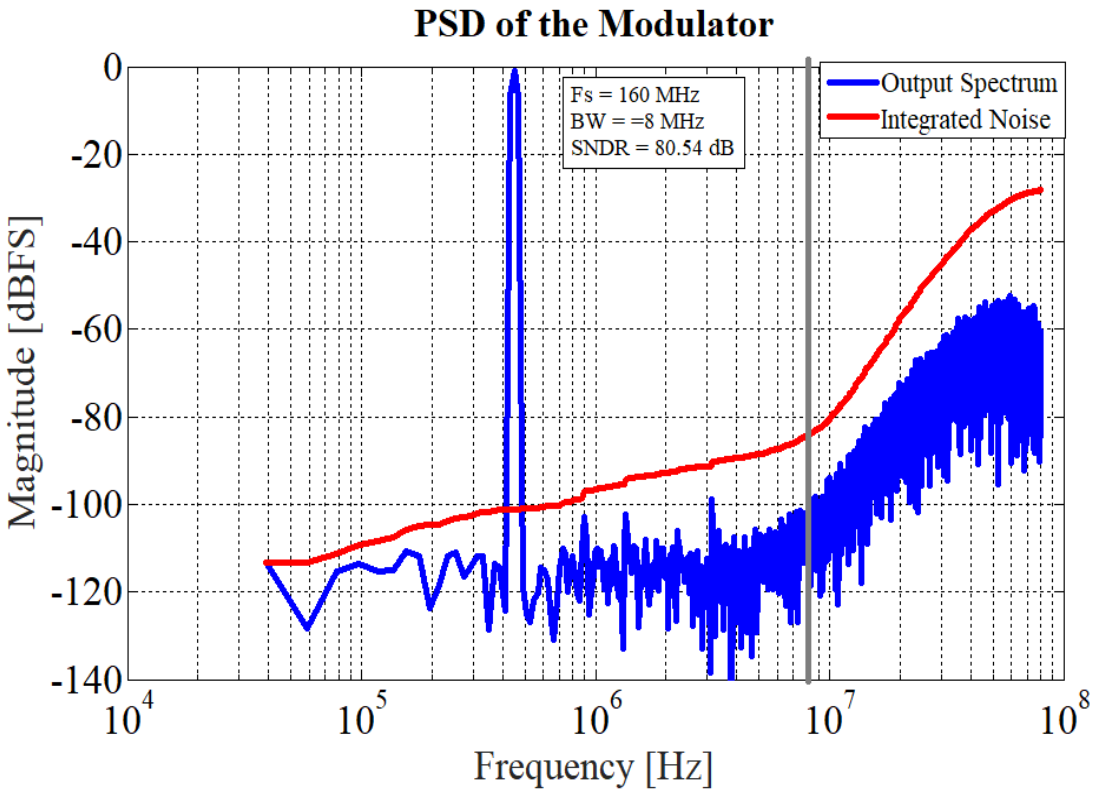


Fig. 4.20 Output power spectrum density.

Table 4-2 Summary of Performance

Technology	0.18 µm CMOS 2P6M
Supply Voltage [V]	1.8 (A), 1.6 (D)
Input Range (Diff) [V]	2.8
Sampling Frequency [MHz]	160
Signal Bandwidth [MHz]	8
Peak SNDR [dB]	80.54
Peak SNR [dB]	81.3
SFDR [dB]	94.6
Power Dissipation [mW]	20.5
FoM_W [fJ/Conv.]	157
FoM_S [dB]	166

$$FOM_W = \frac{Power}{\min\{fs, 2\times ERBW\}\times 2^{ENOB}} \tag{4.8}$$

$$FOM_S = SNDR + 10.\log\left(\frac{BW}{Power}\right) \tag{4.9}$$

4.6 Summary

A noise-coupled VCO-based quantizer was presented. It improves the noise-shaping order of the VCO-based quantizer. A second order noise-shaped quantizer employed by the proposed structure. Then to enhance the dynamic range and achieve higher dynamic range, the proposed quantizer is used in 2-2 MASH delta-sigma modulator. To improve the power efficiency, opamp sharing technique has been employed in the proposed MASH structure. First stage and second stage are sharing the opamp to reduce the number of active elements and thus the power dissipation. The modulator has been designed and implemented at 0.18 µm 2P6M CMOS process technology. It achieves the peak SNDR/SFDR of 80.54 dB/94.6 dB over 8 MHz bandwidth at 160 MHz sampling frequency. The ADC occupies 1.7 mm x 0.7 mm area in a 4 mm x 4 mm chip.

CHAPTER 5. A PASSIVE 3RD ORDER DELTA-SIGMA ADC WITH VCO-BASED QUANTIZER

Abstract

In this chapter a passive delta-sigma ADC with a voltage-controlled-oscillator (VCO) quantizer is presented. By employing the VCO quantizer, a single-bit quantizer is replaced with a multi-bit quantizer while an extra order of noise-shaping was provided. The proposed architecture does not need very large capacitors as compared to the conventional passive delta-sigma ADC. Furthermore, it also does not require external dynamic element (DEM) matching, because the VCO has an inherent DEM. Since there is attenuation in the passive integrators, the input signal range to the VCO is small and within the linear range of the VCO, therefore the nonlinearity of the VCO is not issue. Both conventional second order passive delta-sigma modulator and the proposed structure has been simulated for comparison. The simulation results verify the effectiveness of the proposed structure.

5.1 Introduction

Low power performance is necessary for portable applications and biomedical devices. The passive switched capacitor integrator is very simple, low power and process scalable. Therefore passive delta-sigma modulator (PSDM) which consists only of capacitors, switches and a comparator is a very power efficient and good candidate for low voltage operation. Recently, PSDM were designed and presented in both discrete time DT and continuous time CT. In [59], [60] a discrete time second order passive delta-sigma ADC has been presented. None of the DT PSDM are higher than second order and also they are mostly very narrow bandwidth due to the gain requirement in the comparator. Also in DT PSDM in order to achieve

higher signal-to-noise and distortion ratio SNDR, very large capacitors are required, which are not area efficient especially for body implantable biomedical devices. In [61] a continuous time multi-stage noise shaping MASH ADC were demonstrated with a third order of noise-shaping. However, this requires two stages and thus two gain stages. Also, it needs a matching between the analog and digital path which is a common requirement in MASH structure.

In the all previous presented PSDM, the quantizer is a single-bit. Since there is an attenuation before the quantizer and the input signal of the quantizer is very small and therefore multi-bit quantizer is non-practical. Also single-bit quantizer is used to provide higher gain in the comparator. Usage of the multi-bit quantizer can increase the SNDR.

Voltage controlled oscillator (VCO) based ADCs became popular in oversampling ADCs, due to their highly digital circuit architecture, inherent noise shaping [51]. VCO-based quantizer is a multi-bit quantizer which provides a first order of the noise-shaping and also has inherent dynamic element matching DEM and therefore it does not require explicit DEM which is the main drawback of the multi-bit quantizer and their feedback digital-to-analog DAC. VCO-based quantizer is process scalable and can be operated at lower voltage.

In this work we present a single loop passive VCO-quantizer based delta-sigma ADC with third-order noise-shaping, where two order noise-shaping comes from the SC loop filter and another one comes from the VCO-based quantizer. Since the input signal of the VCO-quantizer is very small therefore it does not suffer from the nonlinearity of the VCO. The VCO quantizer provides a multi-bit quantizer with an inherent DEM.

5.2 Passive Switched Capacitor Integrator and Passive Sigma-Delta Modulator

Figure 5.1 shows the passive switched capacitor integrator with parasitic capacitor included. At φ_1 input signal gets sampled to Cs and at φ_2 it transfers to C_I, where φ_1 and φ_2 are non-overlapping clock signals. C_p represents the parasitic capacitor at the connection node of the C_s and C_I. The transfer function of the integrator is

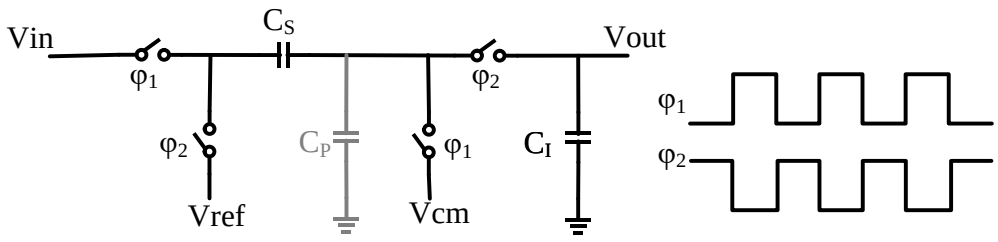


Fig. 5.1 Passive switched capacitor integrator.

$$H(z)=\frac{Vout(z)}{Vin(z)}=\frac{\alpha z^{-1}}{1+\rho-(1-\alpha)z^{-1}} \tag{5.1}$$

$$\alpha=\frac{C_S}{C_S+C_I}\,,\qquad \rho=\frac{C_P}{C_S+C_I}$$

Where C_s, C_I and C_p are sampling, integrating and parasitic capacitor respectively. The DC gain and bandwidth of this integrator is

$$A_{DC}=\left|H(z=1)\right|=\frac{C_S}{C_S+C_P}$$

$$f_{-3dB}=\frac{f_S}{2\pi}.\frac{C_S+C_P}{C_S+C_I+C_P} \tag{5.2}$$

Here Fs is sampling frequency.

Figure 5.2 shows the frequency response of this integrator for different ratio of the C_s/C where C is the sum of the C_s, C_I and C_p. For the fix sampling frequency, lower bandwidth will result in a higher attenuation at the end. Which means a larger C_I with a fix C_s value. Figure 5.3 shows a second order passive modulator based on the passive integrator [59]. The output of this modulator is

$$D_{out} = \frac{G_c H_1 H_2 V_{in} + G_c H_1 H_2 E_{H1} + G_c H_2 E_{H2} + G_c E_{comp} + E_q}{1 + G_c H_2 (b_2 + b_1 H_1)} \qquad (5.3)$$

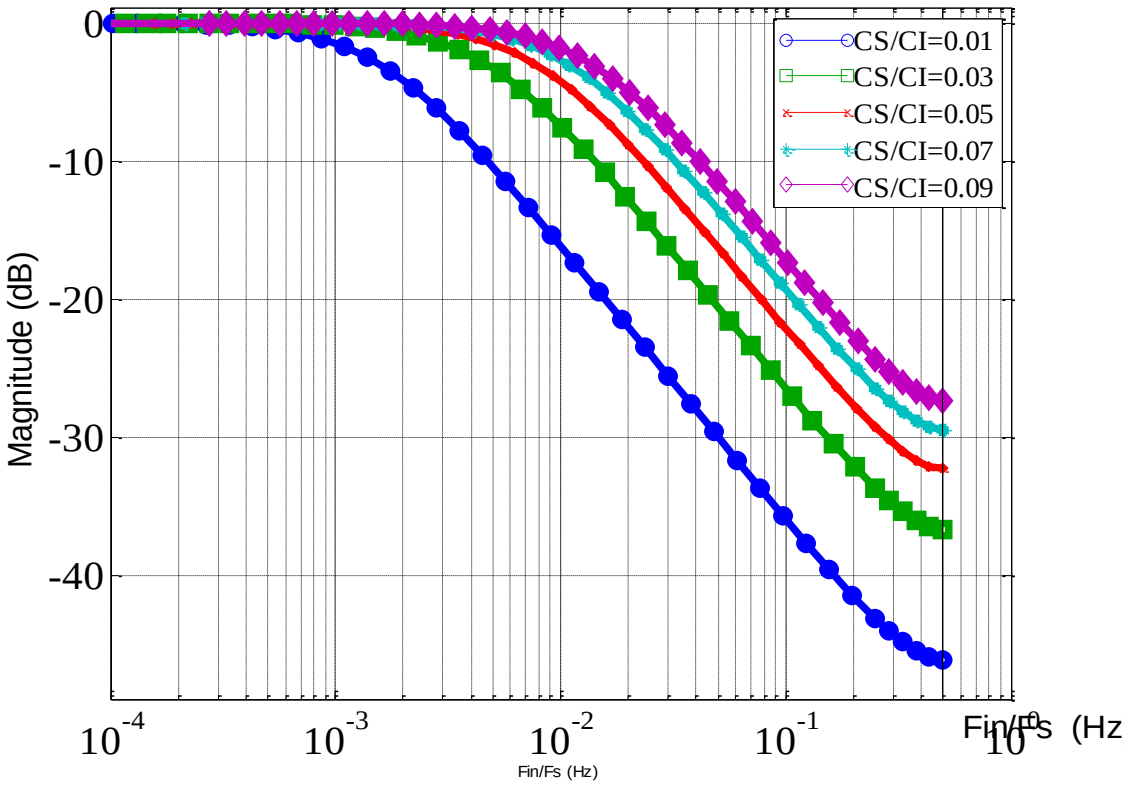


Fig. 5.2 Passive switched capacitor integrator frequency response for different C_s/C_I value.

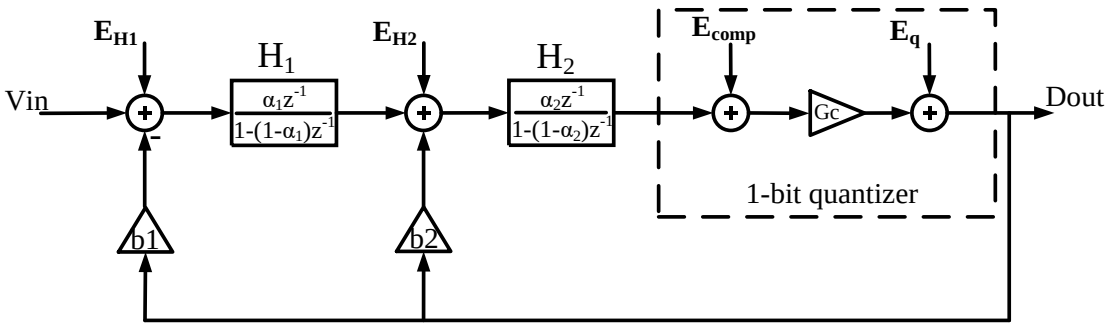


Fig. 5.3 Passive 2nd order delta-sigma ADC with single-bit quantizer.

Since $b_1 >> b_2$ we can simplify the equation to

$$D_{out} \simeq \frac{V_{in}}{b_1} + \frac{E_{H1}}{b1} + \frac{E_{H2}}{H_1 b1} + \frac{E_{comp}}{H_1 H_2 b_1} + \frac{E_q}{G_c H_1 H_2 b_1} \tag{5.4}$$

Where $H_{1,2}$ are the integrators transfer functions, and $E_{H1,2}$ are their input-referred noise, respectively, while E_{comp} and E_q denote the comparator's noise and the quantization noise.

Here G_c is the equivalent gain of the quantizer and larger G_c means smaller quantization noise at the output. The G_c can be calculated by finding the total loop attenuation at the Fs/2

$$G_C = \frac{1}{\left|H(fs/2)\right|} \quad , \quad H = H_1.H_2 \tag{5.5}$$

For the same sampling frequency and sampling capacitor size (which is determined by thermal noise requirement) as shown in Fig. 5.2 larger attenuation and therefore larger G_c needs bigger integrating capacitor. However this will decrease the bandwidth as shown in Fig. 5.2 and equation (5.2). Generally for higher bandwidth we need to increase the sampling frequency dramatically and for lower quantization noise we need to increase the integrating capacitor size.

5.3 The Proposed Passive ΔΣ ADC with VCO-based Quantizer

To improve the SNDR of the passive delta-sigma modulator we can use a multi-bit quantizer or increase the order of noise-shaping. But in a conventional passive delta-sigma modulators, since there is attenuation in the loop and the input of the quantizer is very small, using the conventional multi-bit quantizer is impractical. From the other side the conventional multi-bit quantizer requires dynamic element matching too. Increasing of the noise-shaping order with adding another passive integrator to the loop will cause more attenuation in the loop and therefore introduces more input referred noise.

To overcome these issues, we have proposed a passive delta-sigma ADC employing the VCO-based quantizer as shown in Fig. 5.4. Since the input of the quantizer is very small we can use VCO as quantizer which provides multi-bit quantization. On the other hand, the main issue of the VCO-base quantizer, the nonlinearity of the VCO, would not be a problem in this structure. Since the input of the VCO quantizer is attenuated by the loop; it is very small, and therefore it is within the linear range of the VCO.

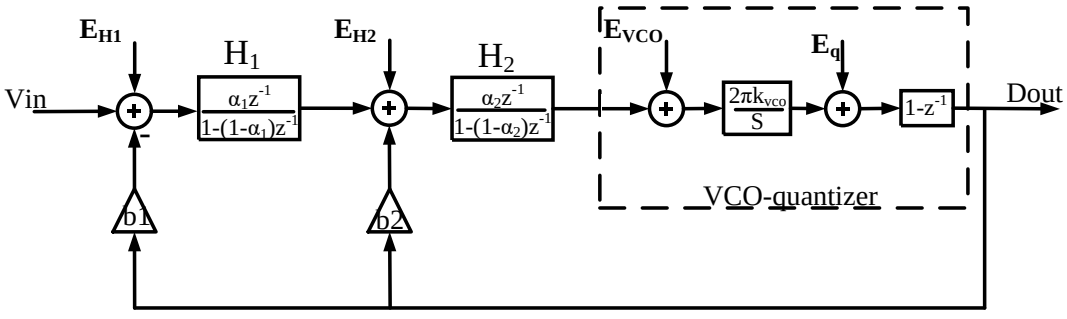


Fig. 5.4 Proposed passive 3rd order ΔΣ ADC with VCO-based quantizer.

The VCO-based quantizer provides an extra order of noise-shaping by itself, therefore the total 3rd order of noise-shaping will be achieved with only two passive integrators. Multi-bit quantization and one more noise- shaping order improves the SNDR of the modulator in comparison to the original one.

The proposed architecture can operate at higher bandwidth in contrast with the conventional single-bit passive modulator. As explained in the previous section very large over sampling ratio OSR is necessary in conventional passive modulator, since the comparator's equivalent gain is proportional to the OSR. On the other hand, the capacitors ratio and size, which determines the integrator's bandwidth and therefore the OSR, increases by the OSR. In the proposed structure the quantizer gain is defined by the VCO gain, which is independent of the attenuation of the passive integrators in the loop. Therefore smaller capacitors can be used and the only consideration is the input referred thermal noise to determine capacitors size.

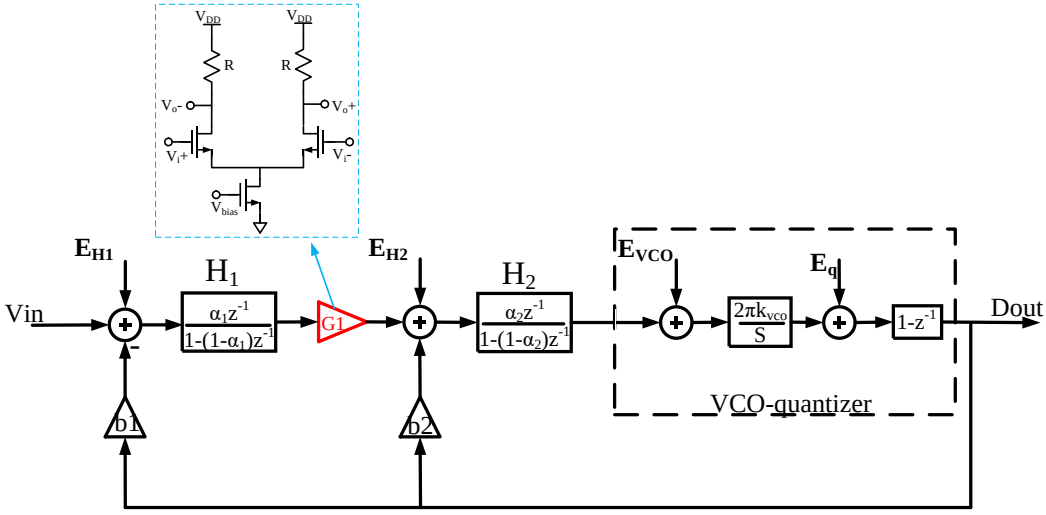


Fig. 5.5 Proposed passive 3rd order ΔΣ ADC with VCO-based quantizer and gain stage between passive integrators.

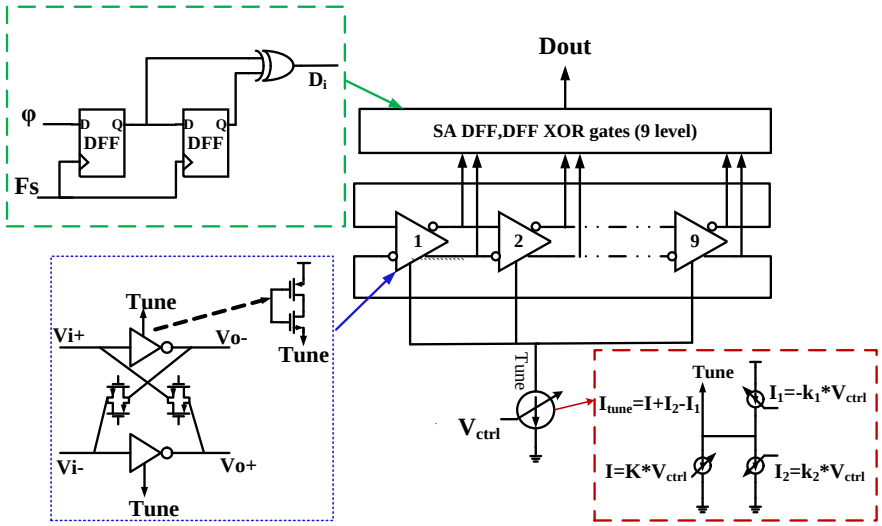


Fig. 5.6 The VCO quantizer circuit schematic with 9-level ring oscillator and the control circuit.

To improve the performance on the proposed structure and also remove the loading effect of the passive integrators, a simple gain stage is introduced between the first and second passive integrator, which acts like a buffer to isolate the two passive integrators and also increases the total loop gain [62]. It helps to have input referred noise suppression too, but with a little power cost. Figure 5.5 shows the structure with the gain stage and its circuit diagram [64].

Figure 5.6 shows the circuit schematic of the designed and used VCO quantizer [50]. It consists of a 9-level ring oscillator with tuning current, which is controlled by the input voltage of the VCO. The output of each stage is detected by the sense amplifier, sampled by DFF, which gets delays by a one clock period and finally XOR of them will be the quantizer output. This circuit is mostly digital. It is voltage and process scalable. The sampling frequency is Fs=625MHz and the VCO is designed for an Fs/4 free running frequency.

5.4 Simulation Results

The proposed passive ΔΣ ADC with a VCO-based quantizer was simulated for a 625 MHz sampling frequency, 10 MHz bandwidth. Also the conventional second order passive delta-sigma was simulated for comparison. Figure 5.7 shows the behavioral simulation result and the output power spectrum density (PSD) of the second order passive delta-sigma ADC with a single-bit quantizer. The sampling capacitor is C_s = 1pF and the integrating capacitor is C_I = 32pF. The SNDR is 44.87 dB in 10 MHz bandwidth with effective number of bits (ENOB) of 7.16 bits. While Fig. 5.8 shows the PSD of the proposed passive delta-sigma ADC with 9-level VCO quantizer. The supply voltage is V_{DD} = 0.9 V in 0.18 µm CMOS process. In the proposed structure the sampling capacitor Cs = 1pF, and the integrating capacitor is C_I = 8pF, which is four times smaller than the conventional counterpart. It achieves third order of noise-shaping. The SNDR is 64.12 dB in 10 MHz bandwidth with ENOB of 10.35 bits [63].

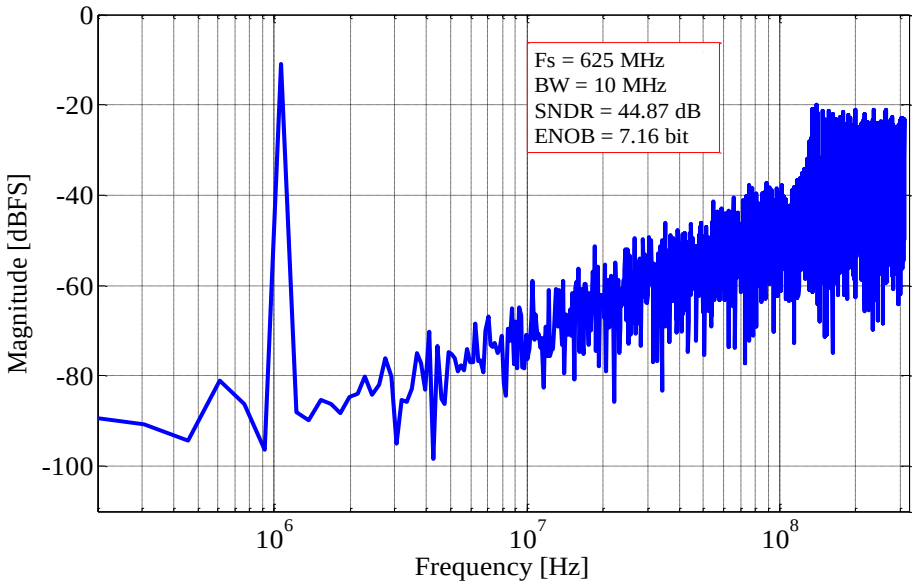


Fig. 5.7 Simulated power spectral density of the second order passive delta-sigma ADC with single-bit quantizer.

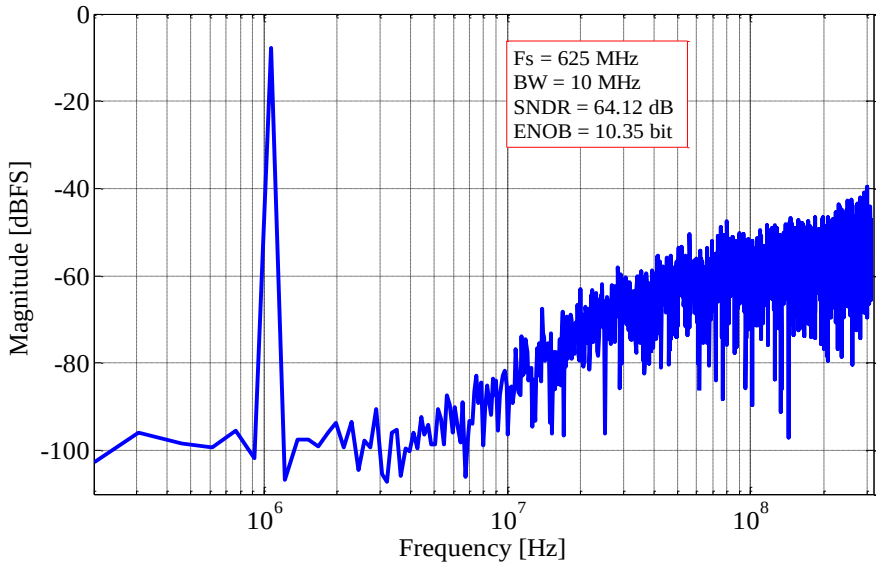


Fig. 5.8 Simulated power spectral density of the proposed passive delta-sigma ADC with VCO quantizer.

Both of the conventional and proposed structures were simulated with added gain stage between first and second passive integrator. Figure 5.9 shows the simulated PSD of the conventional passive delta-sigma ADC with added gain stage with G = 4. It provides a buffering between the first and second passive integrator as well. The SNDR is 53.67 dB in 10 MHz bandwidth with the ENOB of 8.61 bits. Even with added gain stage the performance of the second order passive delta-sigma ADC with the single-bit quantizer is way lower than the proposed architecture. Figure 5.10 shows the simulated power spectral density of the proposed passive delta-sigma ADC with VCO and added gain stage between the first and second passive integrator. The added gain stage amplifies the input signal to the VCO and the nonlinearity of the VCO introduces the harmonics. The SNDR increased to 68.4 dB in 10 MHz bandwidth with ENOB of 11.07 bits.

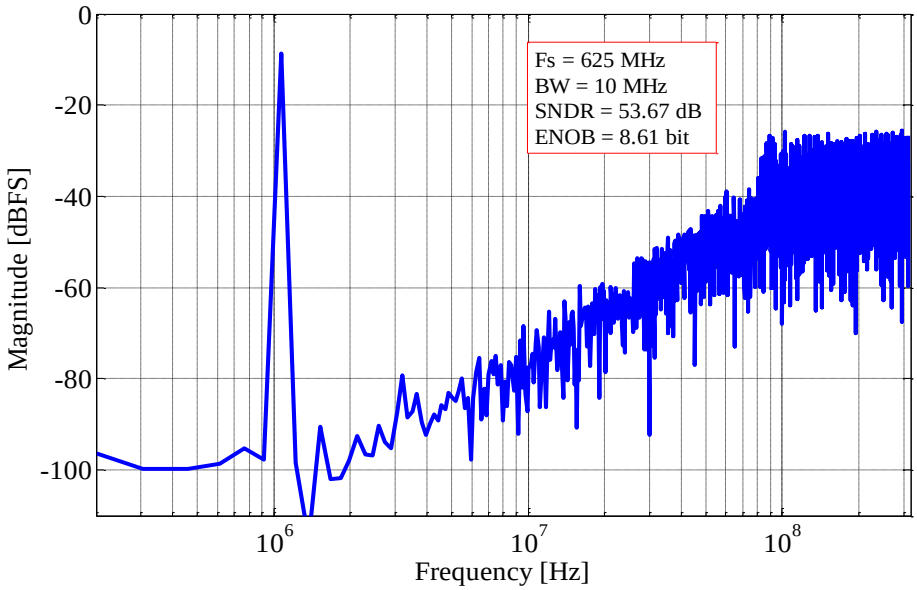


Fig. 5.9 Simulated power spectral density of the second order passive delta-sigma ADC with added gain stage of G_1=4.

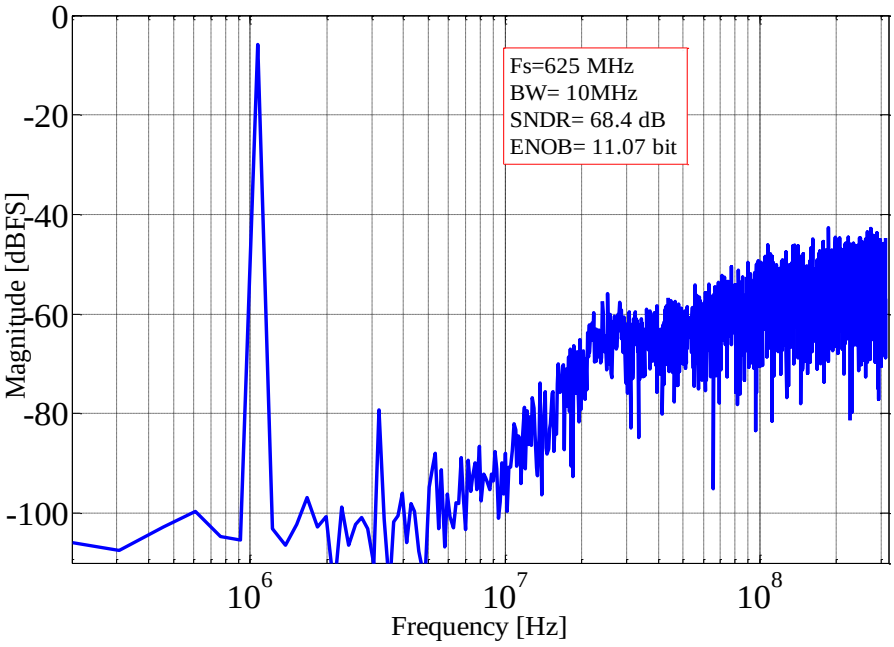


Fig. 5.10 Simulated power spectral density of the proposed passive delta-sigma ADC with VCO quantizer and added gain stage of G_1=4

5.5 Summary

A passive delta-sigma ADC with a VCO quantizer has been presented. By employing the VCO quantizer, a single-bit quantizer was replaced with a multi-bit quantizer while an extra order of noise shaping was achieved. The capacitor sizes are relaxed as compared to the single-bit passive structure. Both conventional passive delta-sigma ADC with single-bit and proposed structure were simulated and compared. The simulation results demonstrate the efficiency of the proposed structure.

CHAPTER 6. CONCLUSION

In this dissertation, first, a power efficient switching scheme for successive approximation register SAR ADC presented. Then based on that an ultra-low power asynchronous SAR ADC presented. The proposed SAR ADC is suitable for biomedical applications, where a low-bandwidth and medium resolution but very low-power ADCs are required. The ADC implemented and fabricated in 0.18 µm 2P4M CMOS process technology. The measurements results shows 9.76 ENOB at 5 kHz bandwidth. The ADC power consumption is 250 nW at Nyquist rate from 0.75 v power supply. Achieve integral-nonlinearity INL and differential-nonlinearity DNL are +0.94/-0.89 LSB and +0.6/-0.37 LSB respectively. The measured peak SNDR was 60.5 dB, the SFDR was 72 dB.

Secondly, a noise-coupled VCO-based quantizer was proposed. In this quantizer the quantization error extracted and feedback to the input of the quantizer through a delay paths. Depending on the delay block one or two order improvement can achieve in total order of noise-shaping. A second order noise-shaped quantizer presented. Then a 2-2 MASH delta-sigma ADC proposed based on the noise-coupled VCO-based quantizer. This helps to reduce the power consumption. To further power saving, the OPAMP of first stage's second integrator and required adder block of second stage were shared. Therefore a 4^{th} order modulator achieved with only two OPAMP. The ADC was designed and implemented in 0.18 µm 2P6M CMOD process technology. Sampling frequency is 160 MHz and bandwidth is 8 MHz. The ADC achieves 80.54 dB peak SNDR at 160 MHz sampling frequency over 8 MHz bandwidth. The achieve peak SFDR is 94.6 dB.

Finally, passive delta-sigma modulator analyzed and a passive 3^{rd} order delta-sigma ADC is presented. A 9-level VCO-based quantizer is used as quantizer to improve SQNR. It also provides higher loop gain comparing to conventional single-bit passive modulator. Another advantage of that is area efficiency, since it needs

smaller capacitance in comparison to conventional passive modulator. The modulator designed in 0.18 μm CMOS process. It achieves more than 64 dB SNDR at 625 MHz sampling rate over 10 MHz bandwidth.

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