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Title DESIGN AND ANALYSIS OF A NANOSECOND PULSE GENERATOR WITH REPEATABLE PULSE WIDTH

Abstract approved

This thesis is concerned with the problems which need consideration when designing a nanosecond pulse generator having a repeatable pulse width and amplitude output. The basic circuit is first presented and analyzed and the reasons for wide variations in pulse width with replacement of transistors are pointed out.

To make the pulse width more repeatable it was necessary to have a constant output from the first stage. This was required since the amount of drive to the second stage was shown to be important for repeatability. The optimum value for the coupling resistor, $R_b$, was determined experimentally by measuring pulse widths for 30 different transistors and various values of $R_b$. A 95% confidence interval was calculated for the variance from the data obtained.

It was shown that it is possible to reduce the response time to the input signal which may be desirable for some applications.
DESIGN AND ANALYSIS OF A NANOSECOND PULSE GENERATOR WITH REPEATABLE PULSE WIDTH

by

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DESIGN AND ANALYSIS OF A NANOSECOND PULSE GENERATOR WITH REPEATABLE PULSE WIDTH

INTRODUCTION

Pulse generation is an important part of much electronic equipment in operation today. Its application can be found in fields such as computer and control systems, radar, television and pulse communications.

For example, a system may contain several waveform generators, and it is usually necessary to incorporate some timing signal so that these waveforms will have some common time reference.

Also a pulse generator may be used to trigger circuits, such as switching a binary counter.

It is the purpose of this paper to describe and analyze a pulse generator with repeatable pulse width. It is assumed that a 100 kHz input square wave is available. An output pulse of fixed duration and a 100 kHz repetition rate is the design objective. In nanosecond circuitry, it is sometimes necessary for the output pulse to occur upon triggering with minimum delay. A way of doing this is described with repeatability of pulse width still intact.

The term "repeatable" is an important consideration in industry. There are circuits which give fast responses with short rise and fall times but are not repeatable. An example of a circuit having a non-repeatable pulse amplitude output is shown in Figure 1. Here,
use is made of the avalanche characteristic of transistors.\footnote{For a transistor to be operating in the avalanche mode, the collector is reversed biased. As the reverse bias is increased, current gradually increases until breakdown is reached. At breakdown the voltage suddenly decreases and the current is limited only by external circuitry.}

The circuit operates as follows. Initially, the supply voltage $V_{cc}$ is adjusted near breakdown, the transistor is cut off and the open circuited delay line is charged to $V_{cc}$. When a trigger pulse of amplitude large enough to carry the transistor into breakdown is applied, a voltage step appears at the collector. This voltage step
travels down the delay line, partially discharging it along the way. At the end of the open line, the voltage is reflected in phase due to the open circuit, and the reflected step voltage continues to discharge the line. If the input is terminated in $Z_o$, the characteristic impedance of the line, the impedance of the line suddenly becomes infinite, the current goes to zero, and no reflections occur. The transistor comes out of avalanche and the line charges through $R_c$ to $V_{cc}$. The circuit is then ready for the next trigger.

For no reflections to occur, the transistor resistance in the avalanche condition and the parallel resistance of $R_s$ and $R_1$ must equal the characteristic impedance. The resistance $R_s$ need be adjusted to match the transmission line to the load whenever replacement of the transistor becomes necessary.

The advantages of this type of pulse generator are fast response to the trigger and short rise and fall times. The disadvantage is of course, the inconvenience of needing to match the line by adjusting $R_s$ for every transistor. This is because terminal transistor characteristics even of the same type vary. Another variation to be expected is the pulse amplitude since the avalanche voltage after breakdown will depend on the particular transistor used.

The pulse generator considered above, while possessing certain advantages, lacks repeatability in that adjustments must be made for each time the transistor is replaced. A repeatable pulse
generator would be one in which an accurate waveshape output can be expected regardless of the transistor characteristic variations expected. Thus, if pulse generators are being produced on a large scale, there is a definite advantage in designing for repeatability.

This paper will outline some of the problems and considerations which must be taken into account when designing for repeatability.
THE BASIC CIRCUIT

The basic circuit with which this thesis will mainly be concerned is shown in Figure 2. The circuit can be separated into two stages. The first stage containing the delay line will act as the drive for the second stage containing the coil.

First-Stage Operation

An R-C coupled input was used to drive the transistor from full off to the active region.

The capacitor, \( C \), was used as a d. c. supply which allows \( T_1 \) to operate at a lower collector voltage and to prevent undesirable spikes which could occur from the power supply. The only requirement on \( C \) is that it be large enough to keep \( V_c \) relatively constant.

To obtain an expression for \( V_c \), the effect of the shorted delay line was disregarded since in this experiment a 60 ns one-way delay line was used. Hence the delay line can be treated as a short circuit.

Assuming \( C \) is large enough so that \( V_c \) can be considered constant, the approximate equivalent circuit is shown in Figure 3.

Since \( V_c \) is nearly constant, when \( i_b = 0 \) (transistor is cut off) equation (1) holds.

\[
i_1 = i_2 = \frac{V_{cc} - V_c}{R_3}
\]  

(1)
Figure 2. The basic circuitry of a pulse generator.
Figure 3. The approximate output equivalent circuit of the first stage.

With the transistor conducting, equation (2) can be written

\[ i_2 = i_1 - \beta i_b = \frac{V_{cc} - V_c}{R_3} - \beta i_b \]  

(2)

In the steady state, the net charge acquired by the capacitor must be zero. By using (1) and (2) and from the equation \( Q = \int idt \), equation (3) follows.

\[ \int_0^{t_1} \left( \frac{V_{cc} - V_c}{R_3} \beta i_b \right) dt = \int_{t_1}^{t_2} \frac{V_{cc} - V_c}{R_3} dt = 0 \]  

(3)

Where: \( t_1 \) = the output pulse width.

\( t_2 \) = the period of the input signal.

Integrating and solving for \( V_c \),

\[ V_c = V_{cc} - \frac{\beta i_b R_3 t_1}{t_2} \]  

(4)
This expression shows the controlling factors which determine $V_c$.

To see how a pulse from the first stage is obtained, consider the circuit shown in Figure 4(a). Initially, assume that the transistor is operating in the active region and all turn-on transients have died down. Hence the delay line is a short circuit with current $\beta i_b$ flowing.

At turn-off $i_b$ is zero and, referring to Figure 4(b), the voltage at the input to the line changes from zero to $V_1 = i_2 R_2$. Also from current continuity, $i_1 = -i_2$.

An equation relating the step voltage and current at the input is

$$\Delta v_i = R_o \Delta i$$

(5)

Where $R_o$ is the characteristic line impedance.

The current step $\Delta i$ at the input can be written

$$\Delta i = i_1 - \beta i_b$$

$$= -i_2 - \beta i_b$$

$$= \frac{V_1}{R_2} - \beta i_b$$

(6)

Where: $i_1 = \text{current traveling down the delay line at } t = 0^+$

(the transistor is cut off).

$\beta i_b = \text{current through the short circuit delay line at } t = 0^-$ (the transistor is conducting).
Figure 4(a). The schematic of the first stage.

Figure 4(b). The output approximate equivalent circuit.
Since the voltage at the input at $t = 0^-$ is zero, then $\Delta v_i = V_1$.

Substituting into equation (5),

$$V_1 = R_o \left( \frac{-V_1}{R_2} - \beta i_b \right)$$

Solving for $V_1$,

$$V_1 = \frac{-R_o \beta i_b}{1 + R_o/R_2}$$

This is the initial step voltage which starts down the transmission line. At the end of the line a voltage of opposite polarity is reflected back due to the short circuit load and discharge of the line begins.

If the input to the line is terminated in its characteristic impedance no reflections will occur. However a slight mismatch at the input with $R_2 > R_o$ would result in an overshoot which would aid turnoff of the following stage.

To determine the amount of overshoot, use was made of the reflection factor given by (3, p. 92)

$$\rho = \frac{R/R_o - 1}{R/R_o + 1}$$

Where: $R$ = the terminating impedance.

$R_o$ = the characteristic line impedance.

Delay lines have definite advantages in pulse forming. One is
that the delay time can be altered by adjusting the length of the line. Another consideration is that the pulse duration depends only on passive elements, and in this way adds stability to the system not present in other pulse generators which depend on active elements.

For convenience, component values of the first stage will not be considered at this time. Instead, attention will now be focused on the second stage.

**Second-Stage Operation**

The second stage is shown in Figure 5(a). $R_b$ and $C_2$ were used to couple from the output of the first stage.

The effect of loading on the output of the first stage is important to consider. At turn-on of $T_2$, the resistance seen by the delay line input is not $R_2$ alone but the parallel combination of $R_2$ and $R_4 + r_f$ where $r_f$ is the forward biased emitter junction resistance of $T_2$. The reason for including $R_4$ is to insure that the resistance seen at the input of the delay line is greater than $R_o$.

At turn-on the transistor is saturated due to the high impedance presented by the inductor, and the diode is reversed biased. The equivalent circuit, neglecting collector-emitter drop, is shown in Figure 5(b). It is required that this equivalent circuit holds for the pulse time. The differential equation for this circuit is
Figure 5(a). Schematic of the second stage.

Figure 5(b). Approximate equivalent circuit after turn-on.
\[ V_{cc} = L \frac{di}{dt} \]

Solving for \( i \) (initial conditions are zero)

\[ i = \frac{V_{cc}}{L} \cdot t \]  \hspace{1cm} (10)

Since \( L \) appears in the denominator a high enough value of inductance is required to insure that the transistor would be saturated for the pulse time.

A sketch of transistor characteristics along with the locus of operation taken when the load is inductive is shown in Figure 6.

At turn-on the collector voltages follows path 1 due to the infinite impedance presented by the inductance. Assuming that the inductance is high enough, the collector current increases linearly according to equation (10), the transistor remains in saturation, and hence path 2 is traversed. At the end of the pulse the transistor switches off. However current in an inductance cannot change instantaneously and as the current starts to decrease, the voltage across the coil falls and attempts to change polarity. As this happens the diode conducts and discharges the coil current. This completes the cycle as path 3 is taken at turn-off and path 4 is taken when the diode conducts.

To gain some insight on selecting a value of inductance, notice that for the transistor to remain in saturation (path 2 in Figure 6) the requirement that \( \beta i_b > I \) must hold. If the base drive is known
Figure 6. Transistor collector characteristics showing locus of operation for an inductive load.
then a safe value for $L$ can be chosen. The upper limit of $L$ is of course physical size since the stray capacitance effects would result in undesirable ringing.

**Second-Stage Design Values**

The input circuit in Figure 5(a) is a clamping circuit. In considering the input circuit, use was made of a clamping circuit theorem which states that (3, p. 270)

$$\frac{R_f}{R_r} = \frac{A_f}{A_r}$$  \hspace{1cm} (11)

Where: $R_f$ and $R_r$ are the forward and reverse resistances seen at $a$ in Figure 7(a).

$A_f$ and $A_r$ are the respective forward and reverse areas referred to in Figure 7(b).

This theorem locates the level at which the input is clamped.

From equation (11) and referring to Figure 7(b)

$$(R_4 + r_f)/R_b = V_1 \cdot \frac{t_p}{(V-V_1)} \cdot T$$  \hspace{1cm} (12)

Where: $r_f$ is the forward biased diode resistance.

$t_p \ll T$, and $R_4 + r_f \ll R_b$.

Solving for $V_1$

$$V_1 = (R_4 + r_f) \cdot T \cdot V / [R_b \cdot t_p + T \cdot (R_4 + r_f)]$$  \hspace{1cm} (13)

In this experiment a 50Ω delay line was used, and $R_4 = 510Ω$. 


was chosen in accordance with the requirement that $R_2 | (R_r + r_f) > R_o$ as discussed earlier.

![Figure 7(a). Equivalent input circuit of second stage.](image)

![Figure 7(b). Voltage appearing at a, showing the forward and reverse areas.](image)

It is now necessary to determine whether enough base drive is available to saturate the transistor. To do this some reasonable approximations will be made. First assume a 4 volt output pulse with a pulse width of 150 ns is available at the output of the first stage and that $R_4 + r_f = 600 \Omega$. For this example calculations are made with $R_b = 100 \, \Omega$. Also since a 100 k. c. rep rate is used, $T = 10 \, \mu s$.

Substituting these values into equation (13)
\[ V_1 = \frac{600 \cdot 10 \cdot 4}{10^5 \cdot 0.15 + 600 \cdot 10} \]
\[ = 1.14 \text{ volts.} \]

The base current is \( i_b = \frac{(1.14 - 0.6)}{0.6} = 0.9 \text{ ma.} \) If more base current is needed a smaller \( R_b \) is chosen.

In picking a value of inductance use was made of equation (10). A supply voltage of 20 volts was used. Also since a value of \( i \) at the end of the pulse can be chosen, \( i = 30 \text{ ma} \) was picked as a safe value for collector current.

Substituting and solving for \( L \)
\[ L = \frac{V_{cc} \cdot t}{i_p} \]
\[ = \frac{20 \cdot 150}{30} \]
\[ = 100 \mu \text{h.} \]

The maximum instantaneous power which can be anticipated is
\[ p_{\text{max}} = V_{\text{max}} \cdot i_{\text{max}} = 20 \cdot 30 = 0.6 \text{ watts.} \] This is below the maximum rating for a 2N3643 transistor.

Since relatively large base currents can be obtained by proper adjustment of \( R_b \), the requirement that \( \beta i_b > 30 \text{ ma} \) was easily met. In the example \( \beta > \frac{30}{0.9} = 33.3 \) is necessary for proper operation.

The coupling capacitor \( C_2 = 0.1 \mu \text{f} \) was chosen arbitrarily large so that tilt at the input is negligible.

Discussion of the Basic Circuit

The pulse generator discussed is much like the avalanche type
in that for a given transistor Tl, it is possible to adjust $R_b$ so that the output pulse width of a prescribed value is obtained. Adjustment is necessary because of the variation of $\beta$ which has a direct effect on the output amplitude of the first stage as shown by equation (8).

The reason for this pulse width variation can be explained by referring to Figure 8 which shows a current pulse to the base and the corresponding collector current for a saturated transistor. Notice that the collector current displays a delay time $t_d$, a rise time $t_r$, a storage time $t_s$, and a fall time $t_f$.

![Figure 8. Response of a transistor when operated in the saturated mode.](image)
The delay time and rise time are both functions of the amount of drive current, $i_b$. A higher drive would result in shortening the delay and rise times. However, such high current drives greatly increase the storage and fall times when trying to turn the transistor off.

The storage time varies from transistor to transistor even of the same type. Because of this, the pulse width will vary depending on the particular transistor characteristics. The following discussion will be aimed primarily at minimizing this effect. In other words, if for a given current drive the storage time remains relatively constant with replacement of transistor $T_2$, then the output pulse width will also remain relatively constant.

The advantage of active region operation of $T_1$ is that the effect of storage time delay is not present. This means that there will be an output pulse from the first stage as soon as the input switches to a lower voltage.

In the discussion of the first stage, it was noted that the magnitude of the current flowing through the transmission line was a function of $\beta$. The first step towards building a more repeatable pulse generator is to have a constant output from the first stage, and output which is not critically dependent upon the transistor characteristics.
DESIGN CONSIDERATIONS FOR REPEATABILITY

A simple and effective way of achieving a constant output from the first stage is to add a current limiting resistor in the collector circuit. Inclusion of the limiting resistor now makes it possible to choose component values for the first stage since $\beta$ need not be known. The first stage with the limiting resistor is shown in Figure 9(a).

$R_2$ was picked at 100 $\Omega$ so that a slight overshoot can be expected since $R_2/(R_4 + R_f) = 86\Omega$ which is greater than $R_o$.

The magnitude of the output voltage from the first stage was picked at 4 volts. The current necessary to produce this can be calculated from equation (8) with $\beta_i$ replaced by $I_{csat}$.

$$I_{csat} = \frac{-V_1 \cdot (1+R/R_o)}{R_o}$$

$$= \frac{4 \cdot (1+100/50)}{50}$$

$$= 120 \text{ ma}$$

A value for $R_3$ can now be selected by using equation (4).

Assume $V_c$ is chosen as 12 volts. Solving for $R_3$:

$$R_3 = \left( V_{cc} - V_c \right) \cdot \frac{t_2}{I_{csat} \cdot t_1}$$
Figure 9. (a) The first stage with limiting resistor $R_c$ with components used in parenthesis. (b) Input voltage $e_i$. (c) Output voltage $V_1$. (d) Expanded sketch of output voltage.
\[(20-12) \cdot \frac{10}{120} = 222 \Omega\]

Experimentally \(R_3 = 249 \Omega\) was used.

With \(I_{csat}\) and \(V_c\) now known, the required value for the limiting resistor \(R_c\) can be calculated.

\[R_c = \frac{V_c}{I_{csat}}\]
\[= \frac{12}{120}\]
\[= 9 \Omega\]

Experimentally \(R_c = 100 \Omega\) was used.

With the current-limiting resistor \(R_c\) known, \(R_1\) was determined experimentally. Assume \(C_1\) is large so that there is negligible tilt at the input of \(T_1\). \(R_1 = 680 \Omega\) was found to be adequate to saturate \(T_1\) for \(v_i = 2\) volts. \(C_1 = 0.1 \mu F\) was large enough for negligible tilt.

The reflection factor can be calculated from equation (9) where \(R = 86 \Omega\).

\[\rho = \frac{R/R_o - 1}{R/R_o + 1}\]
\[= \frac{86/50 - 1}{86/50 + 1}\]
\[= .26\]

The second pulse appearing at the output will be of opposite polarity and amplitude .26 of the first pulse. Similar reasoning can be used for further reflections if desired. A sketch of the waveform
is shown in Figure 10 with $V_1 = 4$ volts.

![Figure 10. First stage calculated output (compare with Figure 9(d)).](image)

The capacitor $C = 1.4 \mu f$ was chosen experimentally since all that is required is that it be large as explained previously.

The importance of selecting a value for $R_b$ will be considered next. In equation (13) it was seen that $V_1$, which locates the zero voltage point, depends upon the value of $R_b$. Increasing $R_b$ has the effect of decreasing the amount of drive to the second stage, while reducing $R_b$ increases the drive. Figure 11 describes what happens as $R_b$ is varied.

![Figure 11. Illustrating the effect of $R_b$ on drive to $T_2$. The dashed lines locate the zero voltage point.](image)

When a transistor is saturated, too high a current drive makes turn-off difficult and storage times differ with different transistors.
This makes the pulse width highly dependent on the particular transistor used. To make the pulse generator more repeatable it will be shown experimentally that picking $R_b$ as high as possible will make the pulse width more insensitive to changes in transistors.

Two factors place an upper limit on $R_b$. One is the deteriorating effect on waveshape as active region operation is approached. Another is that saturation and hence pulse width becomes dependent on the transistor $\beta$, resulting in large fluctuations in pulse width.

To show the extent which $R_b$ affects the shape and width of the output pulse, a pair of transistors were used and only $R_b$ varied. The output sketches in Figure 12 show the effect of input drive (controlled by $R_b$) to the second stage on the output waveform.

Selecting an $R_b$

In order to select an $R_b$, 30 transistors were used as the sample size for six different values of $R_b$. It is assumed that the distribution of the mean of the pulse widths is approximately normally distributed.

A 95% confidence interval test was made on the variances $\sigma^2$. Also point estimations for $\sigma^2$ were calculated. The results are given in Table 1.
Figure 12. Illustrating the effect of $R_b$ on pulse width and waveform.
Table 1. 95% interval estimation and point estimation of variance.

<table>
<thead>
<tr>
<th>( R_b )</th>
<th>Interval estimation of variance</th>
<th>Point estimation of variance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1K</td>
<td>( 130 &lt; \sigma^2 &lt; 371 )</td>
<td>205</td>
</tr>
<tr>
<td>27K</td>
<td>( 77 &lt; \sigma^2 &lt; 221 )</td>
<td>122</td>
</tr>
<tr>
<td>56K</td>
<td>( 21 &lt; \sigma^2 &lt; 61 )</td>
<td>33</td>
</tr>
<tr>
<td>100K</td>
<td>( 7 &lt; \sigma^2 &lt; 19 )</td>
<td>11</td>
</tr>
<tr>
<td>220K</td>
<td>( 20 &lt; \sigma^2 &lt; 58 )</td>
<td>32</td>
</tr>
<tr>
<td>820K</td>
<td>( 30 &lt; \sigma^2 &lt; 86 )</td>
<td>47</td>
</tr>
</tbody>
</table>

Since the variance is a measure of the spread of the distribution of the sample mean, the distribution with minimum variance would be best for repeatability of pulse width. Note that for relatively low values of \( R_b \) (high drive), the difficulty in turning off the transistor is reflected in large variations in pulse width (large variance). As \( R_b \) is increased it is seen that turn-off becomes more precise since the variance decreases. The optimum value for \( R_b \) appears to be at approximately \( R_b = 100K \). At higher values of \( R_b \) where the transistor is at or near active region operation, dependence on the transistor \( \beta \) on whether the transistor saturates or not, results in increased variations in pulse width. This is shown by the increase in the variance.

The graphs in Figure 13 were obtained from the data in Appendix II. The zero reference is the sample mean and the
Figure 13. Density graphs of the deviation of the pulse width from the sample mean for (a) high base drive, (b) optimum drive, and (c) low drive.
points represent the deviation of the pulse widths from the sample mean.
STORAGE-TIME REDUCTION OF THE FIRST STAGE

In nanosecond circuitry it may be necessary for an output pulse to occur with as little delay as possible in response to a trigger pulse. Assuming that the second stage is optimized attention is now focused on the first stage.

It is possible to combine the advantage of active region operation and the principle of current limiting by simply moving the collector resistor to the emitter. The circuit is shown in Figure 14.

![Figure 14. First-stage modification for reduction of storage time.](image)

**Operation**

After a pulse $v_i$ is applied, a current $i_e = v_i - v_{be}/R_e$ flows. Assuming $v_i < V_c$, the transistor is operating in the active region with current $i_c \neq i_e$ flowing through the shorted line.
At turn-off an output occurs nearly instantaneously because storage effects are not present in active region operation. Also the output pulse amplitude can be controlled by adjustment of either $v_i$ or $R_e$. The disadvantages in such operation are that a higher drive signal is necessary and a higher power dissipation rating is required of the transistor. Also the input voltage amplitude $v_i$ must be stable such that the collector current, and hence $e_o$ will also be stable.

Calculation of $R_e$

It was assumed that an input voltage of 7 volts was available. An output pulse voltage of about 4 volts was required as before.

From earlier considerations it follows that

$$R_e = \frac{v_i - v_{be}}{i_e}$$

$$= \frac{7 - .6}{0.12}$$

$$= 53\Omega$$

Where $v_{be} = .6$ volts for silicon transistors

Experimentally an $R_e$ of 52$\Omega$ was used.

The waveshapes observed were similar to those in Figure 8 and will not be repeated. The main difference was in the elimination of the storage-time delay. To determine the amount of
improvement, 20 transistors were tested in the original first stage and storage-time measurements taken. The storage time varied from 14 to 24 ns. The 20 transistors were also used to measure delay time of the second stage. Delay time varied from 16 to 18 ns.

It follows that the total delay introduced between the input of the first stage and the output of the second stage is about 30 to 42 ns. Active region operation of the first stage reduces this to about 16 to 18 ns.

The 20 transistors used to determine delay and storage times were considered adequate in determining the total delay between input and output signals, since statistical statements showing the improvement are not considered necessary.
CONCLUSION

While the basic circuit is a workable pulse generator, it is not practical when repeatability of pulse width is important. By altering the basic design it was shown that it is possible to design for repeatability when customized circuits become impractical.

It was also shown experimentally that it is possible to reduce the response time without affecting repeatability should it be necessary.

The 2N3643 transistor was used since it has a relatively high storage time, typically 120 ns at a collector current of 30 ma. The reason for wanting a transistor type having a high typical storage time is that individual transistor storage times deviate appreciably from the typical value. This is desirable for better resolution since a Tektronix 543 scope was used for pulse width measurements. The 2N3643 also fulfilled the $\beta$ requirement, having a minimum $\beta$ of 100.

If closer tolerance in pulse width variations is needed, a transistor having a shorter storage time could be used. The procedure for optimization used in this thesis would still hold.


APPENDIX A

METHOD USED FOR PULSE-WIDTH, STORAGE-TIME, AND DELAY-TIME MEASUREMENTS

Measurement of Pulse Width

Pulse-width measurements were made from the output of the second stage using an oscilloscope. The pulse width was measured at the half amplitude point of the output.

Measurement of Storage Time

To obtain storage-time measurements, a time reference must first be established. To do this the scope was set at negative external sync with the input of the first stage acting as the sync signal. For convenience time zero was chosen as shown in Figure 15.

![Figure 15](image)

Figure 15. Showing the time relation between input and output signal of the first stage for measuring storage time, $t_s$. 
Measurement of Delay Time

As in storage time measurements, a time reference need first be established. This time the output of the first stage was used as reference, with delay time measurements taken as shown in Figure 16.

Figure 16. Showing the time relation between input and output signal of the second stage for measuring delay time $t_d$. 
## DATA COLLECTED FROM PULSE-WIDTH MEASUREMENTS

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</table>

**Note:** Numbers are given in nanoseconds. Top row is the value of $R_i$. Left column indicates transistor number.
APPENDIX C

ESTIMATION OF VARIANCE

A confidence interval for the variance of a normal distribution is given as (4, p. 254)

\[ P \left[ \frac{\sum (x_i - \bar{x})^2}{b} < \sigma^2 < \frac{\sum (x_i - \bar{x})^2}{a} \right] = \gamma \]

Where: \( x_i \) = the sample value.
\( \bar{x} \) = the sample mean.
\( \gamma \) = the confidence coefficient.
\( a = \chi^2_{.975} \) and \( b = \chi^2_{.025} \) for \( \gamma = .95 \)

The Cumulative Chi-square Distribution table was used to find a and b for a 95% confidence interval with 29 degrees of freedom (sample size of 30).

The point estimation for the variance is

\[ \sigma^2 = \frac{1}{n - 1} \sum (x_i - \bar{x})^2 \]

Where \( n \) = the sample size.

The data in Appendix B was used in the calculations for variance with the results given in Table 1.