Electrical Transport Measurements Show Intrinsic Doping and Hysteresis in Graphene p-n Junction Devices

Garrett Plunkett

Department of Physics

Oregon State University

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Advisor: Dr. Matthew Graham

Department of Physics

Oregon State University

Abstract

Understanding the electrical transport properties of graphene provides a basis for determining its future as a potential semiconducting device that can be used for the next generation of transistors and photodetectors. Graphene p-n junctions can also function as field effect transistors, and thus are a logical starting point for I-V characterization. We perform transport measurements on dual topped gated p-n junctions with CVD grown graphene placed on a SiO_2/Si substrate. I-V curves show the Fermi level of graphene near the Dirac point can be directly tuned by applying voltage to the gate contact and reveal the location of the Dirac point at 3.5 kΩ is shifted -0.02 eV from its expected location at zero gate bias. This indicates that slight intrinsic p-doping is present in the graphene sample. P-doping has been well documented in graphene based devices, and is attributed to adsorption of H_2O or O_2 molecules at the graphene/SiO_2 interface. Using the measured transfer curves of source-drain current vs top gate voltage, the conductance of the graphene sample is plotted as a function of top gate voltage and the differential change in the linear portion of the curve is used to estimate a carrier mobility for the CVD graphene as 17,400 cm^2/Vs. The most commonly reported mobilities for CVD grown graphene on SiO_2 typically fall in the range of 500-10,000 cm^2/Vs, indicating that the device has high mobility. High mobility is attributed to the large grain graphene flakes present in the device, which allow more uniform conduction compared with small grain flakes. When gate sweeps are performed, hysteresis is observed in the p-n junctions, as has been reported in several previous studies on graphene based FETs. Hysteresis is caused by two mechanisms: charge trapping of adsorbates, such as H_2O and O_2, at the graphene/SiO_2 interface and an electrochemical redox reaction that occurs at the interface. The presence of two Dirac peaks in the hysteretic response is the result of the dual top-gate configuration of the device.

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1 Introduction

1.1. Graphene

1.1.1 Graphene Properties, Background, and Bonding

Since its discovery and initial characterization in 2004 by two physicists at the University of Manchester, Graphene has received significant attention in the scientific community due to its incredible material properties. Both physicists were awarded the 2010 Nobel Prize in Physics for "groundbreaking experiments regarding the 2-D material." [1] Graphene's unique properties include its electrical and thermal conductivities, both of which are among the highest of any known material, its mechanical strength, which is two orders of magnitude greater than steel, and its near transparency. [2] Graphene is one of several allotropes of carbon, different forms of the same element that all exist in the same physical state. It is one of many single layer materials, also called 2-D materials, which is currently being heavily researched for its potential as a semiconductor and in the optoelectronics industry. 2-D materials exist in the form of crystalline single layer thick "sheets" of atoms, and often have different optoelectronic properties than many-layered (bulk) materials of the same composition. Since it is effectively a "sheet" of carbon atoms one atom thick, monolayer graphene serves as the basis for understanding the electronic properties of all other allotropes of carbon. [3]. (Figure 1.1). Despite its hype as the semiconductor of the future, graphene exists in its unaltered form as a zero-bandgap semiconductor, and behaves as a semimetal. However, a bandgap can be created in graphene by altering its dimensionality, such as stacking single layer sheets of graphene on top of each other at an angle, or by isolating narrow ribbons of graphene, which can alter the band structure such that a bandgap is introduced [4]. Researchers have found that stacking two single layer sheets of graphene on top of each other to form a new material called bilayer graphene, can introduce a bandgap in the material if an appropriate bias voltage is supplied. Graphene's exceptional electrical conductivity has created much excitement over its potential to be used to create new, faster, and more durable transistors that may someday serve an alternative or replacement semiconducting material for silicon, although the absence of a bandgap limits it's applications [5]. Without a band gap, graphene has no "off" state necessary for creating a transistor. Due to these difficulties, graphene does not currently appear to be an imminent candidate to revolutionize the transistor industry, however, graphene transistors continue to be heavily researched. Graphene is currently used in a wide range of applications, from composites to sensors to photodetectors, and continues to capture the imagination of the scientific world for the novel physics it exhibits.

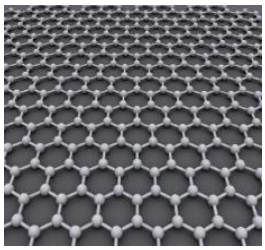

Figure 1.1: The crystal structure of monolayer graphene is a 2-D hexagonal lattice of carbon atoms arranged periodically. Its extraordinary properties led to the awarding of the 2010 Nobel Prize in Physics.

The bonding present in graphene and the periodic nature of its lattice structure gives rise to its unique electrical, mechanical and optical properties. Its molecular structure is formed from the hybridization of 1S and 2P orbitals. Carbon's four valence electrons result in the formation of four bonds between nearest neighbor atoms within the lattice structure of graphene. Atoms in the molecular plane form σ bonds between S and P_x orbitals and between S and P_y orbitals to form a total of three bonds. These bonds account for the mechanical strength of the material [3]. The atoms perpendicular to the molecular plane form a single π bond between P_z orbitals (Figure 1.2). It is the π band that serves as the basis for electron conduction within the material [3]. The π bonds in graphene are thus directly responsible for the unique electronic properties of graphene that originate from their band structure.

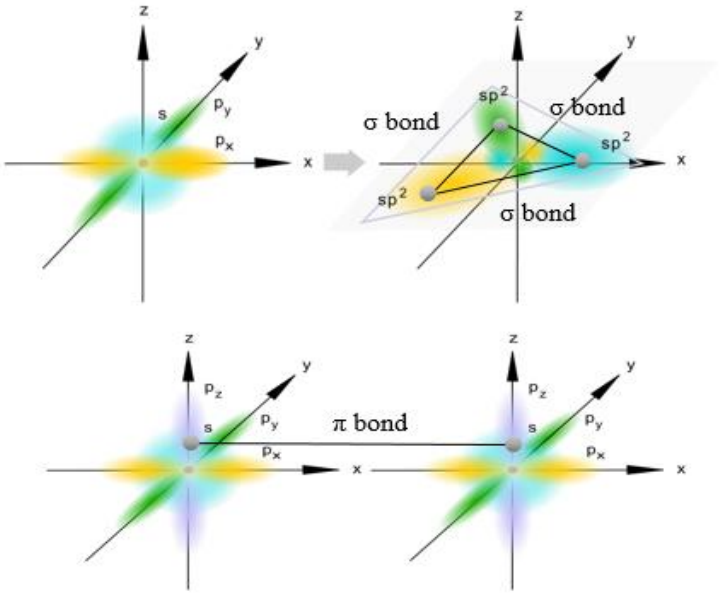

Figure 1.2: Bonding between carbon atoms in a graphene lattice. The central blue sphere represents the S orbital, with green and yellow lobes representing P orbitals. Carbon's four valence electrons in its S and P orbitals result in the formation of hybridized sp^2 orbitals. σ bonds form between hybridized orbitals, while a π bond forms between the hybridized p_z orbitals of two carbon atoms [6].

1.1.2 Graphene Band Structure

The band structure of a material serves as the basis for understanding its conductive properties since it describes the range of allowed energies for an electron within a solid. Calculations of the band structure of solid-state materials are made by determining the allowed wave functions for an electron in a periodic crystal lattice of atoms or molecules. The band structure of graphene is calculated using a tight binding model, which uses an approximate set of wave functions and the principle of superposition to find the allowed wave functions for its periodic lattice structure. Since the wave function of a single atom placed in a crystal lattice will overlap with the wave functions of adjacent atoms, the individual wave functions of single isolated atoms are not true eigenfunctions of the Hamiltonian for the crystal lattice. Therefore, the Hamiltonian of a single isolated atom in this model is given by

$$H(\boldsymbol{r}) = \sum_{\boldsymbol{R}} H(\boldsymbol{r} - \boldsymbol{R_n}) + \boldsymbol{\Delta} U(\boldsymbol{r}) \tag{1.1}$$

Where **r** denotes the position vector of an electron, $\boldsymbol{R_n}$ is the location of an atom within the crystal lattice, and $\boldsymbol{\Delta U(r)}$ is the corrected atomic potential.

The solution to the time independent Schrodinger equation for a single electron can be approximated as a linear combination of atomic orbitals (LCAO). Figure 1.3 shows a representation for a periodic potential in a crystal lattice structure.

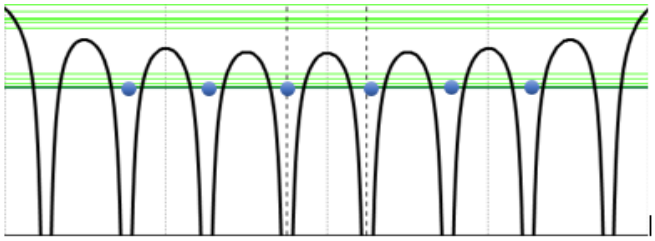

Figure 1.3: A approximate representation of the periodic potential in a crystal lattice containing many atoms in coulombic potential wells. The presence of many atoms in the lattice causes overlap to occur between nearest neighbor wave functions [7].

The wave functions for a crystal lattice are given by Bloch's theorem, which states that the wave function of an electron in a periodic potential, such as a crystal lattice, changes only by a phase factor when in undergoes a translational symmetry operation. The Bloch wave function is then

$$\psi_{n\boldsymbol{k}}(\boldsymbol{r}+\boldsymbol{R}) = e^{i\boldsymbol{k}\cdot\boldsymbol{R}}\psi(\boldsymbol{r}) \tag{1.2}$$

The corresponding molecular wave function for the crystal lattice is a superposition of the wave functions of each individual atom such that

$$\psi_{\boldsymbol{k}}(\boldsymbol{r}) = \frac{1}{\sqrt{N}}\sum_{\boldsymbol{R}} e^{i\boldsymbol{k}\cdot\boldsymbol{R}}\psi(\boldsymbol{r}-\boldsymbol{R}) \tag{1.3}$$

where N is the number of unit cells in the lattice. When equation 1.3 is applied to graphene, the result is given by equation 1.4. The plus and minus signs indicate the solutions for the conduction and valence bands. For each value of the wave vector, **k**, there are multiple solutions to the Schrodinger equation for each index, n, which accounts for different energy bands within the crystal lattice. The periodic nature of the crystal structure of graphene means that there are multiple possible energies for an electron with a given momentum. This relationship between the energy levels of an electron and its momentum is called a dispersion relation. Solving for the dispersion relation $E_n(\boldsymbol{k})$ results in a description of the allowed energies of an electron at a given momentum in the graphene lattice (See Appendix A for the full derivation).

$$E_n(\boldsymbol{k}) = \alpha \pm \beta\sqrt{1+4\cos\frac{k_x a}{2}\cos\frac{\sqrt{3}k_y a}{2}+4\cos^2\frac{k_x a}{2}} \tag{1.4}$$

When plotted, the dispersion relation of graphene indicates six points where the valence and conductance bands meet at the edge of the first Brillouin zone. The first Brillouin zone is a uniquely defined unit cell in reciprocal space, which exists as the Fourier Transform of real space.

In solid-state physics, the reciprocal space is a momentum ($\vec{K}$) space and the 1st Brillouin zone is shown in Figure 1.4.

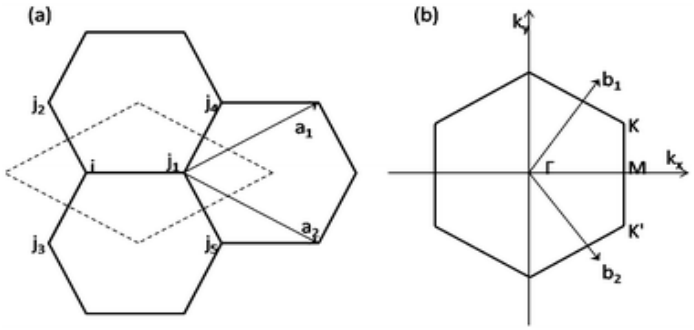

Figure 1.4: (A.) The primitive unit cell of graphene in real space. The dotted line indicates the unit cell. Point "i" represents the position of a carbon atom in the lattice, while points "j_n" represent neighbor atoms. **(B.)** The first Brillouin zone of graphene is its unit cell in reciprocal space. Points K and K' indicate the points where the valence and conduction bands meet [8].

The points where the valence and conduction bands in graphene meet are called Dirac points (Figure 1.5). These points exist at the K and K' symmetry points in the first Brillouin zone. These points directly relate to the Fermi level in graphene, which is defined as the highest energy level of an electron in thermodynamic equilibrium that has a 50% chance of being occupied at any given time. The probability that a quantum mechanical state with energy E_i, is occupied is given by the Fermi-Dirac distribution.

$$\langle n_i \rangle = \frac{1}{e^{(E_i - E_f)/k_B T} + 1} \tag{1.5}$$

Where E_f is the Fermi level of the material.

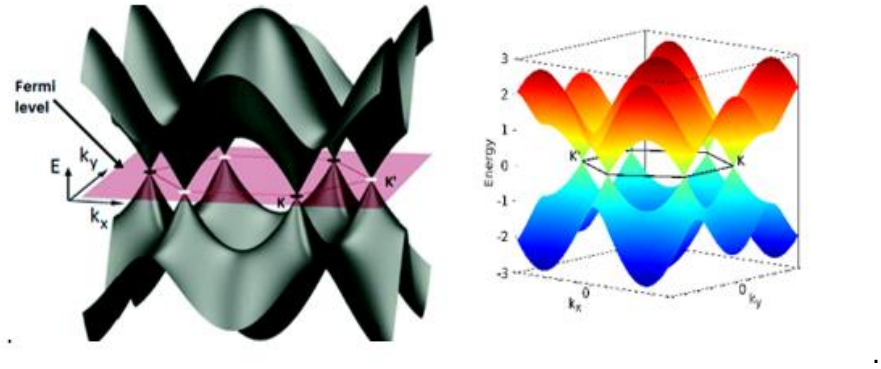

Figure 1.5: (A.) The 3-D electronic band structure of graphene in the first Brillouin zone. The purple plane defines the Fermi level in graphene that has not undergone doping. **(B.)** The valence and conduction bands of graphene. The lower blue band represents the valence band and the upper red band the conduction band. The K and K' points indicate the Dirac points, where the two bands touch. This defines graphene as a gapless semiconductor [9] [10].

1.2 Graphene Based Devices

1.2.1 Graphene p-n Junctions

Graphene p-n junctions exist on a silicon wafer, where a thin strip of graphene is placed between gold electrodes used to contact the device. A thin layer of SiO_2 is present on top of the silicon substrate, since pure silicon will naturally oxidize when exposed to air. Graphene p-n junctions function as a field effect transistor (FET) that has two gates: A top gate and back gate. The gates are electrically insulated, and control the conductivity of charge carriers in the depletion region when a voltage is applied across their terminals. The depletion region is an insulating region within a semiconductor material where all free charge carriers have been diffused away, or have been forced away by an electric field. In the absence of free charge carriers, no current will flow, and the only elements left in the depletion region are ionized donor or acceptor impurities. The density of charge carriers in the depletion region in turn effects the conductivity between the source and drain probes. Among many applications, graphene p-n junctions have garnered excitement in optoelectronics as a candidate for the creation of high speed photodetectors. Graphene is especially promising for photodetectors since its absorption spectrum covers the entire UV to far IR range, however, due to its low optical absorption, its optical response is limited. [11] Although this challenge exists for creating optoelectronic devices, currently graphene p-n junctions are the world's fastest photodetector with a flat photo-response in the visible to mid-IR spectrum [12]. In addition to their optoelectronic potential, p-n junctions are the building blocks for transistors. Thus, understanding the transport properties of graphene p-n junctions is essential to realizing the future of graphene transistors. The unique property of the p-n junctions investigated in this study is the presence of two top gate contacts, both of which connect to the channel.

1.2.2 Transport Measurements on Graphene p-n Junctions

Observing the Dirac points of graphene are of interest when characterizing the electrical properties of graphene based devices because they show the minimum point of conduction, which can be observed on an IV curve. Measurements of current, voltage, or resistance of semiconducting devices are typically referred to as transport measurements, since these quantities describe the movement of electrons within the materials present in a device. Transfer curves, plotting current (I) vs voltage (V) or resistance (R) vs voltage (V), provide the basis for understanding the flow of charge carriers through a device and for their potential extraction. This makes them crucial in determining a device's potential applications in industry or for novel research. In this study, transport curves are made on graphene p-n junction devices and used to calculate the resistance and conductance of graphene. Additionally, because the Fermi level in graphene is directly proportional to the gate voltage applied to the material (Appendix B), transport measurements allow for the Fermi level in graphene to be determined as a function of applied gate voltage. This is important in understanding the physics of any semi-conducting material, and in determining graphene's potential future as a semiconducting material.

1.2.3 Graphene Fabrication Methods and Carrier Mobility

If graphene is to become a major player in commercial electronics, it must be able to be fabricated in large quantities at high quality. One of the challenges currently facing the creation of high performance graphene electronics is optimizing the mobility of graphene grown with different fabrication methods. Currently, graphene is obtained using two methods: mechanical exfoliation and chemical vapor deposition. Mechanical exfoliation involves detaching graphene from a bulk

graphite crystal and using adhesive tape to transfer the graphene flake onto a silicon substrate [13]. Exfoliation is successful in preparing high quality graphene for use in electronic and optoelectronic devices, and is the fabrication method that achieves the highest carrier mobility [13]. Knowing the carrier mobility is highly useful because it provides a measure of how quickly electrons can move through the material. High mobility results in more efficient device performance, and thus a more promising future for use in commercial products or for further study in novel research. However, despite its merits, obtaining graphene via mechanical exfoliation does not allow for larger flakes of graphene to be easily transferred onto a substrate, and is thus not ideal for mass production [13].

A much more easily reproducible method of fabrication of graphene based devices is to grow graphene using chemical vapor deposition (CVD). The method of CVD involves exposing a substrate to gaseous compounds, which decompose on the surface and form a thin film. Typically, graphene is grown by exposing a Ni or CU film to methane gas at high temperature. The methane gas decomposes on the substrate, resulting in the formation of a graphene layer, which can then be transferred onto a silicon substrate [13] (Figure 1.6). CVD grown graphene allows the growth of graphene to be controlled, and large graphene films to be produced, making it an ideal fabrication method for industry. However, CVD grown graphene has consistently been shown to produce graphene flakes with of lower quality and lower carrier mobility than exfoliated graphene [13]. Optimizing the fabrication of CVD graphene is thus critical to graphene's future in commercially available electronic devices. Measuring the electron transport properties of graphene using I-V characterization allows the carrier mobility of graphene to be determined. The mobility of graphene in a p-n junction device can be extracted from the slope of a transfer curve plotting the conductance (1/R) of graphene as a function of top gate voltage. This is given by

$$\mu = \frac{\Delta G}{\Delta V_{TG}} \frac{L}{W} \frac{1}{C_{TG} e} \tag{1.6}$$

Where G is the conductance, V is the applied top gate voltage, L and W are the length and width of the conductive channel, C is the capacitance of the top gate, and e is the fundamental electron charge.

Using this technique, this study provides an estimate for the carrier mobility in CVD grown graphene used in graphene p-n junction devices.

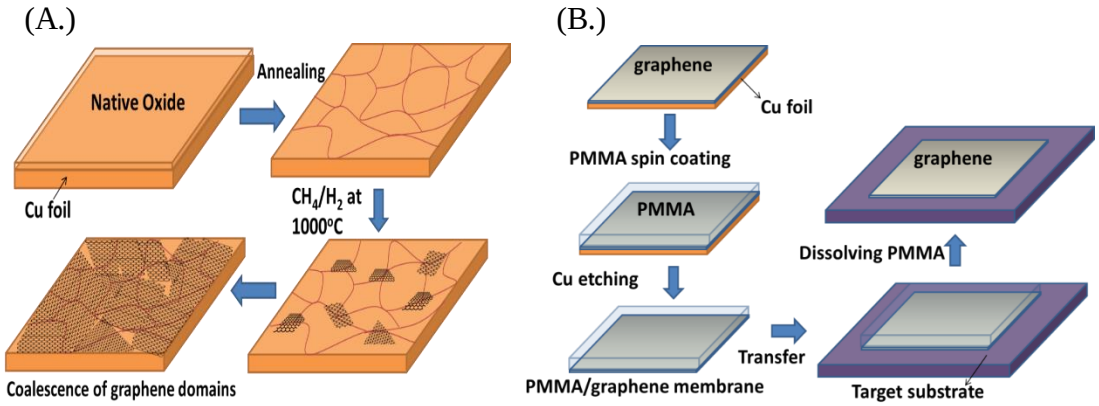

Figure 1.6: (A.) CVD growth of graphene on CU foil. A thin film of graphene is creating by exposing the foil to methane gas at high temperature**. (B.)** Transfer of CVD graphene onto a silicon substrate using PMMA.

2 Methods

2.1 Transport Measurement Station

2.1.1 Station Set-Up

Performing transport measurements on graphene p-n junctions requires the assembly of a transport station capable of measuring I-V curves on either common or novel devices. To create a working station, coaxial RF probes must be properly wired to micromanipulators, which are connected to a power supply and DAQ board. The analog signal input to the DAQ is then converted to a digital signal that can be measured by a computer using LabView software (Figure 2.1). Because chips containing p-n junctions are on the order of 1cm^2, with a single chip containing up to 100 individual devices, optical microscopy must be used to view the chips when making electrical contact with devices.

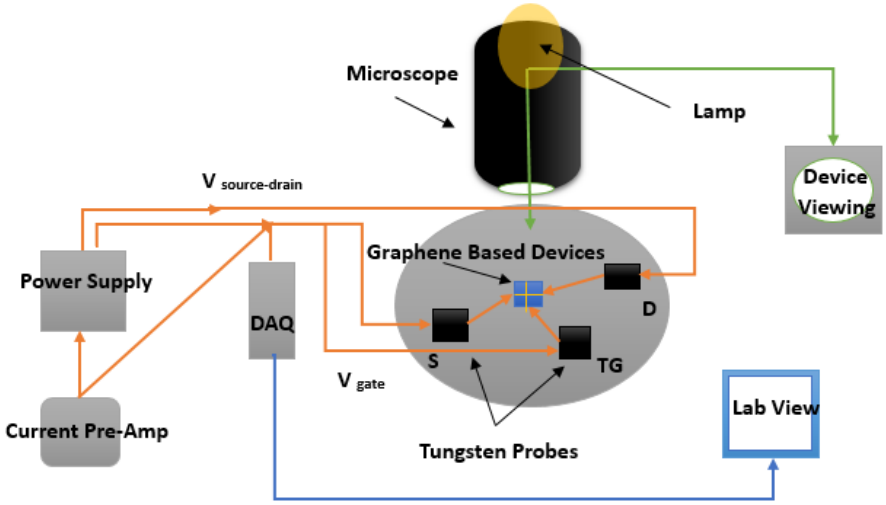

Figure 2.1: The transport station used to make measurements on graphene p-n junction devices. Green arrows represent visible light from a lamp, orange arrows an analog current/voltage signal from tungsten probes, and blue arrows a digital signal read by LabView, which generates IV curves. S, D, and TG denote the source, drain, and top gate contacts.

2.1.2 Station Operation

A power supply capable of supplying 30 V is used to provide the voltage which will power the circuit. The voltage signal from the supply is then sent to a DAQ board, where the analog signal from the power supply is converted to a digital signal that is read by a computer. The digital signal output from the DAQ is detected and measured in a LabView program called MeasureIt, which allows users to fine tune the bias voltage applied to the device when tungsten electrical probes are placed on either source-drain and/or gate electrodes of the device. These probes are attached to micromanipulators which have degrees of freedom in both the (XY) and Z directions. This allows tungsten probe to be extended underneath the microscope objective, lowered onto the sample, and then centered on an individual p-n junction device before electrical contact is established. To optically view sample chips, a lamp emitting wavelengths in the visible spectrum is coupled into an Olympus microscope, which is used to view and magnify the chips containing graphene p-n junction devices. Optical microscopy is necessary since the chip containing devices is on the order of 1cm^2, with source-drain electrode spacing of each device around 20 microns.

2.2 Graphene p-n Junctions

2.2.1 Fabrication

Single-layer graphene on copper foil is grown using Chemical Vapor Deposition (CVD). Raman spectroscopy is used to confirm the growth of large-grain single-layer graphene is of high quality. Graphene was transferred using the lift-off technique onto a 300 nm SiO_2 layer grown on top of a silicon wafer which serves as the global back-gate. The large-grain growth graphene is divided into 30×50 μm stripes using photolithography followed by oxygen plasma etching. Electrode pads of titanium/gold in a ratio of 3nm/150nm are deposited along graphene stripes with variable source-drain distances of 10 or 20 μm. A good dielectric separation with the top gate is achieved with 10 nm of SiO_2 by electron beam deposition, followed by HfO_2 atomic layer deposition. An optically translucent top gate of titanium/gold in a ratio of 2nm/20nm is deposited along the center of the source-drain gap with a width of 6 μm [14]. Figure 2.2 shows a schematic of the p-n junction devices.

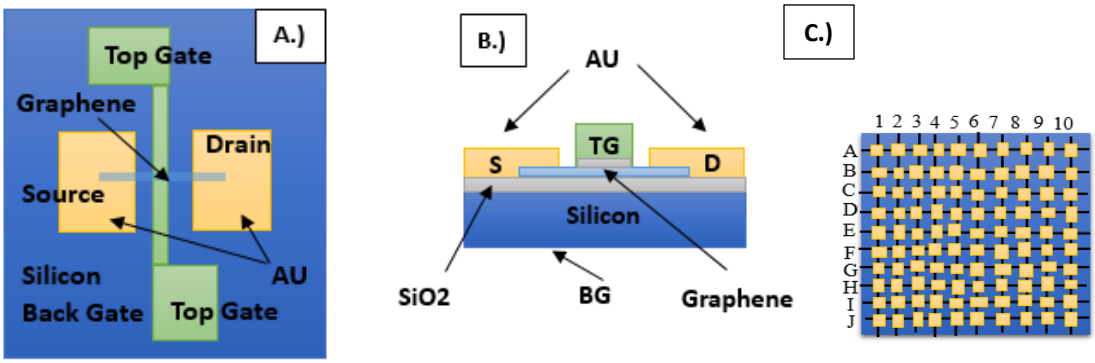

Figure 2.2: **(A.)** Top view of a graphene p-n junction device**. (B.)** Side view of a graphene p-n junction device. A single layer of graphene exists over silicon substrate between source-drain electrodes, which are plated in gold. A thin layer of SiO_2 is present on top of a silicon wafer. Two translucent top gates are insulated from the conductive channel with a small dielectric layer of SiO_2. **(C.)** The grid lay-out of the chip containing p-n junction devices. Each gold box represents an individual p-n junction device.

2.2.2 Identification of Working Devices

Before transport measurements can be made, working devices must be identified on the chip being investigated. To do this, a list is made of potential working devices on a single chip by using optical microscopy at 10X magnification to view devices and determine whether a graphene sample is present between the source and drain electrodes on a device. In practice, this can be difficult to determine because graphene is nearly transparent to visible light, and because the strip of graphene present between electrodes is only tens of microns in width. However, despite the challenges of optically viewing the graphene samples, this procedure does allow the number of grid locations containing potential working devices to be greatly reduced to a manageable number for testing. Of equal importance, imaging the chip before testing individual devices shows which devices are damaged, and are thus unlikely to give a conductive response from the graphene. The chip in this study contains vertical grid coordinates A-H and horizontal coordinates 1-10, and thus contains a total of 100 devices. In total, optical microscopy showed 30 individual devices that appeared to have graphene present. The most pristine devices were then selected for testing. After placing the chip under the microscope and viewing at 4X-10X magnification, two tungsten probes are used to contact the source and drain electrodes of a device (Figure 2.3). If a graphene sample is present between the

source and drain electrodes, current will be generated between the them, which is measured as a voltage in LabView. If no sample is present, the voltage signal seen in LabView will only show noise.

The resistance of the graphene sample is the slope of the I-V curve, which should follow a linear relationship as governed by Ohm's Law such that $R_{sd} = V_{sd}/I_{sd}$.

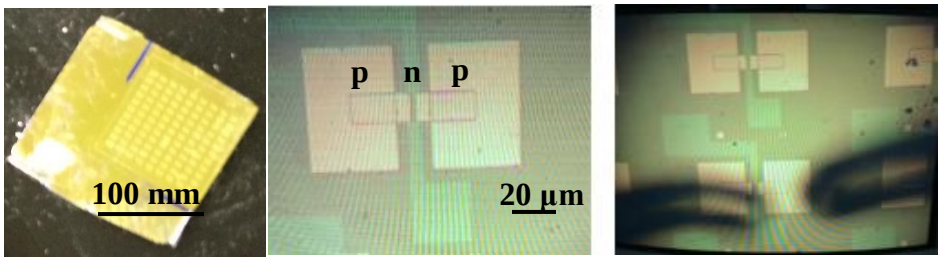

Figure 2.3 (A.): The chip containing 100 graphene p-n junction devices. **(B.)** An individual graphene p-n-p junction device. Source-Drain electrodes are visible as gold colored pads. Light green pads the top gate terminals of the device. **(C.):** Tungsten probes visible under 10X optical magnification.

2.2.3 Transport Measurements

After working devices have been identified on the sample, an additional probe is wired to connect to the power supply, sent through the DAQ, and measured in LabView. This probe is then connected to either the top or back gate of a device. To make conductive measurements that will show the band structure of graphene, at least three probes must be connected to the device, since changing the source-drain bias will not change the Fermi level of graphene. These probes must be very carefully extended across the microscope stage using micromanipulators. While viewing the chip on a monitor screen, the micromanipulators are used to lower the tungsten probe tips onto the electrodes of a device until they make contact. Although this is easily visible by the disappearance of the tip's shadow on screen, care must be taken to make gentle contact with the gold electrodes so that the device is not physically damaged (Figure 2.4). Additionally, when the three probes are simultaneously connected, care must be taken to not touch probe tips when positioning them on the source, drain, and gate electrodes of the device, since the tungsten probe tips are very delicate (1 micron in width). Once contact is made with a device, a constant source-drain bias is applied to the gold electrodes. A sweep measurement of the top gate voltage is then made and plotted as a function of the current across the source-drain electrodes. If the gate voltage is swept at the right source-drain bias, the Dirac point is observed as the minimum on a plot of source-drain current vs gate voltage or the maximum on a plot of the resistance across the source-drain electrodes as a function gate voltage. Transport measurements are made at room temperature (approximately 300 K) and not made in vacuum, thus devices are exposed to ambient conditions during measurements.

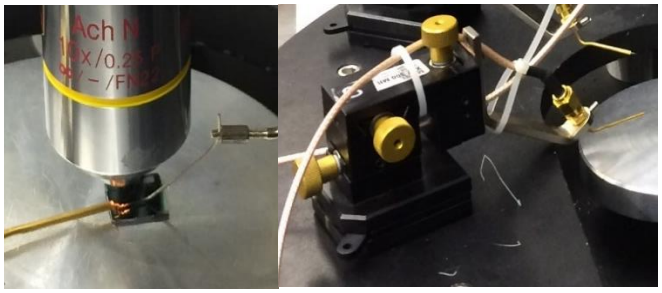

Figure 2.4: (A.) The chip containing graphene p-n junctions underneath a microscope objective. A coaxial RF probe is visible on the right of the microscope objective. **(B.)** A micromanipulator used to position coaxial RF probes onto graphene p-n junction devices. Gold knobs control motion in the X, Y, and Z directions.

3 Results

3.1 Graphene p-n Junctions

3.1.1 Identification of Working Devices

IV curves are taken to determine whether the constructed transport station is working properly. These measurements are then used to determine the grid location of connected devices on the chip containing graphene p-n junctions. Figure 3.1 shows an IV curve taken at grid location E7, which is used to determine whether good electrical contact is established with the device. The two terminal I-V curve is approximately linear with a resistance of 2.8 kΩ, which indicates a working device is present at this grid location. The source-drain voltage applied to the device is swept from +10/-10 mV during this measurement. Connected devices are expected to have resistances on the order of several kΩ, while an unconnected device would have much higher resistance- on the order of MΩ or greater.

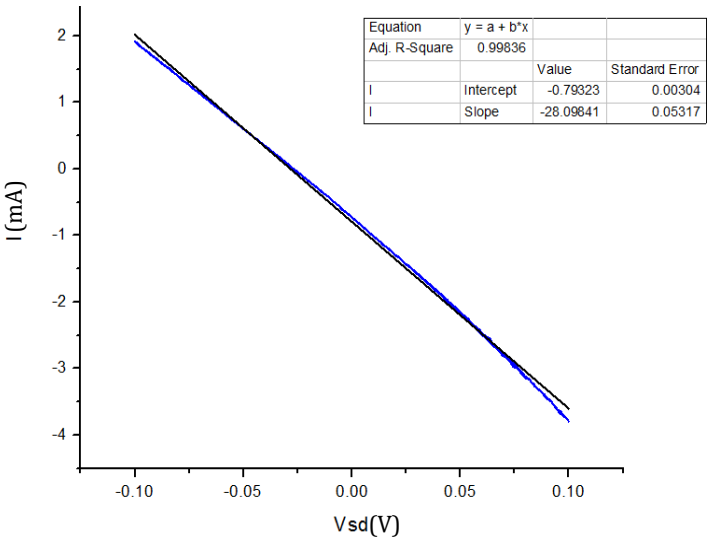

Figure 3.1: (A.): An IV curve taken on a graphene p-n junction device showing the current across the source-drain terminals as a function of the voltage applied to the device. The black line shows the linear fit.

3.1.2 Transport Measurements Near the Dirac point

After devices with good electrical connection are identified, transport measurements are made on working p-n junction devices. An additional tungsten probe is connected to the top gate electrode so that the conductance of graphene can be measured from a 3-terminal IV curve of source-drain current vs top gate voltage. The resulting gate voltage sweeps show the Dirac point in graphene in the range +/- 1 V. The gate voltage range is selected after examining previous papers and studying the theory of the material. Voltage sweeps are performed over a small range so that the Dirac point can be observed in detail. From the I-V curves of source-drain voltage vs gate voltage taken on devices E7 and G5, the resistance and conductance of the graphene sample are extracted. Figure 3.2 shows the transfer curve on device G5 both as resistance as a function of gate voltage, and its inverse, conductance. The Dirac point is located at 3.5 kΩ and 30 mS, respectively. Note that the unit of conductance is given in Siemens (S), the definition of which is simply inverse Ohms.

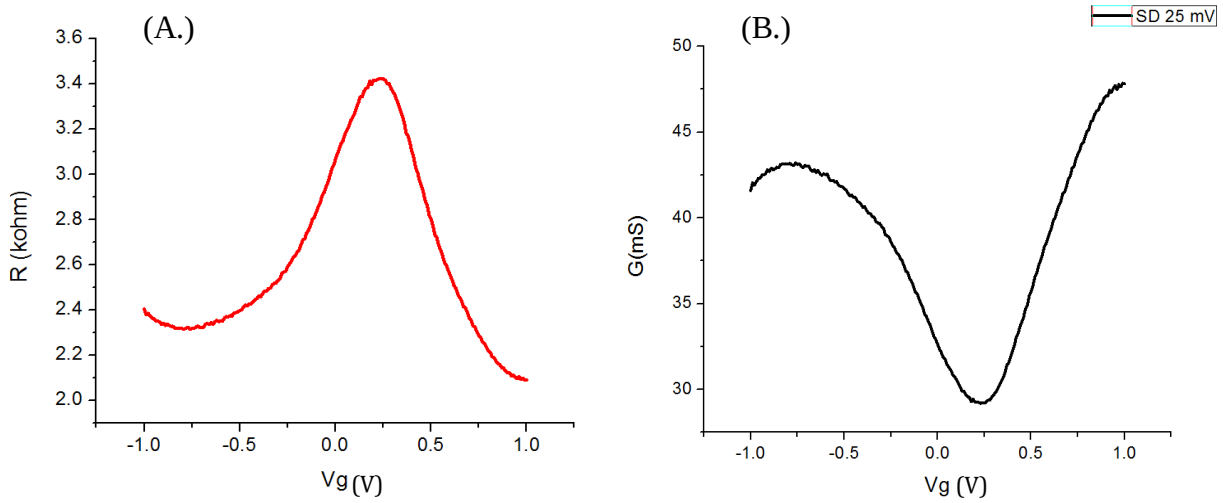

Figure 3.2: Transfer curves of graphene p-n junction device G5 at a constant source-drain bias of 25 mV. **(A.):** Resistance as a function of gate voltage. The Dirac point is the peak resistance value. **(B.):** Conductance plotted as a function gate voltage. The Dirac point is the minimum value.

These transfer curves indicate that the conductance of the graphene p-n junction is dependent upon the gate voltage applied to the device because sweeping the gate voltage tunes the Fermi level of the graphene sample. The Fermi level is calculated from the applied gate voltage using the relation

$$E_F(V_g) = \hbar V_F \sqrt{\frac{\pi \varepsilon_r \varepsilon_0 V_g}{\rho d}} \tag{3.1}$$

Where ε_r *and* ε_0 are the permittivity of vacuum and SiO_2, ρ is the charge density, d is the thickness of SiO_2, and V_g is the applied voltage to the gate terminal (Appendix B). Figure 3.3 shows the results predicted for the change in the Fermi level of graphene as a function of gate voltage and that extracted from transport measurements made on device G5.

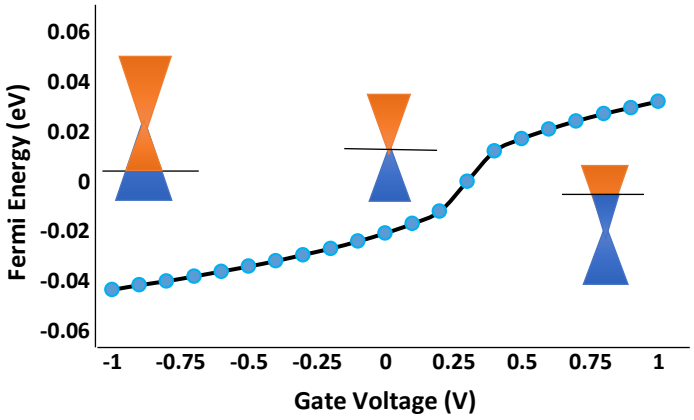

Figure 3.3: The change in the Fermi level of graphene with applied gate voltage. The black curve represents the location of the Fermi energy expected based upon the location of the Dirac point in graphene, while blue dots show the Fermi level calculated for p-n junction device G5. The location of the Fermi level near the Dirac cone is shown as a black line, and the valence and conduction bands are shown as blue/orange.

Because the dispersion relation of graphene is linear near the Dirac point, the theoretical density of states curve can be extracted from the Fermi level and calculated using equation 3.2

$$g(E) = \frac{2E_f}{\pi(\hbar V_F)^2} \tag{3.2}$$

Using this relation, the known value of the Fermi level near the Dirac point is used to plot the density of states as a function of the gate voltage applied to the graphene (Figure 3.4). Since the density of states describes the number of electronic states per energy level that may be occupied, this is analogous to observing the conductive response of graphene visible on an I-V curve.

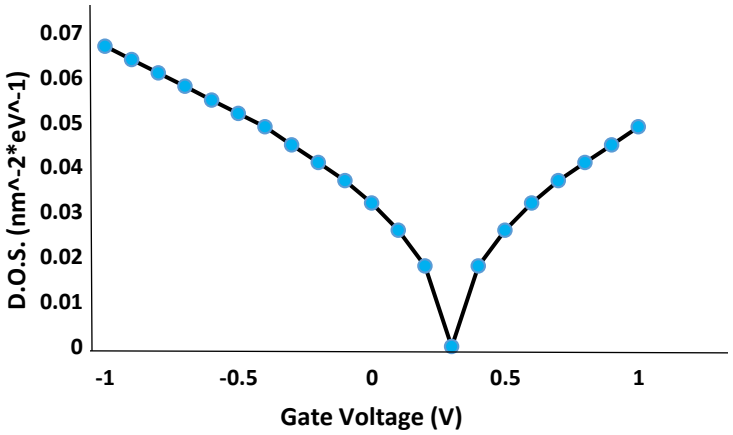

Figure 3.4: The density of states in graphene as a function of gate voltage. The black curve represents the prediction based upon the observation of the Dirac point, while the blue dots show the calculation for the density of states for graphene p-n junction device G5.

3.1.3 Mobility Estimation for Graphene p-n Junction devices

The mobility of the p-n junction devices can be estimated using equation 1.6. The differential change in conductance as a function of top gate voltage is estimated using the linear portion of the curve

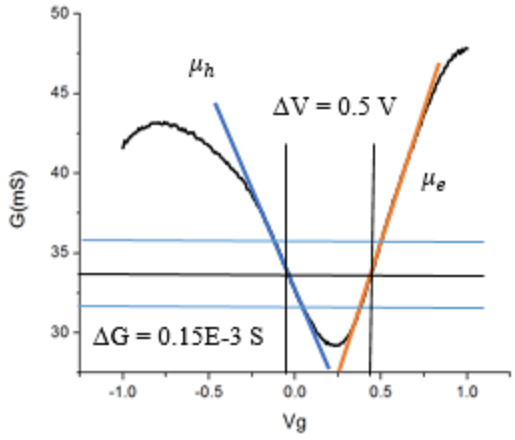

Figure 3.5: Mobility calulation of the graphene p-n junction device using the linear change $\frac{\Delta G}{\Delta V_{TG}}$. Blue and orange arrows indicate electron and hole mobility. The estimated mobility for the CVD graphene is the average of the electron and hole mobilities.

By using the I_{sd} vs V_g curve, the differential change in top gate voltage is estimated as the full width half maximum in the linear portion of the curve, and the change in conductance is found by taking the difference between the maximum and FWHM values coresponding to the linear portion of the curve.

To find the mobility, the capacitance of the top gate electrode must be calculated. Using the definition of capacitance, where A is the area of the eletrode, d is the thickness, and ε is the permeabilty times the dielectric constant of SiO_2 such that $\varepsilon = \varepsilon_0\varepsilon_r = 3.9\varepsilon_0$

$$C = \varepsilon\frac{A}{d} \tag{3.3}$$

Since capacitance is a measure of the top gate's ability to store electrical charge, the total charge present on the electrode is

$$Q = CV = \varepsilon\frac{A}{d} \tag{3.4}$$

However, the total charge is the carrier density, N, multiplied by the fundamental charge of an electron, e. Rewriting 3.4 and dividing by the area gives

$$\frac{Ne}{A} = \frac{\varepsilon}{d}V \tag{3.5}$$

We now defne N/A as the carrier concentration such that

$$C_{TG} = \Delta ne \tag{3.6}$$

Where the carrier concentration per unit area is

$$\Delta ne = C_{TG}\Delta V_{TG} \tag{3.7}$$

The conductivity of the graphene relates to the conductance obtained from transfer curves by

$$\sigma = G\frac{L}{W} = ne\mu \tag{3.8}$$

Where L and W are the length/width of the channel, and μ is the carrier mobility. Rearranging gives

$$\mu = \frac{\sigma}{ne} = \frac{\Delta\sigma}{\Delta ne} \tag{3.9}$$

We now take the differential of the conductivity with respect to carrier concentration, which can directly related to the conductance curve by

$$\mu = \frac{\Delta G}{\Delta ne}\frac{L}{W} \tag{3.10}$$

Finally, plugging in values gives an estimated peak mobility in the linear regime

$$\mu = \frac{\Delta G}{C_{TG}e\Delta V_{TG}}\frac{L}{W} = \frac{1.5\ mS}{(1.77 * 10^{-7}\frac{C}{cm^2})(0.5\ V)}\frac{6\ \mu m}{30\ \mu m} = 17{,}400\ cm^2/(V * S) \tag{3.11}$$

From the carrier mobility, we can also quantatively determine the values for the contact and channel resistances near the Dirac point. The carrier concentration at the Diract point is given by

$$n = \frac{C_{gate}V_{Dirac}}{e} = \frac{\left(1.72\frac{C}{cm^2}\right)(0.2\ V)}{(1.602 * 10^{-19}C)} = 3.23 * 10^{10}\ cm^{-2} \quad (3.12)$$

The total resistance at the Dirac point is the sum of the channel and contact resistances such that

$$R_{total} = R_{channel} + R_{contact} = 3.5\ k\Omega \quad (3.13)$$

Where the resistance value above is obtained from the transfer curve R vs V_g. The channel resistance is

$$R_{channel} = \frac{W}{L}\frac{1}{\sqrt{n_{impurities}^2 + n^2 e\mu}} = \frac{W}{L}\frac{1}{ne\mu} = \frac{6}{30}\frac{1}{ne\mu} = 2.2\ k\Omega \quad (3.14)$$

Where we have simplifed the initial expression because the location of the Dirac point shows the presence of only a small number of impurities. We can now determine the contact resistance as

$$R_{contact} = R_{total} + R_{channel} = 3.5\ \text{k}\Omega - 2.2\ \text{k}\Omega = 1.3\ \text{k}\Omega$$

3.1.4 Hysteresis in Graphene p-n Junctions

A strong hysteresis is observed in I-V curves when the gate voltage is scanned over the same range repeatedly, thus multiple peaks are observed on a plot of resistance vs gate voltage. Hysteresis is present at source-drain bias voltages of both 10 and 25 mV. When scanned over a single forward and reverse sweep, the location of the Dirac point appears to shift, indicating that the direction of applied voltage changes the location of the Dirac point (Figure 3.4).

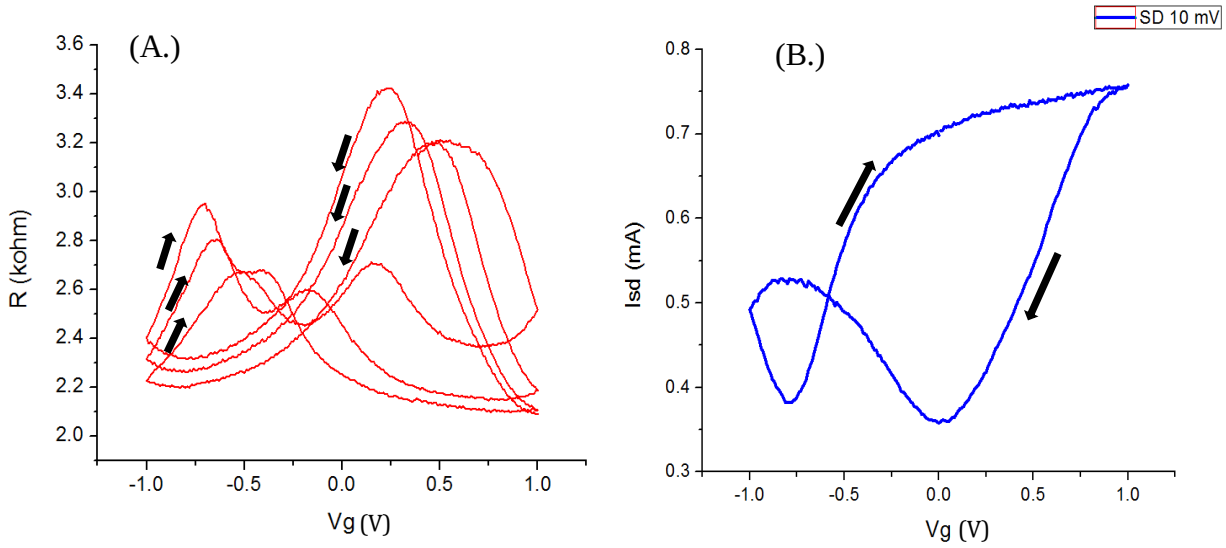

Figure 3.6: (A.) Hysteresis in graphene p-n junctions occurs in transfer curves when the gate voltage is swept multiple times over the same range with a 25-mV source-drain bias. When this occurs, it results in a shift of the Dirac point on the I-V curve. **(B.)** Forward and reverse sweeps on device E7 show a shift in the Dirac Point based upon the direction of applied voltage. Black arrows indicate the direction of the hysteresis loop.

4 Discussion

4.1 Graphene p-n Junctions

4.1.1 Identification of Working Devices

Electrical contact was successfully made on p-n junction devices E7 and G5 using tungsten probes. The linear relationship between source-drain voltage and current is expected, since the device operates as a FET, and confirms the Ohmic nature of the contacts. The relationship between source-drain current and gate voltage is also characteristic of the response expected, with the current increasing non-linearly with applied gate voltage.

4.1.2 Transport Measurements Near the Dirac point

Transport measurements made on graphene p-n junctions devices show the band structure of graphene near the Dirac point. Specifically, resistance and conductance plots show the electronic properties of graphene as charge carriers are excited from the top of the valence band into the conduction band. As the gate voltage is swept from negative to positive values, the Fermi level moves from its initial location between the valence and conduction bands, into the conduction band. (Figure 4.1) Thus, transport measurements near the Dirac point provide a map of the conduction band of graphene. This can also be seen in the plots of the Fermi level and density of states vs gate voltage. The density of states, is theoretically zero at the Fermi level in pristine graphene, since the dispersion relation at the Dirac point is a singularity in k-space. However, transport measurements reveal that the location of the Dirac point is not at unbiased gate voltage, but is instead shifted to a value of +0.3 V. The +0.3 gate-voltage-shift of the Dirac point from its expected location at zero gate voltage corresponds to a shift in the minimum in the density of states in the graphene sample, and thus a shift in the Fermi level of 0.02 eV. The shifting of the Dirac point also shows the presence of a small number of impurities in the material, which may have occurred during the fabrication process and from the devices exposure to air. This effectively means that the graphene sample is intrinsically slightly p-doped.

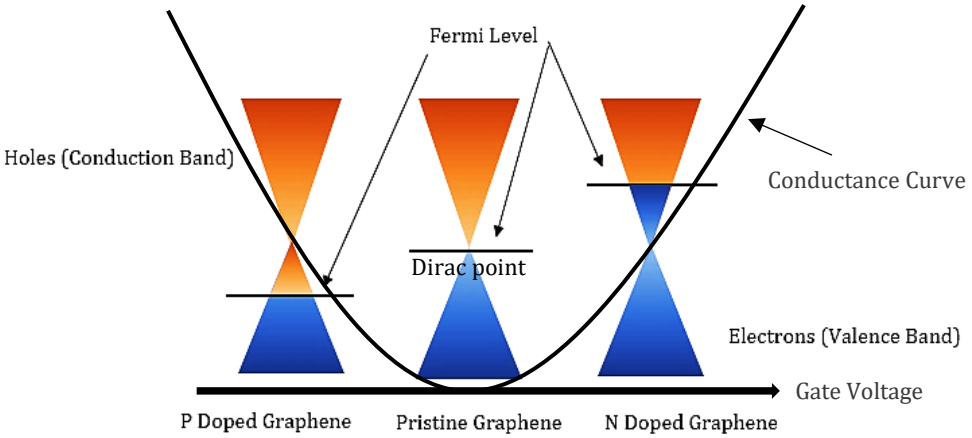

Figure 4.1: Change in conduction of graphene near the Dirac point with gate voltage. As the gate voltage is increased from negative to positive bias, the Fermi level in the graphene sample is increased and carriers are excited into the conduction band. Although increasing gate voltage results in n-doped graphene, charge trapping at the graphene/SiO_2 interface results in "clean" graphene being slightly p-doped at the Dirac point.

Many studies have previously shown that adsorption of molecules such as H_2O, CO_2, and O_2 at the graphene/SiO_2 interface during the fabrication process or from exposure to air lead to unintentional p-doping of graphene [15] [17] (Figure 4.2). Electron transfer from graphene to the adsorbed molecule is facilitated through the graphene/SiO_2 interface, producing p-doped graphene through the formation of weak C-O bonds between graphene and the SiO_2 substrate. These bonds enable p-type conductivity in graphene at unbiased gate voltage, which increases the hole concentration in graphene, and thus shifts the Dirac point to positive gate voltages and a negative Fermi level. The fabrication of these devices using PMMA, which is an insulator, has been previously shown to prevent unwanted adsorption so that the Dirac point can be observed within a narrow gate voltage sweep [15].

In this study, the Dirac point is found very near zero applied gate voltage, indicating that additional unintentional doping beyond that incurred during the fabrication process or from exposure to air is not present in the graphene p-n junctions. The lack of strong p-doping present in the graphene sample is unexpected in many graphene based devices, considering the difficulty in removing p dopants. Often the unintentional p-doping of graphene is strong enough that it results in a shift of the Dirac point to gate voltages outside of a 30 or even 60 V sweep [17]. One possible reason may be due to the use of electron-beam deposition (EB-deposition or irradiation) on the SiO_2 during the fabrication process. Previous studies have found that using EB irradiation during or after fabrication can result in a shift of the Dirac point towards zero gate voltage. This suggests that EB- irradiation aids in cleaning charged impurities from the surface of the graphene sample, or that it neutralizes charged impurities, both of which would result in a shift in the Dirac point towards the value of V_g = 0 V predicted for pristine graphene. [18]. Irradiation generates electron-hole pairs, which can become trapped at the SiO_2/Si interface. The trapped charge creates an additional positive bias that attracts electrons in the graphene sample, resulting in a shift of the Dirac point from p-doped to effectively pristine. Performing electron beam irradiation enough times on graphene after fabrication has even been shown to shift the Dirac point to negative gate voltage, resulting in strong n-doping [18]. Measurements on device G5 suggest this is may be one reason why the graphene present in these p-n junction devices is so clean.

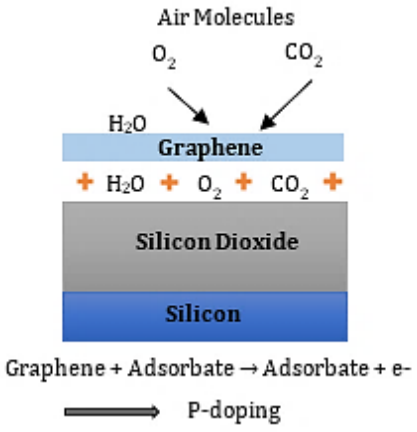

Figure 4.2: Adsorption of air or water molecules at the graphene/SiO_2 interface leads to intrinsic p-doping of graphene in p-n junction devices.

Resistance and conductance values obtained from figure 3.2 shows the total resistance measured. Contact resistance created by the coaxial RF probes touching the gold electrodes placed over the graphene sample is quantitatively estimated to be 1.3 kΩ based on the calculation of the channel resistance. This value is higher than previously reported values, which estimate a contact resistance of around 500 Ω [18]. In general, the exact resistance values observed at the Dirac point in graphene are dependent upon both the material of the electrodes (Ti, Au, Pd, etc), the substrate on which the graphene sample is placed (SiO_2, BN, etc) and most strongly upon the temperature of the sample. The resistance of graphene grown on SiC measured at 2K compared with 300 K, for example, has been found to increase from 12 kΩ to 239 kΩ [21]. Previous studies of the transfer characteristics of graphene on SiO_2 have typically shown resistance values at the Dirac point between 2-10 kΩ, with most showing values around 5 kΩ [15]. Thus, the resistance peaks at the Dirac point are in excellent agreement with previous literature values. Contact resistance of 100 Ω*μm has been reported as desirable for transport measurements made on graphene, although larger contact resistances have been reported [18]. A previous study of transport measurements on graphene FET's with Nb/Au electrodes found the Dirac Peak to be located at 40 kΩ, with a contact resistance of 5 kΩ. One possible explanation for the high contact resistance found is tensile induced strain. Previous studies have found that strains over 3% can increase the total resistance of graphene on a silicon substrate from 5 kΩ to over 25 kΩ[19]. While the tensile strain has not been quantitatively accounted for, the observation of the Au metal peeling off the source-drain electrodes during measurements is a strong indication that stress was being applied to the electrodes and transferred to the graphene present underneath. These same observations were made in the study which introduced a 3% strain on their device electrodes.

4.1.3 Mobility Estimation in Graphene p-n Junctions

CVD grown graphene has made significant strides in the last half decade and is currently the method of fabrication most promising for the realization of commercially available graphene based electronics. However, despite advances, it consistently exhibits greater impurity doping, lower mobility, and greater electron-hole conduction asymmetry than exfoliated graphene [24]. Typical carrier mobilities for graphene transistors in SiO_2 vary widely, but are normally reported in the range of 500-10,000 cm^2/Vs, with increased mobility reported when transport measurements are made in vacuum [25]. The estimation of 17,400 cm^2/Vs found in this study shows remarkably high mobility for CVD graphene grown on SiO_2. The highest previously reported values to date lie in the range of 25,000 cm^2/Vs [24], with a predicted limit of 40,000 cm^2/Vs due to extrinsic scattering by surface phonons [26]. One explanation for the high mobility estimated for these graphene p-n junction devices is the large grain size of the graphene present on the devices. One previous study of CVD grown graphene on SiO_2 found that small grain graphene flakes sized less than 20 μm exhibited mobilities in the range of 2,000 cm^2/Vs, while large flakes of 30 to 50 μm exhibited much higher mobilities, on the order of 20,000 cm^2/Vs [25]. The estimation for the mobility found in this study is in strong agreement with these findings, since flakes of 30 μm large grain graphene are present in the p-n junction devices. Large flake graphene also exhibits less asymmetry in conduction between the n and p branches in graphene stemming from more spatially correlated charges [25]. Additionally, the use of low concentration PMMA during the fabrication process may have aided in the high mobility of the devices. Lower concentrations of PMMA during the fabrication process have previously been shown to aid in limiting p doping in graphene, and in enhancing the mobility of CVD grown graphene devices. Low concentration PMMA leaves less residue, and thus require less dissolution with additional chemicals to remove. [27]

4.1.4 Hysteresis in Graphene P-N Junctions

When scanned multiple times over the same gate voltage range, a hysteresis loop is formed, which shows a change in the transport characteristics of the p-n junction. This has previously been observed in graphene, graphene oxide, and carbon nanotubes, as well as in both graphene p-n junctions and graphene based FET's [16]. Previous studies have suggested the hysteresis loop forms due to interactions between the silicon substrate and adsorbates, primarily H_2O. One explanation for these interactions is charge trapping of H_2O molecules bound to the surface of the SiO_2 substrate. Charge trapping is caused by defects at the graphene/SiO_2 interface, which allows H_2O molecules or other impurities to become bound to the surface of the SiO_2 substrate (Figure 4.3). This enables charge tunneling through the graphene/SiO_2 interface to occur. The concentration and reactivity of the Si-OH groups that interact at the interface play an important role in determining the transfer characteristics of graphene p-n junctions and FET's, in addition to being the origin of hysteresis in these devices [15]. However, charge trapping at the interface alone is not enough to explain the hysteresis. The strong ambient dependence of hysteresis suggests a second electrochemical mechanism contributes to the hysteresis in addition to the physical mechanism of charge trapping. This mechanism is the reaction of graphene with H_2O and O_2 molecules through an electrochemical oxidation/reduction reaction described by

$$O_2 + 2H_2O + 4e^- \leftrightharpoons 4OH^- \tag{4.1}$$

Where negative charges from the OH result in a shift of the Fermi level in graphene to a positive gate bias. It has been shown that this electrochemical reaction can take place even in with the presence of a dielectric layer of Al_2O_3 covering graphene, which suggests removing the mechanisms that cause hysteresis is another challenge facing the development of graphene based electronics [22]. Previously, hysteresis in graphene based FETs has also been shown to be highly temperature dependent and dependent upon the maximum applied gate voltage. Higher temperature values increase the trapped charge density at the interface and lower the activation energy necessary for an oxidation/reduction reaction to take place [23]. Applying larger gate voltages at higher temperature also introduces mobile ions within SiO_2, which increases the width of the hysteresis loop [23].

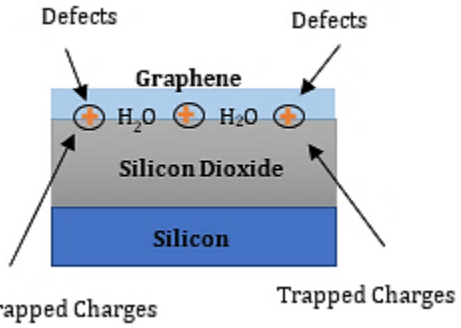

Figure 4.3: Charge trapping of adsorbates at the graphene/SiO_2 interface leads to hysteresis in graphene p-n junction devices.

Interestingly, from figure 3.5, it is observed that each successive forward sweep changes the location of the Dirac point from an initial value of approximately 0.5 V to 0.2 V on the final sweep. The initial value of 0.5 V closely matches the location of the Dirac point at 0.6 V when measured in vacuum, where the shift from 0 V is once again due to charge trapping. [17]. Previous studies on carbon

nanotube FET's have indicated that charge trapping/de-trapping caused by bound H_2O molecules to the SiO_2 surface takes longer than several seconds, which results in hysteresis occurring when measurements are time evolved [16]. This is consistent with the hysteresis observed in graphene p-n junction devices E7 and G5, which exhibited hysteresis after multiple forward/reverse gate voltage sweeps taken over the course of approximately 5 seconds.

Of interest in examining the hysteresis on p-n junction devices G5 and E7 is the presence of a secondary Dirac point at a negative gate bias. This occurs both when source-drain voltages of 10 mV and 25 mV is applied to the devices. On Device E7, the location of the first Dirac point is at 0 V with the additional peak occurring at a negative bias of -0.8 V (Figure 4.3). This second peak is the result of the device having two top gate contacts via which the channel can be accessed, and has been previously reported in devices with two top gates [20]. Tuning the bias across one top gate will result in the appearance of a second Dirac point with a polarity opposite that of the applied bias when swept from -1 to +1 V. Applying a reverse bias injects additional p-type carriers (holes) into the graphene, resulting in a shift of the Dirac point towards more positive gate bias. Similarly, applying forward bias to graphene injects additional n-type carriers (electrons), resulting in a shift towards negative gate bias. This behavior is also observed on Device G5, where peaks are observed at gate voltages of -0.7, -0.65, and -0.5 V on successive reverse sweeps, and +0.6, +0.35, and +0.25 V on successive forwards sweeps.

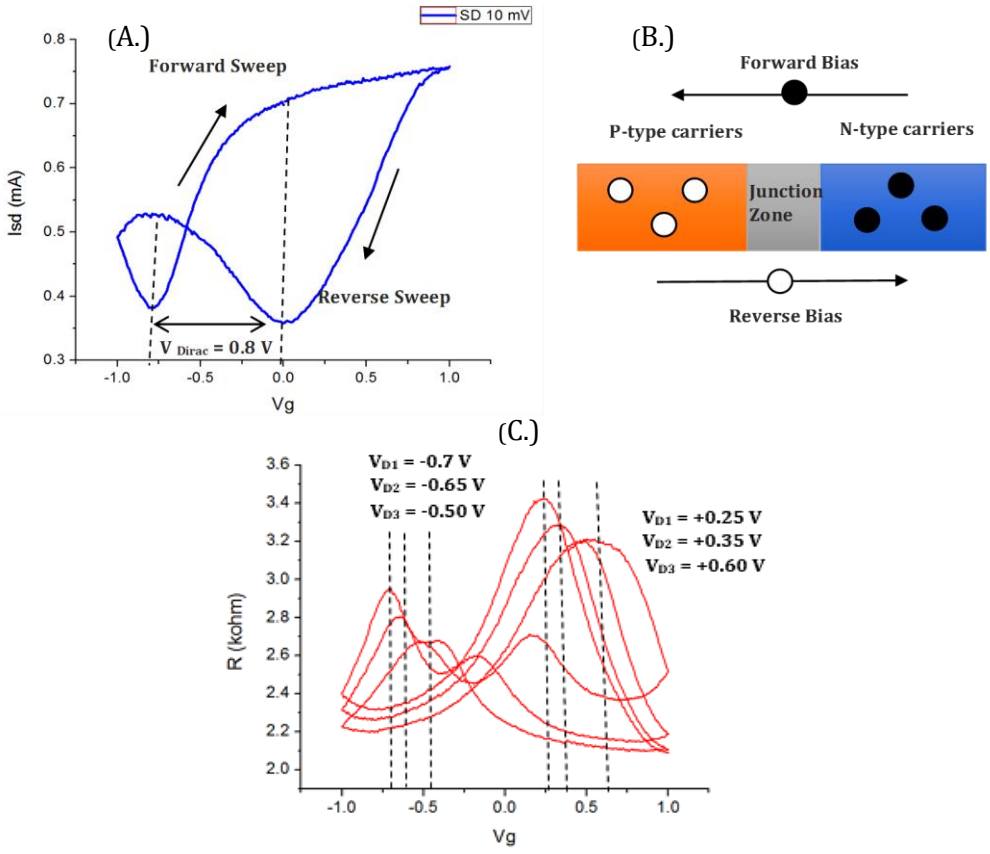

Figure 4.4: (A.) Hysteresis in a graphene p-n junction device E7 results in shifted Dirac points for forward and reverse gate sweeps. The Dirac point shifts 0.8 V based upon the direction of applied bias voltage**. (B.)** Injection of different dopants at the p-n junction occurs based upon the direction of applied gate bias. **(C.)** The Dirac point shifts for each successive forward and reverse gate sweep on device G5.

5 Conclusion

Transport measurements on graphene p-n junction devices reveal the electronic band structure of graphene near the Dirac point. As the gate voltage is swept, the Fermi level in the graphene is tuned from the meeting point of the valence and conduction bands into the conduction band, and doping changes from hole to electron dominated. Measurements on devices G5 and E7 reveal a shift in the Dirac point from its theoretically expected location at zero gate bias, to a value of +0.3 V, which corresponds to a change of -0.02 eV in the Fermi level. This indicates that slight intrinsic p-doping is present in the graphene, which has been well documented in graphene based FETs. The shift in the Dirac point can be attributed to adsorption of H_2O or O_2 molecules at the graphene/SiO_2 interface. This may have occurred during the fabrication process, or from the device's exposure to air during I-V characterization. Many previous studies have found molecular adsorption to shift the Dirac point past a typical gate sweep range of +30 V, indicating the presence of much more significant intrinsic p-doping than is observed in this study. The relative cleanness of the graphene present in p-n junction devices may possibly be attributed to the use of EB irradiation during the fabrication process or to the low concentration of PMMA used when transferring the graphene onto a silicon substrate.

The mobility of the CVD graphene present in p-n junction devices is estimated by taking the differential change of conductance with respect to gate voltage in the linear portion of the curve and averaging the electron and hole mobilities. Using this method, a mobility of 17,400 cm^2/Vs is calculated for the graphene sample in the device. This shows impressively high mobility is present in the CVD graphene on SiO_2, since the average mobility found for CVD graphene on a SiO_2 substrate is on the order of 2000-4000 cm^2/Vs. The high mobility in this device is attributed to the large grain graphene present in the device, which has previously been shown to possess much higher mobility than small grain flakes. The high mobility found provides promising evidence that CVD growth of graphene can be used as the preferred method of growth for commercially based graphene electronics, optoelectronics, and composites.

Hysteresis is observed in the p-n junctions both when the gate voltage is swept multiple times over the same range, and during a single forward and reverse sweep. Hysteresis occurs due to two processes: charge trapping of adsorbates H_2O and O_2 at the graphene/SiO_2 interface and the oxidation/reduction reaction that occurs at the interface from their interaction with the Si/SiO_2 substrate. Additionally, the presence of a two Dirac points on a single gate sweep on devices E7 and G5 shows the shift of the Dirac Point is based upon the direction of applied gate bias. This shift of 0.034 eV (0.8 V), may be attributed to the injection of additional n/p type carriers based upon the application of either positive or negative gate bias, which tunes the Fermi level in the device. The origin of the two Dirac points is due to the dual top gated configuration of the device, where both gates have access to the conduction channel.

5.1 Future Work

There are numerous opportunities for future work on this project. The width of the hysteresis loop and its dependence upon the magnitude of applied gate voltage and on temperature are two such possibilities. Although the physical and electrochemical mechanisms which result in hysteresis have previously been studied, the vanishing of the hysteresis in graphene transistors at low temperature is still not well understood, and the change in the hysteresis at large bias has not been explored in this study. A few studies have examined the dependency of hysteresis on temperature, but more research is needed to understand how hysteresis can be eliminated in graphene based devices.

Acknowledgements

I would like to thank my advisor, Matt Graham, for suggesting this project, and for providing helpful feedback on the research and on the theory and operation of the graphene p-n junctions. I would also like to thank Hiral Patel for helping me troubleshoot the transport station set-up and taking successful preliminary 3-probe transport measurements. Finally, special thanks to Sufei Shi for fabricating the graphene p-n junction devices.

Appendix A: Derivation of the Band Structure of Monolayer Graphene Using Bloch Wave Functions

If we consider the primitive unit cell of graphene, we can find all information about the crystal structure from considering the two carbon atoms present within the 2-D unit cell and a set translation vectors. Since graphene is a 2-D material, two translation vectors are all that is needed to describe its lattice structure. For graphene, these vectors are:

$$\overrightarrow{a_1} = a\begin{bmatrix}1\\0\end{bmatrix} \; and \; \overrightarrow{a_2} = a\begin{bmatrix}\frac{1}{2}\\ \frac{\sqrt{3}}{2}\end{bmatrix} \tag{A.1}$$

The graphene lattice can be created by placing the primitive unit cell at a position described by

$$\vec{R} = n_1\overrightarrow{a_1} + n_2\overrightarrow{a_2} \tag{A.2}$$

Where n_i can be any integer value. The resulting network of points in space is called the Bravais lattice. The wavefunctions within a periodic crystal lattice can be described by Bloch wavefunctions of the form

$$\psi_{\boldsymbol{k}}(\vec{r}) = \frac{1}{\sqrt{N}}\sum_{\vec{R}} e^{i\vec{k}\cdot\vec{R}}\cdot\psi\left(\vec{r}-\vec{R}\right) \tag{A.3}$$

When applied to graphene the Bloch wavefunctions become

$$\psi_{\boldsymbol{k}}(\vec{r}) = \frac{1}{\sqrt{N}}\sum_{\vec{R}} e^{i\vec{k}\cdot\vec{R}}\frac{1}{\sqrt{2}}\left[\phi^{A}_{Pz}\left(\vec{r}-\vec{R}\right) + \lambda_{\vec{R}} * \phi^{A}_{Pz}\left(\vec{r}-\vec{R}\right)\right] \tag{A.3}$$

Here ϕ^{A}_{Pz} and ϕ^{B}_{Pz} are the $2P_z$ orbitals of atom A and on B inside the original primitive unit cell. $\vec{R}$ is the set of all vectors that point to the primitive unit cell within the graphene lattice and $\lambda_{\vec{R}}$ is the phase difference between the ϕ^{A}_{Pz} and ϕ^{B}_{Pz} orbitals.

We know that the Bloch wave functions must satisfy the Schrodinger equation

$$\hat{H}\left|\psi_{\vec{k}}\right\rangle = E\left(\vec{k}\right)\left|\psi_{\vec{k}}\right\rangle \tag{A.4}$$

Converting equation A.3 into Dirac notion we obtain

$$\hat{H} * \textstyle\sum_{\vec{R}} e^{i\vec{k}\cdot\vec{R}}\left(\left|\overrightarrow{R_A}\right\rangle + \lambda_{\vec{R}}\left|\overrightarrow{R_A}\right\rangle\right) = E\left(\vec{k}\right) * \textstyle\sum_{\vec{\boldsymbol{R}}} e^{i\vec{k}\cdot\vec{R}}\left(\left|\overrightarrow{R_A}\right\rangle + \lambda_{\vec{R}}\left|\overrightarrow{R_A}\right\rangle\right) \tag{A.5}$$

Now by projecting the left and right hand sides of the equation onto the complex conjugate, $\left|\overrightarrow{R'_A}\right\rangle$ we obtain

$$\sum_{\vec{R}} e^{i\vec{k}\cdot\vec{R}}\left(\left\langle\overrightarrow{R'_A}\right|\hat{H}\left|\overrightarrow{R_A}\right\rangle + \lambda_{\vec{R}}\left\langle\overrightarrow{R'_B}\right|\hat{H}\left|\overrightarrow{R_B}\right\rangle\right) = E\left(\vec{k}\right)e^{i\vec{k}\cdot\vec{R}} \tag{A.6}$$

Solving for the dispersion relation gives

$$E(\vec{k}) = \sum_{\vec{R}} e^{i\vec{k}\cdot\vec{R}} \left(\langle \overrightarrow{R'_A} | \hat{H} | \overrightarrow{R_A} \rangle + \lambda_{\vec{R}} \langle \overrightarrow{R'_B} | \hat{H} | \overrightarrow{R_B} \rangle \right) \quad (A.7)$$

There are only four non-zero terms in this summation: all the rest go to zero. To simply the expression, we define

When $\vec{R} = \vec{R}'$:

$$\langle \overrightarrow{R'_A} | \hat{H} | \overrightarrow{R_A} \rangle = \alpha \; ; \; \langle \overrightarrow{R'_A} | \hat{H} | \overrightarrow{R_B} \rangle = \beta$$

When $\vec{R} = \vec{R}' + \frac{\sqrt{3}}{2} a\hat{y} \pm \frac{a}{2}\hat{x}$:

$$\langle \overrightarrow{R'_A} | \hat{H} | \overrightarrow{R_B} \rangle = \beta$$

Thus equation A.7 becomes

$$E(\vec{k}) = \alpha + \beta\lambda_{\vec{R}} \left(e^{i\vec{k}\cdot\vec{o}} + e^{i\vec{k}\cdot\left(\frac{\sqrt{3}}{2}a\hat{y} - \frac{a}{2}\hat{x}\right)} + e^{i\vec{k}\cdot\left(\frac{\sqrt{3}}{2}a\hat{y} + \frac{a}{2}\hat{x}\right)} \right) \quad (A.8)$$

Because the allowed energies must be real valued, the phase factor is constrained such that in has equal and opposite phase to the sum of the exponential terms:

$$\lambda_{\vec{R}} = 1 + e^{ik_y\left(\frac{\sqrt{3}}{2}a\cdot\right)} 2\cos\frac{a}{2}k_x \quad (A.9)$$

The term in parentheses is, $\pm \left| 1 + 2\cos\frac{a}{2}k_x \, e^{ik_y\left(\frac{\sqrt{3}}{2}a\cdot\right)} \right| = \pm \left| 1 + 2\cos\frac{K_x a}{2}\left(\cos\frac{\sqrt{3}}{2}k_y a + i * \sin\frac{\sqrt{3}}{2}k_y a\right) \right|$

Solving for the dispersion relation we now obtain

$$E(\vec{k}) = \alpha \pm \beta \sqrt{\left(1 + 2\cos\frac{k_x a}{2} * \cos\frac{\sqrt{3}}{2}k_y a\right)^2 + \left(2\sin\frac{\sqrt{3}}{2}k_y a * \cos\frac{K_x a}{2}\right)^2} \quad (A.10)$$

$$= \alpha \pm \beta \sqrt{1 + 4\cos\frac{k_x a}{2} * \cos\frac{\sqrt{3}}{2}k_y a + 4\cos^2\frac{k_x a}{2}\cos^2\frac{\sqrt{3}}{2}k_y a + 4\sin^2\frac{\sqrt{3}}{2}k_y a * \cos^2\frac{k_x a}{2}} \quad (A.11)$$

And finally

$$E(\vec{k}) = \alpha \pm \beta \sqrt{1 + 4\cos\frac{k_x a}{2}\cos\frac{\sqrt{3}k_y a}{2} + 4\cos^2\frac{k_x a}{2}}$$

Appendix B: Derivation of the Fermi level in Graphene as a Function of Applied Gate Voltage

We treat the capacitive coupling of gated graphene by modelling it as a parallel plate capacitor. With no dielectric present between the plates, the electric field is given by

$$\oint \vec{E} \cdot d\vec{A} = \frac{Q}{\varepsilon_o} = \frac{Q}{\varepsilon_0 A} \tag{B.1}$$

The potential difference is then

$$V = -\int_0^d \vec{E} \cdot d\vec{x} = -Ed \tag{B.2}$$

The capacitance between the plates is defined as

$$C = \frac{Q}{V} = \frac{\varepsilon_0 AE}{Ed} = \frac{\varepsilon_0 A}{d} \tag{B.3}$$

However, with SiO_2 dielectric present between the gate and graphene, we replace the permittivity of vacuum with the permittivity of SiO_2, ε_r, which is 3.9.

We now consider the charge on one plate of the capacitor which is

$$Q = VC = V_g \varepsilon_r \varepsilon_0 A * \frac{1}{d} \tag{B.4}$$

Where V_g is the gate voltage applied to the graphene at V = 0, A is the area of the plate, and d is the thickness, which for these devices is 200 nm.

This can also be thought of in terms of charge carriers. Let N be the total number of charge carriers. The number of carriers times the charge density is the total charge on the plate.

$$\rho N = V_g \varepsilon_r \varepsilon_0 A * \frac{1}{d} \tag{B.5}$$

If we let δn be, N/A, which is the increase in carrier density from applying a gate voltage

$$\rho \delta n = \frac{V_g \varepsilon_r \varepsilon_0}{d} \tag{B.6}$$

We can directly relate the Fermi level to the applied gate voltage through the carrier density. The band structure of graphene is given by

$$E(k) = \hbar V_F |k| \tag{B.7}$$

The density of states, $g(E)dE$, is related to the carrier density and band structure by

$$g(E) = \frac{dn}{dE} = \frac{dn}{dk}\frac{dk}{dE} \tag{B.8}$$

The total number of states in 2-D will by the volume in real space times the volume in momentum space times the fermion (electron) spin degeneracy

$$N = 2\left(\frac{1}{2\pi}\right)^2 V_r V_k \qquad (B.9)$$

We now consider the continuous limit with Avogadro's number of states for a given wave-vector in 2-D space, $\vec{K} = (k_x, k_y)$ (This limit means the states are no longer discrete, but are now continuous). This quantity is defined as $n = \frac{N}{V_r}$. As a function of k this gives

$$n(k) = \frac{2\pi k^2}{(2\pi)^2} = \frac{k^2}{2\pi} \qquad (B.10)$$

If we recall the band structure of graphene near the K point given in equation 1.7 and relate it to the density of states, we obtain (for the + K point)

$$g(E) = \frac{dn}{dE} = \frac{dn}{dk}\frac{dk}{dE} = \frac{k}{\pi}\left(\frac{1}{\hbar V_f}\right) = \frac{E}{\pi\left(\hbar V_f\right)^2} \qquad (B.11)$$

The increase in carrier density, δn, from applying the gate voltage is the integral over all space of the density of states

$$\int_0^\infty 2 * g(E)dE = \delta n \qquad (B.12)$$

However, we know that the density of states is zero for energies greater than the Fermi level, thus the integral becomes

$$\int_0^{E_F} \frac{2E}{\pi(\hbar V_F)^2} dE = \frac{E_F^2}{\pi\left(\hbar V_f\right)^2} \qquad (B.12)$$

Where the factor of two comes from counting the K states. If we now solve for $E_F(V_g)$ by equating equations 1.6 and 1.12. We obtain

$$\frac{E_F^2}{\pi\left(\hbar V_f\right)^2} = \frac{V_g \varepsilon_r \varepsilon_0}{d} \qquad (B.13)$$

$$E_F(V_g) = \hbar V_F \sqrt{\frac{\pi \varepsilon_r \varepsilon_0 V_g}{\rho d}}$$

For graphene p-n junctions, the constants have the following values when V_g is tuned

$\varepsilon_r = 3.9$

$\varepsilon_0 = 8.854 * 10^{-12}\ F/m$

$\rho = 1.6 * 10^{-19}\ C$

$d = 300\ nm$

$V_F = 1 * 10^6\ m/s$

$\hbar = 6.582 * 10^{-36}\ eV * s$

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