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This thesis considers the worst-case design of transistor circuits for the realization of Majority Logic.

First the meaning of Majority Logic is discussed. The requirement of an odd number of inputs for the realization of Majority Logic is justified. The usefulness of Majority Logic in synthesizing a Boolean expression is shown with an example.

Next, three separate circuits for the realization of Majority Logic are considered in detail. The three circuits are designated as:

(1) Variable Threshold Transistor-Resistor Logic Circuit (VTTRL)

(2) Variable Threshold Logic Circuit (VTL)

(3) Transistor Tunnel-diode Resistor Logic Circuit (TTDRL).

The three circuits are compared for their relative advantages and disadvantages.

MAJORITY LOGIC CIRCUITS

by

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SYMBOLS

$K_1'(1+x)$	Upper limit resistance tolerance
$K_1(1-x)$	Lower limit resistance tolerance
N	# of fan-out
M	# of fan-in
L	Threshold value in units of fan-in
$(V_{cs})^*$	Maximum collector ON voltage at $(I_{b_1})_*$
$(V_{cs})_*$	Minimum collector ON voltage
$(V_{bs_1}')^*$	Maximum base ON voltage at $(I_{b_1})_*$
$(V_{bo})_*$	Minimum base OFF voltage (if base-emitter diode is reverse biased)
$(V_{bo})^*$	Maximum base OFF voltage (if base-emitter diode is forward biased)
(I_c')	Maximum collector current at $(I_{b_1})_*$
$(I_{bs})^*$	Worst case base current at edge of saturation for I_c'
$(h_{fe})_*$	Minimum forward current transfer ratio
$(h_{fe})_*$	$=\frac{(I_c')}{(I_{bs})^*}$
$(I_{b_1})_*$	Minimum base ON current

SYMBOLS (Cont'd)

$(\rho)_*$	Minimum overdrive factors $(I_{b_1})_*/(I_{bs})^*$
$(I_o)^*$	Maximum base OFF current (if base-emitter diode is reverse biased)
$(I_o)_*$	Minimum base OFF current (if base-emitter diode is forward biased)
I_{co}	Maximum collector OFF current at maximum operating temperature
$(I_{rc})^*$	Maximum reverse clamping diode current
ν_c	Forward voltage drop of clamping diode
$(\ )_*$	Minimum value
$(\ )^*$	Maximum value
β_1, β_T, h_{fe}	Normal Beta (Forward current transfer ratio)
$\beta_{c_{max}}$	Turn ON circuit beta $((I_c')/(I_{b_1})_*)$
β_{cc}	Turn OFF circuit beta $(I_c'/(I_2')^*) =$
$\beta_{c_{min}}$	Turn ON circuit (storage) beta $(I_c'/(I_{b_m})^*)$

MAJORITY LOGIC CIRCUITS

PART I

MAJORITY LOGIC

Majority logic can be represented in the form of a Boolean expression as

$$M = A \cdot B + B \cdot C + C \cdot A \tag{1}$$

if the three inputs are A, B, and C. In other words, the form of the output depends on the majority of the inputs. There is a concept of practical value which is useful in the design of the majority logic. It appears here as L_C, the complementary threshold level. Given a function, its complement is the funtion which results when the logical states, input and output, are inverted. The complementary level is found from the equation (2).

$$L_C = M - L + 1 \tag{2}$$

where M = total number of inputs

L = threshold level

L_C = complementary threshold level.

In the case the Majority Logic

$$L_C = L \quad (6). \tag{3}$$

This limits the use of majority-gates with an odd number of inputs (table I).

Table I. Threshold and its complementary level

Number	M	L	L_C	Is $L = L_C$?
1	2	1	2	No
2	3	2	2	Yes
3	4	3	2	No
4	5	3	3	Yes
5	6	4	3	No
6	7	4	4	Yes

In table I, it is noted that for all odd number of inputs, $L = L_C$; while for even number of inputs, $L \neq L_C$.

The importance of $L \neq L_C$ is realized when a function F has to be synthesized using only majority gates.

According to Lemma I (1, p. 15), if F is synthesized using only majority gates, then for any input a_i,

$$F(a_i) = \text{"not"}\ F(\text{"not"}\ a_i). \tag{4}$$

This says that if F is built with only majority gates, then complementing the inputs to F will result in the outputs being complemented. This condition can be satisfied only if, $L = L_C$.

Hence it follows that a majority gate must have an odd number of inputs.

The truth table representation of the three-input Majority-Logic is as shown in the table II.

Table II. Three-input majority-logic truth table

A	B	C	M
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Usefulness of Majority Logic

As shown in equation (1), the Boolean representation of three-input Majority Logic is,

$$M = A \cdot B + B \cdot C + C \cdot A \qquad (5)$$

if a Boolean function of this kind is to be realized using AND-OR Logic, it requires three AND gates and one OR gate. The same function can be realized by using one Majority gate. This does not necessarily mean that there will be a reduction in cost and components. It will depend on the type of Majority circuit designed, and the type of components used in its design.

A simple example (4, p. 23-24) of synthesizing a serial-binary

adder using conventional AND-OR-Invert logic and Majority-Invert Logic is considered. Fig. 1-A shows the synthesized serial binary adder using AND-OR-Invert logic. It uses four AND gates, four OR gates and one Invert gate, making a total of nine gates with 17 input elements. It is possible to realize this circuit in other ways but this is one of the simplest, unless special rather than general gates are used.

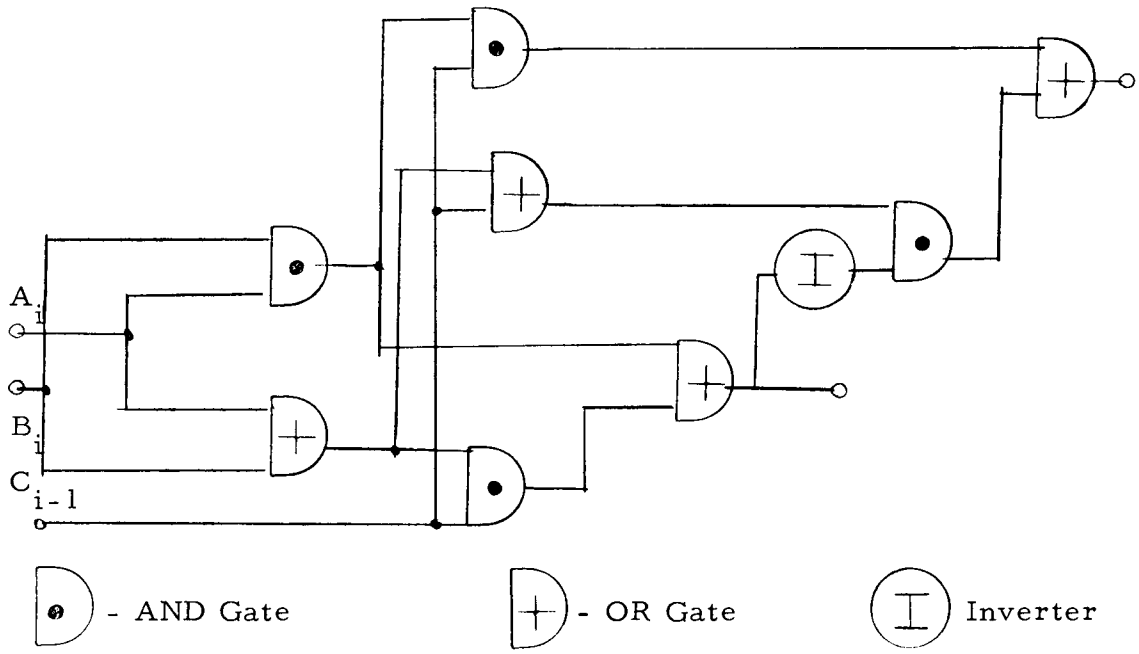
Fig. 1-B shows the same adder using Majority-Invert gates. This arrangement requires three Majority and one Invert gate, making a total of four gates with ten input elements.

The preceding example does not prove that a digital machine composed of three-input M gates and INVERT gates will require less than 50 percent of the circuits required for the more conventional gates. It merely illustrates that M gate approach is simpler in certain cases.

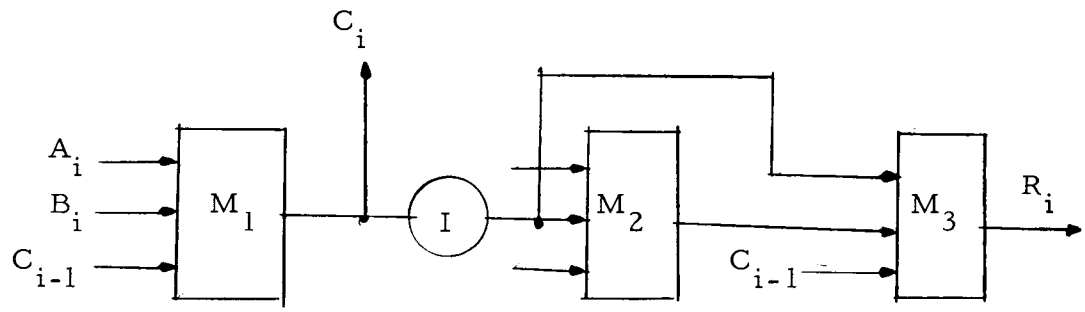
Another important use of Majority Logic comes in the design of Reliable circuits (5, p. 43) using Majority Redundancy techniques.

In order to have a reliable binary operation, an odd number of identical binary units are used in parallel with their inputs connected together and the outputs fed into a Majority gate. If the number of binary units connected is three, one of the units can fail while the redundant system still functions properly.

The importance of Majority Logic in the design of reliable



(A)



(B)

Fig. 1. Serial Binary Adder.

machines and in synthesizing complex Boolean functions, thus, can not be overlooked.

The problem now is to design a Majority-Logic Circuit, which, in itself is simple, at least as fast as the conventional logic circuits and not very expensive.

Three different circuits are considered in detail and then compared for relative advantages and disadvantages.

PART II

CIRCUIT # 1

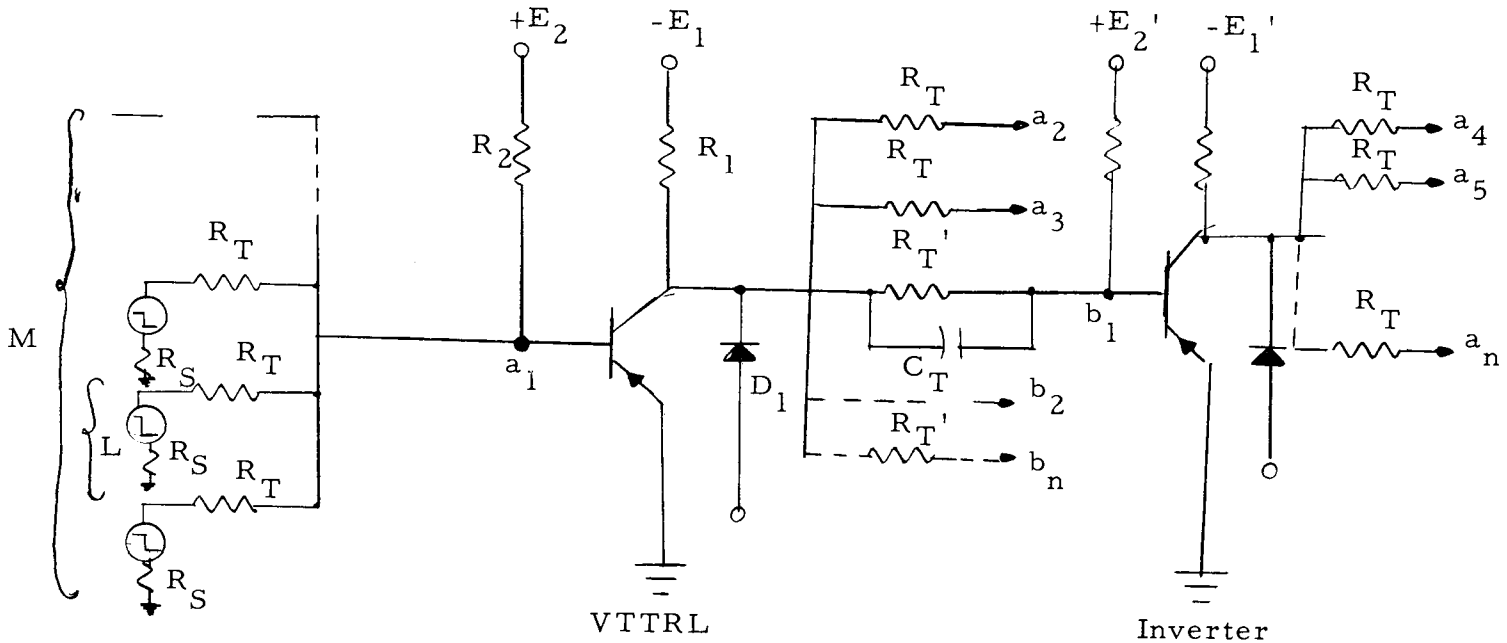
Variable Threshold Transistor Resistor Logic (VTTRL)(6)

The VTTRL circuit considered here uses transistor in common-emitter configuration (Fig. 2). This results in the inversion of the output. Hence an additional transistor is used to get the output in the true form.

The design of the Majority-Logic circuit is divided into two parts: (1) Design of VTTRL circuit: Here the transfer-resistors (R_T) are used to act as a Kirchoff's-Adder for current, such that the transistor turns ON when the Majority of the inputs are present (equal to $-E_C$ volts). The number of inputs in this design is three. (2) Design of Inverter circuit: This design is similar to an ordinary NOR circuit design, where there is only one input. The transistor turn ON, when the input ($-E_C$ volts) is present.

Effect of Source Impedance (R_S)

Ideally a voltage source should have zero impedance. In practice, the impedance of the voltage source should be negligible as compared to the load (transfer-resistors in this case).



R_T - Transfer-resistor for VTTRL

R_T' - Input Resistor for Inverter stage

D - Clamping Diode

M - Number of inputs

L - Threshold level

N - Fan-out

R_S - Source impedance of inputs

Fig. 2. "Majority-Logic circuit using VTTRL and Inverter circuit".

Due to the clamping of the output in each VTTRL and inverter stage, the source impedance of an OFF transistor will be very small (equal to the forward-resistance of the clamping diode).

Also assuming that the flip-flops which supply the voltage pulse to the first stage of the VTTRL circuit have diode-clamping, their source impedance can be neglected.

The source impedance of the D-C voltage supply is about 1ohm to 2 ohms, and if transfer-resistors are of the order of a few k-ohms, it will be less than 0.5% of the transfer-resistors.

If however the transfer-resistors are assumed to be ±1% tolerance, and the source impedance is about 50 ohms, it has to be taken care of. This can be done by selecting the transfer-resistors 50-ohms less than the calculated value.

The Majority Logic circuit of Fig. 2 operates as follows:

(1) VTTRL: When one of the three inputs is $-(E_C)$ volts and the other two are zero, representing logic 1 and logic 0 respectively, the base-emitter voltage of the transistor is made slightly positive by the use of $+E_2$, R_2 current source. At this time, the transistor is cut-off and the collector voltage is equal to $(-E_C)$ volts. The use of the clamping Diode D is to reduce the voltage swing from $(-E_1)$ to $(-E_C)$ volts. This results in a smaller value for the transfer resistors (R_T), which helps improve the transient response of the circuit.

When two of the inputs are $(-E_C)$ volts and one is zero volts, the current supplied by the transfer resistor not only nullifies the effect of back biasing current source $(E_2\text{-}R_2)$ but also supplies enough current to the base-emitter junction of the transistor to saturate the transistor, and thus make the collector voltage zero volts.

The circuit operation is such that when one of the inputs is 1 $(-E_C$ volts) and the other two are 0 (0 volts), the output is 1$(-E_C$ volts). When two or more of the three inputs are 1$(-E_C$ volts) the output is 0 (0 volts). Thus the output wave form is inverted. Hence an additional inverter stage is required to obtain the output in the desired form. The base-emitter voltage is determined by the magnitude and the direction of the current flowing in the base-emitter junction.

When the transistor is to be kept OFF, a small reverse current is allowed to flow through the base-emitter junction to take care of the leakage collector current. Under these circumstances, the transistor is an open circuit for all practical purposes. The steady state base voltage will then be determined by current supplied by the reverse biasing current source (E_2/R_2) and the Input current (Fig. 3).

In the present case, assuming V_n is the base emitter voltage,

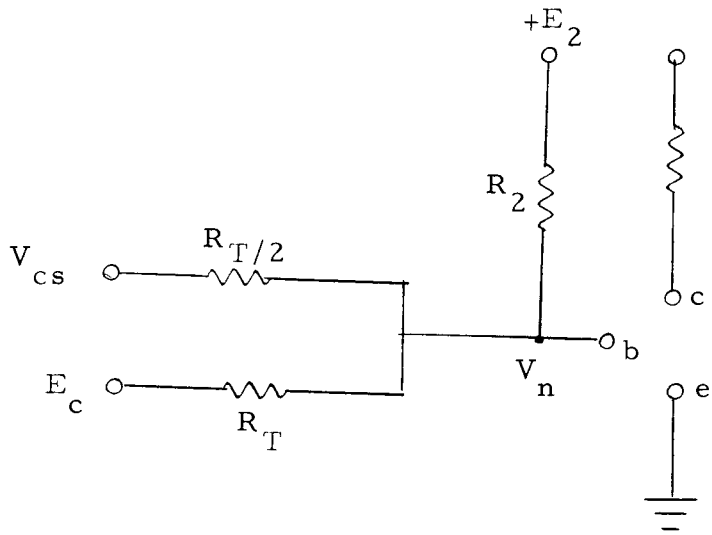


Fig. 3. Base-emitter voltage when the transistor is OFF (assuming transistor to be open circuited).

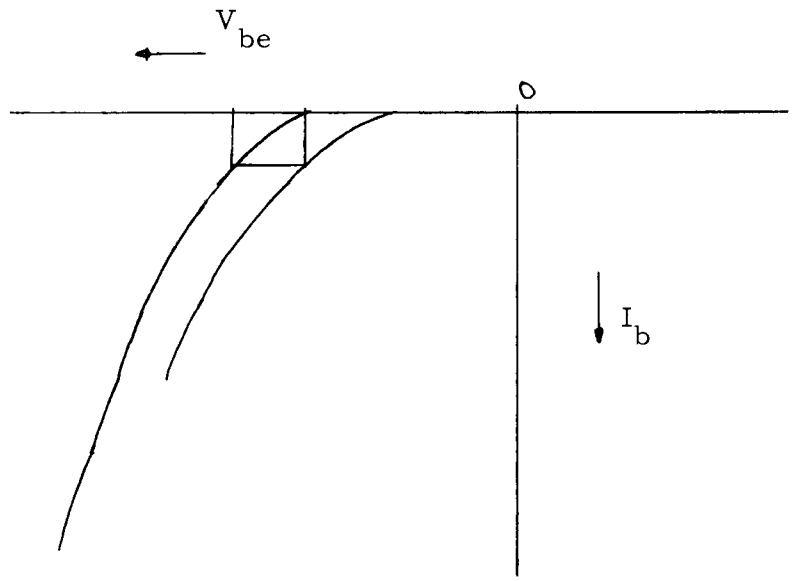


Fig. 4. Base-emitter diode characteristics.

$$\frac{E_2 - V_n}{R_2} = (I_o) + \frac{E_c + V_n}{R_T} + \frac{(V_{cs} + V_n)}{R_{T/2}} \qquad (6)$$

V_n will vary according to the variation of E_2, R_2, E_c and R_T. In order to keep the transistor OFF under worst-case conditions, V_n should be slightly positive for a PNP transistor. Some designers assume this minimum voltage to be 0·5 v, and some 0·1 v (2).

Base-Emitter junction voltage when the transistor is ON

The base-emitter diode is clamped to a certain negative voltage. Once this voltage is reached the base-emitter junction is forward biased. Its characteristics are as shown in Fig. 4. This characteristic has a certain tolerance. Hence for a particular base current, V_{be} has a minimum and maximum limit.

Also as the current through the base-emitter junction increases the base-emitter junction voltage increases according to the characteristics.

Hence, when the transistor is saturated, there has to be an equilibrium among the various current sources and the base-emitter junction diode.

VTTRL Design

Design objective: The basic goal of the design is to insure an

adequate separation between the OFF and ON values of the threshold function in the worst-case situation so that in all other situations, there will be no possibility of losing distinction between the two states. This is done for the OFF state by specifying the minimum OFF base voltage $(V_{bo})_*$, and for the ON state by specifying the minimum ON base current $(I_{b_1})_*$.

The design carried out here is based on Worst-case calculations. This approach is preferred over other methods, such as, Statistical Design because,

1. This design is more reliable.
2. The calculations are much simpler.
3. In the design of VTTRL circuit the tolerance limits on components cannot be appreciably increased by the use of Statistical-Design.

Important Parameters

$(V_{bo})_*$ Minimum Base OFF Voltage

In order to keep the transistor OFF in the presence of maximum leakage current the base-emitter junction is reverse biased. Under the Worst-case conditions, this voltage is assumed to be +(0·1) volts for the PNP transistor used in this circuit.

$(V_{cs})^*$ Maximum Collector ON Voltage

Ideally, the collector ON voltage should be zero volts. If it is not zero volts, it has to be considered with respect to the next stage, because it will supply a small current to the base of the next transistor stage. It depends on the transistor parameters. Hence a transistor with a low $(V_{cs})^*$ is preferable.

(I_c') Maximum Collector Current at $(I_{b_1})_*$

The maximum collector current can be arbitrarily chosen for a particular transistor depending on the collector voltage E_1 and the collector resistance R_1. Its maximum value is however limited by the maximum power dissipation permissible for the transistor being used.

$(h_{fe})_*$ Minimum Forward Current Transfer Ratio

$(h_{fe})_*$ is the most important parameter in the design of VTTRL circuits. It determines the minimum Worst-case base current required to just saturate the transistor. The transistors used for the VTTRL circuit should not have their (h_{fe}) minimum below $(h_{fe})_*$, otherwise the circuit will not function.

$(I_{co})^*$ Maximum Transistor Leakage Current

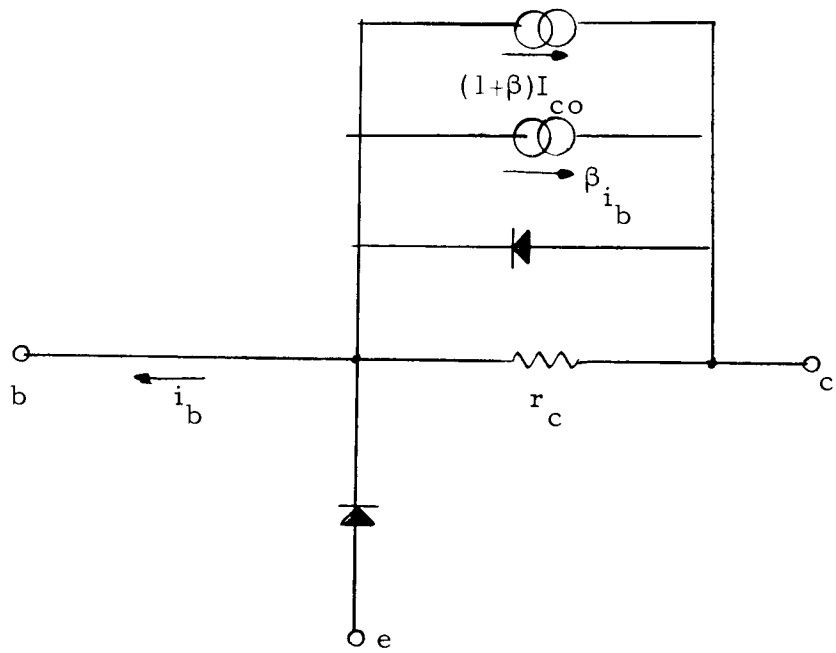
The transistor leakage current, though very small at 25° C, doubles for every 10° C rise in temperature. Hence if the designed circuit has to operate at 70° C, the leakage current at 70° C should be considered in the design. The best way to reduce its effect is to pass a current equal to $(I_o)^*$ in the base of the transistor in the opposite direction. This will cancel $\beta(I_o)^*$ in the collector. Thus the leakage current is reduced from $(1+\beta)(I_o)^*$ to $(I_o)^*$ (Fig. 5).

Selection of a Transistor for VTTRL Circuit

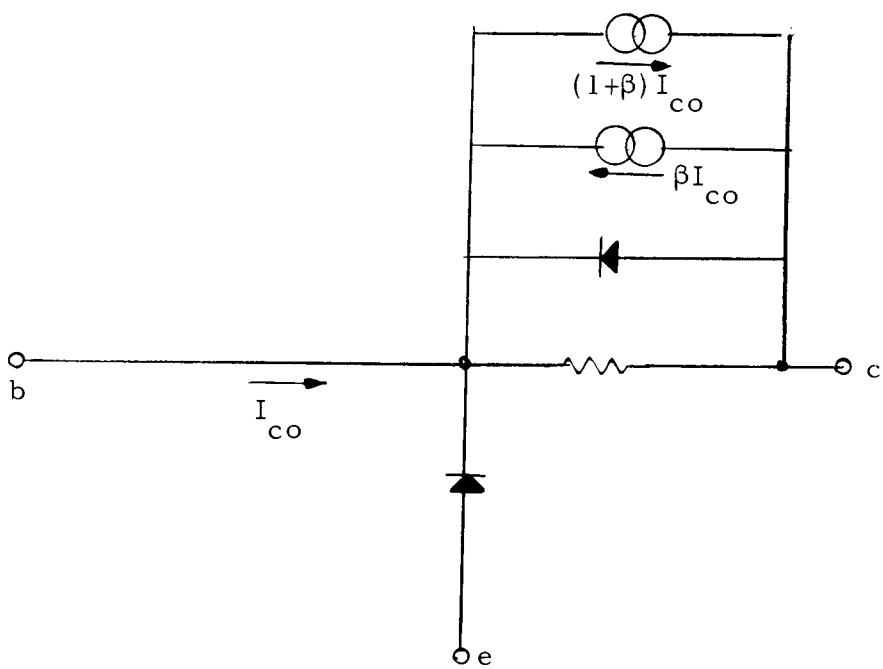
The most important parameter in the steady-state, worst-case design of VTTRL is the minimum forward current transfer ratio, or $(h_{fe})_*$. In order to have a design useful for all transistors of a particular type, it is necessary to know (h_{fe}) minimum for this transistor. Also for a particular transistor, (h_{fe}) minimum should not drop below the specified $(h_{fe})_*$, throughout the working life of the transistor.

The speed of the switching circuit will be determined by the type of transistor, i. e., its Turn-ON and Turn-OFF times, α-cutoff frequency etc. The transient-response for VTTRL is similar (6) to TRL circuits.

The transistor chosen for the design of the following VTTRL



(A) Transistor in Active Region



(B) Transistor in OFF Region

Fig. 5. Effect of Leakage-current.

circuit is 2N1305 PNP Ge transistor. It has $(h_{fe})_* = 40$, and "it is intended for medium speed switching applications where reliability is of prime importance".

Being a Ge transistor, its leakage current is of the order of 100 μA at 70°C, but this is taken care of in the worst-case design and hence does not effect the operation of the circuit at elevated temperatures.

Table III. 2N1305 PNP(Ge) Transistor Characteristics

Absolute Max. Ratings:		
Voltage		
Collector to base	V_{CBO}	-30 V
Collector to emitter	V_{CER}	-25 V
Emitter to base	V_{EBO}	-20 V
Temperature	T_s	-65°C to 100°C
Current:	I_c	-300 mA
Power Dissipation	P_M	150 mW

Electrical Characteristics (25°C)

		Min	Typ	Max.
Forward Current Transfer Ratio (V_{CE} = -1·0V I_c = 1omA)	h_{fe}	40	115	200
Collector-emitter sat. voltage (I_c = -10mA, I_B = -0.25mA)	$V_{CE(sat.)}$			-0·2V
Base-emitter sat. voltage (I_c = 10mA, I_B = -0.25mA)	$V_{BE(sat.)}$	-0.15		-0.35
Cut off: Collector Current	I_{CBO}			-6μA
Alpha cutoff frequency	f_{hfb}	5		14Mcs
Collector Capacity	C_{ob}			20 pf
I_{CBO} at 70°C				100μA

Table IV. Pre-Assigned Parameters

K_1 (1+x)	1.03
K_1 (1-x)	0.97
M	3
L	2
$(V_{cs})^*$	-0.20V
$(V_{bs_1}')^*$	-0.35V
$(V_{bo})^*$	+0.10V
I_c'	10mA
$(I_{bs})^*$	10/40 = 0.25mA
$(h_{fe})^*$	40
$(\rho)^*$ $(I_{b_1})^*/(I_{bs})^*$	1.20
$(I_{b_1})^*$	0.30mA
$(I_o)^*$	0.12mA
$(V_{cs})^*$	0.01 V
$(I_{rc})^*$	0.05mA
ν_c	0.1 V
$V_{bs(3)}$	0.45V
E_1	-15V
E_2	+15V
E_c	-5V

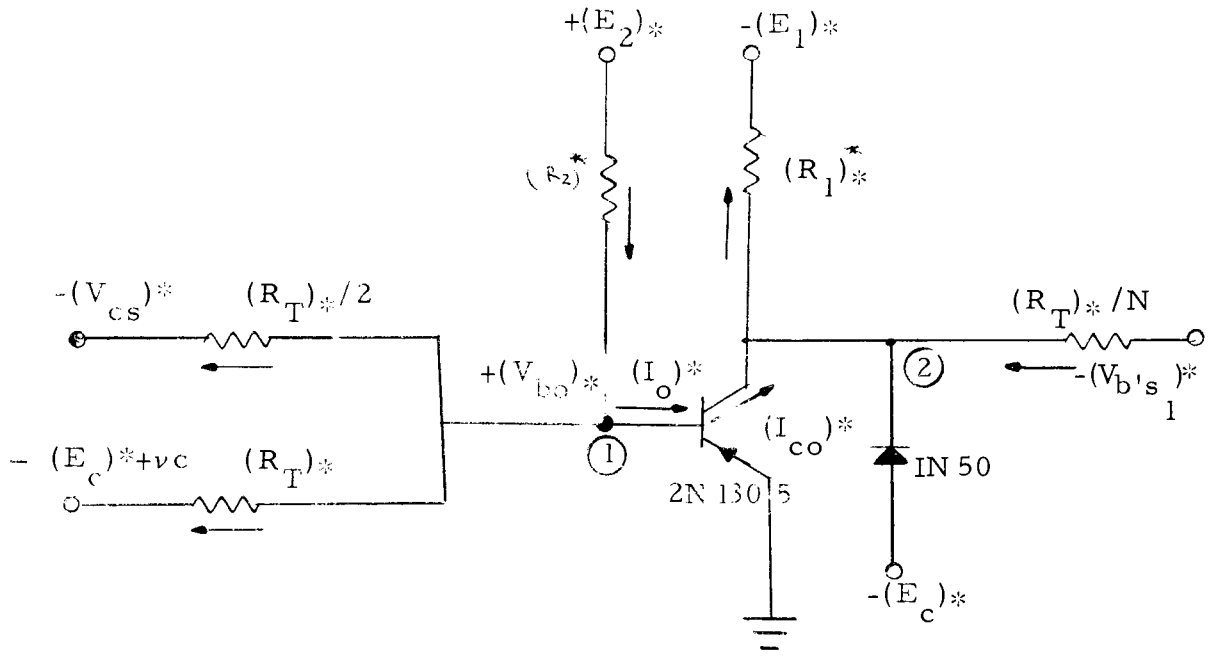


Fig. 6-A Worst-case OFF condition (VTTRL).

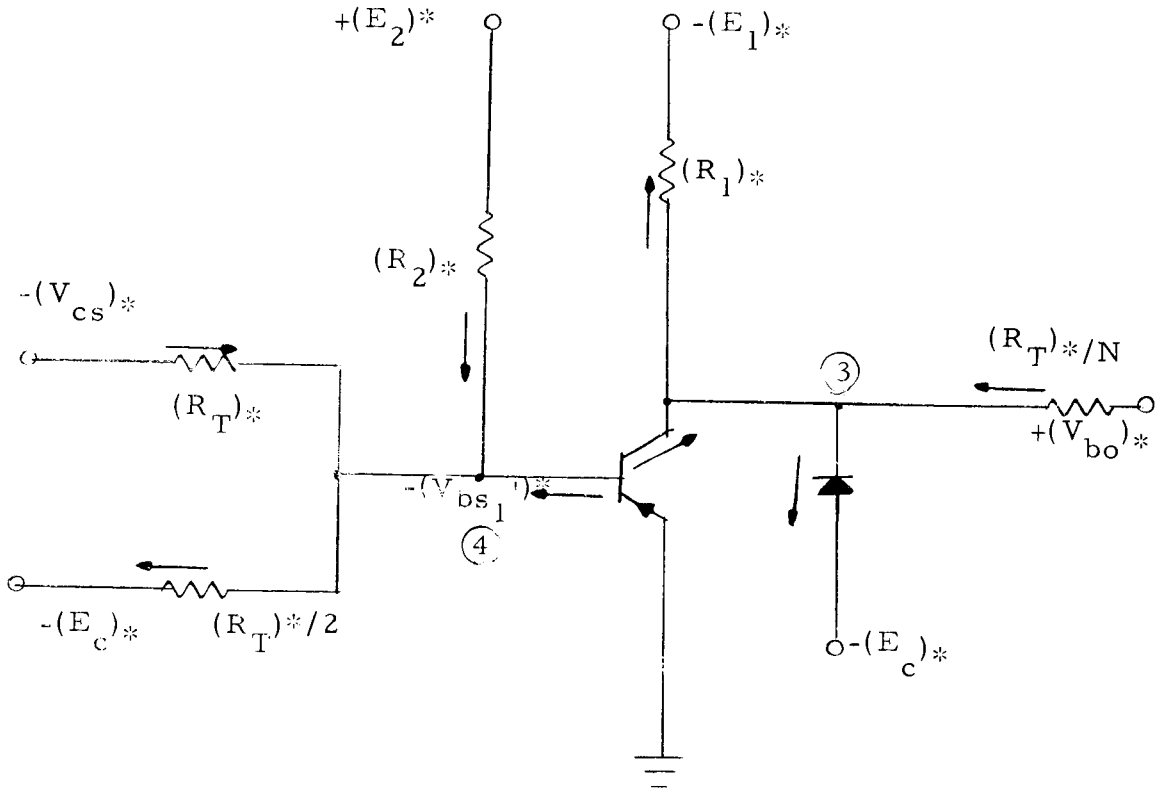


Fig. 6-B Worst-case ON condition (VTTRL).

Worst-Case OFF Condition Fig. 6-A

The values of the circuit parameters used in this circuit are such as to make the transistor ON. The reverse-bias current supplied by (E_2/R_2) is assumed to be a minimum. The collector of the two preceding ON stages is assumed to be at its maximum value and so is the clamping voltage (E_c) of the preceding OFF stage. The values of the transfer resistors (R_T) are assumed to be minimum. This causes the reverse current in the base-emitter junction to be minimum. In order to take care of the leakage current at elevated temperatures, this leakage current, at its maximum value, should be balanced by an equal reverse current in the base-emitter junction. Using these conditions, equation (1) is written for node (1).

$$\frac{((E_2)_* - (V_{bo})_*)}{(R_2)^*} = (I_o)^* + \frac{((V_{bo})_* + (V_{cs})^*)(2)}{(R_T)_*} + \frac{((E_c)^* + \nu_c + (V_{bo})_*)(1)}{(R_T)_*} \qquad (7)$$

In the collector circuit, the output current supplied by the E_1-R_1 current source is assumed to be a minimum. The clamping voltage (E_c) is also assumed to be minimum. This results in

minimum current supplied to the output transfer resistors. The output of the VTTRL is connected directly to an Inverter circuit; the base-ON voltage of Inverter circuit is assumed to be the maximum for this condition. If the transfer resistors at these conditions are at their minimum value, the number of outputs is reduced to a minimum. It is also assumed that a leakage current $(I_{co})^*$ is flowing in the collector at this time, which is also obtained from (E_1, R_1), thus reducing the current supplied by (E_1, R_1) to the output transfer resistors to a minimum. Writing the current equations for Node (2).

$$\frac{((E_1)_* - (E_c)_*)}{(R_1)^*} = (I_{co})^* + \frac{((E_c)_* - (V_{bs_1},)^*) \times N}{(R_T)^*} \qquad (8)$$

Worst-Case ON Conditions Fig. 6-B

In the collector circuit, the current supplied by the $(E_1 R_1)$ current source and the reverse current through the clamping diode balance the maximum collector ON current and the small current taken by the succeeding Inverter stage5 which is assumed to be OFF. As the maximum collector ON Current is assumed to be of a fixed value, the increase in fan-out will decrease this current. Decrease in the collector current results in reduced base ON current, which if it becomes appreciably less, will turn ON the transistor when it should not. This also limits the maximum number of outputs

possible.

Writing the current equation for node (3)

$$(I_C') = (I_{RC})^* + \frac{((E_1)_* - (V_{cs})^*)}{(R_1)_*} - \frac{((V_{bo})_* + (V_{cs})^*)}{(R_T)^*/N} \qquad (9)$$

Worst-Case ON Condition Node 4, Fig. 6-B

In the base circuit (Node 4), two of the inputs are present ($-E_c$ volts) and one of the inputs is absent (approx. zero volts). In this case a forward current, of enough magnitude to saturate the transistor, has to be supplied to the base-emitter junction by the two inputs that are present. It must also supply additional current to cancel the reverse bias current (E_2/R_2) and the small current due to one of the inputs that is approx. zero volts. Hence the clamping voltage (E_c) is assumed to be a minimum, transfer resistors for the two inputs, that are present, to be a maximum. This results in the minimum forward current. Also the base on voltage is assumed to be a maximum so that the difference in input and base ON voltage is a minimum, resulting in less input current. Maximum base ON voltage increases the current taken by the reverse bias current source, because the two voltages E_2 and $(V_{bs_1},)^*$ are of opposite polarity. E_2 is assumed to be a maximum and R_2 to be a minimum. The transfer resistor of the other input is assumed to be a minimum and the input voltage near zero, so that it takes a

maximum current.

The Node equation is:

$$\frac{((E_c)_* - (V_{bs_1'})^*) \times 2}{(R_T)^*} = (I_{b_1})_* + \frac{((E_2)^* + (V_{bs_1'})^*)}{(R_2)_*} + \frac{((V_{bs_1'})^* - (V_{cs})_*)(1)}{(R_T)_*} \qquad (10)$$

Calculation of Circuit Parameters

All the calculations done here are for

$$M = 3, \quad L = 2.$$

Four equations (equations 7, 8, 9, 10) are written for as many unknowns. The unknowns are R_T, R_1, R_2, N.

It is possible to assume clamping voltage ($-E_c$) as unknown, and then solve the four equations to get $N = f(R_T)$, and maximize, N. After going through one such calculation, it was found that N_{max} lies between 4 and 5. E_c for this case is slightly higher than 5 volts. The solution for $N = f(R_T)$ results in a fourth degree equation and the calculations are very involved. On assuming $E_c = -5$ volts and then solving the four equations (7, 8, 9, 10) for the four unknowns gives $N_{max} = 4$. In this case the solution $N = f(R_T)$ is in the form of a second degree equation, and is much simpler.

The calculation here are based on the assumption that the

succeeding stage is an inverter circuit, i. e., when VTTRL is OFF, Inverter is ON and vice-versa. It is possible to use the fan-out directly as the fan-in of a VTTRL circuit. Due to change in base-voltage conditions (it may be OFF or ON depending on majority of the inputs), the fan-out is reduced to 3. The fan-in for the Inverter is 1, so that the speed-up capacitor can be used without causing "Cross-talk," which occurs, if the fan-in is more than 1, due to the interaction between various inputs.

Effect of Tolerance on the Design of VTTRL Circuit

Due to the use of threshold of inputs in VTTRL, the usual tolerance limits (used in TRL NOR Logic) can not be used.

On increasing the tolerance limits for voltage supplies and resistors, the value of transfer resistor starts decreasing, after a certain limit, the value of R_T becomes negative, i. e., the design is not feasible.

Table V shows the effect of tolerance limits on R_T.

Table V. Tolerance effect

No.	Voltage supply tolerance limit	Resistor tolerance limit	Value of R_T in KΩ
1	3%	3%	2. 90 K
2	3%	5%	1. 62 K
3	5%	5%	0. 044 K
4	10%	10%	-10. 4 K

It was therefore decided to use 3% tolerance limit for resistors and voltage supplies.

Values of the unknowns:

$$R_T = 2.90 \pm 3\% K\Omega$$

$$R_2 = 6.25 \pm 3\% K\Omega$$

$$N_{max} = 4.04$$

$$R_1 = 1.54 \pm 3\% K\Omega$$

Though most of the resistors available commercially are of 5% or 1% tolerance, it is usually stated that the 1% resistors vary to 3% tolerance limit in their working life.

Also, the purpose of the design, here is to show how much maximum tolerance limits can be imposed on the components.

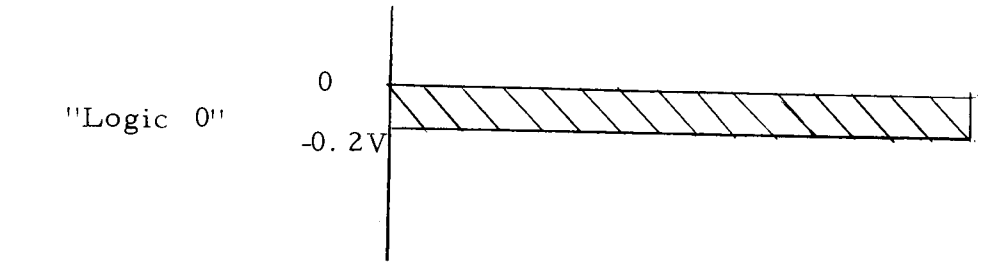
For this design, the output voltage tolerance and base-emitter junction voltage tolerance will be as shown in Fig. 7-A and 7-B.

Maximum Power Dissipation for Each Variable Threshold TRL Circuit (6)

$$P_{max(ON)} = \frac{(E_2^2)^*}{(R_2)_*} + \frac{(E_1^2)^*}{(R_1)_*} \tag{11}$$

$$P_{max(OFF)} = \frac{(E_2^2)^*}{(R_2)_*} + \frac{(E_1)^*}{(R_1)_*}((E_1)^* - (E_c)_*) - N\frac{(E_c^2)_*)}{(R_T)^*} \tag{12}$$

$$\left.\begin{aligned} P_{max(ON)} &= 196.8 \text{ mW} \\ P_{max(OFF)} &= 86.45 \text{ mW} \end{aligned}\right\}$$



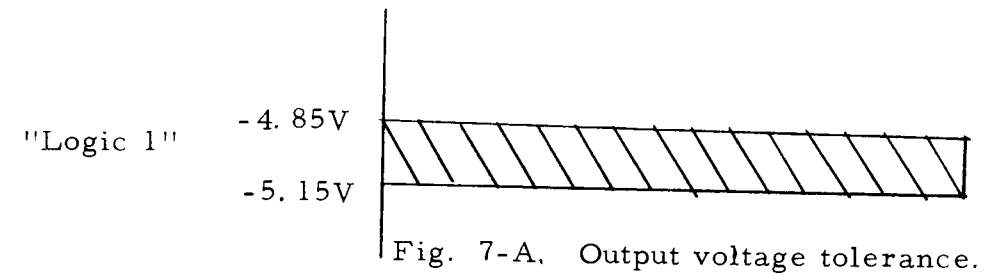


Fig. 7-A. Output voltage tolerance.

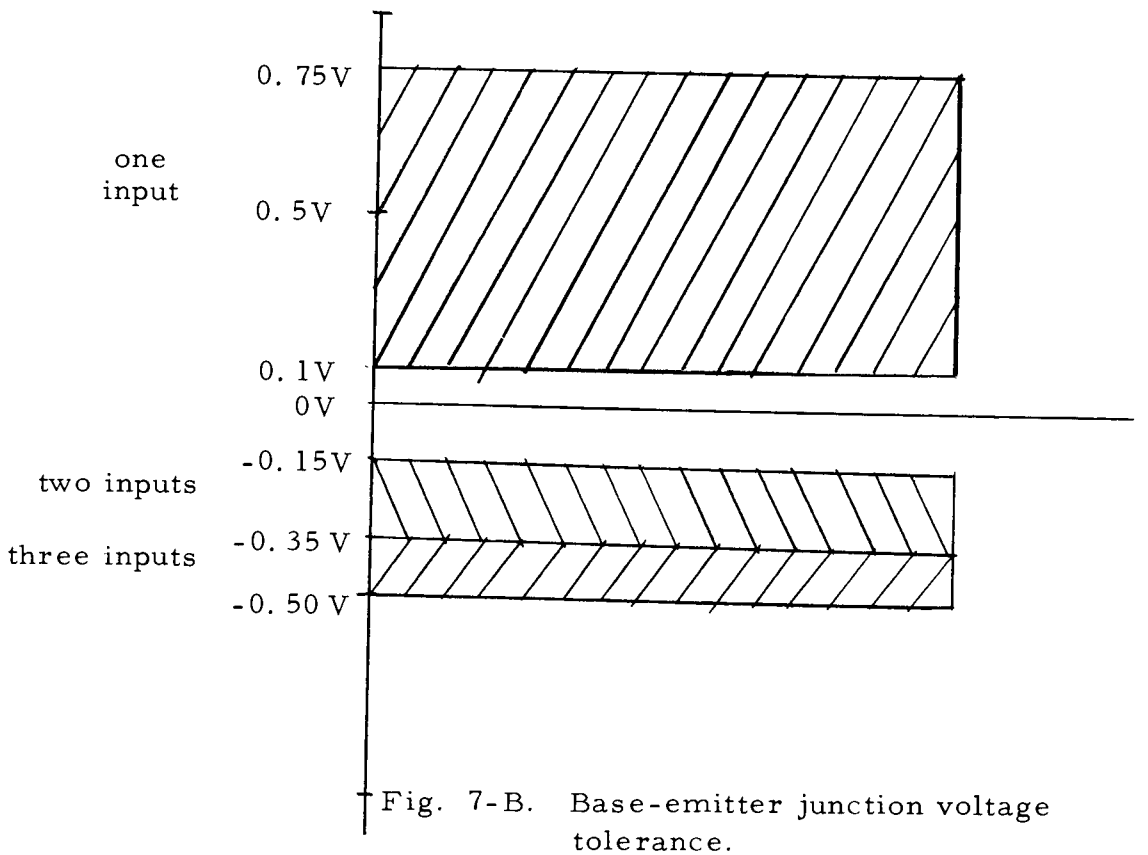


Fig. 7-B. Base-emitter junction voltage tolerance.

For 50% (Worst case) duty cycle

$$\left.\begin{aligned} P_{AV} &= 141.63 \text{ mW} \\ P_{max\ (allowed)} &= 150 \text{ mW} \end{aligned}\right\}$$

Hence the operation is well within the dissipation limits.

Transient Response

In order to calculate the transient response, some additional parameters have to be determined.

(1) $(I_{bm})^*$ = Maximum base ON current (Fig. 8).

$$(I_{bm})^* = \frac{M((V_{co})^* - V_{bs}'(3))}{(R_T)_*} - \frac{((E_2)_* + V_{bs(3)})}{(R_2)^*} \qquad (13)$$

$(V_{co})^*$ = Maximum collector OFF voltage

$V_{bs}'_{(3)}$ = base ON voltage when all the three inputs are present. It is assumed to be slightly higher then,

$(V_{bs_1}')^*$ = Max base ON voltage at $(I_{b_1})_*$.

$(I_{bm})^*$ obtained here was equal to 2.68 mA.

(2) (I_2') = Minimum available transient turn OFF current.

The current (I_2') is chosen as the Worst-case turn OFF, immediately following $(I_{bm})^*$, i.e., the ratio $(I_{bm})^*/(I_2')_*$ is maximum. For this case base voltage = $V_{bs}'_{(3)}$. The tolerance of the $(R_T)_*$ resistors was established for $(I_{bm})^*$, and it is not

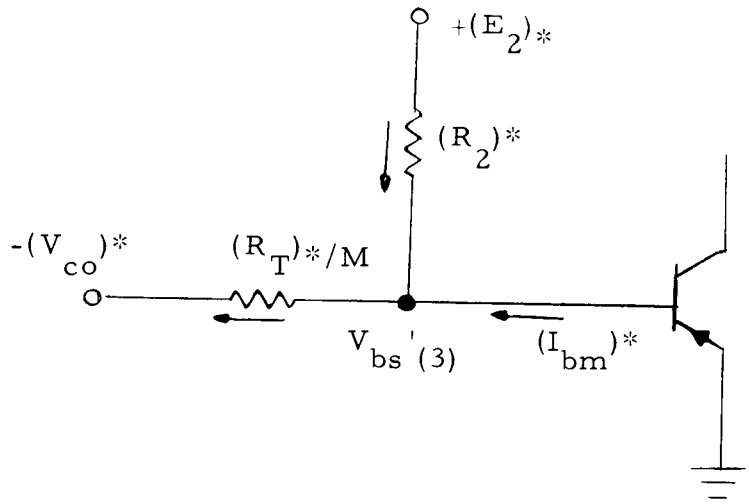


Fig. 8. Maximum base-ON current.

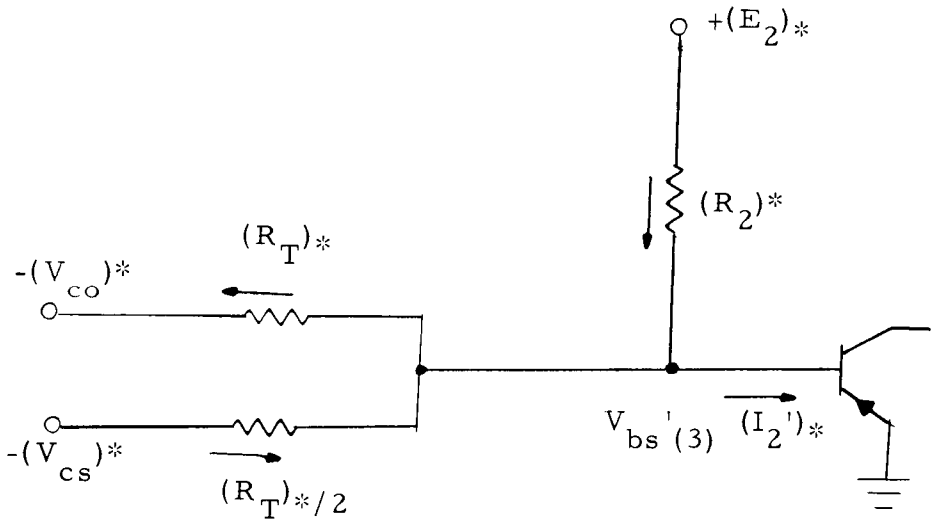


Fig. 9. Minimum available turn-OFF current.

reasonable to assume that some (M-L+1) would change to the upper bound, just as the transistor is switched OFF. Hence $(I_2')_*$ is designated as the minimum available turn OFF current. The true steady state $(I_2)_*$ as calculated in Worst Case OFF condition for base voltage $(V_{bo})_*$ is not used for transient conditions.

$$(I_2')_* = \frac{((E_2)_* + V_{bs'(3)})}{(R_2')^*} + \frac{((V_{bs(3)}) - (V_{cs})^*)(M-L+1)}{(R_T)_*} - \frac{((V_{co})^* - (V_{bs'(3)}))(L-1)}{(R_T)_*} \qquad (14)$$

$(I_2')_* = 0.82$, $(I_{bm})^*/(I_2')_* = 2.68/0.82 = 3.27$

Worst-case transient response prediction for 2N1305 transistors with $t_{total\ (max)} = 1.50\ \mu sec.$ (For VTTRL)

Though the minimum α cutoff frequency for 2N1305 is 5Mc/s and typical α - cutoff frequency is 14 Mc/s (Appendix I), it was found that the majority of the transistors tested in the lab had their turn ON and turn OFF time very close to the times for a typical transistor as given in the data sheet.

On this basis, the Worst case transient response was calculated (Appendix II) for the variable threshold logic and its typical collector and base currents.

$$\left.\begin{aligned} t_d + t_r &= 0.90\ \mu\text{sec. max.} \\ t_f &= 0.38\ \mu\text{sec. max.} \\ t_s &= 1.11\ \mu\text{sec. max.} \end{aligned}\right\}$$

The observed max. times are: (Fig. 12, 13)

$$\left.\begin{aligned} t_d + t_r &= 0.60\ \mu\text{sec. (two inputs)} \\ t_f &= 0.40\ \mu\text{sec. (two inputs)} \\ t_s &= 0.60\ \mu\text{sec. (three inputs)} \end{aligned}\right\}$$

The difference in the observed and calculated values is because of the fact that the worst case max. base ON current (I_{bm})* is not reached resulting in less storage time.

The turn-on time (0.60 μsec.) is less than the worst-case calculated turn-on time (0.90 μsec.) because under worst-case a base current of 0.30mA is required to just turn-on the transistor, but under normal circumstances this current is much higher. In this circuit it was found to be 0.50 mA. This changes the circuit β from 33.3 to 20 which results in the reduction of calculated rise-time from 0.90 to 0.54 μs. Adding a delay time of 0.06 μs, the total turn-on time is now 0.60 μs.

Fall time seems to agree for both the observed and calculated cases. This is because the turn-off currents in the two cases are approximately equal.

Hence it can be concluded that when the worst-case design is used for calculating the steady-state and transient response, the

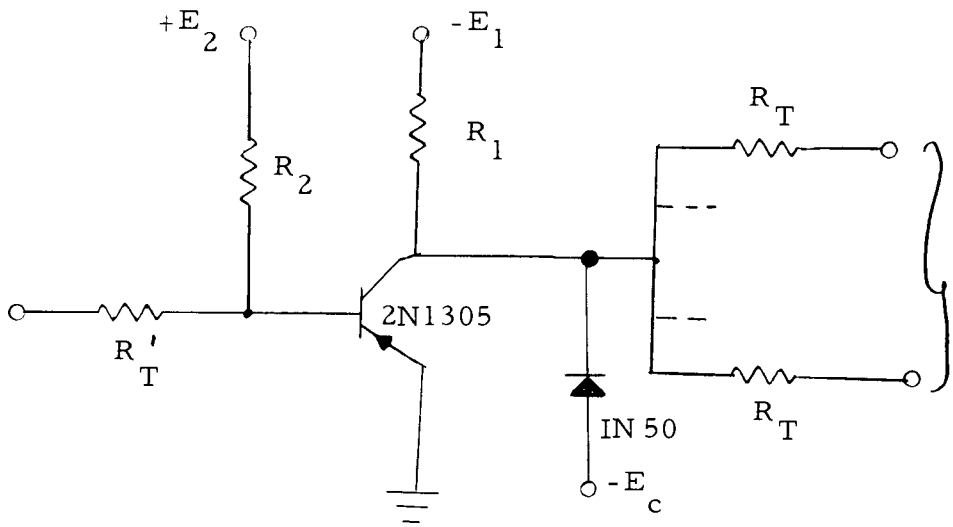


Fig. 10-A. Inverter circuit.

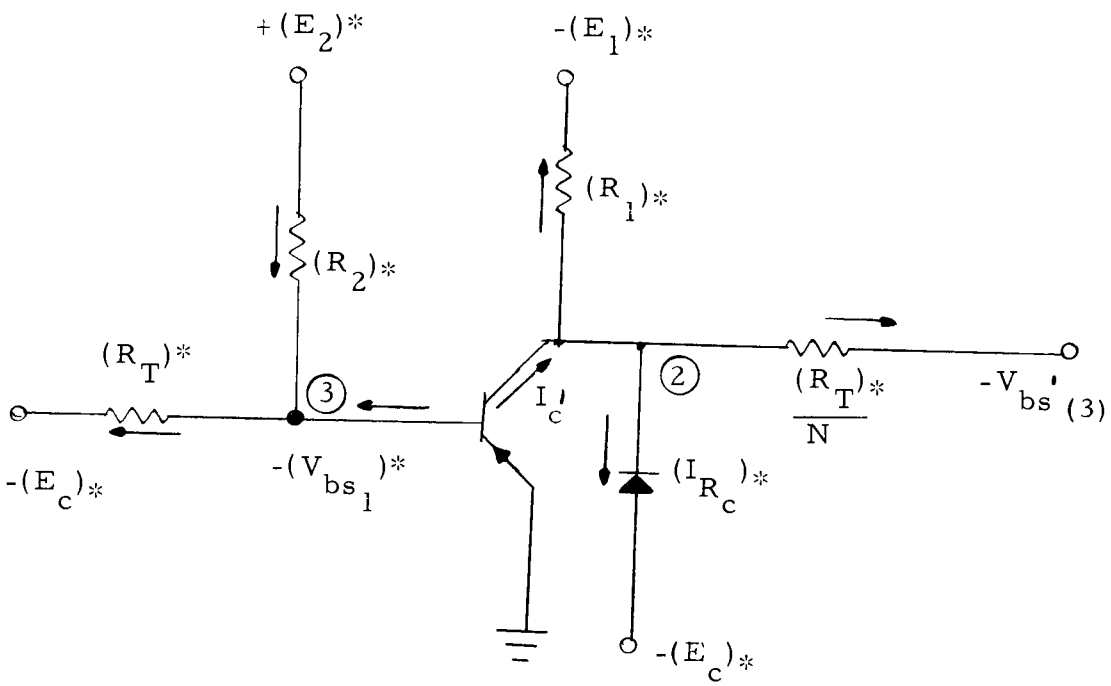


Fig. 10-B. Worst-case ON condition (Inverter).

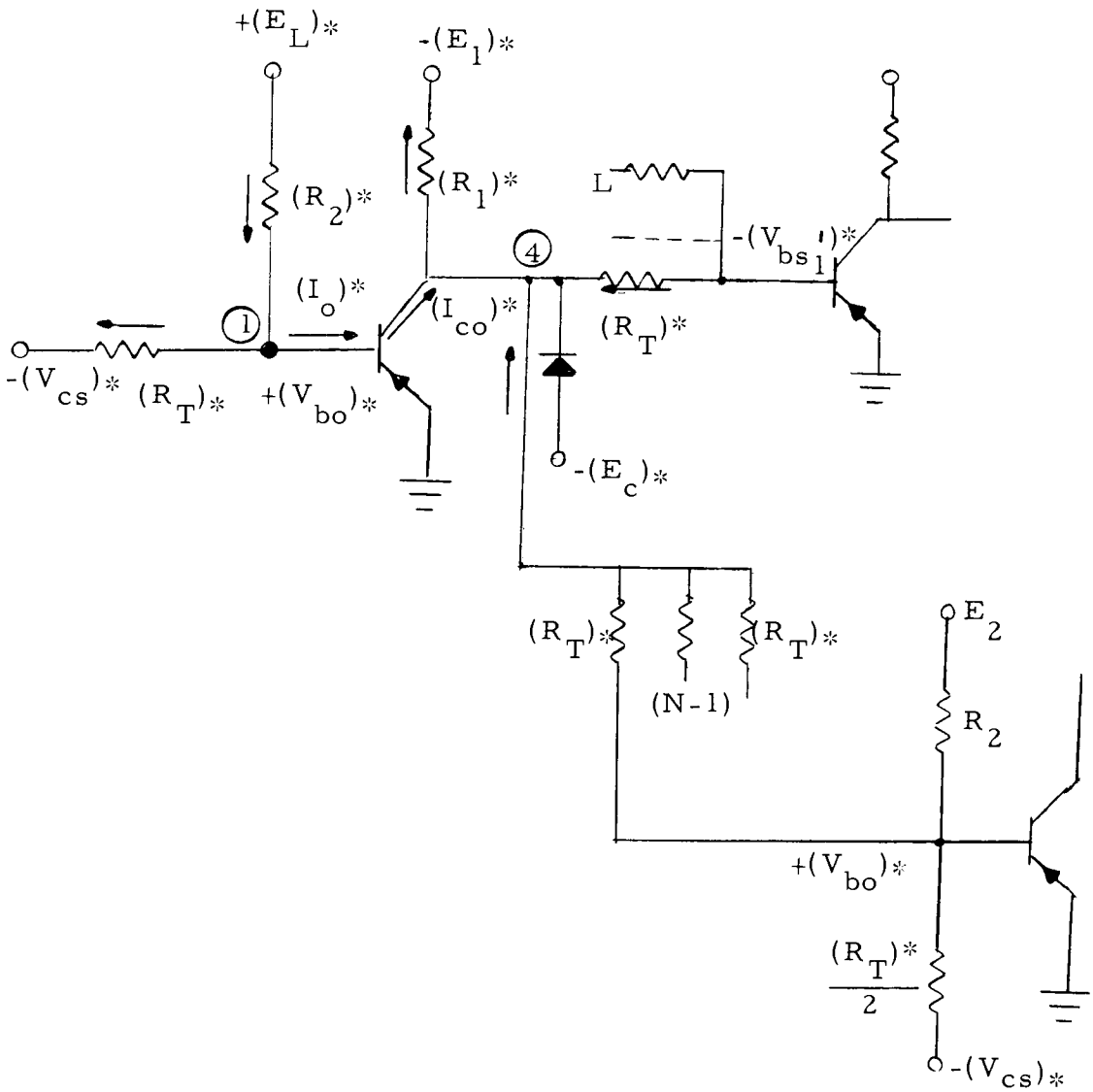


Fig. 10-C. Worst-case OFF condition (Inverter).

switching times calculated for the worst case conditions are much longer than the observed times (under typical conditions).

For the standard TRL Inverter circuit, the fan-in is just one. The fan-out is to be maximized.

Under the Worst-case OFF condition (Fig. 10-C), the preceding transistor is assumed to be ON. Similar to the case of VTTRL worst-case design, the parameter values are assumed, such that the reverse bias current due to (E_2, R_2) is a minimum, and the current due to the preceding ON stage is a maximum. The reverse base-emitter bias current is the difference of these two currents and is therefore a minimum.

In the collector circuit, the fan-out can be connected to both, ON and OFF transistors. In the worst case it is assumed, that one of the outputs is connected to an ON transistor, and the rest of the outputs are inputs for transistors which are OFF.

The fan-out connected as fan-in for an ON transistor will have its transfer resistor (R_T) at its upper tolerance limit. The fan-out connected as fan-in for OFF transistors will have their transfer resistor at its minimum tolerance limit.

The four node equations are then written, as in case of VTTRL. Equations (15) for Node (1) in Fig. 10-C and Equation (16) for Node (3) in Fig. (10-B) are solved for $(R_2)_{min}$ and $(R_2)_{max}$. Equation (17) for Node (2) in Fig. 10-B and Equation (18) for Node (4) in

Fig. 10-C are solved for N and R_1.

Node (1) Worst-case OFF

$$\frac{((E_2)_* - (V_{bo})_*)}{(R_2)^*} = (I_o)^* + \frac{((V_{cs})^* + (V_{bo})_*)}{(R_T)_*} \tag{15}$$

In this equation all the parameters are known except $(R_2)^*$. Hence $(R_L)^*$ is determined using equation (1).

Node (3) Worst-case ON

$$\frac{((E_c)_* - (V_{bs_1'})^*)}{(R_T)^*} = (I_{b_1})_* + \frac{((E_2)^* + (V_{bs_1'})^*)}{(R_2)_*} \tag{16}$$

From this equation $(R_2)_*$ is calculated.

$$\left.\begin{aligned} (R_2)^* &= (R_2)_{max.} = 64\,k \\ (R_2)_* &= (R_2)_{min} = 14.5\,k \end{aligned}\right\}$$

Choosing a value near $(R_2)_{max}$ increases the base current resulting in a larger storage time. Hence R_2 is chosen close to $(R_2)_{min}$, i.e.,

$$R_2 = 15\ k$$

Additional base current for fast rise is provided by the speed up capacitor.

Worst-case ON: Node (2)

$$(I_c') = (I_{RC})^* + \frac{((E_1)_* - (V_{cs})^*)}{(R_1)^*} + \frac{((V_{bs})^* - (V_{cs})^*)}{(R_T)^*/N} \quad (17)$$

Worst-case OFF: Node (4)

$$\frac{((E_1)_* - (E_c)_*)}{(R_1)^*} = (I_{co})^* + \frac{((E_c)_* + (V_{bo}))(N-1)}{(R_T)^*} + \frac{((E_c)_* - (V_{bs_1}')^*)}{(R_T)^*} \quad (18)$$

Using equations (2) and (4), the two unknowns N and R_1 are calculated.

$$\left.\begin{array}{ll} N = 3.60 & R_1 = 1.52 \text{ k.} \\ \text{For } N = 3.0 & R_1 = 1.82 \text{ k} \end{array}\right\}$$

N = 3.0 is assumed as maximum fan out. and $R_1 = 1.60 \pm 5\%$ is chosen.

It seems that N_{max} is the only parameter in the Inverter circuit that can be optimized.

Because R_T and the voltage swing (0 to -5V) are specified, the only way to increase N is to increase the max. collector ON current (I_c').

For the present circuit

$I_{in} = 1.50$ mA, if the current thru (E_2, R_2) is used to

just cancel the reverse current $(I_{CBO})_{max}$, then,

$$(I_c')_{max} = 1.50 \times 40 = 60 \text{ mA.}$$

However $(I_c')_{max}$ is limited by the power dissipation of the transistor being used.

With the present circuit design the average power dissipation for TRL circuit is 116.4 mW. Hence it is highly unlikely that N_{max} can be increased beyond 4.

However if the output transfer-resistors (R_T) of VTTRL circuit are raised in value as compared to the input transfer resistances, the fan-out of VTTRL can be increased. The disadvantage is that the fan-out of VTTRL cannot be used as the fan-in of some other VTTRL if an inverted signal is to be directly applied to that VTTRL.

Transient response

$$\left.\begin{aligned} (I_{bm})^* &= 0.70 \\ (I_2')_* &= 1.06 \end{aligned}\right\} \quad \text{calculated values}$$

The calculation for the switching times were made similar to the sample VTTRL calculation of Appendix II.

The calculated switching times are

$$t_{r_1} = 0.90 \mu\text{sec}$$

$$t_{f_1} = 0.304 \mu\text{sec}$$

$$t_{s_1} = 0.40 \mu\text{sec}$$

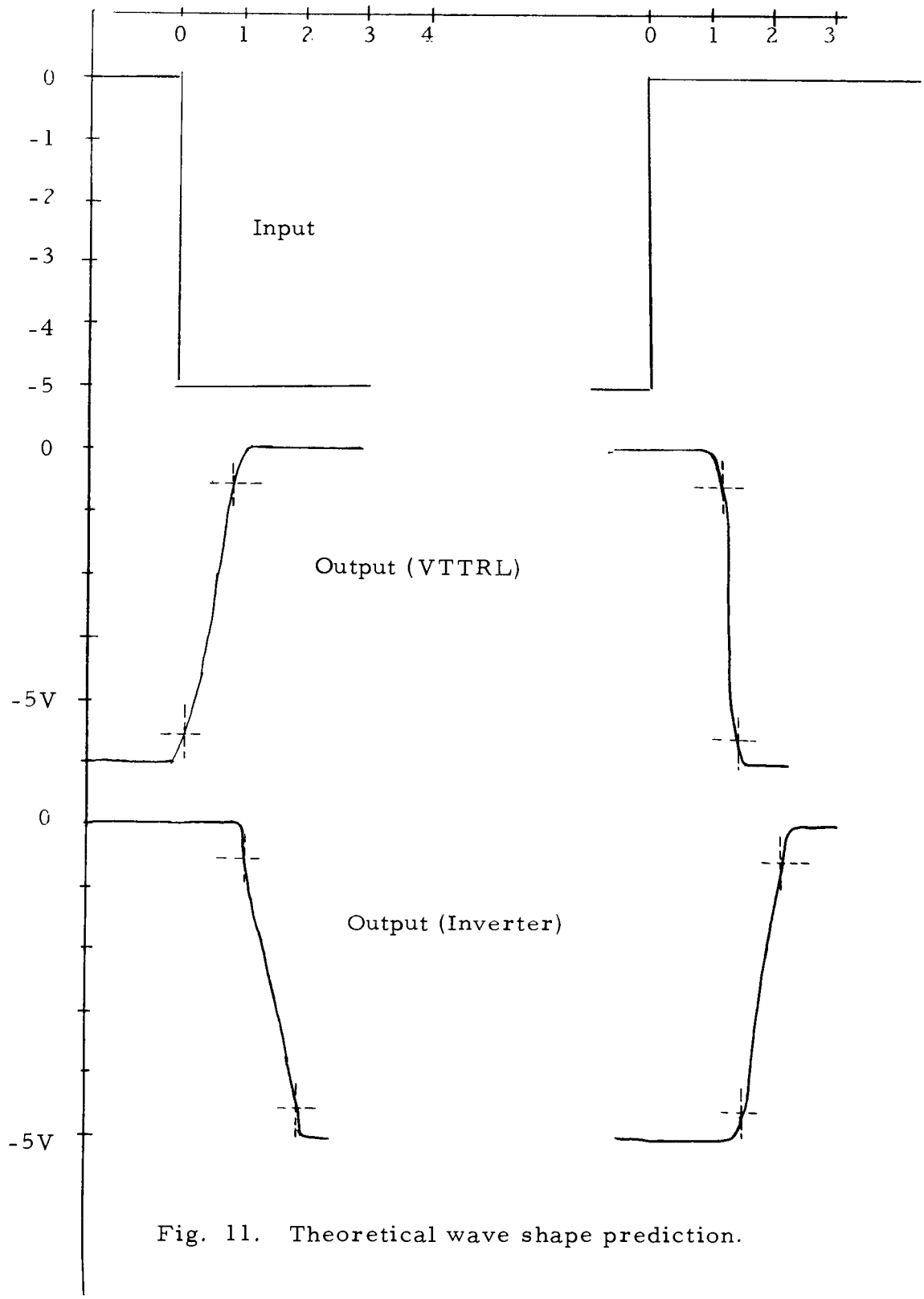


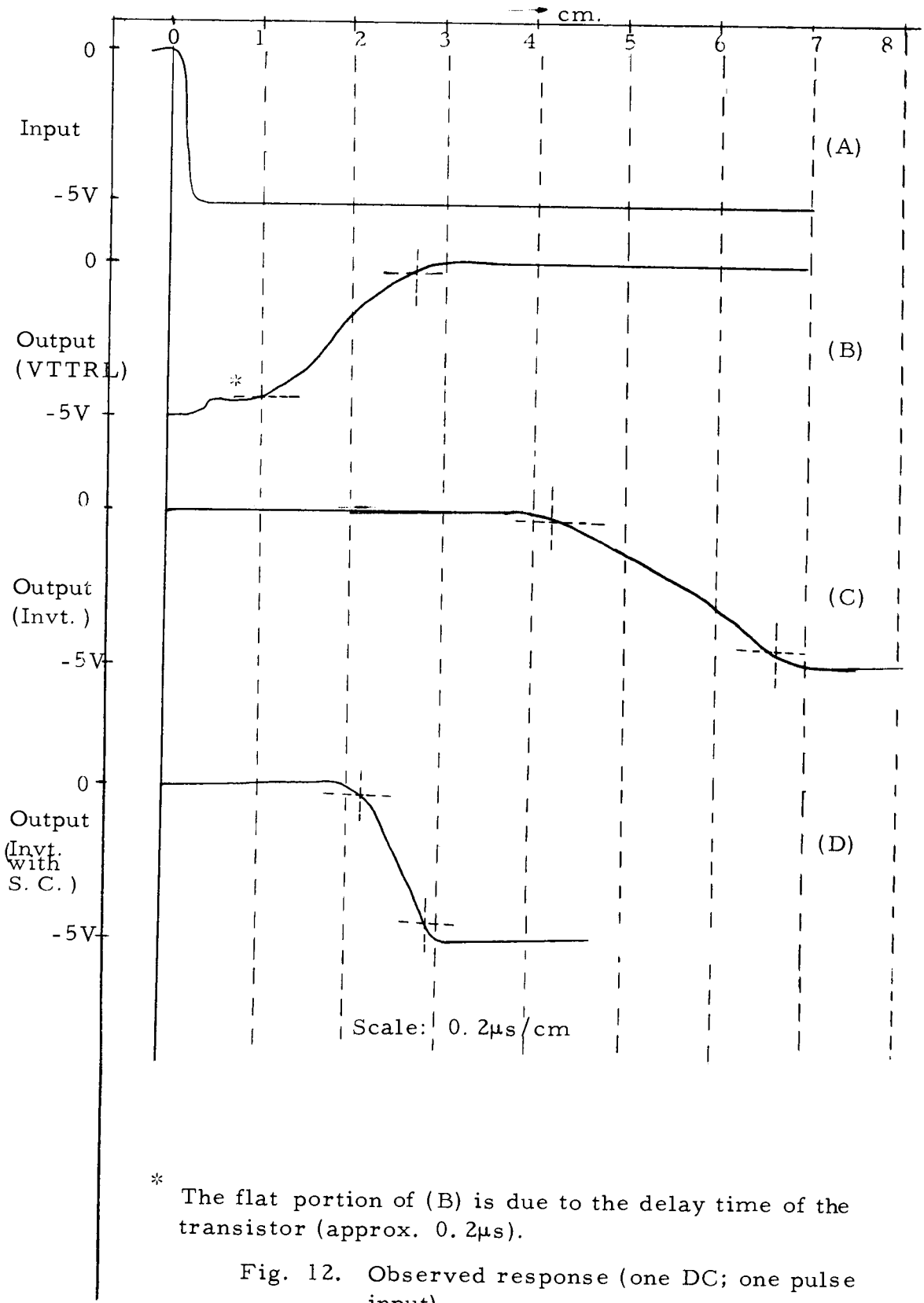
Fig. 11. Theoretical wave shape prediction.

Fig. 11 shows the expected worst-case wave-shape at the output of the inverter-stage without using speed-up capacitor.

In case of the output of the inverter, the calculated turn-OFF time is 1.60 μsec. The observed turn-OFF time is 1.20 μsec. Considering that the turn-on time of VTTRL is actually 0.60 μsec. compared to the worst-case turn-on time of 0.90 μsec., the observed and the calculated turn OFF times for the inverter stage are approximately equal. This implies that the $t_{storage}$ and t_{fall} of the inverter stage, both calculated and observed, are equal. The turn-OFF time is a maximum when two inputs are present in the VTTRL circuit.

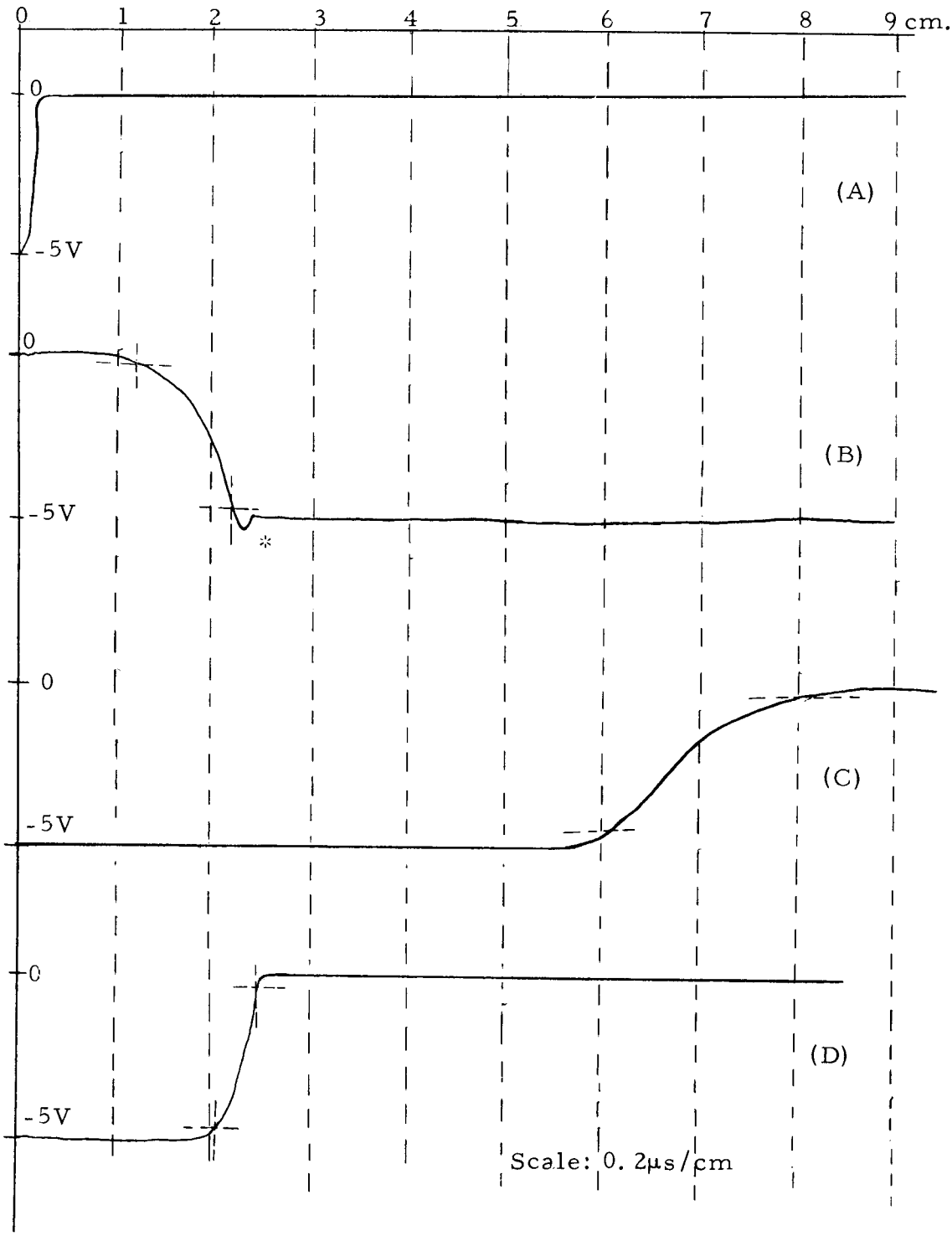
For the maximum turn-on time, consideration is given to the case (Figs. 14, 15) where all the three input are present in VTTRL. The calculated turn-ON time is 2.39 μsec for worst-case. This includes the rise-time of 0.90 μsec. for the inverter stage alone. It also includes the storage time of the VTTRL (Fig. 11), which for a typical case is much less than the maximum storage time of 1.11 μsec. Because of these two considerations, the maximum turn-on time observed is 1.40 μsec. as compared to the calculated value (2.39 μsec.).

The worst-case calculated total switching time is 4.0 μsec. The observed total switching time (maximum) is 2.3 μsec. The switching times for different samples of 2N1305 were observed. The total switching time varied from 2.20 to 2.50 μsec. Hence it can be concluded that the total switching time for this circuit, with the components used, can be assumed to be 60% of the worst-case switching time.



* The flat portion of (B) is due to the delay time of the transistor (approx. 0. 2μs).

Fig. 12. Observed response (one DC; one pulse input).



* Due to the steep fall time, the reasonable frequency of lead inductance and stray capacitance is reached giving rise to overshoot.

Fig. 13. Wave shapes for one D-C; one pulse input.

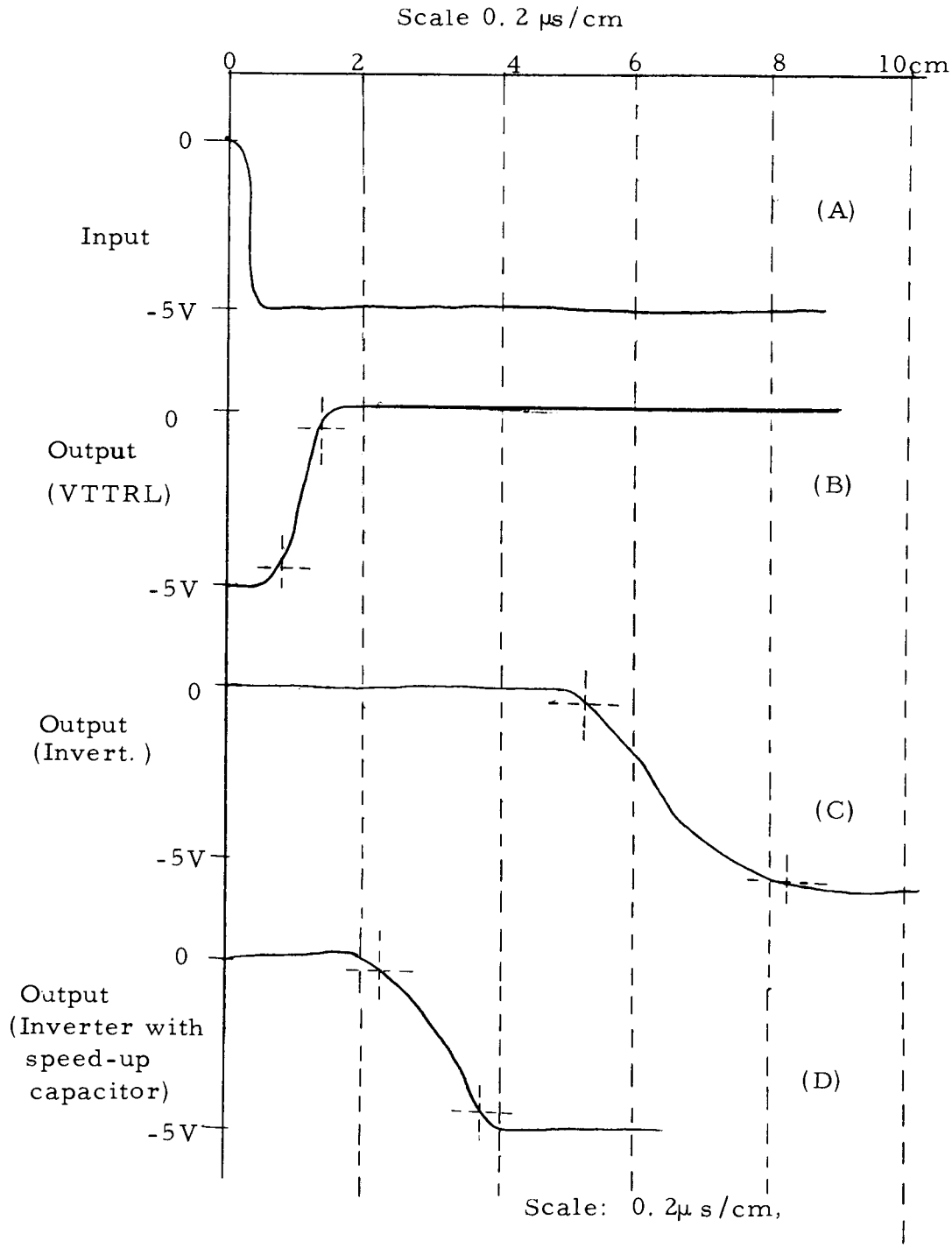


Fig. 14. One input D-C, two pulse inputs.

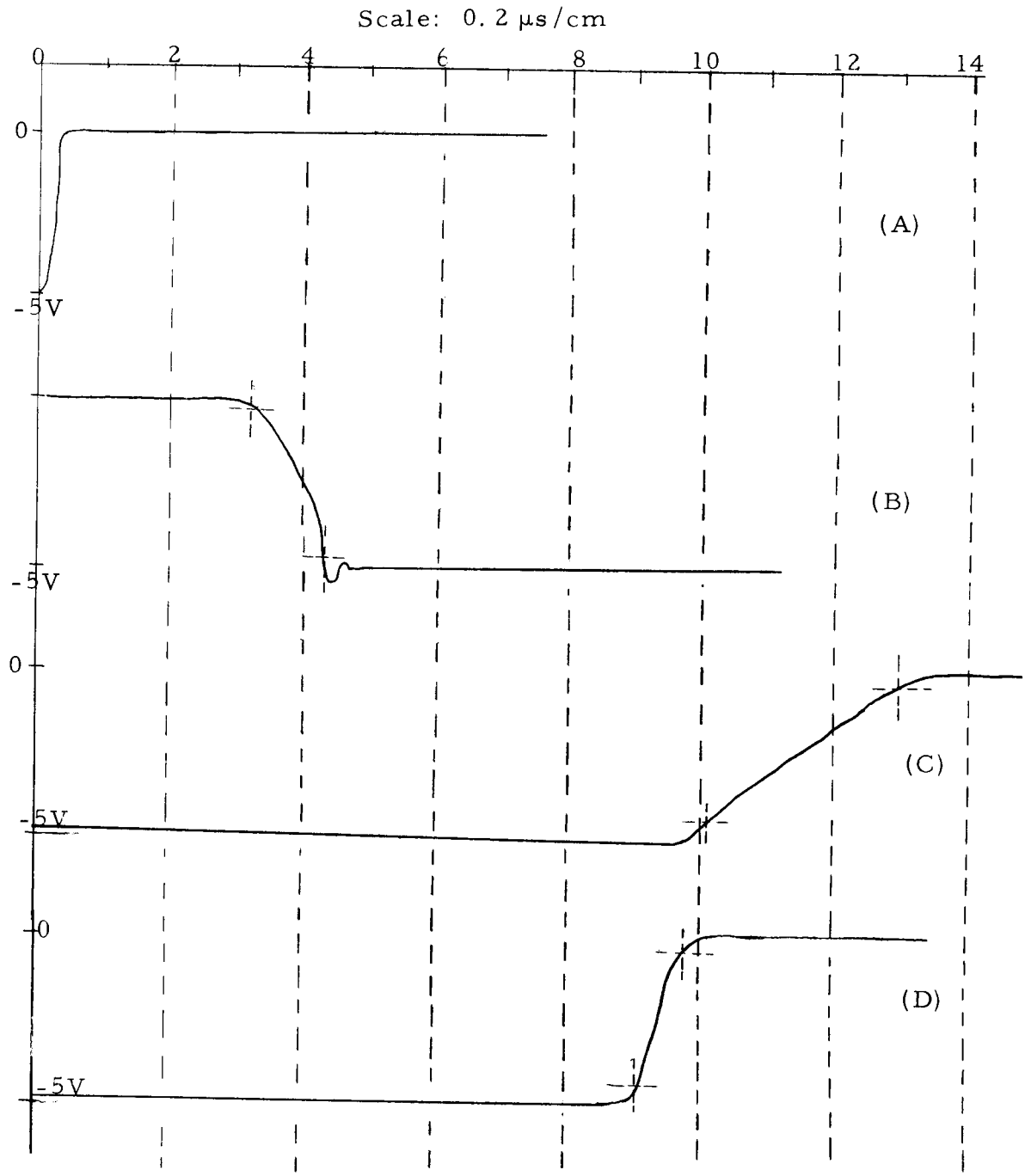


Fig. 15. One D-C input, two pulse inputs.

Transient Response Improvement Using Speed-Up Capacitor:

Typical base current (without C_T)

$$= \frac{5 - 0.35}{2.90} - \frac{15 + 0.35}{15}$$

$$= 1.60 - 1.02$$

$$(I_{b_1})_{\text{typ}} = 0.59 \text{ mA}$$

also,

$$(I_{b_1})_{*} = 0.30 \text{ mA}$$

In order to have a faster response, more turn-ON current must be supplied during transient conditions. This will automatically result in a high turn OFF current of opposite polarity during turn OFF period. Thus the total switching time will be reduced.

Observed switching time of the output at the inverter stage as a function of speed-up capacitor values is shown in Table VI.

Table VI. Switching times

Number	Speed-up Capacitor pf	t_d μs	t_r μs	t_f μs	t_f μs	t_{total} μs
1	-	0.40	0.60	0.80	0.30	2.10
2	100	0.40	0.20	0.65	0.30	1.55
3	250	0.40	0.15	0.50	0.20	1.25
4	400	0.40	0.15	0.50	0.20	1.25
5	500	0.40	0.15	0.50	0.20	1.25
6	1,000	0.40	0.10	0.40	0.20	1.10
7	1,500	0.40	0.10	0.40	0.20	1.10
8	3,000	0.50	0.10	0.35	0.20	1.15
9	10,000	0.50	0.10	0.35	0.20	1.15

C is chosen, equal to 1000pf. The total switching for this case 1.10 μs.

Current supplied by R_T = 1.60 mA. Assuming that the capacitor supplies 10mA of current in 0.5 μsec.

$$c = \frac{I \times \Delta t}{\Delta V} \tag{19}$$

For a constant base voltage during switching the voltage swing = 5V

$$C = \frac{10\times10^{-3}\times0.5\times10^{-6}}{5}$$

$$C = 0.001\ \mu F$$

The transient current supplied by C_T is assumed to be 6 times that supplied by R_T.

The observed values of Turn ON and Turn OFF times are 0.50 and 0.60 μ sec respectively.

Hence by the use of the speed-up capacitor, the total switching time of the combined VTTRL is made 1.40 μ sec (max.) which is comparable to the switching time of only the VTTRL stage.

The calculation of the exact value of speed-up capacitor is not possible. Therefore a table (table VI) of switching time, using various values of speed-up capacitor was drawn. It also gave $C_T = 0.001\ \mu F$ as the speed-up capacitor giving minimum switching time.

It can thus be concluded that the use of the speed-up capacitor in the input of the inverter-stage helps in reducing the switching time of the combined VTTRL-Inverter circuit, to that of an VTTRL circuit alone. The total switching time is comparable to the switching time of the transistor alone.

Effect of base current on switching time: Figs. 12, 13, 14, and 15 show the transient response of the VTTRL-Invert circuit.

In Figs. 12 and 13, one pulse and one D-C input are present. This results in a minimum base current, which makes the turn-on time, large and the storage time, short.

In Figs. 14 and 15, one D-C. and two pulse inputs are present. This results in a maximum base current, which makes the turn on time, short and the storage time, large.

The fall time which depends on the turn-off current remains almost the same in both cases.

The total switching-time also remains the same because increased turn-on time results in a decreased storage-time and vice-versa.

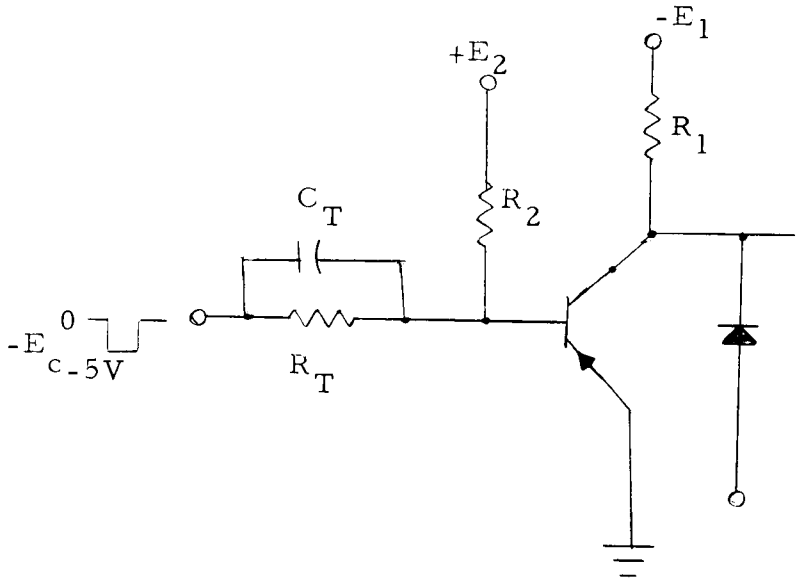


Fig. 16. Transient response improvement using speed-up capacitors (INVT).

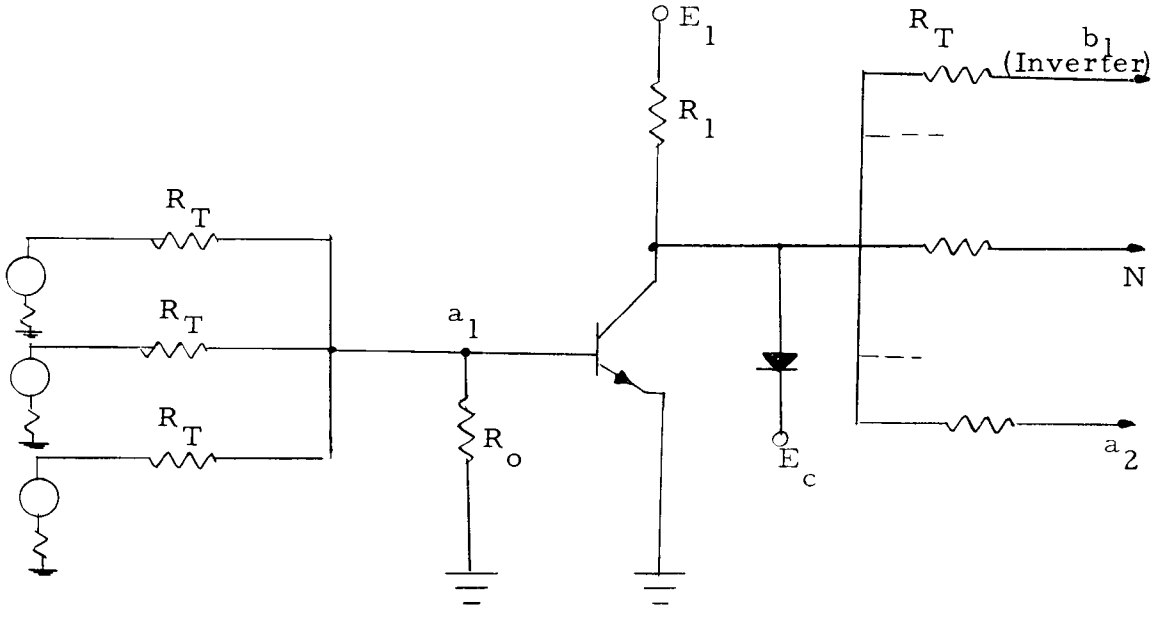


Fig. 17. Variable threshold logic circuit.

PART III

CIRCUIT # 2

Variable Threshold Logic (Fig. 17) (4)

Here the transistor is kept forward-biased both in the worst-case-OFF and worst-case-ON conditions. The input resistors (R_T) act as Kirchoff's adder, supply a definite input current for one, two, or three inputs, (E_c volts).

The base-emitter junction forward-voltage, when the transistor is OFF is determined by the small resistance R_o. During the OFF state, all the current supplied by the input transfer-resistors passes through R_o. The base-emitter junction voltage is determined by the amount of current passing through R_o and the value of R_o. The base-emitter-junction voltage should not exceed the minimum base turn-ON voltage for the transistor used. In practice, this voltage is kept much below the turn-on base voltage for the transistor.

For the turn-on condition, the base-emitter-junction voltage should exceed the minimum base turn-on voltage, and there should be sufficient current in the base-junction to saturate the transistor.

In this particular circuit, the fan-in is three. Two of the three inputs are required to saturate the transistor.

Important Parameters

$(V_{bo})^*$: Maximum base-OFF Voltage

Since in this case the base voltage is kept forward-biased with respect to the base-emitter junction, it should not exceed the minimum base turn-on voltage. Since the minimum base-on voltage is not a well-defined parameter, the maximum base-off voltage is kept much below the minimum base turn-on voltage under worst-case conditions.

$(V_{bs_1}')^*$: Maximum Base Turn-ON Voltage

During the turn-on condition, the current supplied by the transfer-resistors is divided between the base-emitter junction diode and R_o. The higher the base voltage, the more current will be taken by R_o. Under the worst-case conditions, there should be enough current through the base-emitter junction to saturate the transistor.

$(V_{cs})^*$:
$(I_c')^*$
$(h_{fe})^*$

} discussed in VTTRL circuit

$(I_{co})^*$: Maximum Transistor Leakage Current

In this circuit there is no back biasing voltage to nullify the effect of leakage current. Hence the maximum leakage current should be very small.

However, it is assumed that the transistors used in this circuit have a high base turn-ON voltage. Also, there is a small resistance (R_o) in parallel with the base-emitter junction.

Because of these two reasons, the effect of leakage current in forward biasing the base-emitter junction and turning ON the transistor when it should be OFF is negligible.

It is however inferred that the transistors having a high base turn-ON voltage have a low leakage current. Hence the effect of leakage current can be neglected in this circuit.

Selection of a Transistor for VTL Circuit

The most important parameter in the steady-state, worst-case design of the VTL is the minimum base turn-on voltage.

Since the transistor is not back-biased during the OFF period, the base turn-on voltage has to be sufficiently high (greater than 0. 70 V), in order to have an adequate separation between the ON and OFF conditions in the base circuit.

Due to the use of the small resistance (R_o) in the base circuit,

Table VII-A. 2N 2713 NPN silicon epitaxial transistor characteristics

Absolute maximum ratings				
Voltage				
Collector emitter	V_{CEO}			18V
Emitter to base	V_{EBU}			5V
Collector to base	V_{CBO}			18V
Current (collector)	I_C			200mA
Power dissipation	P_T(25°C)			200mW
	P_T(55°C)			120mW
Derate 2.67mW/°C increase above 25°C				
Electrical characteristics	(25°C)	MIN	TYP	MAX
Forward current transfer ratio (V_{CE} = 4.5V, I_C = 50 mA)	h_{fe}	30	60	90
Collector-emitter saturation voltage (I_C = 50mA I_B = 3mA)	V_{CE}			0.3V
Base-emitter saturation voltage (I_C = 15, I_B =)		0.7	0.9	
Cut off: collector current	I_{CBO} (25°C)			1.5 μA
	150°C			15 μA
Input impedance	h_{fe}		200 ohms	

Switching times

t_d = 60nsec, t_r = 85nsec, t_s = 85nsec, t_f = 40nsec

I_{B_1} = 3 mA

I_{B_2} = 3.84 mA

Table VII-B. Pre-assigned parameters

M	3
L	2
$(V_{cs})^*$	0.3V
$(V_{bs_1}')^*$	0.90V
$(V_{bo})^*$	0.45V
I_c'	15mA
$(I_{bs})^*$	15/30 = 0.50mA
$(h_{fe})^*$	30
$(\rho)^* = (I_{b_1})^*/(I_{bs})^*$	1.2
$(I_{b_1})^*$	0.60mA
$(I_o)^*$	0.01mA (75°C)
$(V_{cs})^*$	0.01V
$(I_{rc})^*$	0.05mA
ν_c	0.1 volts
$V_{bs(3)}'$	1.0 volts
E_1	+12V
E_2	-12V
E_C	+6V

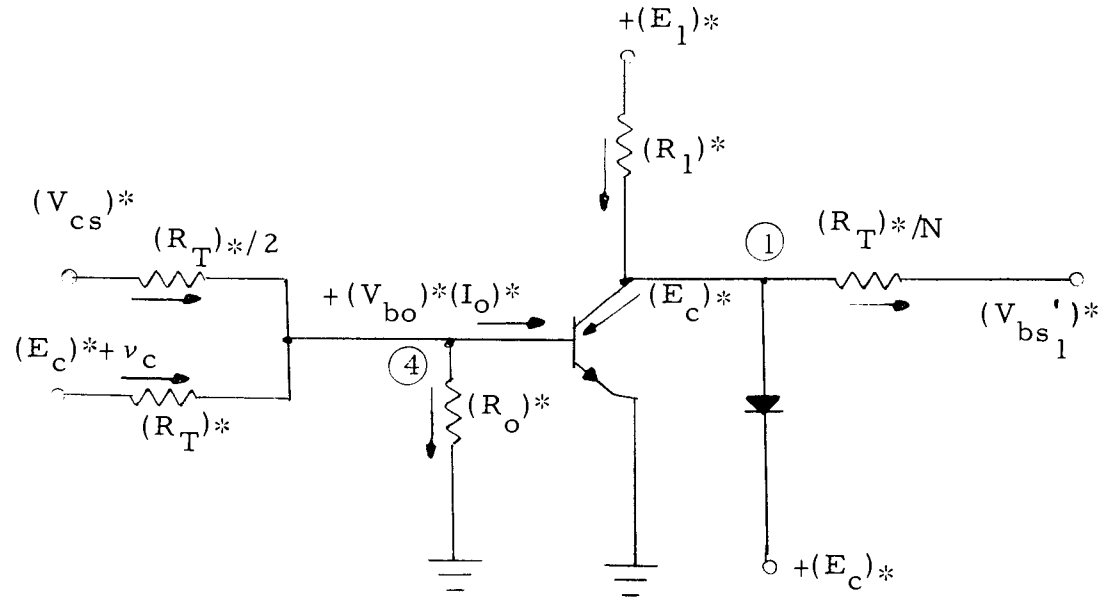


Fig. 18-A. Worst-case OFF condition.

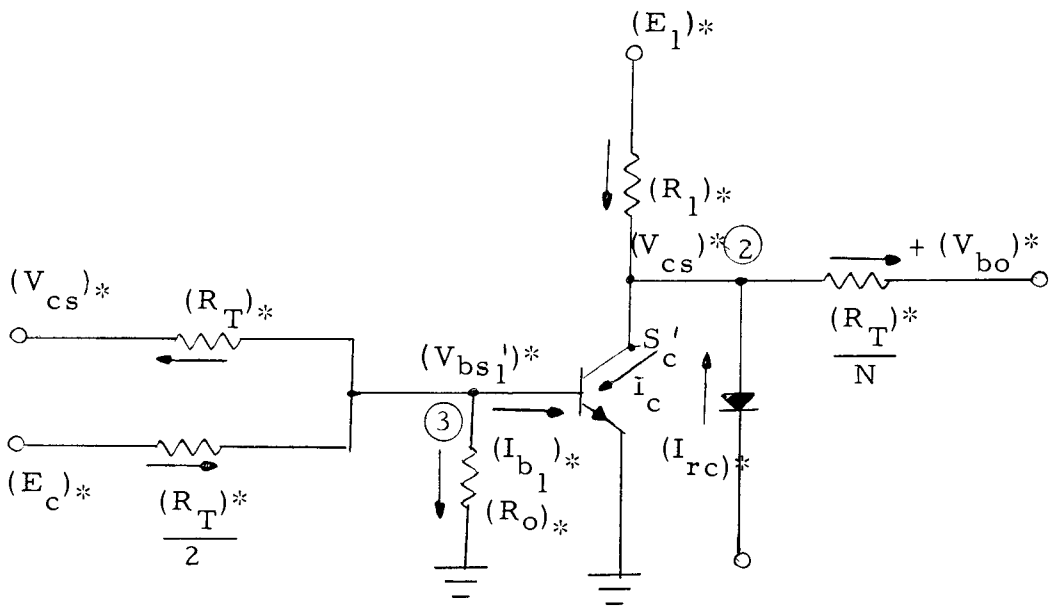


Fig. 18-B. Worst-case ON condition.

the effect of the leakage-current (I_{co}) is negligible.

The other parameter that is very important in the design is $(h_{fe})_*$. Also, for a particular transistor, $(h_{fe})_{min}$ should not fall below $(h_{fe})_*$ throughout the working life of the transistor.

A NPN 2N 2713 epitaxial silicon transistor was chosen for realizing this circuit.

A 1N 50 clamping diode was used for clamping the output voltage.

Fig. 18-A. Worst-case, OFF Condition

Node (1)

$$(I_o)^* = \frac{((E_c)^* + V_c - (V_{bo})^*)}{(R_T)^*} + \frac{((V_{cs})^* - (V_{bo})^*)}{(R_T)^*/2} - \frac{(V_{bo})^*}{(R_o)^*} \quad (20)$$

In order that the transistor remains off,

$$(I_o)^* = 0.$$

Node (4)

$$\frac{((E_1)_* - (E_c)_*)}{(R_1)^*} = (I_{co})^* + \frac{((E_c)_* - (V_{bs'_1})^*) \times N}{(R_T)^*} \quad (21)$$

The values of the circuit parameters used in this circuit are such as to turn the transistor ON. The collectors of the two preceding ON stages are assumed to be at their maximum value and so is

the clamping voltage (E_c) of the preceding OFF stage. The values of the transfer resistors (R_T) are assumed to be minimum. The base-emitter junction voltage is assumed to be at its maximum allowable limit. The small resistance (R_o) is assumed to be at its maximum limit so that it takes least current. Under these circumstances it is assumed that the transistor is an open-circuit, and th[illegible] is no current passing through the base-emitter junction.

Worst-Case ON Condition (Fig. 18-B) (Node 2)

The conditions are similar to that discussed for VTTRL collector circuit.

The node equation is

$$(I_c') = (I_{Rc})^* + \frac{((E_1)_* - (V_{cs})^*)}{(R_1)_*} - \frac{((V_{bo})^* - (V_{cs})^*)}{(R_T)^*/N} \quad (22$$

Node (3)

$$\frac{((E_c)_* - (Vbs_1')^*)}{(R_T)^*/2} = \frac{((V_{bs_1}')^* - (V_{cs})_*)}{(R_T)_*} + (I_{b_1})_* + \frac{(V_{bs_1}')^*}{(R_o)_*} \quad (2$$

In the base circuit (node 3), two of the inputs are present ($+E_c$ volts), and one of the inputs is absent (approx. zero volts). In this case, a forward current of enough magnitude to saturate the transistor, has to be supplied to the base-emitter junction by the two inputs that are present. It must also supply additional current to (R_o), in order to keep the base-emitter junction at the

minimum base turn-on voltage, and a small current to one of the inputs that is absent (zero volts). Hence the clamping voltage (E_c) is assumed to be a minimum, and the transfer-resistors for the two inputs, that are present, are assumed to be at their maximum value. The base-on voltage is assumed to be at its maximum value, so that the difference in input and base-on voltage is a minimum, resulting in the least input current. The transfer-resistor of the remaining input is assumed to be a minimum, so that it takes a maximum current.

Solving equations (20) and (23) for the worst-case OFF and worst-case ON conditions at the base-emitter junction, the two equations are,

$$R_{T_{max}} = f(R_o) = 9.79/(0.60+0.70/R_o) \tag{24}$$

$$R_{T_{min}} = f(R_o) = 11.72\,R_o \tag{25}$$

The values of $R_{T_{min}}$ and $R_{T_{max}}$ for various values of R_o are tabulated (table VIII), and plotted (Fig. 19).

From the plot, a value of R_o and R_T is chosen to obtain a maximum tolerance limit for R_T and R_o (table IX).

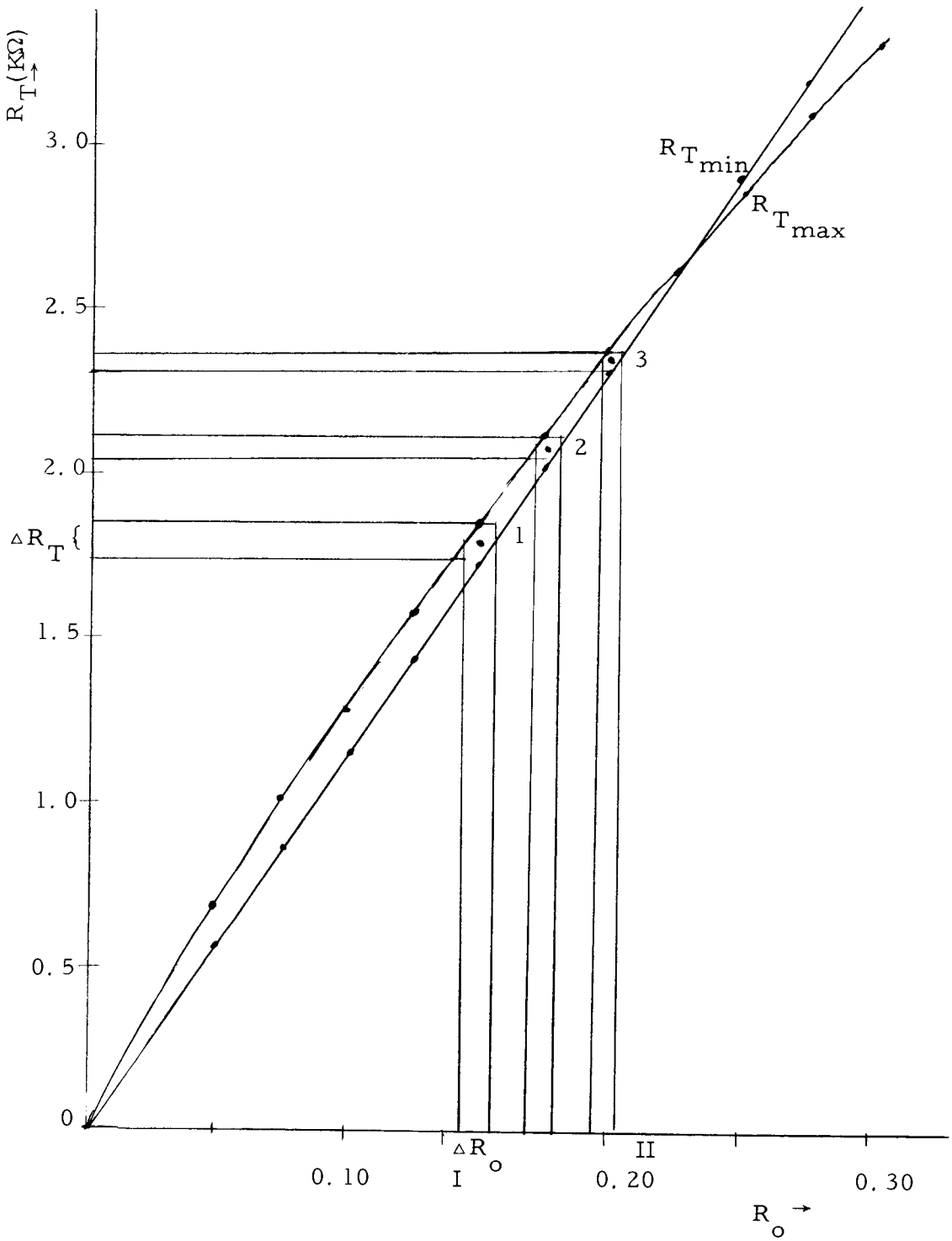


Fig. 19. Tolerance of R_T and R_o.

Table VIII. R_T v/s R_o

Number	R_o KΩ	$R_{T_{min}}$ KΩ	$R_{T_{max}}$ KΩ	$R_{T_{max}} - R_{T_{min}}$ KΩ
1	0.050	0.586	0.670	.084
2	0.100	1.172	1.290	0.118
3	0.125	1.465	1.580	0.115
4	0.150	1.758	1.860	0.102
5	0.175	2.051	2.120	0.069
6	0.200	2.344	2.380	0.036
7	0.225	2.637	2.630	-0.007
8	0.250	2.930	2.880	-0.050
9	0.275	3.223	3.100	-0.113
10	0.300	3.516	3.330	-0.186

Though the tolerance limits for lower values of R_T and R_o are more, choosing a low value of R_T will increase interactions between various input.

Table IX. Circuit parameter tolerances

Point on Fig. 19	R_o ohms	Permissible tolerance of R_o %	R_T K Ω	Permissible tolerance of R_T	N_{max}	Permissible N
1	147	4.75	1.800	2.77	2.72	2.0
2	175	3.60	2.085	1.68	3.30	3.0
3	200	2.50	2.360	0.96	3.64	3.0

Hence VTL circuit with

$$\left.\begin{aligned} R_T &= 2.085 \pm 1\%\ K\Omega \\ R_o &= 175 \pm 3\%\ \text{ohms} \\ R_1 &= 0.775 \pm 3\%\ K\Omega \\ N_{max} &= 3 \\ E_1 &= 12 \pm 1\% \\ E_c &= 6V \pm 1\% \end{aligned}\right\}$$

is chosen.

As the oscilloscope amplitude calibration is accurate to ± 3%, it was impossible to obtained the required ± 1% voltage tolerance. The increased voltage-tolerance was, however balanced by reducing the tolerance of R_T and R_o to ±1%. The value of R_o was especially very critical in the working of VTL circuit. Voltage-levels were adjusted to less than ± 1% using precision D. C. voltmeter and D. C. inputs. It was observed that under typical conditions, the circuit

worked with about ± 3% voltage tolerance. However, in a worst-case condition, ±1% voltage tolerance will be required.

Maximum Power Dissipation

$$P_{max(ON)} = \frac{(E_1^2)^*}{(R_1)_*} \tag{26}$$

$$P_{max(OFF)} = \frac{(E_1)^*}{(R_1)_*}\left((E_1)^* - (E_c)_* - N\frac{((E_c)^2_*)}{(R_T)^*}\right) \tag{27}$$

$$\left.\begin{aligned} P_{max(ON)} &= 200 \text{ mW} \\ P_{max(OFF)} &= 67.4 \text{ mW} \end{aligned}\right\}$$

Due to the absence of the back-biasing current source (E_2-R_2), the power dissipation of an off transistor is comparatively small. This is one of the important advantages of this circuit.

Transient Response

Some additional parameters have to be determined in order to predict the transient response.

(1) Maximum base-ON current: (Fig. 20)

Here the base-voltage is assumed to be the maximum (all the three inputs are present). The value of the transfer-resistors is a minimum. The value of R_o is at its maximum. $(I_{bm})^*$ is calculated from the base node equation (28).

$$(I_{bm})^* = \frac{3((V_{co})^* - V_{bs'(3)})}{(R_T)_*} - \frac{(V_{bs'(3)})}{(R_o)^*} \tag{28}$$

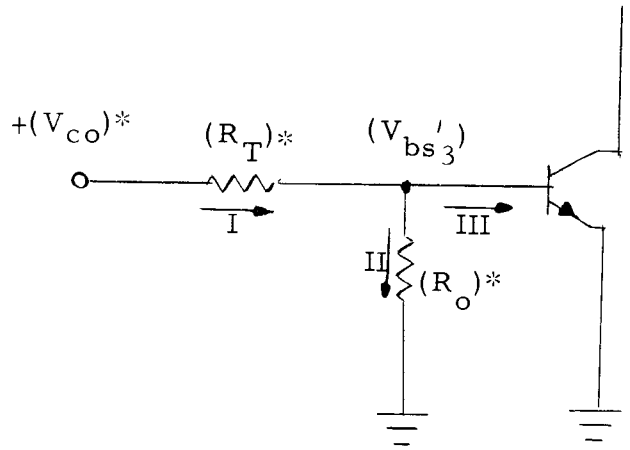


Fig. 20. Maximum base ON current.

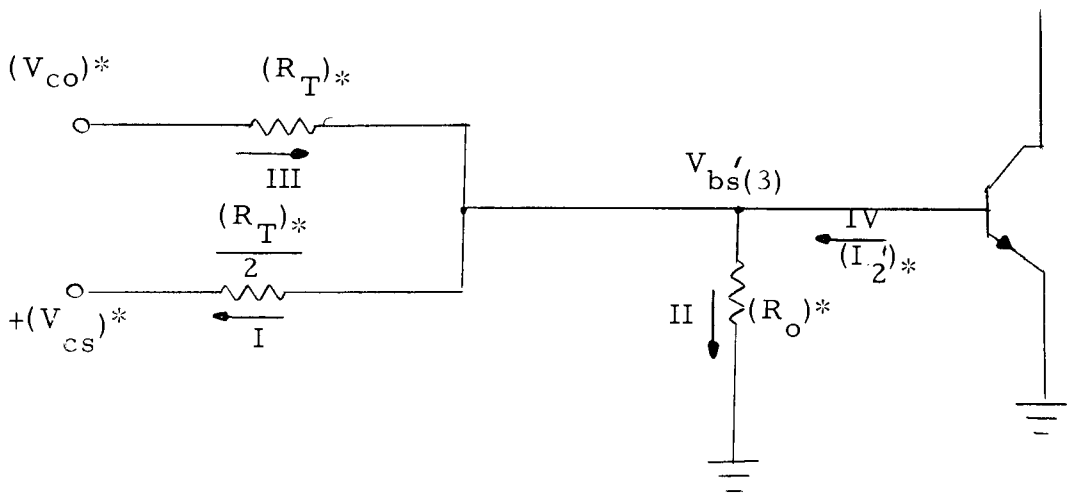


Fig. 21. Minimum available Turn-OFF current.

(2) Minimum Available Turn-OFF current (Fig. 21)

This current is calculated immediately following $(I_{bm})^*$ Hence the base voltage is assured to be $V_{bs'(3)}$. Under these conditions the current going out of the node through R_o, and preceding ON stage is larger than the current flowing into the node due to the preceding OFF stage. This results in a transient back-biased current flow into the base emitter junction.

$$-(I_2')_* = \frac{((V_{co})^* - V_{bs'(3)})}{(R_T)_*} - \frac{V_{bs'(3)}}{(R_o)^*} - \frac{(V_{bs'(3)} - (V_{cs})^*)}{(R_T)_*/2} \qquad (29)$$

From the present calculations, it appears that the turn-OFF current is not reduced very much because of the absence of the back-biasing current source. The small grounded resistance (R_o) supplies enough base turn-OFF current.

Design of the Inverter Circuit

The design of the inverter-circuit for VTL will be similar to that for VTTRL. A back-biasing current source $(E_2\text{-}R_2)$ is necessary to limit the base current in the Inverter. The circuit diagrams and the node equations are similar to those for the Inverter circuit previously designed, and are therefore, not repeated.

The values obtained are:

$$R_T = 2.085 \pm 1\% \text{ K}$$

$$(R_2)_{max} = 54\ K$$

$$(R_2)_{min} = 7.45\ K$$

$$(R_2)_{chosen} = 7.75\ K \pm 5\%$$

$$R_1 = 820\ ohms$$

$$N_{max} = 2.62$$

$$(N_{max})_{permissible} = 2.0$$

R_2 is chosen close to $(R_2)_{min}$ in order to avoid large base turn-on current.

Transient Response

The calculated values of the minimum base turn-OFF current $(I_2')_*$ and the maximum base-ON current $(I_{bm})^*$ are:

(1) For test circuit (I_c = 50 mA)

$$(I_{bm})^* = 3\ mA$$

$$(I_2') = 3.84\ mA$$

(2) For VTL circuit (I_c = 15 mA)

$$(I_{bm})^* = 4.55\ mA$$

$$(I_2')_* = 1.80\ mA$$

(3) For Inverter circuit (I_c = 15 mA)

$$(I_{bm})^* = 1.07\ mA$$

$$(I_2')_* = 1.05\ mA$$

Using the switching equations of Appendix I and the above values, the worst-case switching times for the designed VTL and inverter circuits are calculated. They are shown in table IX.

Figs. 22 and 23 indicate the observed wave shapes. The speed-up capacitor (0.001 μF) improves the performance of the circuit considerably.

Fig. 24 indicates the tolerances of the base voltage for one, two and three inputs.

The comparison of the calculated and observed switching-times is shown in table X.

For the VTL circuit, the worst-case total switching time is 625 nsec. the observed total switching time for

(1) one D. C., one pulse input is 430 n secs

(2) one D. C., two pulse inputs is 510 nsecs

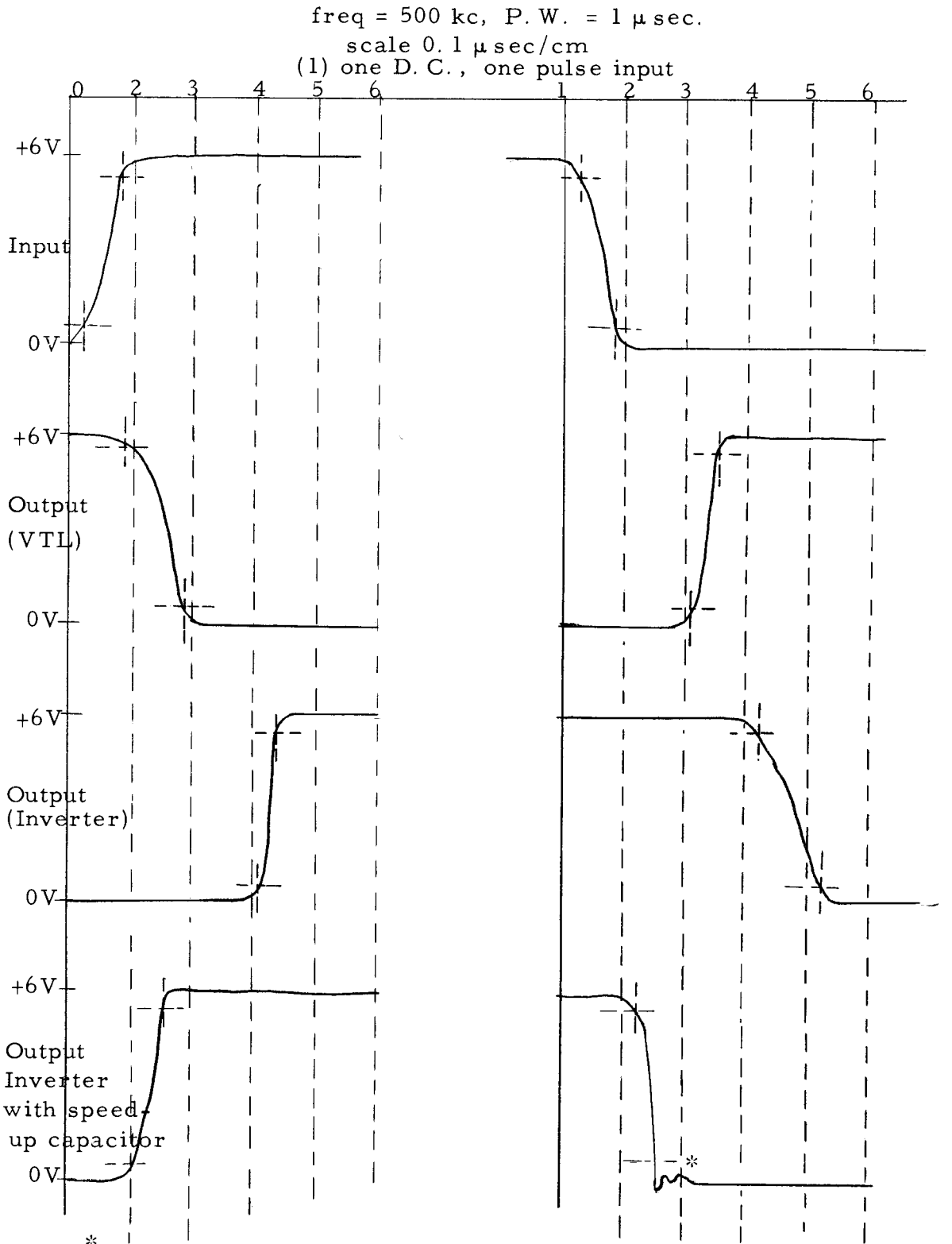
Because the Data-Pulse has 50 nsecs of rise and 50 nsecs of fall time, the observed switching times are longer than they would be if a step-input pulse was used.

Rise-time. The observed rise-time (maximum) for one D. C. and one pulse-input is 100 n secs. The calculated maximum is 145 n secs. This difference is due to a larger turn-on current compared to the worst-case value.

Storage-time. The observed storage time (maximum) for one D.C. and two pulse inputs is 370 n secs. The calculated value is

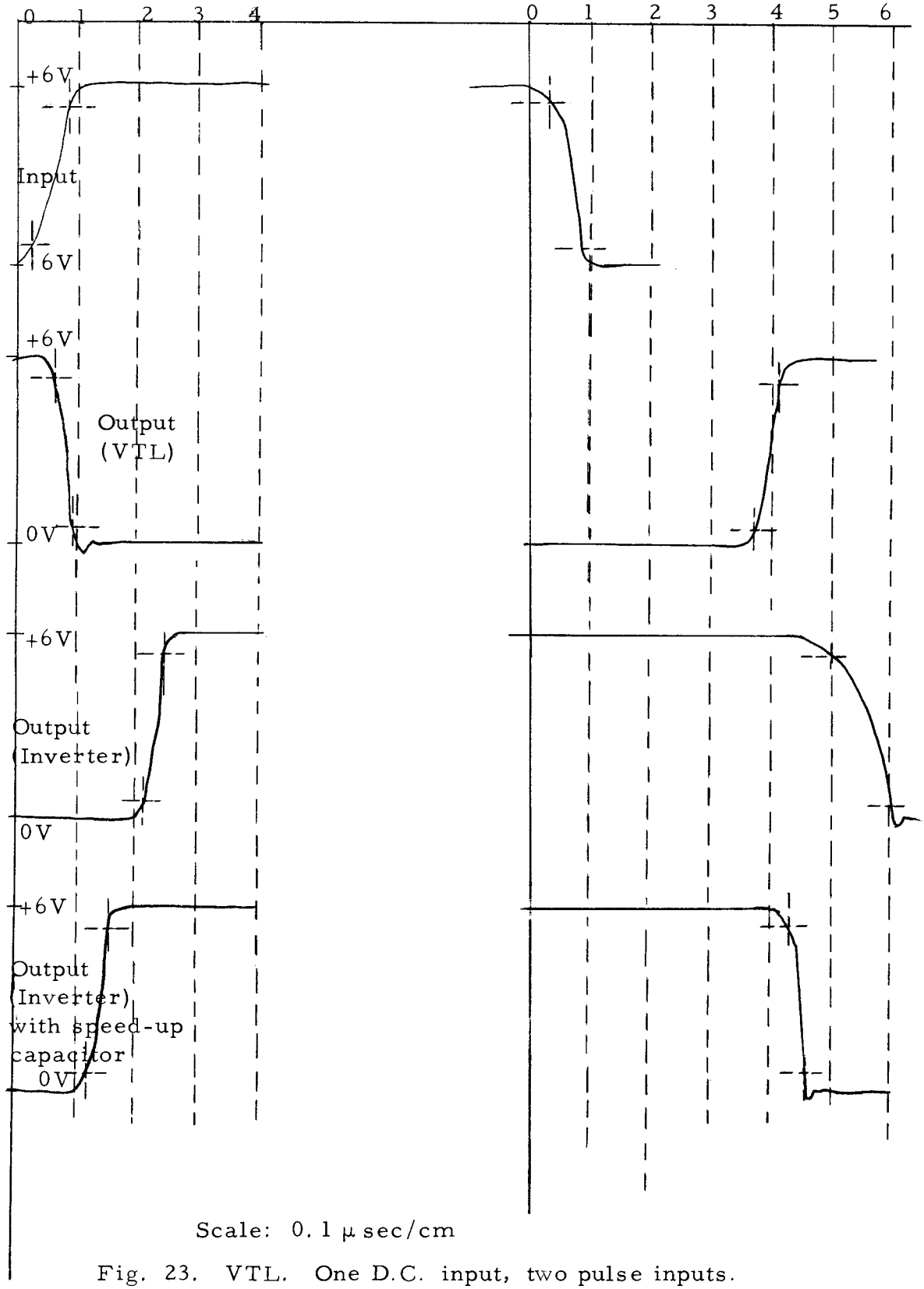
Table X. Comparison of switching times

	t_d ns	t_r ns	t_s ns	t_f ns	t_{total} ns	Type of Wave-shape
	60	145	370	36	625	Calculated VTL output for step-input
	60	145	150	50	405	Calculated Inverter output for step-input
	-	50	-	50		Pulse input (from data-pulse pulse generator
one D. C., one pulse input	80	100	200	50	430	VTL output (obs)
	320	110	310	40	780	Inverter output
	120	20	100	50	290	Inverter output with 0.001 μF speed-up capacitor
one D. C. two pulse inputs	60	40	370	40	510	VTL output (obs.)
	500	100	210	40	850	Inverter output
	425	25	120	30	600	Inverter output with 0.001 μF speed-up capacitor



*Overshoot is caused due to the resonance frequency of lead inductance and stray capacitance which coincides with the operating frequency of the circuit when the rise or fall time become very small.

Fig. 22. VTL circuit wave shapes.



Scale: 0.1 μ sec/cm

Fig. 23. VTL. One D.C. input, two pulse inputs.

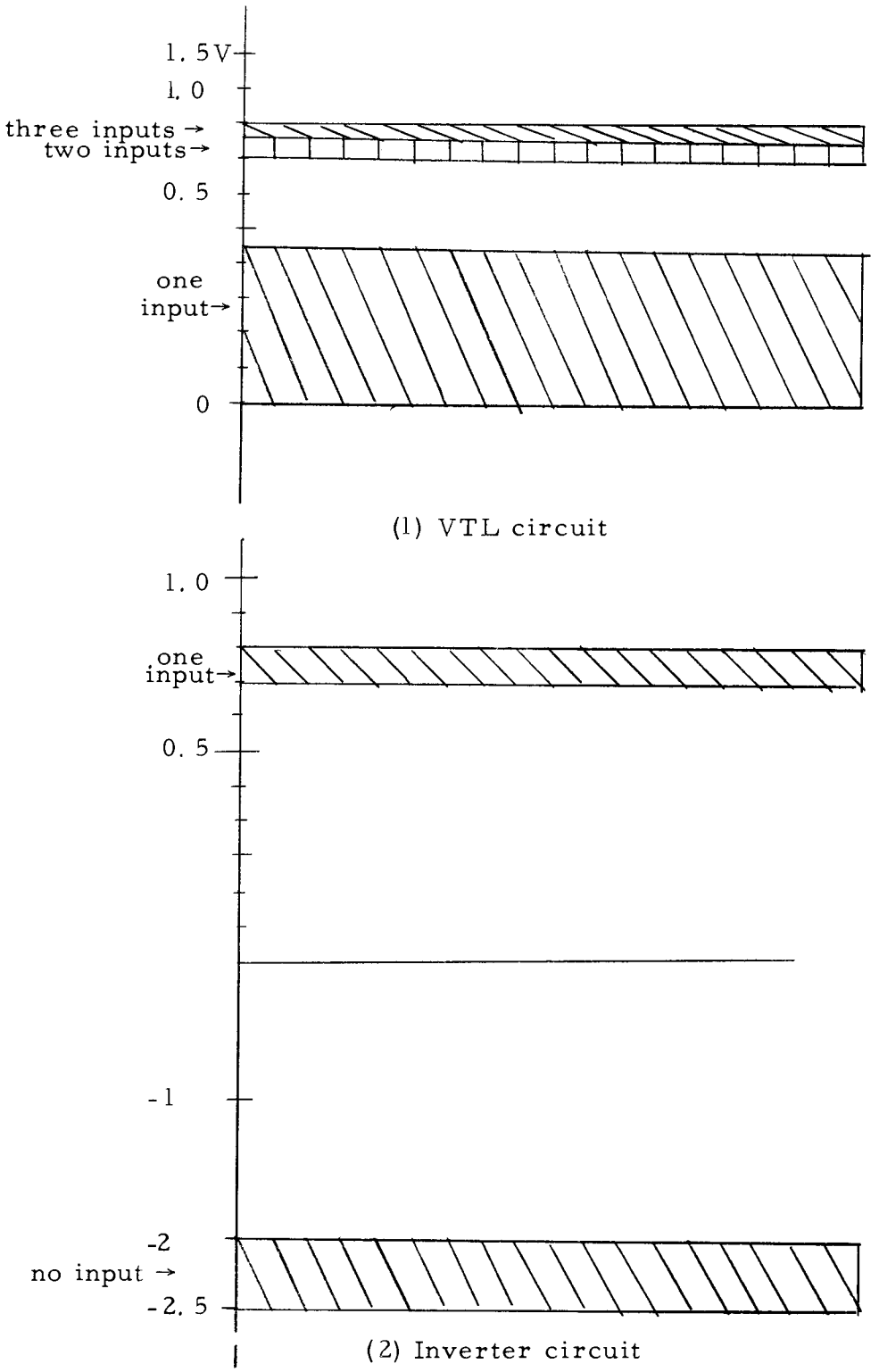


Fig. 24. Base voltage variations.

370 n secs. This is because the worst case and the typical maximum ON currents are approximately equal in this circuit.

Fall-time. The observed and (for the same collector current) the calculated fall times are equal (50 n secs) because the turn OFF current in the two cases is almost identical (for the same collector current).

The total maximum switching time (510 nsecs) is larger compared to the test circuit value (270 nsec.). The increase is mainly due to increased rise-time (about two times) and increased storage time (about four times). The rise-time increase is due to the smaller minimum turn ON current. The storage time increase is due to a larger maximum turn-on current.

PART IV

CIRCUIT #3 (4)

Transistor Tunnel-Diode Resistor Logic (TTDRL)

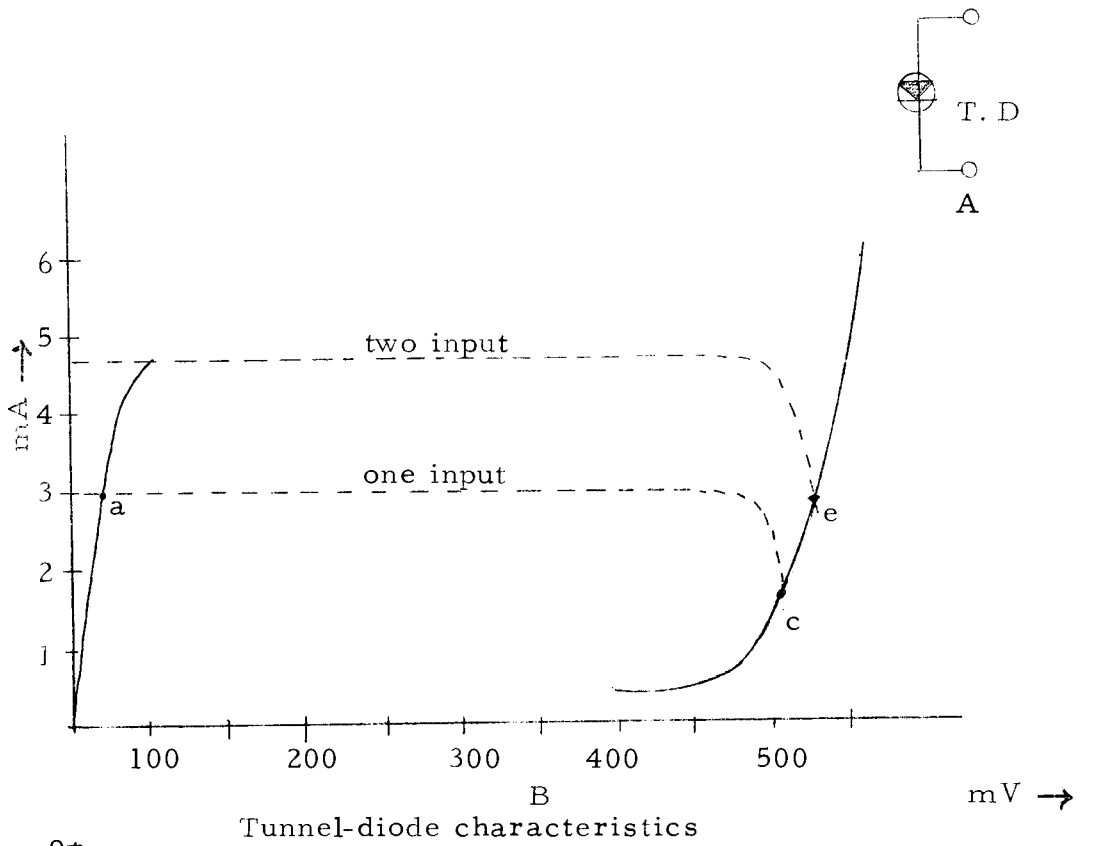
The design of the VTTRL and VTL is mainly based on the threshold-effect. A minimum base-ON voltage and a minimum base-on current is required to turn the transistor ON. By using a back-biasing current source (E_2-R_2) in VTTRL, and by using a small resistance (R_o) in VTL, the parameters of the circuit are so chosen as to keep the transistor OFF with one input present (equal to $-E_c$ volts) and just turn it on with two of the tree inputs.

The thresholding effect can be enhanced (4) by the use of a Tunnel-Diode in the base of the transistor.

However a number of problems have to be solved before the use of the tunnel diode in this circuit is justified. The problems are:

1. The peak current of an ordinary tunnel-diode varies by almost ±10%. The best tunnel-diodes available have a peak current tolerance of ±2.5%.

2. (Fig. 24-B) represents the characteristics of the base-emitter junction of a transistor superimposed on the tunnel-diode characteristics, assuming that no back-biasing current source is



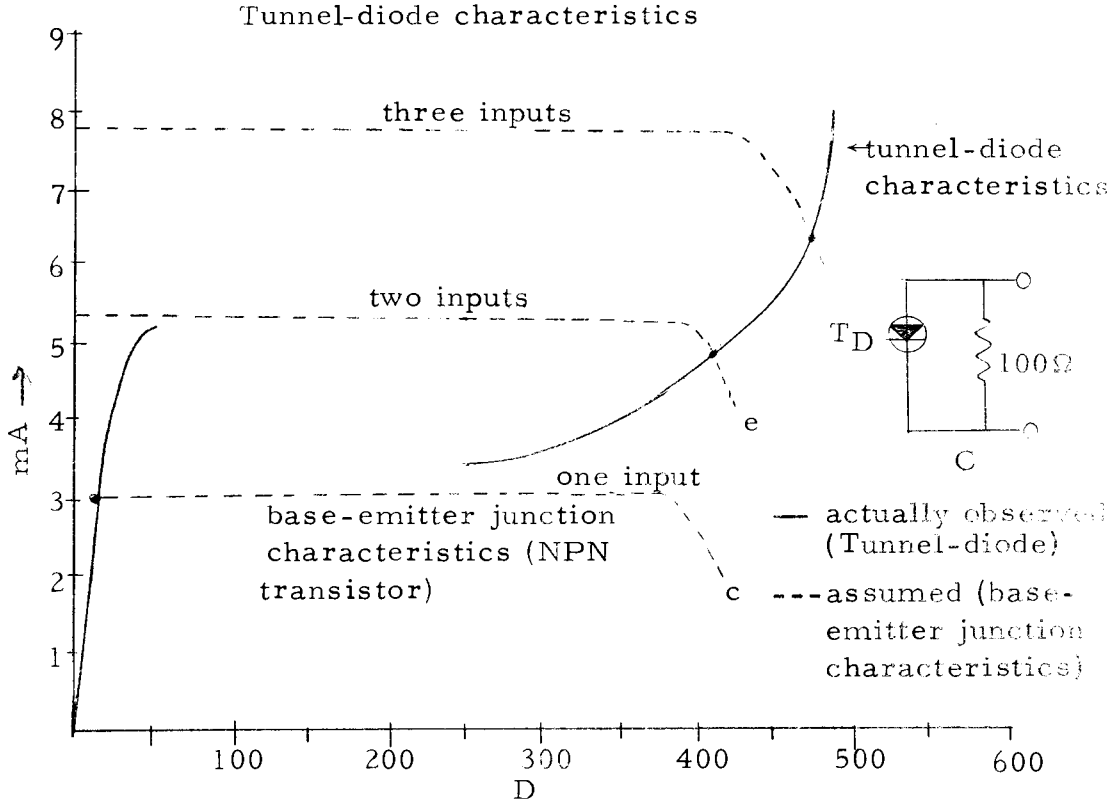


Fig. 24. Tunnel-diode characteristics (with 100 ohms parallel resistor).

applied in the base circuit. Upon applying one input, the stable points are (a) and (c). Since the tunnel-diode is at its low voltage state, the stable point is therefore, (a) in this case.

Upon applying two inputs, the peak current point of the tunnel-diode characteristics is just reached and now the stable point is (e) in the high voltage region. Due to the high voltage, the base-emitter junction of the transistor is forward biased. If sufficient current is pumped into the base-emitter junction, the transistor turns ON.

However, upon removing one of the two inputs, the stable point is (c) in the high voltage region, which keeps the transistor ON.

(3) When the tunnel-diode is in the high voltage state, the stable points (e or c) are such that the tunnel diode takes very small current, thus deeply saturating the transistor. This results in an increased storage time for the transistor.

Possible Solutions

(1) In order for the tunnel-diode to return to its low voltage state when the number of inputs present (equal to $-E_c$ volts) decreases from two to one, the base-emitter junction characteristics should not touch the high-voltage positive region of the tunnel-diode when only one input is present. This can be accomplished (Fig. 24-C) by connecting a small resistor in parallel with the tunnel-diode. The

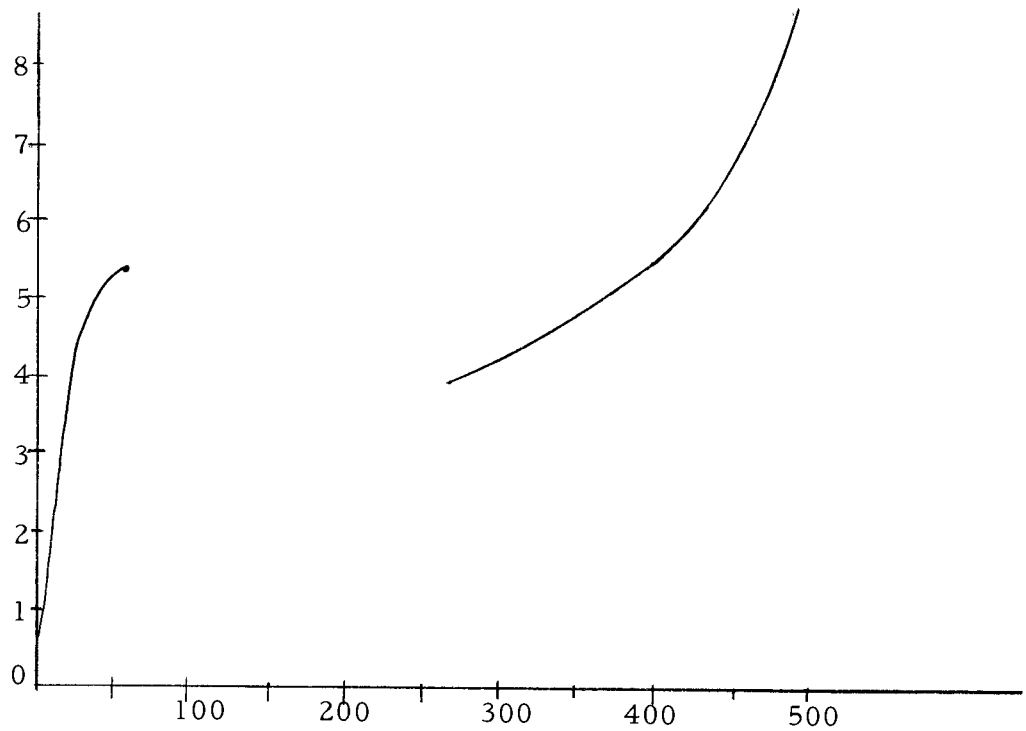


Fig. 24-F. Tunnel-diode characteristics (with 82 ohm parallel-resistor).

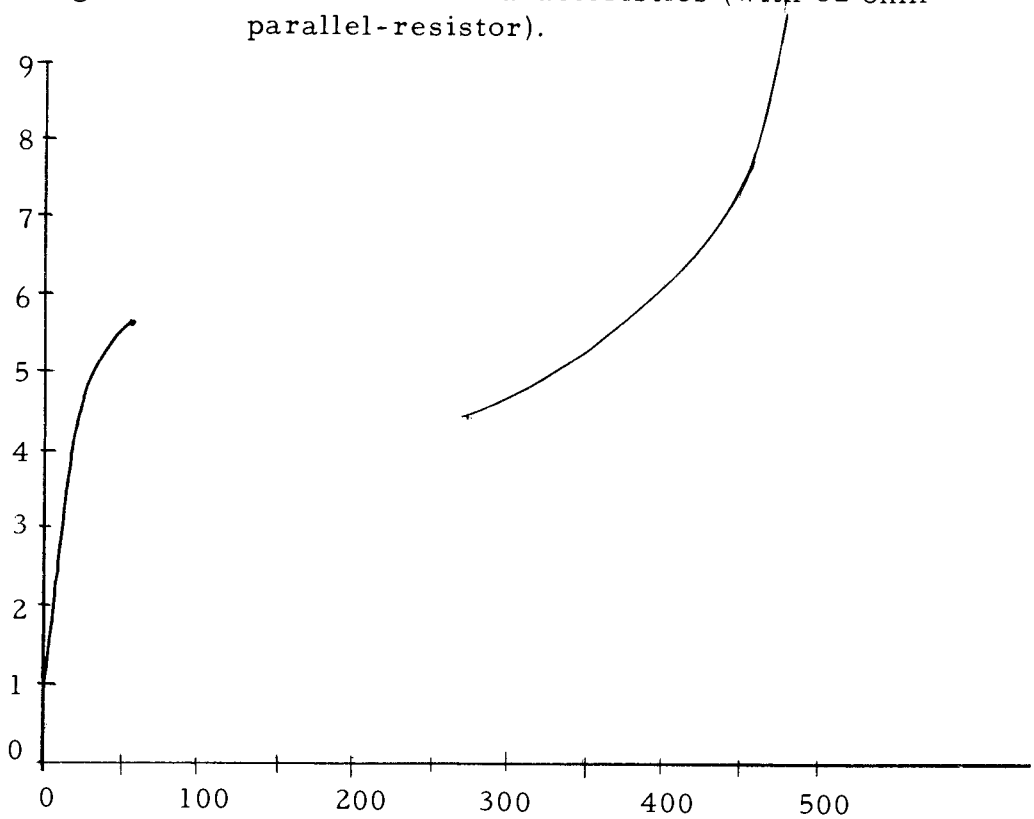


Fig. 24-G. Tunnel-diode characteristics (with 60 ohms parallel-resistor).

combined characteristics are shown in (Fig. 24-D).

Due to the shape of the tunnel diode characteristic, the bias of the base-emitter junction characteristics should be below $(I_v')_{min}$ for one input present and equal to $(I_p')_{max}$ for two inputs present.

It is practical to design such a circuit if the fan-in is three and the threshold value is two. However, it is not feasible for larger fan-in.

The other advantage of using a parallel resistor is that the combined tunnel-diode, and resistor characteristics takes appreciable current in the high voltage state, thus reducing the saturating current in the base-emitter junction.

(2) For fan-in greater than 3, a reset pulse has to be used for the tunnel diode threshold. It is claimed (4) that a circuit with 51 inputs was built utilizing tunnel diode threshold effect.

Selection of a Transistor for TTDRL Circuits

(1) From the "steady-state" point of view: The minimum turn-on base voltage of the transistor should be large compared to the peak-current voltage of the tunnel-diode (V_p), in order to keep the transistor OFF under worst-case conditions.

The minimum base turn-on voltage should be of such a magnitude that when the tunnel diode switches to the high voltage state, the base-emitter junction characteristics (Fig. 24-D) should intersect

the tunnel diode characteristics in the high-voltage region. If this condition is not satisfied, the high-voltage stable point cannot be obtained.

The value of the minimum base turn-on voltage should be near the valley-point tunnel-diode voltage (V_v), to facilitate this.

The value of the base-emitter junction voltage is determined by the point of intersection of the tunnel-diode, and the base-emitter junction characteristics. The input biasing current shifts the base-emitter junction characteristics up or down, depending on the value of the biasing current. The maximum base ON voltage is thus limited by the maximum allowable voltage on the tunnel-diode characteristics.

The specifications regarding $(h_{fe})_*$ and $(V_{cs})^*$ are the same as for VTTRL.

The effect of leakage current $(I_{CBO})^*$ is negligible due to the presence of low resistance tunnel-diode in the base circuit.

(2) From "transient-response" point of view: Since the tunnel diode switches very rapidly from low-voltage to the high-voltage state, the transistor used in this circuit should be a high-speed transistor.

The transistor chosen for this circuit is 2N967 which has a total switching time of 180 nsec.

The tunnel diodes used are 1N2941 and 1N3717. Both have

the same characteristics. The peak current tolerance for 1N2941 is ± 10% while that for 1N3717 is ± 2.5%. A tunnel diode with a high peak current (4.7mA) was chosen because the tolerance limit required for a low peak current (1mA) tunnel diode were very severe, especially after connecting a parallel resistance. However, if a low peak current tunnel diode is used, it will take smaller current which will result in a higher value for the transfer resistors and a greater fan-out.

Selection of a parallel resistor for the tunnel diode

The parallel resistor has to be of such a magnitude as to lift the valley point of the combined tunnel-diode, parallel-resistance characteristics above the base-emitter junction characteristics in the presence of one input.

100 ohms, 82 ohms, and 70 ohms resistances were tried. The combined characteristics with the tunnel-diode was plotted with the help of Tektronix 545 curve-tracer and are shown in Fig. 24-D, 24-E and 24-F.

Calculation for R_T and N_{max} were made for various values of circuit parameter tolerances using the combined characteristics of the 100 ohm and 82 ohm parallel resistors. Since the new valley point tolerance depends mainly on the tolerance of the parallel resistor, 1% tolerance limit is put on these resistances. Table XII

Table XI(A). 2N 967 PNP Ge transistor

Absolute maximum ratings		
Collector base voltage	V_{CBO}	12V
Collector emitter voltage	V_{CEO}	12V
Emitter base voltage	V_{EBO}	1.25V
Collector current	I_c	100mA
Total power dissipation	P_T(25°C Free Air)	150mW
	P_T(25°C case)	300mW

Electrical characteristics		MIN	TYP	MAX
Collector-base breakdown voltage I_c = 100μA, I_E = 0	BV_{CBO}	-12V		
Emitter base breakdown voltage I_E = 100 μA, I_c = 0	BV_{EBO}	-1.25V		
Collector cut off current	I_{CBO}			-5μA
Base-emitter sat. voltage I_B = 1mA, I_c = -10μA	V_{BE} sat.	-0.3		-0.5V
Collector-emitter sat. voltage I_D = -1mA, I_c = 10mA	V_{CE} sat.			-0.2V
Static forward current transfer-ratio (V_{CE} = 1.3, I_c = -10mA)		40	80	
Switching times for I_c = -10mA, $I_{B_{(1)}}$ = -1mA = $I_{B_{(2)}}$ = 0.25, $V_{BE_{(OFF)}}$ = 1.25V R_L = 300 ohms	t_{ON}		60 nsec	
	t_{OFF}		120 ns	

Table XI(B). Preassigned parameters

M	3
L	2
$(V_{cs})^*$	-0.2V
$(V_{bs_1}')^*$	-0.5V
(I_c')	15mA
$(I_{bs})^*$	0.375mA
$(h_{fe})^*$	40
$(\rho)_*$	1.2
$(I_{b_1})_*$	0.45mA
$(V_{cs})_*$	0.01V
$(I_o)^*$	0.1mA
$(I_{rc})^*$	0.05mA
ν_c	0.1 V
$V_{bs(3)}'$	-0.5V
E_1	-12V
E_c	-6V

shows the calculated values.

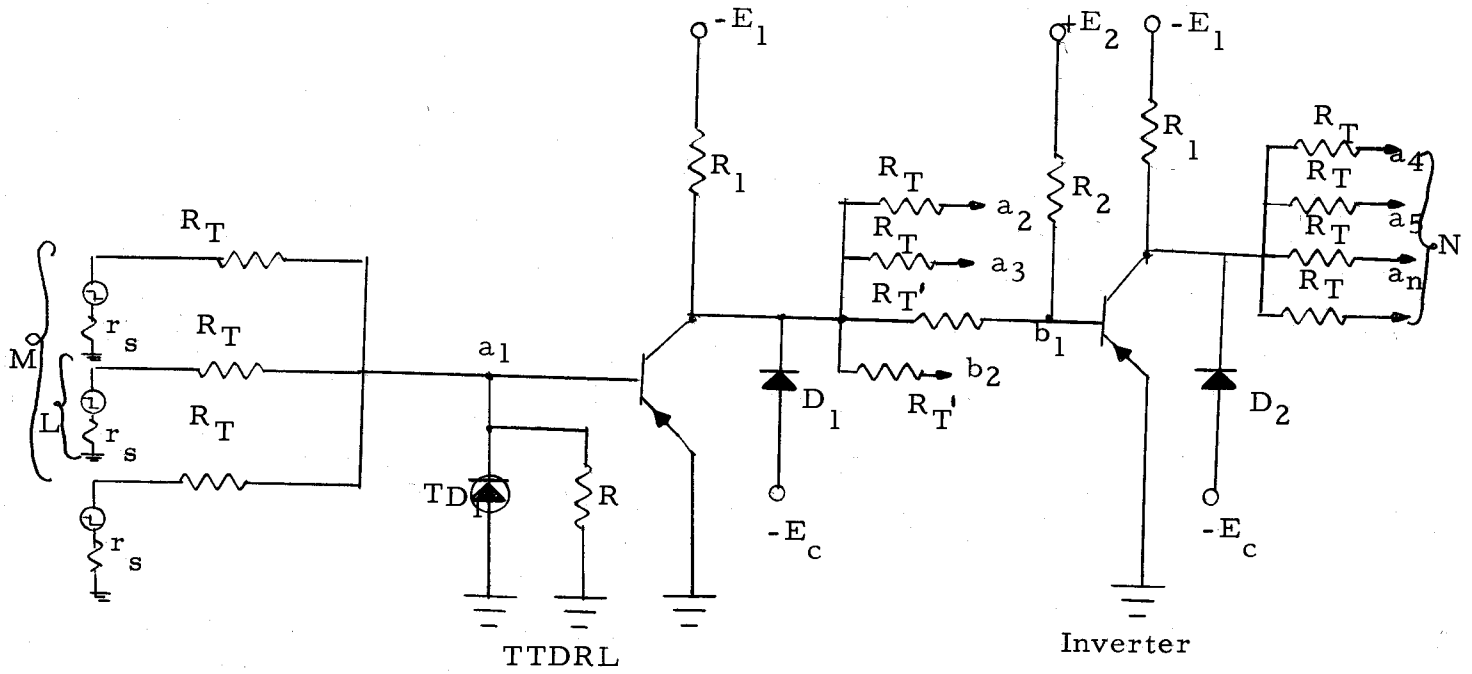
Steady-State Calculations

The conditions for the worst-case-OFF state junction characteristics does not touch the high voltage region of the tunnel diode characteristics. In other words, the bias current for one input should be less than the valley-point current of the tunnel diode characteristics.

Due to the presence of the tunnel diode, the transistor can never turn on (if the tunnel diode is in its low voltage state), in the presence of just one input, because the bias current under the worst conditions is about half of the peak-current.

However if the tunnel diode is switched to the high-voltage state by the presence of two or more inputs, then the tunnel diode will return to the low-voltage state when all but one input is removed, only if the base-emitter characteristic does not touch the high-voltage region under this condition. This condition is satisfied by connecting a parallel resistance to the tunnel diode.

Here the design procedure is as follows: The transfer resistor is chosen from the worst-case ON condition alone. It is chosen such that under worst-case ON conditions, the input current is just sufficient to cross the worst-case maximum peak current of the combined tunnel-diode, parallel-resistor characteristics. This



R_T	Transfer-resistor for TTDRL	M	Number of Inputs (3 in this circuit)
R_T'	Input-resistor for Inverter	L	Threshold level (2 in this circuit)
D	Clamping diode	N	Number of outputs to be optimized
T_D	Tunnel diode	R_s	Source impedance of inputs

Fig. 25. Transistor tunnel-diode circuit.

value of the transfer resistor is substituted in the worst-case-OFF conditions and the maximum input current pumped into the tunnel diode under these conditions is calculated. If the value of this current is less than the valley current of the combined tunnel-diode, resistance characteristics the design is valid. Otherwise the procedure has to be repeated for various values of parallel resistors until the above conditions are satisfied.

Worst-case, OFF Condition (Fig. 26-A)

The maximum value of the tunnel diode resistor characteristic in the high-voltage state is V_p'. Assuming this as the worst-case OFF base voltage, and maximum input current, the current pumped into the tunnel diode is calculated. It is also assumed that no current flows through the transistor. This current should be less than the valley-point current of the combined tunnel diode, resistor characteristics in order to have the monostable circuit operation.

For node (1) the equation is

$$(I_{TDL}) = \frac{((E_c)^* + (\nu_c) - V_p)}{(R_T)^*} + \frac{2((V_{cs})^* - (V_p))}{(R_T)^*} \qquad (32)$$

For node (2), the equation is

$$\frac{((E_1)^* - (E_c)^*)}{(R_1)^*} = (I_{co})^* + \frac{((E_c)^* - (V_{bs_1})^*)N}{(R_T)^*} \qquad (33)$$

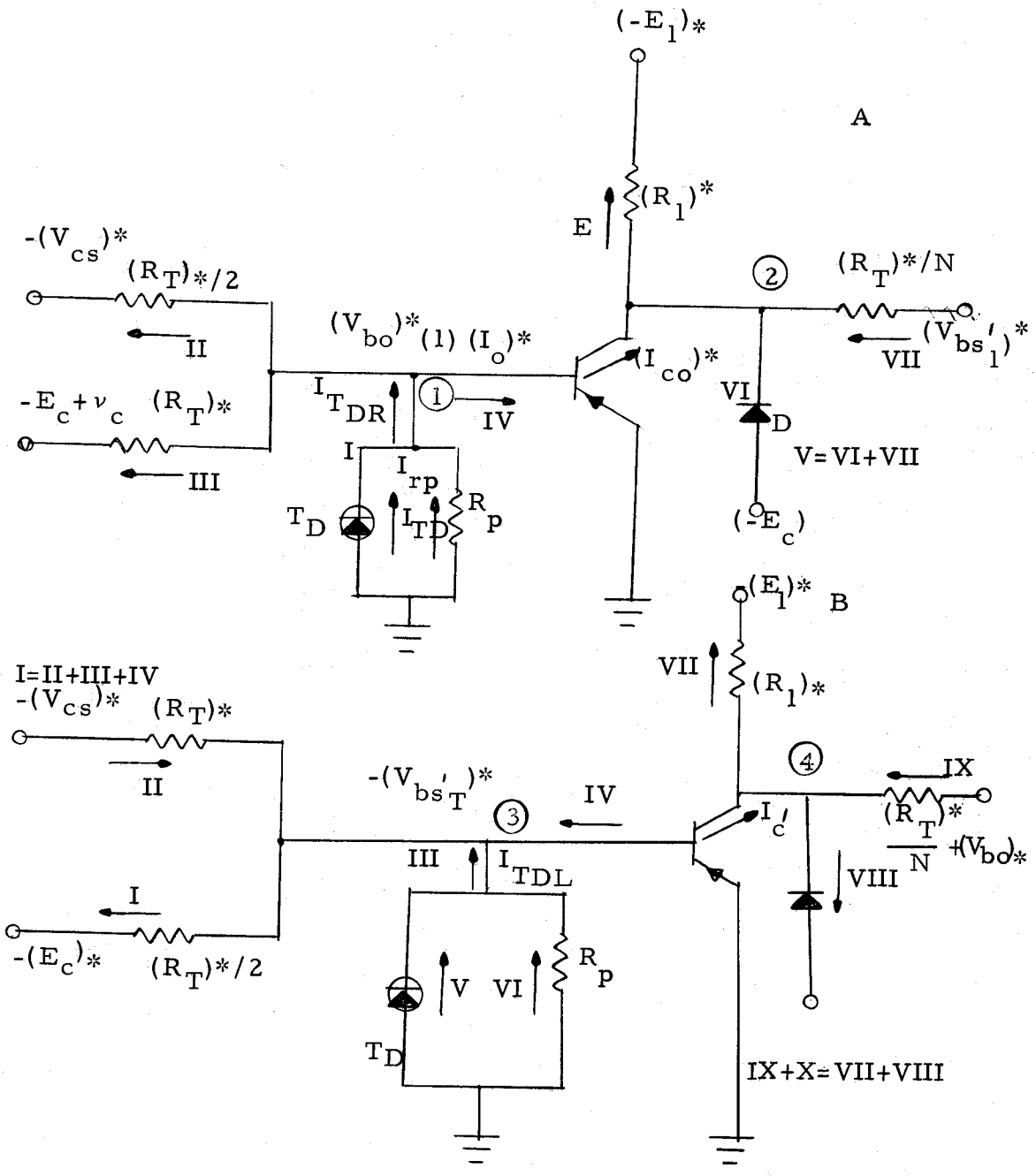


Fig. 26-A. Worst-case OFF conditions.
B. Worst-case ON conditions.

Worst-Case ON Conditions (Fig. 26-B)

The base node equation is written under the following conditions:

The input current supplied by the transfer resistors is a minimum. In other words, the input voltage is at its minimum value and the transfer resistors are at their maximum value.

The tunnel diode, resistor combined characteristic has a maximum peak current value.

The bias current due to the inputs is just sufficient to cross the maximum peak-current value.

Since the tunnel diode switches very fast to the high voltage state from the low voltage state, and takes less current in the high voltage state compared to its peak current (Fig. 24-D), the current required to saturate the transistor is not added to the peak current of the tunnel diode, resistor. The difference between the peak-current and high voltage state current is sufficient to saturate the transistor.

The node (3) equation is:

$$\frac{((E_c)_* - (V_{bs_1}')) \times 2}{(R_T)_*} = (I_{b_1})_* + \left(\frac{(V_{bs_1}) - (V_{cs})_*}{(R_T)_*} + (I_{TDL})\right) \quad (34)$$

Table XII. Effect of parallel-resistor, parameter tolerances on the working of the TTDRL circuit (I_c = 15mA)

Parallel-resistor ± tolerance %	T. D. Peak current tol. %	R_T KΩ	Tol of R_T %	Tol. of voltages %	Worst-case I_{TDL}	I_{TDL} permissible	Will the circuit operate?	N_{max} perm.	R_1 ±5%
100 ohms ± 1%	2.5	1.99	1	1	3.25	3.40	yes	3.0	0.725
	10	1.85	1	1	3.48	3.40	no		
	2.5	1.94	3	1	3.40	3.40	yes		
	2.5	1.90	5	1	3.50	3.40	no		
82 ohms ± 1%	2.5	1.88	3	3	3.50	4.07	yes	2	
	10	1.76	3	3	3.74	4.07	yes	2	
	2.5	1.86	5	3	3.66	4.07	yes	2	
	10	1.74	5	3	3.74	4.07	yes	2	0.825
	2.5	1.78	5	5	3.92	4.07	yes	2	0.830
	10	1.66	5	5	4.20	4.07	no		

For the present circuit, R_T = 1.78 ± 5% was selected with power supply tolerance of ± 5% and tunnel-diode (1N3717) with ± 2.5% peak-current tolerance.

The node equation for the collector is similar to one for VTTRL, and is not discussed in detail (node (4)),

$$(I_c) = (I_{RC})^* + \frac{((E_1)^* - (V_{cs})^*)}{(R_1)^*} - \frac{((V_{bo})^* + (V_{cs})^*)}{(R_T)^*/N} \qquad (35)$$

Design of the Inverter Circuit

The design of the inverter circuit for TTDRL is similar to that for VTTRL and VTL. A back-biasing current source is necessary to limit the base current in the inverter circuit.

The circuit diagrams and the node equations are the same as for the inverter circuits, previously designed, and are therefore not repeated.

The values obtained are:

Assuming $R_T = 1.78 + 5\%$

$(R_2)_{max} = 41.6\ K\Omega$

$(R_2)_{min} = 5.45\ K\Omega$

In order that base is not heavily saturated, R_2 is chosen close to $(R_2)_{min}$

$R_2 = 5.8 \pm 5\%$

$R_1 = 0.790\ K\Omega$

$N_{max} = 2.08$

$N_{permissible} = 2.0$

Transient Response

The values of $(I_{bm})^*$ and $(I_2')_*$ are calculated as in case of the other circuits.

Transient Response (TTDRL)

Maximum available turn-ON current and minimum available turn-OFF current have to be determined in order to calculate the switching times.

(1) Maximum base-on current (Fig. 27-A) Maximum base-on current is the difference between the maximum input current and minimum current taken by the tunnel-diode in its high voltage state (Fig. 27-B). It will also depend on the base-emitter-junction characteristics. Since this characteristic is changing within a certain tolerance (e.g. base turn on voltage for I_c = 15 mA, varies between 0.35 and 0.45 V), it is difficult to determine the exact current taken by the tunnel diode.

The maximum input current calculated is 10.3 mA. The current taken by base-emitter junction is calculated as follows:

Assuming turn on voltage (base = 0.45V

slope of the base-emitter diode ≃ 20 Ω

steady state tunnel diode voltage $= \frac{(0.50-0.45) \times 10^3}{20}$ mA

= 2.5 mA.

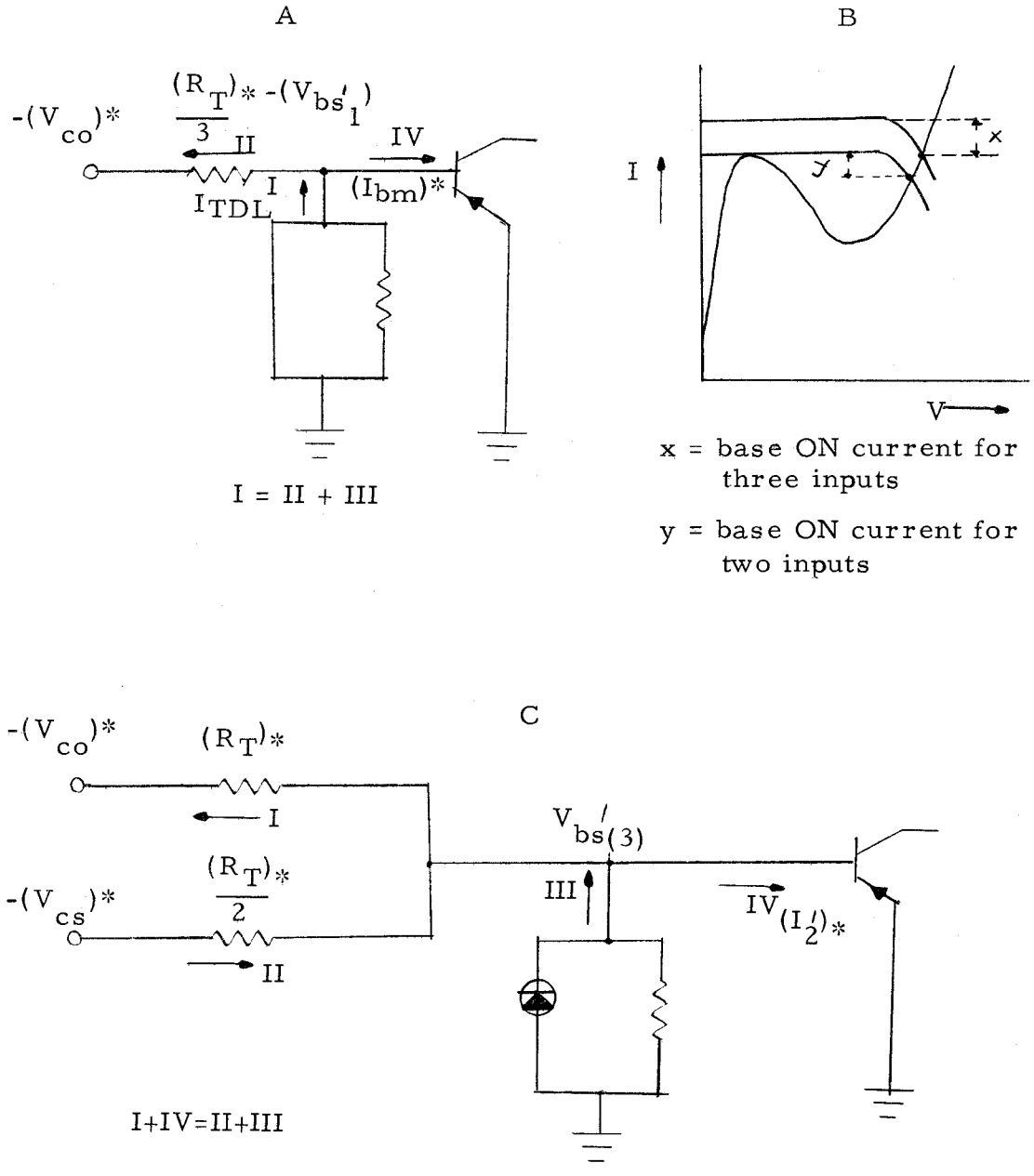


Fig. 27. (A) Maximum base ON current
(B) Base ON current determination
(C) Minimum Available Turn-OFF current.

This is one of the advantages of the TTDRL circuit. Irrespective of high input currents, the base-emitter junction current does not become very high due to the presence of the tunnel-diode and parallel resistor in the base node. Also the minimum on base current is much higher than the one required to just turn-ON the transistor. This reduces the turn-on time.

Minimum Available Turn-OFF Current (Fig. 27-C)

Assuming that the tunnel-diode is just shifting from the high to the low voltage state, it has current of 4.0 mA (82 ohm parallel resistor).

The nodal equation is

$$-(I_2')_* = \frac{((V_{co})^* - V_{bs}'(3))}{(R_T)_*} - I_{TDL} - \frac{(V_{bs}'(3) - (V_{cs})^*)}{(R_T)^*/2} \qquad (36)$$

It is assumed that the fall in the tunnel-diode voltage in the high voltage stage towards the valley point is much faster compared to the transistor switching. Then for transient considerations, the valley point is assumed to be point under consideration.

$(I_2')_*$ is found to be 0.92 mA.

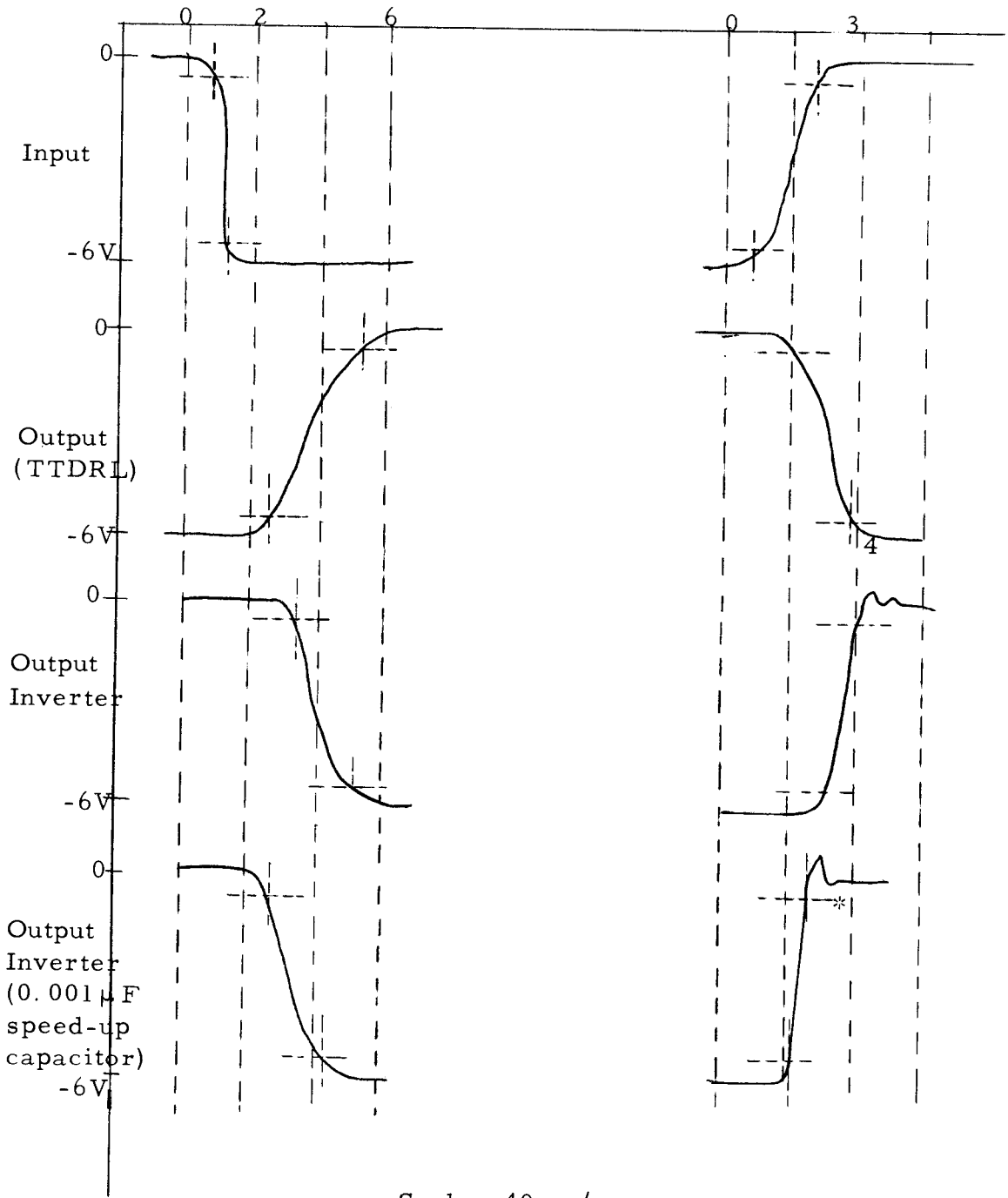
$(I_{bm})^* = 2.5$ mA $(I_2')_* = 0.92$ mA	TTDRL (I_c = 15 mA)
$(I_{bm})^* = 0.74$ $(I_2') = 2.37$	Inverter (I_c = 15 mA)
$(I_{bm})^* = 1.0$ $(I_2') = 0.50$	Test circuit (I_c = 10 mA)

The switching times are calculated using Appendix I and are tabulated in table XIII and compared with the observed switching times.

Table XIII. Comparison of switching times

	t_d ns	t_r ns	t_s ns	t_f ns	t_{total} ns	Type of wave-shape
	20	80	106	36	242	Calculated TTDRL output for step input
	20	160	54	20	254	Calculated Inverter output for step input
		80		40		Pulse input
One D. C., one pulse input	120	80	80	60	340	TTDRL output (obs.)
	120	40	130	70	360	Inverter output (obs.)
	80	30	100	70	280	Inverter output with 0.001 μF speed-up capacitor
One D. C., two pulse inputs	70	40	80	100	290	TTDRL output
	140	20	120	50	330	Inverter output
	100	40	60	80	280	Inverter output with 0.001 μF speed-up capacitor

The calculated times are less than the observed values mainly because in calculations, a step-input pulse is assumed. In the present circuit, the input pulse has a 80 ns Rise and 40 ns fall-time. The output of the Inverter seems to be as good as the output of TTDRL. This is because the effect of the rise and fall time of the input on the Inverter stage is much less than its effect on TTDRL. TTDRL requires input voltage pulse of exact magnitude $(-E_c)V$ before the transistor can turn-on.



Scale: 40 ns/cm

* An overshoot at the Inverter output is observed due to the presence of high turn-on current.

Fig. 28-A. TTDRL circuit (one D. C., one pulse).

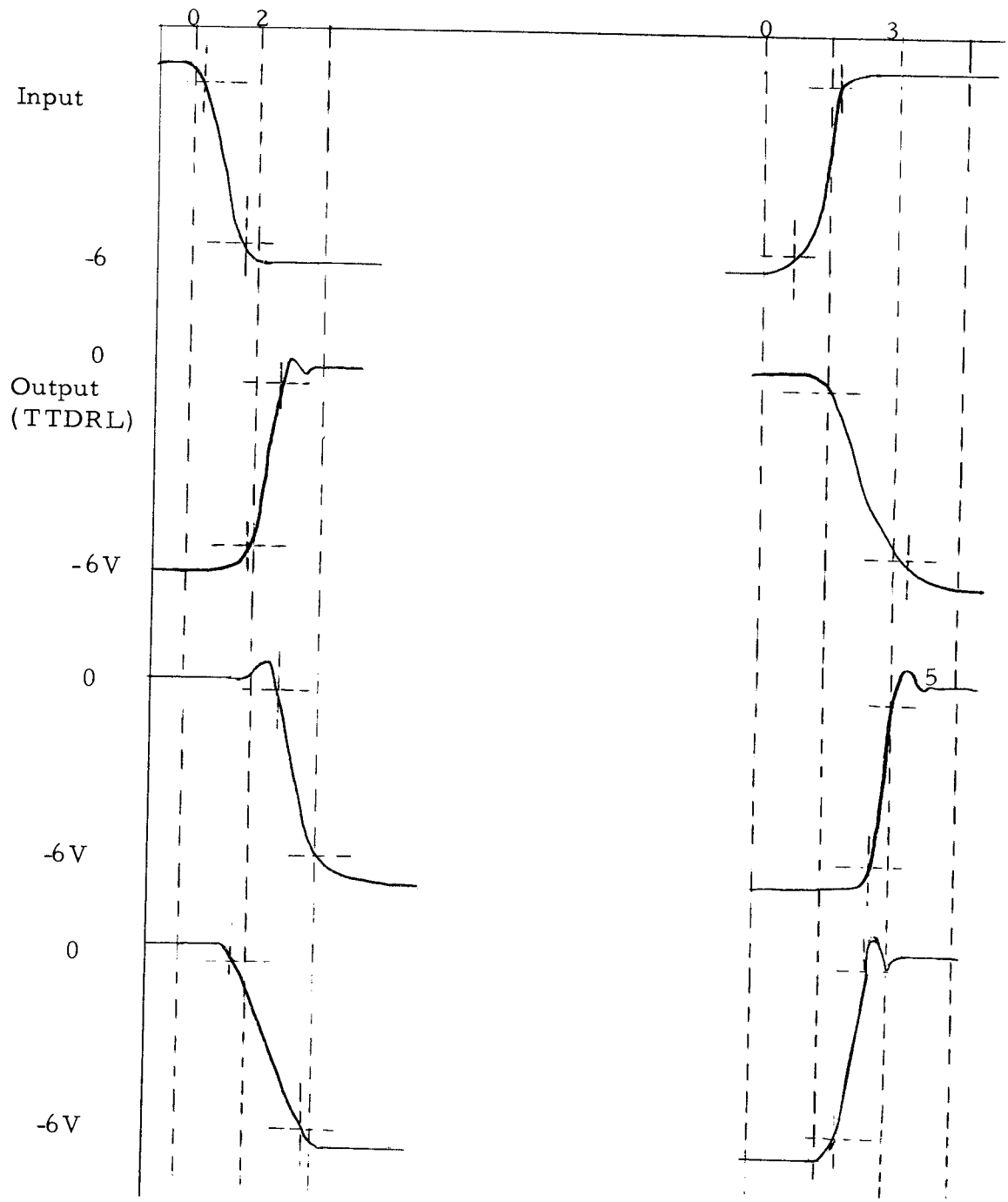


Fig. 28-B. One D. C., two pulse inputs.

PART V

COMPARISON OF VTTRL, VTL, TTDRL CIRCUITS

(1) Circuit Parameter Tolerance

VTTRL. It is not practical to design a three input Majority-Logic circuit with more than ± 3% tolerance limit. It is also not practical to design majority circuits with more than three inputs.

VTL. The tolerance limits are more severe. The voltage supply is assumed to be ±1%. Other circuit parameters must be more than ±3% accurate.

TTDRL. As far as the worst case OFF condition is concerned, the tolerance limit for this circuit can be increased much more than the first two circuits. However in order to avoid the use of a reset pulse for three input case, the tolerance limits have to be kept at ± 5%. It is possible to design majority gate with five or more inputs but the use of a reset pulse then becomes essential.

(2) Transistor Type

VTTRL. Can be designed using any kind of transistor, once the $(h_{fe})_{minimum}$ is known. There are no special requirements for the transistor to be used in this circuit.

VTL. Only transistors with a high base-ON voltage can be

used in this design, because no back-biasing current source is used here.

TTDRL. The transistor type is dependent mainly on the tunnel-diode characteristics. The parameter of most significance here is the minimum and maximum base ON voltage, and the base-emitter diode characteristics. The base-emitter characteristics should intersect the tunnel-diode characteristics at the specific points in the presence of one, two, and three inputs. This is important to avoid heavy saturation of the transistor and to have proper circuit operation without the use of a reset pulse.

The tunnel-diode characteristics can be modified by the use of series and/or parallel resistance with the tunnel-diode. The parallel resistance is required in order to have the proper circuit operation. Hence in order to avoid extra tolerance because of the series resistance, it is desirable to have a transistor with a base-ON voltage approximately equal to the valley point tunnel-diode voltage.

(3) Cost

One important cost factor is the transistor type. The second is tolerance limits of other circuit parameters.

VTTRL and VTL require components with more rigid tolerance and TTDRL with comparatively less. But in TTDRL the additional

cost of the tunnel-diode has to be taken into account.

The type of transistor used in each circuit will be cheap or expensive depending upon its maximum power rating, switching speed, reliability of its parameters, etc. and therefore cannot be considered separately for each circuit.

(4) Switching Times

VTTRL. Here the maximum base-ON current will be increased if parameters of low tolerance are used and vice-versa. The turn-OFF current should be large due to the presence of the back-biasing current source.

VTL. Here the turn-ON current (maximum) is comparatively more due to the absence of any back biasing source. However the turn-OFF current is comparative to the VTTRL. This current is obtained due to large current flowing through R_o (Fig. 17) when the transistor turns-OFF from maximum saturation limit.

TTDRL. The use of the parallel resistance with the tunnel-diode passes an appreciable turn-ON current for two out of the three inputs and does not increase the turn-ON current too much when all the three inputs are present. However if no parallel resistance is used the maximum turn-ON current is very high. Also the parallel-resistor has to be properly selected in order to obtain the best switching times.

(5) Power-Dissipation

Due to the absence of the back-biasing current source in VTL and TTDRL, their power dissipation for a particular value of maximum collector current is less than the power-dissipation for VTTRL circuit.

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APPENDICES

APPENDIX I (3)

Predicting the turn ON and turn OFF times under given current conditions of the circuit using the typical switching characteristics given in the specification sheet under certain curent condition.

Let the subscript o represent the conditions specified in the specification sheet and the subscript 1 represent the conditions of the circuit for which the switching time need be found.

(1) RISE TIME: (Fig. 29)

$$\frac{t_{r_1}}{t_{r_o}} = \frac{\beta_{T_1}\left(\frac{1.25}{W_{T_1}} + 1.7\,R_{L_1}C_{C_1}\right)\ell n\left(1-\frac{\beta_{C_1}}{\beta_{T_1}}\right)}{\beta_{T_o}\left(\frac{1.25}{W_{T_o}} + 1.7\,R_{L_o}C_{C_1}\right)\ell n\left(1-\frac{\beta_{C_o}}{\beta_{T_o}}\right)} \tag{37}$$

$$\frac{t_{r_1}}{t_{r_o}} = K_B K_T K_C \tag{38}$$

$$K_B = \frac{\beta_{T_1}}{\beta_{T_o}} \simeq 1.0$$

$$K_T = \frac{\left(\frac{1.25}{W_{T_1}} + 1.7\,R_{L_1}C_1\right)}{\left(\frac{1.25}{W_{T_o}} + 1.7\,R_{L_o}C_o\right)} \simeq 1 \tag{39}$$

$$K_C = \frac{\ell n \left(1 - \frac{\beta_{C_1}}{\beta_{T_1}}\right)}{\ell n \left(1 - \frac{\beta_{C_o}}{\beta_{T_o}}\right)} = \frac{x}{y} \tag{40}$$

y v/s x is plotted on a graph for different K_C. Knowing n y, K_C is determined.

Fall Time (Fig. 10)

$$\frac{t_{f_1}}{t_{f_o}} = \frac{\beta_{T_1}\left(\frac{1.25}{W_{T_1}} + 1.7\, R_{L_1} C_1\right) \ell n \left(1 + \frac{\beta_{CC_1}}{\beta_{T_1}}\right)}{\beta_{T_o}\left(\frac{1.25}{W_{T_o}} + 1.7\, R_{L_o} C_o\right) \ell n \left(1 + \frac{\beta_{CC_o}}{\beta_{T_o}}\right)} \tag{41}$$

$$\frac{t_{f_1}}{t_{f_o}} = K_\beta K_T K_C \tag{42}$$

$$K_p = K_T \simeq 1$$

$$K_C = \frac{\ell n \left(1 + \frac{\beta_{CC_1}}{\beta_{T_1}}\right)}{\ell n \left(1 + \frac{\beta_{CC_o}}{\beta_{T_o}}\right)} = \frac{r}{y} \tag{43}$$

Knowing x, y, K_C is determined from the graph of for various values of K_C.

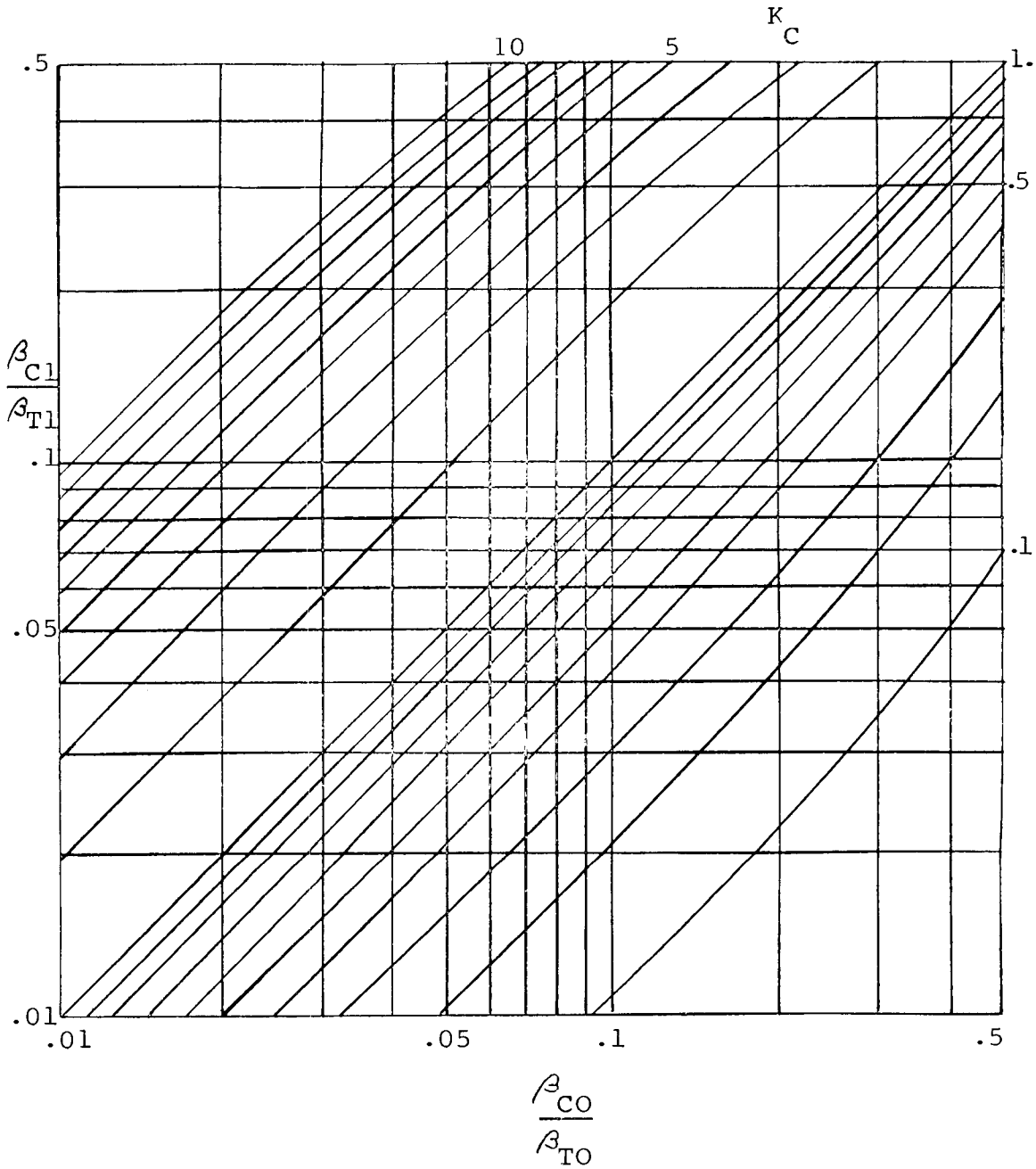

Fig. 29. Plot for finding K_C of the rise time equation.

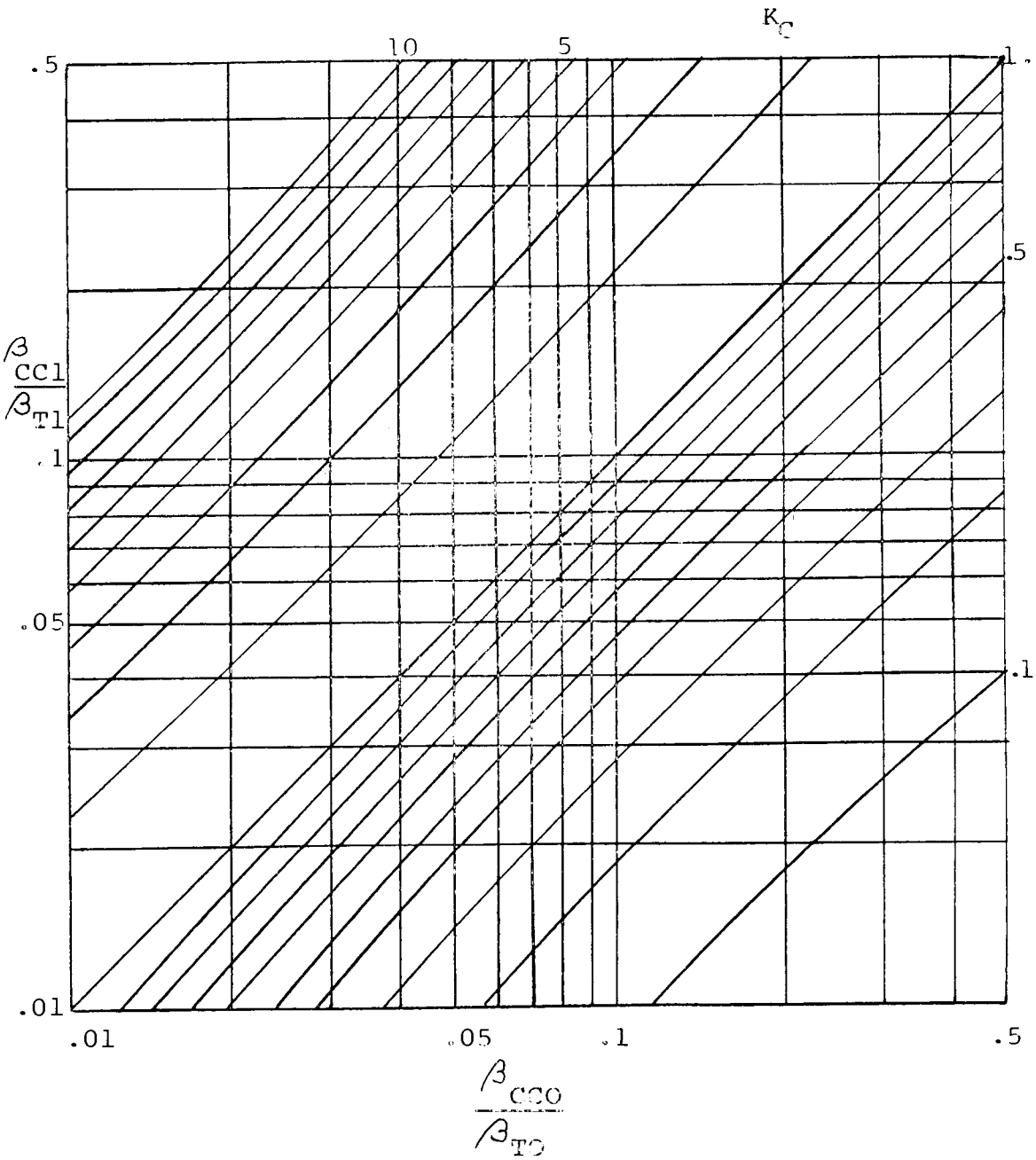

Fig. 30. Plot for finding K_C of the fall time equation.

Storage Time (Fig. 11)

$$\frac{t_{s_1}}{t_{s_o}} = \frac{f(T_{s_1}) \ln\left(\dfrac{\dfrac{\beta_{CC_1}}{\beta_{C_1}} + 1}{\beta_{CC_1}/\beta_{T_1} + 1}\right)}{f(T_{s_o}) \ln\left(\dfrac{\dfrac{\beta_{CC_o}}{\beta_{C_o}} + 1}{\dfrac{\beta_{CC_o}}{\beta_{T_o}} + 1}\right)} \tag{44}$$

$$\frac{t_{s_1}}{t_{s_o}} = K_T K_C$$

$$K_T = \frac{f(T_{s_1})}{f(T_{s_o})} \approx 1$$

$$K_C = \ln\left[\frac{\left(\dfrac{\dfrac{\beta_{CC_1}}{\beta_{C_1}} + 1}{\dfrac{\beta_{CC_1}}{\beta_{T_1}} + 1}\right)}{\left(\dfrac{\dfrac{\beta_{CC_o}}{\beta_{C_o}} + 1}{\dfrac{\beta_{CC_o}}{\beta_{T_o}} + 1}\right)}\right] = \frac{K_{C_1}}{K_{C_o}} \tag{45}$$

K_{C_1} is plotted on log paper for β_{CC_1} β_{T_1} on vertical and β_{CC_1}/β_{C_1} on horizontal axis. Having determined K_C, the new storage time can be determined.

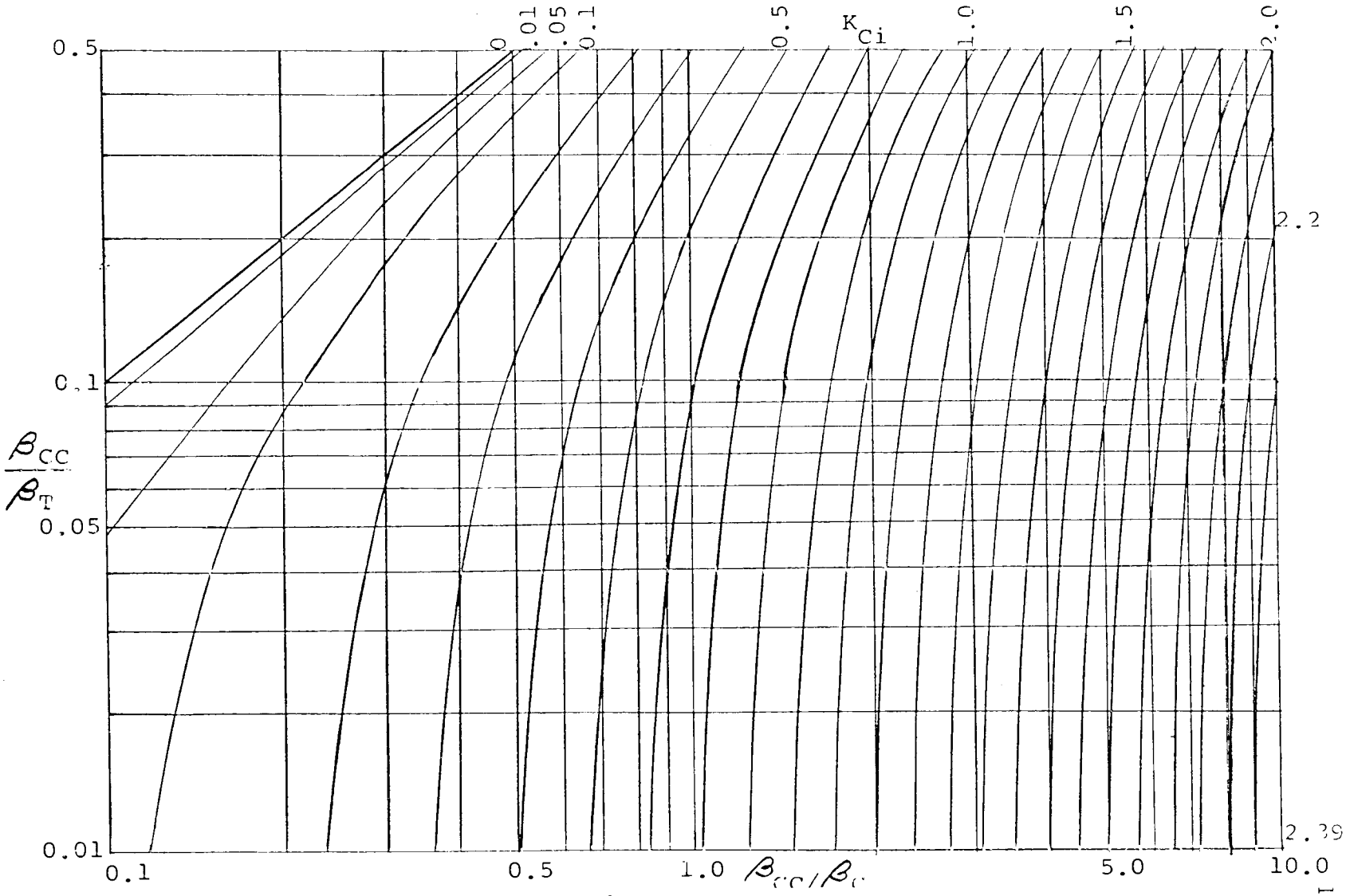

Fig. 31. Plot for finding K_{C_i} of the storage equation circuit Function K_C.

APPENDIX II

Parameter Measurement Information

Test Circuit (For 1305 PNP Transistors)

1. Input pulse supplied by generator with the following characteristics:
   a. Output impedance 50Ω
   b. Repetition rate 1 kc
   c. Rise and fall time 20 nano sec. max.
   d. Pulse width 10 μsec
   e. Pulse amplitude 16.5 volts
2. Waveform monitored on scope with following characteristics:
   a. Input resistance 10 megohms (minimum)
   b. Input capacitance 15 pf (max.)
3. All resistor ± 1% tolerance
4. Test conditions:

   $I_c = -10mA$, $I_{B(1)} = -1.3mA$

   $I_{B(2)} = 0.7$ mA $V_{BE(OFF)} = 0.8V$
5. Switching characteristics at 25° C

   $t_d = 0.006$, $t_r = 0.18$, $t_{ON} = 0.24$ μsec

   $t_s = 0.80$, $t_f = 0.38$, $t_{OFF} = 1.18$ μsec

   $t_{total} = 1.42$ μsec.

The test circuit was built and tested in the laboratory with the Tektronix 585 oscilloscope (Rise time = 30 nano sec.).

Table XIV. Transistor switching times

Transistor 2N 1305 sample #	$t_{ON} = t_d + t_r$ μ sec	$t_{storage}$ μ sec	t_{fall} μ sec	t_{total} μ sec
From data sheet	0. 24	0. 80	0. 38	1. 42
1	0. 25	0. 60	0. 60	1. 45
2	0. 30	0. 60	0. 60	1. 50
3	0. 20	0. 60	0. 40	1. 20
4	0. 10	0. 80	0. 60	1. 50
5	0. 05	0. 40	0. 40	0. 85
6	0. 05	0. 80	0. 60	1. 45
7	0. 15	0. 60	0. 60	1. 35
8	0. 20	0. 60	0. 70	1. 50
9	. 20	0. 80	0. 60	1. 60
10	0. 10	0. 60	0. 40	1. 10
Average	0. 16	0. 64	0. 51	1. 31

APPENDIX III

Transient Response*
(Sample calculation for 2N 1305 transistor)

Rise Time

From the data sheets2 the "turn ON" and "turn OFF" time are given at certain collector and base current.

At $I_c = -10\text{mA}$, $I_b = -1.3$ mA

(typical) $t_{r_o} = 0.18\ \mu\text{sec.}$

In order to determine it at

$$I_c = 10 \text{ mA}, \quad I_{b_1} = 0.30 \text{ mA.}$$

We have

$$\frac{t_{r_1}}{t_{r_o}} = K_\beta K_T K_C$$

Assuming $K_\beta = 1$, $K_T = 1$

$$\beta_{co} = \frac{10}{1.3} = 7.7$$

$$\beta_{T_o} = 115$$

(typical)

$$\beta_{T_1} = 115$$

$$\beta_{C_1} = \frac{10}{0.30} = 33.3$$

---

*Appendix I.

$$\frac{\beta_{C_o}}{\beta_{T_o}} = \frac{7.7}{115} = 0.067, \qquad \frac{\beta_{C_1}}{\beta_{T_1}} = \frac{33.3}{115} = 0.29$$

From graph of $\frac{\beta_{C_o}}{\beta_{T_o}}$ v/s $\frac{P_{C_1}}{\beta_{T_1}}$

$$K_C = 5$$

$$t_{r_1} = 5 \times 0.18 = 0.90 \ \mu\text{sec.}$$
(max)

Fall Time

At $I_c = 10$ mA. $I_{B(2)} = 0.7$ mA

$V_{B_{E(OFF)}} = 0.8$ volts

t_{fall} (typical) $= 0.38 \ \mu$sec.

$$\beta_{CC_o} = \frac{10}{0.7} = 14.3$$

$$\beta_{T_o} = 115 = \beta_{T_1}$$

In the present circuit, $I_{B(2)} = 0.82$ mA

$$\beta_{CC_1} = \frac{10}{0.82} = 12.2.$$

$$\frac{\beta_{CC_o}}{\beta_{T_o}} = \frac{14.3}{115} = 0.124$$

$$\frac{\beta_{CC_1}}{\beta_{T_1}} = \frac{12.2}{115} = 0.106$$

From Graph of $\frac{\beta_{C_o}}{\beta_{T_o}}$ v/s $\frac{\beta_{C_1}}{\beta_{T_1}}$,

$K_C \cong 1.0$ Assuming $K_\beta = K_T = 1$

$$\frac{t_{f_1}}{t_{f_o}} = K_\beta K_C K_T,$$

$$t_{f_1} = t_{f_o} = 0.38\ \mu\text{sec.}$$

Storage Time

At $I_c = 10\text{mA}$, $I_{B(1)} = -1.3\text{mA}$

$I_{B_2} = 0.7\text{mA}$

$t_{s_o} = 0.80\ \mu\text{sec}$ (typical)

Also

$$\frac{t_{s_1}}{t_{s_o}} = K_T K_C$$

$$K_T = \frac{f(T_{s_1})}{f(T_{s_o})} \simeq 1$$

$$K_C = \frac{K_{C_1}}{K_{C_o}}$$

$$K_{C_i} = \frac{\beta_{CC_i}}{\beta_{T_i}}$$

$$\beta_{T_1} = \beta_{T_o} = 115 \text{ (typical)}$$

$$\beta_{CC_o} = \frac{10}{0.70} = 14.3$$

$$\beta_{CC_1} = \frac{10}{0.82} = 12.2$$

$$\beta_{C_o} = \frac{10}{1.3} = 7.7$$

$$\beta_{C_1} = \frac{10}{2.68} = 3.74$$

$$\frac{\beta_{CC_o}}{\beta_{C_o}} = \frac{14.3}{7.7} = 1.86$$

$$\frac{\beta_{CC_o}}{\beta_{T_o}} = 0.124$$

$$\frac{\beta_{CC_1}}{\beta_{C_1}} = \frac{12.2}{3.74} = 3.26$$

$$\frac{\beta_{CC_1}}{\beta_{T_1}} = \frac{12.2}{115} = 0.106$$

From graph of

$$\frac{\beta_{CC}}{\beta_T} \text{ vs } \frac{\beta_{CC}}{\beta_C} \quad \text{we have}$$

$$K_{C_o} = 0.85$$

$$K_{C_1} = 1.19$$

$$K_C = \frac{1.19}{0.85} = 1.39$$

$$\frac{t_{s_1}}{t_{s_o}} = K_T K_C = 1.39$$

$$t_{s_1} = 0.80 \times 1.39$$

$$t_s = 1.11 \ \mu\text{sec} \quad \text{(typical)}$$