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Title: High-Linearity Switched-Capacitor Circuits in Digital CMOS Technologies

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Gabor C. Temes

In this thesis, novel design techniques have been proposed for implementing high-linearity SC circuits in a standard digital CMOS process. They use nonlinear MOSFET capacitors instead of linear double-poly capacitors. To reduce their nonlinearities, a bias voltage is applied to keep MOSFET capacitors in their accumulation regions. For further reduction of distortion, two capacitors can be connected in series or in parallel so that a first-order cancellation of the nonlinearity can be achieved. Experimental results demonstrated that the among these techniques series compensation is the most effective for reducing the nonlinearity of MOSFET capacitors.

A novel predictive SC amplifier has been proposed for its insensitivity to op-amp imperfections. Experimental results show that the S/THD of the predictive SC amplifier was 10 dB larger than that of the non-predictive one. It was also shown that a predictive circuit was effective for reducing the nonlinearity caused by the op-amp and/or the MOSFET capacitors.

It has been demonstrated that a two-stage op-amp with a large output swing can be fabricated in a standard digital CMOS process. The frequency compensation was accomplished using a source follower and a MOSFET capacitor. An SC amplifier using this two-stage op-amp and double-poly capacitors was fabricated, and it exhibited a large linear output range.

A MOSFET-only digitally controlled gain/loss circuit was designed and fabricated in a 1.2 μm CMOS process. It demonstrated that the series compensation is effective not only for a large output swing in an amplifier, but also for a large input swing in an attenuator.

A pipeline D/A converter utilizing MOSFET capacitors was designed as another application of charge processing technique. It consisted of three parts: a V-Q conversion stage, a charge transfer stage, and a Q-V converter.

A new switch configuration which enables the series compensation to have a large bias voltage has also been proposed. It was shown that it works well, and it will be helpful for low-voltage operation, too.

High-Linearity Switched-Capacitor Circuits in Digital CMOS Technologies

by

Hirokazu Yoshizawa

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To my parents

High-Linearity Switched-Capacitor Circuits in Digital CMOS Technologies

Chapter 1

INTRODUCTION

1.1 Introduction

There is an increasing demand for combining analog and digital integrated circuits on a single chip. Because of their great capabilities for dense integration and low power consumption, complementary metal-oxide-semiconductor (CMOS) technologies are dominantly used in digital circuits and memory devices. To integrate analog circuits on the same chip with digital ones, it is preferable to realize the analog circuits also by the CMOS technologies. For realizing CMOS analog circuit functions such as amplifiers, filters, and data converters, switched-capacitor (SC) circuits have been the principal technique for nearly two decades.

When analog and digital circuits are integrated on the same chip, an extra processing step creating a second polysilicon (poly) layer is usually added to fabricate linear double-poly capacitors for the analog circuit. This represents a significant added cost, even though the chip area required for the analog circuitry is usually much smaller than that of the digital part. In addition, double-poly capacitors are not available in some inexpensive digital CMOS processes. In such a process, metal-1 to poly or metal-1 to metal-2 capacitors are often used to implement linear capacitors. However, these capacitors require a large chip area, because their Si-oxide layers are very thick. Also, their matching properties are inferior due to the rough surface of their bottom plates and the poor uniformity of the chemical-vapor-deposition (CVD) oxide [1], [2]. In addition, these capacitors have large

parasitic capacitance to the substrate, which affects the signal processing, and increases the dc power loss.

The other possibility is to use MOSFET capacitors*. These have a large capacitance per unit area because the gate oxide is thinner than the oxide layer of any other capacitors in the CMOS process. As an example, for a typical 1.2 μm CMOS process the properties of several kinds of capacitors are shown in Table 1-1.

Table 1-1 Oxide thickness and equivalent capacitor size

	Thickness of oxide [Angstrom]	Capacitance per unit area [fF/μm^2]	Equivalent size
MOSFET capacitor	225	1.53	1
Double-poly capacitor	700	0.49	3.1
M1-poly capacitor	5200	0.066	23
M1-M2 capacitor	7500	0.046	33

In the process considered in Table 1-1, a MOSFET capacitor requires a chip area which is less than 1/3 of that needed by a double-poly capacitor with the same capacitance and a small fraction of the size of equivalent metal-poly or metal-metal capacitors. In other processes the area saving is even larger. The MOSFET capacitor also offers good matching accuracy, due to the uniformity of its thermally-grown gate oxide and the smooth surface of its single-crystal silicon bottom plate [1]. Finally, MOSFET capacitors are available in any CMOS process because they are intrinsic elements of MOS technology. Nevertheless, they normally cannot be directly used in SC circuits because of their strong voltage dependence.

* Throughout this thesis,"MOSFET capacitor" is used to refer to a poly-gate-to-channel capacitor without a heavily-doped diffusion layer under the gate oxide. By contrast, the term "MOS capacitor" is used to refer to any capacitor realized in metal-oxide-semiconductor technology such as a double-poly, metal-poly, poly-diffusion, and MOSFET capacitor.

In this thesis, circuit design techniques are described for linearizing the operation of CMOS analog ICs using MOSFET capacitors in digital CMOS processes. The usefulness of these techniques will be illustrated by applying them to some common SC building blocks.

1.2 Thesis Outline

Chapter 2 of this thesis explores capacitors in CMOS technology. It begins with a description of capacitors available in analog and digital CMOS processes. Then, MOSFET capacitors are introduced. The characteristics of the MOSFET capacitor will be described such as its C-V curve, parasitics, HSPICE models. A practical layouts will be also shown.

Chapter 3 describes the background of this research work. Simple biasing and charge processing techniques using MOSFET capacitors will be introduced. Next, switched-current circuits will be described as a signal-processing technique which does not require high-linearity capacitors. Finally, sample-and-hold circuits are introduced as an example illustrating the feasibility of high-precision SC circuits using nonlinear capacitors.

Chapter 4 shows design techniques for MOSFET-only switched-capacitor circuits. Three design techniques will be described for reducing the nonlinearity of the MOSFET capacitors.

Chapter 5 introduces the predictive correlated-double-sampling (CDS) technique, and a new predictive SC amplifier will be described. Finally, the effects of CDS on the circuit nonidealities will be discussed.

Chapter 6 provides experimental results obtained for the switched-capacitor amplifiers. A test circuit and a clock generator circuit will be shown. Finally, the measured results will be discussed.

Chapter 7 describes the circuitry of some operational amplifiers suitable for digital CMOS processes.

Chapter 8 introduces a digitally controlled gain/loss circuit using MOSFET capacitors. First, an overview of some relevant earlier work will be given. Then the circuit design and experimental results will be shown.

Chapter 9 discusses a MOSFET-only pipeline digital-to-analog converter. The design and simulation results will be given.

Chapter 10 describes a compensation technique for deep submicron and low-voltage process. New switch configurations suitable for low-voltage processes are proposed.

Finally, Chapter 11 gives the conclusions of this thesis and suggests future research work.

Chapter 2

CAPACITORS IN CMOS TECHNOLOGY

In this chapter, the various capacitor realizations available in both analog and digital CMOS processes are described. Then, MOSFET capacitors are introduced. The characteristics and models of MOSFET capacitor will be described, such as C-V curves, parasitics, and HSPICE models. Finally, the practical layout of the MOSFET capacitor will be also shown.

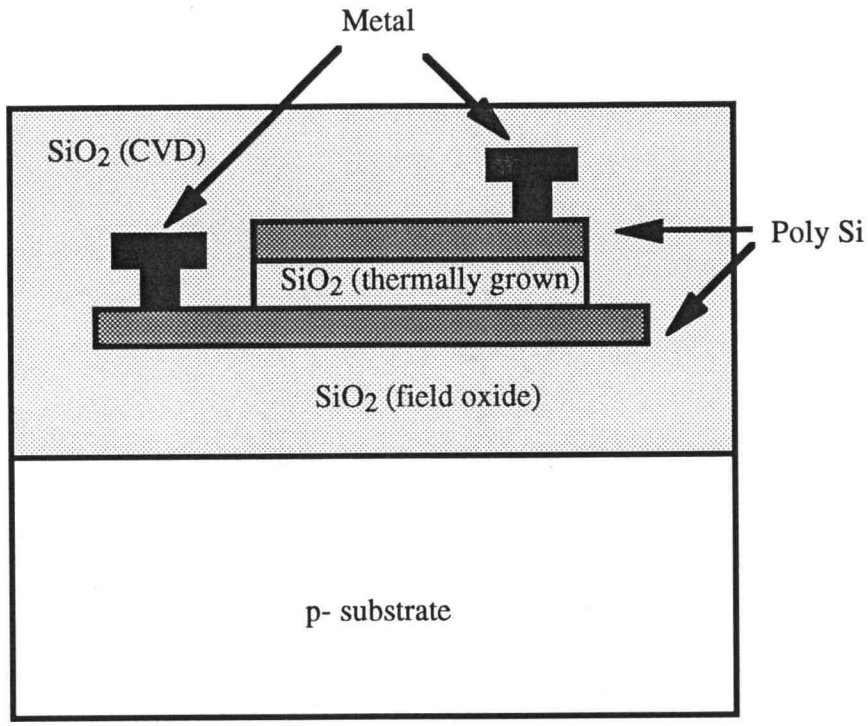
2.1 Capacitors in Analog CMOS Technology

The double-poly capacitor is most widely used for realizing high-linearity SC circuits because of its good linearity properties. Practical realization of the double-poly capacitor is illustrated in Figure 2.1a. Both poly layers are highly doped, and one surface accumulates while the other depletes so that its voltage dependence is greatly reduced [1]. The total capacitance C_t is modeled in Figure 2.1b, and is given by the series combination of the oxide and space-charge capacitances:

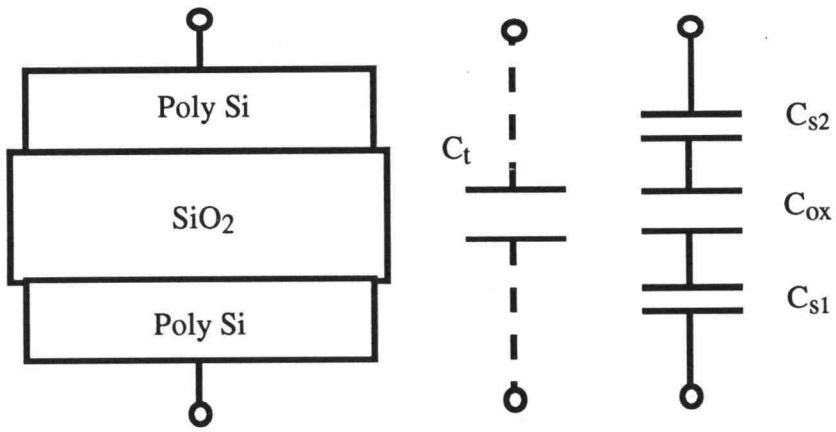
$$\frac{1}{C_t} = \frac{1}{C_{ox}} + \frac{1}{C_{S1}} + \frac{1}{C_{S2}} \qquad (2\text{-}1)$$

This capacitor has a relatively small parasitic capacitance (about 15 % of the main capacitor) associated with its bottom plate because the field oxide between the lower poly layer and the single-crystal silicon substrate is much thicker than the poly-poly oxide.

In some CMOS processes, a capacitor with thermally grown oxide on heavily-doped single-crystal silicon is available as shown in Figure 2.2a. This capacitor has good matching properties and relatively small voltage coefficient for high doping density in the bottom plate [1]. For metal-gate processes, the heavily-doped diffusion layer under the gate oxide can be realized without an extra process step because the source/drain diffusions are



(a)



(b)

Figure 2.1 Double-poly capacitor structure: (a) practical realization; (b) model with two space-charge capacitances [1].

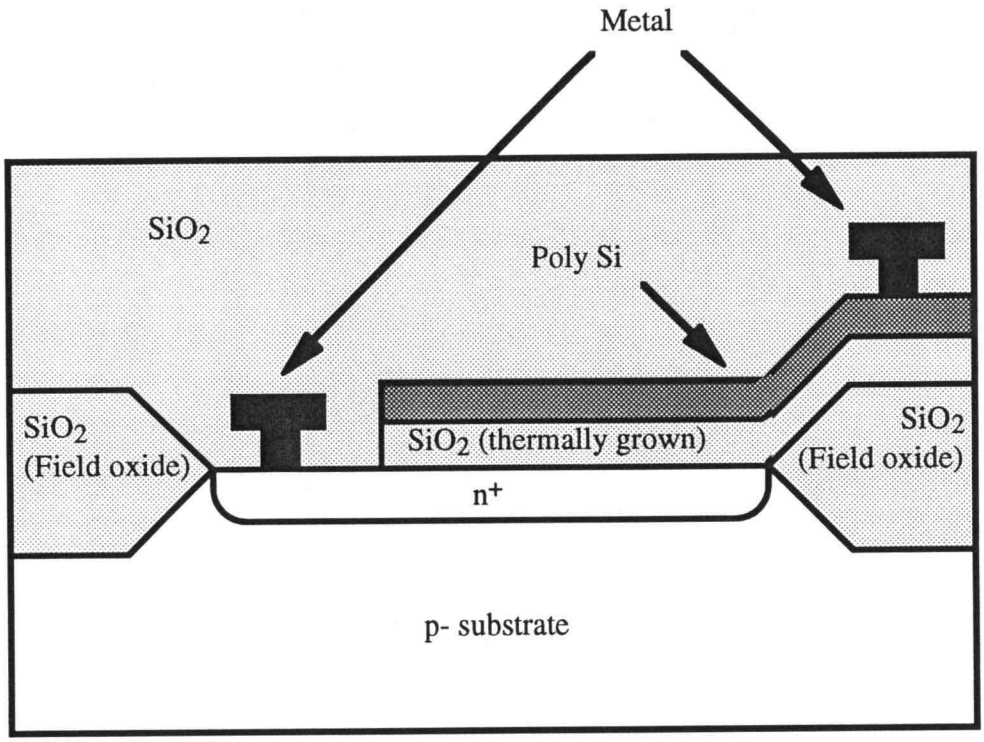


Figure 2.2 Poly-diffusion MOS capacitor structure.

formed before fabricating the metal gate. By contrast, for the self-aligned Si-gate process, which is the current standard for CMOS process, additional process steps are needed for the formation of the heavily-doped diffusion layer under the poly gate.

Again, the total capacitance C_t is given by equation 2-1. Notice that both the poly layer and the single-crystal silicon layer must be equally heavily doped to achieve high linearity. If the single-crystal silicon layer, for example, is more lightly doped than the poly layer, then this layer provides the dominant space charge capacitance (C_{s1} in Figure 2.1b) [1]. In this case, the total capacitance decreases with decreasing bias voltage because the crystalline silicon layer is depleting, its space-charge layer is widening, and consequently C_{s1} decreases.

As the gate oxide becomes thinner in advanced CMOS processes, it becomes more difficult to achieve a low voltage coefficient because the higher-dose capacitor implant associated with the use of thinner oxides can lead to a reduced dielectric breakdown [3].

Table 2-1 shows an example of voltage coefficients of poly/heavily-doped single-crystal silicon capacitors.

Table 2-1 Voltage coefficients of MOS capacitors

	α_V [ppm/V]	N_d [cm^{-3}]	Oxide thickness [Angstrom]	MOS structure
McCreary [1]	7	1.1e20	> 1000 *	poly/SiO_2/n^+
	340	5.5e18	> 1000 *	poly/SiO_2/n^+ (Figure 2.2a)
Slater, Paulos [3]	70	2e20	225	silicide/poly/SiO_2/n^+
	590	4e19	225	silicide/poly/SiO_2/n^+

α_V: the first-order voltage coefficient.

N_d: impurity concentration in heavily-doped silicon.

2.2 Capacitors in Digital CMOS Technology

Several realization for capacitors are available in digital CMOS technologies. However, most of these require large chip area, and have large parasitics and poor matching properties.

The metal-metal capacitor (shown in Figure 2.3) has a low voltage dependence because the metal plate surfaces do not accumulate or deplete. However, the bottom plate, which is aluminum in most cases, has a low melting point, and that mandates the use of low-temperature CVD oxide, which is known to be inferior compared to the thermally-grown oxide in terms of thickness uniformity, dielectric strength, and leakage [3].

* This is an estimate, based on the state of the art at the time of ref. [1].

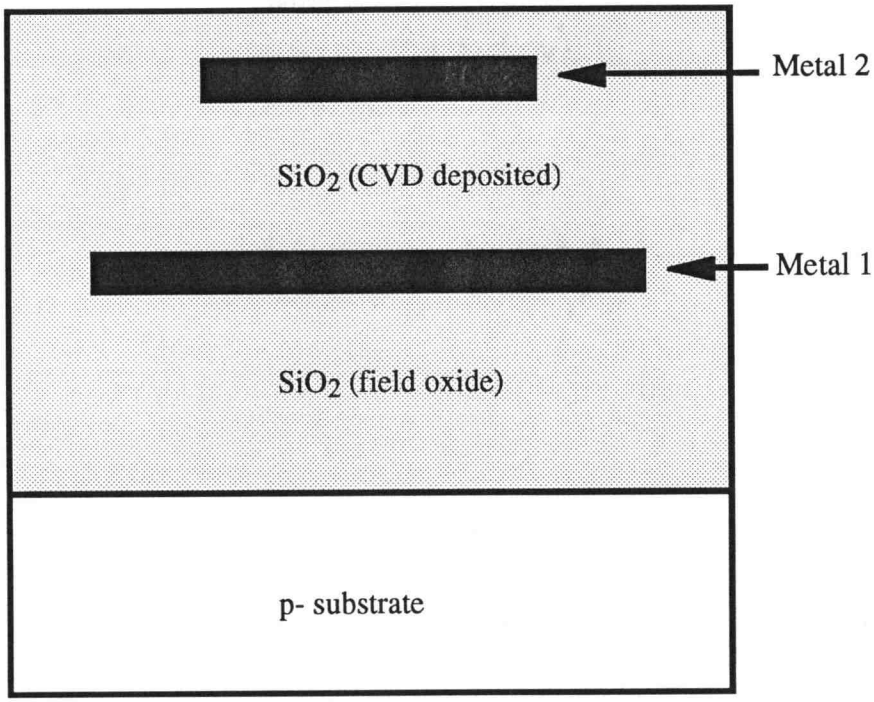


Figure 2.3 Metal-metal capacitor.

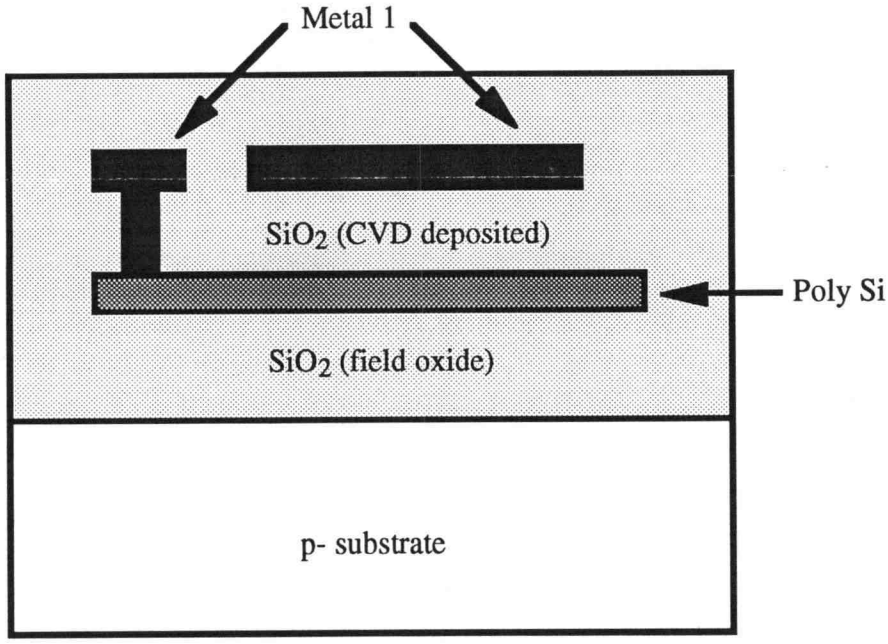


Figure 2.4 Metal-poly capacitor.

The metal-poly capacitor illustrated in Figure 2.4 has a relatively large voltage dependence compared to the metal-metal one because the surface of the poly accumulates or depletes while the surface of the metal does not, and therefore the space-charge capacitance cannot be compensated [3]. In addition, CVD oxide is used as an insulator between the metal and the poly layers, and this results in poor matching property because of its inferior uniformity.

For the capacitors described above, the parasitic capacitance associated with their bottom plates is about 50 to 100 % of the main capacitance, because their parasitic oxide thickness is of the same order as the main capacitor oxide thickness.

These two capacitors can be combined into a sandwich structure by connecting the poly and the upper metal layers to increase the capacitance per unit area. Even in this case, the chip area required is much larger than for double-poly capacitors.

Table 2-2 summarizes the properties of the capacitors described above.

Table 2-2 Capacitors in CMOS processes

Capacitor	Advantages	Disadvantages
Double-poly	Excellent linearity. Good matching property.	Requires additional process steps to a standard digital process.
Poly-diffusion	Moderate linearity. Good matching property. Large capacitance per unit area.	Requires additional process steps to a standard digital process. Small breakdown voltage.
M1-M2	Available in a standard digital process. Good linearity.	Poor matching property . Requires large area. Large parasitics.

Table 2-2 continued

Capacitor	Advantages	Disadvantages
M1-poly	Available in a standard digital process. Moderate linearity.	Poor matching property. Requires large area. Large parasitics.

2.3 MOSFET Capacitor

2.3.1 Gate Structure

In an n-well CMOS process, four types of gate-structure capacitors (MOSFET capacitors) are available [4] as shown in Figure 2.5. (Note that similar capacitors can also be realized in a p-well CMOS process. However, since n-well processes are more often used for fine-line-width processes, only n-well CMOS processes are discussed in this thesis.) Figure 2.5a shows a floating capacitor which operates in its accumulation region. The capacitor of Figure 2.5b is a grounded capacitor which also works in its accumulation region. The bottom plate (p+ channel) has the same potential as the p-substrate, which is permanently connected to Vss. The capacitors of Figures 2.5c-d operate in their strong inversion regions. In Figure 2.5c, the bottom plate of the MOSFET capacitor can be shielded from the substrate noise by connecting the n-well to a clean fixed potential such as V_{DD}. However, this shielding will boost the threshold voltage of this MOSFET capacitor due to the body effect so that higher bias voltage will be required to keep this capacitor in its strong inversion region. In Figure 2.5d, an increase of threshold voltage due to the body effect is unavoidable unless the bottom plate is tied to V_{SS}.

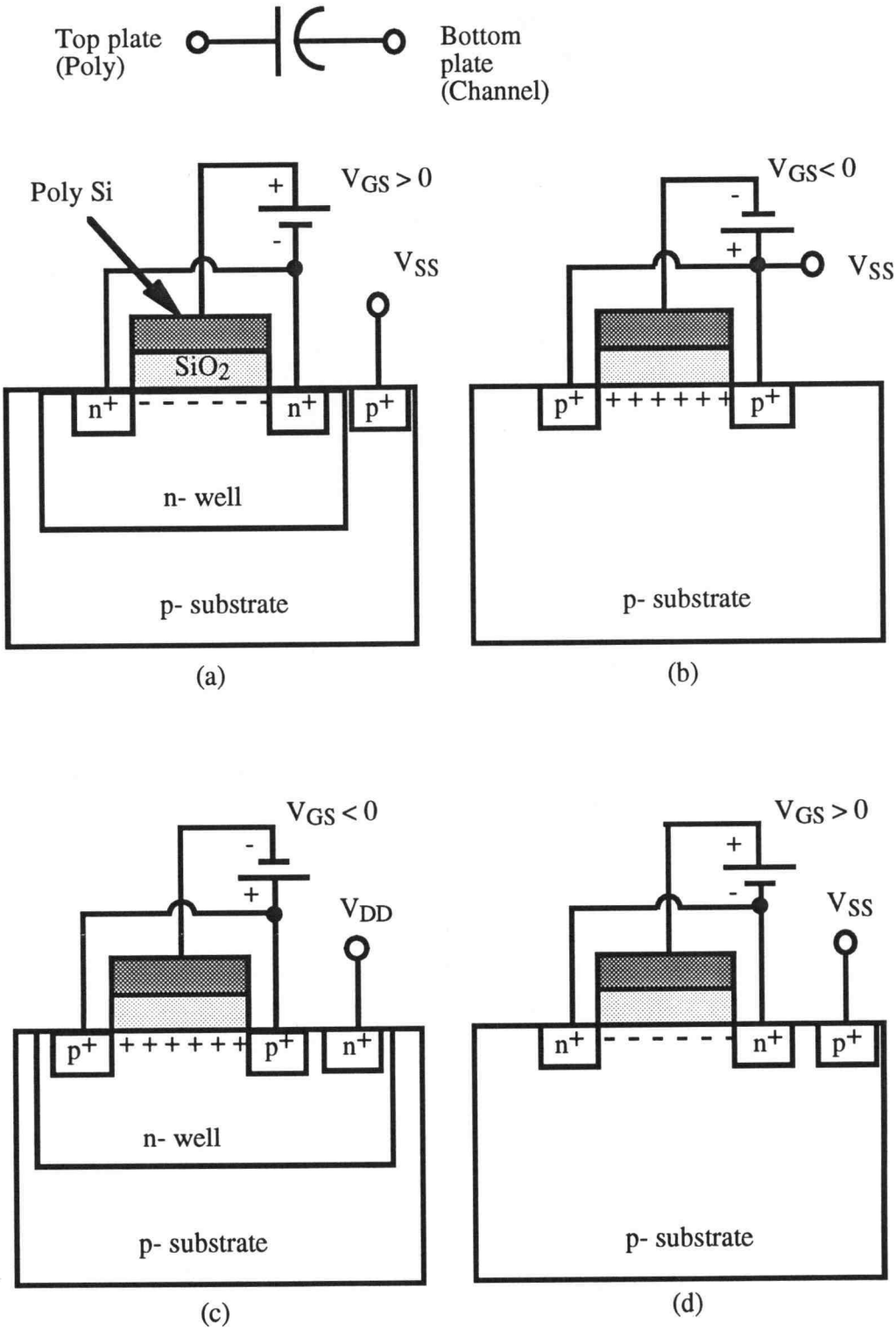


Figure 2.5 MOSFET capacitors.

To implement high-linearity SC circuits, these capacitors have to be sufficiently biased to operate in their accumulation or strong inversion region. The total small-signal gate capacitance is given by

$$C_g^{-1} = C_{ox}^{-1} + C_s^{-1}$$

$$C_g = C_{ox}\left[1 - \frac{2\Phi_t}{|V_{GS} - V| + 2\Phi_t}\right] \qquad (2\text{-}2)$$

where Φ_t is the thermal voltage, V_{GS} is the gate-to-source voltage, V is the flatband voltage (V_{FB}) for accumulation or the threshold voltage (V_{TH}) for strong inversion, C_{ox} is the gate-oxide capacitance, and C_s is the space-charge capacitance of the single-crystal silicon [4]. Therefore, V_{GS} has to be large enough to achieve $C_g = C_{ox}$ for good linearity. (The space-charge capacitance of the poly layer is neglected in equation 2-2 because of the high poly doping density normally used.)

Notice that all four capacitors can be realized in any conventional n-well CMOS process without additional process steps such as the second poly layer. Thus they are compatible with digital CMOS processes.

For the capacitors of Figures 2.5a,c and d, the bottom plate (n-well) has a parasitic pn junction diode, which has a nonlinear C-V characteristic. This parasitic capacitance and its effects will be discussed in Sections 2.3.3 and 4.3.

2.3.2. C-V Characteristic

The capacitance-voltage (C-V) characteristics of MOSFET capacitors are among the most important issues in this research because the linearity of MOSFET capacitors can limit the linearity of SC circuits.

The C-V characteristics of two MOSFET capacitors with the structures of Figure 2.5a-b were measured using the HP4061 C-V meter as illustrated in Figure 2.6, and the measured C-V curves are shown in Figure 2.7. The DC bias voltage was swept between -5

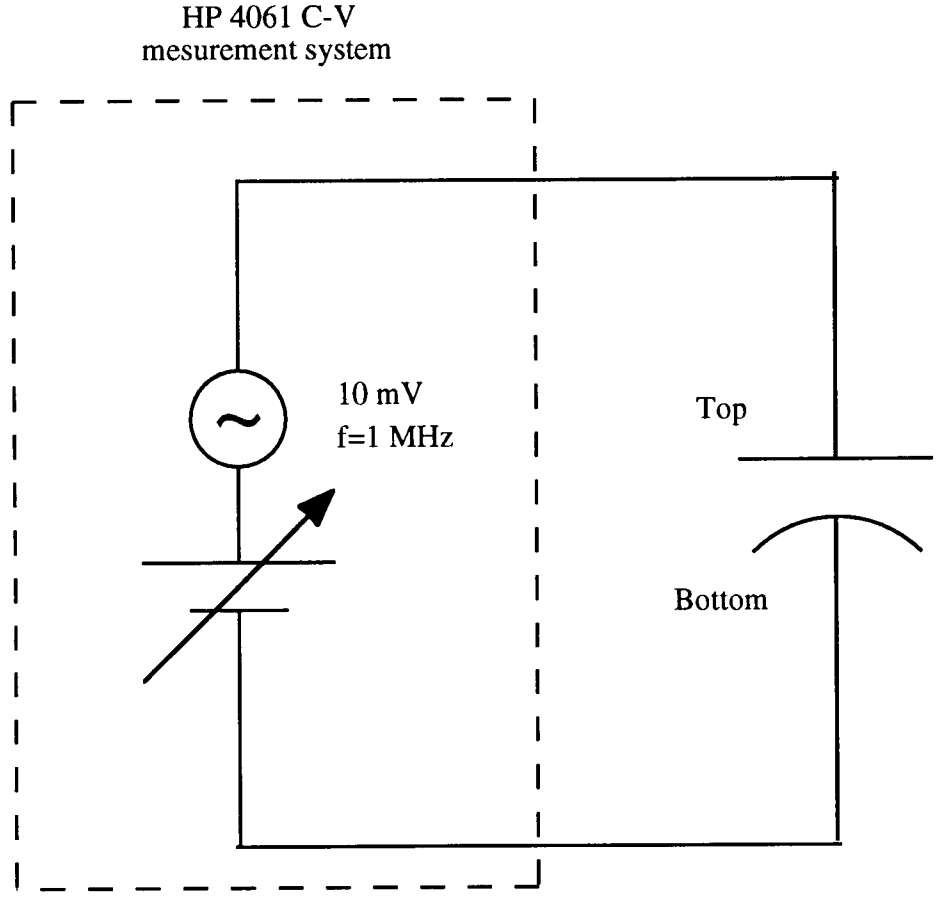


Figure 2.6 C-V curve measurement of MOSFET capacitors

and 5 V while a sinusoidal voltage signal of 10 mV peak amplitude with a frequency of 1 MHz was applied. And the capacitance C was defined as C=dq/dv.

The electron-accumulated structure of Figure 2.5a can be operated in its accumulation region by applying a positive bias voltage or in its strong inversion region by using a negative bias voltage. As shown in Figure 2.7a, its capacitance is close to gate-oxide capacitance C_{ox} even without a bias voltage (V=0) because near the interface between the single-crystal silicon and SiO_2 positive fixed oxide charges exist [5] and they attract electrons to the surface of the single-crystal silicon.

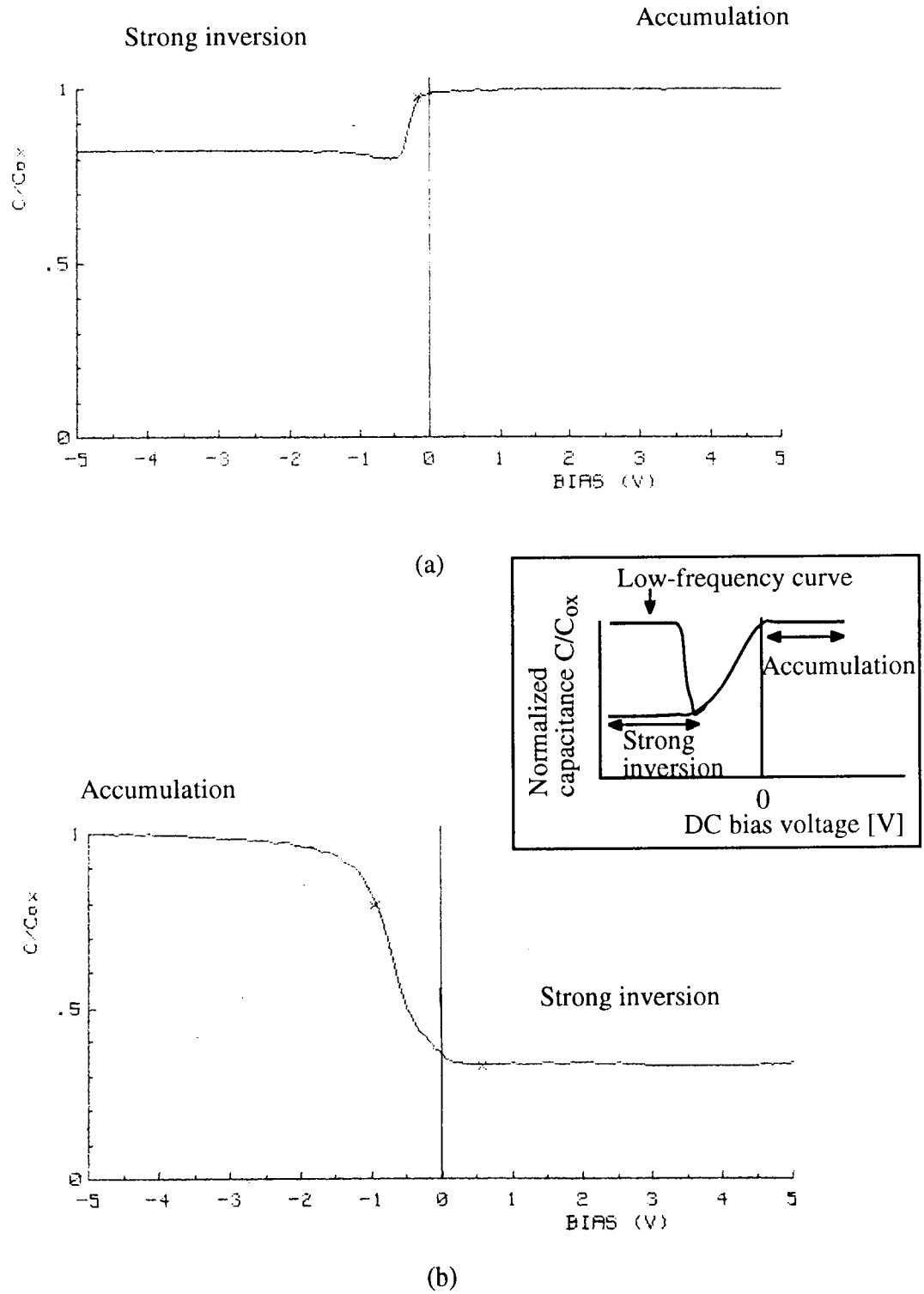


Figure 2.7 Measured C-V curves of MOSFET capacitors:
(a) electron-accumulated MOS structure (Figure 2.5a);
(b) hole-accumulated MOS structure (Figure 2.5b).
The insert shows the frequency effect.

The first-order voltage coefficient was 850 ppm/V for the operating dc bias range between 0.5 V and 5 V, which corresponds to the range with sufficiently accumulated channel at the surface of the single-crystal silicon. When a negative DC bias voltage is applied to this capacitor, the space-charge layer which is in series with the gate-oxide capacitance depletes, and finally the surface of the n-well inverts as the negative bias voltage increases. In this structure, the only source for positive charge is minority carriers in the n-well (holes in this case) and the recombination-generation rates of the minority carriers cannot keep up with the high-frequency small-signal variations [5]. Hence in strong inversion, the total capacitance decreases for high-frequency signal and has a strong frequency dependence. (If the AC signal frequency is very low, e.g. 100 Hz, the total capacitance rises to C_{ox} because the minor carriers can follow the signal and the depletion-layer capacitance increases. See the insert in Figure 2.7)

The measured C-V curve for the hole-accumulated structure of Figure 2.5b is shown in Figure 2.7b. With a negative bias voltage, this capacitor is kept in its accumulation region and the capacitance approaches to C_{ox}. The first-order voltage coefficient was 12,300 ppm/V for the operating dc bias range between -2 V and -5 V, in which holes are accumulated at the surface of the single-crystal silicon. With a positive dc bias voltage, the surface of the p-substrate inverts and the electron channel is formed (strong inversion). A small dc bias voltage is required to keep this capacitor in the strong inversion region, and its linearity is much better there than in its accumulation region. However, again, the capacitance in the strong inversion is frequency-dependent and it decreases for high-frequency signal because its minor carriers in the p-substrate (in this case, electrons) cannot follow the high-frequency signal, and the depletion layer capacitance, which is in series with C_{ox}, limits the total capacitance.

Therefore, both structures of Figures 2.5a-b have to operate in their accumulation region when they are used in SC circuits; otherwise they will show a frequency dependence along with the dc bias voltage dependence.

As shown in Table 2-3, the voltage coefficient in the accumulation region of Figure 2.7a was much smaller than that of Figure 2.7b. The reason is as follows. Figure 2.8 illustrates two poly/SiO_2/Si structures and their space-charge layers. In Figure 2.8a, the surfaces of the poly and n-well are depleting and space-charge layers are facing the SiO_2 surface. In a typical CMOS process, the poly layer is n+ doped. Therefore the impurity polarity of the poly is the same as of the n-well. When a positive gate voltage V_G is applied, the space-charge layer in the poly increases while it decreases in the n-well. When a negative gate voltage is applied, the space-charge layer in the poly decreases while it increases in the n-well. Thus, the variation of their space-charge layer thickness is compensated. (Since the poly is much heavily doped more than the n-well, they do not compensate completely. However, even the partial compensation results in a reduced voltage coefficient.) In Figure 2.8b, the surfaces of the poly and the p-substrate are also depleting. Note that the poly and the p-substrate have opposite impurity polarities. When a positive gate voltage V_G is applied, both space-charge layers in the poly and in the n-well increase. When a negative gate voltage is applied, both space-charge layers in the poly and in the n-well decrease. Therefore, the variation of their space-charge layer thickness is much larger than of the structure in Figure 2.8a, and that results in the large voltage coefficient.

Table 2-3 Measured voltage coefficients of MOSFET capacitor structures

MOSFET structure	α_V [ppm/V]	Operating dc bias voltage [V]
poly/SiO_2/n-well (Figure 2.5a)	850	$0.5 < V < 5.0$
poly/SiO_2/p-substrate (Figure 2.5b)	12,300	$-5.0 < V < -2.0$

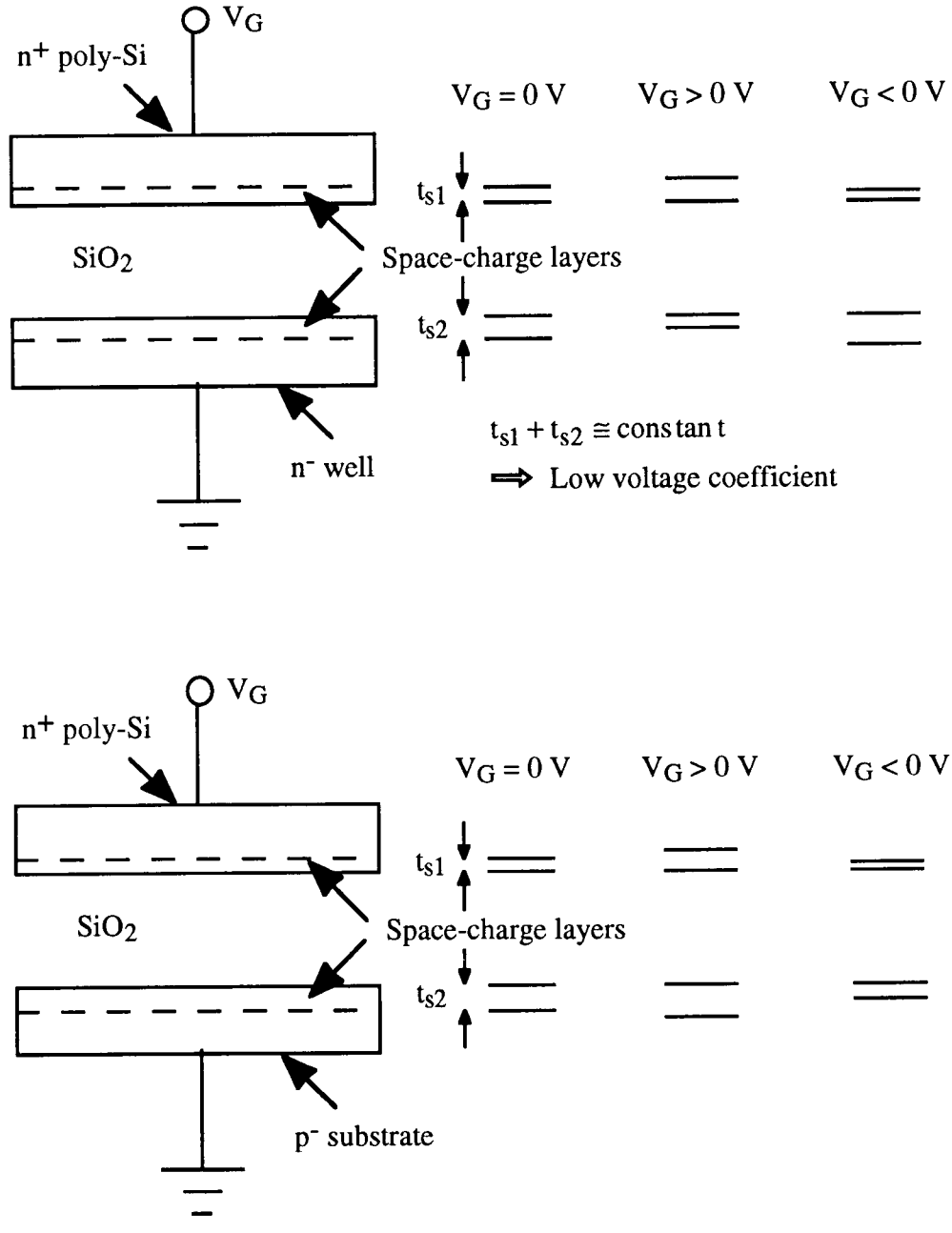


Figure 2.8 Space-charge layers: (a) poly-Si/n-well; (b) poly-Si/p-substrate.

It should be also pointed out that the electron-accumulated MOS structure requires a smaller minimum bias voltage (around 0.5 V) than the hole-accumulated MOS structure (around -2 V) to operate in the accumulation region. This can be explained as follows. Figure 2.9 illustrates the charges at the interface of SiO_2 and single-crystal silicon: Q_{it} is the interface-trapped charge and Q_f is the fixed oxide charge. The interface-trapped charge (sometimes called fast state or surface state charge) is due to the interruption of the periodic lattice structure at the surface of the silicon [5] and is known to cause 1/f noise. (The effect of the 1/f noise will be discussed in Section 6.4.11) The fixed oxide charge Q_f originates from excess silicon or the loss of an electron out of excess oxygen centers near the Si-SiO_2 interface, and it has the following properties [5]: it is fixed and generally positive; it cannot be charged or discharged over a wide variation of surface potential. When the fixed oxide charge is present at the interface, a MOS C-V curve shifts along the voltage axis as shown in Figure 2.10. In Figure 2.10a, the positive fixed oxide charges help the electron-accumulated capacitor operate in accumulation region with smaller bias voltage because they attract negative charges to the surface of the crystal silicon. By contrast, due to the positive fixed oxide charges, the hole-accumulated capacitor must have a larger negative dc bias voltage to operate in its accumulation region (Figure 2.10b).

Next consider the two inverted-channel MOSFET structures of Figures 2.5c-d.

Since we didn't have test structures of Figure 2.5c-d, no measured results are available. However, in refs.[4][9][24], measured C-V curves of MOSFET capacitors with the structure of Figure 2.5c-d are shown. For example, in reference [9], the measured first-order voltage coefficient α_V in strong inversion was given as 42.7 kppm/V and 27.9 kppm/V for the structures of Figure 2.5c and d, respectively (Table 2-4). Their C-V curves do not have a frequency dependence in strong inversion, and their total capacitances in the strong inversion region approach the gate-oxide capacitance C_{ox} even for a high-frequency signal, because they have source/drain p+ or n+ diffusions, and channel carriers are provided rapidly enough to follow the high-frequency signal.

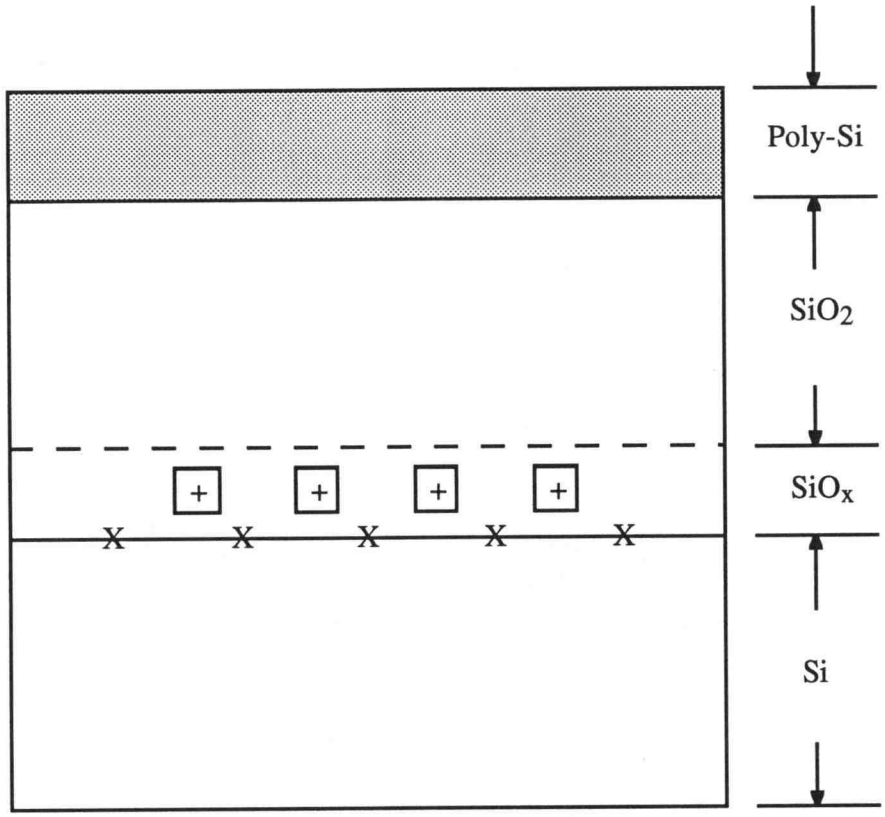


Figure 2.9 Charges at the interface of SiO_2 and single-crystal silicon [5].

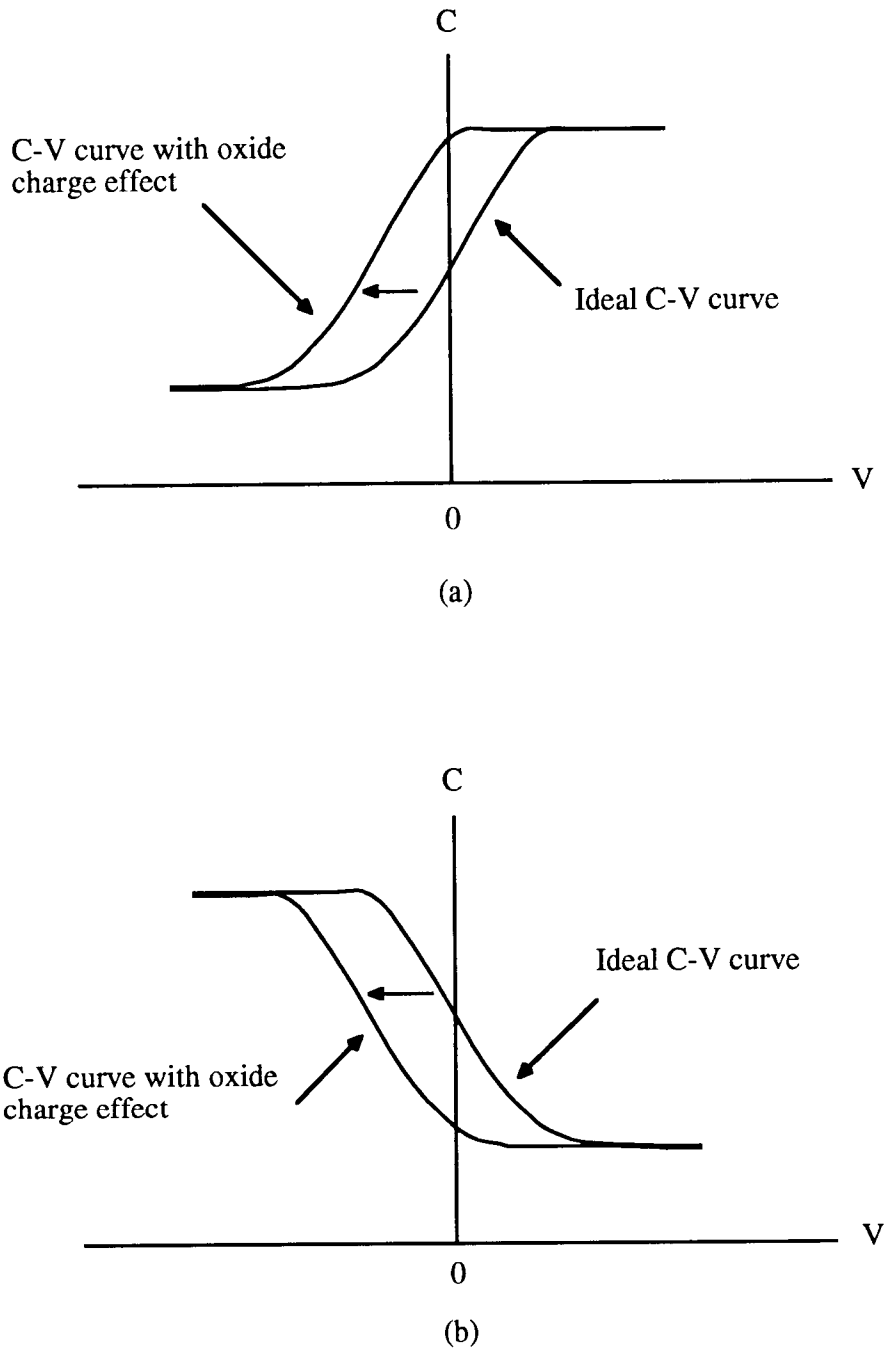


Figure 2.10 C-V curve shift due to positive fixed oxide charge [5]: (a) electron-accumulated MOS structure; (b) hole-accumulated MOS structure.

Table 2-4 Voltage coefficients of MOSFET capacitor structures [9]

MOSFET structure	α_V [ppm/V]	Operating dc bias voltage [V]
PMOSFET (Figure 2.5c)	42,700	-3.0 < V < -2.0
NMOSFET (Figure 2.5d)	27,900	2.0 < V < 3.0

It is easily realized that these structures require bias voltages at least equal to their threshold voltages to operate in their strong inversion regions. When the body effect is incorporated, even larger voltage will be needed to achieve good linearity.

Among the four structures described above, the MOSFET capacitor with accumulated electrons at the surface of the single-crystal silicon (Figure 2.5a) was found to be the most useful because it shows a smaller voltage coefficient than other structures and requires a small dc bias voltage to operate in a good linearity region. Therefore throughout this thesis, it will be used to design SC circuits in digital CMOS processes.

2.3.3 Parasitics

In this section, the parasitic capacitances of the MOSFET capacitor are discussed. As already mentioned, the electron-accumulated MOSFET capacitor will be used in this thesis. This capacitor has a nonlinear parasitic capacitance at its bottom plate and a relatively linear stray capacitance at its top plate (Figure 2.11). We shall estimate the parasitic capacitance at the bottom plate first. Then the effect of the top parasitic capacitance will be discussed.

Figure 2.12 illustrates a 1 pF unit MOSFET capacitor laid out with the MOSIS 1.2 μm design rule. The width of the depletion layer between the p-substrate and the n-well is given by

$$d = \sqrt{\frac{2\varepsilon_{Si}}{q}\frac{N_A + N_D}{N_A N_D}(V_{bi} + V)} \qquad (2\text{-}3)$$

where ε_{si} is the permittivity of silicon, q is the electron charge, N_A is the acceptor impurity concentration, N_D is the donor impurity concentration, V_{bi} is the built-in potential, and V is the reverse voltage for the pn junction [5]. We assume the following physical parameters for a standard CMOS process:

$$N_D = 2\times10^{16}[cm^{-3}],\ N_A = 5\times10^{14}[cm^{-3}],\ V_{bi} = 0.64[V],\ q = 1.6\times10^{-19}[C],$$

$$\varepsilon_{si} = 11.7\cdot 8.854\times10^{-14}[F/cm]$$

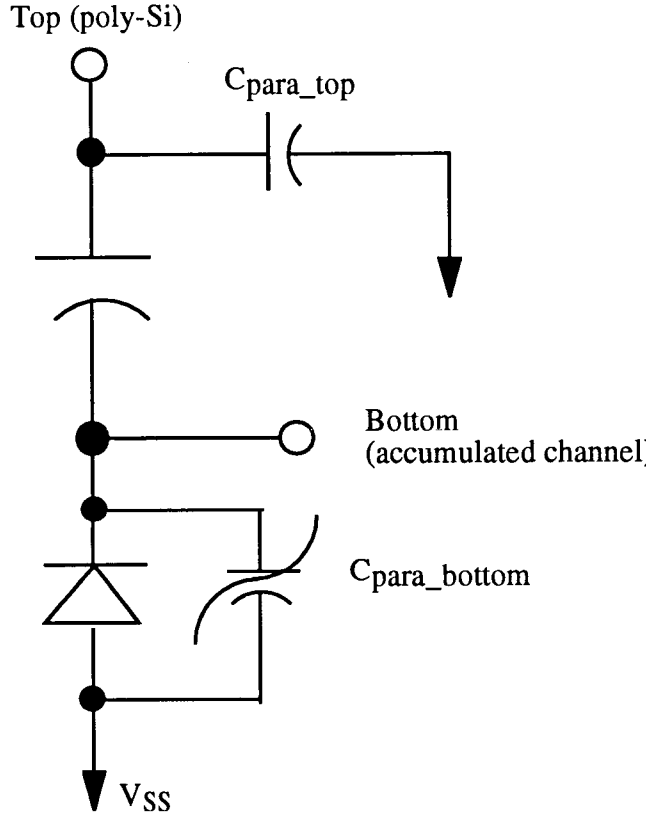


Figure 2.11 Parasitic capacitances of MOSFET capacitor

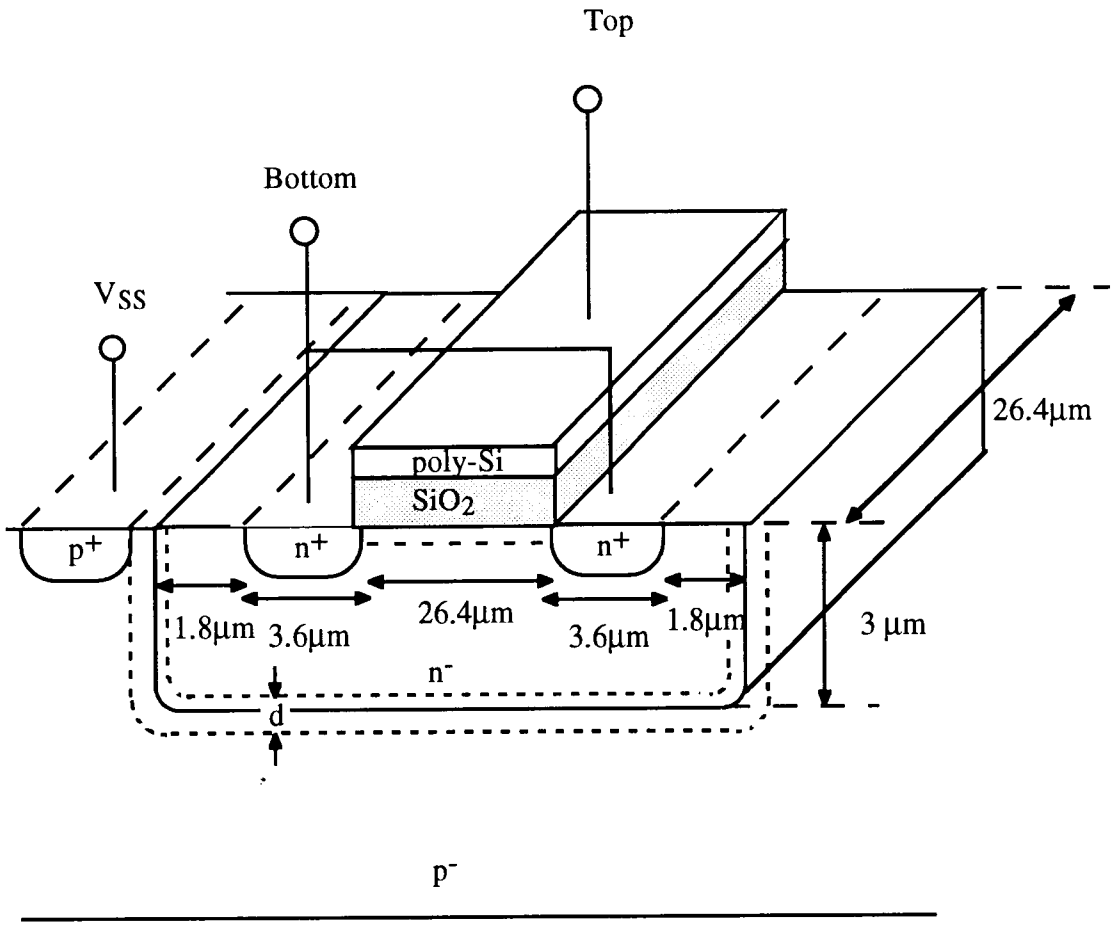


Figure 2.12 MOSFET unit capacitor

For V=0 V, the depletion-layer width is given by

$$d = \sqrt{\frac{2 \cdot 11.7 \cdot 8.854 \times 10^{-14}\left(2 \times 10^{16} + 5 \times 10^{14}\right)}{1.6 \times 10^{-19} \cdot 2 \times 10^{16} \cdot 5 \times 10^{14}}(0.64 + 0)} \qquad (2\text{-}4)$$

$$= 1.31 \times 10^{-4}\,\text{cm}$$

The pn junction capacitance per unit area is given by

$$C = \frac{\varepsilon_{si}}{d} = \frac{11.7 \times 8.854 \times 10^{-14}}{1.31 \times 10^{-4}} = 7.9 \times 10^{-9} [F/cm^2]$$
$$= 7.9 \times 10^{-5} [F/m^2] \qquad (2\text{-}5)$$

Then the parasitic capacitance C_{par} is calculated as

$$C_{par} = C_{bottom} + C_{sidewall}$$
$$= 7.9 \times 10^{-5} \cdot 37.2 \times 10^{-6} \cdot 33.6 \times 10^{-6}$$
$$+7.9 \times 10^{-5} \cdot 3 \times 10^{-6} \cdot 2 \cdot (37.2 + 33.6) \times 10^{-6} \qquad (2\text{-}6)$$
$$= 0.13 pF$$

This is a worst case because the reverse voltage V was assumed to be equal to 0 V. As the reverse voltage increases, the depletion layer widens, and consequently C_{par} decreases. For example, when V is increased to 2.5 V, the depletion-layer width increases to 2.88 μm, and C_{par}=0.06 pF. In this case, the parasitic capacitance is only 6 % of the main capacitance.

Thus, the parasitic capacitance at the bottom plate of this unit capacitor is estimated as only 15 % or less of the main capacitance. This value is of the same order as for the double-poly capacitor and is much smaller than for the metal-metal or metal-poly capacitor. However, this parasitic capacitance is nonlinear, and hence the bottom plate should not be a floating node to avoid nonlinear distortion. The effect of the nonlinear parasitic capacitance on SC circuits will be discussed in Section 4.3.

Next consider the parasitic capacitance associated with the top plate of the MOSFET capacitor. As illustrated in Figure 2.13, the top plate (poly layer) overlaps the field oxide. Its thickness is not constant due to the birds-beak shape of the field oxide, hence it is not straightforward to estimate the parasitic capacitance quantitatively. However, since the thickness of the field oxide is 4000 to 8000 angstrom, and the overlap width is about 10 % of the MOSFET width, the parasitic capacitance is expected to be less than 10 % of the

main capacitance. To minimize the matching error due to these parasitics, a parallel combination of several smaller unit capacitors will be used in the layout [6].

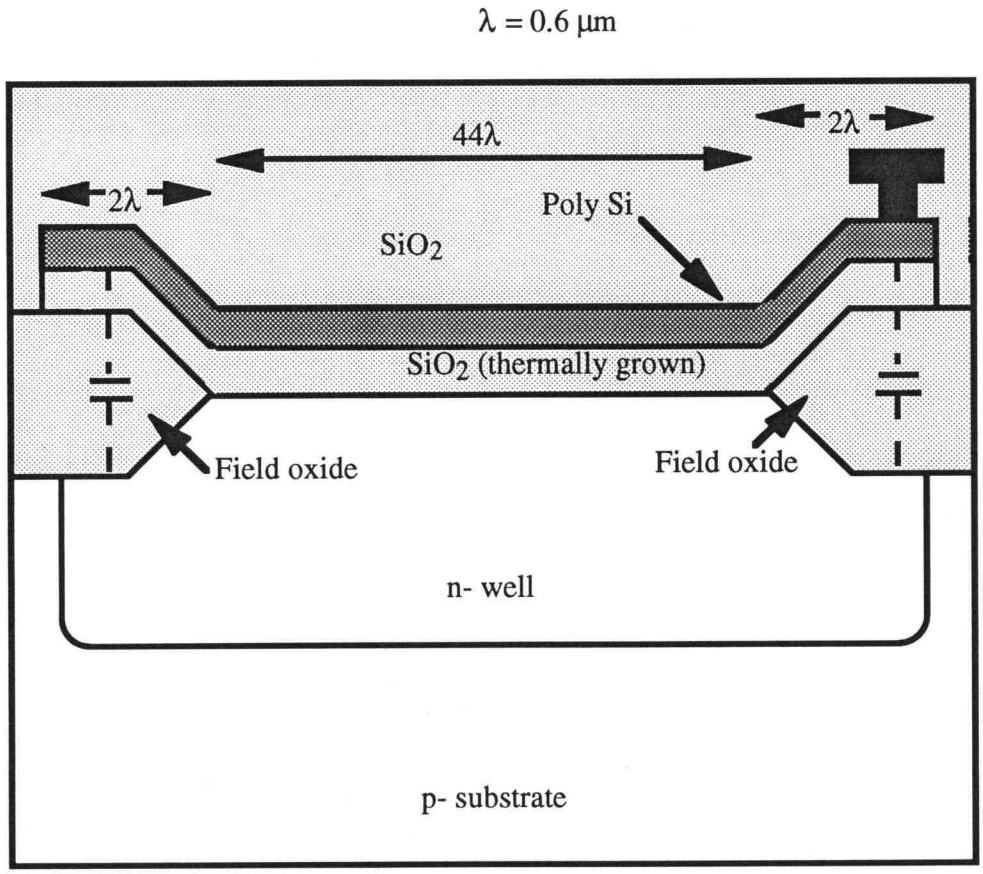


Figure 2.13 Profile of MOSFET capacitor

2.3.4 HSPICE Models

In this section, the models for the MOSFET capacitor and the pn junction diode which have been used in HSPICE simulations will be discussed.

2.3.4.1 MOSFET Capacitor Model

The Level-2 HSPICE models optimized for the Orbit 1.2 μm CMOS process have been used throughout this thesis. HSPICE provides several MOS gate capacitance models, and they are selected by the CAPOP command [7] as follows:

CAPOP=0 Original Meyer model in SPICE

CAPOP=1 Modified Meyer model

CAPOP=2 Parameterized modified Meyer model (default)

CAPOP=3 Parameterized modified Meyer model with Simpson integration

CAPOP=4 Charge conservation model

Figure 2.14 shows simulated PMOSFET C-V curves for different CAPOP values: (a) 0; (b) 1; (c) 2; (d) 3; (e) 4. For CAPOP = 0 and 4, the PMOSFET capacitance was constant in both accumulation (V > 0.5 V) and strong inversion regions (V < -1.5 V), that is, they did not show any nonlinear behavior in those regions (Figure 2.14a, e). By contrast, the MOSFET capacitances with CAPOP = 1, 2, 3 (Figure 2.14b, c, d) show weakly nonlinear behavior in the accumulation region (V > 0.5 V), relatively strongly nonlinear behavior in the strong inversion (V < -1 V), and very strongly nonlinear behavior in the depletion region (-1 < V < 0.5 V). No big differences were observed among the three CAPOPs. To include the weak nonlinearity of the MOSFET capacitor in the accumulation region, CAPOP=2 was chosen for HSPICE simulations in this work.

Next, the PMOSFET and NMOSFET C-V curves are compared. Figure 2-15 shows the C-V curves of the PMOSFET and NMOSFET for CAPOP=2. Their first-order voltage coefficients of these MOSFETs are shown in Table 2-5 and 2-6, respectively. Both MOSFETs have a much better linearity in their accumulation region than in the strong inversion region. The first-order voltage coefficient of the PMOSFET is 750 ppm/V for the dc bias range of 0.5-2.5 V, and that of the NMOSFET is 610 ppm/V between -3 and -1 V. In the experimental results described in Section 2.3.2, the first-order voltage coefficient of the MOSFET capacitor with the structure of Figure 2.5a was 850 ppm/V for the operating

dc bias range between 0.5 and 5 V. Therefore the simulated PMOSFET C-V curve is closer to that of the electron-accumulated MOSFET capacitor in accumulation region, and the PMOSFET model was adopted to simulate the MOSFET capacitor in HSPICE, even though the actual structure used (Figure 2.5a) was an n-channel one.

Table 2-5 Voltage coefficients of the HSPICE PMOSFET capacitor model

Operating mode	α_V [ppm/V]	Operating dc bias voltage [V]
Accumulation	750	$0.5 < V < 2.5$
Strong inversion	21,200	$-3.0 < V < -1.0$

Table 2-6 Voltage coefficients of the HSPICE NMOSFET capacitor model

Operating mode	α_V [ppm/V]	Operating dc bias voltage [V]
Strong inversion	23,500	$1.0 < V < 3.0$
Accumulation	610	$-2.7 < V < -0.7$

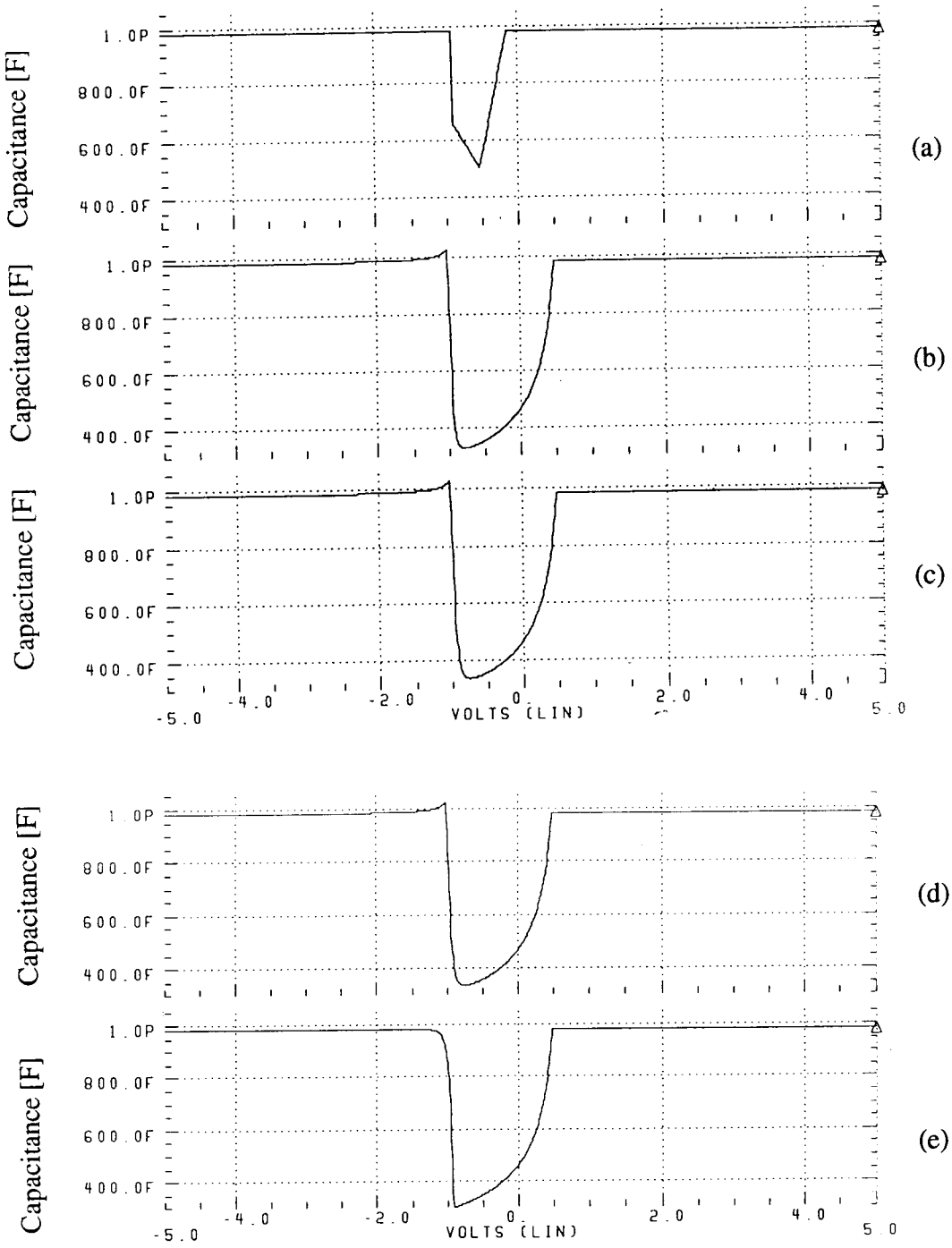


Figure 2.14 Simulated C-V curves of PMOSFET for different CAPOP values: (a) 0; (b) 1; (c) 2; (d) 3; (e) 4

Note that this model has discontinuities at the boundary of the depletion and accumulation (or strong inversion) regions. However, if MOSFET capacitors operate only in their accumulation regions in HSPICE simulations, this model can achieve a good agreement with actual devices. (Remember that the accumulation region of the electron-accumulated MOSFET capacitor is the most important one among all MOSFET capacitor configurations.)

In addition, it should be pointed out that the slope d(C/Cox)/dV in the accumulation region of the simulated PMOSFET C-V curve is negative as shown in Figure 2.15c, while it is positive in a real device. However, the absolute value of the voltage coefficient is more important than the polarity of the slope when the nonlinearity of the MOSFET capacitor is taken into account for circuit simulations, and hence using the wrong polarity will not give a serious problem on simulation results.

2.3.4.2 PN Junction Diode Model

Since a MOSFET capacitor has a parasitic pn junction diode at its bottom plate, a pn junction diode model should be connected at the bottom plate of each MOSFET capacitor in HSPICE simulations.

Based on the physical parameters described in Section 2.3.3, the C-V curve for a pn junction diode was obtained. The bottom plate area is 37.2 μm x 33.6 μm, the peripheral length of the sidewall pn junction is 2 x (37.2 μm + 33.6 μm), and the n-well depth is estimated as 3 μm. Figure 2.16 shows a simulation result of C-V curve for the pn junction diode. This simulation result agrees with the analytical result in Section 2.3.3.

2.3.5 Accuracy Considerations

Two factors determine the accuracy of MOS capacitors: systematic and random errors. These errors have been extensively investigated in refs.[1][2][6][8].

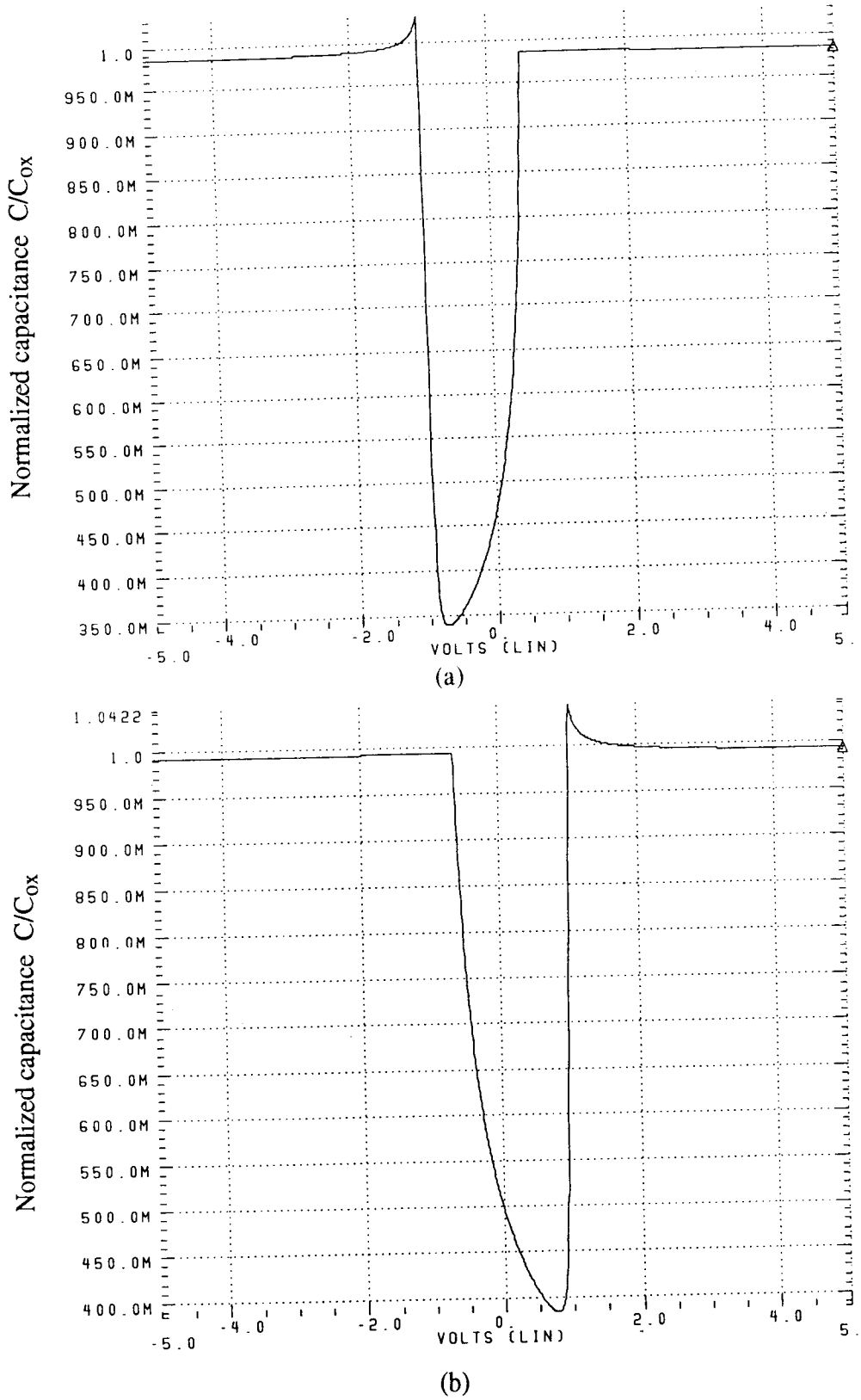
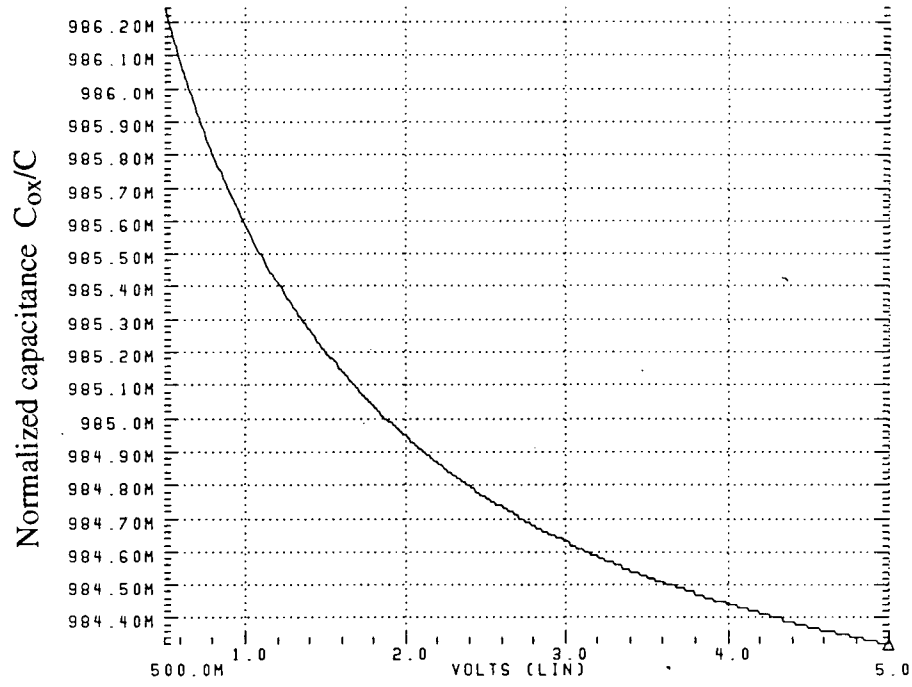


Figure 2.15 Simulated C-V curves for CAPOP=2: (a) PMOSFET; (b) NMOSFET; (c) magnified PMOSFET C-V curve ($0.5 < V < 5$ [V]).



(c)

Figure 2.15 continued.

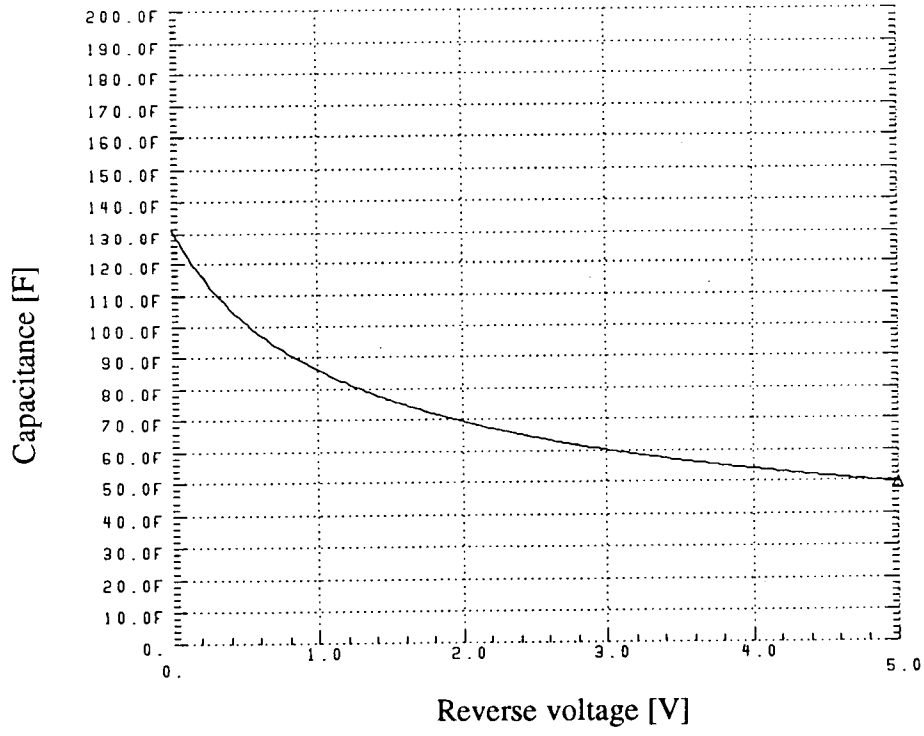


Figure 2.16 Simulated C-V curve of the pn junction diode

Systematic errors affect capacitors with identical geometries equally, hence they can be reduced by unit-capacitor layout and common-centroid geometry [6] as shown in Figure 2-17.

By contrast, random errors are uncorrelated from capacitor to capacitor and they cannot be improved by layout techniques. They are divided into two categories: random edge effect and random oxide thickness effect.

The nominally straight edges of the top layer (poly or metal) of a MOS capacitor are wavy in a practical fabrication process due to the granular nature of the poly (or metal) and the jagged edges of the developed photoresist [8]. This is called random edge effect. The expected relative error $\Delta C/C$ is proportional to $C^{-3/4}$ [6].

Random oxide effect is caused by fluctuations of the oxide thickness and permittivity. The expected relative error $\Delta C/C$ is proportional to $C^{-1/2}$ [6].

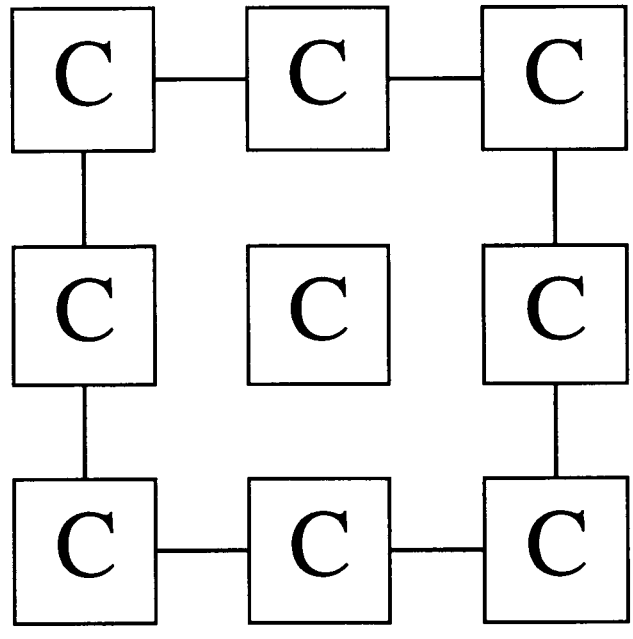


Figure 2.17 Unit capacitors with common-centroid geometry

When a capacitance is small, the edge effect dominates; by contrast, oxide effects limits the accuracy for a large capacitance. Although the crossover value depends on technologies, it is estimated around L = 20 to 50 μm [6].

2.3.6 Layout

In this Section, the practical layout of a MOSFET capacitor will be presented. Some remarks associated with CAD tools will be also made.

Figure 2.18a shows a possible layout of a unit MOSFET capacitor. To implement the structure of Figure 2.5a, n+ diffusions are formed inside the n-well. A p+ guard ring surrounds the capacitor to reduce substrate noise.

The following remarks should be taken into account for the Mentor layout tool. They can also be applied to other CAD tools.

1. When a design-rule check (DRC) is run on the MOSFET capacitor with the gate structure of Figure 2.5a, a design error message "N-type gate must not be in n-well" will appear, because n+ regions are formed inside an n-well for the MOSFET capacitor. However, one can ignore this DRC error if it relates only to the MOSFET capacitor, and it should not cause a problem in fabrication.

2. When the layout is completed, it is advisable to extract devices and parasitics to run a post-layout simulation. Before extraction of the MOSFET capacitors, the n+ implant-select layer, which determines an area where n+ doping is given, must be replaced by the p+ implant-select layer (Figure 2.18b) so that the CAD tool can recognize them as PMOSFETs. Otherwise, the CAD tool will not be able to extract the MOSFET capacitors because the n-type gate is formed in the n-well.

This operation should be done only for the post-layout simulation. In the final layout file, all MOSFET capacitors must have the N+ IMPLANT-SELECT LAYERS instead of the p+ implant-select layers as it was originally laid out.

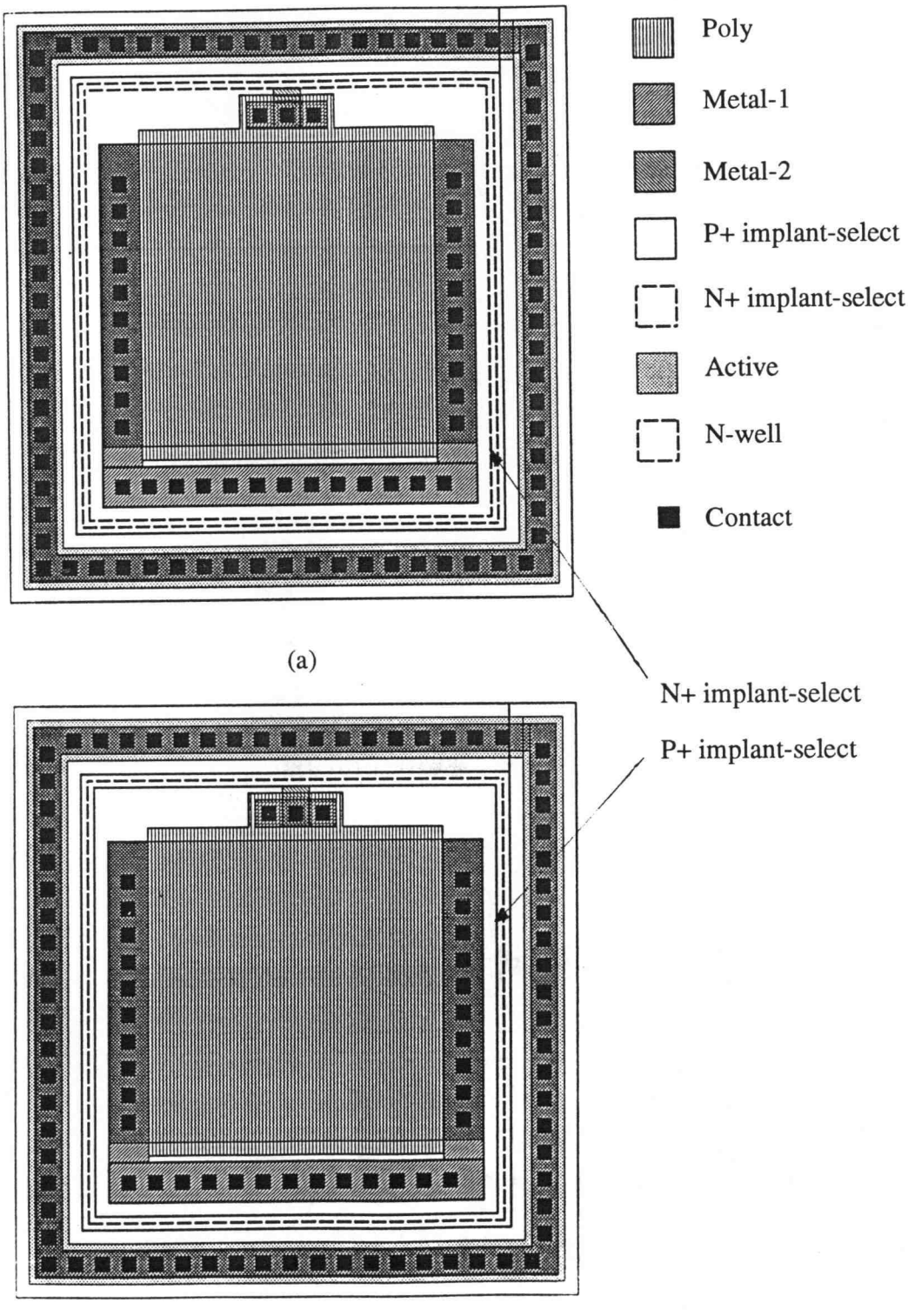


Figure 2.18 Layout of unit MOSFET capacitor:
(a) original; (b) with dummy p+ implant-select layer.

3. When a post-layout simulation is performed by HSPICE, a PMOSFET model should be used for the MOSFET capacitor as it is extracted.

4. In the HSPICE netlist file generated, parasitic capacitors can be extracted as linear components even if some capacitances, such as pn junction capacitance between n-well and p-substrate, are nonlinear. If the circuit is very sensitive to parasitic pn junction capacitances and one wants to see their effects in post-layout simulations, it is necessary to put them manually in the extracted netlist file.

Chapter 3

EARLIER TECHNIQUES FOR LINEAR ANALOG SIGNAL PROCESSING IN DIGITAL CMOS TECHNOLOGY

In this chapter, earlier research results on the realization of SC circuits using MOSFET capacitors and on other analog signal processing techniques without linear capacitors are described. For illustration, sample-and-hold circuits are described which can be realized using nonlinear capacitors.

3.1 Simple Biasing

Figure 3.1 shows an example of how MOSFET capacitors can be operated in their accumulation or strong inversion regions to achieve high linearity in a lossy SC integrator circuit [4]. Since the non-inverting node of the operational amplifier (op-amp) is connected to a bias voltage V_b, the dc voltage of the virtual ground also becomes V_b assuming that the op-amp is ideal. Thus, if V_b is large enough, all capacitors in this circuit can be kept in their accumulation or strong inversion regions according to the polarity of V_b and the MOS gate structure. Notice that the voltage difference between V_b and the input (or output) voltage must be large enough to keep all MOSFET capacitors in the high-linearity regions over the full signal range.

Bazarjani et al. designed a fourth-order SC bandpass delta-sigma modulator using such simple biasing technique [10]. The bandpass modulator consists of cascaded resonators. Each resonator was implemented with two SC delay cells in a negative feedback loop. PMOSFET capacitors were used in the SC delay cells and were kept in their strong inversion region using a simple biasing technique. Their simulation results showed a S/(THD+noise) ratio 28.5 dB (vs. a simulated 36 dB) over a band of 5 MHz.

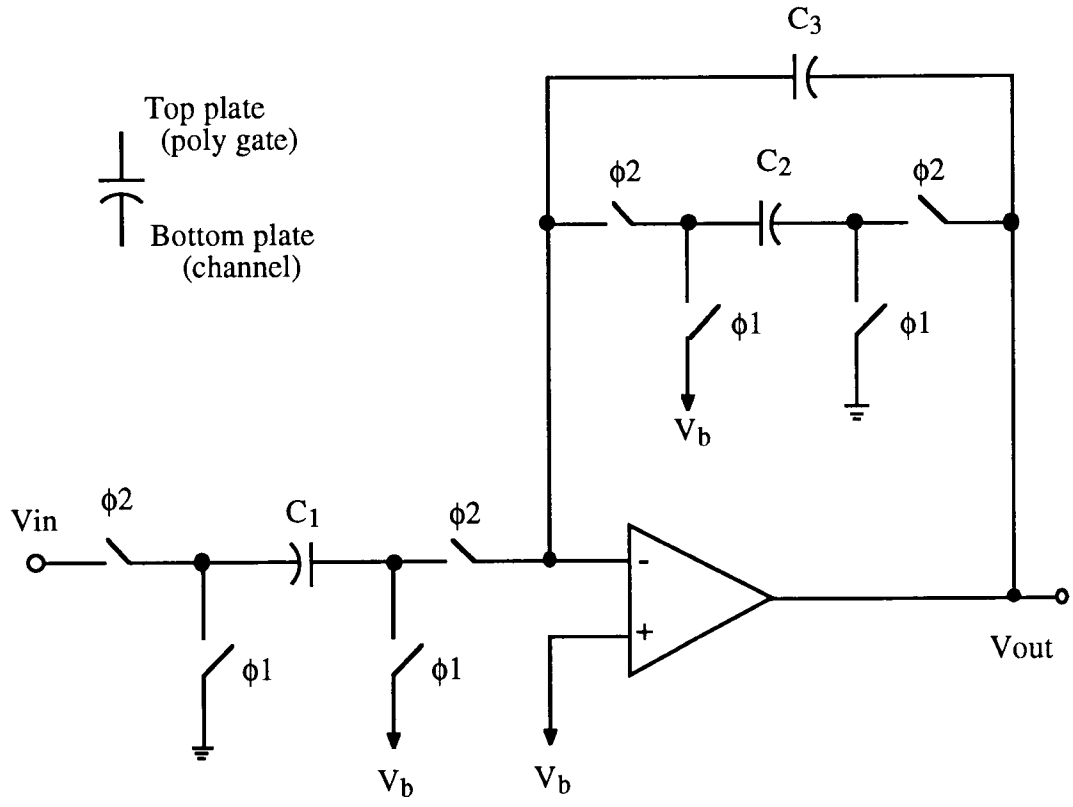


Figure 3.1 Lossy integrator using simple biasing technique [4].

3.2 Charge Processing

Bermudez et al. proposed a concept of charge processing [11], which is similar to current processing in switched-current techniques [12]. In Figure 3.2, suppose that a charge Δq_1 is transferred to capacitor C_1 from an input branch. Then the increment of output ΔV_o is given by

$$\Delta V_o = \Delta q_1 / C_1 \qquad (3\text{-}1)$$

assuming the op-amp is ideal. The charge across the load capacitor C_2 is given by

$$\Delta q_2 = C_2 \Delta V_o \qquad (3\text{-}2)$$

Notice that the ratio of charges is given by

$$\frac{\Delta q_1}{\Delta q_2} = \frac{C_1 \cdot \Delta V_o}{C_2 \cdot \Delta V_o} = \frac{C_{10}\, f_1[V_o] \cdot \Delta V_o}{C_{20}\, f_2[V_o] \cdot \Delta V_o} = \frac{C_{10}}{C_{20}} \quad \text{if } f_1[\cdot] \cong f_2[\cdot] \tag{3-3}$$

where the C_{io} are constant scale factors determined by capacitor geometries, and the $f_i[\cdot]$ are nonlinear functions of the voltages across the capacitors. Thus, even if these capacitors are voltage-dependent, this circuit provides a linear charge mirror with a gain defined by capacitor geometries if C_1 and C_2 have matched nonlinearities.

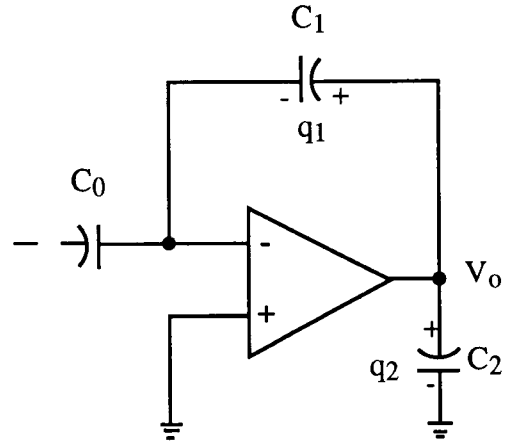


Figure 3.2 Charge processing.

To achieve this, two conditions have to be satisfied [11]: (a) after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage; (b) all capacitors connected to the same op-amp output must exhibit identical nonlinearities. In SC circuits, these conditions are usually satisfied, and hence charge processing can be applied to general SC circuits.

Charge processing is useful for internal charge transfers in SC circuits. However, just as a switched-current circuit requires a linear V-I transfer circuit at its input and a linear I-V transfer circuit at its output, a switched-capacitor circuit using charge processing requires a linear V-Q circuit at its input and a linear Q-V circuit at its output. Therefore, the

input and output capacitors have to be linear*, and in digital CMOS processes, the choice for such linear capacitors would be metal-metal, metal-poly, or MOSFET capacitors. It was reported that a S/THD ratio of 50 dB for an input frequency of 1 kHz was experimentally obtained at the output of a third-order lowpass SC filter with MOSFET capacitors [11].

3.3 Switched-Current Circuits

Switched-current (SI) circuits were proposed as an inexpensive alternative to SC circuits [12]. Figure 3.3 shows a simple current mirror, in which a current i_A is linearly scaled to a current i_B in spite of the nonlinear I-V device characteristics. Analog signal processing steps such as summation, integration, inversion, and scaling can be achieved in the current mode, and highly linear capacitors are not required. Hence, SI circuits are compatible with a standard digital CMOS process, and that is the main advantage of this technique.

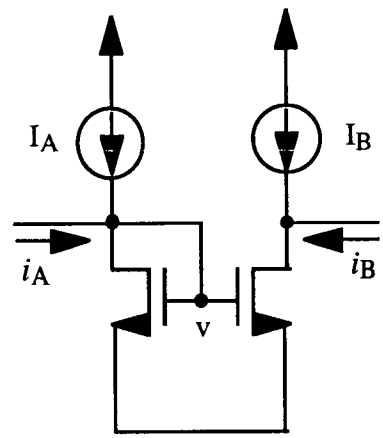


Figure 3.3 Current processing.

* Or have matched nonlinearities. In general, this is not feasible since V_{out} is not equal to V_{in}.

A comparison of SI and SC circuits can be found in reference [13]. SC circuits have advantages such as high accuracy, low power consumption, and high speed under the same power consumption. By contrast, SI circuits have higher speed (because SI circuits are not constrained by the op-amp gain-bandwidth products [14]) but at the expense of more power, and small chip area. However, SI circuits generally require V-I and I-V conversion circuits because most of the signals are available or needed as voltages. In addition, the signal-dependent charge injection caused by switches limits the accuracy of SI circuits.

3.4 Sample-and-Hold Circuits

The sample-and-hold (S/H) circuit is one of the most important analog building blocks. In this section, some S/H circuits are introduced to show the feasibility of SC circuit realization without using highly linear capacitors or special nonlinearity compensation technique.

Figure 3.4 shows a simple offset-free S/H circuit [15]. In this circuit, the same capacitor is used for sampling the input voltage and holding the stored charge for the output. Therefore, that capacitor can be realized even by a nonlinear capacitor such as a MOSFET capacitor because capacitance matching is not needed.

An improved offset-free S/H circuit for fast settling [16] is illustrated in Figure 3.5. In this circuit, capacitor C_S is used only for holding the output voltage during $\phi_1 = 1$, and the nonlinearity of C_S is also irrelevant to the output linearity. Hence, this S/H circuit can be also realized using nonlinear capacitors.

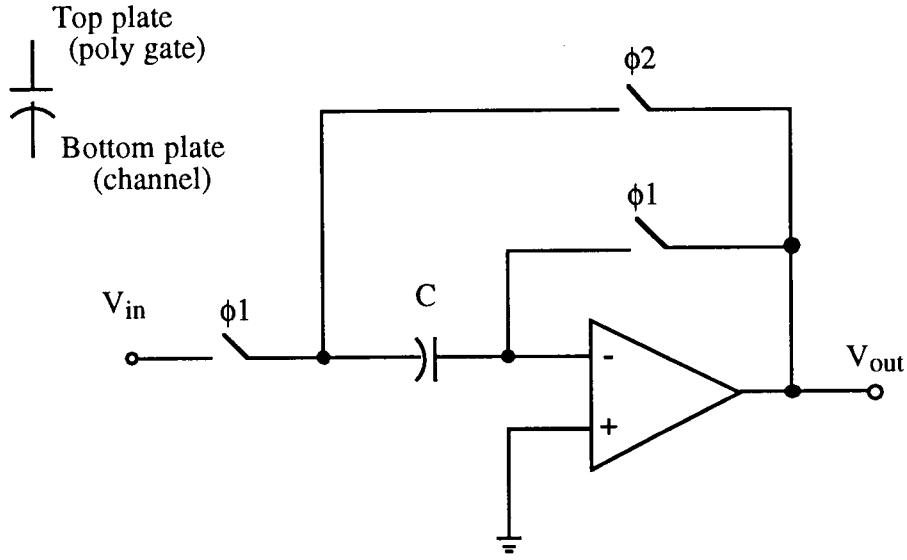


Figure 3.4 Simple S/H circuit.

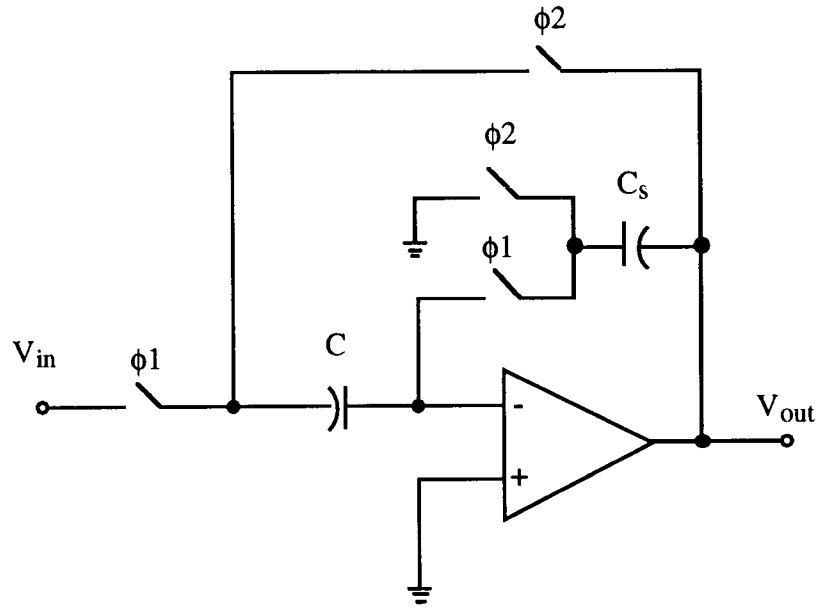


Figure 3.5 Improved S/H circuit.

Chapter 4

MOSFET-ONLY SWITCHED-CAPACITOR AMPLIFIERS USING NONLINEARITY COMPENSATION TECHNIQUES

In this chapter, novel design techniques will be presented to reduce the effects of MOSFET capacitor nonlinearity. MOSFET-only SC amplifiers will be described using these techniques. The validity of the method will be verified by HSPICE simulations.

4.1 Early Work and Applications

The SC amplifier is a fundamental analog building block, which is used not only as an amplifier, but also widely used in many applications such as digital-to-analog (D/A) converters, multiplying circuits, and programmable gain/loss circuits [17].

Various kinds of SC amplifiers were already proposed in refs.[18]-[21]. The SC amplifier shown in Figure 4.1 has several special features [21]: a) offset voltage cancellation; b) 1/f noise reduction; c) insensitivity to finite op-amp gain and slew rate.

This SC amplifier is a suitable test vehicle for estimating the capacitor nonlinearity effects because of its simplicity. Therefore, we used MOSFET capacitors in the SC amplifier of Figure 4.1 for an estimation of their nonlinearities.

4.2 Simple Biasing Technique

Figure 4.2 shows an SC amplifier using MOSFET capacitors and the simple biasing technique proposed in ref.[4]. MOSFET capacitors in the signal paths of this circuit operate in their accumulation regions by having a positive dc bias voltage at the inputs of the op-amp (virtual grounds). To establish a positive dc bias voltage at the virtual grounds, the analog ground which was connected to the virtual ground via an SC branch in Figure 4.1 was replaced by a positive dc bias voltage V_b. Fully differential configuration was used to

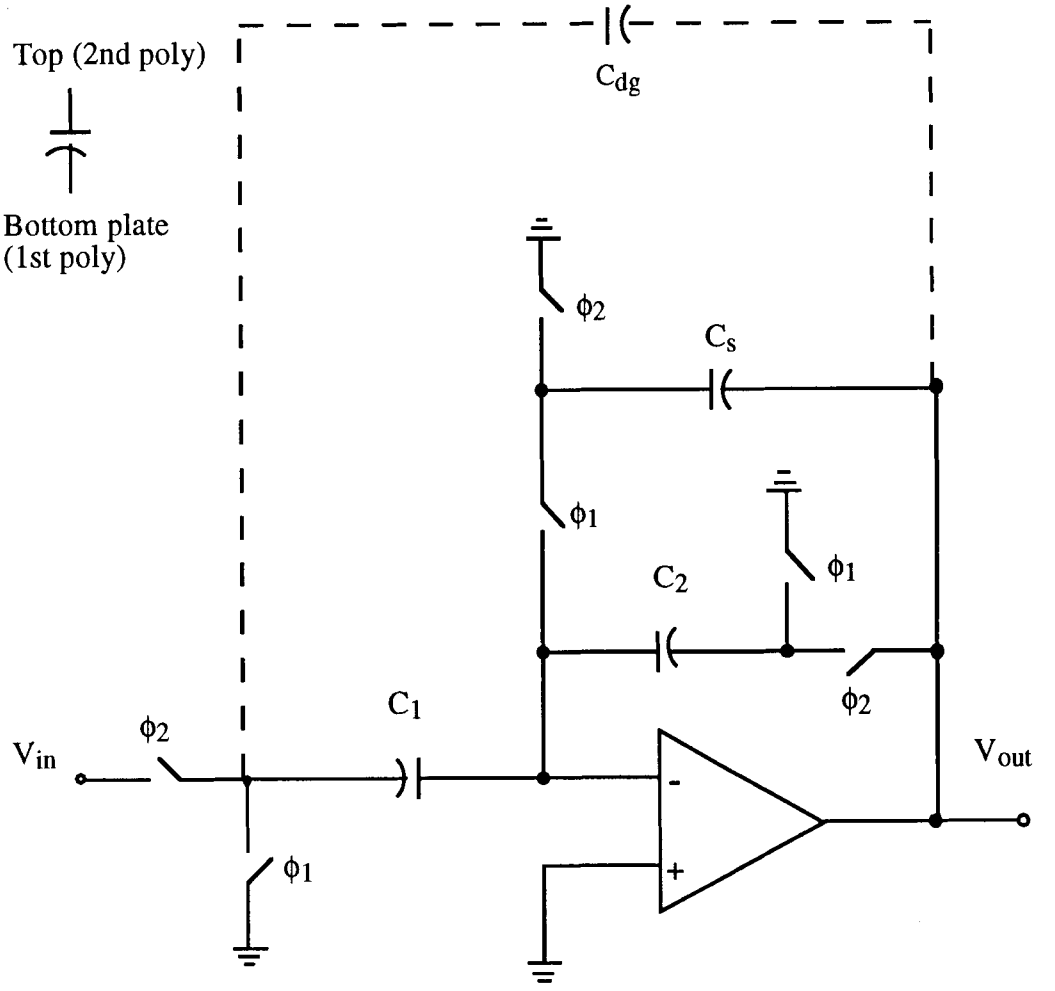


Figure 4.1 Gain- and offset-compensated SC amplifier [20]

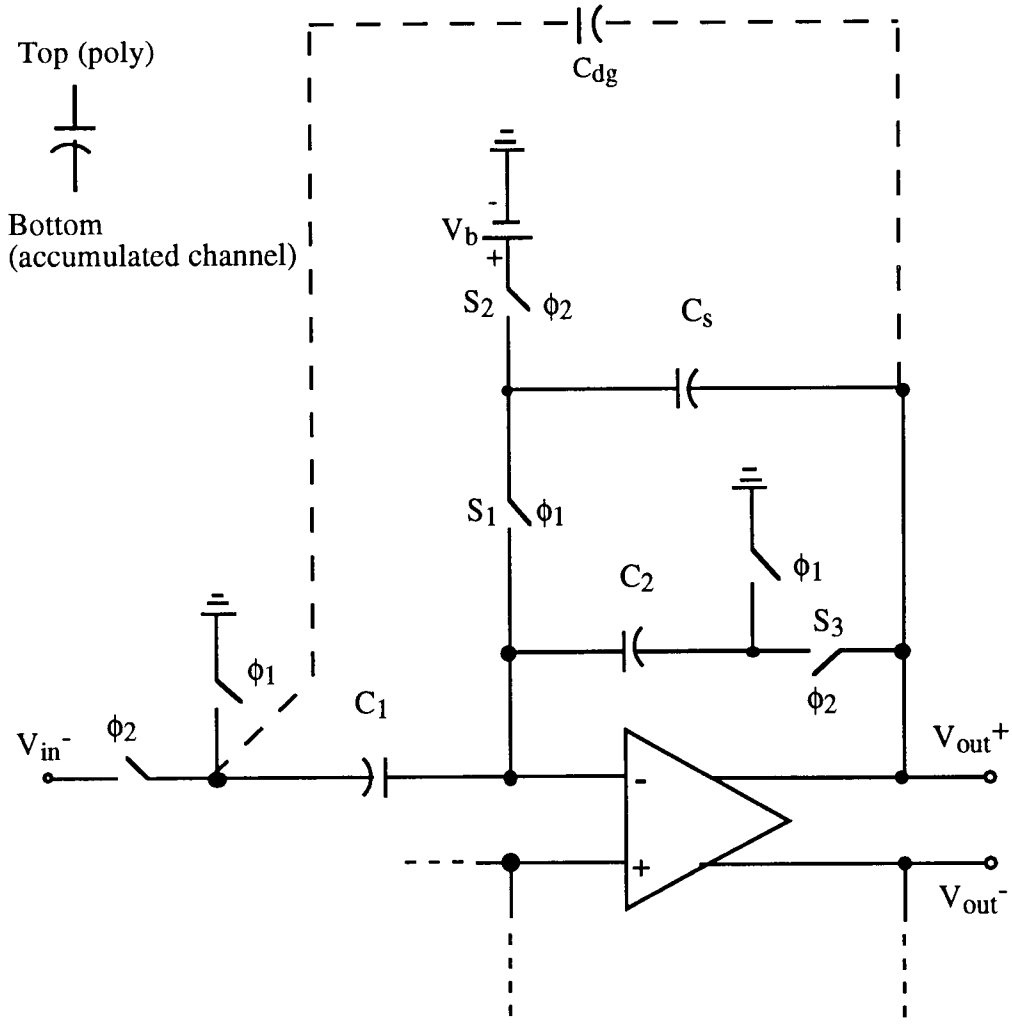


Figure 4.2 SC amplifier using simple biasing arrangement
(only half of the fully differential circuit is shown).

reduce the effect of the supply and substrate noise, as well as clock feedthrough and charge injection [22]. (In Figure 4.2 and other figures of SC amplifiers in this chapter, only half of the fully differential circuit is shown for simplicity.)

The deglitching capacitor C_{dg} was connected between the input and output terminals to reduce the generation of output spikes during the non-overlapping period of clock phases [23].

4.3 Parallel Compensation

To achieve better linearity, a novel design technique, called parallel compensation, was developed [25]. Figure 4.3 illustrates a conceptual structure of the parallel compensation. Two MOSFET capacitors C_1 are connected with floating bias voltages so that these capacitors operate in their accumulation regions. When ϕ_1 is high, the capacitors are discharged. In the next clock phase ϕ_2, these capacitors are connected to the input. Then the voltage across one of the two capacitors increases, while the voltage across the other decreases; hence one of these capacitances increases while the other decreases. When the charges are transferred to the feedback path via the virtual ground, their nonlinearities are canceled to a first-order approximation.

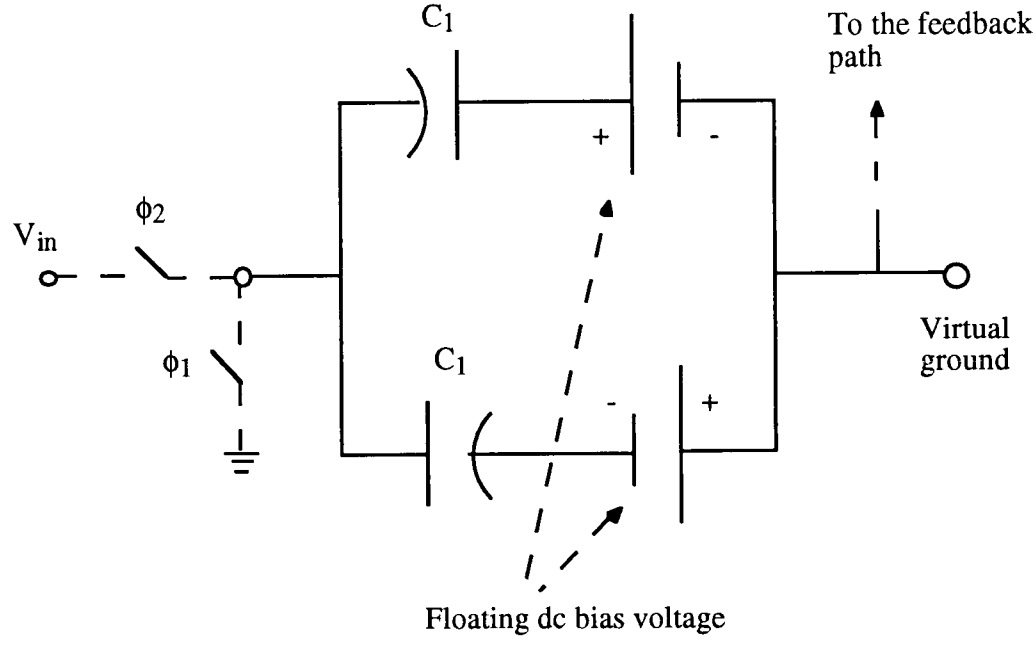


Figure 4.3 Conceptual structure of the parallel compensation.

Figure 4.4 shows a practical realization of the circuit of Figure 4.3. Two extra capacitors C_H are added to the main capacitors C_1. When ϕ_1 is high, node A is connected to

the positive bias voltage while node B is connected to the negative bias voltage so that all four capacitors operate in their accumulation regions. When ϕ_1 goes low, nodes A and B will be floating. Since the switch connected to the virtual ground is turned off, no charge flows into or out of the virtual ground node, and the charges stored on the holding capacitors C_H will be conserved. Thus, the voltages at nodes A and B will be constant and those two nodes will become ac virtual grounds. The main capacitors C_1 will be kept in their accumulation regions throughout the operation.

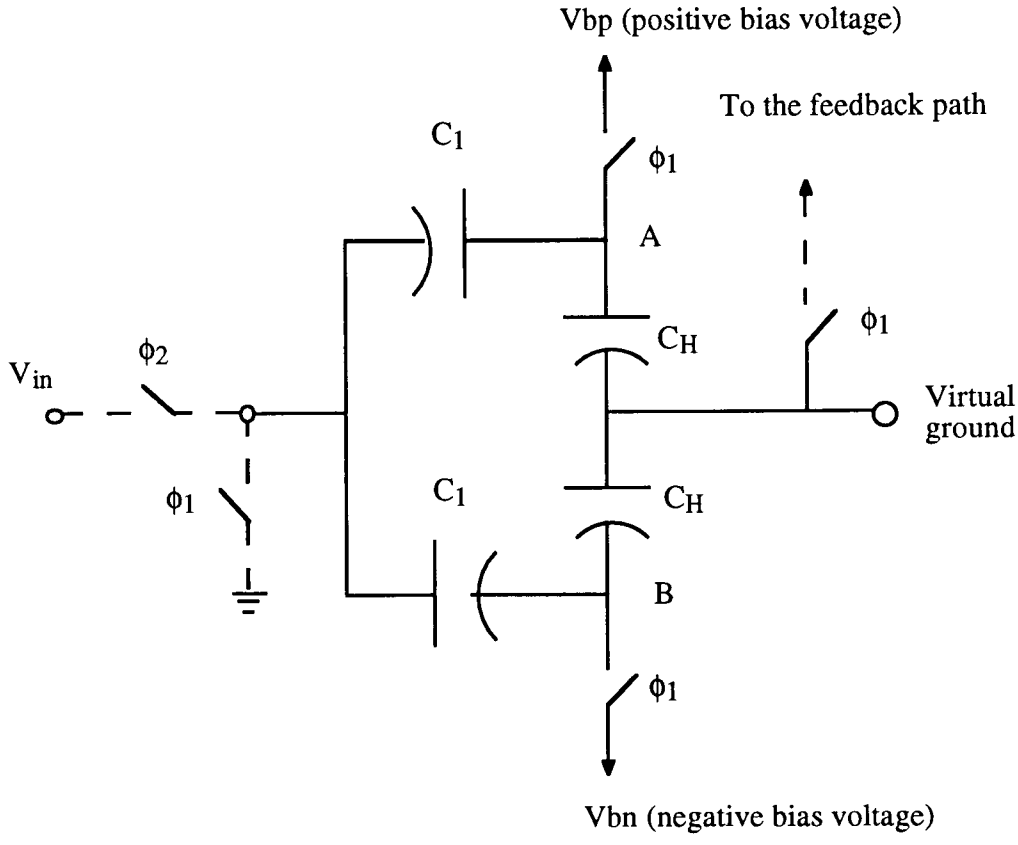


Figure 4.4 Practical realization of the parallel compensation

Figure 4.5 illustrates the resulting SC amplifier using the parallel compensation. In practical SC circuits, the input and feedback branches can share the holding capacitors C_H. The value of C_H can be much smaller than C_1, because C_H's, C_1's and C_2's are connected

in parallel, and hence the kT/C noise of the C_H branches can be neglected. Therefore, although the capacitor area increases compared to the simple biasing circuit, the increase is insignificant.

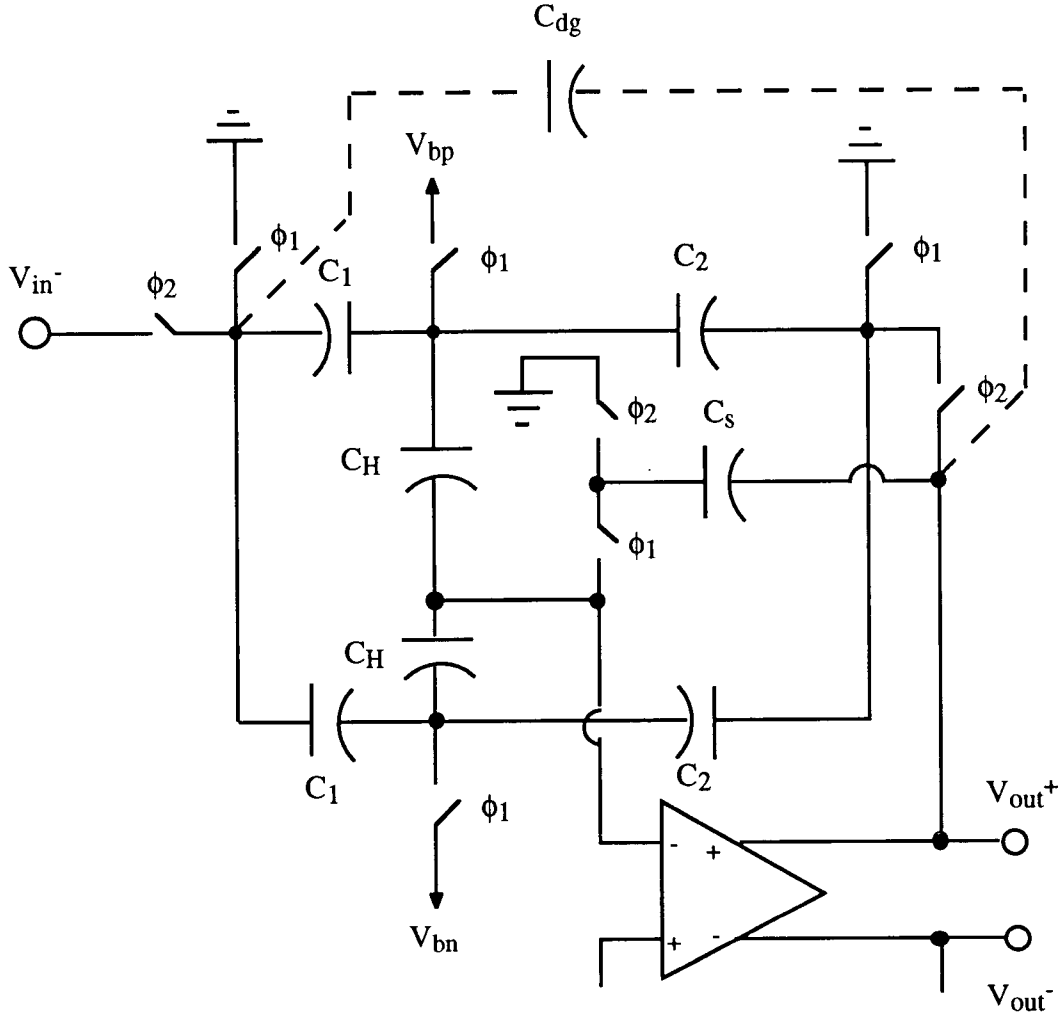


Figure 4.5 SC amplifier using parallel compensation

4.4 Series Compensation

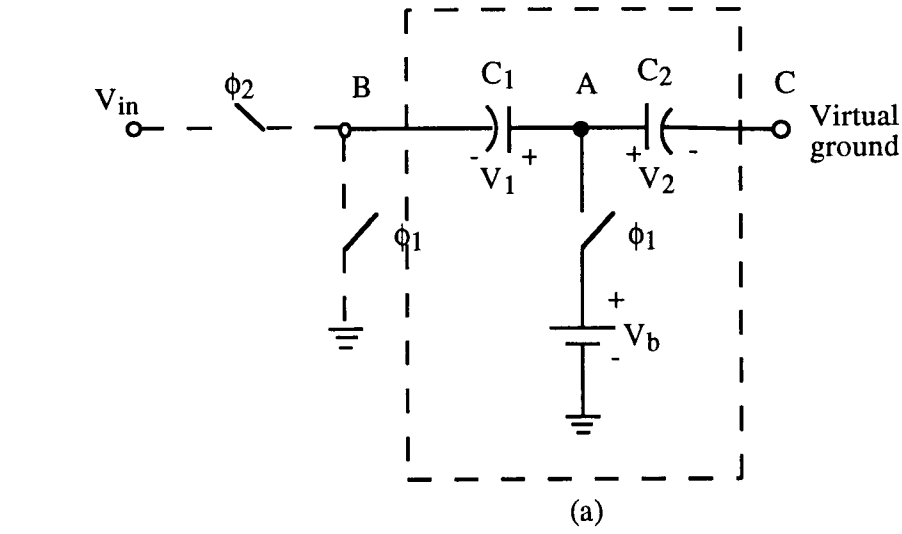
Figure 4.6a shows another novel design technique which was developed to reduce the nonlinearity of capacitors, called series compensation [26]. Two MOSFET capacitors are connected at their top plates, and when ϕ_1 goes high, the top plates are connected to the dc bias voltage V_b. The bottom plates of these capacitors are connected to the ground (one to the analog ground and the other to the virtual ground) during the phase ϕ_1, and the two capacitors are biased to operate in their accumulation region. In the next clock phase ϕ_2, the switch connected between the bias voltage V_b and the top plates is open, and node A will be floating. Since the input is connected to the bottom plate of C_1, the potential of the floating node A will be changed. Then, one of the two capacitances increases while the other decreases. Since the two capacitors are connected in series, the nonlinearity of their total capacitance will be canceled out to a first-order approximation. A possible implementation is shown in Figure 4.6b. Since the two bottom plates (n-wells) have different potentials, the n-wells have to be separated.

Let us analyze how linearly charges will be transferred to the feedback path from this series SC branch. Using the notations used in [11], the nonlinear capacitances C_1 and C_2 in Figure 4.7 can be expressed as

$$\begin{aligned} C_1 &= C_{10}\, f_1[V_1] \\ C_2 &= C_{20}\, f_2[V_2] \end{aligned} \tag{4-1}$$

where C_{i0} is a scale factor independent of the applied voltage, and $f[\cdot]$ is a nonlinear function of the voltage across the capacitor. Assuming that $C_{10} = C_{20} = C$ and that $f_1[\cdot] \equiv f_2[\cdot]$, i.e. the nonlinearity of capacitor C_1 matches that of C_2, the charge delivered by this series branch during the phase ϕ_2 is given by

$$\begin{aligned} \Delta q = C\, & \frac{f[V_A(n)]\ f[V_A(n) - V_{in}(n)]}{f[V_A(n)] + f[V_A(n) - V_{in}(n)]}\, V_{in}(n) \\ & + C\, \frac{f[V_b]\ (f[V_A(n)] - f[V_A(n) - V_{in}(n)])}{f[V_A(n)] + f[V_A(n) - V_{in}(n)]}\, Vb \end{aligned} \tag{4-2}$$



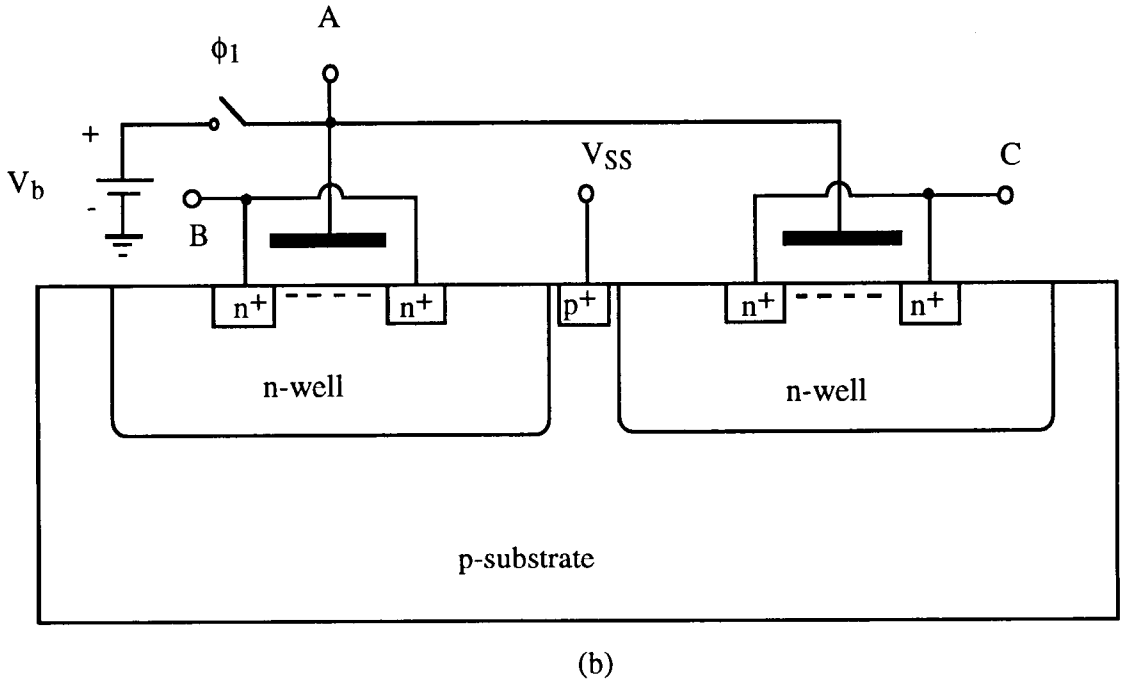
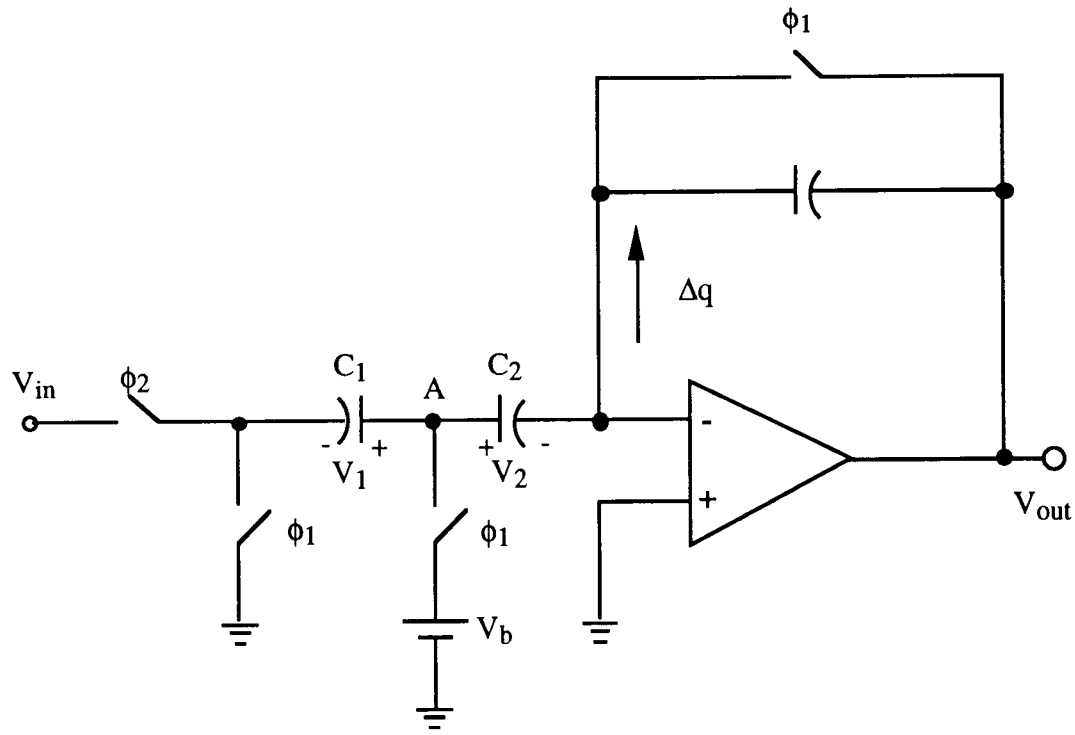
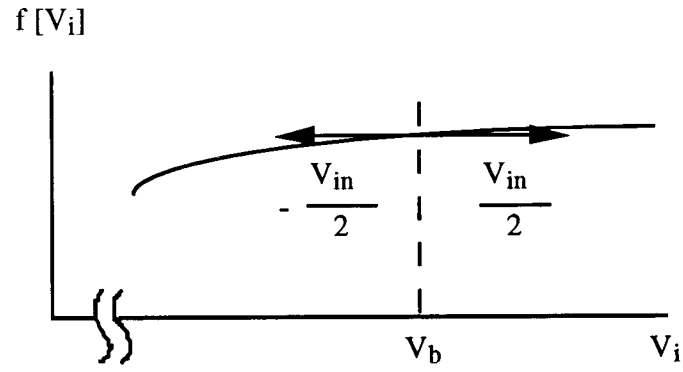


Figure 4.6 Series compensation SC branch: (a) circuit diagram; (b) practical implementation.

where V_A is the voltage at node A in Figure 4.7. If the MOSFET capacitors operate in their accumulation region during the phase $\phi 2$, V_A can be approximated as



(a)



(b)

Figure 4.7 Capacitance linearization: (a) Charge transfer from the series SC branch; (b) nonlinear function f[V]

$$V_A(n) \cong V_b + \frac{1}{2}V_{in}(n) \tag{4-3}$$

Then,

$$\begin{aligned} f[V_A(n)] &\cong f[V_b + \frac{1}{2}V_{in}(n)] \\ &\cong f[V_b] + \left.\frac{df}{dV}\right|_{V_b} \delta V(n) \end{aligned} \tag{4-4}$$

$$\begin{aligned} f[V_A(n) - V_{in}(n)] &\cong f[V_b - \frac{1}{2}V_{in}(n)] \\ &\cong f[V_b] - \left.\frac{df}{dV}\right|_{V_b} \delta V(n) \end{aligned} \tag{4-5}$$

where $\left.\frac{df}{dV}\right|_{V_b}$ is the first-order derivative of the nonlinear function $f[\cdot]$ at V_b, $\delta V(n) \cong \frac{1}{2}V_{in}(n)$ is the deviation of $V_A(n)$ from V_b, and $\delta V(n) << V_b$ is assumed. From equations (4-4) and (4-5),

$$\begin{aligned} &\frac{f[V_A(n)] \cdot f[V_A(n) - V_{in}(n)]}{f[V_A(n)] + f[V_A(n) - V_{in}(n)]} \\ &\cong \frac{(f[V_b])^2 - \left\{\left.\frac{df}{dV}\right|_{V_b} \delta V(n)\right\}^2}{2\, f[V_b]} \\ &\cong \frac{1}{2} f[V_b] \end{aligned} \tag{4-6}$$

Here the second-order small term was neglected. Also,

$$\begin{aligned} &\frac{f[V_A(n)] - f[V_A(n) - V_{in}(n)]}{f[V_A(n)] + f[V_A(n) - V_{in}(n)]} \\ &\cong \frac{\left.\frac{df}{dV}\right|_{V_b} \delta V(n)}{f[V_b]} \end{aligned} \tag{4-7}$$

By equations (4-2), (4-6) and (4-7),

$$\begin{aligned}\Delta q &\cong \frac{C}{2} V_{in}(n)\, f[V_b] + \frac{C}{2} V_b \left.\frac{df}{dV}\right|_{V_b} V_{in}(n) \\ &\cong \frac{C}{2}\left[f[V_b] + \left.\frac{df}{dV}\right|_{V_b} V_b \right] V_{in}(n)\end{aligned} \tag{4-8}$$

In equation (4-8), the expression in the square bracket is constant because V_b is a fixed potential. Therefore, to a first-order approximation, Δq is a linear function of V_{in}.

We applied the MOS SC branch of Figure 4-6 in the fully differential SC voltage amplifier. Figure 4-8 shows a circuit diagram of the SC amplifier, in which all capacitors in the signal path were replaced by the series-compensation SC branch. When $\phi 1$ is high, all capacitors are biased and kept in their accumulation region. In the subsequent phase $\phi 2=1$, the capacitors still stay in the accumulation region. Then, the output voltage of the SC amplifier can be estimated by

$$\begin{aligned}V_{out}(n) \cong & -\frac{C_1}{C_2} V_{in}(n) \\ & -\frac{2}{f[V_b]} V_b \left.\frac{df}{dV}\right|_{V_b} \left\{ \frac{C_1}{C_2} \delta V_1(n) - \delta V_2(n) \right\}\end{aligned} \tag{4-9}$$

where $\delta V_1(n) \cong \left| \frac{1}{2} V_{in}(n) \right|$ and $\delta V_2(n) \cong \left| \frac{1}{2} V_{out}(n) \right|$. Since $\delta V_2(n) \cong \frac{C_1}{C_2} \delta V_1(n)$, the nonlinearity at the output will be further reduced.

Notice that voltage at the gate node of the feedback MOS SC branch increases as the output swing increases. This node voltage should not go beyond the positive supply voltage because then the pn junction between the drain and the n-well of the PMOS switch may turn on, and that results in a leakage of charges (Figure 4.9). This limits the output swing in this configuration. (A switch configuration to overcome this constraint will be described in Chapter 10.)

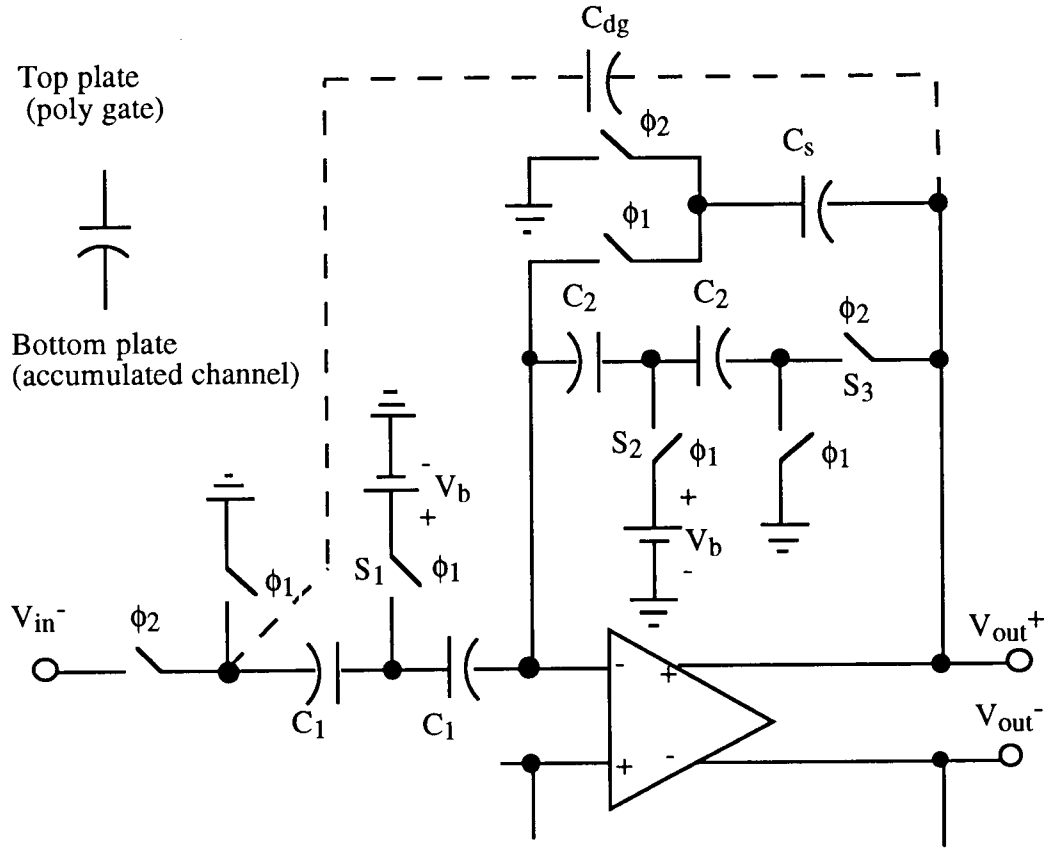


Figure 4.8 SC amplifier using series compensation.

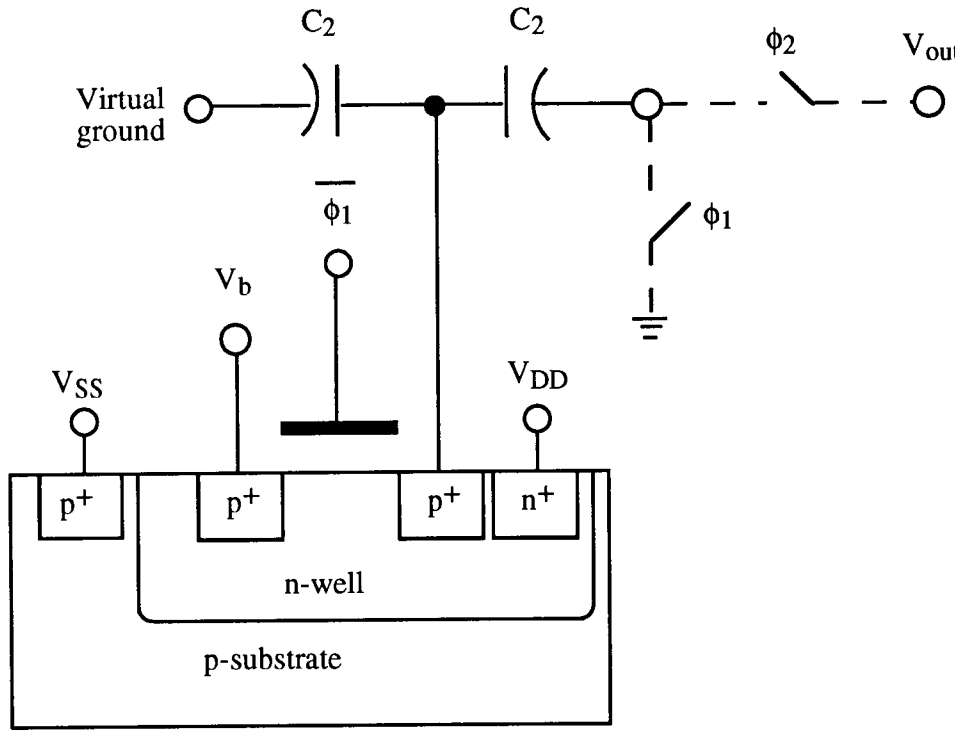


Figure 4.9 Practical realization of a PMOS switch

Since no dc bias voltage is given to the capacitor C_s in Figure 4.8, it operates in a strongly nonlinear region. However, it does not affect the linearity of the SC amplifier because its role is just to provide a feedback to the op-amp during the phase ϕ_1 to keep the op-amp from saturation. (When ϕ_1 is high, the top plate of C_s is connected to the virtual ground, and the charges from C_1 and C_2 flow into C_s. In the next clock phase ϕ_2, which is the valid phase, the top plate of C_s is switched to the ground, and C_s does not contribute to the charge redistribution with C_1 and C_2.)

Note that a nonlinear parasitic capacitance (pn junction diode) is connected to the bottom plate of each MOSFET capacitor as shown in Figure 4.10. Let us consider the effect of the parasitic capacitance. In Figure 4.10, node 1 is switched to the ground or to the input, both of which are low impedance nodes, and hence the charge on C_{d1} does not contribute to the charge redistribution of the series-compensation SC branch. Since node 3 is the virtual ground, the charge on C_{d2} is constant. Thus, these nonlinear parasitic

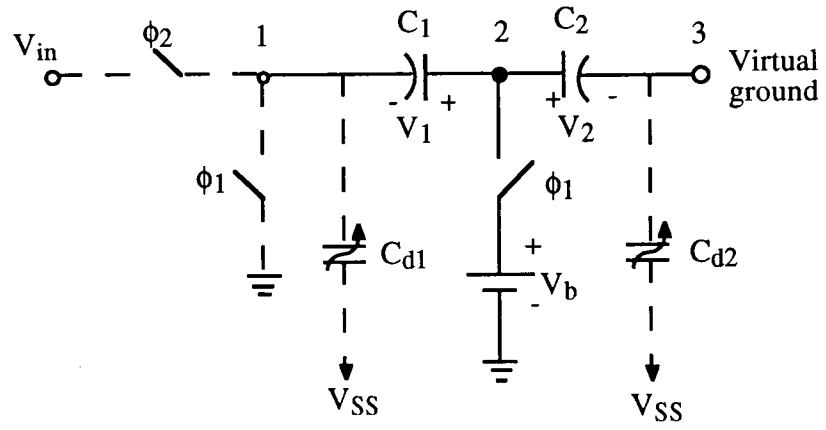


Figure 4.10 Nonlinear parasitic capacitances of the series SC branch.

capacitances will not generate distortion in the SC amplifier. The same explanation can be applied to the SC branch in the feedback path.

Another possible structure of the series-compensation SC branch is illustrated in Figure 4.11. The bottom plates of the two MOSFET capacitors are tied together and switched to a negative dc bias voltage during the phase ϕ_1 to keep these capacitors in their accumulation regions. The basic operation is the same as the other series SC branch described earlier. However in this configuration, the nonlinear parasitic capacitance of the MOSFET bottom plate will cause a serious distortion problem. When ϕ_2 is high, the input is connected to the top plate of C_1, and the potential of node 2 changes in consequence of the charge redistribution between C_1, C_2 and C_d. Since C_d is nonlinear, the resulting charge redistribution causes distortion, which is generally unacceptable.

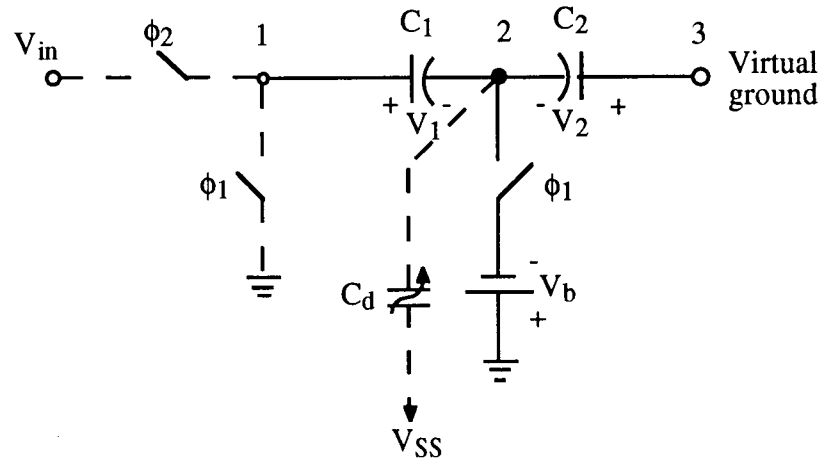


Figure 4.11 Another possible structure of the series SC branch.

4.5 Simulation Results

To verify the operation of these SC amplifiers and the effectiveness of the proposed design techniques, the SC amplifiers were simulated using HSPICE. A voltage gain of 10 was assumed.

4.5.1 Simple Biasing

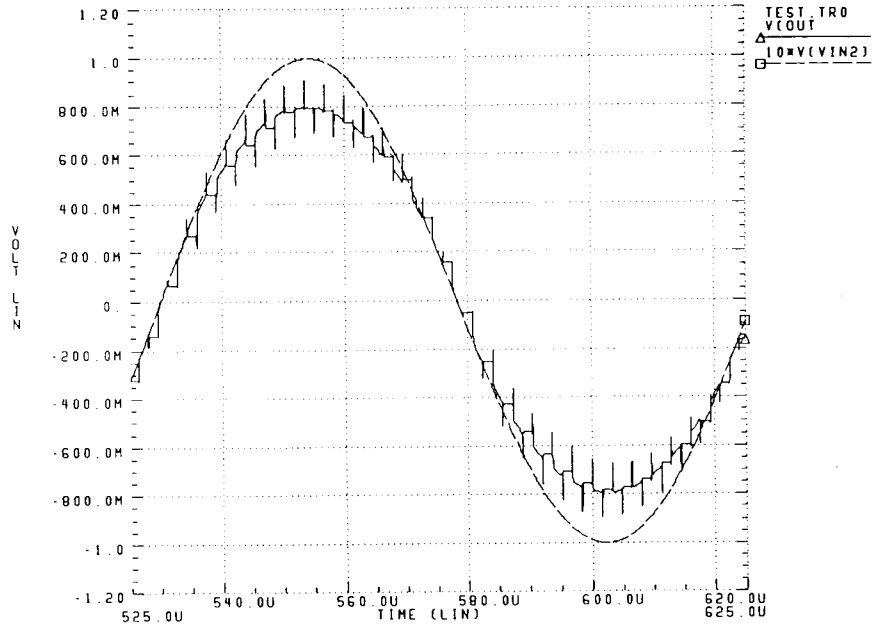
First, the parameters and conditions used in HSPICE simulations are described. They remain the same in Sections 4.5.2 and 4.5.3, unless otherwise specified. The PMOSFET model of CAPOP=2 described in Section 2.3.4 was used for all capacitors. The size of the unit capacitor was 18 μm x 18 μm, which corresponds to 0.5 pF. C_1 consisted of the parallel connection of 10 unit capacitors, while C_2 and C_s were single-unit capacitors. The deglitching capacitor C_{dg} was connected between the input and output terminals to reduce the generation of output spikes during the non-overlapping period of clock phases [23]. The MOSFET capacitor size for C_{dg} was 8.4 μm x 8.4 μm (about 0.1

pF). In each MOSFET capacitor, the well was connected to the source and the drain. A CMOS transmission gate was used for the output node, PMOS switches were used for the biased SC branches, and NMOS switches for the rest of the circuit. The switch size was 3.6 μm x 1.2 μm. We used a SPICE macro model for the op-amp with the following conditions: DC gain 70 dB; unity-gain bandwidth 30 MHz; offset voltage 5 mV. The frequencies of the input sinusoidal and clock signals were 10.4 kHz and 312.5 kHz, respectively. The bottom plate of an MOSFET capacitor has a parasitic capacitance between n-well and p-substrate. To incorporate an effect of the nonlinear capacitance into the simulation, a pn junction diode was connected to the bottom plate of each MOSFET capacitor. The power supply voltages were +/- 2.5 V. We assumed a sinusoidal signal with an amplitude 200 mVp-p for each differential input, and the resulting swing was expected to be 2 Vp-p for each output node. To investigate the nonlinear effects due to the MOSFET capacitors, an FFT analysis of the output was performed in MATLAB. For the FFT analysis, the differential outputs were sampled at the end of each clock phase ϕ_2. The amplitude in the FFT analysis was normalized in such a way that a sinusoidal waveform with an amplitude of 4 Vp-p corresponds to 0 dB.

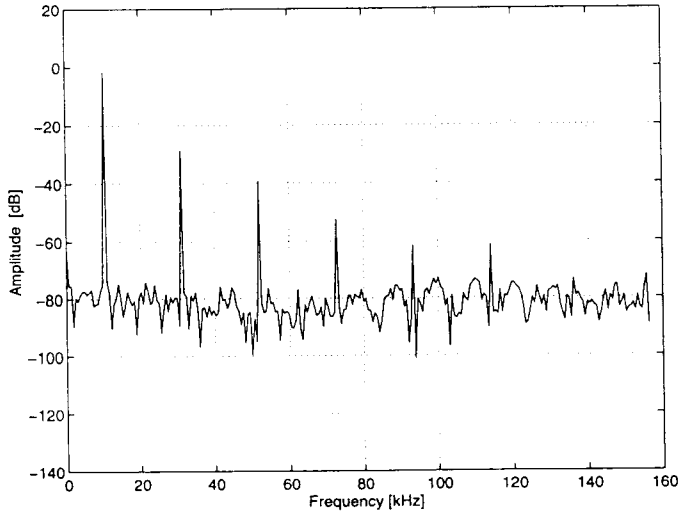
Figure 4.12 shows the time-domain and frequency-domain outputs of the SC amplifier of Figure 4.2 with Vb = 0 V. Since no dc bias voltage is provided, the MOSFET capacitors operate mostly in their depletion regions, and hence the gain was smaller than expected (Figure 4.12a) and the output was badly distorted (Figure 4.12b).

When a dc bias voltage of 1.5 V is applied in the circuit, the linearity is greatly improved as shown in Figure 4.13 because each MOSFET capacitor in the signal paths now operates in its accumulation region. In Figure 4.13b, the signal-to-total-harmonic-distortion ratio (S/THD) was 86 dB.

When the input amplitude is doubled, the harmonic distortion increases as shown in Figure 4.14. The S/THD is down to only 26 dB. This is because the output amplitude increases (now the maximum output amplitude is 2 V), while the dc bias voltage across the

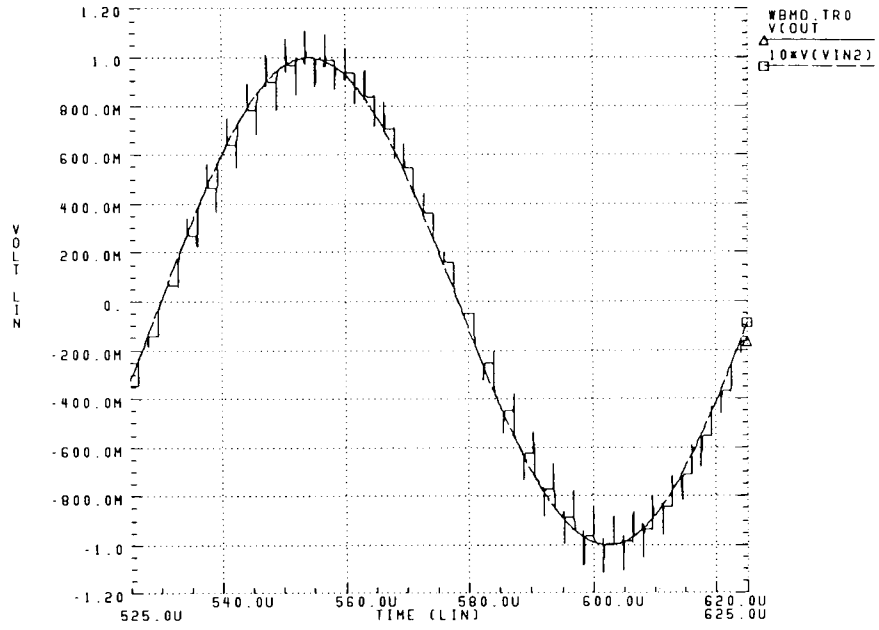


(a)

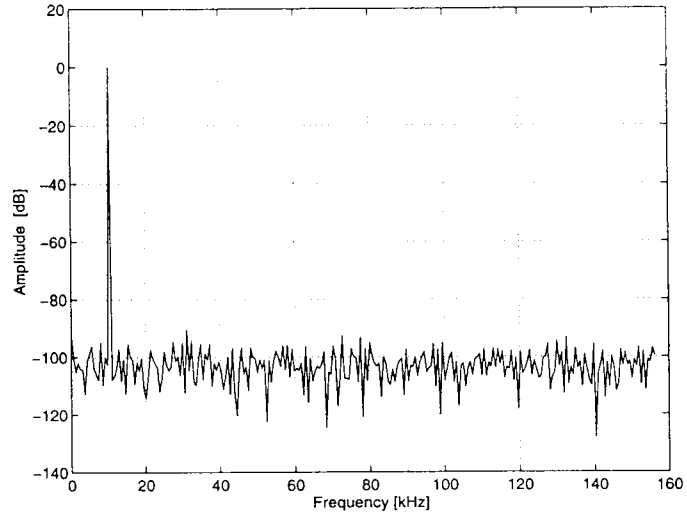


(b)

Figure 4.12 The output of the circuit of Figure 4.2 with V_{in} = 200 mV_{p-p} and V_b = 0 V: (a) time domain. The dashed line represents Vin multiplied by a gain of 10; (b) frequency domain.

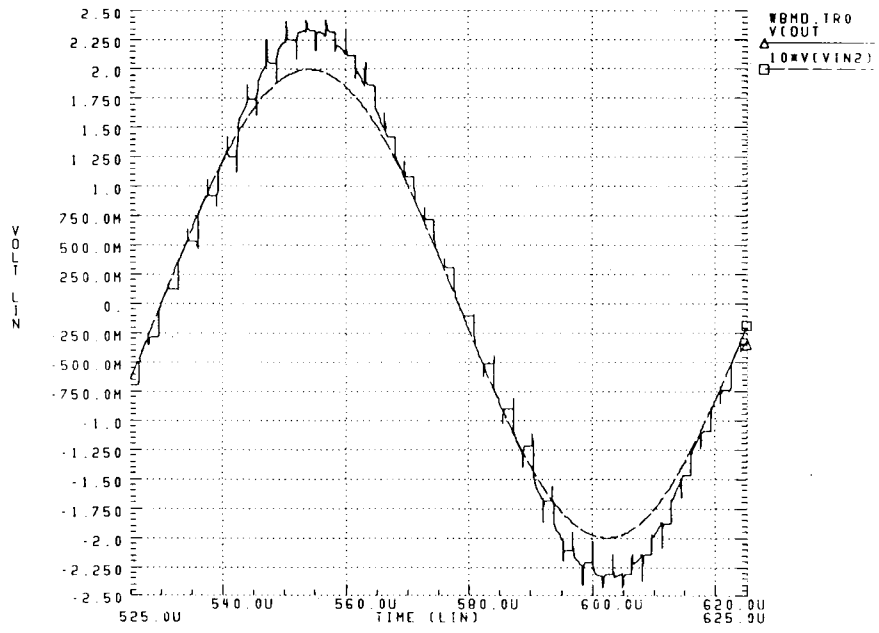


(a)

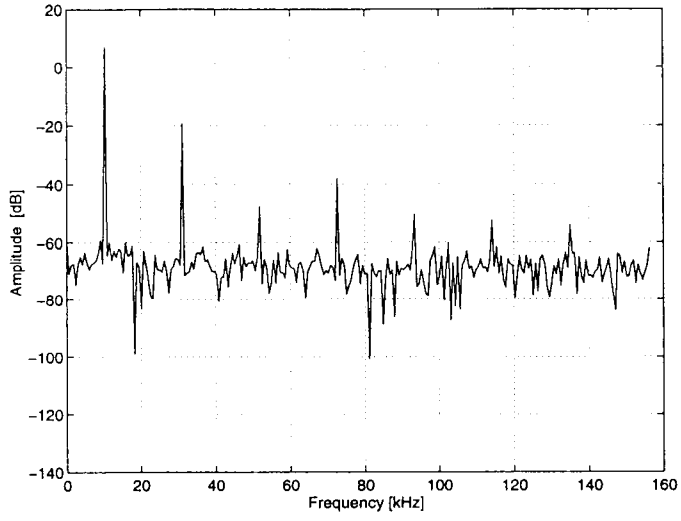


(b)

Figure 4.13 The output of the circuit of Figure 4.2 with V_{in} = 200 $mV_{p\text{-}p}$ and V_b = 1.5 V: (a) time domain. The dashed line represents Vin multiplied by a gain of 10; (b) frequency domain.



(a)



(b)

Figure 4.14 The output of the circuit of Figure 4.2 with V_{in} = 400 mV_{p-p} and V_b = 1.5 V: (a) time domain. The dashed line represents Vin multiplied by a gain of 10; (b) frequency domain.

MOSFET capacitor C_2 decreases (the minimum dc bias voltage is -0.5 V), and hence the capacitor operates in the depletion region instead of the accumulation region. Therefore, the simple biasing technique is not very effective for a large output swing*.

4.5.2 Parallel Compensation

When the SC amplifier using the parallel compensation was simulated, the capacitor size was chosen to have the same kT/C noise as in the simple biasing. (Although HSPICE does not simulate noise, the capacitor size was chosen in this way for fabrication.) The size of the unit capacitor was 13.2 μm x 13.2 μm, which corresponds to 0.25 pF. C_1 consisted of the parallel connection of 10 unit capacitors, while C_2 was a single unit capacitor. Since two C_1 capacitors are connected in parallel, the total input capacitance is 5 pF. In the same manner, the total feedback capacitance is calculated as 0.5 pF. Other capacitors were chosen as follows: C_H = 1 pF; C_S = 0.5 pF; C_{dg} = 0.1 pF. A CMOS transmission gate was used for the output node, a PMOSFET was used for any switch connected to V_{bp}, and NMOS switches for the rest of the circuit. V_{bp} and V_{bn} were +/- 2.5 V, respectively.

Figure 4.15 shows the output spectrum of the SC amplifier illustrated in Figure 4.5. For a sinusoidal signal with an amplitude 200 mVp-p, the S/THD was 86 dB (Figure 4.15a). When the input amplitude is doubled, capacitors in this circuit still operate in their accumulation regions, and the S/THD of 74 dB was obtained (Figure 4.15b). Hence, the parallel compensation is effective even for a large signal swing. A 12-dB decrease of S/THD implies that the second-order voltage coefficient of the MOSFET capacitors increased 4 times when the signal was doubled.

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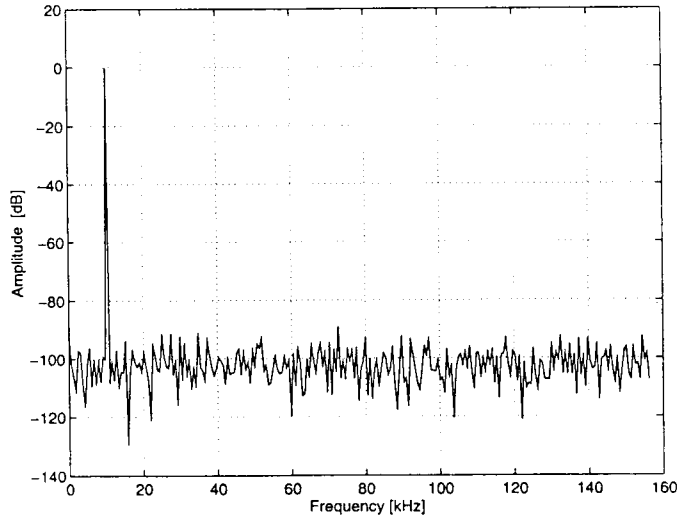
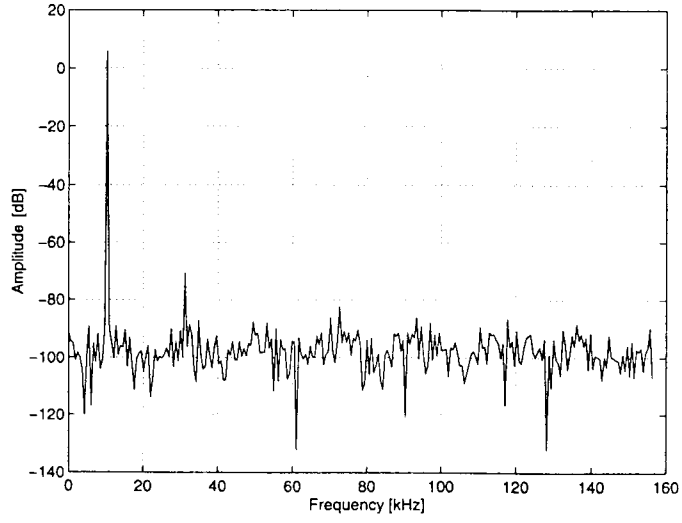
* If the input capacitance C_1 is smaller than the feedback capacitance C_2, the voltage swing across C_1 will be larger than across C_2. In such a case, the maximum input voltage swing limits the linearity of the circuit.



(a)



(b)

Figure 4.15 The output spectrum of the circuit of Figure 4.5: (a) V_{in} = 200 $mV_{p\text{-}p}$; (b) V_{in} = 400 $mV_{p\text{-}p}$.

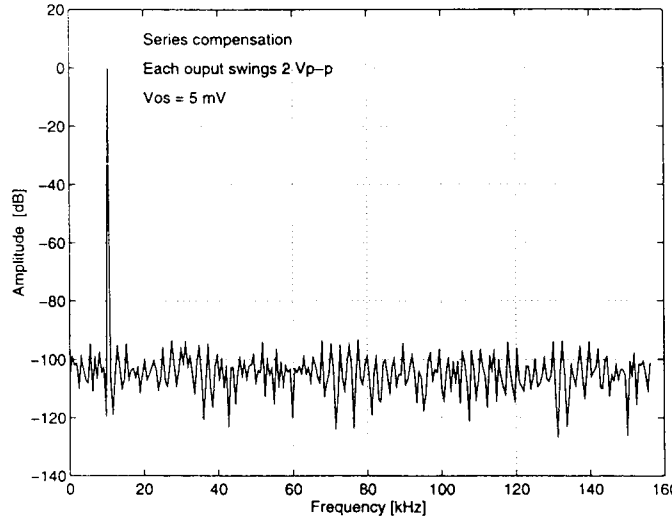
4.5.3 Series Compensation

When the SC amplifier using the series compensation shown in Figure 4.8 was simulated, the capacitor size was chosen as follows. The size of the unit capacitor was 26.4 μm x 26.4 μm, which corresponds to 1 pF. C_1 consisted of the parallel connection of 10 unit capacitors, while C_2 was a single unit capacitor. Since two C_1 capacitors are connected in series, the total input capacitance is 5 pF. In the same manner, the total feedback capacitance is estimated as 0.5 pF. Hence, the total capacitance is the same as in the SC amplifier using the simple biasing or parallel compensation. C_s was a single unit capacitor and the capacitor size for C_{dg} was 8.4 μm x 8.4 μm. A CMOS transmission gate was used for the output node, a PMOSFET was used for a switch connected to V_b, which was equal to 1.5 V, and NMOS switches for the rest of the circuit.

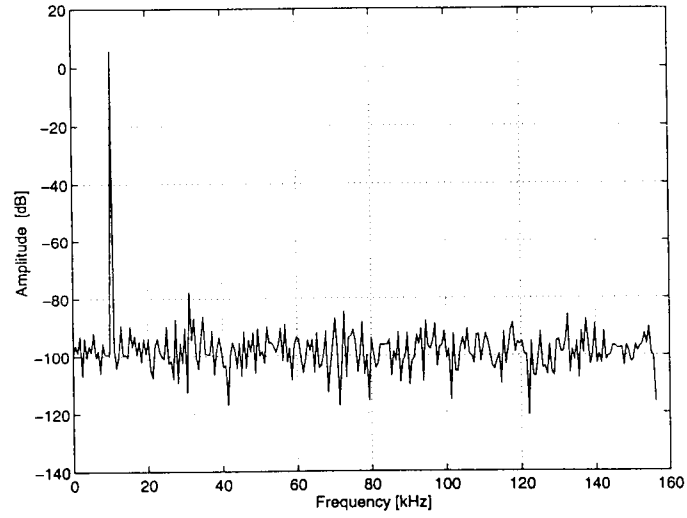
Figure 4.16 shows the output spectrum of the SC amplifier illustrated in Figure 4.8. For a sinusoidal signal with an amplitude 200 mVp-p, the S/THD was 89 dB (Figure 4.16a). When the input amplitude is doubled, capacitors in this circuit still operate in their accumulation regions, and the S/THD of 82 dB was obtained (Figure 4.16b).

To have an equivalent kT/C noise, the unit capacitance should have been four times larger here than for the simple biasing or the parallel compensation; hence the capacitor area increases considerably. However, the best linearity among these design techniques was achieved by the series compensation because the voltage swing across each capacitor is divided by half, and that results in a smaller operating region and hence less capacitor nonlinearity.

For a comparison, the SC amplifier using the bottom-to-bottom connected series SC branch, shown in Figure 4.17, was also simulated using HSPICE. Capacitor sizes were the same as for the SC amplifier of Figure 4.8. NMOSFETs were used for all switches except for the one connected to the output, which was realized by a CMOS switch.



(a)



(b)

Figure 4.16 The output spectrum of the circuit of Figure 4.8: (a) V_{in} = 200 $mV_{p\text{-}p}$; (b) V_{in} = 400 $mV_{p\text{-}p}$.

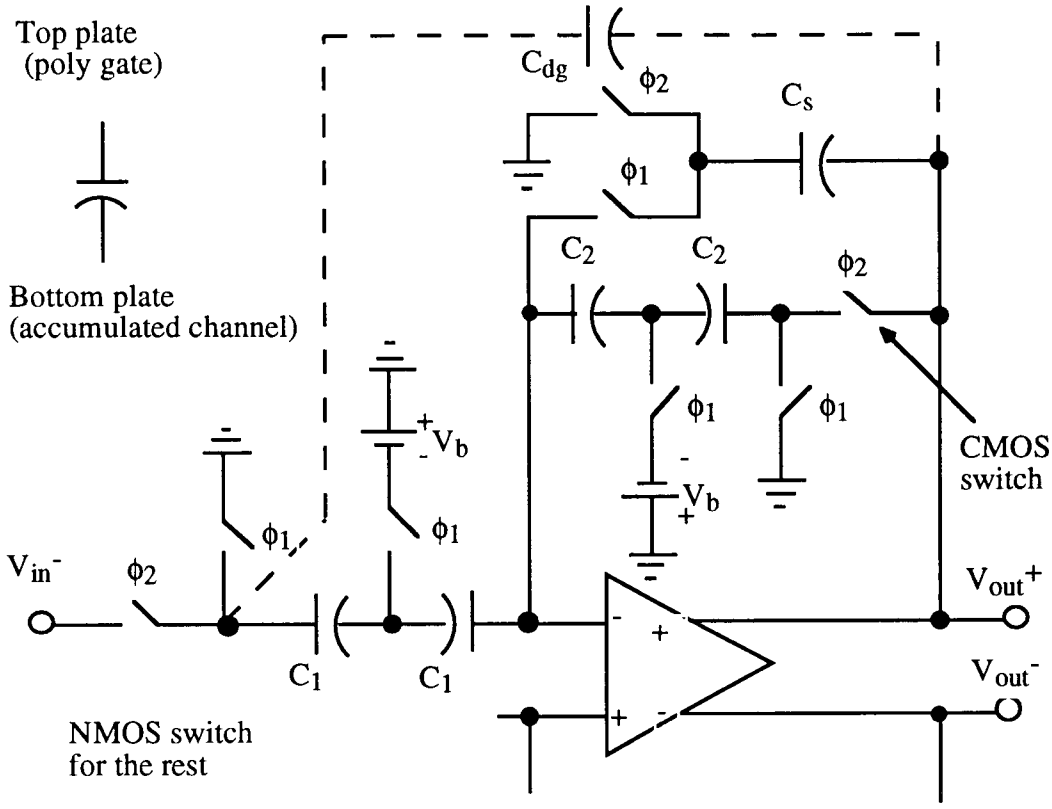


Figure 4.17 SC amplifier using the bottom-to-bottom-connected series compensation.

Figure 4.18 shows the output spectrum of the SC amplifier of Figure 4.17. For a sinusoidal signal with an amplitude 200 mVp-p, the S/THD was 72 dB and large harmonic components can be seen because the nonlinear parasitic capacitance connected to the MOSFET capacitors generated distortion as discussed in Section 4.4.

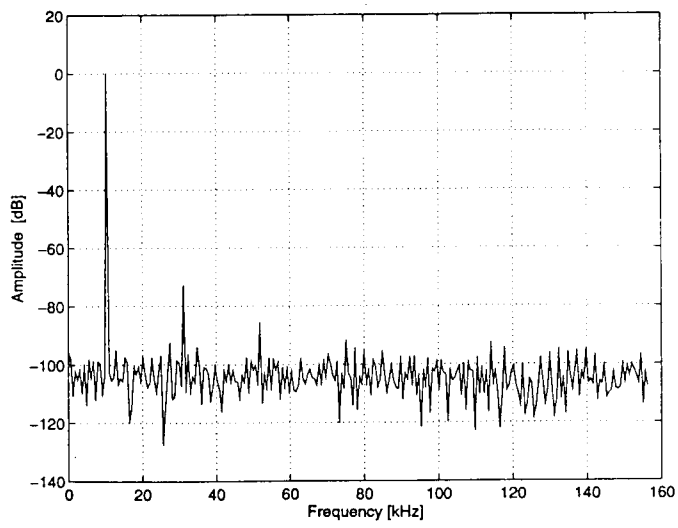


Figure 4.18 The output spectrum of the circuit of Figure 4.17 with V_{in} = 200 $mV_{p\text{-}p}$.

Chapter 5

PREDICTIVE CDS TECHNIQUE

In this chapter, predictive correlated-double-sampling (CDS) techniques will be presented. First, a background of predictive CDS will be described. Then, novel predictive SC amplifiers will be introduced. Next, MOSFET-only predictive SC amplifier stages based on the novel amplifiers will be shown. Finally, the usefulness of the predictive CDS technique will be verified by HSPICE simulations.

5.1 Background of the Predictive CDS Technique

In the SC amplifier shown in Figure 4.1, the DC gain is obtained from the formula [21]

$$|H(z)|_{z=1} = \frac{-\frac{C_1}{C_2}}{1+\left(1+\frac{C_1}{C_2}\right)\mu^2} \cong -\frac{C_1}{C_2}\left[1-\left(1+\frac{C_1}{C_2}\right)\mu^2\right] \qquad (5\text{-}1)$$

where $\mu << 1$ is the reciprocal of the DC gain of the op-amp. The second term in the bracket represents the DC gain error. Since the DC gain error is proportional to a square of the reciprocal of the op-amp DC gain, the requirement for the op-amp DC gain is greatly alleviated. This is called the gain-squaring effect [21]. The gain squaring is very effective when $V_{out}(n\text{-}1/2)$ at the phase $\phi_1=1$ and $V_{out}(n)$ at the phase $\phi_2=1$ are close to each other, or when the input frequency is much lower than the sampling frequency. The gain error increases with the input signal frequency, because the difference between $V_{out}(n\text{-}1/2)$ and $V_{out}(n)$ widens.

For wideband applications, predictive SC amplifiers, such as the one illustrated in Figure 5.1, are more suitable because they have a small gain error over a wide frequency range [27]. In Figure 5.1 we assume that $C_1/C_2=C_3/C_4$. It was also assumed that the input signal is already sampled and held, and changes only when ϕ_1 goes high as shown in Figure 5.2. During the phase ϕ_1, the predictive path containing capacitors C_3 and C_4 is active while the main path including capacitors C_1 and C_2 is open, and the SC amplifier output anticipates the output voltage of the next half clock cycle ϕ_2. When ϕ_2 goes high, the predictive path is open while the main signal path is active, and the valid output is obtained. Since the capacitors C_1 and C_2 are permanently tied to the virtual ground node, the main signal path can cancel the offset voltage and reduce the 1/f noise. Also, because the output voltage was already predicted during the previous half clock cycle ($\phi_1=1$), the output voltage varies only slightly during the transition from ϕ_1 to ϕ_2 (Figure 5.2), and the effects of finite op-amp DC gain are greatly reduced. In addition, the op-amp does not require a high slew rate during the valid ($\phi_2=1$) phase.

The DC gain error of the circuit shown in Figure 5.1 is given [27] by

$$|H(z)|_{z=1} = \frac{-\frac{C_1}{C_2}}{1+\left(1+\frac{C_1}{C_2}\right)^2 \mu^2} \cong -\frac{C_1}{C_2}\left[1-\left(1+\frac{C_1}{C_2}\right)^2 \mu^2\right] \qquad (5\text{-}2)$$

Since in the second term both μ and $(1+C_1/C_2)$ are squared, and since C_1/C_2 is larger than 1 in amplifiers, that makes the DC gain error larger than that of the non-predictive SC amplifier of Figure 4.1. However, the gain error is nearly independent of signal frequency, because the outputs at ϕ_1 and ϕ_2 are nearly equal to each other even for high signal frequency. Hence, when the input frequency becomes higher, the predictive SC amplifier can achieve a better gain accuracy than the non-predictive one.

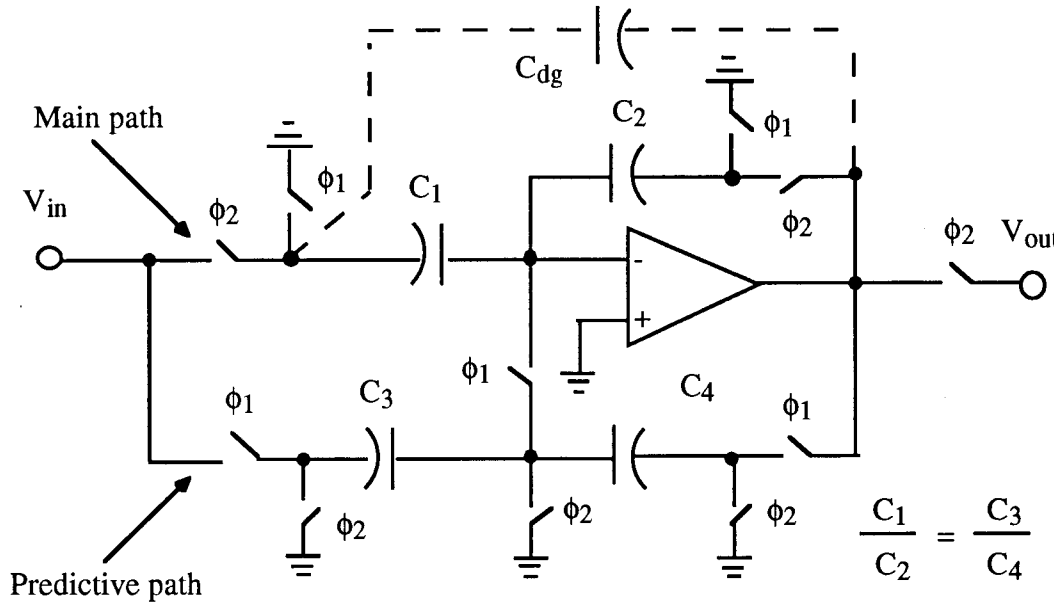


Figure 5.1 Predictive SC amplifier [27]

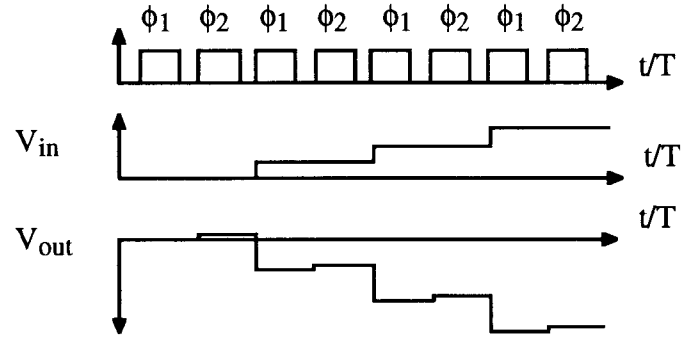


Figure 5.2 Signal waveform of the predictive SC amplifier

In ref.[28], it was shown that predictive SC amplifiers are also effective for reducing the nonlinear distortion caused by the op-amp. The output voltage of the predictive SC amplifier in Figure 5.1 can be expressed as

$$v_{out}(n) = -\frac{C_1}{C_2} v_{in}(n) + v_e(n) \qquad (5\text{-}3)$$

where $v_e(n)$ is the output error voltage, given by

$$v_e(n) = \left(1 + \frac{C_1}{C_2}\right)\left[v(n) - v\left(n - \frac{1}{2}\right)\right] \qquad (5\text{-}4)$$

In equation (5-4), v(n) and v(n-1/2) are the voltages at the virtual ground node during ϕ_2=1 and ϕ_1=1, respectively. In the predictive CDS circuit, v(n)≅v(n-1/2) because v_{out}(n-1/2) is nearly equal to v_{out}(n) and v(n)=-μv_{out}(n). Hence, the error voltage v_e(n) in equation (5-3) can be neglected in the predictive circuit.

In a predictive circuit using nonlinear capacitors, the linearity of the circuit is determined by the coefficient of the first term of the RHS in equation (5-3), C_1/C_2. By applying an appropriate compensation for these capacitors, the nonlinearity of C_1/C_2 will be also suppressed, and consequently an output with low distortion can be obtained.

5.2 Novel Predictive SC Amplifier

Figure 5.3a shows a novel predictive SC amplifier [29] which has a simpler configuration than other predictive SC amplifiers in refs.[27] and [30]. This circuit is obtained simply by adding capacitor C_3 between the input node and the node at the top plate of capacitor C_s in the non-predictive SC amplifier of Figure 4.1. Hence, it uses fewer switches than the circuit in Figure 5.1 and has a simpler configuration. Assuming that the input signal is sampled and held as shown in Figure 5.2, the DC gain error of this circuit is also given by the equation (5-2).

Figure 5.3b shows another possible structure [29]. A switch is inserted between the input and the capacitor C_3 in the circuit of Figure 5.3a. If capacitor sizes are chosen as C_1=C_3 (and C_2=C_4), the capacitance seen from the input node is constant during ϕ_1 and ϕ_2. That is, the load capacitance seen by the previous stage is constant. That makes it easier to

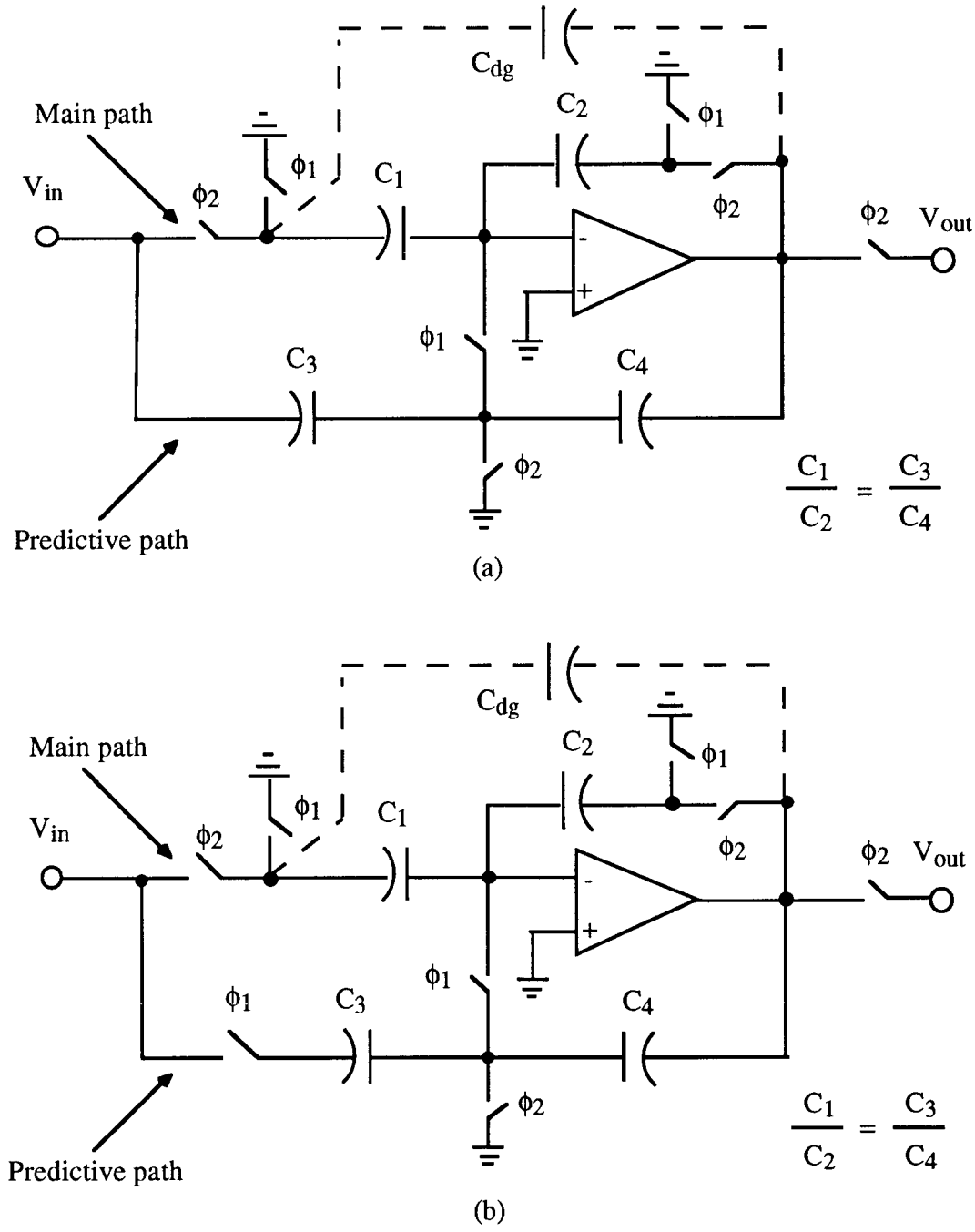


Figure 5.3 Novel predictive SC amplifiers: (a) simplified predictive SC amplifier; (b) improved predictive SC amplifier.

design the op-amp of the previous stage. By contrast, the load capacitance of the op-amp in this circuit (and of the circuit of Figure 5.3a) is not constant: C_4 at ϕ_1; C_2+C_4 at ϕ_2.

However, C_2 and C_4 are smaller than C_1 and C_3 in amplifiers, and the variation of the load capacitance is usually not a major problem for op-amp design. A very important feature of this circuit is that the DC gain error is given by equation (5-1), hence it is the same as that of Figure 4.1 and smaller than those of Figures 5.1 and 5.3a. In addition, it also has a small gain error over a wide frequency range due to the predictive property.

The reason why the circuit of Figure 5.3b works better than that of Figure 5.1 or Figure 5.3a is explained as follows. Assuming that the input signal is constant (DC), the output of the predictive amplifiers is shown in Figure 5.4. For the circuit of Figure 5.1, $V_{out}(\phi 1)$ is determined by the charge Δq coming from C1, C2 and C3 to C4 during $\phi 1=1$, and by the voltage of the virtual ground node, i.e.,

$$V_{out}(\phi_1) = -\frac{\Delta q}{C_4} + V_x(\phi_1)$$

where V_X is the voltage of the virtual ground node. Since the charges coming from C1 and C2 cancel each other, Δq is equal to the charge coming from C3. Then Δq is given by

$$\Delta q = -C_3(V_x(\phi_1) - V_{in})$$

$$\therefore V_{out}(\phi_1) = \frac{C_3}{C_4}(V_x(\phi_1) - V_{in}) + V_x(\phi_1)$$

$$= -\frac{C_3}{C_4}V_{in} + \left(1 + \frac{C_3}{C_4}\right)V_x(\phi_1)$$

Assuming that $V_{out}(\phi_2) \cong -\frac{C_3}{C_4}$,

$$\Delta V_{out} = V_{out}(\phi_1) - V_{out}(\phi_2)$$

$$\cong \left(1 + \frac{C_3}{C_4}\right)V_x(\phi_1) \qquad (5\text{-}5)$$

For the circuit of Figure 5.3a, ΔV_{out} is also given by equation (5-5). By contrast, for the circuit of Figure 5.3b, ΔV_{out} is given by

$$\Delta V_{out} \cong V_x(\phi_1) \qquad (5\text{-}6)$$

because the charges coming from C1 and C2 cancel each other, and no charge is coming from C3 to C4. (Note that the input signal and Vx(ϕ1) are constant.) Hence, ΔV_{out} is smaller in Figure 5.3b than in Figure 5.1 or Figure 5.3a. Since the voltage at the virtual ground node is less affected by the smaller ΔV_{out} and it is stored on the capacitors C1 and C2, the DC gain error becomes smaller in Figure 5.3b. Hence, the circuit of Figure 5.3b gives a better performance than that of Figure 5.1 or 5.3a for the DC input signal. And the predictive CDS helps all these predictive SC amplifiers to keep their gain errors small in the wide range of the input frequency.

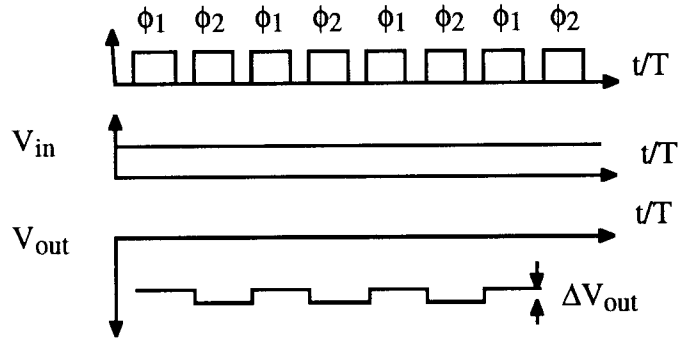


Figure 5.4 Signal waveform of the predictive SC amplifiers for a DC input

To verify the behavior of the gain error of these novel predictive circuits, they were simulated using SWITCAP. For comparison, the non-predictive and no-gain-compensated SC amplifier of Figure 5.5 and the non-predictive gain-compensated SC amplifier of Figure 4.1 were also simulated. The conditions used in the simulations were as follows: DC gain of the op-amp = 40 dB; offset voltage = 5 mV; gain of the SC amp = 10; clock frequency = 312.5 kHz. To the three predictive SC amplifiers, the sampled-and-held input illustrated in Figure 5.2 was applied. The gain errors of these SC amplifiers are shown in Table 5-1 and Figure 5.6.

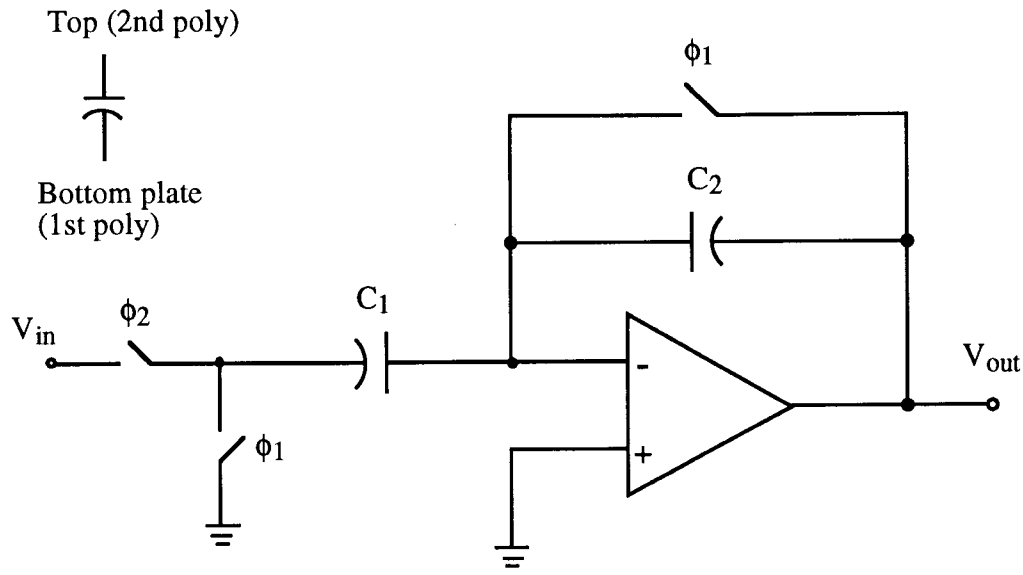


Figure 5.5 Gain-uncompensated non-predictive SC amplifier

Table 5-1 Gain errors of SC amplifiers

SC amplifier	Input frequency 10.4 kHz	Input frequency 61.6 kHz
Gain-uncompensated non-predictive amplifier (Figure 5.5)	0.91 dB	0.91 dB
Gain-compensated non-predictive amplifier (Figure 4.1)	0.04 dB	0.76 dB
Gain-compensated predictive amplifier (Figure 5.1)	0.09 dB	0.14 dB
Gain-compensated predictive amplifier (Figure 5.3a)	0.10 dB	0.15 dB
Gain-compensated predictive amplifier (Figure 5.3b)	0.02 dB	0.15 dB

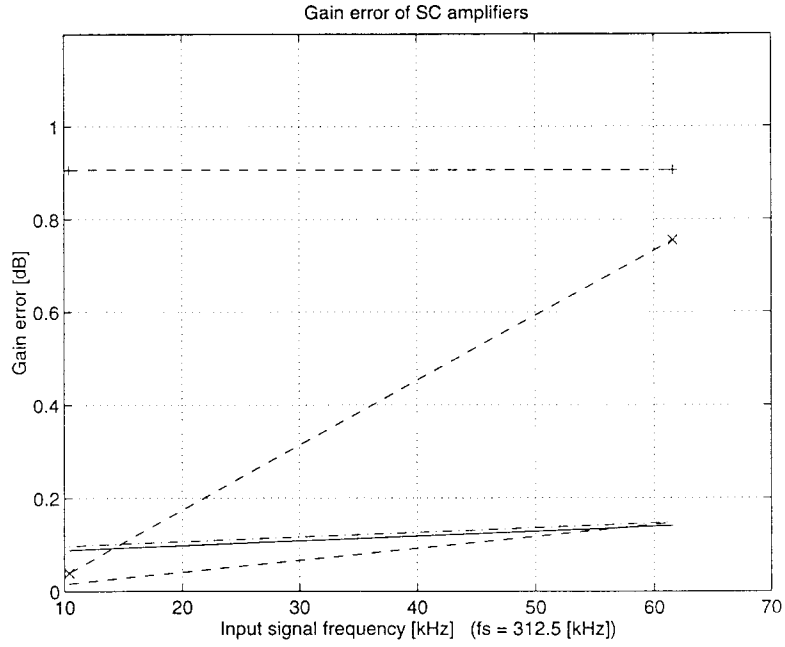


Figure 5.6 Gain error of SC amplifiers: solid line for Figure 5.1; dashdot line for Figure 5.3a; dashed line for Figure 5.3b; +------+ Figure 5.5; x------x Figure 4.1.

As can be seen from Figure 5.6 and Table 5-1, the gain-uncompensated non-predictive amplifier of Figure 5.5 has a constant but large gain error over the operating frequency range. The gain-compensated non-predictive amplifier of Figure 4.1 has a very small gain error at low frequency, however the error increases rapidly with the signal frequency. The gain errors of the gain-compensated predictive amplifiers of Figures 5.1 and 5.3a are nearly identical: the error is slightly larger than that of the non-predictive amplifier of Figure 4.1 at low frequency, and it remains small even for a high-frequency input signal. The circuit of Figure 5.3b has a very small error over a wide range, because of the gain squaring given by equation (5-1) and the predictive feature.

The key features of the three predictive amplifiers are summarized in Table 5-2.

Table 5-2 Summary of the key features of the three predictive amplifiers

SC amplifier	DC gain error	Number of switches	$C_{in}(\phi_1)=C_{in}(\phi_2)$	$C_{out}(\phi_1)=C_{out}(\phi_2)$
Figure 5.1	$-\mu^2(1+C_1/C_2)^2$	10	possible	possible
Figure 5.3a	$-\mu^2(1+C_1/C_2)^2$	6	not possible	not possible
Figure 5.3b	$-\mu^2(1+C_1/C_2)$	7	possible	not possible

5.3 MOSFET-Only Predictive SC amplifier

To realize the novel predictive SC amplifiers in a digital CMOS process, MOSFET capacitors using the parallel and series compensations may be used, as discussed next.

5.3.1 Parallel Compensation

Figure 5.7 shows a predictive SC amplifier based on the circuit of Figure 5.3b using the parallel compensation technique. In this circuit, the main path uses parallel compensation while the predictive path is realized by only half of the parallel compensation circuit (Figure 5.7b), because the predicted output (during $\phi_1=1$) does not have to be so accurate as the valid output during $\phi_2=1$. The other predictive circuits (Figures 5.1 and 5.3a) can be also implemented using MOSFET capacitors, as shown in Figure 5.8 and 5.9, respectively. For comparison, they will be simulated as well.

5.3.2 Series Compensation

Figure 5.10 illustrates predictive SC amplifiers using the series compensation technique. In both circuits shown in Figure 5.10, the predictive path is realized by simple

biasing, because high accuracy is not required for the output in the predictive phase and also because the simple biasing requires less capacitor area.

5.4 Simulation Results

To verify the operation of the predictive SC amplifiers using MOSFET capacitors, the SC amplifiers were simulated using HSPICE. The parameters and conditions used in the HSPICE simulations are the same as in Section 4.5, unless otherwise specified.

Figure 5.11a shows the output spectrum of the SC amplifier with the parallel compensation of Figure 5.7. A S/THD ratio of 101 dB was obtained for a 4 Vp-p differential output swing. The linearity is further improved compared to that of the non-predictive SC amplifier of Figure 4.5 (the S/THD ratio is 86 dB).

Figures 5.11b and c show the output spectra of the circuits of Figures 5.8 and 5.9. The S/THD ratios were 96 dB and 98 dB, respectively. Among the three circuits, the circuit of Figure 5.7 had the best S/THD ratio. However, it is fair to say that these results are nearly equivalent because the few dB differences at this high linearity level, obtained in HSPICE, are not significant.

Figure 5.12 shows the simulation results for the predictive amplifiers with series compensation shown in Figure 5.10. The S/THD ratios in Figure 5.12a and b were 97 dB and 99 dB, respectively. Again, these results are nearly the same.

In all of these predictive circuits, a very high linearity was obtained in spite of using nonlinear MOSFET capacitors.

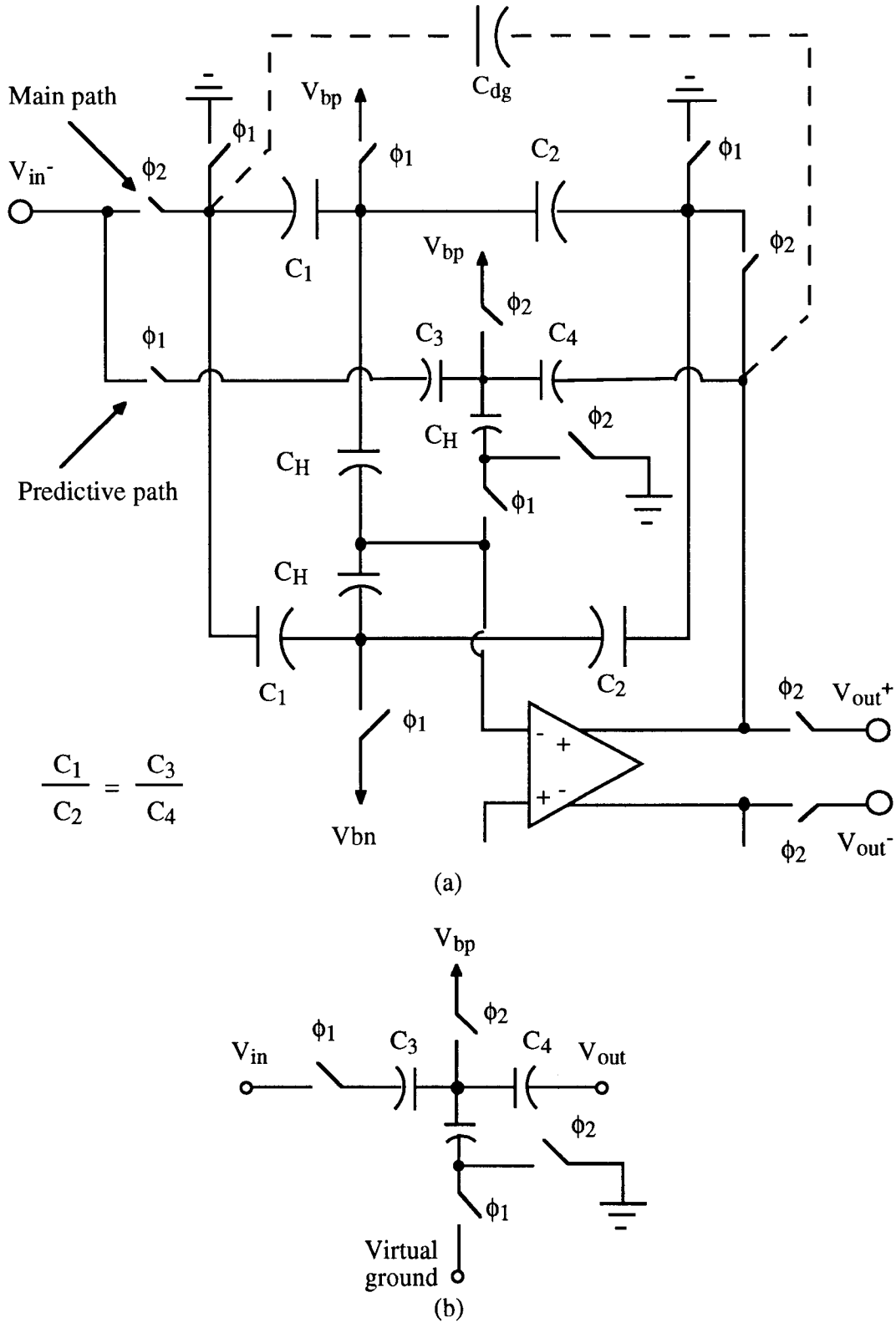


Figure 5.7 Predictive SC amplifier using parallel compensation: (a) half of the whole circuit; (b) predictive path

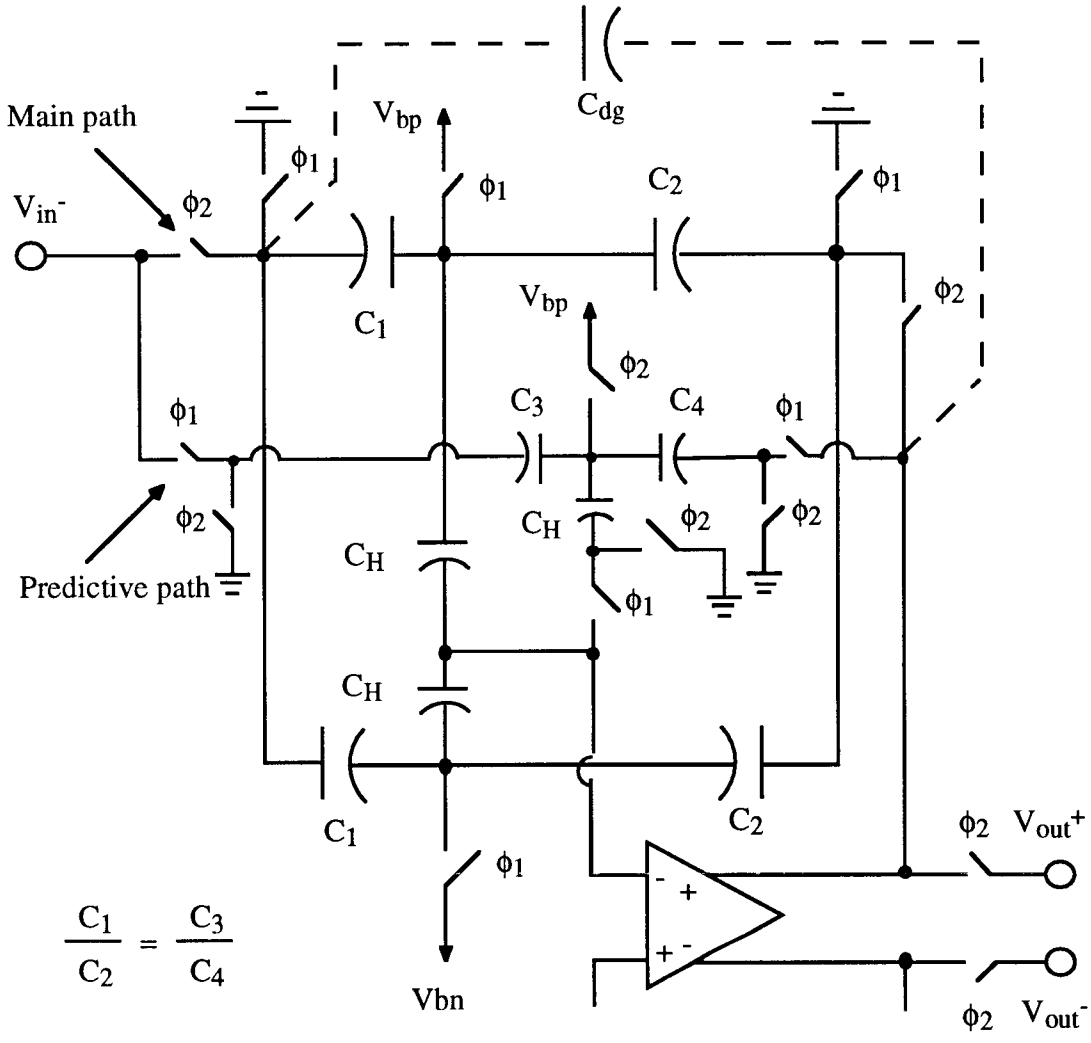


Figure 5.8 Predictive SC amplifier using parallel compensation based on the circuit of Figure 5.1

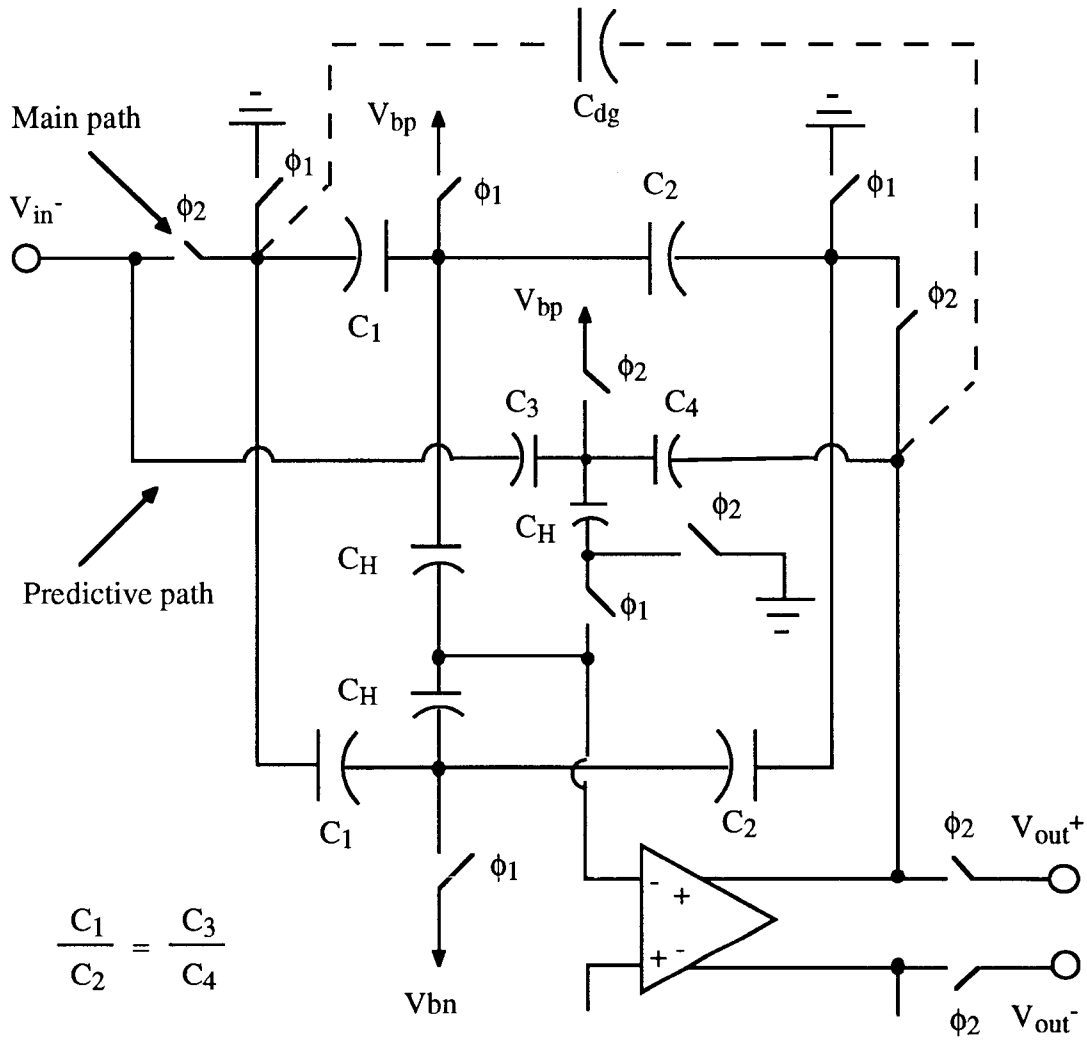


Figure 5.9 Predictive SC amplifier using parallel compensation based on the circuit of Figure 5.3a

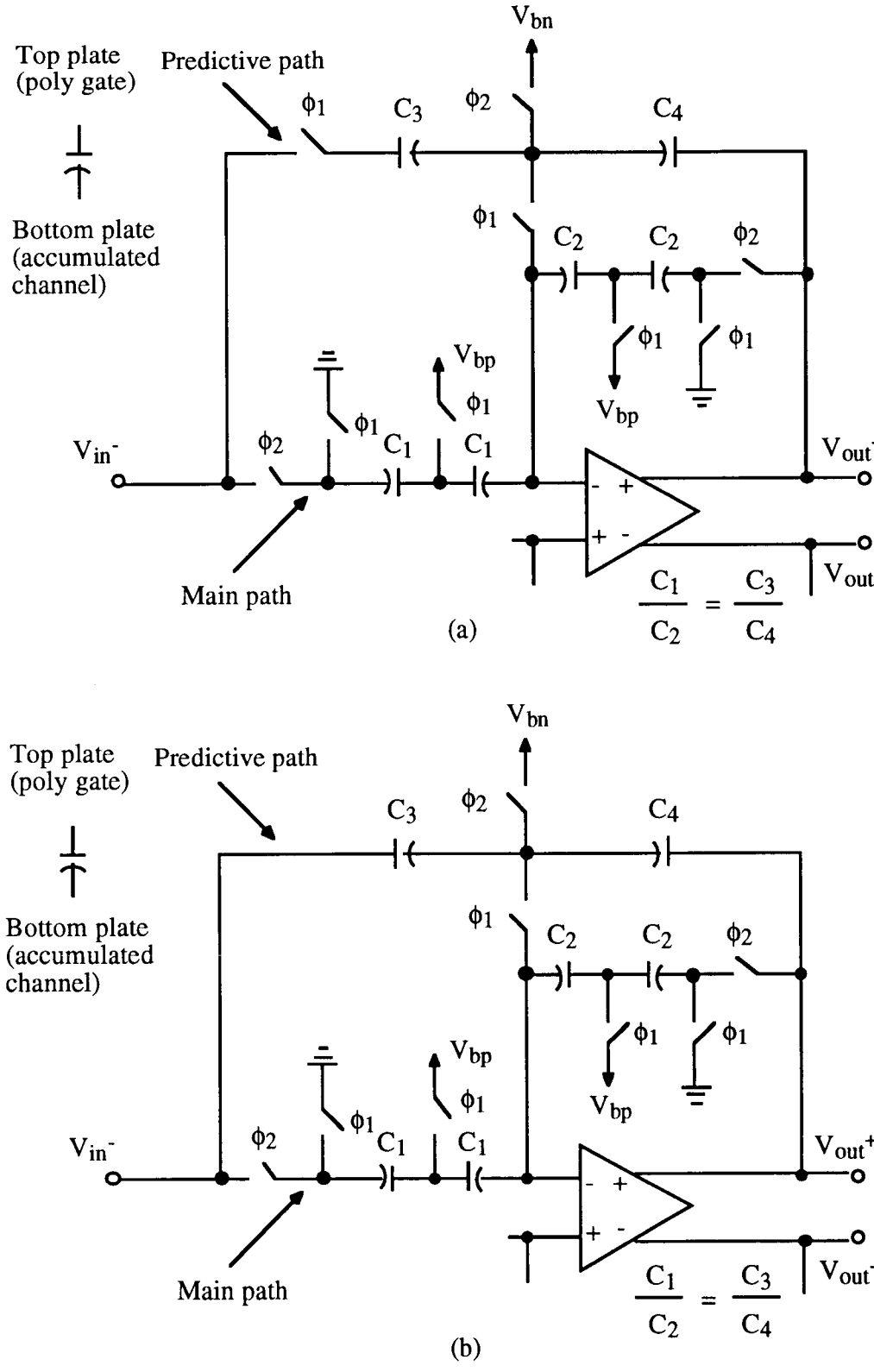
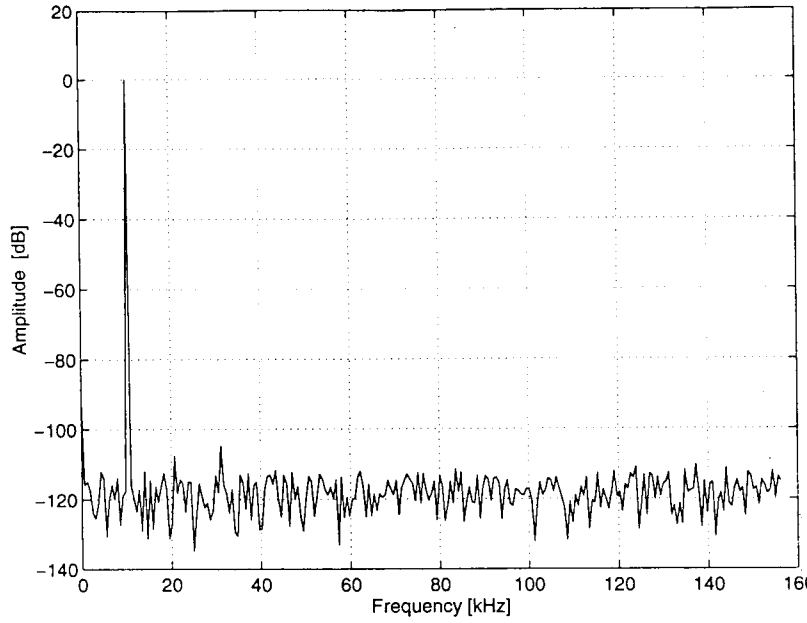
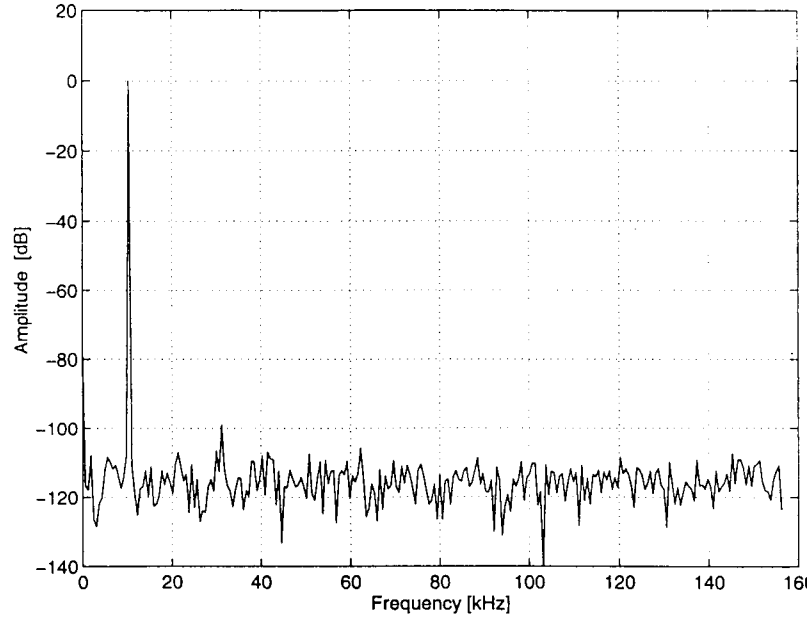


Figure 5.10 Predictive SC amplifiers using MOSFET capacitors with series compensation based on: (a) Figure 5.3b; (b) Figure 5.3a.

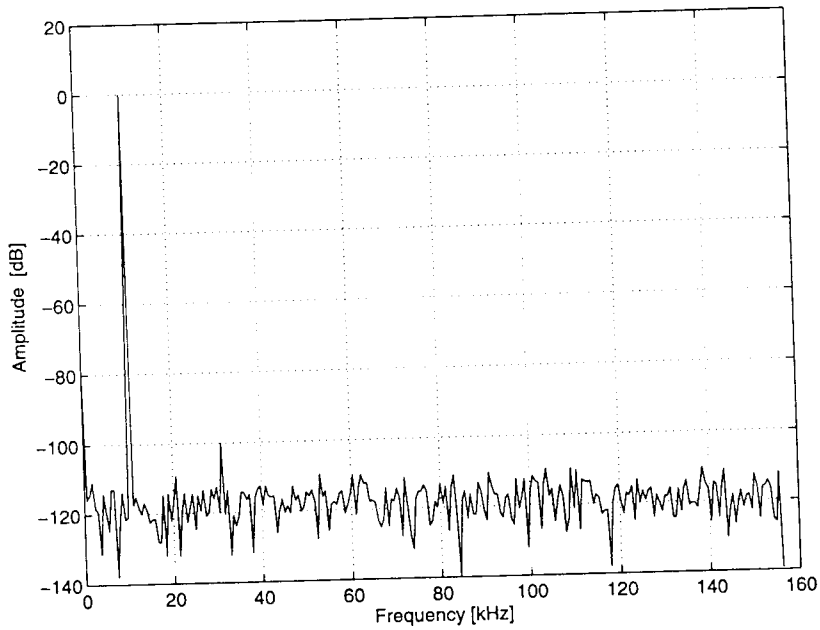


(a)



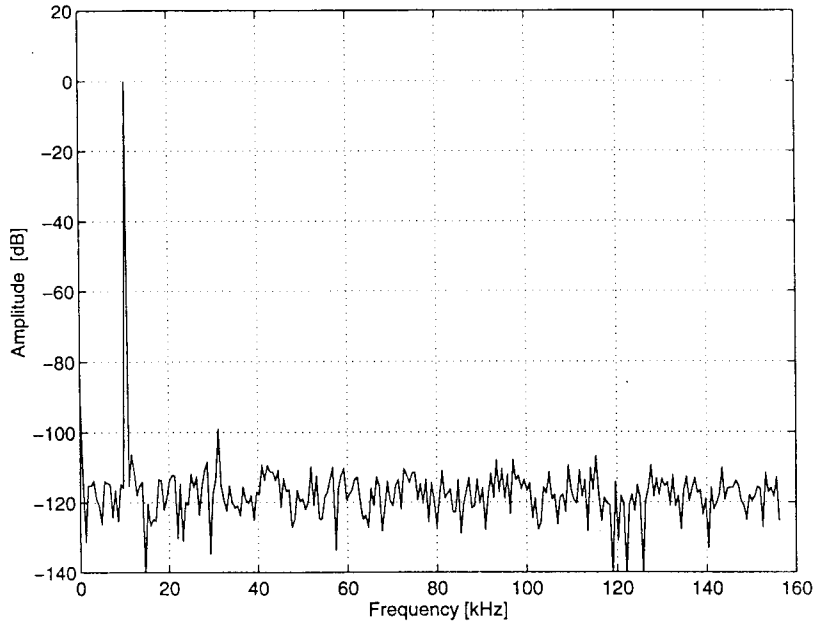
(b)

Figure 5.11 The output spectrum of the circuit: (a) Figure 5.7; (b) Figure 5.8; (c) Figure 5.9.

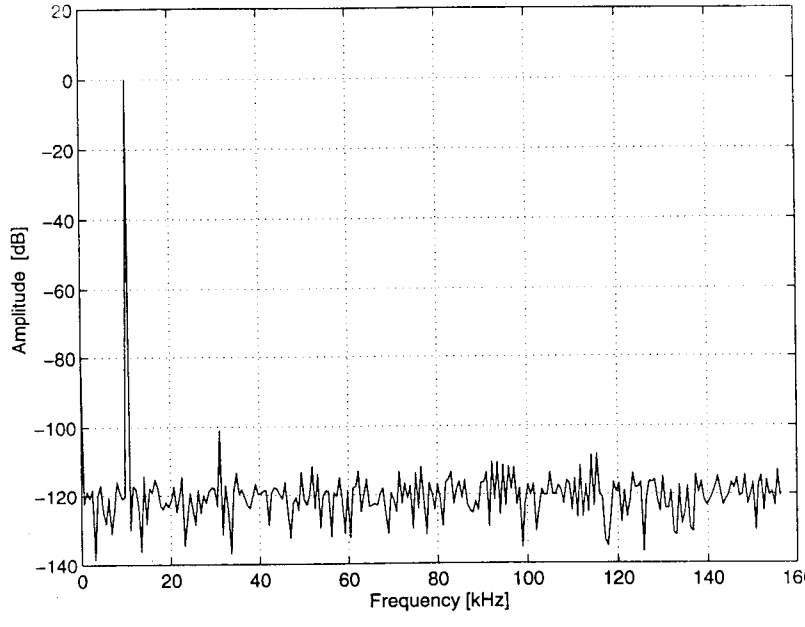


(c)

Figure 5.11 continued



(a)



(b)

Figure 5.12 The output spectrum of the circuit: (a) Figure 5.10a; (b) Figure 5.10b.

Chapter 6

EXPERIMENTAL RESULTS FOR SWITCHED-CAPACITOR AMPLIFIERS

The SC amplifiers described in Chapters 4 and 5 were fabricated in the Orbit 1.2 μm CMOS process. In this chapter, their experimental results will be shown. The test circuit, op-amp, and clock generator circuit will also be described.

6.1 Test Circuit

Figure 6.1 shows the test circuit used for SC amplifiers. Since the SC amplifiers are fully differential, a single-ended-to-differential converter was needed at the front end of the test circuit. It consists of two inverting op-amps, and it also works as a low-pass filter. The loss is 0.2 dB at 20 kHz. Linear ceramic capacitors (NPO capacitors*) were used in this test circuit to avoid signal distortion.

A 0.01 μF NPO capacitor was used from each input pin of the chip to the analog ground plane, and a 0.0047 μF NPO capacitor was placed between the input pins to minimize the RF transmission and reception capability of the inputs [31]. These capacitors will not degrade the input signal.

Several bias voltages needed by the op-amp were externally applied to the SC amplifier chip.

A buffer was connected to the output of the SC amplifier followed by a differential-to-single-ended converter. The buffer was added to drive the low input resistance of the converter because the on-chip op-amp in the SC amplifier cannot drive a resistive load. Figure 6.2 shows the differential-to-single-ended converter without its 100 pF NPO capacitors. For a

* Originally an NPO capacitor is for low temperature-coefficient use. Generally it has a low voltage-coefficient, too.

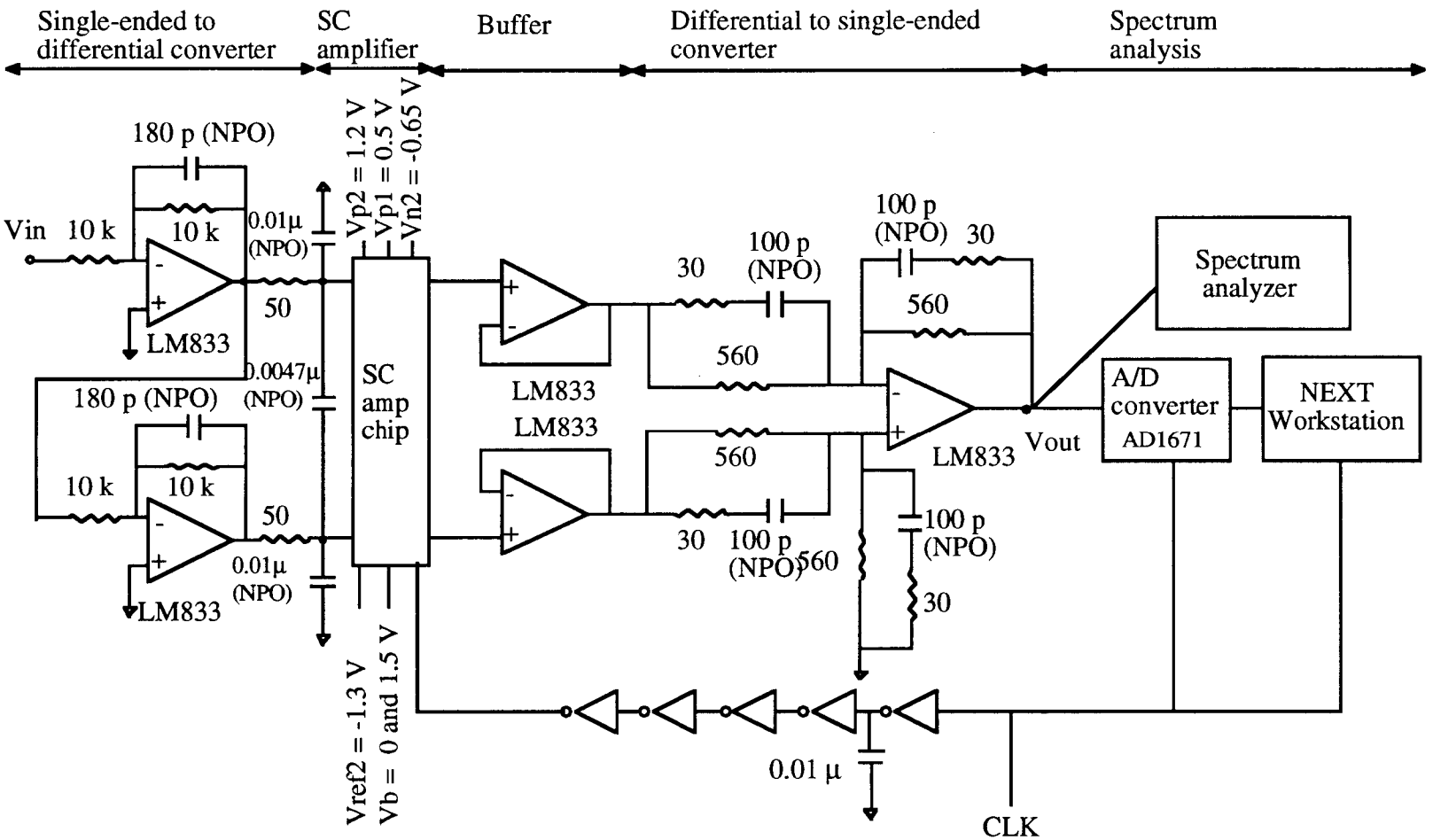


Figure 6.1 Test circuit for SC amplifiers

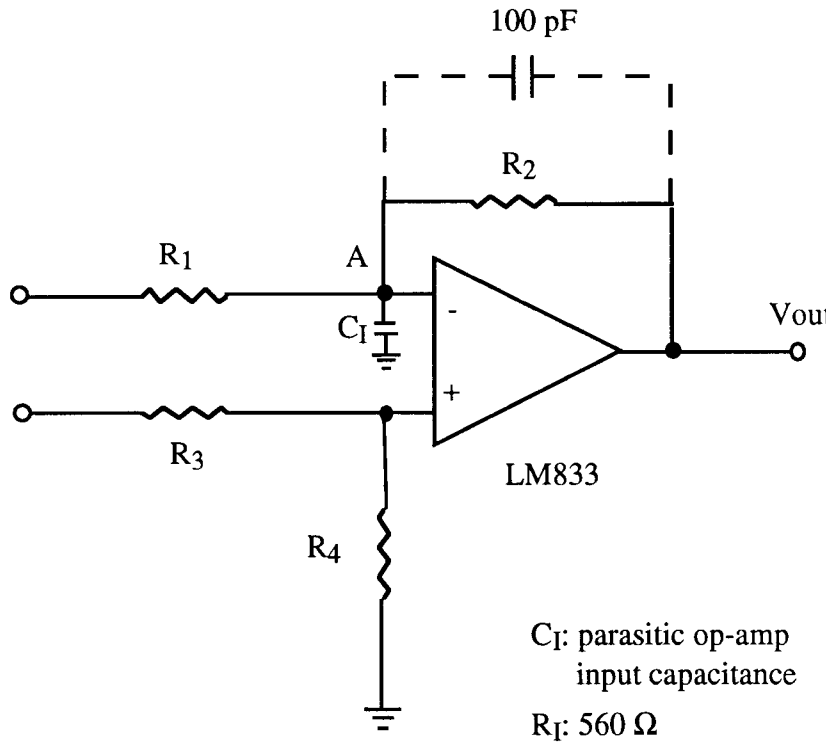


Figure 6.2 Differential-to-single-ended converter.

high-frequency signal, the voltage at node A rolls off due to resistor R_2 and parasitic capacitance C_I. To prevent this, a 100 pF NPO capacitor was connected in parallel with R_2, and also in parallel with the other 560 Ω resistors to have an equivalent impedance for a high-frequency signal. In addition, a 30 Ω resistor is connected in series with each 100 pF NPO capacitor to prevent oscillation in the op-amp in the converter due to the large capacitive load.

After the differential-to-single-ended conversion, the output signal is evaluated by the spectrum analyzer. Also, it was fed into a 12 bit A/D converter. The digital output was fed into a NEXT workstation, then FFT analysis was performed by MATLAB.

6.2 Op-Amp

Figure 6.3 shows the fully differential folded-cascode op-amp [32] which was used in the SC amplifiers. Since this is a single-stage op-amp, internal frequency compensation is not necessary. However, it requires a common-mode feedback (CMFB) circuit to keep the output common-mode voltage at the middle of the supply voltages. The CMFB circuit was realized by a switched-capacitor circuit [33]. In most of these SC amplifiers, the CMFB of the op-amp was realized using double-poly capacitors to prevent op-amp nonlinearity. In one SC amplifier, MOSFET capacitors were used in the CMFB of the op-amp for comparison. In this case, the top and bottom plate of capacitors were interchanged, as shown in Figure 6.4, so that all MOSFET capacitors had a positive dc bias voltage and operated in their accumulation region.

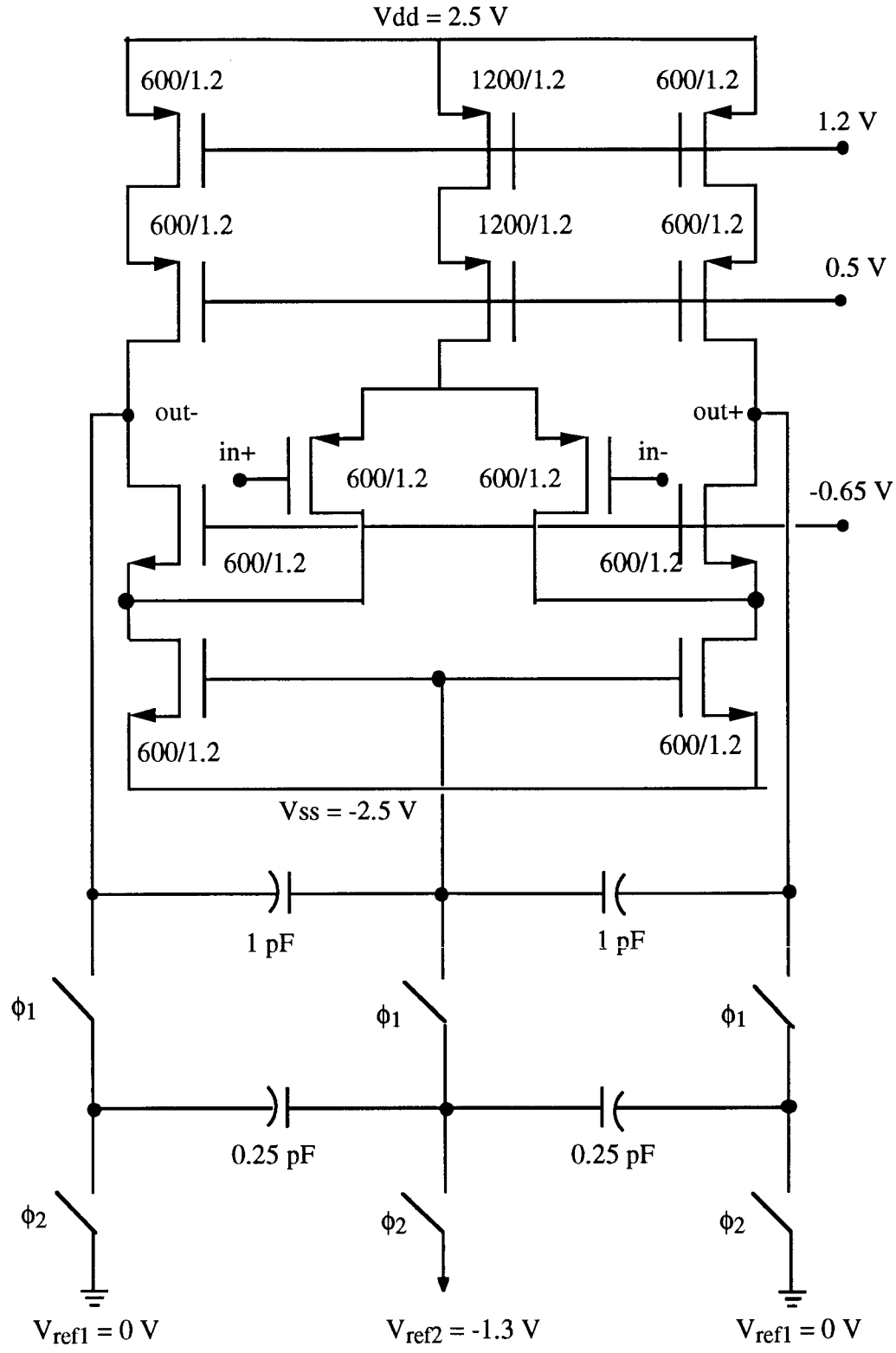


Figure 6.3 Folded-cascode op-amp [32]

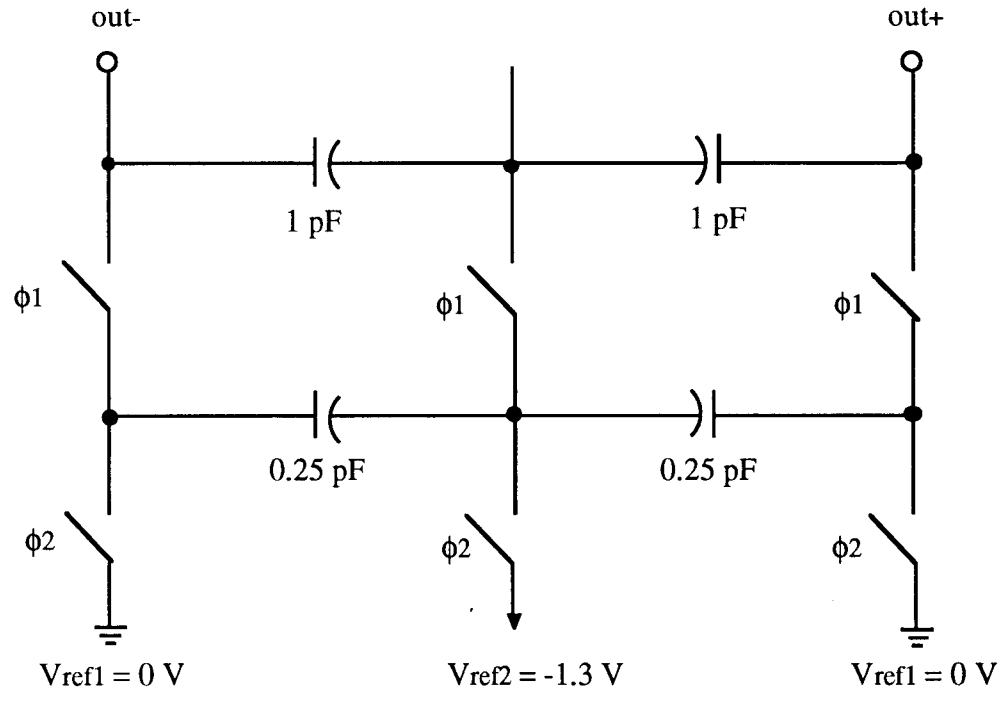


Figure 6.4 Common-mode feedback circuit using MOSFET capacitors

6.3 Clock Generator

Figure 6.5 shows the clock generator circuit. For the last two inverters, analog V_{DD} and V_{SS} were used. For the rest, digital V_{DD} and V_{SS} were applied. The layout of the clock generator circuit is shown in Figure 6.6.

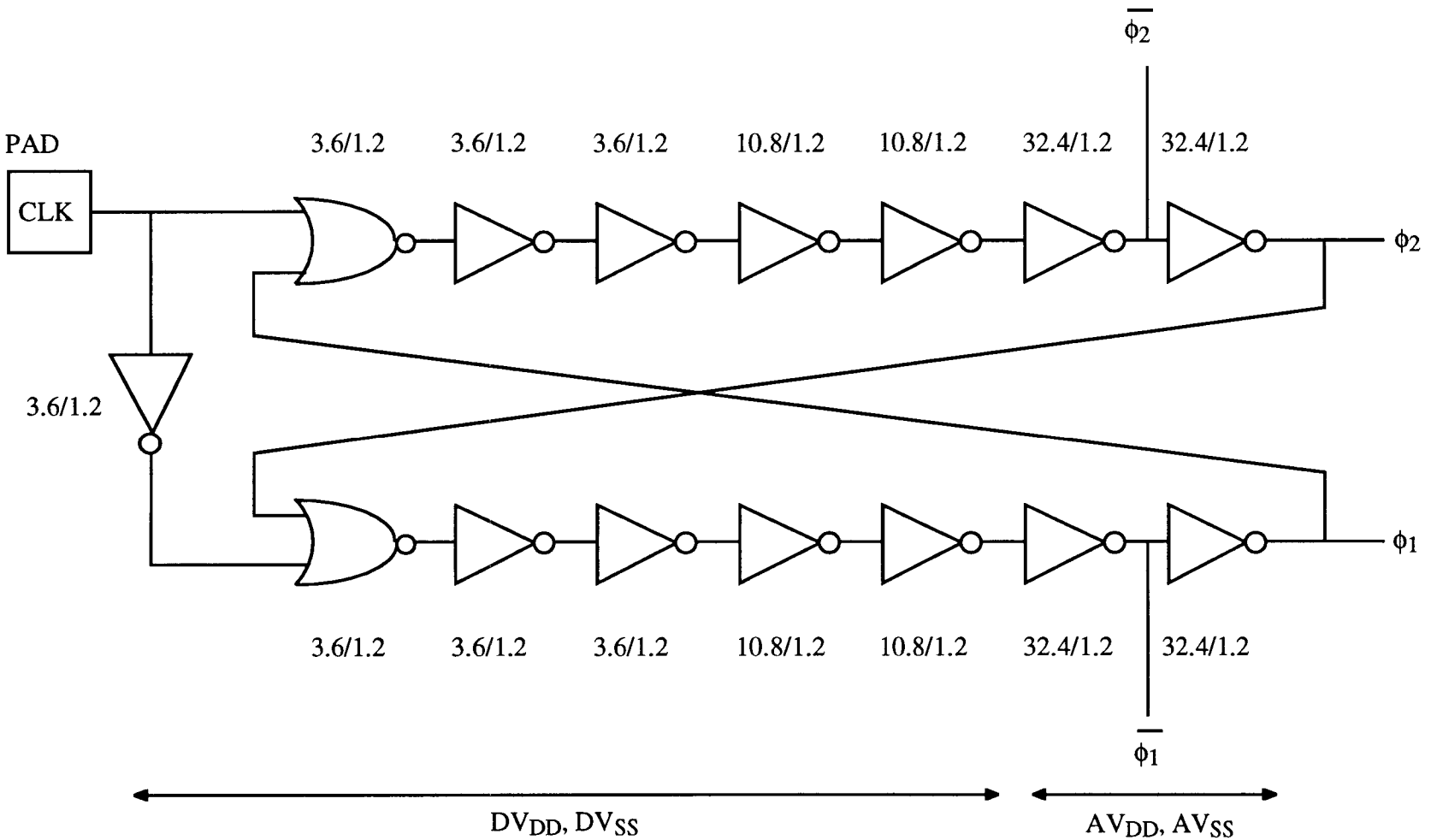


Figure 6.5 Clock generator circuit

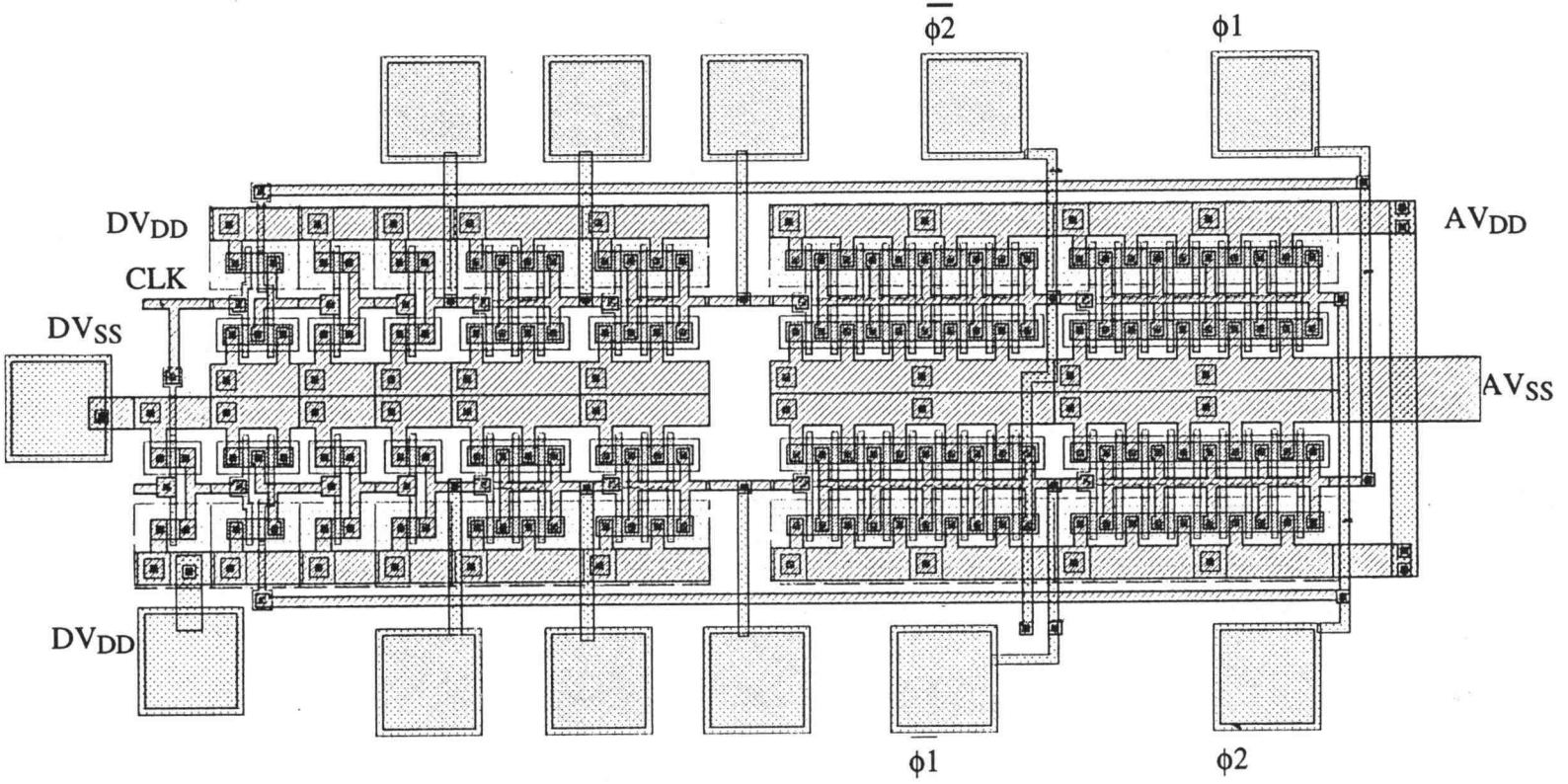


Figure 6.6 Layout of the clock generator circuit

6.4 Experimental Results

Six kinds of SC amplifiers, described in Table 6-1, were fabricated in the Orbit 1.2 μm CMOS process. Their die photos and pad locations are shown in Figures 6.7-6.9. A spectrum analyzer was used to obtain the experimental results described in Section 6.4.1-6.4.9. Section 6.4.10 gives the results obtained by using an A/D converter and NEXT workstation.

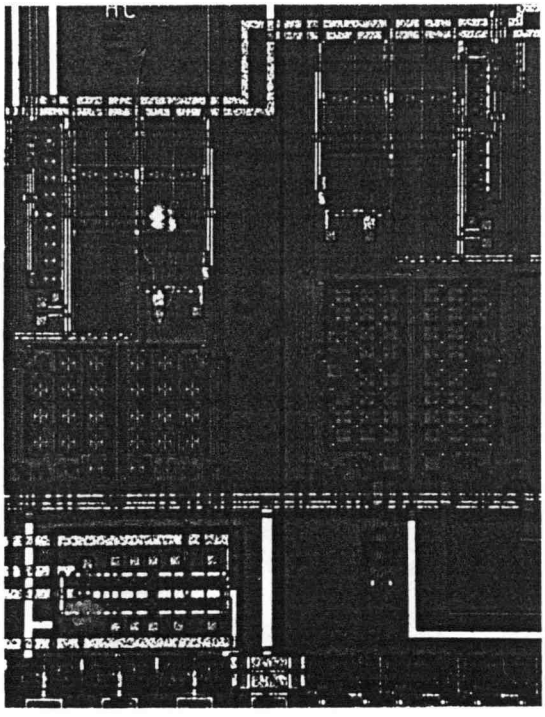
Table 6-1 SC amplifiers on chip

	Figure	SC amplifier code name	Capacitor compensation method	Capacitor array	CMFB of op-amp
(1)	6.8	DP	Without compensation	Double-poly	Double-poly
(2)	6.7	SCOMP_1	Series compensation	MOSFET	Double-poly
(3)	6.8	SCOMP_2	Series compensation	MOSFET	MOSFET
(4)	6.7	SB	Simple biasing	MOSFET	Double-poly
(5)	6.9	PCOMP_1	Parallel compensation	MOSFET	Double-poly
(6)	6.9	PCOMP_2	Parallel compensation (Predictive SC amp)	MOSFET	Double-poly

6.4.1 Non-Predictive SC Amplifier with Simple Biasing

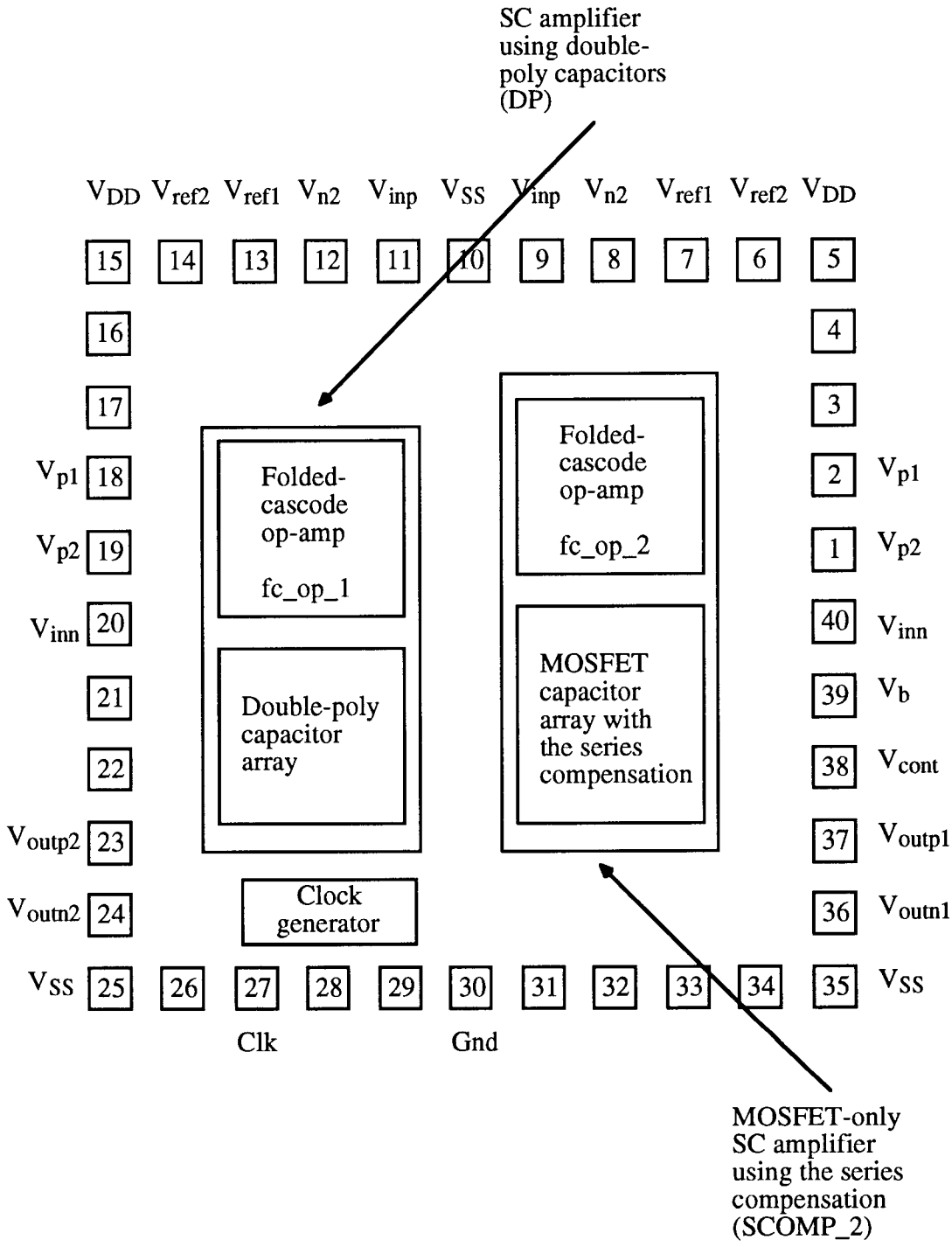
Figure 6.10 shows the output spectra measured using the spectrum analyzer of the simpler circuit of Figure 4.2 with $V_b = 0$ V and 1.5 V. The input signal (V_{in} in Figure 6.1) was a 1 kHz, 200 mVp-p sinewave. Hence, after the differential-to-single-ended conversion, the output signal was a 4 Vp-p sinewave. This was a large amplitude for the +/- 2.5 V bias voltages used. The clock frequency was 16 kHz. Without the bias voltage, the output waveform was totally distorted (Figure 6.10a). With a bias voltage of 1.5 V (Figure 6.10b), the largest harmonic component was 58 dB below the input signal. Thus, it was shown that the simple biasing could reduce the nonlinearity caused by the MOSFET

capacitors. In Figure 6.10b, we can see both the second and third harmonic components at the same level. Even though this SC amplifier is a fully differential circuit, the second harmonic component was not cancelled. It is likely that it was due to the effect of the offset voltage of the SC amplifier.



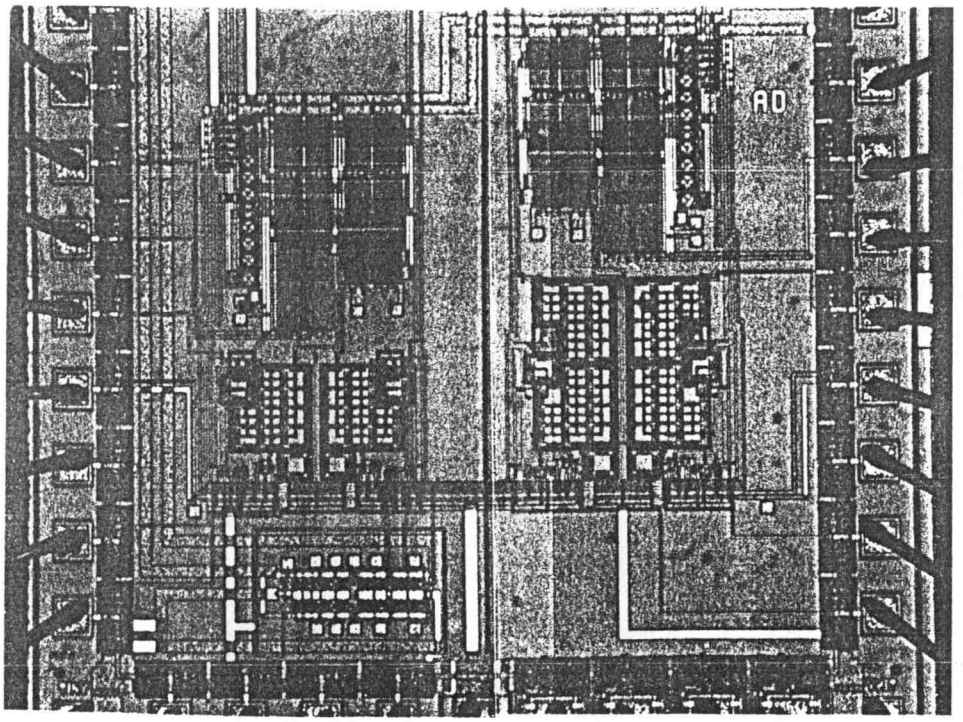
(a)

Figure 6.7 SC amplifiers (1)(3): a) die photo; b) floor plan.



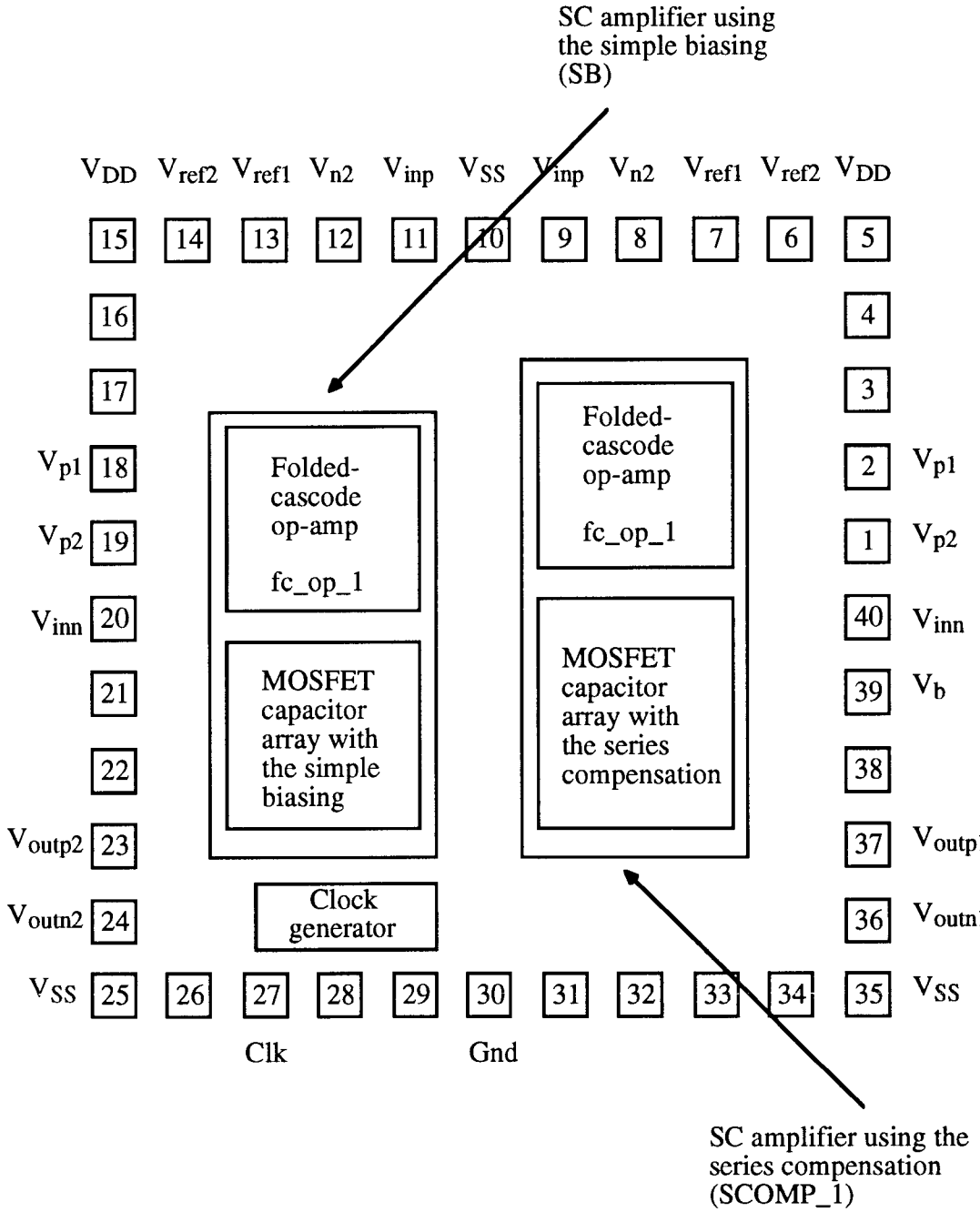
(b)

Figure 6.7 continued.



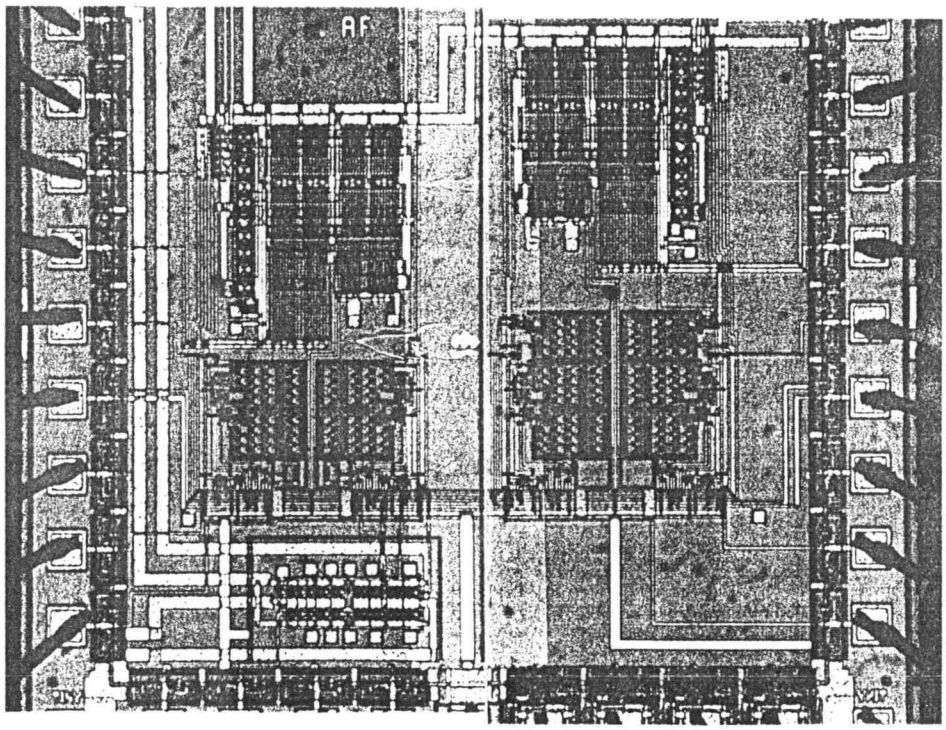
(a)

Figure 6.8 SC amplifiers (2)(4): a) die photo; b) floor plan.



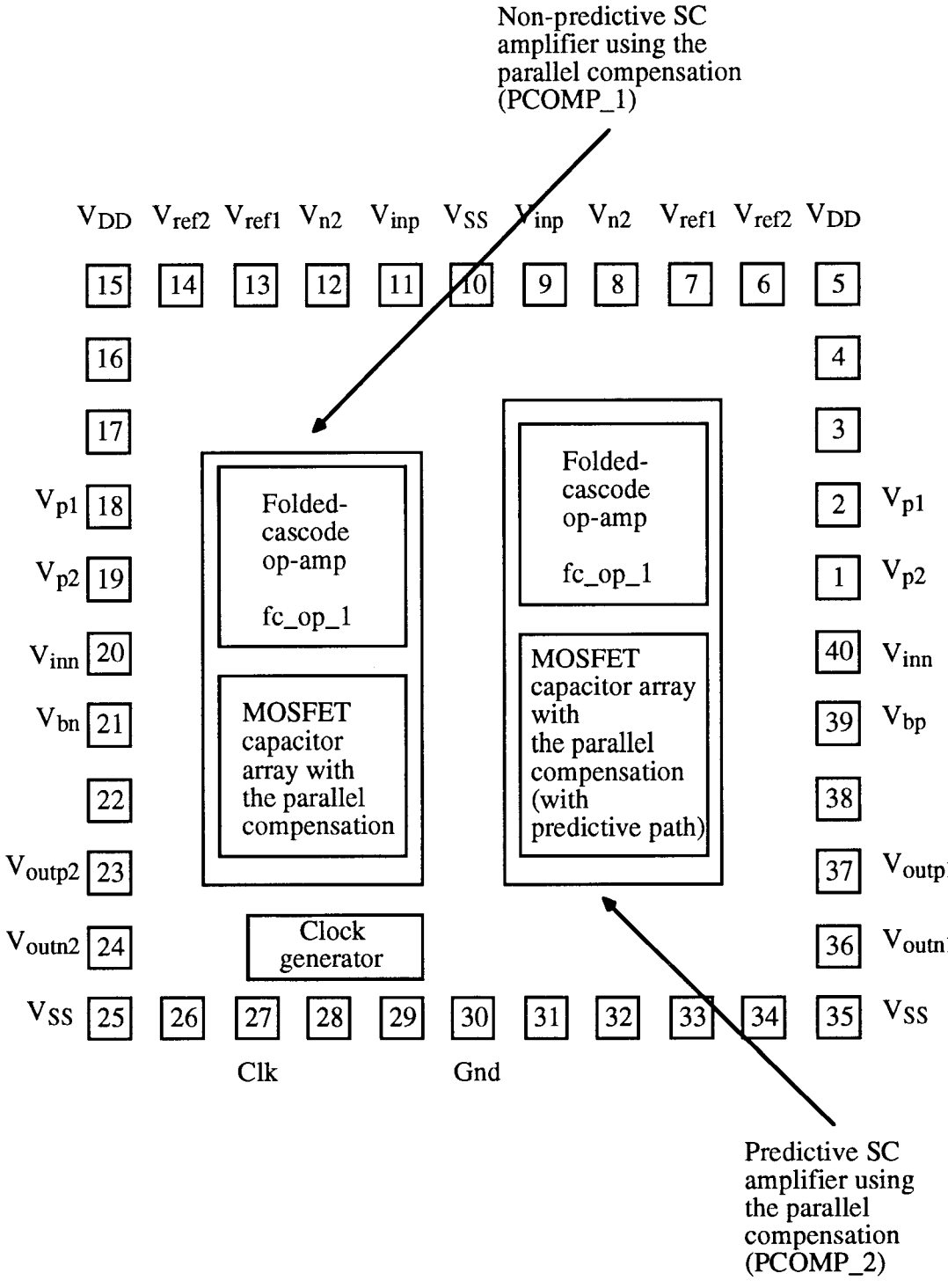
(b)

Figure 6.8 continued.



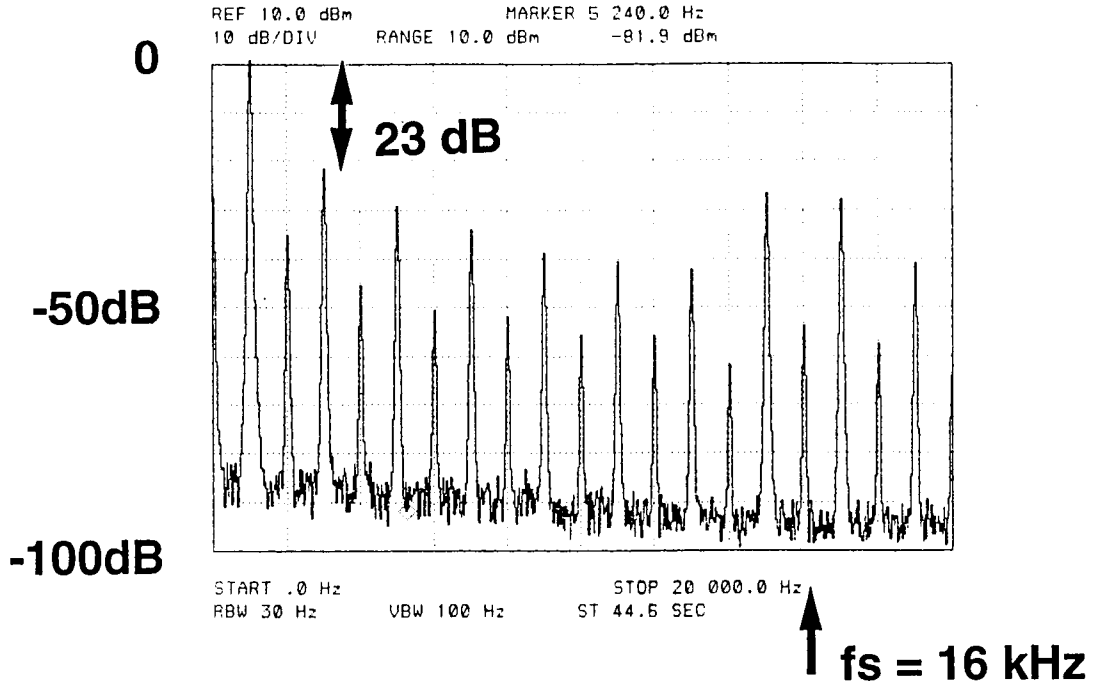
(a)

Figure 6.9 SC amplifiers (5)(6): a) die photo; b) floor plan.

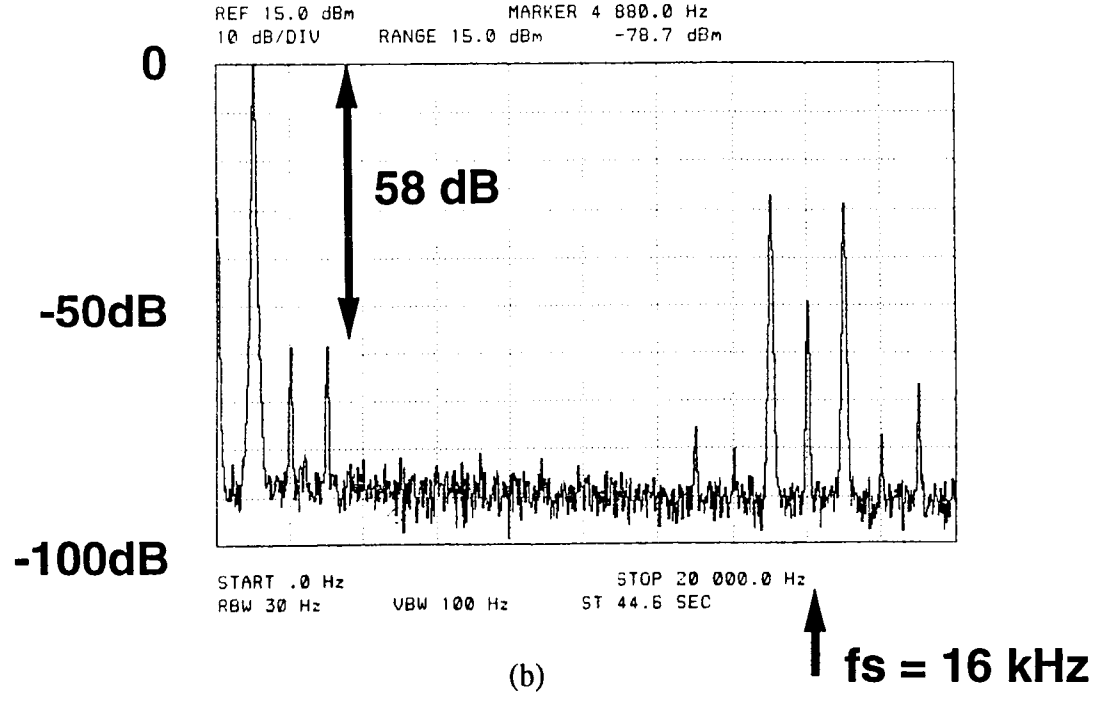


(b)

Figure 6.9 continued.



(a)



(b)

Figure 6.10 The measured output spectra of the SC amplifier using simple biasing: a) $V_b = 0$ V; b) $V_b = 1.5$ V;

6.4.2 Non-Predictive SC Amplifier with Series Compensation

Figure 6.11 shows the output spectrum measured with the spectrum analyzer of the circuit of Figure 4.8 using the series compensation scheme, with V_b = 1.5 V. Now the largest harmonic component was 72 dB below the fundamental of the input signal; the signal-to-THD ratio was 70 dB. Thus, the linearity of the circuit was further improved by the series compensation scheme. In Figure 6.11, we see higher-order harmonic components. It is likely that they were caused by the interactive effects of the op-amp and MOSFET capacitor nonlinearities.

Figure 6.12 shows the output waveform observed on an oscilloscope.

6.4.3 Non-Predictive SC Amplifier Using Double-Poly Capacitors

Figure 6.13 shows the output spectrum measured using the spectrum analyzer of the circuit of Figure 4.1 using double-poly capacitors, with V_b = 1.5 V. Now the largest harmonic component was 70 dB below the fundamental of the input signal; the signal-to-THD ratio was 69 dB. Therefore, a large part of this small remaining nonlinear distortion can be attributed to the op-amp, which had a narrow linear output voltage range.

6.4.4 Non-Predictive SC Amplifier with Parallel Compensation

Figure 6.14 shows the output spectrum measured using the spectrum analyzer of the circuit of Figure 4.5 using the parallel compensation scheme, with $V_{bp} = -V_{bn} = 2.5$ V. The largest harmonic component was 57 dB below the signal level, which is nearly the same as the result obtained by the simple biasing arrangement. However, HSPICE simulations show that a S/THD of 86 dB can be obtained using an ideal op-amp. The post-layout simulation showed that the S/THD is limited to 67 dB because of the small linear output range of the folded-cascode op-amp used in the chip.

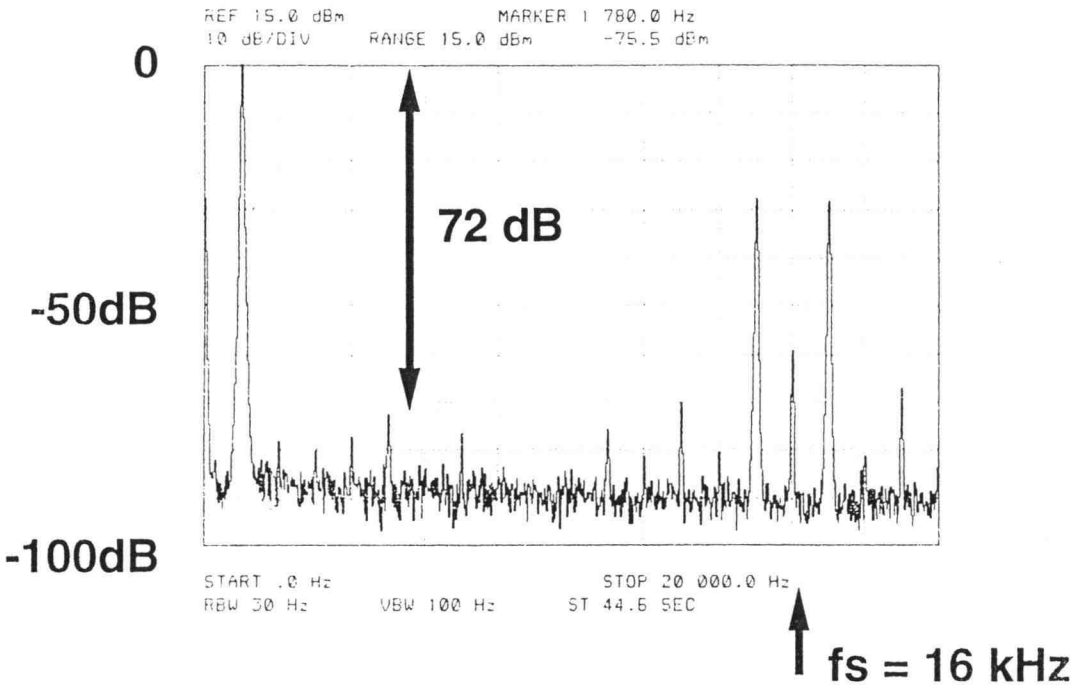


Figure 6.11 The measured output spectrum of the SC amplifier using the series compensation with V_b = 1.5 V.

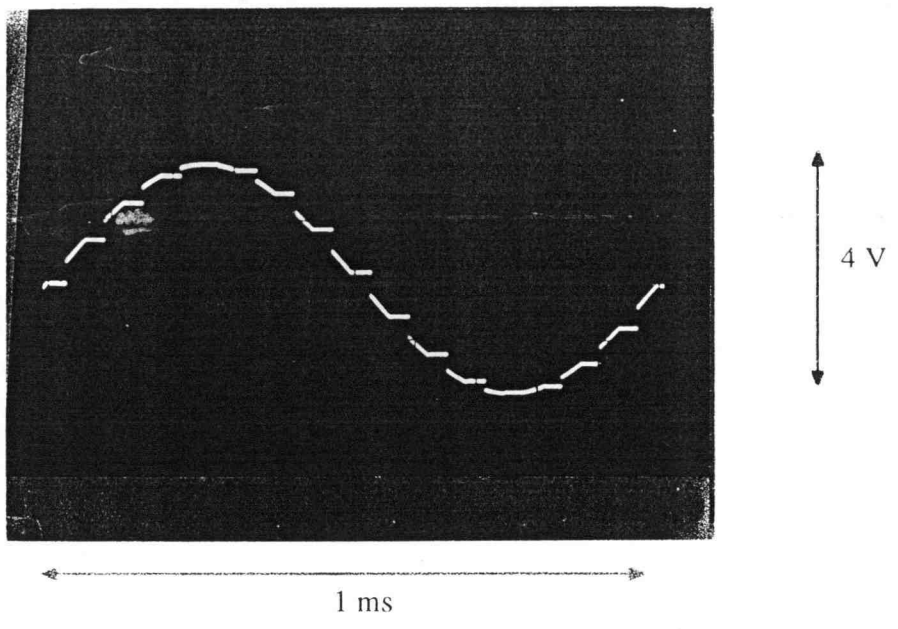


Figure 6.12 The output waveform of the SC amplifier using the series compensation with V_b = 1.5 V.

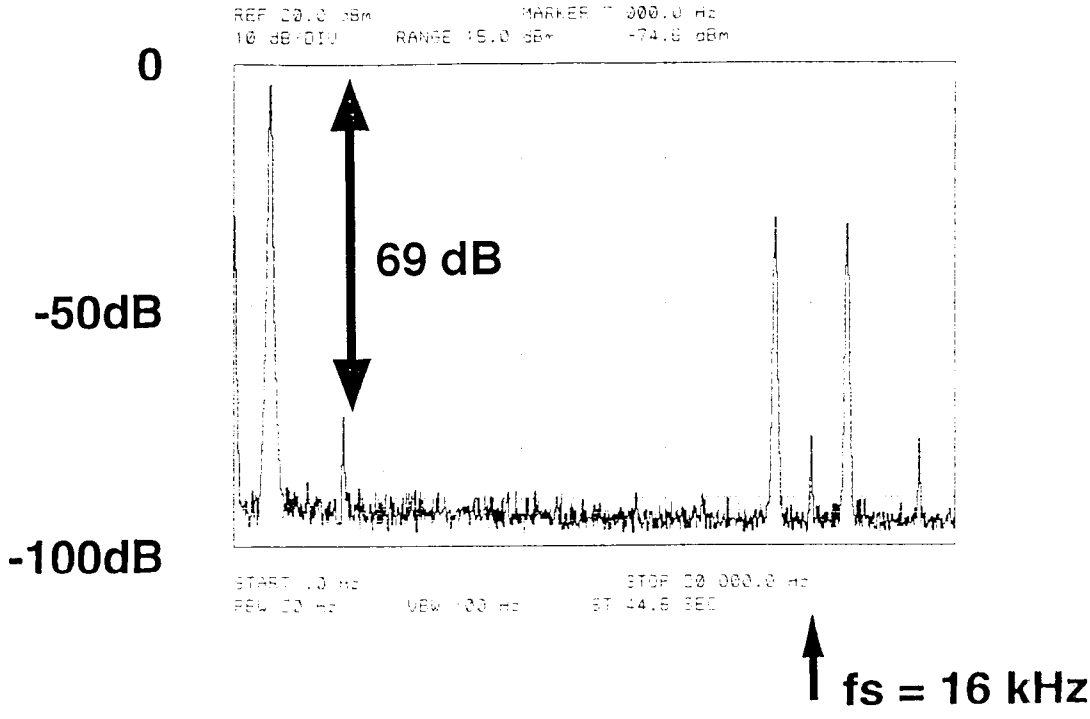


Figure 6.13 The measured output spectrum of the SC amplifier using double-poly capacitors.

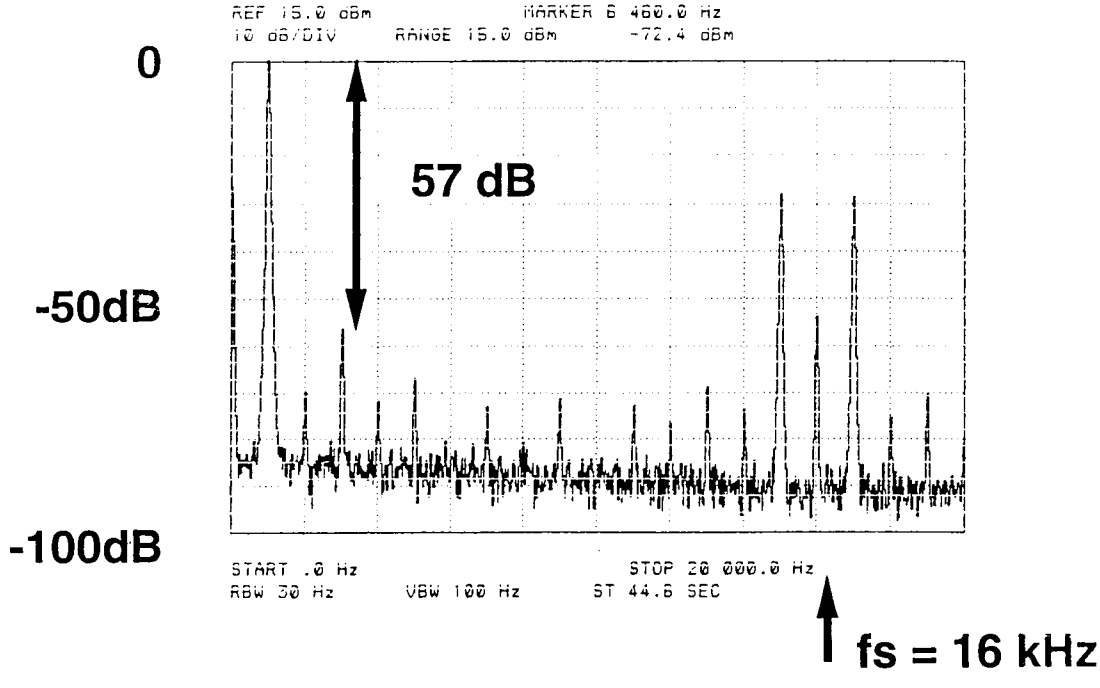


Figure 6.14 The measured output spectrum of the SC amplifier using the parallel compensation with $V_{bp} = -V_{bn} = 2.5$ V.

6.4.5 Predictive SC Amplifier with Parallel Compensation

Figure 6.15 shows the output spectrum measured with the spectrum analyzer of the predictive SC amplifier using the parallel compensation scheme shown in Figure 5.7, with $V_{bp} = -V_{bn} = 2.5$ V. Its largest harmonic component was 66 dB below the signal level. Thus, the predictive SC amplifier had a 9 dB linearity improvement compared to the non-predictive SC amplifier of Figure 4.5. The post-layout simulation by HSPICE also showed that a 9 dB linearity improvement can be obtained by the predictive SC amplifier compared to the non-predictive one.

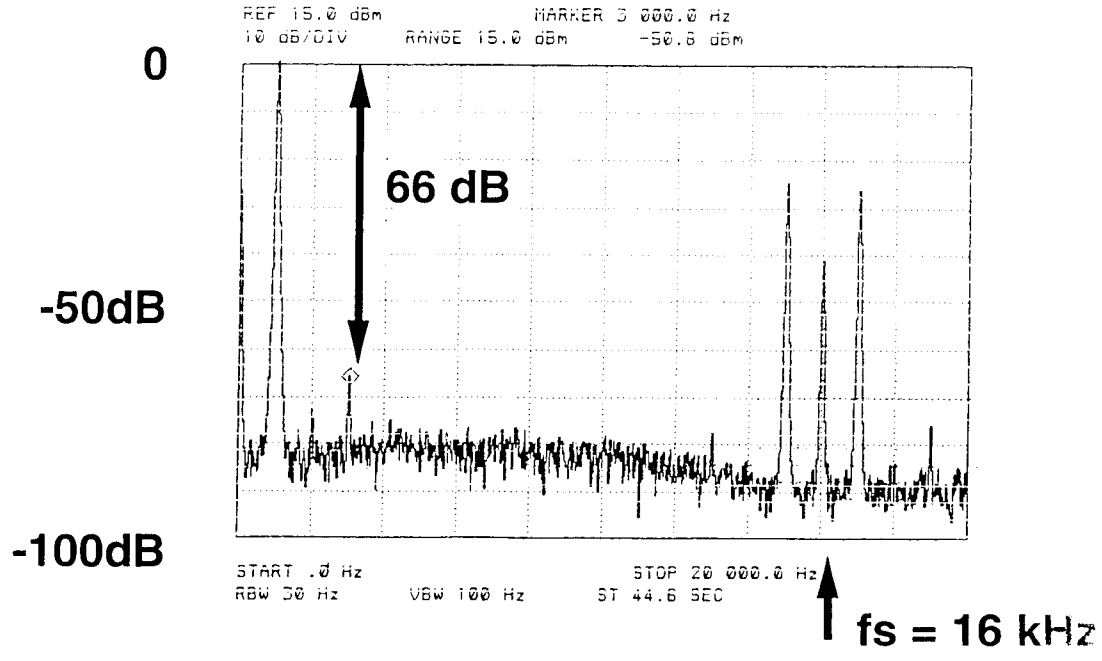


Figure 6.15 The measured output spectrum of the predictive SC amplifier using the parallel compensation with $V_{bp} = -V_{bn} = 2.5$ V.

6.4.6 Output Swing (Inverting Mode)

Table 6-2 shows the largest harmonic components and S/THD ratios obtained using a spectrum analyzer HP 3585B for a differential output swing of 2 Vp-p and 4 Vp-p. An input signal frequency was 1 kHz and a clock frequency was 16 kHz. All SC amplifiers were in their inverting mode.

Table 6-2 Input signal frequency (f_{in}): 1 kHz; clock frequency (f_S): 16 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-79 dB	-70 dB	76 dB	69 dB
SCOMP_1	-67 dB	-71 dB	64 dB	67 dB
SCOMP_2	-70 dB	-64 dB	66 dB	62 dB
SB	-71 dB	-58 dB	68 dB	57 dB
PCOMP_1	-56 dB	-57 dB	55 dB	56 dB
PCOMP_2	-73 dB	-66 dB	68 dB	65 dB

For most of these results, an S/THD ratio decreases as an output increases. For example, an S/THD of SC amplifier DP is limited to 69 dB for 4 V_{p-p} output swing. It was caused by the small linear output range of the op-amp.

In SCOMP_1, the common-mode feedback (CMFB) circuit of the op-amp consists of double-poly capacitors and the rest of the SC amplifier were MOSFET capacitors. On the other hand, in SCOMP_2, all capacitors in the SC amplifier were MOSFET capacitors including the CMFB circuit of the op-amp. For a large output swing, SCOMP_1 shows a better result than SCOMP_2. This is because in SCOMP_2 no specific compensation but

simple biasing was given in MOSFET capacitors of CMFB circuit, and these capacitors were out of the linear (accumulation) region when the output swing became large.

For an output swing of 2 Vp-p, SC amplifier SB showed comparable results with SCOMP_1 and SCOMP_2 because the nonlinearity of MOSFET capacitors were considerably smaller in this operating range. However, the linearity of SB is much lower than that of SCOMPs for a large signal swing.

Parallel compensation was not effective in this testing. For 4 Vp-p, PCOMP_1 is only comparable to SB. For 2 Vp-p, PCOMP_1 was much worse than other amplifiers. The linear output range of the op-amp should be fine, therefore the capacitance was limiting the performance. However, once a predictive path is added, the linearity is much improved. At 2 Vp-p voltage swing, the largest harmonic component of PCOMP_2 was 14 to 17 dB smaller than that of PCOMP_1.

6.4.7 Frequency Dependence (Inverting Mode)

To investigate a frequency dependence of these circuits, measurements were also performed with an input signal frequency of 100 Hz and 10 kHz. The test results are shown in Table 6-3. The results for an input signal frequency of 100 Hz were nearly the same as those for 1 kHz. However, linearity worsened at 10 kHz even for the SC amplifier using double-poly capacitors. Since MOSFET capacitors are operating in their accumulation region, these capacitors should be just as frequency independent as the double-poly capacitors. Therefore, it is presumed that the degradation of linearity at 10 kHz were caused by the op-amp slew rate and/or the on-resistance of the switches.

Table 6-3 (a) Input signal frequency (f_{in}): 100 Hz; clock frequency (f_S): 1.6 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-79 dB	-71 dB	75 dB	71 dB
SCOMP_1	-65 dB	-73 dB	62 dB	67 dB
SCOMP_2	-71 dB	-66 dB	67 dB	64 dB
SB	-72 dB	-58 dB	69 dB	57 dB
PCOMP_1	-56 dB	-58 dB	55 dB	57 dB
PCOMP_2	-73 dB	-63 dB	69 dB	62 dB

Table 6-3 (b) Input signal frequency (f_{in}): 10 kHz; clock frequency (f_S): 160 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-66 dB	-57 dB	65 dB	57 dB
SCOMP_1	-67 dB	-53 dB	65 dB	51 dB
SCOMP_2	-61 dB	-52 dB	60 dB	50 dB
SB	-66 dB	-55 dB	63 dB	54 dB
PCOMP_1	-55 dB	-51 dB	54 dB	50 dB
PCOMP_2	-69 dB	-59 dB	66 dB	58 dB

6.4.8 Non-inverting Mode

Table 6-4 shows the experimental results for SC amplifiers in the non-inverting mode. Again, the largest harmonic components and S/THD ratios are shown for various input signal frequencies and output swings.

Table 6-4 (a) Input signal frequency (f_{in}): 100 Hz; clock frequency (f_S): 1.6 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-76 dB	-66 dB	74 dB	66 dB
SCOMP_2	-69 dB	-66 dB	65 dB	64 dB

Table 6-4 (b) Input signal frequency (f_{in}): 1 kHz; clock frequency (f_S): 16 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-72 dB	-64 dB	71 dB	63 dB
SCOMP_2	-68 dB	-67 dB	65 dB	63 dB

Table 6-4 (c) Input signal frequency (f_{in}): 10 kHz; clock frequency (f_S): 160 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-57 dB	-51 dB	57 dB	50 dB
SCOMP_2	-57 dB	-54 dB	56 dB	50 dB

For SC amp using double-poly capacitors, the output waveform has double steps as shown in Figure 6.16 because during $\phi 1=1$, charge coming from the input capacitor and charge coming from the feedback capacitor do not cancel each other. In addition, the output voltage keeps changing as the input voltage changes.

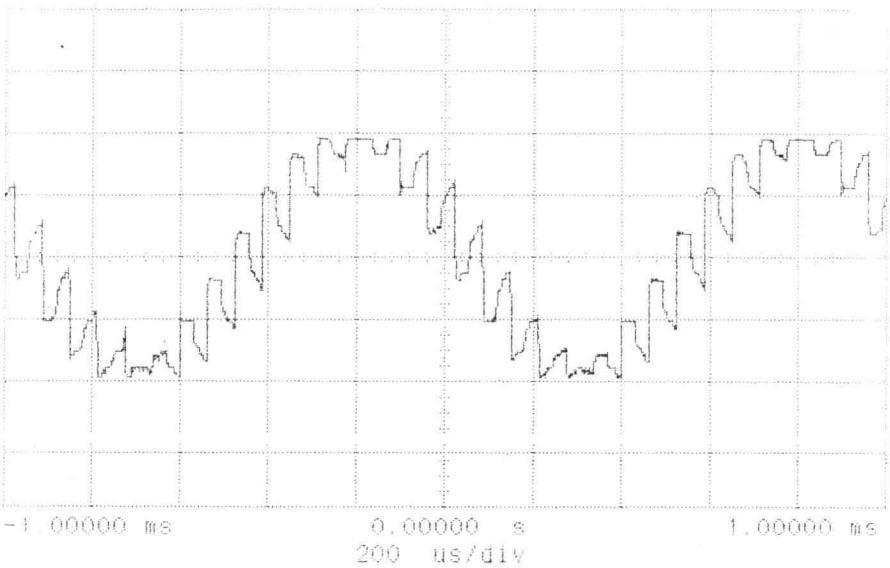


Figure 6.16 The output waveform of the non-inverting SC amplifier using double-poly capacitors.

By contrast, for the MOSFET-only SC amplifier SCOMP_2, the output waveform is kept constant even during the reset phase $\phi 1$ as shown in Figure 6.17. This is because charge coming from the input capacitor and charge coming from the feedback capacitor have opposite polarities and the same amount of charges. Hence they cancel each other, and no charge is flowing into the supporting capacitor Cs in Figure 4.8.

Therefore, CDS is less effective for SC amplifier DP in the non-inverting mode compared with the inverting mode. And hence, experimental results in the non-inverting mode were not so good as those in the inverting mode. By contrast, the MOSFET-only SC amplifier SCOMP_2 in the non-inverting mode has a comparable linearity with that in the inverting mode because CDS is working effectively.

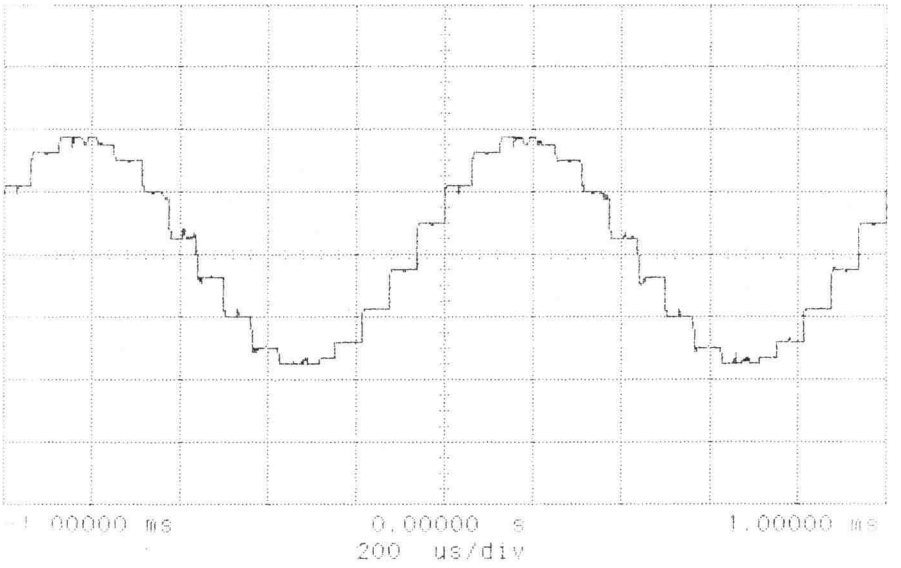


Figure 6.17 The output waveform of the non-inverting SC amplifier using series compensation.

6.4.9 Continuous Output Waveform without Clock Signal

SC amplifier circuits were evaluated without having clock signals. Suppose that all circuits have inverting-mode configuration. After working in a regular condition for a while, the clock signals were changed in such a way that $\phi 2$ was kept high while $\phi 1$ remained low. Then these amplifiers worked as continuous-time inverting amplifiers, as shown in Figures 6.18 and 6.19. Since there is no DC path to their virtual grounds, the op-amp saturates within 20 to 30 seconds after the clock was stopped, and then these circuits could not work properly anymore. However, that period was enough to store the output waveforms for FFT analysis. Table 6-5 shows the linearity of SC amplifiers without clock signals. The input signal frequency was 10 kHz.

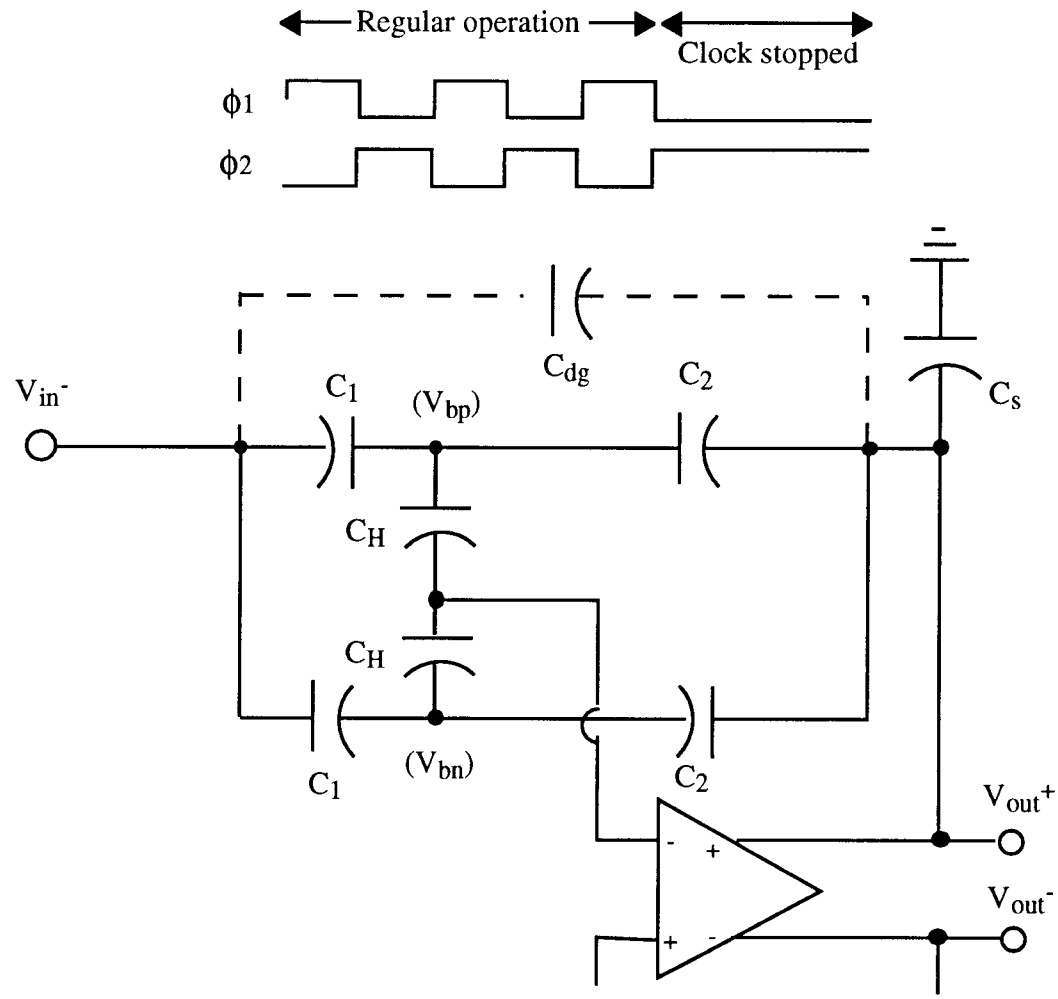


Figure 6.18 SC amplifier using the parallel compensation at $\phi 2=1$.

Table 6-5 Input signal frequency (f_{in}): 10 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-83 dB	-73 dB	79 dB	72 dB
SCOMP_2	-84 dB	-72 dB	81 dB	71 dB
SB	-69 dB	-57 dB	67 dB	56 dB
PCOMP_1	-80 dB	-72 dB	77 dB	70 dB
PCOMP_2	-84 dB	-76 dB	81 dB	73 dB

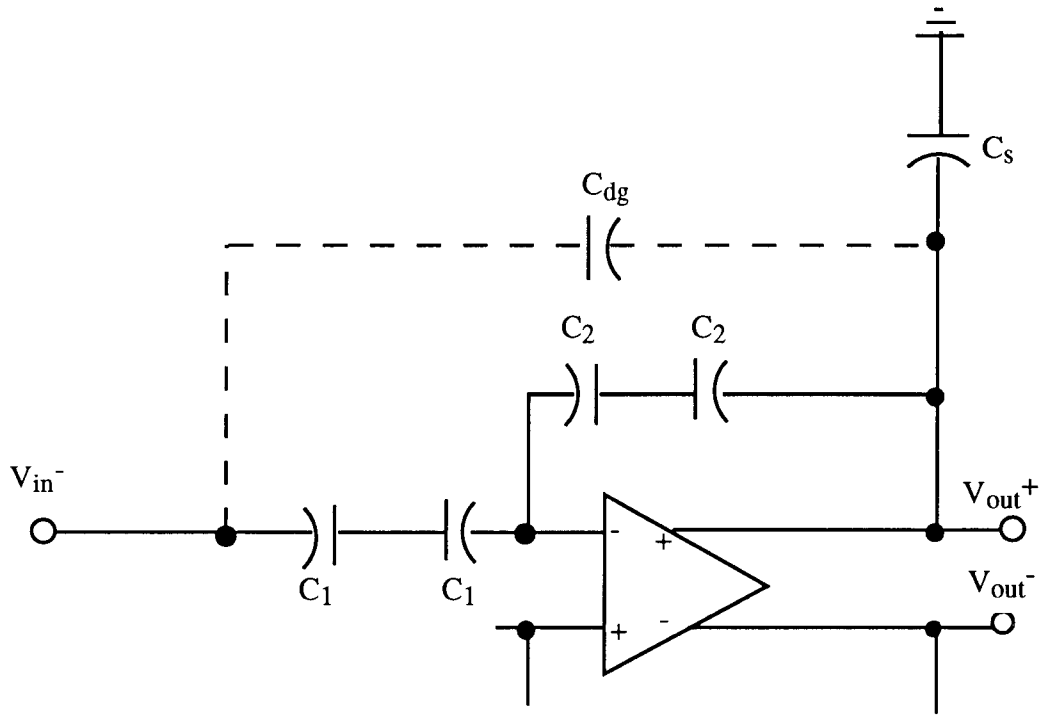


Figure 6.19 SC amplifier using the series compensation at $\phi 2=1$.

In these experiments, the S/THD values were nearly the same for both SC amplifiers, those with double-poly capacitors and those with MOSFET capacitors using series compensation: 79 dB and 81 dB for vout = 2 Vp-p, and 72 dB and 71 dB for vout = 4 Vp-p, respectively. (MOSFET capacitors seems to have obtained a better result than double-poly, however, the differences are considered to be in the error range.) The limiting factors in these results are the signal source and the op-amp.

The linearity was much better for a 2 Vp-p output swing than for 4 Vp-p. The S/THD ratio was 72 dB for DP (double-poly capacitors), and it is presumed that it was limited by the linearity of the op-amp. Notice that for the SCOMP_2 (series compensation) and PCOMP_1 (parallel compensation), the S/THD ratios were comparable to that of the DP. In these two circuits, a pair of MOSFET capacitors compensate each other's capacitance variations due to voltage change.

The S/THD ratio of SB is only 56 dB for a 4 Vp-p output swing, because the capacitance variation due to the voltage swing is not compensated in the SB.

Notice again that the predictive amplifier PCOMP_2 is better than the non-predictive one PCOMP_1. This can be explained as follows. Once $\phi 2$ is kept high level, the resulting circuit is the same for both PCOMP_1 and PCOMP_2. However, during the regular clocked operation, the potentials of their virtual grounds are slightly different from each other because they are related to their output voltage. (PCOMP_2 has a better linearity than PCOMP_1.) Therefore, in each amplifier, the error voltage at the virtual ground is stored on the capacitors connected to the virtual ground. There is no charge flowing in or out of the virtual ground node after $\phi 2$ becomes constantly high. Therefore, based on the error voltage at the virtual ground, the linearity of SC amplifier is determined. It is even better than for the DP because predictive CDS can reduce the nonlinearity caused by the op-amp [28].

6.4.10 FFT Analysis Using an A/D Converter and NEXT Workstation

Experimental results described in previous sections were measured using a spectrum analyzer. Hence, all undesirable effects such as glitches and slewing were incorporated in the spectra.

To eliminate these effects from the measured spectra, another spectrum analysis was completed. The data acquisition system is shown in Figure 6.20. The output waveform of SC amplifier was sampled by an A/D converter (AD1671) at the end of the valid phase $\phi 2$, and it was converted into 12-bit (parallel) digital data. Then the parallel digital data were converted to serial data and taken into a NEXT workstation for data acquisition. Finally, the FFT analysis was accomplished by using MATLAB.

First, a sinusoidal signal from the signal source Tektronix SG5010 was fed into the A/D converter and it was tested how much linearity can be obtained using the A/D converter. Its result is shown in Table 6-6.

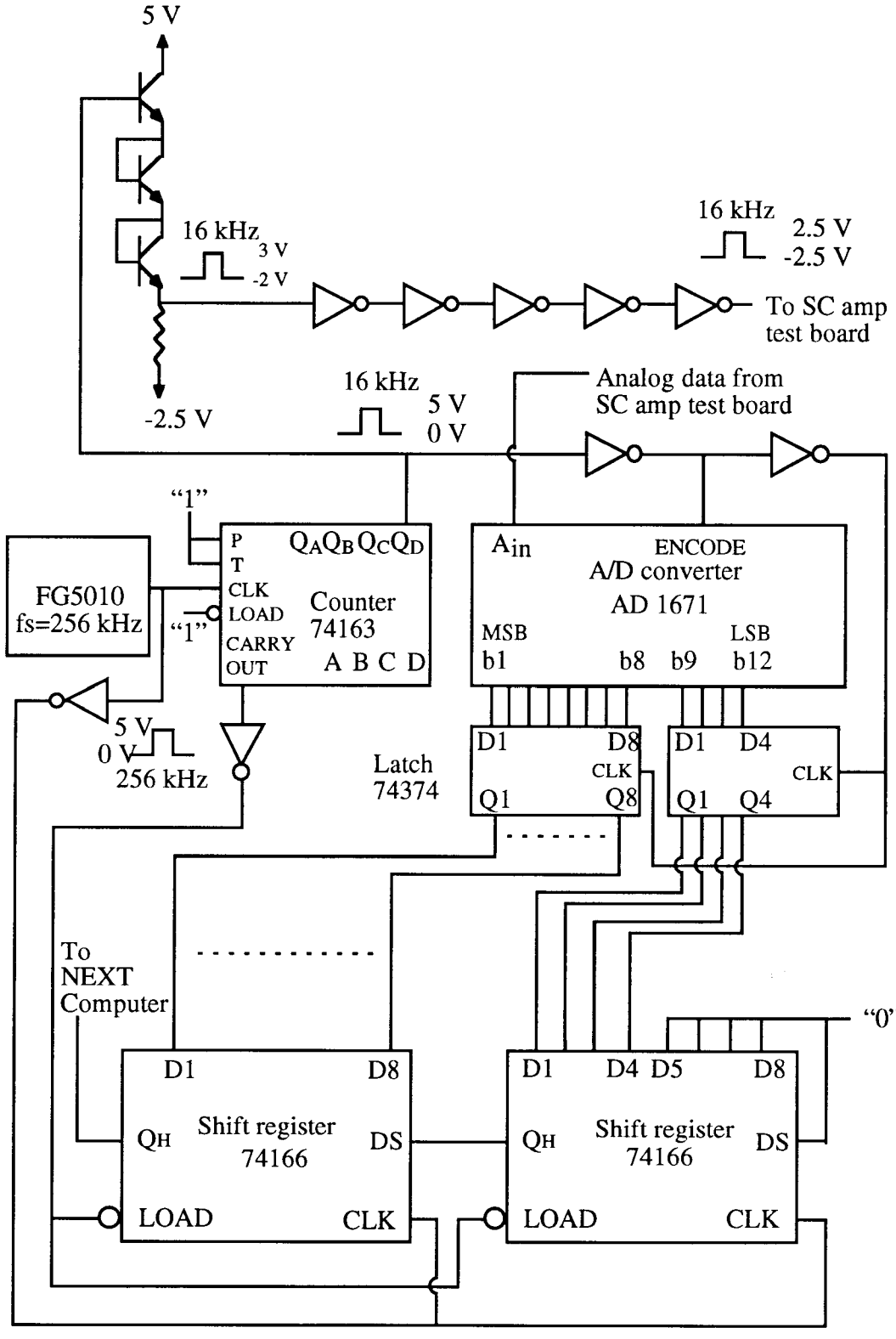


Figure 6.20 Data acquisition using an A/D converter

Then, FFT analyses of the SC amplifiers DP, SCOMP_1, SCOMP_2, and SB were performed. The output waveforms of the SC amplifiers are shown in Figure 6.21. In the inverting mode, the output still changes during the phase $\phi 2$, and hence clock jitter can cause distortion when it is sampled during $\phi 2$. By contrast, the phase $\phi 1$ is not valid but stable, hence the jitter effects can be avoided. Measurements in the inverting mode were completed using both phases: Table 6-7a shows the test results sampled at the end of $\phi 2$; Table 6-7b shows results sampled at the end of $\phi 1$. In the non-inverting mode, $\phi 2$ is the valid and stable phase as shown in Figure 6.21. Table 6-8 shows experimental results for outputs sampled at the end of $\phi 2$.

No big difference was found in these results compared with those obtained by the spectrum analyzer. Also, the results taken during $\phi 1$ were nearly the same as those taken during $\phi 2$.

From these experimental results, it is concluded that linearity of these SC amplifiers were limited not by the nonlinearity of MOSFET capacitors, but by other factors such as nonlinearity of the op-amp.

Table 6-6 Sinusoidal signal from Tektronix SG5010: the input signal frequency (f_{in}) was 1 kHz.

	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
Signal source	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
SG5010	-75 dB	-85 dB	70 dB	80 dB

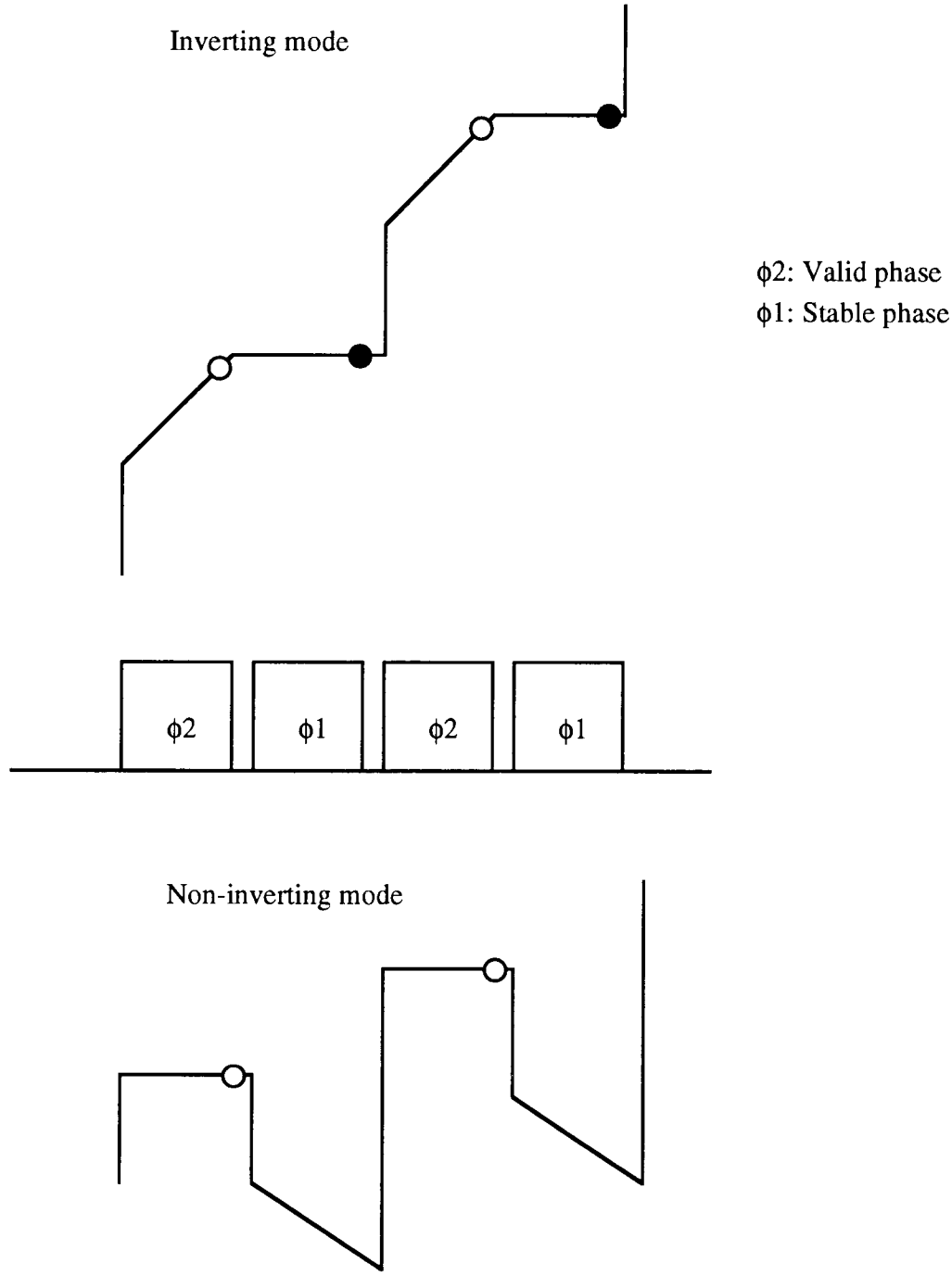


Figure 6.21 Output waveforms and timing of sampling time

Table 6-7 (a) Inverting mode sampled at the end of $\phi 2$; Input signal frequency (f_{in}): 1 kHz; clock frequency (f_S): 16 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-75 dB	-72 dB	70 dB	71 dB
SCOMP_1	-58 dB	-64 dB	55 dB	61 dB
SCOMP_2	-64 dB	-65 dB	62 dB	61 dB
SB	-65 dB	-59 dB	60 dB	58 dB

Table 6-7 (b) Inverting mode sampled at the end of $\phi 1$; Input signal frequency (f_{in}): 1 kHz; clock frequency (f_S): 16 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-66 dB	-70 dB	59 dB	67 dB
SCOMP_1	-68 dB	-58 dB	61 dB	57 dB
SCOMP_2	-64 dB	-67 dB	60 dB	66 dB
SB	-65 dB	-56 dB	60 dB	55 dB

Table 6-8 Non-inverting mode sampled at the end of $\phi 2$; Input signal frequency (f_{in}): 1 kHz; clock frequency (f_S): 16 kHz

SC amplifier code name	Largest harmonic component		S/THD ratio	
	Differential output signal swing		Differential output signal swing	
	2 Vp-p	4 Vp-p	2 Vp-p	4 Vp-p
DP	-66 dB	-66 dB	62 dB	66 dB
SCOMP_2	-66 dB	-65 dB	62 dB	62 dB

6.4.11 Noise

1/f noise is a major factor which limits the S/N ratio in SC circuits. As already described in Section 2.3.2, 1/f noise is caused by interface-trapped charges (surface state charges) due to the interruption of the periodic lattice structure at the surface of the silicon [5]. In a MOSFET capacitor, the periodic lattice structure is interrupted between the bottom silicon bulk layer (single crystalline) and gate-oxide layer (amorphous), hence interface-trapped charges can cause 1/f noise. In a double-poly capacitor, interface-trapped charges are also generated because phases changes between the bottom poly layer (poly-crystalline) and insulated oxide layer (amorphous). Therefore, the 1/f noise level is about the same for an SC amplifier using double-poly capacitors as for the one using MOSFET capacitors.

In experimental results, no difference in noise level was observed between double-poly capacitors and MOSFET capacitors, and it was shown that the 1/f noise of MOSFET capacitor are at the same level as for double-poly capacitors.

Chapter 7

OPERATIONAL AMPLIFIERS IN DIGITAL CMOS TECHNOLOGY

In this chapter, operational amplifier (op-amp) configurations for realization in a digital CMOS process are discussed. First, the earlier work will be summarized. Then, a folded-cascode op-amp used in our chips will be described. Finally, a novel two-stage op-amp using MOSFET capacitors will be proposed.

7.1 Earlier Work

In a digital CMOS process, the op-amp also has to be implemented without the second poly layer. A digital-compatible op-amp was proposed in ref. [34]. As shown in Figure 7.1, the authors used a set of PMOSFET and NMOSFET capacitors in the frequency compensation branches of a class-AB op-amp so that their nonlinearities could be compensated. However, the threshold voltage of an NMOSFET capacitor in this circuit is increased because of the body effect, and that results in a C-V curve shift. Each time the output voltage changes, the threshold voltage of the NMOSFET capacitor changes as well as its C-V curve. Therefore, the nonlinearity of the PMOSFET and NMOSFET capacitors in this configuration cannot be fully cancelled. The experimental S/THD was only 55 to 65 dB for a 10 kHz signal.

7.2 Folded-Cascode Op-Amp

In our fabricated chips, a folded-cascode op-amp was used. As shown in Chapter 6, the MOSFET capacitors in the CMFB circuitry generate distortion when the output signal has a large swing and they operate out of their accumulation region.

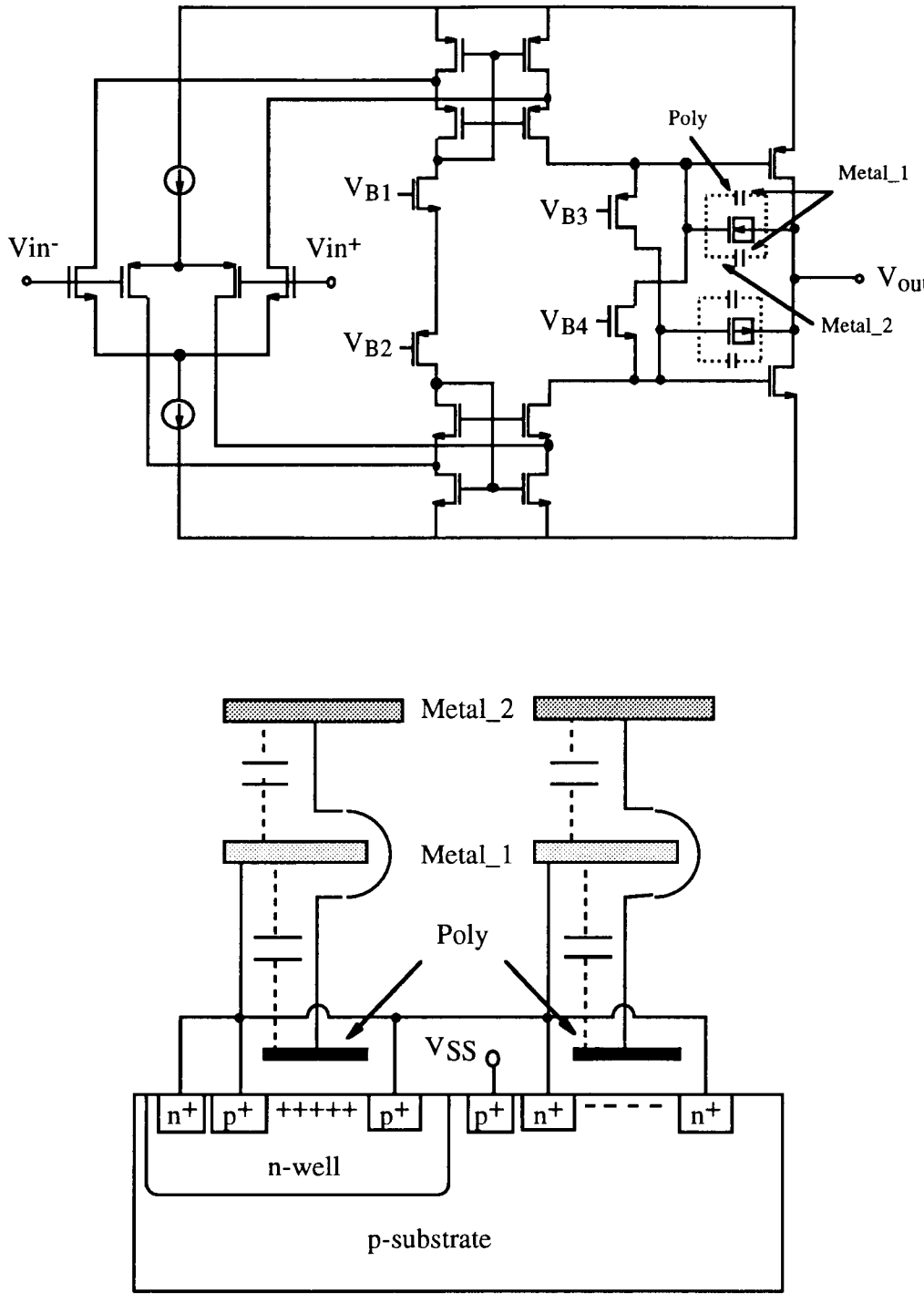


Figure 7.1 A digital-process compatible op-amp [34]: (a) whole op-amp schematic; (b) practical implementation of Miller compensation by MOSFET capacitors.

Figure 7.2 shows a post-layout simulation of the output spectrum of the MOSFET-only SC amplifier using the folded-cascode op-amp of Figure 6.4. In this op-amp, the CMFB was realized by MOSFET capacitors. For a single-ended output, large-order even harmonic components are observed (Figure 7.2a). However, since it is a fully differential circuit, these harmonic components are canceled at the differential output (Figure 7.2b).

By applying series compensation to the CMFB, the linearity at a single output can be improved. Figures 7.2c and d show a post-layout simulation of the SC amplifier using the folded-cascode op-amp of Figure 7.3. For single-ended output, the linearity is improved compared to that of Figure 7.2a as shown in Figure 7.2c. However, for the differential output (Figure 7.2d), the S/THD ratio was the same as in Figure 7.2b under ideal symmetry conditions.

Figures 7.2e and f show the post-layout simulation of the SC amplifier using the folded-cascode op-amp of Figure 6.3. Here, the CMFB was realized by double-poly capacitors. As shown in Figures 7.2e and f, the linearity was as same as that shown in Figures 7.2c and d even if linear capacitors are used. By contrast, when the op-amp is replaced by an ideal op-amp, the linearity is much improved. Therefore, it is likely that the linearity of the SC amplifier is limited by the relatively small linear output range of the folded-cascode op-amp due to the cascoded output transistors.

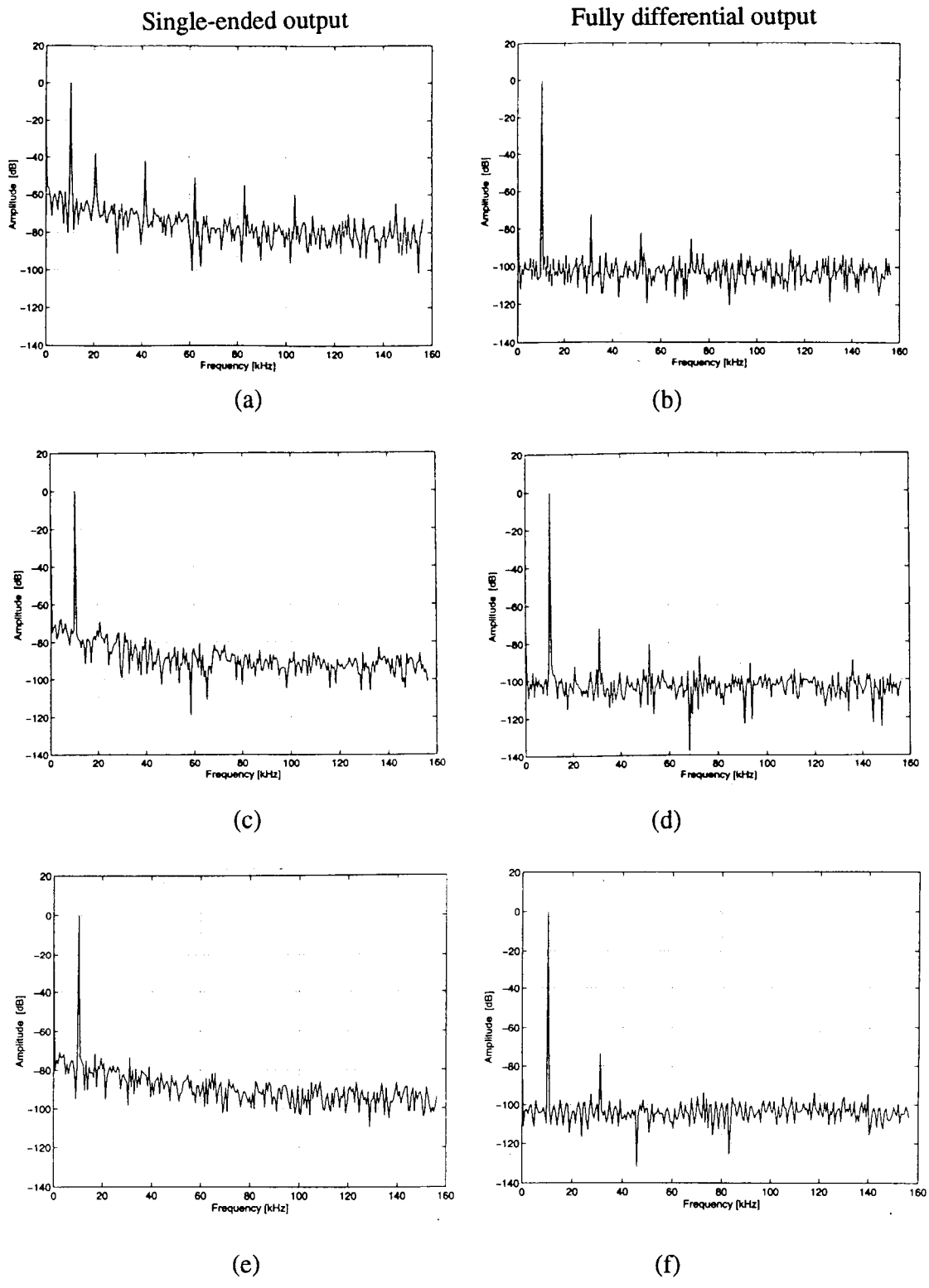


Figure 7.2 HSPICE simulation results of the SC amplifier: (a)(b) op-amp of Figure 6.4; (c)(d) op-amp of Figure 7.3; (e)(f) op-amp of Figure 6.3; (a)(c)(e) single output; (b)(d)(f) differential output.

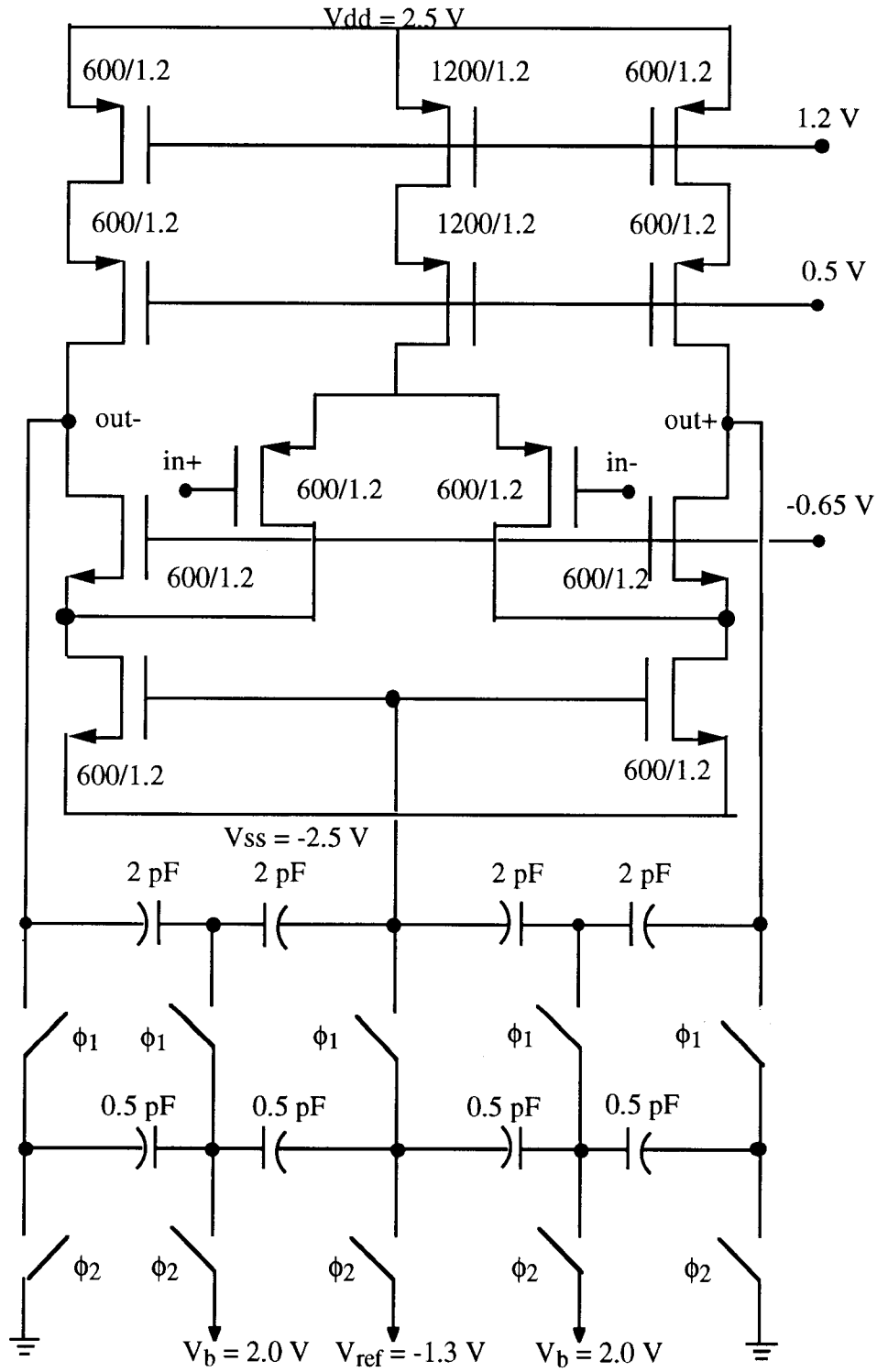


Figure 7.3 Folded-cascode op-amp using MOSFET capacitors with series compensation

7.3 Two-Stage Op-Amp

It was found that the folded-cascode op-amp used in our past chips had a relatively narrow linear output range. To widen the linear output range of the op-amp, a two-stage op-amp with a class-A output stage was designed. The two-stage op-amp requires frequency compensation to avoid oscillation, and since we are attempting to fabricate our chips in a digital CMOS process, the capacitors used in the frequency compensation also had to be MOSFET capacitors, rather than double-poly ones.

Figure 7.4 shows a two-stage op-amp with the Miller compensation capacitor C_c. In this op-amp, the dominant pole, the non-dominant pole and the zero are given by [35]

$$p_1 = -\frac{1}{g_{mII} R_I R_{II} C_c}$$

$$p_2 = -\frac{g_{mII}}{C_{II}} \qquad (7\text{-}1)$$

$$z = \frac{g_{mII}}{C_c}$$

respectively, where g_{mII} is the transconductance of the second stage, and R_I (R_{II}) is the output resistance of the first (second) stage. Notice that the zero is in the right-half-plane, and hence it degrades the phase margin of the op-amp. (In a bipolar op-amp, the transconductance of the transistor is large enough to place the zero at a very high frequency in the right-half-plane so that the zero does not affect the phase margin. However, in a CMOS op-amp, the transconductance of the transistor is much smaller, hence the phase margin may be degraded. Therefore, the right-half-plane zero has to be shifted to a very high frequency or to the left half plane.) In addition, if the capacitor is realized by a MOSFET capacitor, it will operate out of the accumulation region when the output swing becomes large.

Two frequency compensation methods are widely used to move the right-half-plane zero to the left half plane or remove it altogether. One is to use both a resistor and a capacitor in the feedback branch, as illustrated in Figure 7.5.

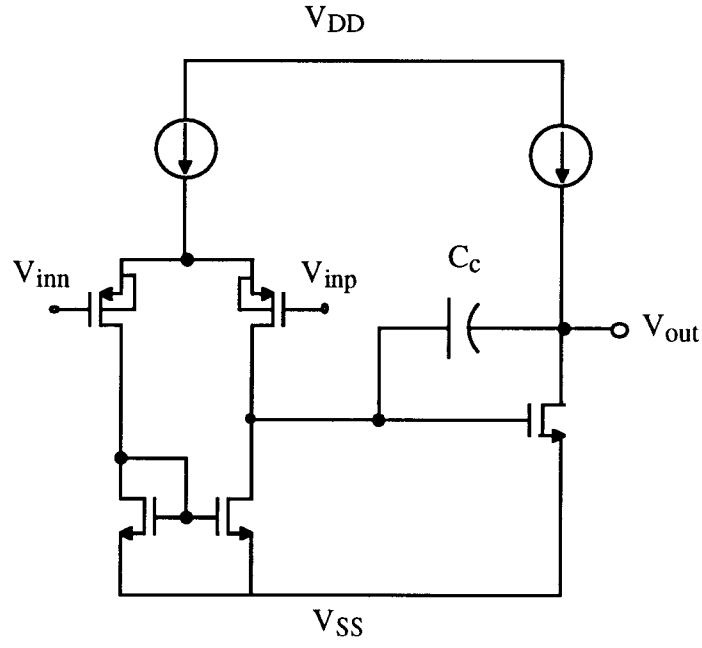


Figure 7.4 Op-amp compensation (1)

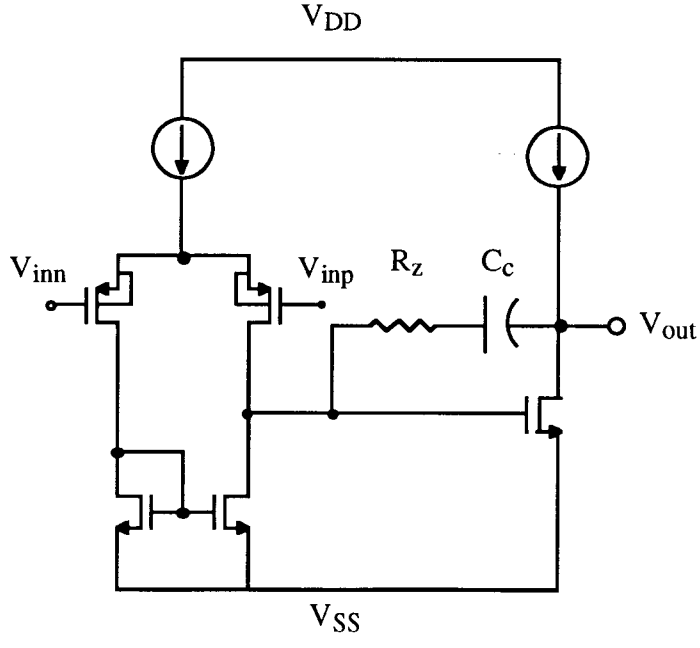


Figure 7.5 Op-amp compensation (2)

The dominant and non-dominant poles are given by (7-1), and the zero and an additional pole are given by [35]

$$z = \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_Z\right)}$$
$$p_3 = -\frac{1}{R_Z C_I} \qquad (7\text{-}2)$$

where C_I is the capacitance to ground seen from the output of the first stage. By controlling R_Z, the zero z and pole p_2 can be made to cancel each other.

The other frequency compensation method is to use a buffer and a capacitor as shown in Figure 7.6. Again, the dominant and non-dominant poles are given by (7-1), and the zero and another pole is given by [35]

$$z = -\frac{1}{R_o C_c}$$
$$p_3 = -\frac{1}{R_o C_I} \qquad (7\text{-}3)$$

where R_o is the output resistance of the buffer amplifier. This method is convenient for a digital CMOS process because the unity-gain buffer (source follower) provides a dc bias voltage for the MOSFET capacitor, and thus keeps it in its accumulation region. The practical realization of this compensation is illustrated in Figure 7.7.

A fully differential configuration of this op-amp is shown in Figure 7.8 [36]. Because the output impedance is relatively small in the two-stage op-amp, resistors can be used for the CMFB. Although this op-amp was fabricated in such a way that the CMFB resistors were connected to the output nodes Voutp and Voutn as shown in Figure 7.8, these resistors could have been connected to the nodes Voutp' and Voutn' because the impedances of these nodes are further smaller than those of Voutp and Voutn.

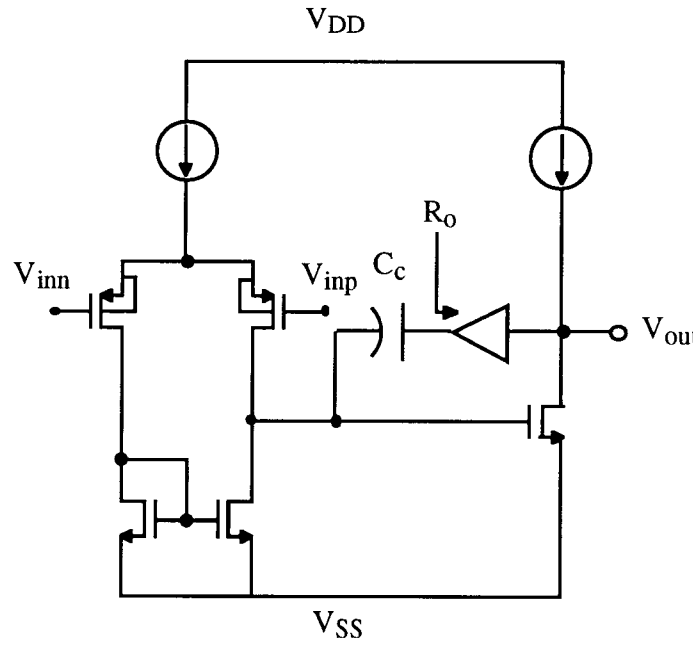


Figure 7.6 Op-amp compensation (3).

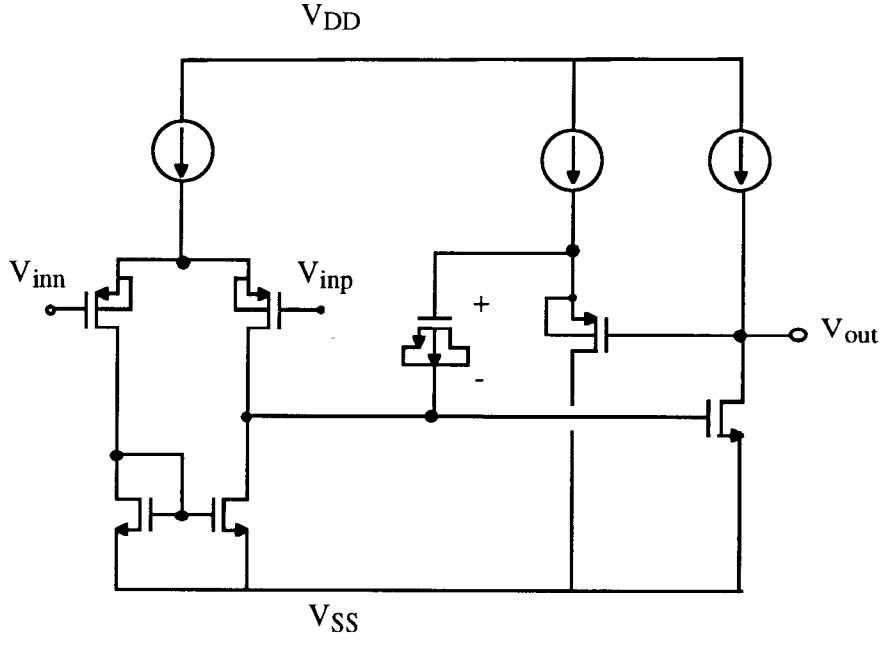


Figure 7.7 Practical realization of Figure 7.6.

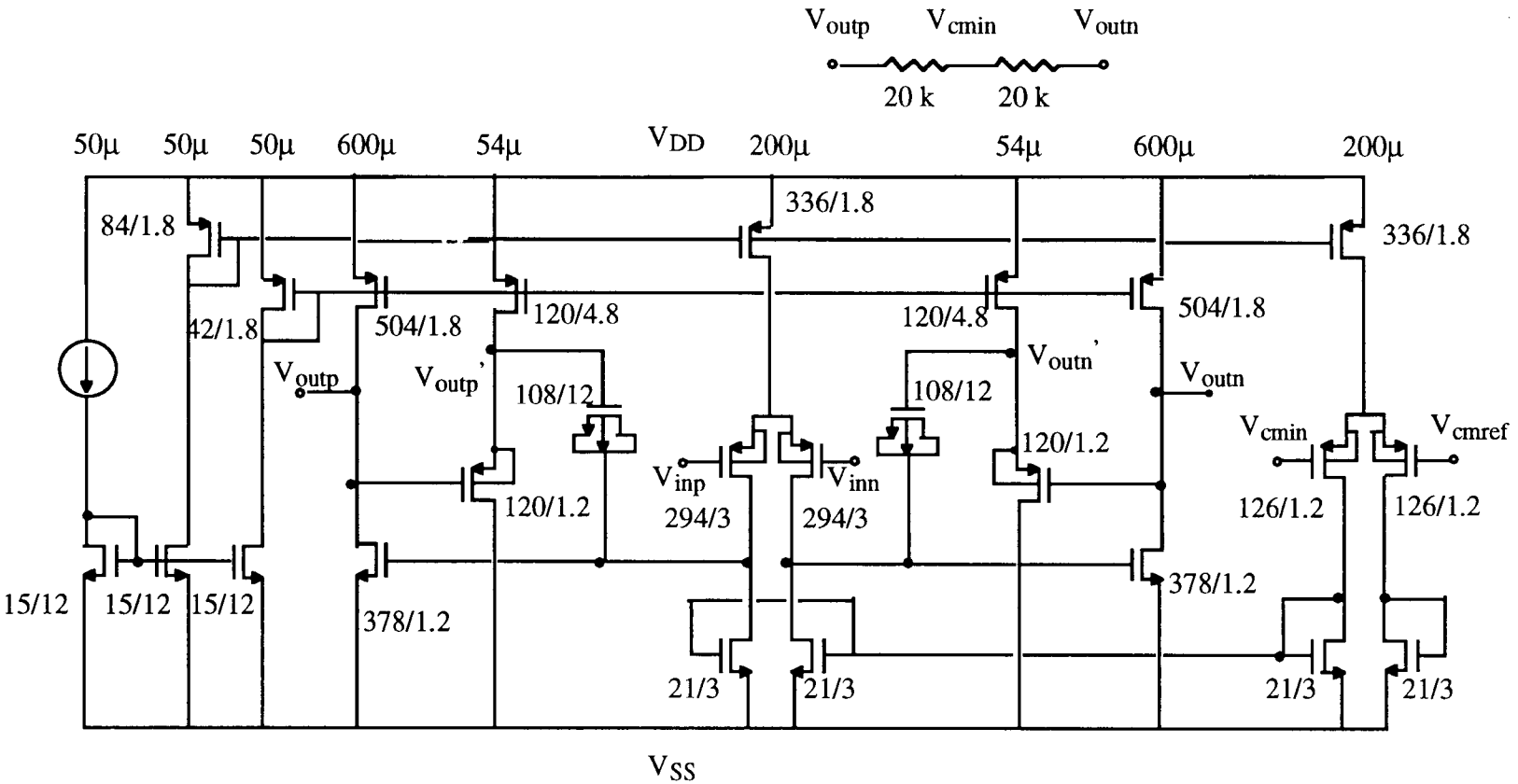


Figure 7.8 Fully differential two-stage op-amp using MOSFET capacitors

Table 7-1 summarizes the characteristics of the op-amp simulated using HSPICE. The Bode plot is shown in Figure 7.9. In this Figure, two curves are shown for the positive and negative output signals.

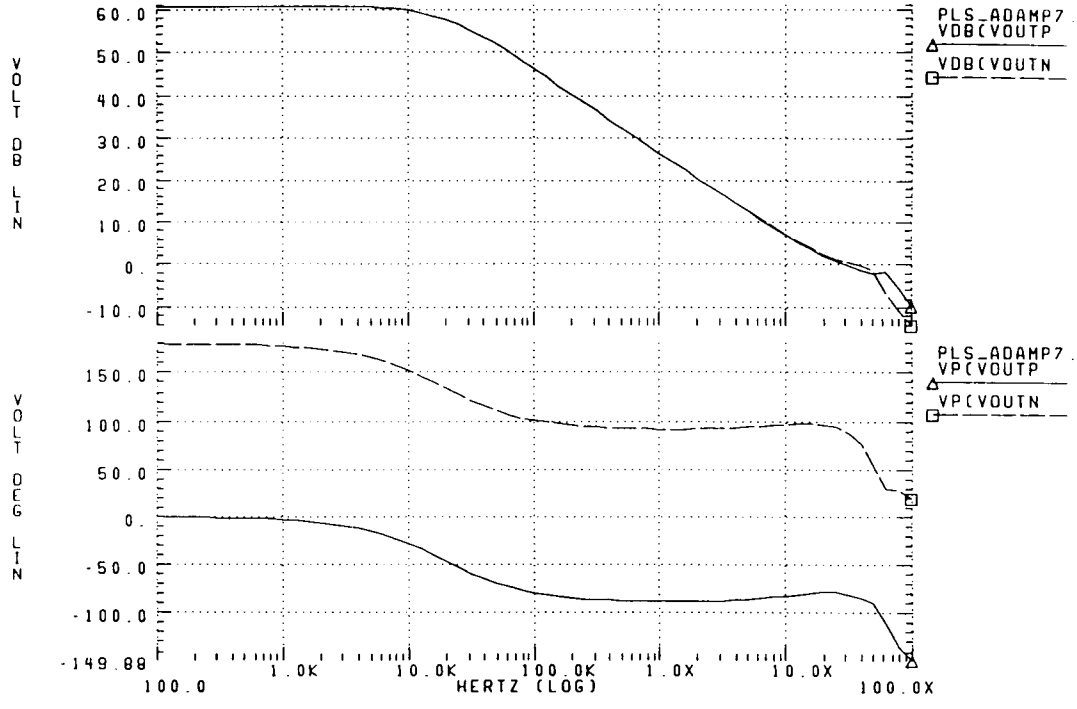


Figure 7.9 Bode plot of the two-stage op-amp

Table 7-1 Characteristics of the op-amps

	Op-amp of Figure 7.4 using linear capacitors	Op-amp of Figure 7.8 using MOSFET capacitors
DC gain [dB]	67	67
Gain-bandwidth [MHz]	20	28
Phase margin [deg]	73	99

7.4 Simulation Results

To compare the op-amps described above, the SC amplifier of Figure 4.8 incorporating these op-amps was simulated using HSPICE. The simulation results are shown in Table 7-2 and Figure 7.10.

Table 7-2 Comparison of the SC amplifier performances with various op-amps

Op-amp	Peak harmonic component below the signal [dB]	Signal/THD [dB]
(a) Macro-model op-amp (ideal op-amp)	-94	88
(b) Folded-cascode op-amp; CMFB using linear capacitors	-71	68
(c) Two-stage op-amp; compensation using linear capacitors (Figure 7.4)	-89	85
(d) Two-stage op-amp; compensation using MOSFET capacitors and source followers (Figure 7.8)	-89	85

Clearly the use of the two-stage op-amp with MOSFET capacitors improves the linearity of the series-compensated SC amplifier by more than 15 dB compared to the folded-cascode op-amp which was employed in the previous chips.

7.5 Layout and Post-Layout Simulation

An SC amplifier with series compensation was laid out using the two-stage op-amp, and the chip is in the process of fabrication. The layout plot of the two-stage op-amp is shown in Figure 7.11.

Post-layout simulations by HSPICE show that an S/THD of 91 dB can be obtained for the predictive SC amplifier using series compensation.

Experimental results will be described in Section 8.4.1.

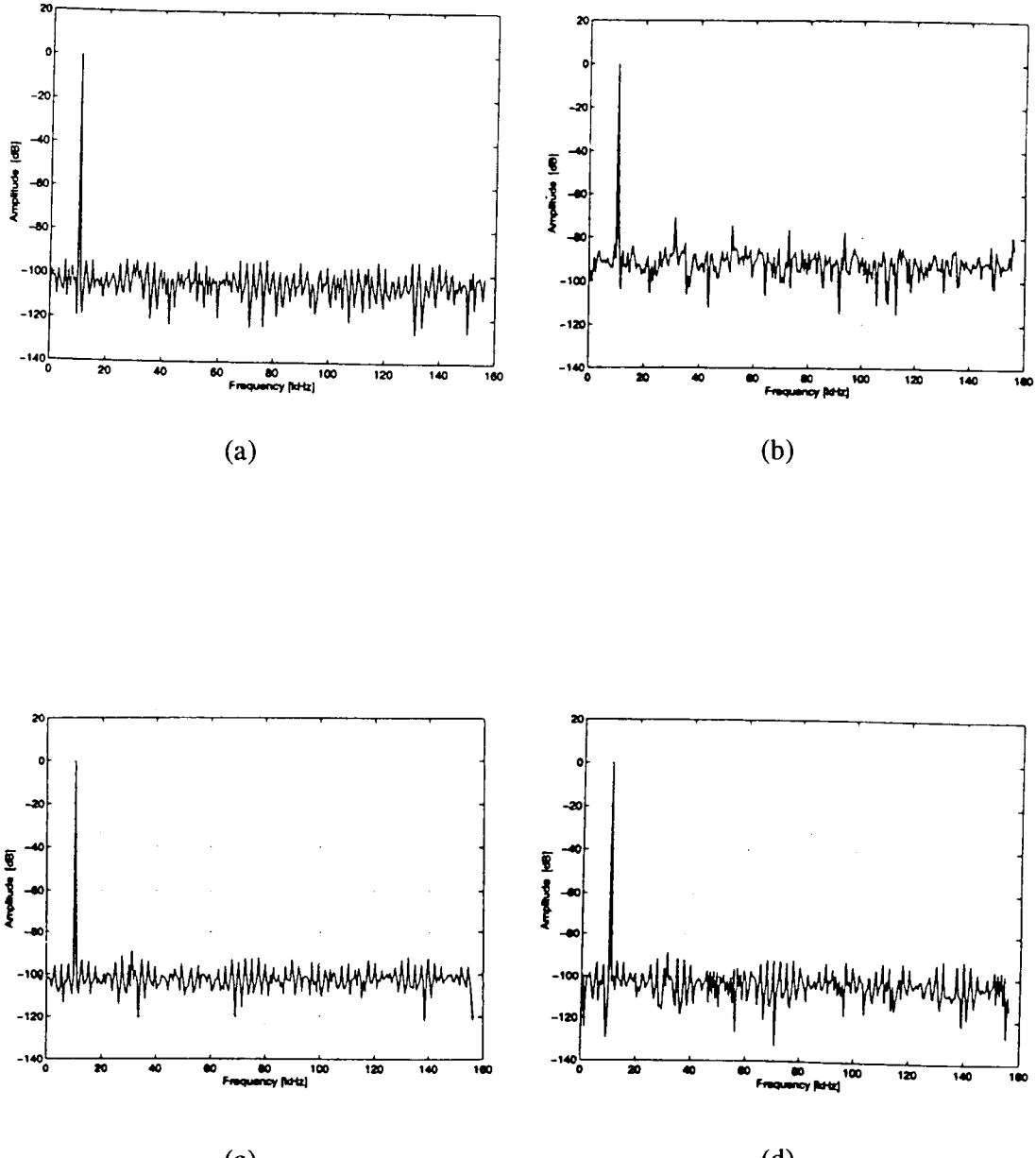


Figure 7.10 HSPICE simulations of the SC amplifier by various kinds of op-amp: (a) macro model; (b) folded-cascode op-amp; (c) two-stage op-amp with linear capacitors; (d) two-stage op-amp using MOSFET capacitors

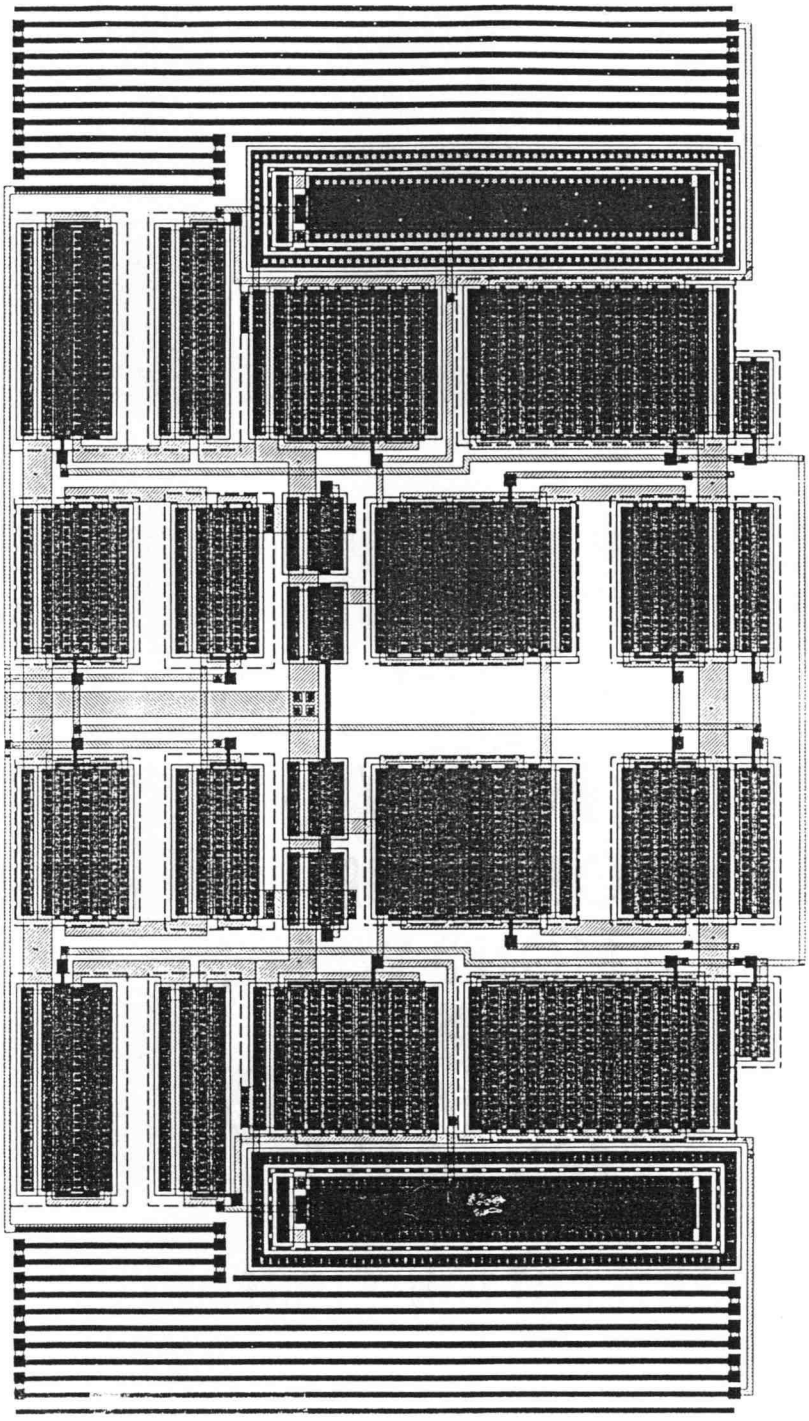


Figure 7.11 Layout of the two-stage op-amp

Chapter 8

DIGITALLY CONTROLLED GAIN/LOSS CIRCUIT

In this chapter, the design of a MOSFET-only digitally controlled gain/loss circuit will be described. First, the research background will be summarized. Then, the design details of the MOSFET-only digitally controlled gain/loss circuit will be presented. Finally, simulation and experimental results will be provided.

8.1 Research Background

Digitally controlled gain/loss circuits are useful in telecommunication and other applications. For example, when the amplitude of a signal is too large in a telecommunication channel, the amplitude has to be reduced by an attenuator. By contrast, the input signal to an A/D converter may need to be amplified to increase the dynamic range. The gain/loss circuit functions as a multiplying D/A converter (MDAC) by generating the product of the analog input signal and the digital signal [17]. If the input signal is a constant reference voltage, the circuit operates as a D/A converter.

Baldwin and McCreary used precision capacitors for their digitally controlled analog attenuator [37]. In Figure 8.1, $2^{k-1}C$ denotes the feedback capacitor, and all other capacitors can be switched either to the input or to the output node depending on the digital word. The loss of this circuit is given by

$$\frac{V_{out}}{V_{in}} = \frac{N}{2^k - N} \qquad (8\text{-}1)$$

where N=1, 2, ..., 2^{k-1}. Therefore, e.g. for k=4, its loss can be 1/15, 2/14, 3/13, ..., 1.

Babanezhad and Gregorian utilized resistors for their programmable gain/loss circuit [38] as shown in Figure 8.2. Gain or loss can be selected by a digital word, and the magnitude of gain (or loss) is determined by other digital words controlling a multiplexer.

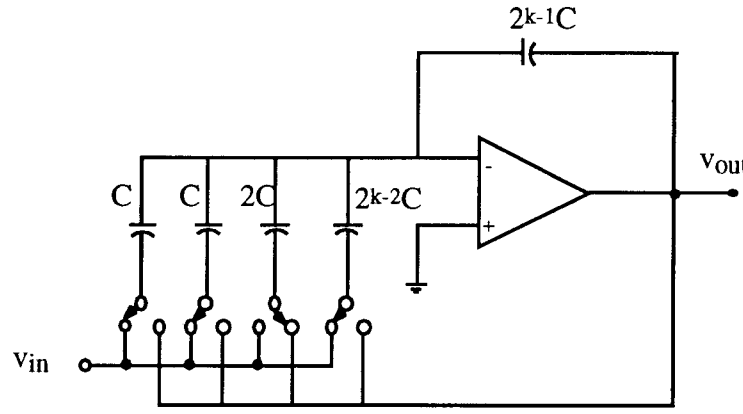


Figure 8.1 Digitally controlled attenuator [37]

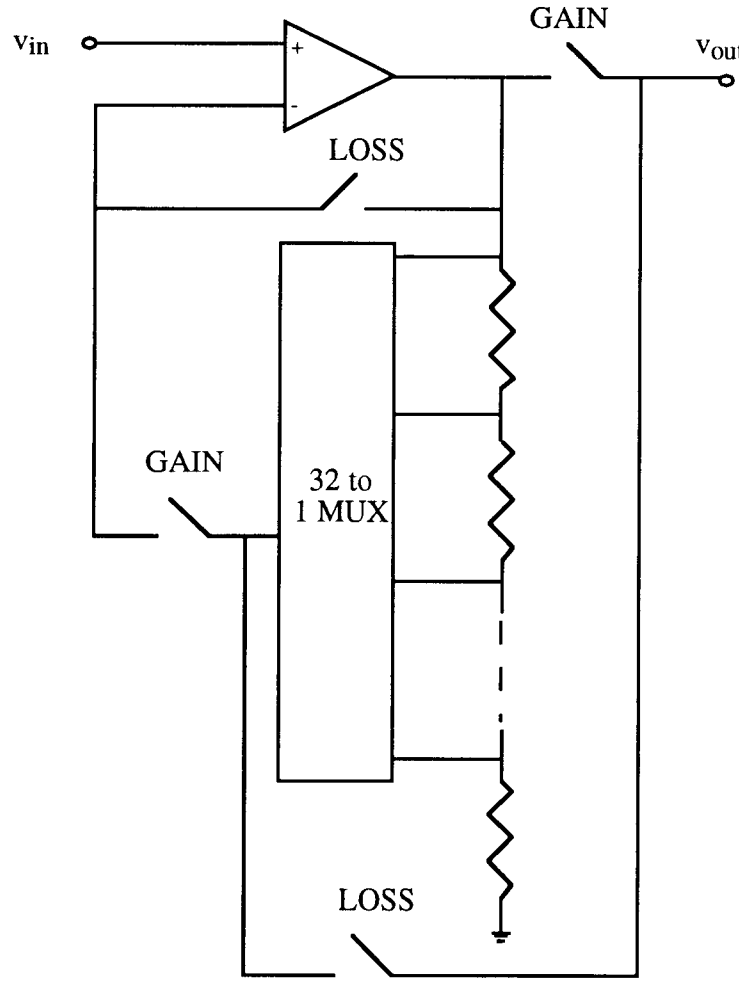


Figure 8.2 Digitally controlled gain/loss circuit [38]

8.2 Circuit Design

We have designed a MOSFET-only 4-bit digitally controlled gain/loss circuit [36]. This is useful not only for the applications described above, but also for verifying that series compensation is effective for large signal swings at both input and output nodes.

For simple explanation, Figure 8.3a shows a one-bit gain/loss circuit. When the GAIN option is selected, this circuit works as an amplifier with a gain of 8 as shown in Figure 8.3b. If LOSS is chosen, the circuit of Figure 8.3a operates as an attenuator with a loss of 1/8 as illustrated in Figure 8.3c. To utilize MOSFET capacitors in the circuit, all capacitors in the signal paths are series compensated.

Figure 8.4 shows the details of a MOSFET-only digitally controlled gain/loss circuit, and Figure 8.5 illustrates its control circuits. In the circuit of Figure 8.4, the binary signal d3 is the MSB, and d0 is the LSB of the control input word. Digital signal G determines whether the circuit works as an amplifier or as an attenuator: when G is 1, the circuit is an amplifier whose gain varies from 1 to 15 with a step of 1, while for G=0, it is an attenuator with a loss of 1/15, 1/14, 1/13, ..., 1. Since both input and output swings can be large, CMOS transmission gates are used in all switches connected to the input and output nodes.

This gain/loss circuit was laid out using the two-stage op-amp described in Section 7.3. For comparison, an SC amplifier using double-poly capacitors and the two-stage op-amp was also laid out. Figure 8.6 shows the layout and floor plan of this circuit.

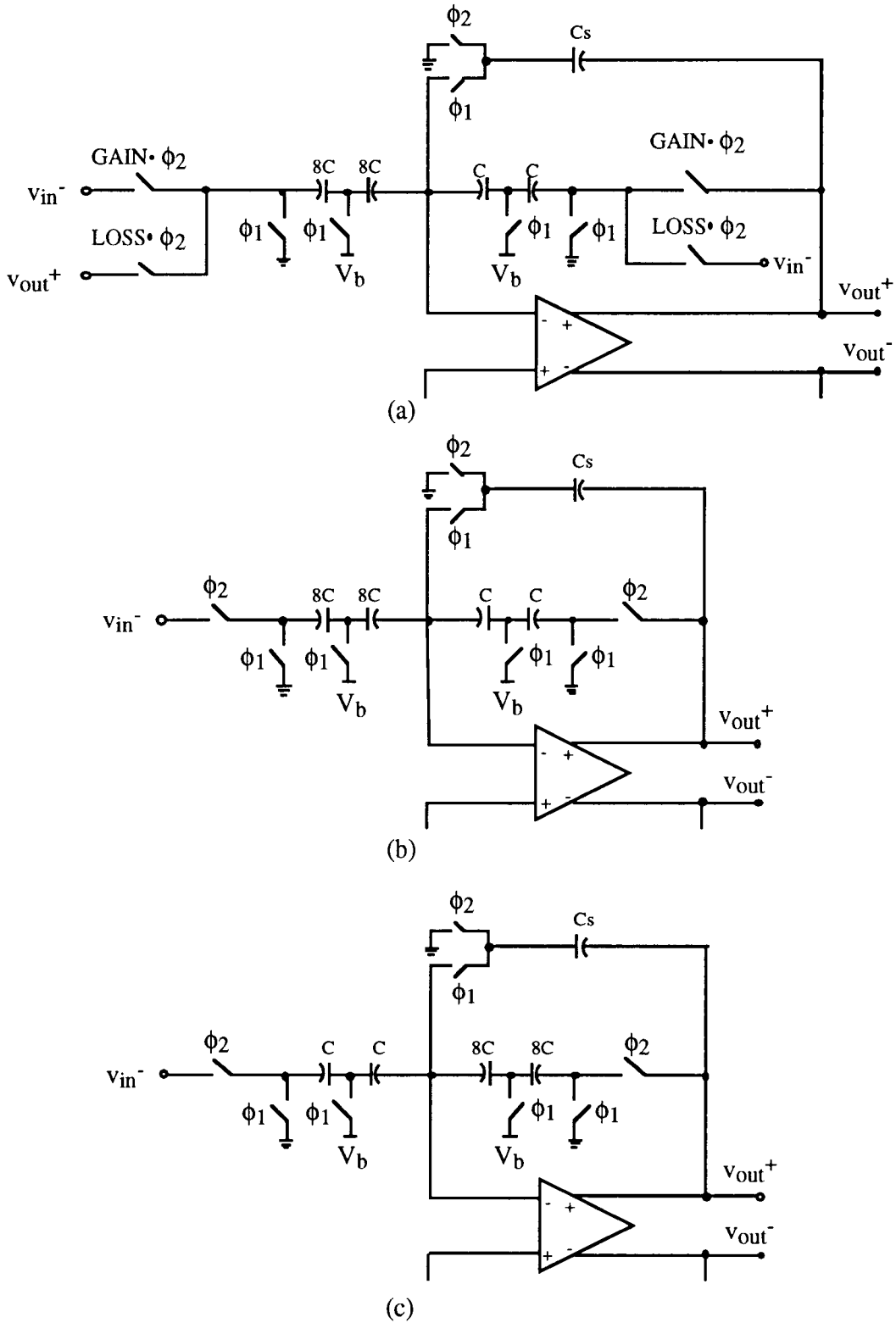


Figure 8.3 (a) One-bit gain/loss stage; (b) amplifier; (c) attenuator.

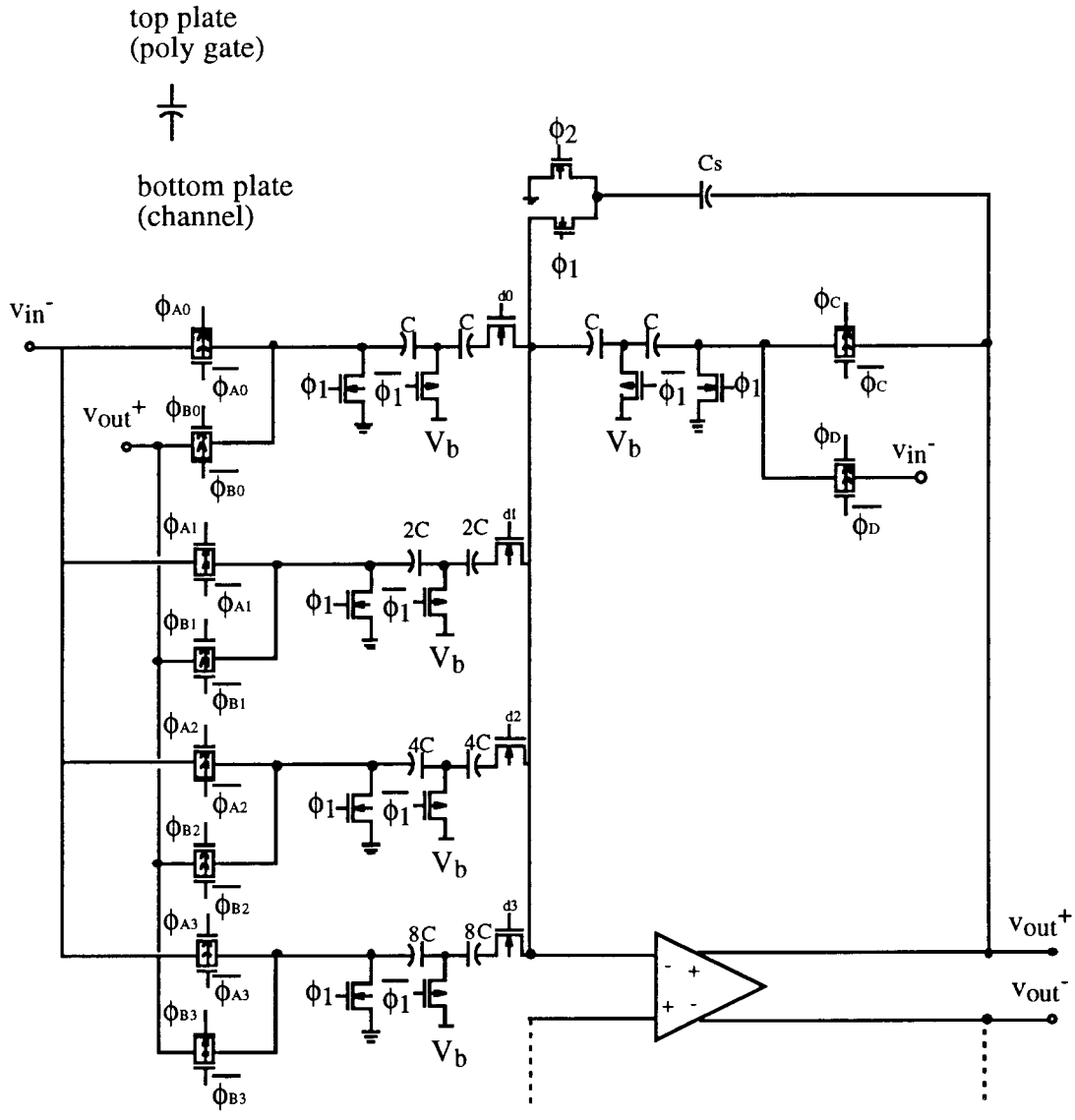


Figure 8.4 MOSFET-only digitally controlled gain/loss circuit

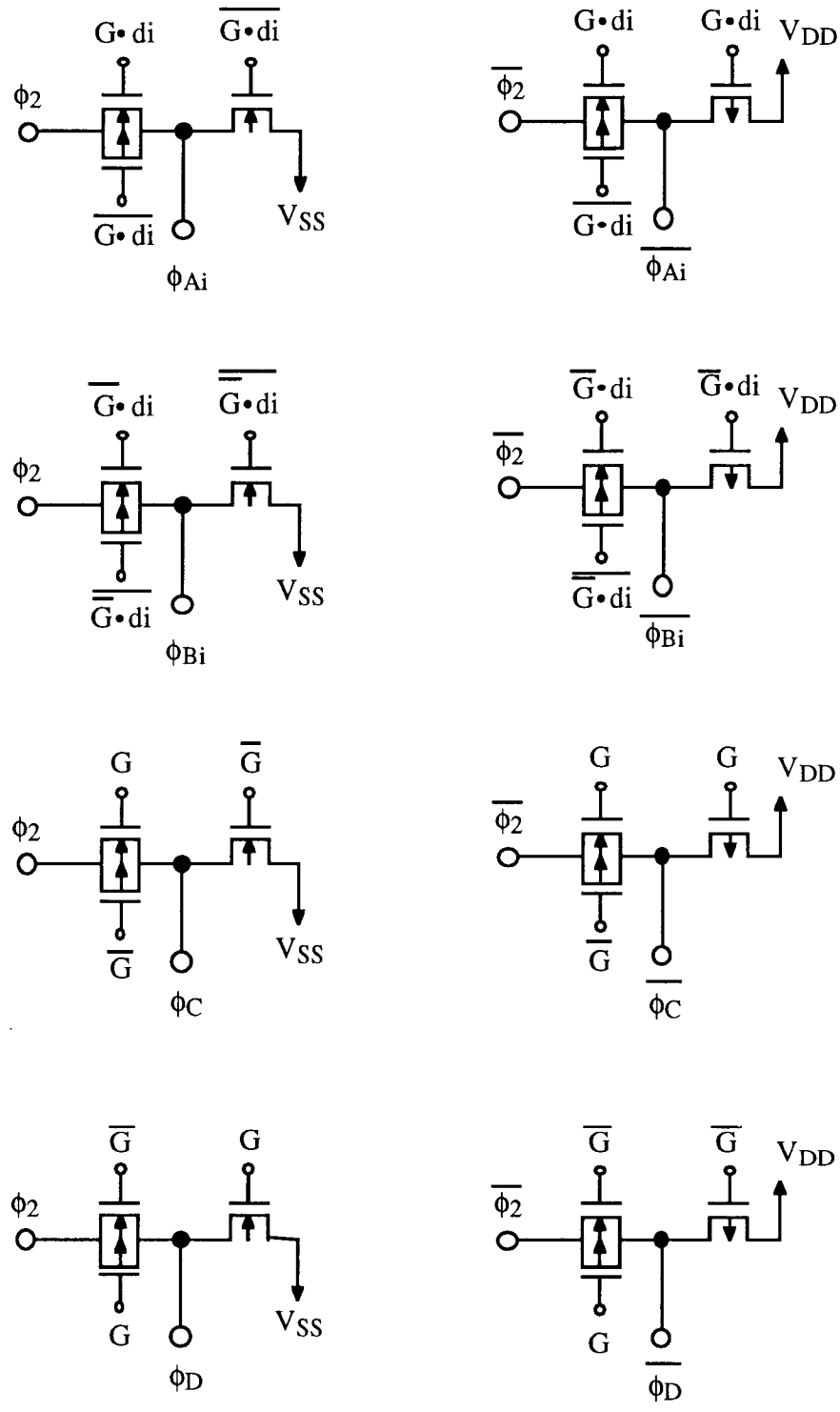


Figure 8.5 Control circuit

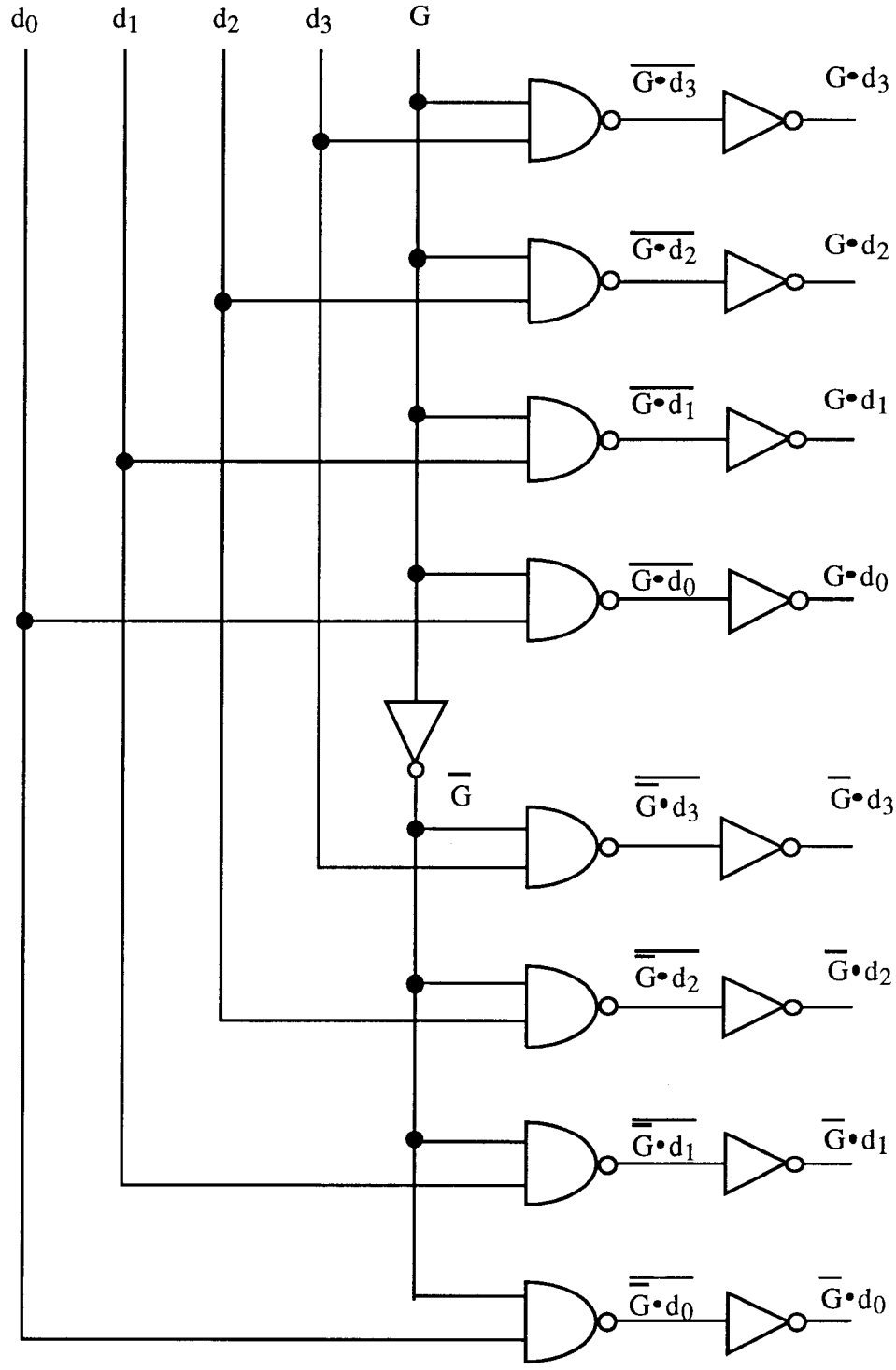
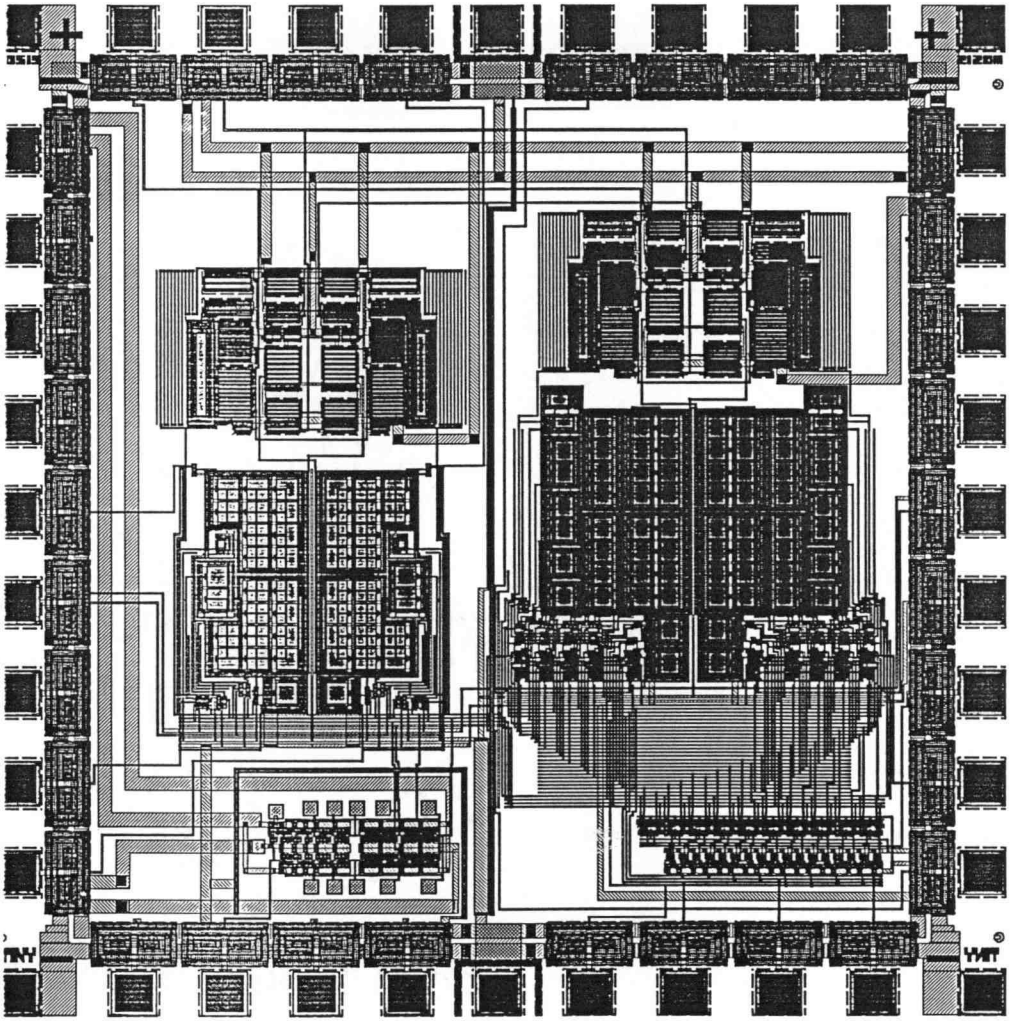
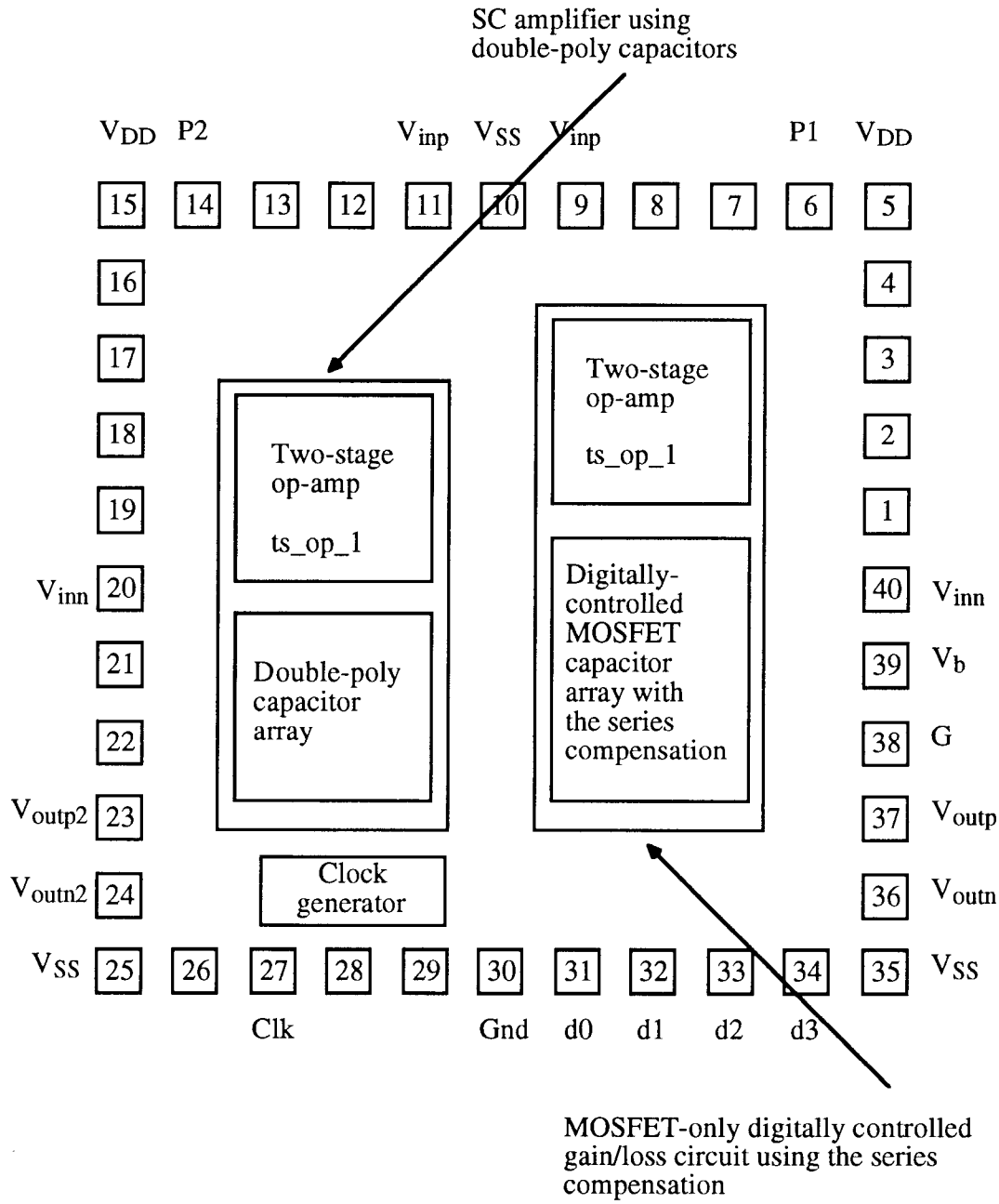


Figure 8.5 continued



(a)

Figure 8.6 Digitallly controlled gain/loss circuit: (a) layout; (b) floor plan.

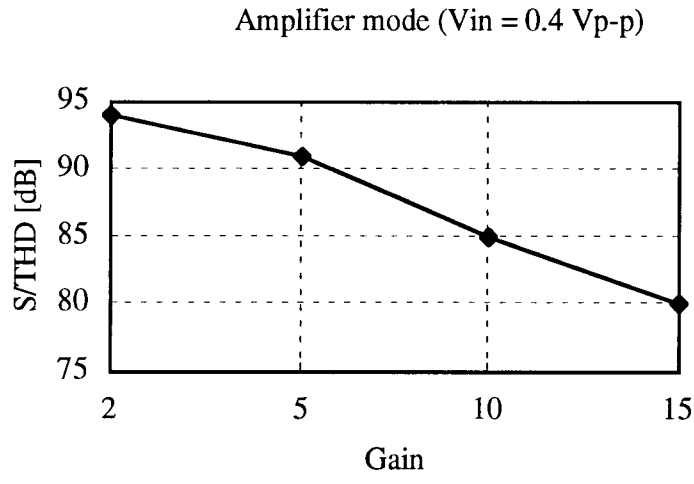


(b)

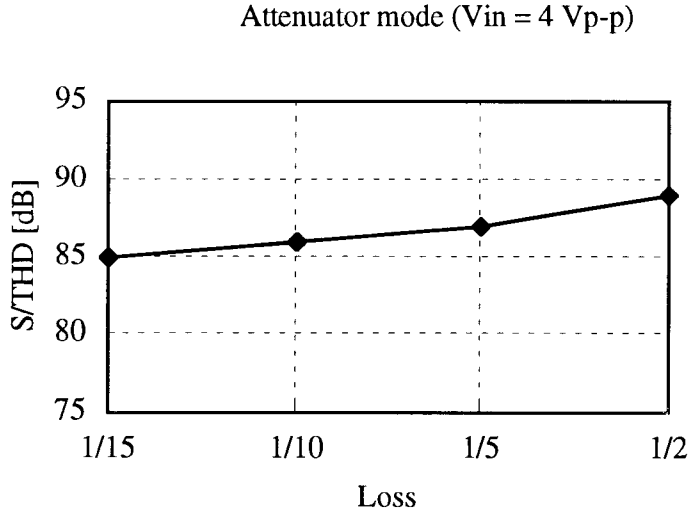
Figure 8.6 continued.

8.3 Simulation Results

Figure 8.7 shows the S/THD ratios for various gains and losses obtained by post-layout simulations using HSPICE. In this figure, the amplitude of the fully differential input signal was 0.4 Vp-p for the amplifier mode, and it was 4 Vp-p for the attenuator mode. In Figure 8.7a, the S/THD ratio decreases as the gain increases. When the gain increases, so does the output signal level. However, the increase of the voltage across the capacitor in the feedback path induces a distortion because the nonlinear operating range of the MOSFET capacitor widens. As the gain increases, the increase of distortion is faster than that of signal, hence the S/THD ratio decreases. On the other hand, in Figure 8.7b, the S/THD ratio increases slightly as the loss increases. In this attenuator configuration, the amplitude of the input signal is much larger than the output swing, and hence the nonlinearity caused by the input capacitors is the dominant factor for generating distortion rather than the nonlinearity caused by the feedback capacitors. The increase of the output signal is larger than that of the distortion; therefore, as the amplitude of the output signal increases, the S/THD ratio also increases.



(a)



(b)

Figure 8.7 Post-layout simulation results by HSPICE
(a) S/THD vs. gain; (b) S/THD vs. loss.

8.4 Experimental Results

The SC amplifier using double-poly capacitors and the MOSFET-only gain/loss circuit was fabricated in the Orbit 1.2 μm CMOS process. Figure 8.8 shows the die photo of this chip. In the following experimental results, the signal source HP8903A and the spectrum analyzer HP4195A were used. The test circuit and other experimental conditions were similar to those described in Chapter 6.

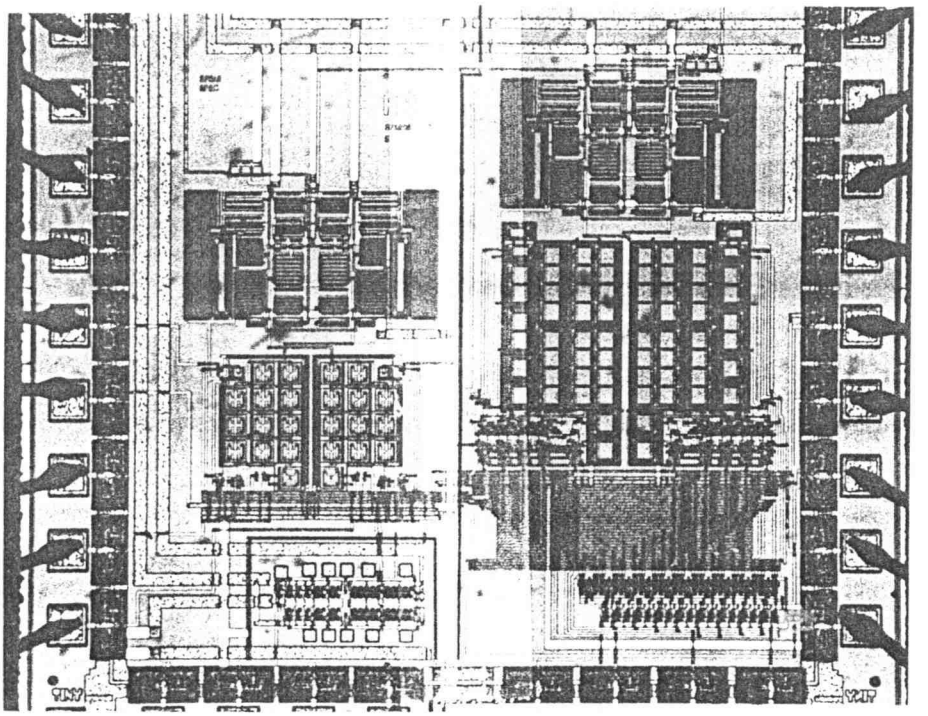
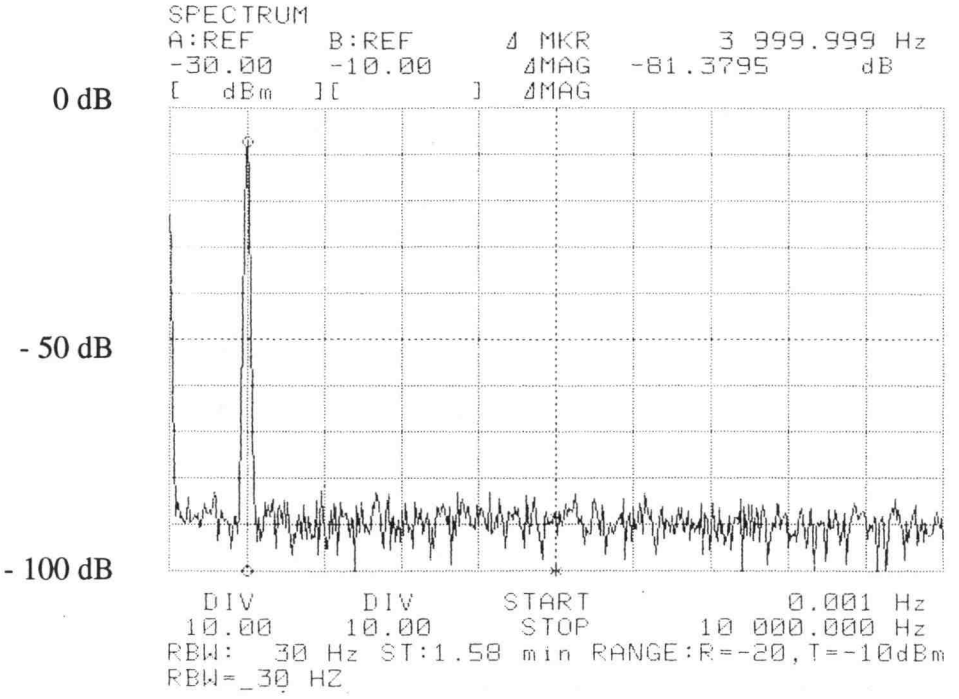


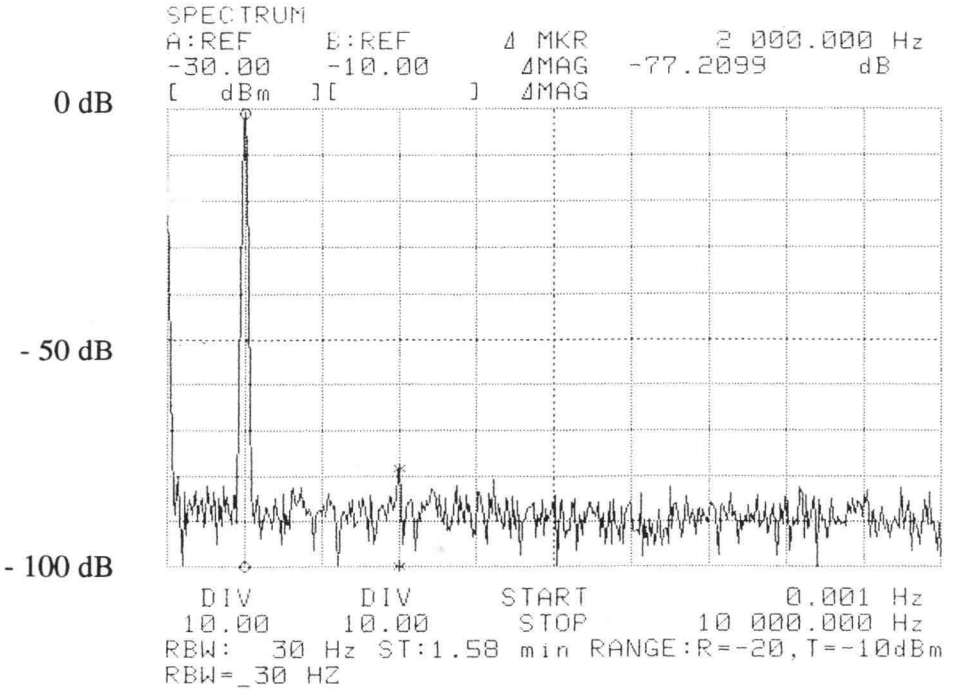
Figure 8.8 Die photo of the digitally-controlled gain/loss circuit.

8.4.1 SC Amplifier Using Double-Poly Capacitors

Figure 8.9a shows an output spectrum of the SC amplifier using double-poly capacitors for a fully differential output of 2 Vp-p. The input signal was a 1 kHz sinewave



(a)



(b)

Figure 8.9 The measured output spectrum of the SC amplifier using double-poly capacitors: a) Vout = 2 Vp-p; b) Vout = 4 Vp-p.

and the clock frequency was 16 kHz. The largest harmonic component was -81 dB below the fundamental signal, almost hidden in the noise level, and a S/THD ratio of 76 dB was obtained. For a 4 Vp-p output swing, the third harmonic component was -77 dB below the signal, and the S/THD was 76 dB (Figure 8.9b). For a 6 Vp-p output swing, the S/THD ratio decreased to 68 dB. It is likely that the distortion was caused by the nonlinearity of the op-amp. However, compared to the folded-cascode op-amp used in previous chips, this two-stage op-amp has a better linearity. For example, in Sec. 6.4.6, the SC amplifier with double-poly capacitor had a S/THD ratio of 69 dB for the output of 4 Vp-p. Hence, in this case, the two-stage op-amp contributed 7 dB improvement in linearity over the folded-cascode op-amp.

8.4.2 MOSFET-Only Gain/Loss Circuit (Amplifier Mode)

First, the MOSFET-only digitally controlled gain/loss circuit was tested in the amplifier mode. A bias voltage of 1.5 V was applied to keep all MOSFET capacitors in their accumulation regions. The amplitude of the input signal was set in such a way that the amplitude of the output signal would be 2, 4, and 6 Vp-p.

The test results are summarized in Table 8-1 and Figure 8.10. Figure 8.11a shows the output spectrum of the gain circuit with a gain of 10 for a fully differential output of 2 Vp-p. The largest harmonic component was -78 dB below the signal level, and a S/THD of 74 dB was obtained. For a 4 Vp-p output swing, the third harmonic component was -73 dB below the signal, and the S/THD was 71 dB (Figure 8.11b). These few dB discrepancies compared to the results of the SC amplifier using double-poly capacitors can be attributed to the nonlinearity of the MOSFET capacitors. For a 6 Vp-p output swing, the S/THD ratio decreases to 63 dB. It is likely that this distortion was caused by both the limited output range of the op-amp and the nonlinearity of the MOSFET capacitors.

Table 8-1 S/THD ratios of the MOSFET-only gain circuit

V_{out}	Gain = 1	Gain = 2	Gain = 5	Gain = 10	Gain = 15
2 Vp-p	76 dB	75 dB	75 dB	74 dB	73 dB
4 Vp-p	80 dB	74 dB	72 dB	71 dB	70 dB
6 Vp-p	75 dB	65 dB	63 dB	63 dB	63 dB

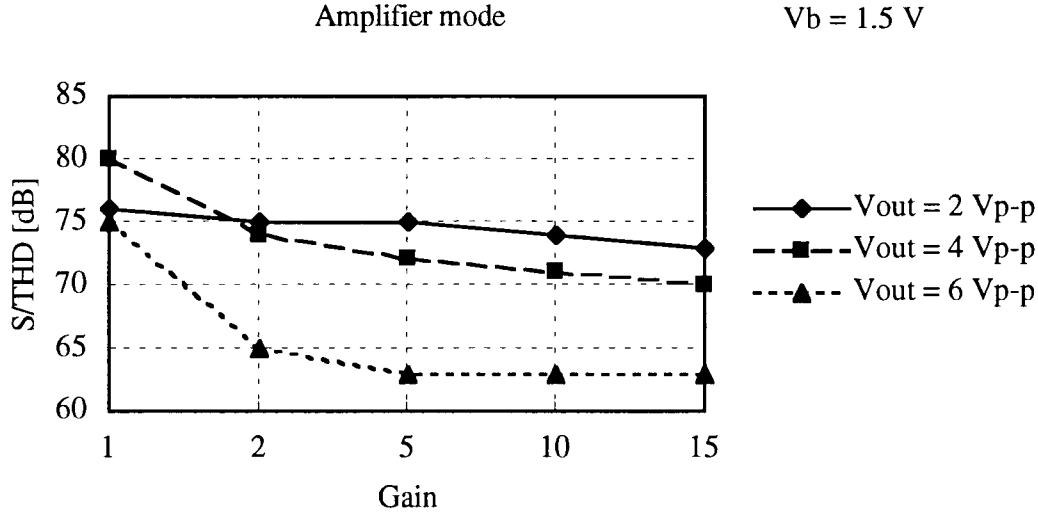
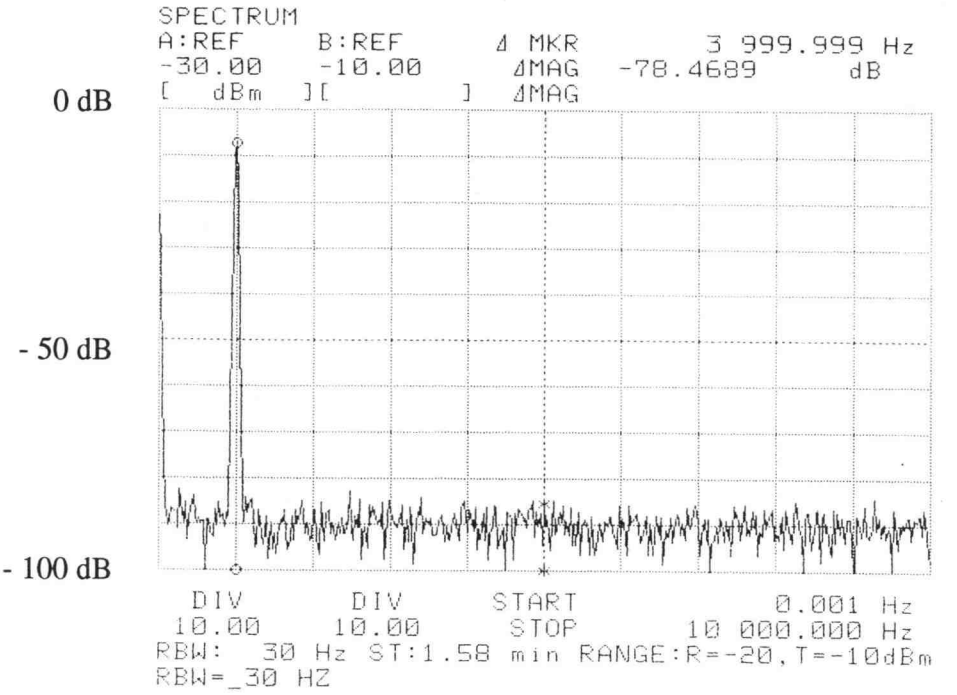
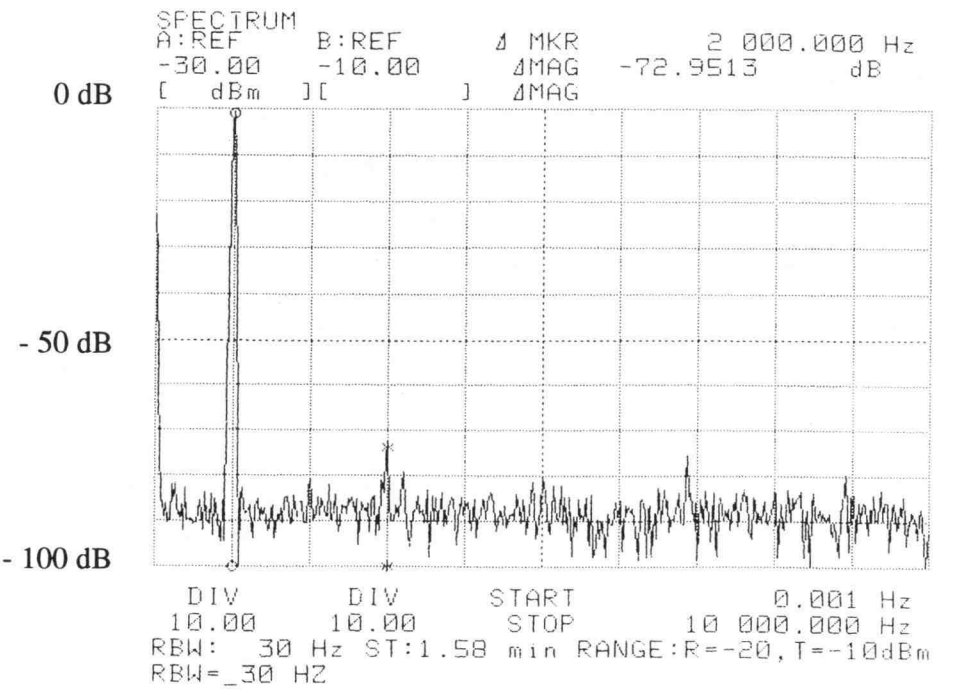


Figure 8.10 S/THD ratios of the MOSFET-only amplifier

The linearity of the gain circuit improves when the circuit operates with a unity gain. A S/THD ratio of 76 dB and 80 dB were obtained for 2 Vp-p and 4 Vp-p output swings, respectively, as shown in Figure 8.12. A S/THD of 75 dB was obtained even for a 6 Vp-p output swing while that of the SC amp using double-poly capacitors was only 68 dB. In addition, for a gain of unity, its S/THD ratios are better for 4 Vp-p than for 2 Vp-p, while the S/THD ratios are better for 2 Vp-p than for 4 Vp-p in other gain configurations with a gain of 2 to 15. The reason is considered as follows. In general (such as for a gain of 2 to 15), the distortion increases as the output swing increases, because the operating range of MOSFET capacitors widens. In addition, because the minimum voltage across the MOSFET capacitors decreases, the nonlinearity caused by the capacitors becomes larger.

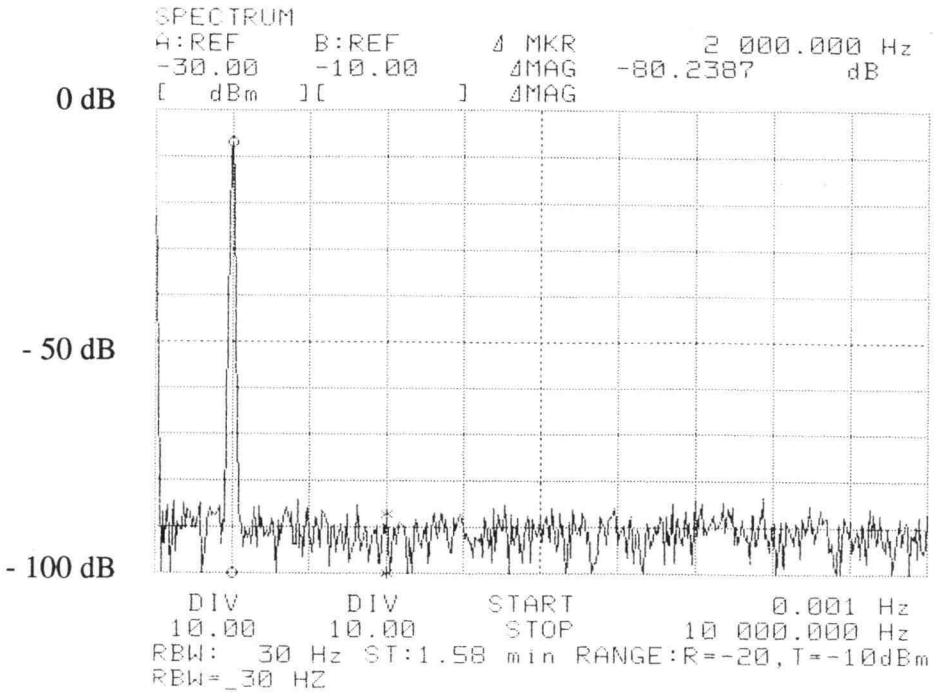


(a)

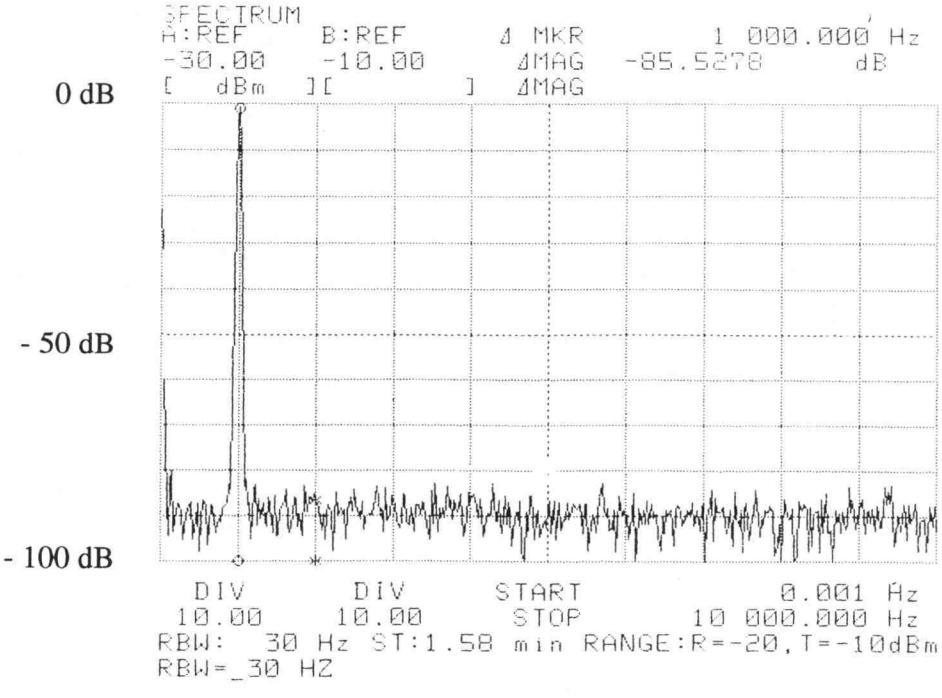


(b)

Figure 8.11 The measured output spectrum of the MOSFET-only SC amplifier with a gain of 10: a) Vout = 2 Vp-p; b) Vout = 4 Vp-p.



(a)



(b)

Figure 8.12 The measured output spectrum of the MOSFET-only SC amplifier with a gain of unity: a) Vout = 2 Vp-p; b) Vout = 4 Vp-p.

By contrast, a gain of unity is a special case because the voltage across the input capacitor and the output capacitor becomes equal. If the nonlinearities of the two capacitors match well, their capacitances also become equal even if they are nonlinear, and then their nonlinearities cancel each other. In this special case, linearity degradation by increased voltage swing seems to be insignificant. On the contrary, an increased signal level helps to improve the S/THD ratio in the unity-gain SC amplifier. Thus, the linearity of the unity-gain configuration is extremely good, even better than that of the double-poly SC amp with a gain of 10.

8.4.3 MOSFET-Only Gain/Loss Circuit (Attenuator Mode)

Next, the MOSFET-only digitally controlled gain/loss circuit was tested in the attenuator mode. The amplitude of the input signal was set at 2, 4 and 6 Vp-p. The experimental results are summarized in Table 8.2 and Figure 8.13. Their linearity was lower than those obtained in the amplifier mode. Since an attenuator reduces the signal level, the S/THD ratio reduces as the output swings smaller, or as the loss gets smaller.

In an attenuator with a loss of 1/10 for a fully differential input of 2 Vp-p, the largest harmonic component was -58 dB below the signal, and it was nearly the same as the noise level. The S/THD ratio was 55 dB. For a 4 Vp-p input, both the signal and the third harmonic increased, and its S/THD was nearly the same level as for 2 Vp-p. When the circuit operated with a loss of 1/2, a S/THD ratio increased to 67 dB and 72 dB for a 2 Vp-p and 4 Vp-p input swing, respectively. In the unity-loss configuration, the linearity of the circuit further improved as in the case of the equivalent unity-gain configuration.

When the input amplitude is constant for various loss values, the nonlinearity caused by the input capacitors dominated the distortion level because the input swing was much larger than the output swing, and nonlinearity caused by the op-amp and output capacitors was negligible compared to the nonlinearity caused by input capacitors as long as

an output swing was not very large. Thus, a larger output signal contributed to a better linearity. Hence, the linearity of the loss circuit improved as the loss approached 1.

Table 8-2 S/THD ratios for the MOSFET-only loss circuit

V_{in}	Loss = 1/15	Loss = 1/10	Loss = 1/5	Loss = 1/2	Loss = 1
2 Vp-p	52 dB	55 dB	62 dB	67 dB	75 dB
4 Vp-p	55 dB	55 dB	67 dB	72 dB	81 dB
6 Vp-p	58 dB	57 dB	64 dB	63 dB	74 dB

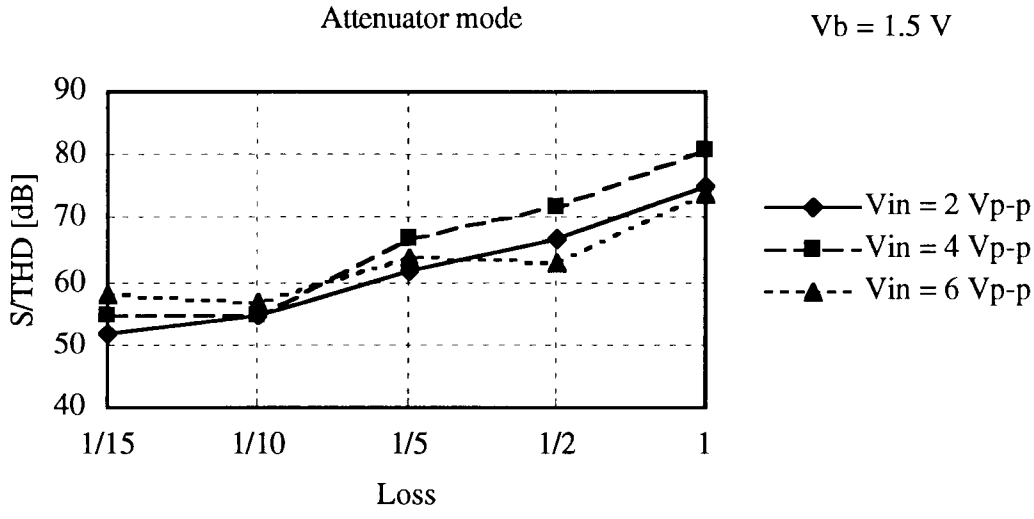


Figure 8.13 S/THD ratios of the MOSFET-only attenuator

8.4.4 Linearity Dependence on the Bias Voltage

So far, all experimental results of the MOSFET-only gain/loss circuit were achieved with a bias voltage of 1.5 V to enable a large output swing. If the bias voltage increases to 2.0 V, the amplitude of the fully differential output and/or input will be limited to 4 Vp-p: otherwise a pn junction in PMOS switches will turn on and charges stored on MOSFET capacitors will be lost. (A solution to increase a bias voltage while keeping a large signal

swing will be described in Chapter 10.) However, by applying a larger bias voltage, MOSFET capacitors will be kept in their accumulation region more deeply so that some linearity improvement will be expected.

Table 8-3 and Figure 8.14 show the S/THD ratios of the MOSFET-only gain circuit with Vb = 2.0 V and Vout = 4 Vp-p as well as with Vb = 1.5 V for comparison. In the entire gain range, we can see linearity improvements with increasing Vb. Figure 8.15a shows the output spectrum for a gain of 10. The largest harmonic component was -81.7 dB

Table 8-3 S/THD ratios of the MOSFET-only gain circuit with Vb=1.5 V and 2.0V (Vout = 4 Vp-p)

V_b [V]	Gain = 1	Gain = 2	Gain = 5	Gain = 10	Gain = 15
1.5	80 dB	74 dB	72 dB	71 dB	70 dB
2.0	82 dB	78 dB	77 dB	76 dB	74 dB

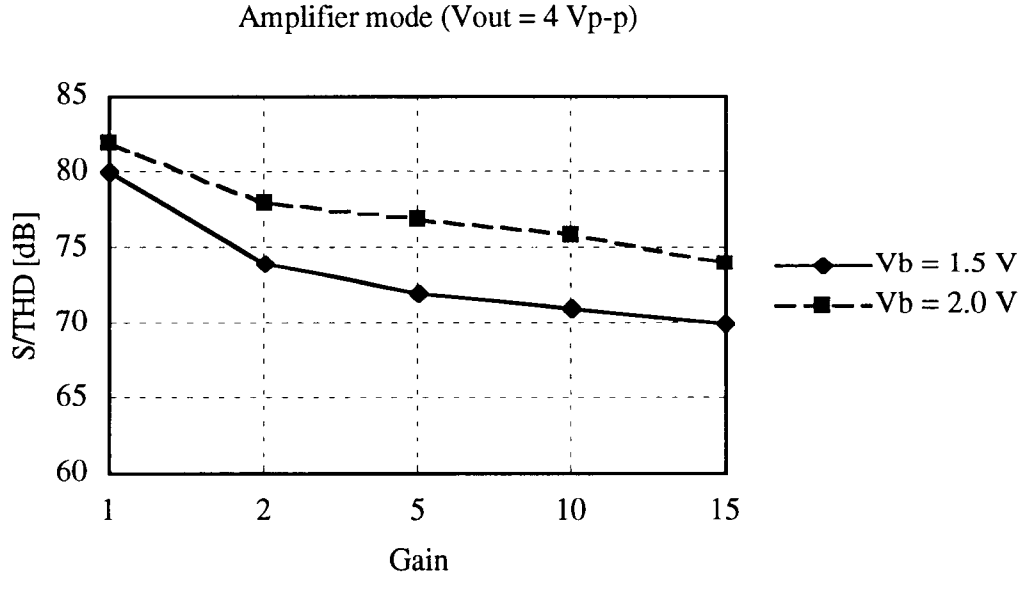
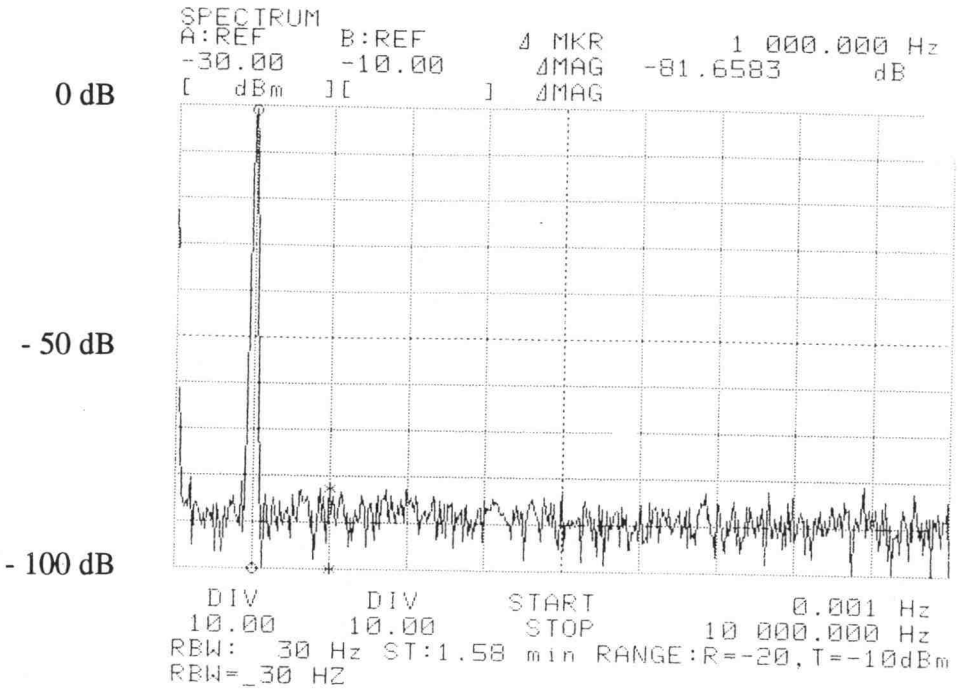
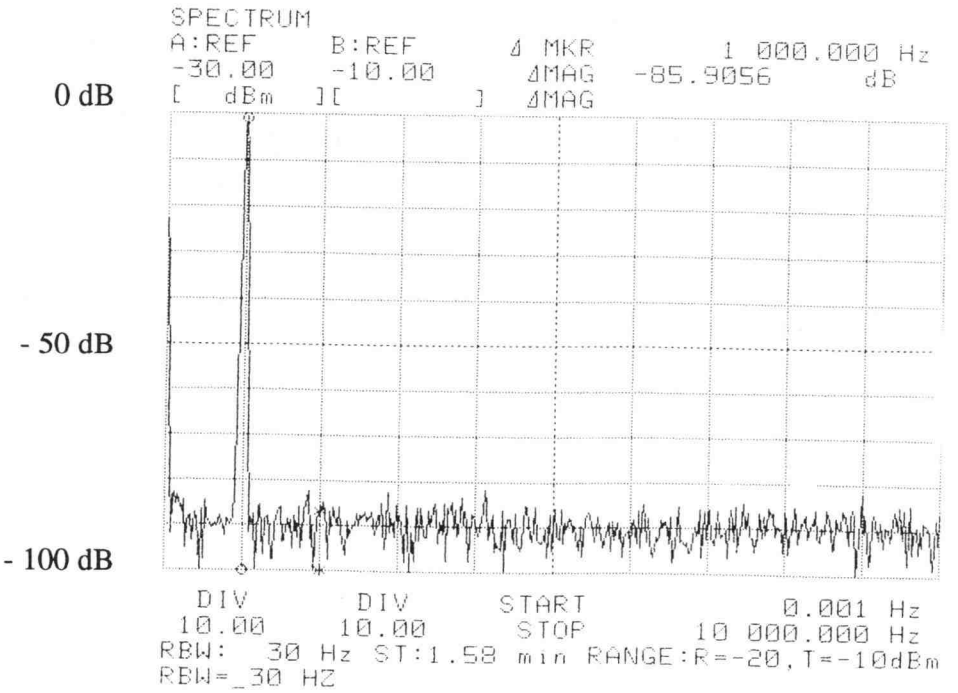


Figure 8.14 Linearity dependence on bias voltage (Vout = 4 Vp-p)



(a)



(b)

Figure 8.15 The measured output spectrum of the MOSFET-only SC amplifier with Vb = 2.0 V: a) gain = 10; b) gain = 1.

below the signal level, and its S/THD was 76 dB, which is the same as the S/THD for the SC amplifier with double-poly capacitors. Figure 8.15b shows the output spectrum for a gain of 1. The harmonic components are almost hidden in the noise, and the S/THD was 82 dB. Table 8-4 and Figure 8.16 show a comparison of S/THD ratios of the MOSFET-only gain circuit with Vb = 1.5 V and 2.0 V at Vout = 2 Vp-p. The improvement of linearity for Vout = 2 Vp-p was not so outstanding as for Vout = 4 Vp-p, however, a slight increase of S/THD was observed.

Table 8-4 S/THD ratios for the MOSFET-only gain circuit with Vb=1.5 V and 2.0 V (Vout = 2 Vp-p)

V_b [V]	Gain = 1	Gain = 2	Gain = 5	Gain = 10	Gain = 15
1.5	76 dB	75 dB	75 dB	74 dB	73 dB
2.0	77 dB	77 dB	75 dB	76 dB	71 dB

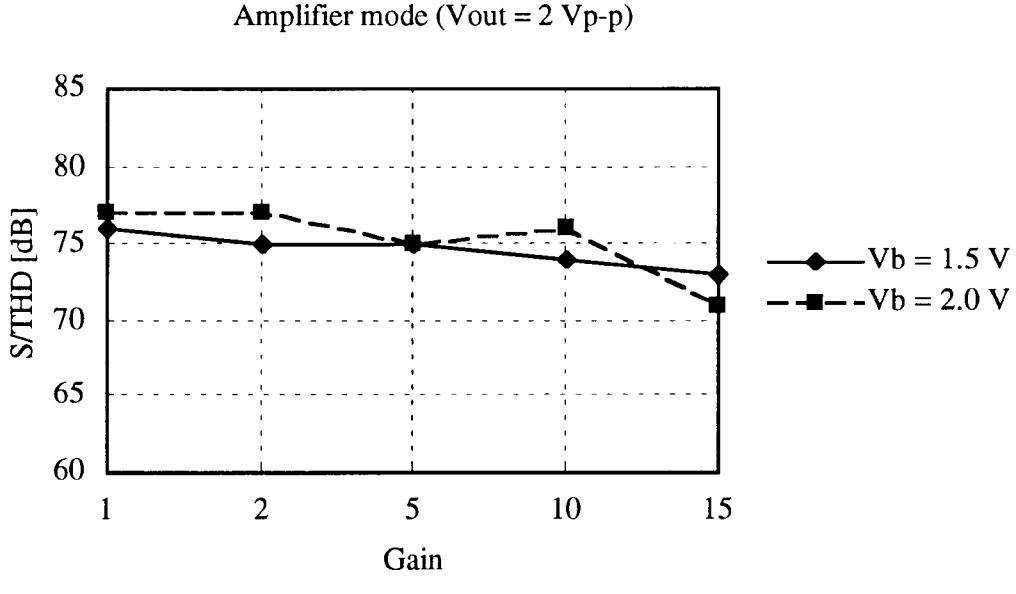


Figure 8.16 Linearity dependence on bias voltage (Vout = 2 Vp-p)

Figure 8.17 shows a comparison of S/THD ratios for the MOSFET-only gain circuit with Vout = 2 Vp-p and 4 Vp-p at Vb = 2.0 V. In the case of Vb = 2.0V, the S/THD ratios were equal or better for 4 Vp-p than for 2 Vp-p even with gains of 2 to 15. The reason is as follows. All MOSFET capacitors are biased deeply enough to operate in their linear region even for a 4 Vp-p swing. Thus, a larger signal level contributes to a better linearity.

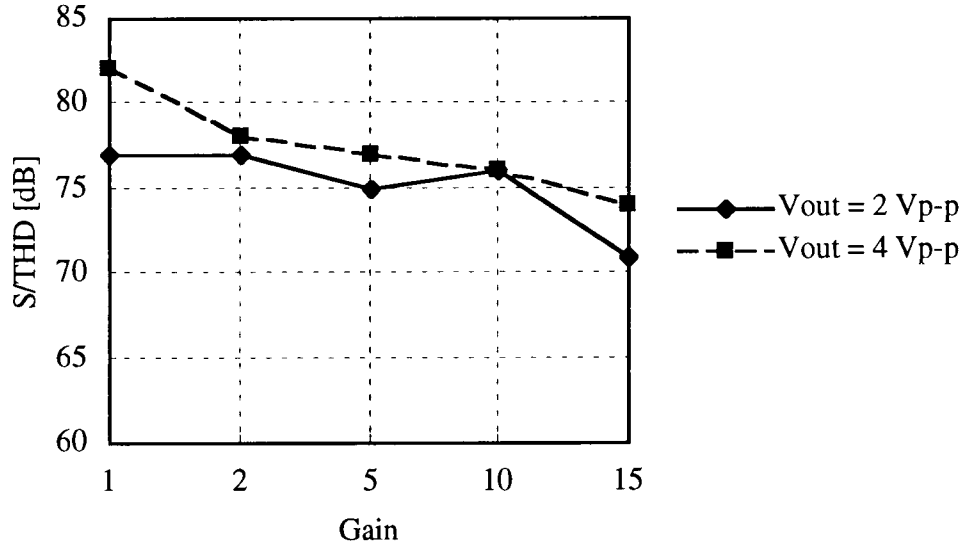


Figure 8.17 S/THD ratios for the MOSFET-only amplifier with Vb = 2.0 V

Figure 8.18 and Table 8-5 show the linearity dependence on bias voltage for the MOSFET gain circuit. For a gain of 10, the output was totally distorted with Vb = 0.5 V. As the bias voltage Vb increases to 1.0 V, a S/THD of 59 dB was obtained. However, this was still not enough to keep the MOSFET capacitors in their deep accumulation regions. By contrast, for a gain of 1, a S/THD was 78 dB even for Vb = 1.0 V. As already described, the nonlinearities of the input and output capacitors cancel each other in the unity-gain configuration, thus this high linearity can be obtained even with a small bias voltage.

Table 8-5 Linearity dependence of the MOSFET-only gain circuit on the bias voltage (S/THD ratio at Vout = 4 Vp-p)

Gain	Vb = 0.5 V	Vb = 1.0 V	Vb = 1.5 V	Vb = 2.0 V
1	51 dB	78 dB	80 dB	82 dB
10	18 dB	59 dB	71 dB	77 dB

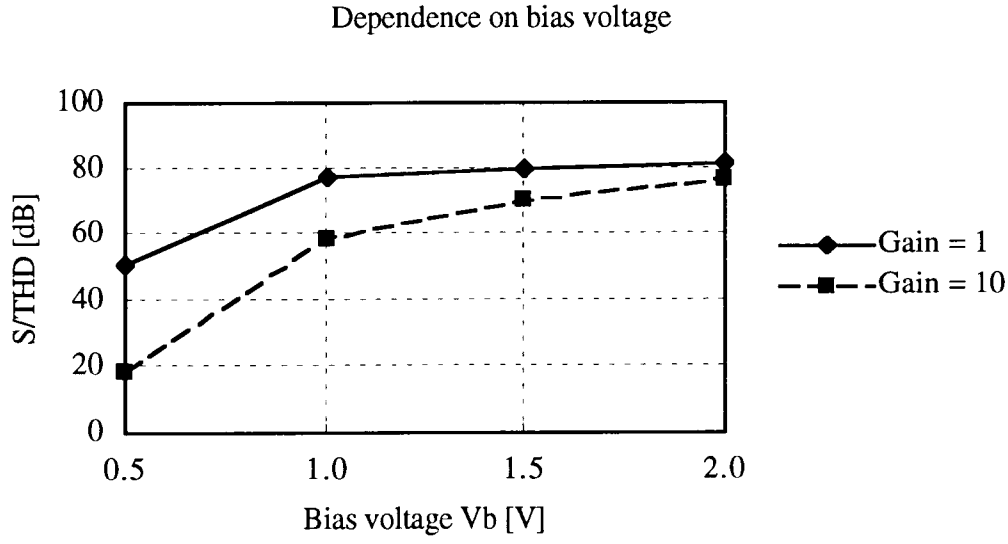
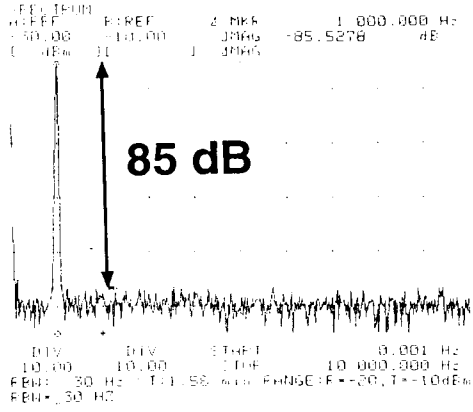


Figure 8.18 Linearity dependence on the bias voltage for the MOSFET gain circuit (Vout = 4 Vp-p)

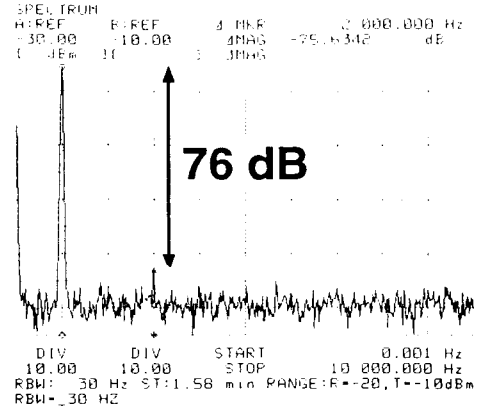
Table 8-6 and Figures 8.19-8.22 summarize the experimental results with different gains and Vb. When applying a bias voltage of 2.0 V, the linearity of the MOSFET-only gain-controlled amplifier with gain of 10 was equivalent to that of the SC amplifier with double-poly capacitors. For a gain of 1, further improvement in linearity was obtained.

Table 8-6 S/THD ratios for SC amplifiers with double-poly capacitors and with MOSFET capacitors

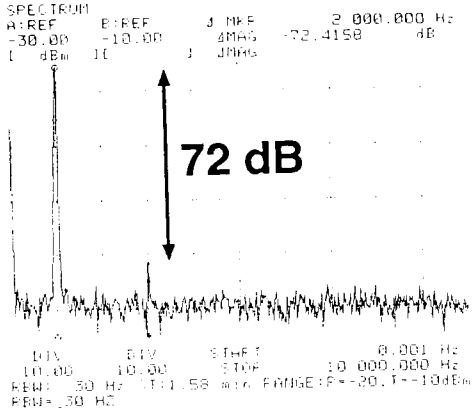
Circuit	Gain	Vb	Vout = 2.0 V	Vout = 4.0 V
SC amp with double-poly capacitors	10	0 V	76 dB	76 dB
MOSFET-only gain-controlled amp	10	2.0 V	76 dB	76 dB
MOSFET-only gain-controlled amp	10	1.5 V	74 dB	71 dB
MOSFET-only gain-controlled amp	1	2.0 V	77 dB	82 dB
MOSFET-only gain-controlled amp	1	1.5 V	76 dB	80 dB



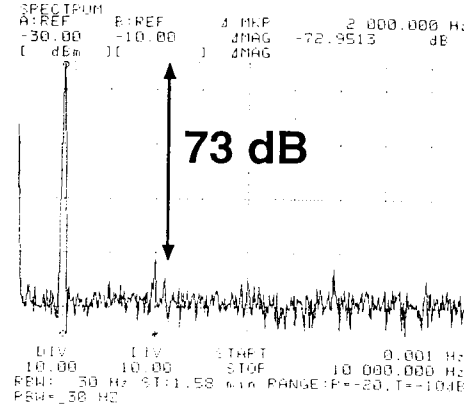
Gain=1



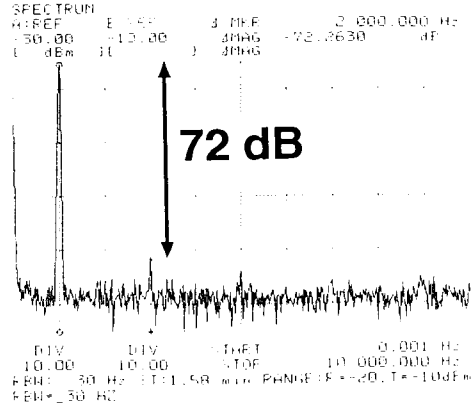
Gain=2



Gain=5

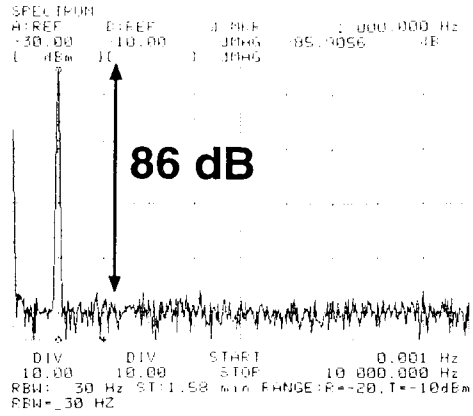


Gain=10

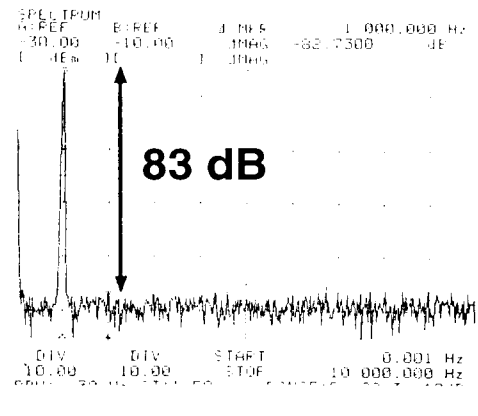


Gain=15

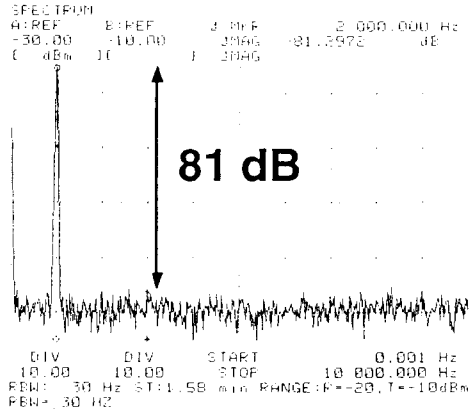
Figure 8.19 Measured output spectra in amplifier mode: Vout = 4 Vp-p; Vb = 1.5 V.



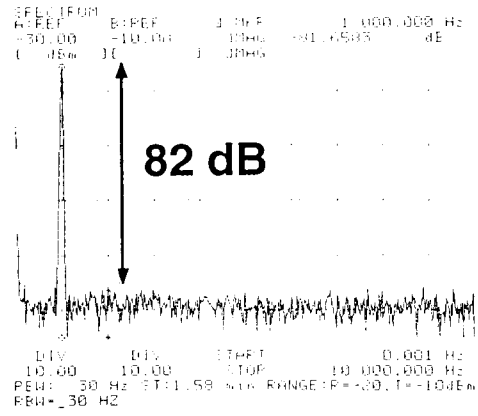
Gain=1



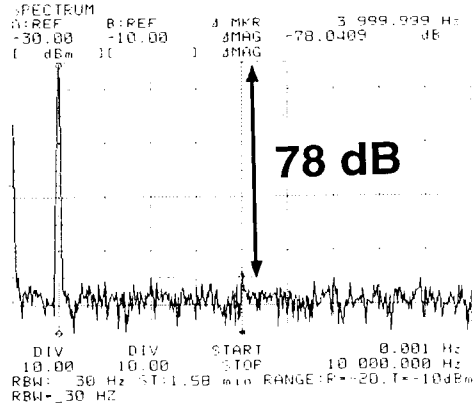
Gain=2



Gain=5

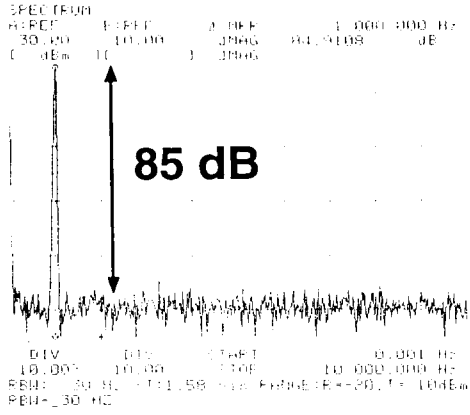


Gain=10

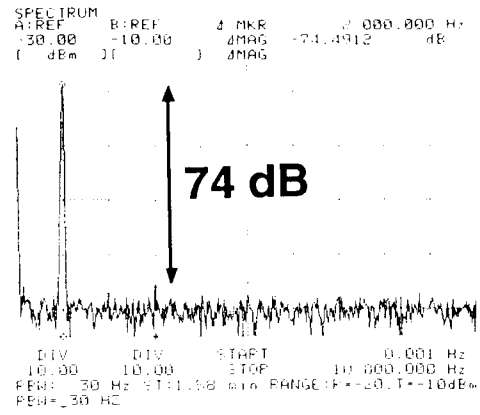


Gain=15

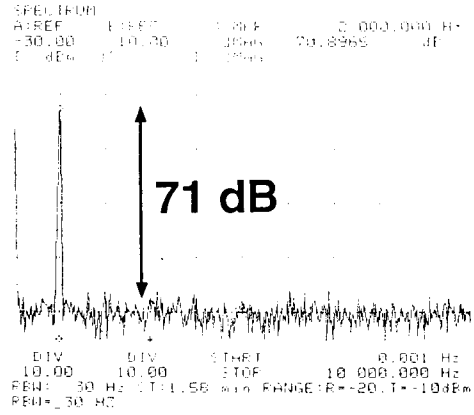
Figure 8.20 Measured output spectra in amplifier mode: Vout = 4 Vp-p; Vb = 2.0 V.



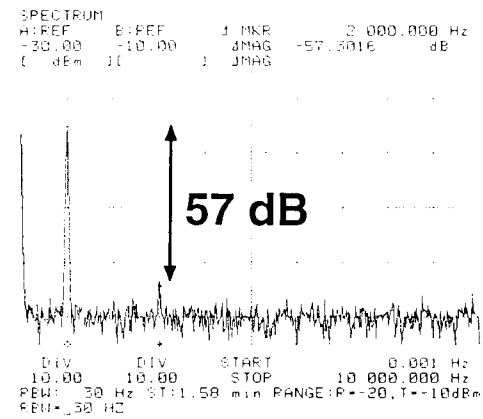
Loss=1



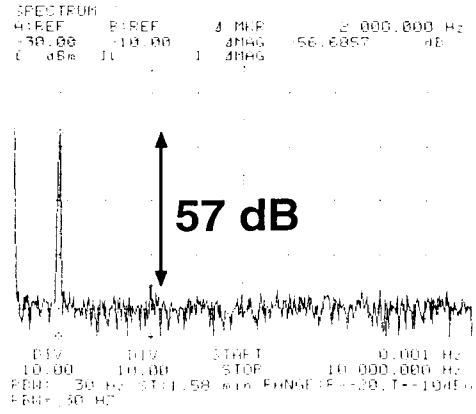
Loss=1/2



Loss=1/5

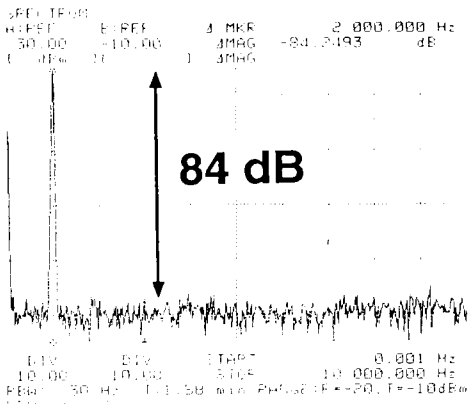


Loss=1/10

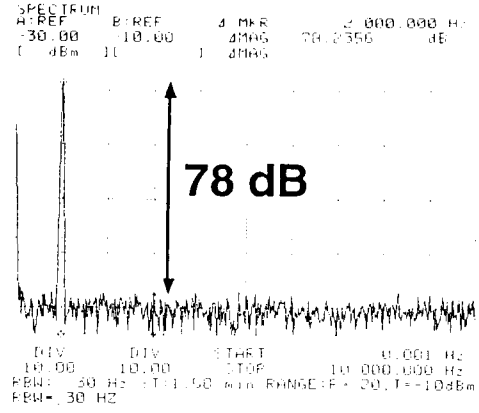


Loss=1/15

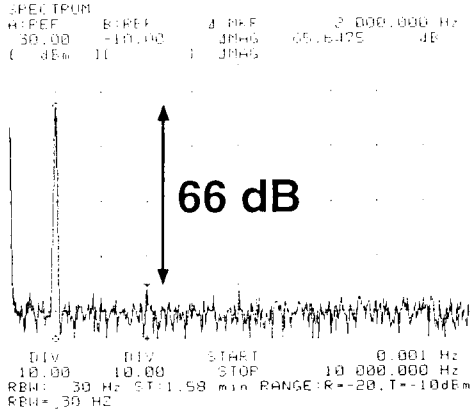
Figure 8.21 Measured output spectra in attenuator mode: Vin = 4 Vp-p; Vb = 1.5 V.



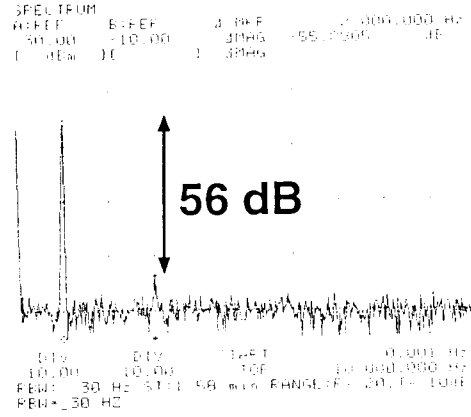
Loss=1



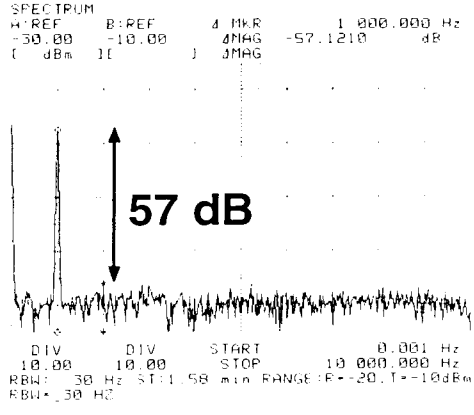
Loss=1/2



Loss=1/5



Loss=1/10



Loss=1/15

Figure 8.22 Measured output spectra in attenuator mode: Vin= 4 Vp-p; Vb = 2.0 V.

Chapter 9

PIPELINE DIGITAL-TO-ANALOG CONVERTER

An analog signal processing system which consists of an A/D converter, digital signal processor (DSP), and a D/A converter has become a popular structure because the development of a fine-line-width CMOS process has made digital circuits smaller, faster and cheaper. Consequently, A/D and D/A converters have become very important building blocks because the accuracy of the system is often determined by the performance of these data converters.

In this chapter, the design of a MOSFET-only pipeline D/A converter will be described as an example of charge processing technique. First, the background of the pipeline D/A converter will be shown. Then, circuit design using MOSFET capacitors will be presented. Finally, HSPICE simulation results will be provided.

9.1 Background of the Pipeline D/A Converter

The pipeline D/A converter (DAC) shown in Figure 9.1 has several favorable features: a) high accuracy because of small capacitor mismatch error; b) low power consumption compared to resistive array or current source DAC; c) small area because of using equal-valued capacitors instead of binary-weighted ones; d) high speed improved by a pipeline structure [39]. In addition, it can be realized using MOSFET capacitors because the charge-processing technique can be easily applied. Figure 9.2 shows the concept of charge processing. First, an input voltage is linearly converted to charge (V-Q conversion), then the charge is transferred to the later stage, and finally the charge is linearly converted to a voltage (Q-V conversion).

In this pipeline DAC, when a MOS capacitor in the capacitor array is charged to a reference voltage, it is biased in its accumulation region, and hence the voltage-to-charge

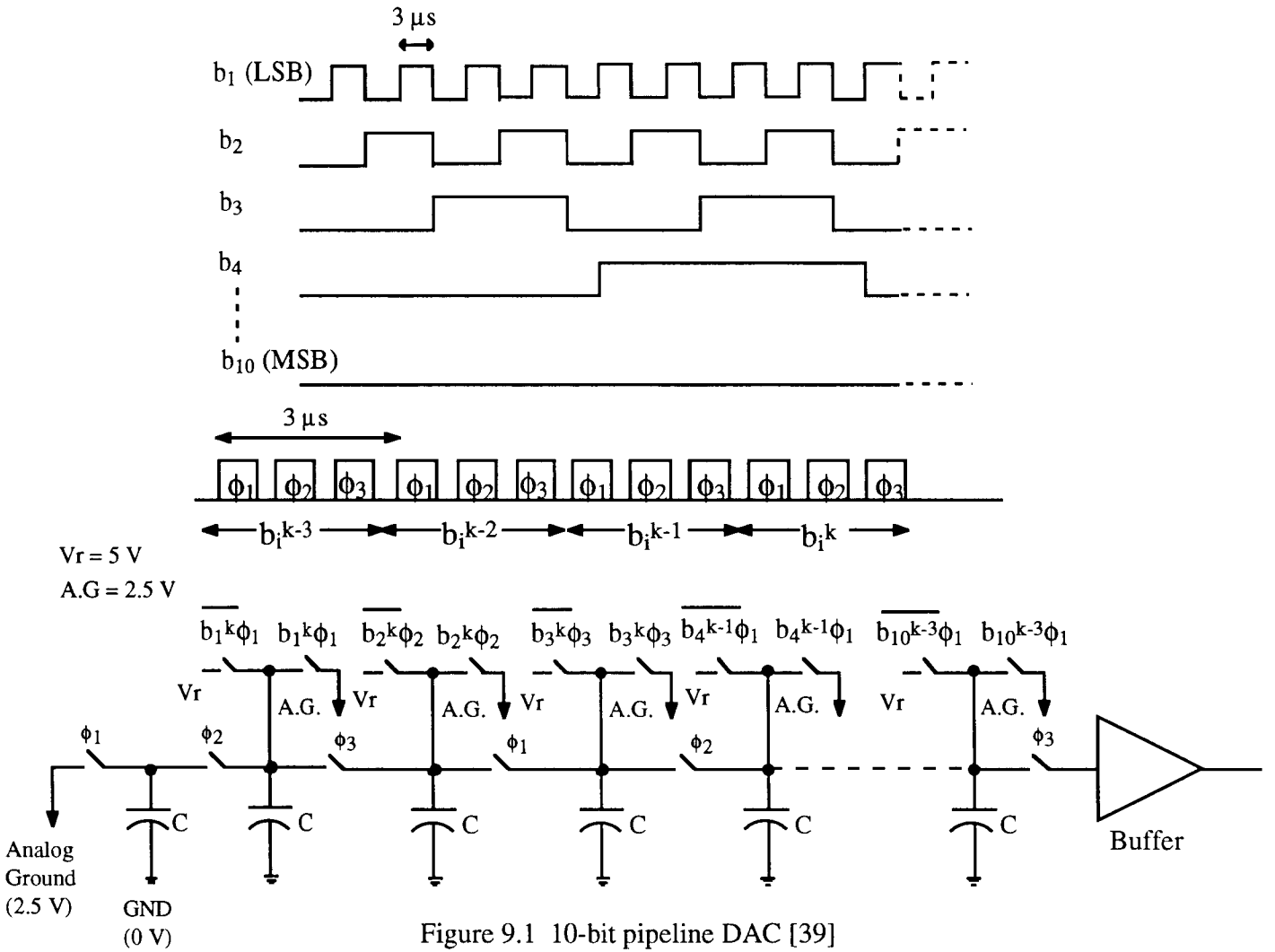


Figure 9.1 10-bit pipeline DAC [39]

conversion is performed nearly linearly. Also, the charge acquired is nominally the same for all capacitors. When the capacitor is switched to ground, no nonlinear effects will be encountered. Finally, when a capacitor is connected to its neighbor, the two capacitors share their charges and their total charge is conserved. Thus by means of charge processing, the DAC converts digital inputs to an analog output linearly even with nonlinear MOSFET capacitors. However, in order to have an output voltage signal, a charge-to-voltage (Q-V) converter has to follow the pipelined capacitors. This Q-V conversion can be achieved by using one of the proposed SC branches.

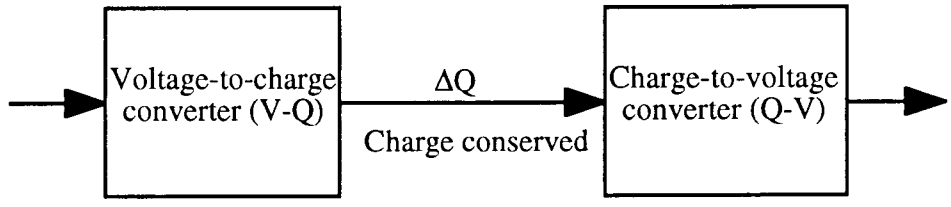


Figure 9.2 The concept of charge processing

Theoretically, when a digital input is high, its corresponding capacitor of the pipeline should be charged between V_r and V_{SS} (instead of the analog ground) to have a large dynamic range. However, in HSPICE simulation, when a voltage across a MOSFET capacitor reduced to 0 V, the charge stored on the capacitor was not zero, and that resulted in an error. It is believed that this was caused by the integration algorithm of HSPICE. Therefore, to avoid the nonlinear depletion region in the simulation, all capacitors in the pipeline are switched either the reference voltage V_r (V_{DD}) or the analog ground (instead of V_{SS}) as shown in Figure 9.1.

9.2 Circuit Design

Figure 9.3 shows a simple Q-V conversion circuit using MOSFET capacitors. When $\phi 2$ goes high (reset phase), two series-compensated MOSFET capacitors are biased

in their accumulation region. In the next clock phase $\phi 3$, these MOSFET capacitors are connected between the output and virtual ground of the op-amp. At the same time, charge is transferred from the pipelined capacitor array to these capacitors. Since the series-compensated branch converts charge to voltage linearly, a desired output signal is obtained (valid phase).

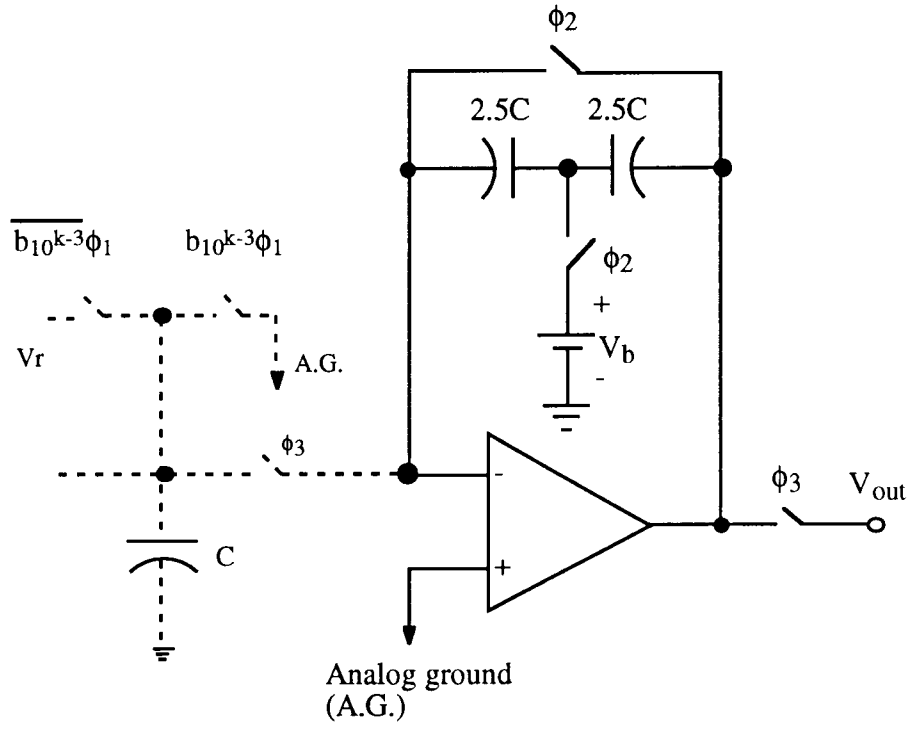


Figure 9.3 Charge-voltage converter

Figure 9.4 shows the output waveform of the pipeline DAC using this Q-V converter. For simplicity, only 4-bit configuration is used here. As can be seen from Figure 9.4, each time when $\phi 2$ goes high, the output is reset to the virtual ground level (2.5 V). Consequently, a high slew-rate op-amp will be required.

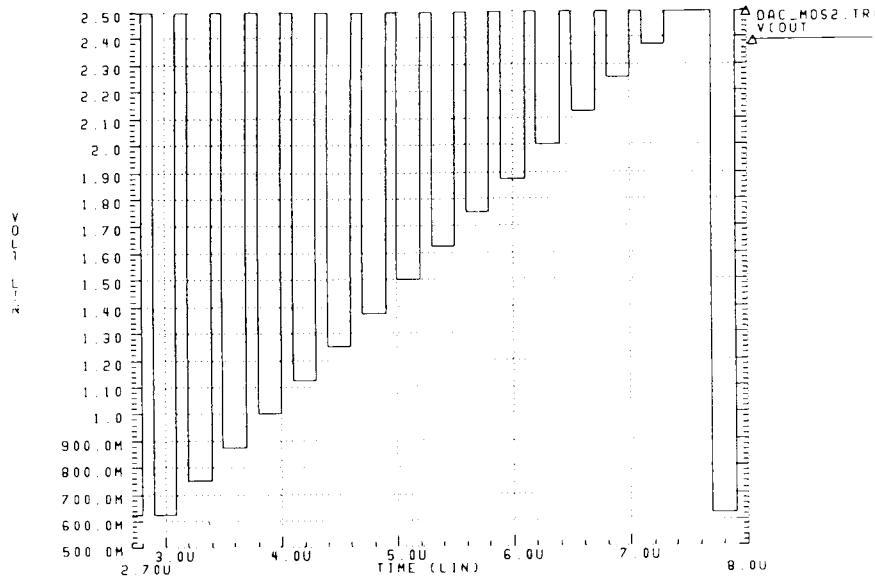


Figure 9.4 The output waveform of 4-bit pipeline D/A converter using the charge-voltage converter of Figure 9.3

To reduce the output change rate, and to alleviate the slew-rate requirements for the op-amp, another Q-V converter (with a 4-bit pipelined capacitor array) can be used. It is illustrated in Figure 9.5. When $\phi 1$ and $\phi 2$ are high, the two series-compensated capacitors are reset (and biased to operate in their accumulation region). A capacitor Cc is biased to 2.5 V during $\phi 1$ and $\phi 2$. Capacitor Cs provides a feedback path to the op-amp to prevent it from saturating during this period.

When $\phi 3$ goes high, the output becomes available. Now the capacitor Cc is charged to the output level. In the next clock $\phi 1$, Cc is connected to the virtual ground, and the charge flow from the top plate of Cc into the virtual ground node is negative because the voltage across Cc during $\phi 3$ was less than 2.5 V. On the other hand, the charge flow from the series-connected capacitor C_1 is positive. The change in the voltage across Cc between $\phi 2$ and $\phi 3$ is twice as large as that for C_1, but C_1 is twice as large as Cc. Thus, the charge flows from Cc and from C_1 when $\phi 3$ goes high cancel each other.

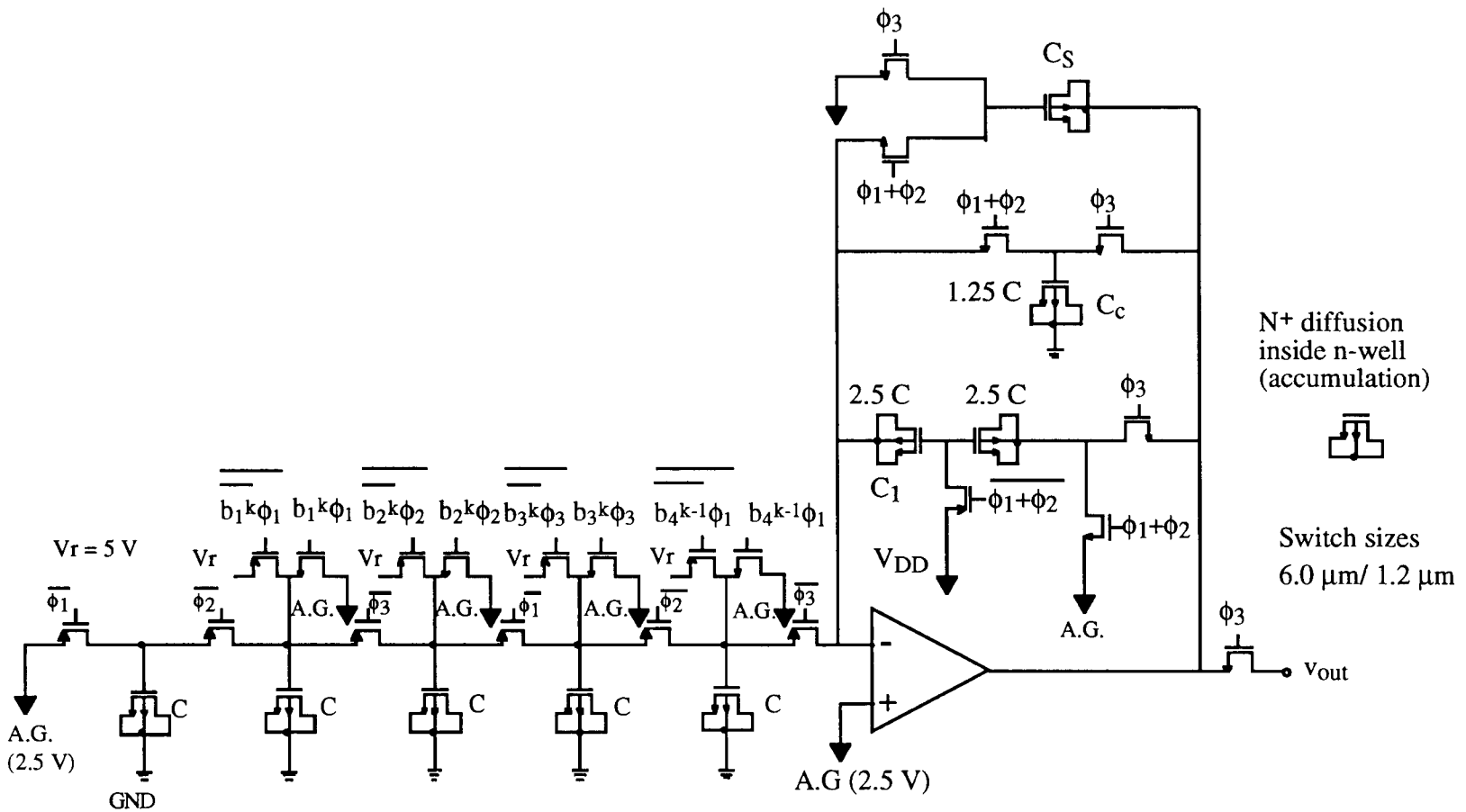


Figure 9.5 Pipeline D/A converter using an improved charge-voltage converter

An alternative Q-V converter is shown in Figure 9.6. In this circuit, an auxiliary capacitor Cv is added to create an improved virtual ground, and the last capacitor of the pipelined array is connected to that node instead of the real ground. The role of C_S is the same as in Figure 9.5 and C_{dg} works as a deglitching capacitor to prevent spikes in the output signal.

Figures 9.7 and 9.8 show the simulated output waveforms for the circuits of Figure 9.5 and 9.6, respectively. In Figure 9.8, the output changes when $\phi 3$ goes high, and it keeps that level in the consecutive clock phases $\phi 1$ and $\phi 2$. Thus, the slew-rate requirement for the op-amp is greatly reduced. We see glitches, however, during the non-overlapping period because no deglitching capacitor is used.

In Figure 9.8, the glitches are reduced by the deglitching capacitor C_{dg}. Also, in this circuit, the output during the valid phase $\phi 3$ is held during the consecutive clock phases $\phi 1$ and $\phi 2$.

9.3 Simulation Results

The circuits shown in Figure 9.5 and 9.6 were simulated using HSPICE. In these simulations, the capacitor array was extended to 10 bits. The size of a MOSFET capacitor C was 12 x 18 μm x 18 μm, which corresponds to 6 pF. The size of switches was 6.0 μm x 1.2 μm for both PMOS and NMOS devices. An op-amp macro model was used in the simulations.

Figure 9.9 and 9.10 show an integral non-linearity (INL) of the 10-bit pipeline D/A converter using the Q-V converters of Figure 9.5 and 9.6, respectively. The INL was +/- 1.30 mV for Figure 9.5 and +/- 1.55 mV for Figure 9.6. Both of them were slightly larger than 1 LSB for a 10 bit accuracy (+/- 1 mV). Figure 9.6 is a glitch-free circuit. However, the last capacitor of the pipelined array in Figure 9.6 may have a mismatch with the other capacitors in the array because its bottom plate is switched from the real ground to the virtual ground while the bottom plates of other capacitors are fixed to the real ground.

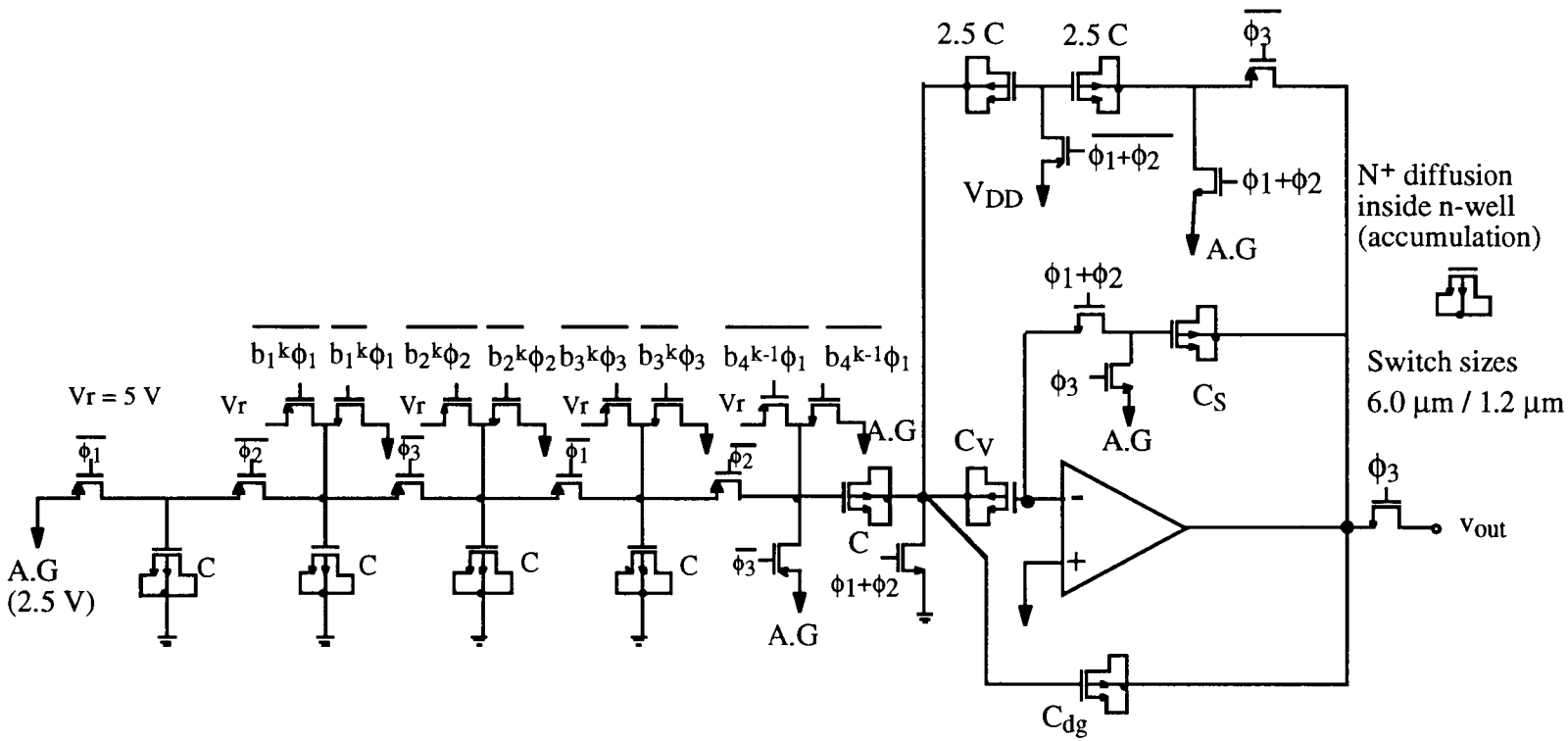


Figure 9.6 Pipeline D/A converter using an alternative charge-voltage converter

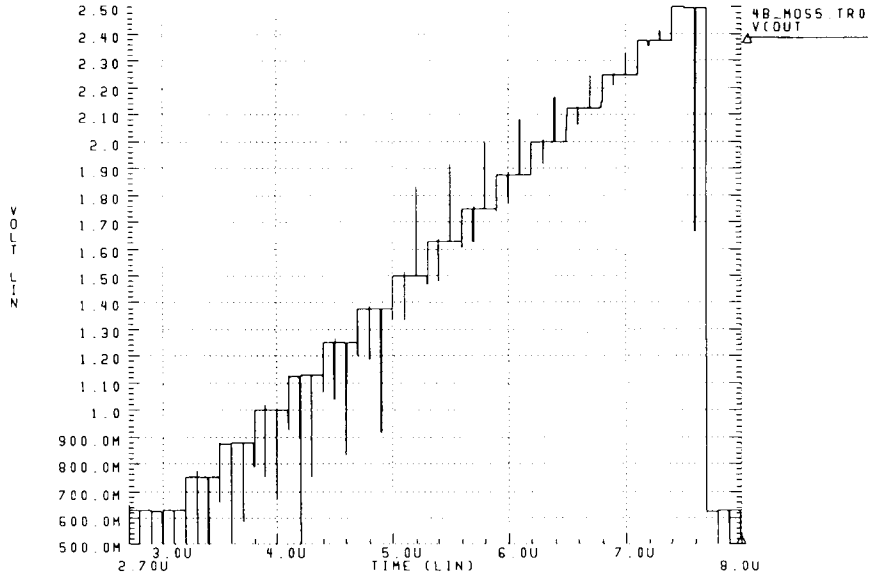


Figure 9.7 The output waveform of 4-bit pipeline D/A converter using the charge-voltage converter of Figure 9.5

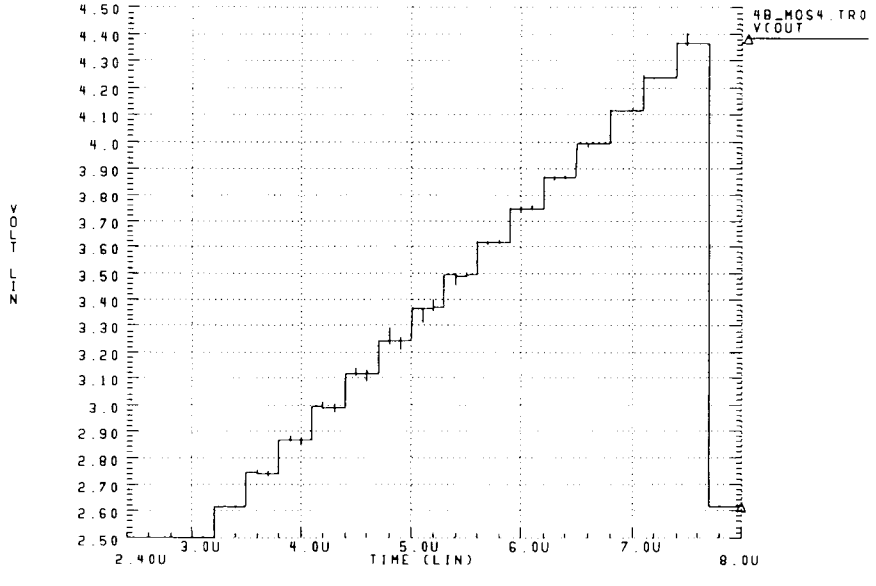


Figure 9.8 The output waveform of 4-bit pipeline D/A converter using the charge-voltage converter of Figure 9.6

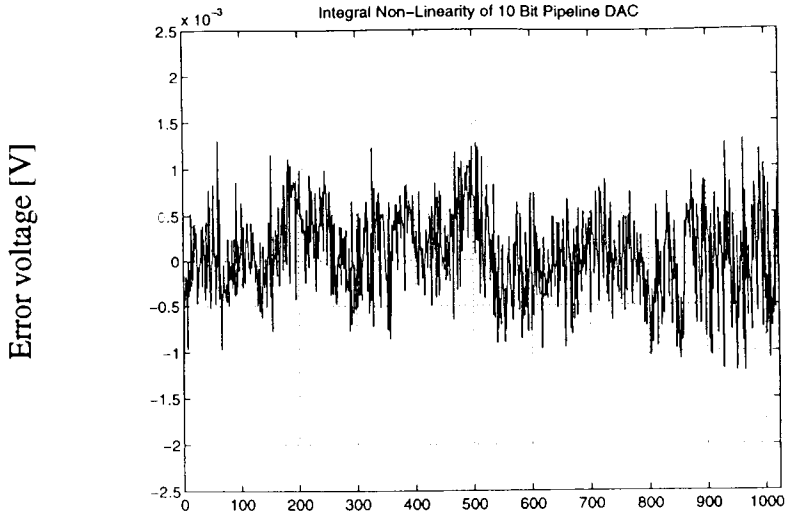


Figure 9.9 Integral nonlinearity (INL) of the 10-bit pipeline D/A converter using the Q-V converter of Figure 9.5

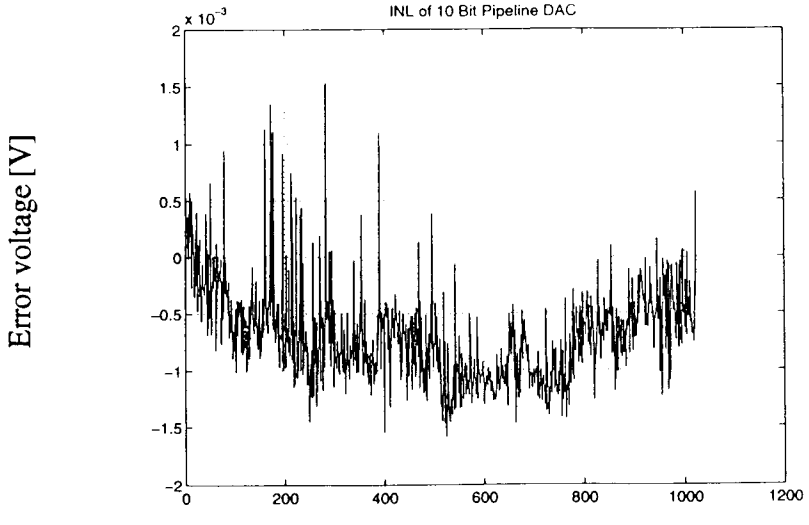


Figure 9.10 Integral nonlinearity (INL) of the 10-bit pipeline D/A converter using the Q-V converter of Figure 9.6

Chapter 10

NONLINEARITY COMPENSATION IN DEEP SUBMICRON AND LOW-VOLTAGE PROCESSES

A demand for higher integration density forces CMOS processes to use deep submicron line widths. In a deep submicron process, the gate oxide becomes thinner and electrical field increases. Consequently, the carrier distribution in the MOSFET channel will be affected, and that results in an increase of the MOSFET capacitor nonlinearity. Hence it is preferred that the bias voltage across MOSFET capacitors be increased to have a better linearity. However, in such a process, the supply voltage has to be lowered for the reliability of the MOS devices. In addition, the need for battery-operated equipment also demands low-voltage operation.

In this chapter, a capacitor nonlinearity compensation scheme suitable for deep submicron and low-voltage processes will be discussed. First, series compensation in low-voltage operation will be described. Then, a new switch configuration which provides larger bias voltage to series-compensated MOSFET capacitors will be presented, along with HSPICE simulation results.

10.1 Series Compensation in Low-Voltage Operation

In circuits using the series compensation technique described in Section 4.4, the voltage of the top capacitor plates (node A in Figure 10.1) should not exceed V_{DD}, because any voltage larger than V_{DD} at node A can forward bias the pn junction between a p+ diffusion and the n-well of the PMOS switch M1, and that results in a leakage of the charge stored in the capacitors and harmonic distortion at the output. However, when a very large voltage swing is required, or for low-voltage operation, it is desirable to allow the top-plate

node potential to exceed V_{DD}, so that a large bias voltage can be applied to the MOSFET capacitors to guarantee that all MOSFET capacitors operate in their accumulation regions.

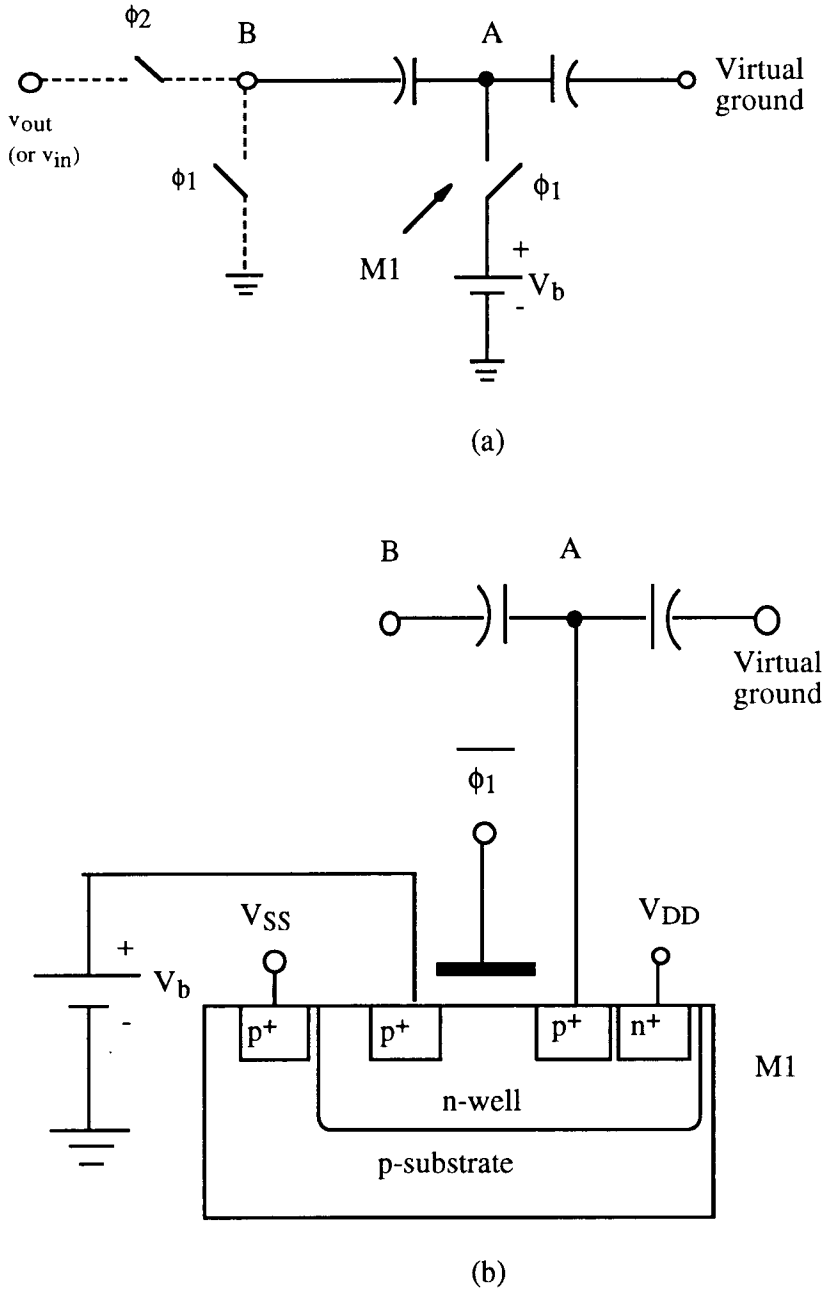
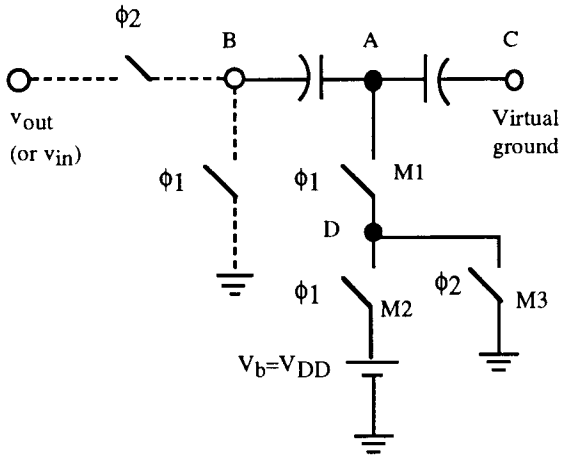
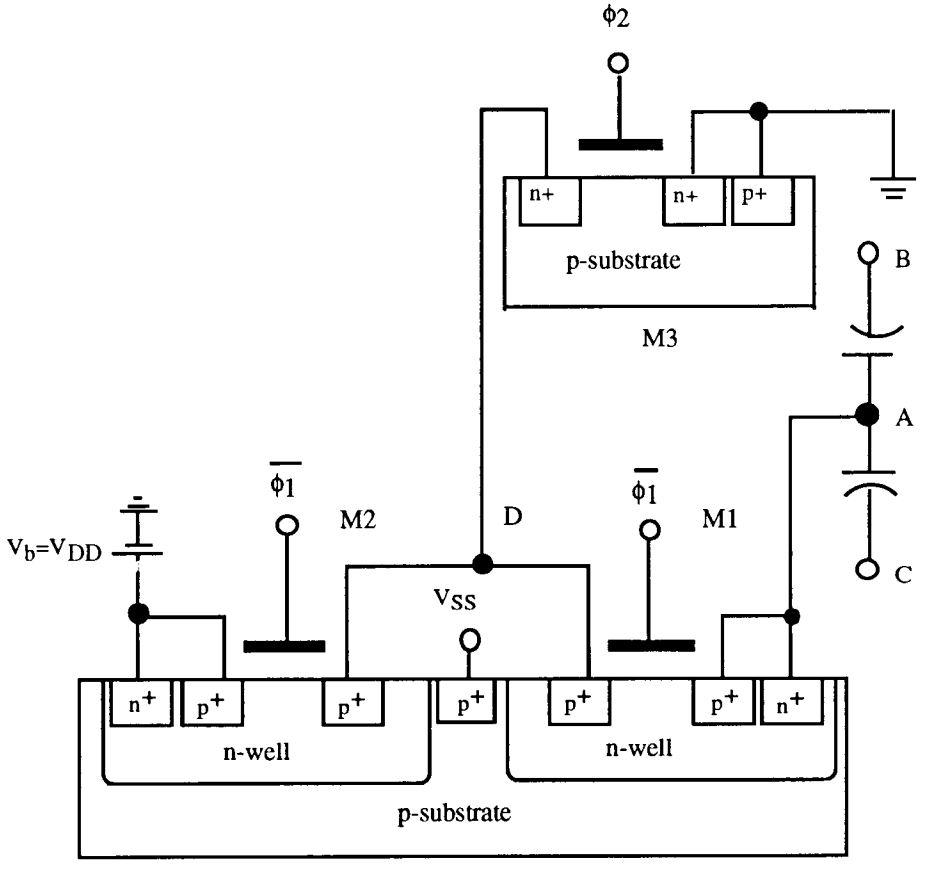


Figure 10.1 (a) Switch configuration in series compensation; (b) Practical realization of switch M1.



(a)



(b)

Figure 10.2 (a) New switch configuration for series compensation; (b) Practical realization of series switches M1 and M2.

For example, assume that $V_b = V_{DD} = -V_{SS} = 1.5$ V in Figure 10.1. During $\phi 1=1$, the switch M1 turns on, and the voltage at node A becomes equal to $V_b = 1.5$ V. When v_{out} increases to say 1.0 V during $\phi 2 = 1$, the voltage potential of node A exceeds V_{DD}. Then the pn junction between the p+ diffusion of M1 at node A and the n-well of M1 turns on and leakage current starts to flow if the n-well of M1 is tied to V_{DD}. If the n-well of M1 is connected to the p+ diffusion of M1 at node A, then the leakage problem can be avoided for a large positive output. However, if v_{out} decreases to -1.0 V during $\phi 2 = 1$, the voltage of node A becomes 1.0 V. Then the pn junction between the p+ diffusion of M1 connected to V_b (= 1.5 V) and the n-well of M1 (= 1.0 V) will get forward biased, and leakage current begins to flow.

10.2 New Switch Configuration for Series Compensation

To overcome this constraint, we have developed a series switch configuration, illustrated in Figure 10.2 [36]. An additional PMOS switch M2 is connected in series with the PMOS switch M1 to prevent the flow of leakage current, and an NMOS switch M3 is connected to node D to guarantee that the pn junctions at node D are reverse-biased during $\phi 2=1$. The n-wells of M1 and M2 are tied to their sources. Assume that $V_b = V_{DD} = -V_{SS} = 1.5$ V. During $\phi 1=1$, M1 and M2 turn on, and the voltage at node A becomes equal to $V_b = 1.5$ V. During $\phi 2=1$, these PMOS switches are off, and the NMOS switch M3 turns on. If v_{out} is equal to 1.0 V when $\phi 2=1$, the potential of node A goes up to 2.0 V as does the voltage of the n-well of M1. Then, the pn junction between the p+ diffusion of M1 at node D and the n-well of M1 is reverse-biased, because node D is connected to the ground. (The other pn junction between the p+ diffusion of M2 at node D and its n-well is also reverse-biased.) The pn junction between node A and the n-well of M1 is short-circuited, thus it is not forward biased. If v_{out} is equal to -1.0 V during $\phi 2 = 1$, the potential of node A becomes 1.0 V. Again, the pn junction between p+ diffusion of M1 at node D and the n-well of M1 are reverse biased. Therefore, using this switch configuration, a large voltage

swing at output (and input) node can be achieved without the leakage problem even for low supply voltages.

Notice that the additional PMOS and NMOS switches (M2 and M3) can be shared by all M1 PMOS switches in Figure 10.1. Thus, only two additional devices are required to realize this switch structure for the whole SC circuit.

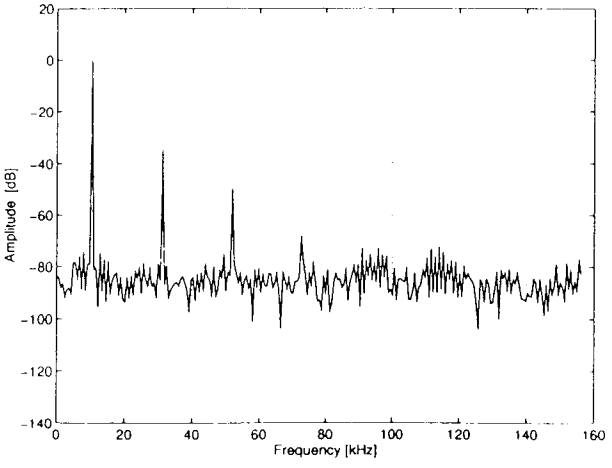
10.3 Simulation Results

To verify the effectiveness of the new switch configuration, two SC amplifiers were simulated using HSPICE: a) the original series-compensated SC amplifier shown in Figure 4.8; b) the improved circuit of Figure 4.8 in which series compensated SC branches were replaced by the new branch shown in Figure 10.2. In the new switch structure (b), a parasitic pn junction diode capacitance between the n-well and the p-substrate is connected to the node A as show in Figure 10.2. To include the effect of the parasitic capacitance in simulations, a pn junction diode model was added to the n-well of PMOS switches in the HSPICE netlist*. The conditions assumed in this simulation were similar to those used in Section 4.5 except that $V_b = V_{DD} = -V_{SS} = 1.5$ V was used. In addition, to exclude the nonlinear distortion caused by the on-resistance of switches, the clock signal for CMOS switches connected to inputs and outputs swang +/- 2.5 V.

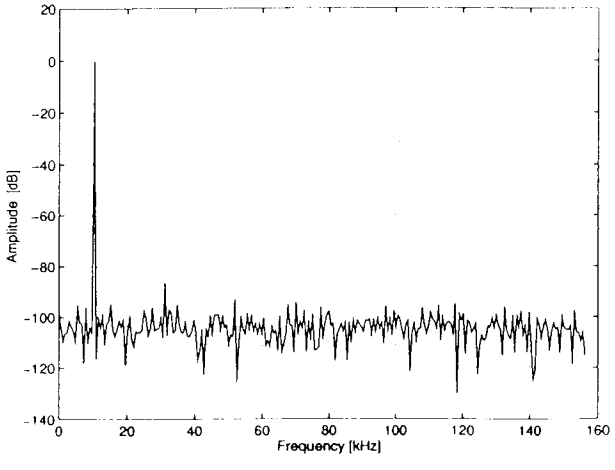
Figure 10.3a shows an output spectrum of the original SC amplifier for a 3 V supply voltage. Large harmonic components are observed in this Figure and a S/THD ratio was only 33 dB because charges stored on capacitors were lost due to leakage current through the pn junctions. Figure 10.3 b shows an output spectrum of the improved SC amplifier for a 3 V supply voltage. An S/THD of 84 dB was now obtained. The effect of the parasitic capacitance connected to the n-well of PMOS switches were insignificant because the switch size was much smaller than the main capacitor area, and also because

*A parasitic pn junction diode capacitance is connected to the node A even in the original switch configuration as shown in Figure 10.1. However, the parasitic capacitance is originally included in the SPICE MOSFET model as the drain-bulk capacitance.

the depletion width of the pn junction diode was much thicker than the gate oxide thickness. Hence, it is clear that this new switch configuration is effective for low voltage operation.



(a)



(b)

Figure 10.3 The output spectrum of the circuit of Figure 4.8 with $V_{DD} = -V_{SS} = V_b = 1.5$ V: (a) using the original switch configuration; (b) using the novel series switch scheme.

Chapter 11

CONCLUSIONS AND SUGGESTED FUTURE WORK

11.1 Conclusions

In this thesis, novel design techniques have been proposed for implementing high-linearity SC circuits in a standard digital CMOS process. They use nonlinear MOSFET capacitors instead of linear double-poly capacitors. To reduce their nonlinearities, a bias voltage is applied to keep the MOSFET capacitors in their accumulation regions. For further reduction of distortion, two capacitors are connected in series or in parallel so that a first-order cancellation of the nonlinearity can be achieved.

To realize high-linearity SC circuits, the series compensation has an advantage over the other two methods (parallel compensation and simple biasing), because the operating ranges of nonlinear capacitors are reduced by a factor of two. Several chips were fabricated in a 1.2 μm CMOS process using the series compensation, parallel compensation, and simple biasing circuits. It was demonstrated that among these techniques, the series compensation is the most effective for reducing the nonlinearity of MOSFET capacitors.

If the requirement for linearity is not too tight, the parallel compensation or the simple biasing may be useful to save chip area. To have the equivalent kT/C noise, the unit capacitance can be four times smaller for these techniques than for the series compensation. Hence the capacitor area decreases considerably.

A novel predictive SC amplifier has been proposed for reduced sensitivity to op-amp imperfections. An SC amplifier using this predictive structure and the parallel compensation was fabricated in the 1.2 μm CMOS process. Experimental results show that the S/THD of the predictive SC amplifier was 10 dB larger than that of the non-predictive one. It was shown that the predictive circuit was effective to reduce nonlinearity caused by the op-amp and/or MOSFET capacitors.

It was also demonstrated that a two stage op-amp with a large output swing can be fabricated in a standard digital CMOS process. The frequency compensation was accomplished using a source follower and a MOSFET capacitor. The source follower provides a bias voltage to the MOSFET capacitor and keeps it in its accumulation region. An SC amplifier using this two-stage op-amp and double-poly capacitors was fabricated in a 1.2 μm CMOS process, and its S/THD was 76 dB for a differential output swing of 4 Vp-p.

Using this two-stage op-amp and the series compensation, a MOSFET-only digitally controlled gain/loss circuit was designed and fabricated in a 1.2 μm CMOS process. It was demonstrated that the series compensation is effective not only for a large output swing in an amplifier, but also for a large input swing in an attenuator. For an amplifier gain of 10, the SC circuit had a S/THD of 76 dB for a 4 Vp-p output swing, which was comparable to that of the SC amplifier using double-poly capacitors. For an attenuator with a loss of 1/2, the S/THD was 72 dB for a 4 Vp-p input swing. For a unity-gain configuration, a S/THD of over 80 dB was obtained for a 4 Vp-p input and output swing.

A pipeline D/A converter utilizing MOSFET capacitors was described as an application of the charge processing technique. It consists of three parts, V-Q conversion, charge transfer, and Q-V conversion. The V-Q conversion can be linearly achieved by using two reference voltages to which MOSFET capacitors are charged or discharged. The charge transfer with pipeline operation does not require linear capacitors, because each capacitor just shares their charges with their neighbors. Finally, the V-Q conversion can be linearly performed by using series compensation. In HSPICE simulation, 9-bit accuracy has been obtained using only MOSFETs.

Having a large bias voltage helps MOSFET capacitors operate in their deep accumulation region with high linearity. However, in the series compensation, this could have lead to a charge leakage because the parasitic pn junction diode of the PMOS switch

connected to the connecting node of two series-connected MOSFET capacitors turns on. Therefore, the bias voltage was limited to some extent. A new switch configuration to solve this leakage problem and to enable the series compensation have a large bias voltage has been proposed. HSPICE simulation shows that it works well and it will be helpful for a low-voltage operation, too.

11.2 Suggested Future Work: SC Integrators and Filters

The SC integrator is an important building block for realizing SC filters. Parallel compensation and simple biasing, which were described in Chapter 4, can be applied to an SC integrator as shown in Figures 11.1 and 11.2.

It is also possible to build an SC integrator by using series compensation. For example, Figure 11.3 shows a modified SC integrator whose transfer function is given by

$$\frac{C_1}{C_2}\frac{2-z^{-1}}{1-z^{-1}} \qquad (11\text{-}1)$$

However, it is difficult to apply series compensation to an SC integrator whose transfer function is given by

$$\frac{1}{1-z^{-1}} \qquad (11\text{-}2)$$

One way to solve this problem is, as shown in Figure 11.4, to add a charge-to-voltage (Q-V) converter to the output of an SC integrator. Here, the nonlinearity errors caused by nonlinear capacitors C_2 and C_3 cancel each other because the voltage across these capacitors become equal during $\phi 1=1$. The concept of charge processing, described in Chapter 3, can be extended to more complicated higher-order filters. Figure 11.5 shows a realization of high-Q biquad. The circuit surrounded by the broken line is a conventional high-Q biquad [17] followed by a charge-to-voltage (Q-V) converter. Once the input voltage is converted to charge, then the charges are transferred to the last Q-V converter where they are reconverted into voltages.

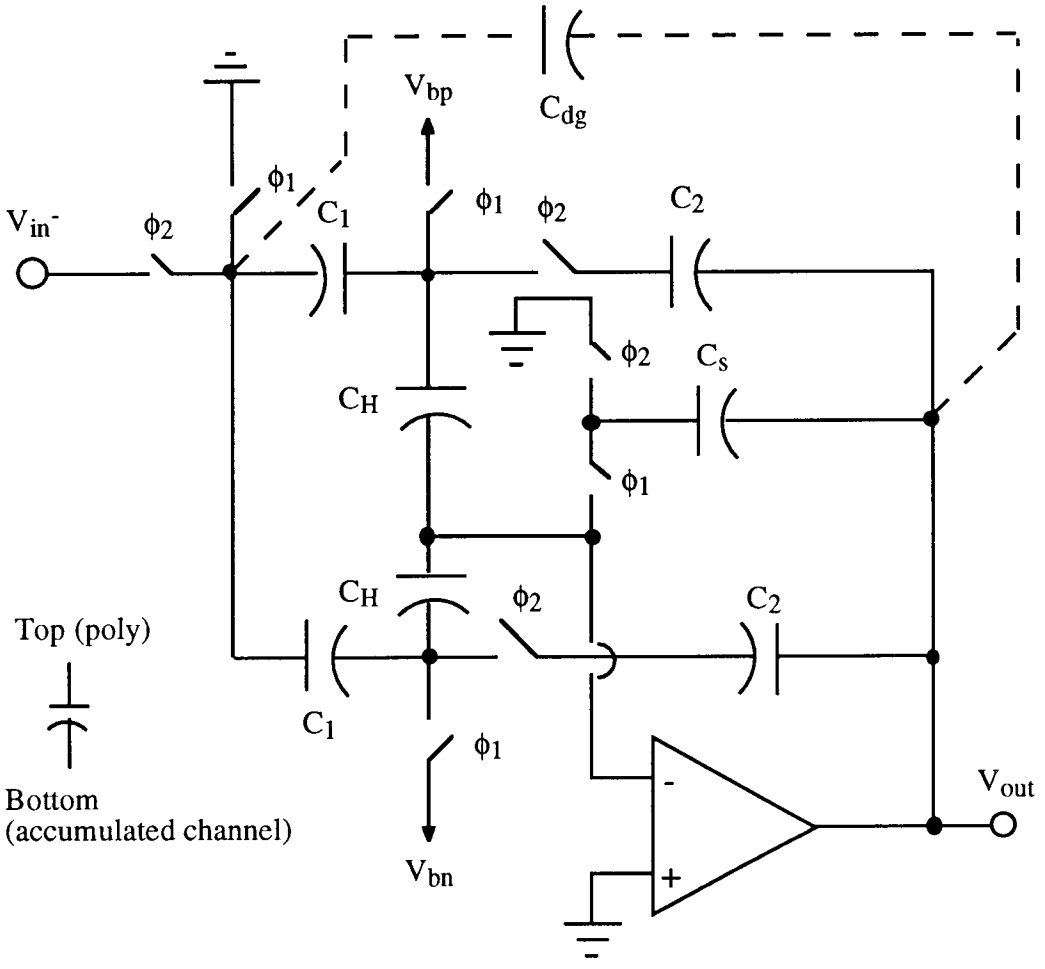


Figure 11.1 SC integrator using parallel compensation

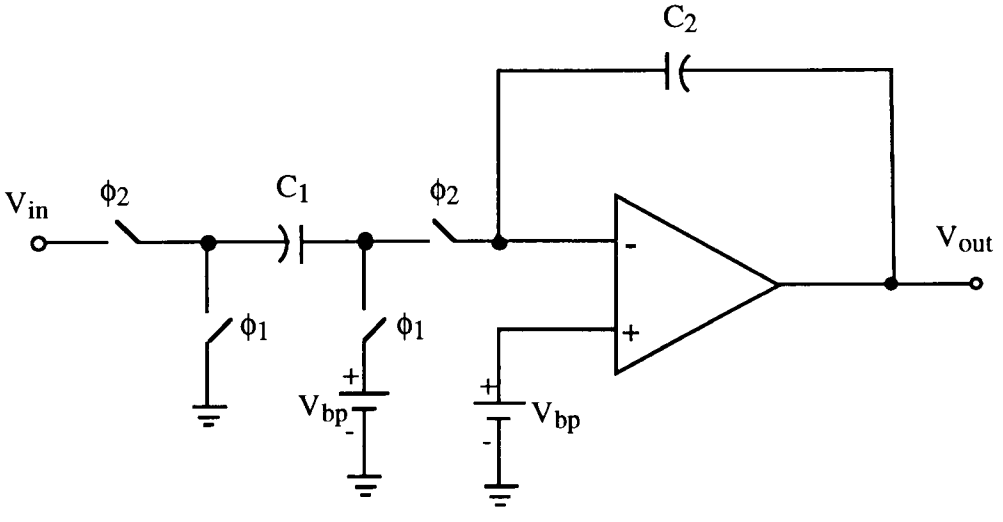


Figure 11.2 SC integrator using a simple biasing arrangement

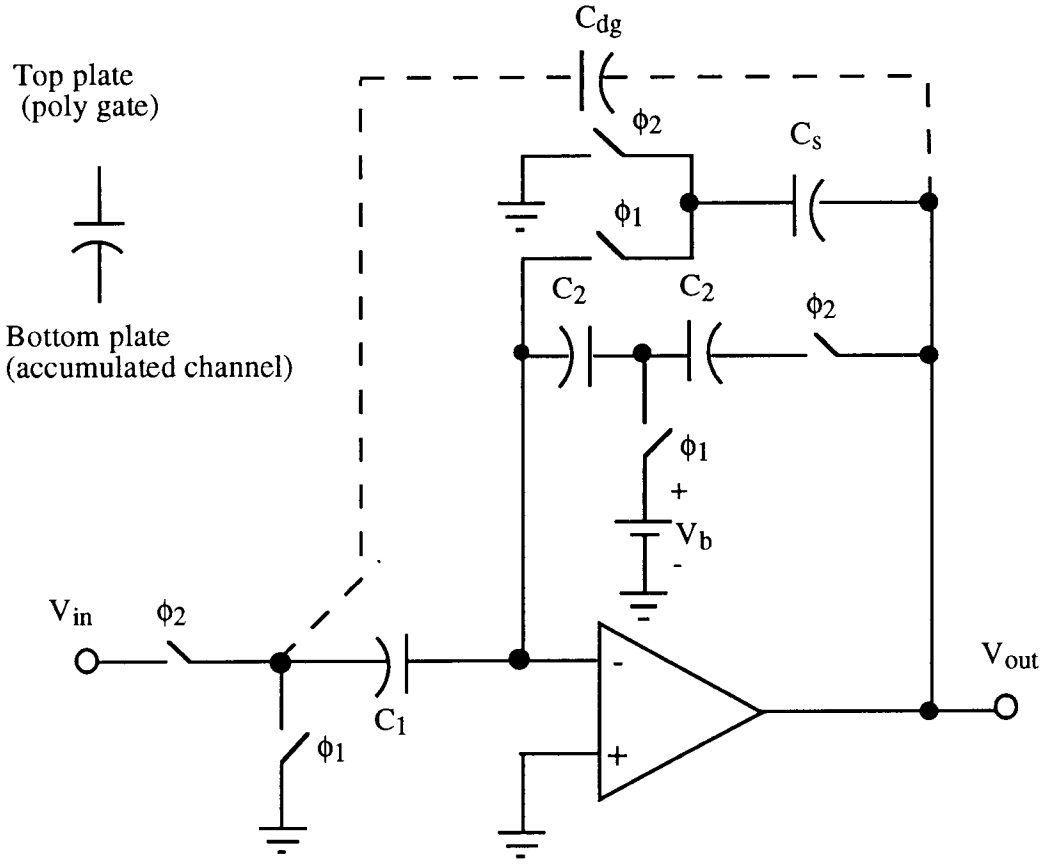


Figure 11.3 SC integrator using series compensation

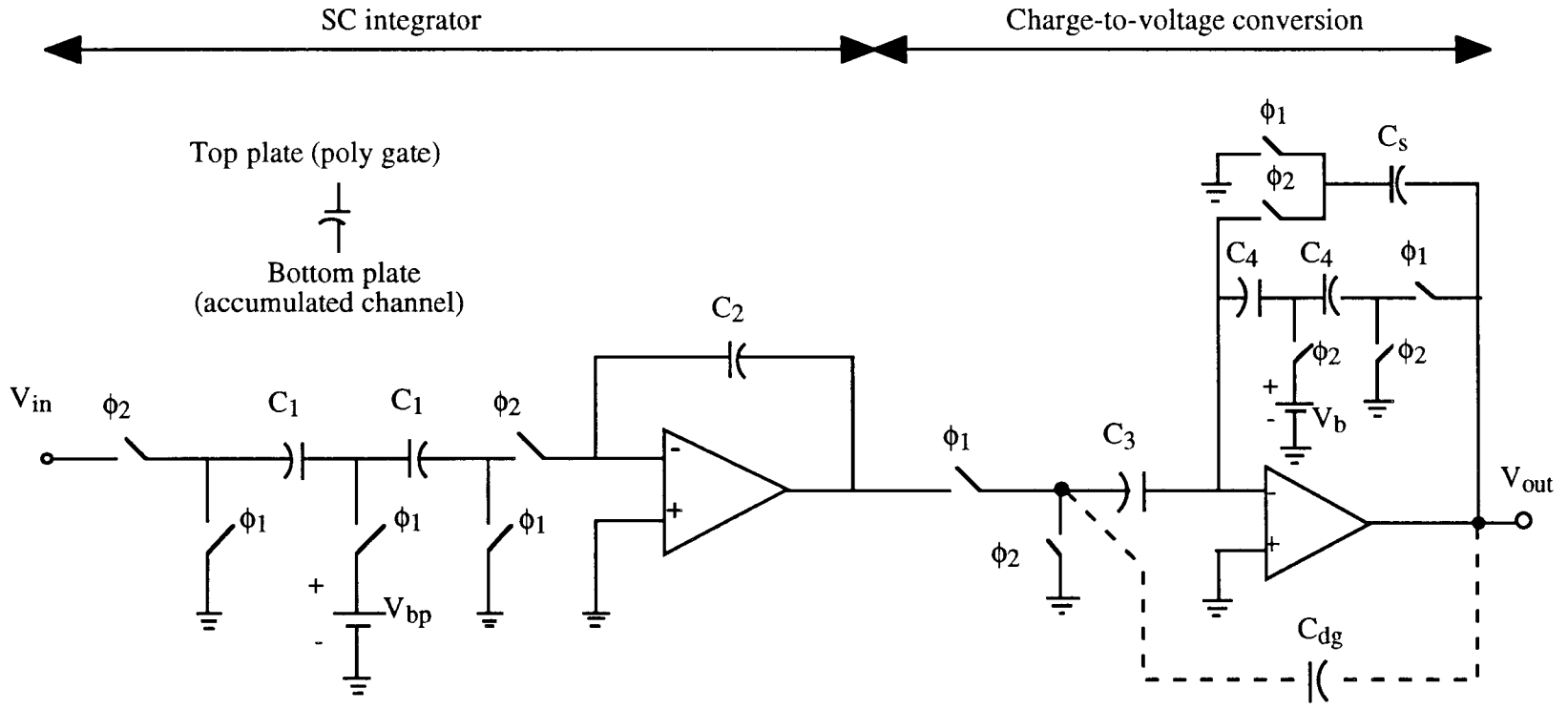


Figure 11.4 SC integrator using series compensation

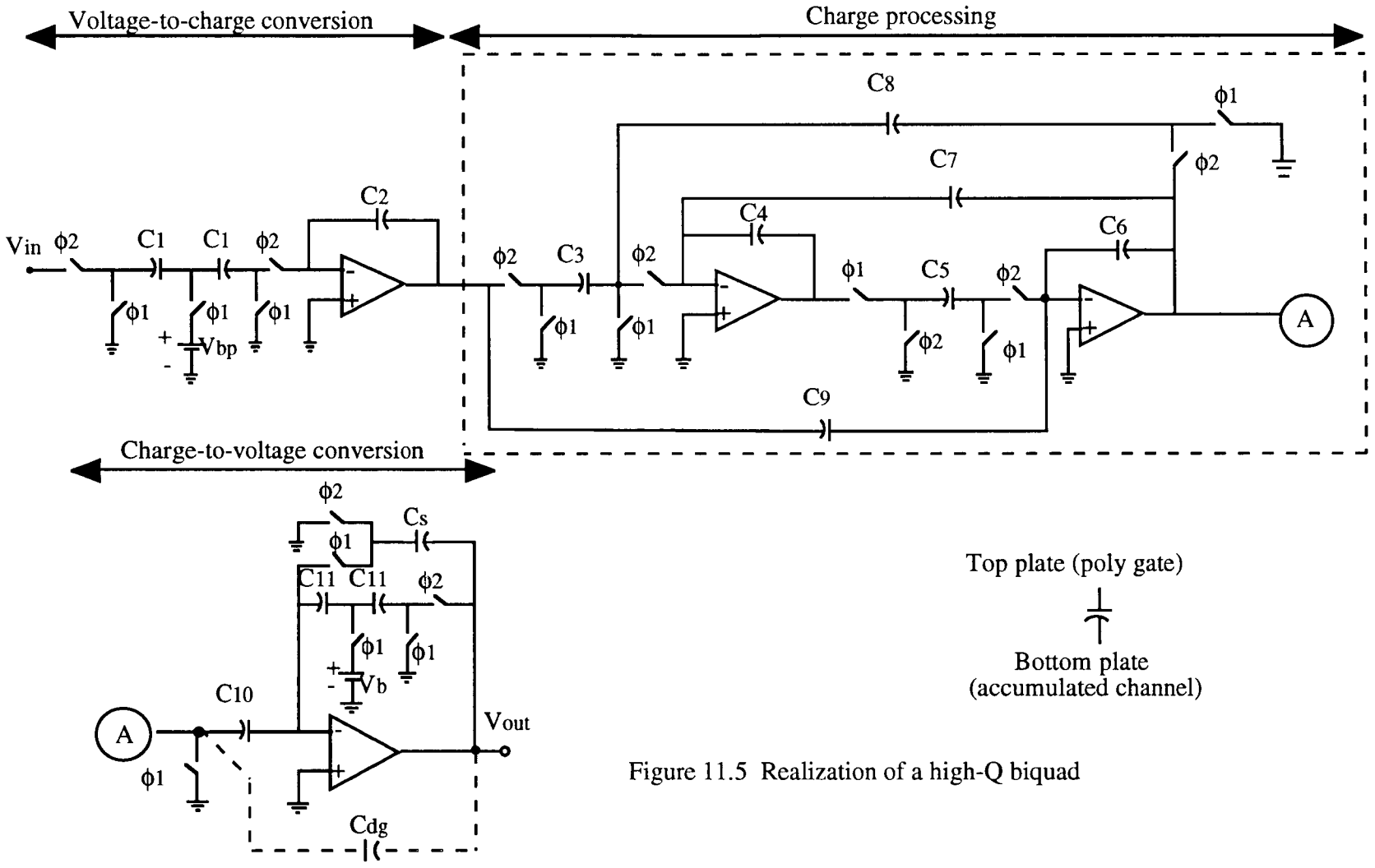


Figure 11.5 Realization of a high-Q biquad

In this configuration, some nonlinear MOSFET capacitors operate in their accumulation region, but some in their depletion region. In the depletion region, capacitance mismatch can affect the performance much more than in the accumulation region, because the voltage coefficient of a MOSFET capacitor |dC/dV| is much larger there.

To reduce the error caused by capacitance mismatch due to a voltage mismatch, a bias voltage may be applied to the feedback capacitors. To make sure that the capacitors operate in their linear region, a negative bias voltage V_{bn} may be applied to the positive input terminal of each op-amp as shown in Figure 11.6, so that all capacitors within the broken line are simply biased*. Note that the feedback capacitors are turned over so that the polarity of the bias voltage across the MOSFET capacitors associated with their bottom plates becomes positive. In this configuration, the bottom plates of MOSFET capacitors are connected to the virtual grounds of op-amps. Hence, a fully differential circuit is recommended to suppress common-mode noise coupling from the substrate. A drawback of the circuits shown in Figures 11.4-6 is that they require additional chip area for the V-Q converter and the Q-V converter.

In some applications such as in delta-sigma modulators, the V-Q converter may not be necessary due to the presence of a comparator. Huang realized a delta-sigma modulator with a S/THD ratio of 94 dB by combining series compensation and charge processing [40] [41].

When all input branches of a filter contain only switched capacitors (and no unswitched capacitors), i.e., there is no C9 in Figure 11.5, they can be replaced by a series compensated SC branch as illustrated in Figure 11.7. Hence, the voltage-to-charge conversion can be combined with the front end of the filter, and the chip area needed for the voltage-to-charge conversion can be saved.

Many other applications of the compensation techniques introduced in this work may exist. It is hoped that they will be explored by future researchers.

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* If a positive bias voltage V_{bp} is applied instead of V_{bn}, it is harder to keep the series-connected input capacitors in their accumulation regions.

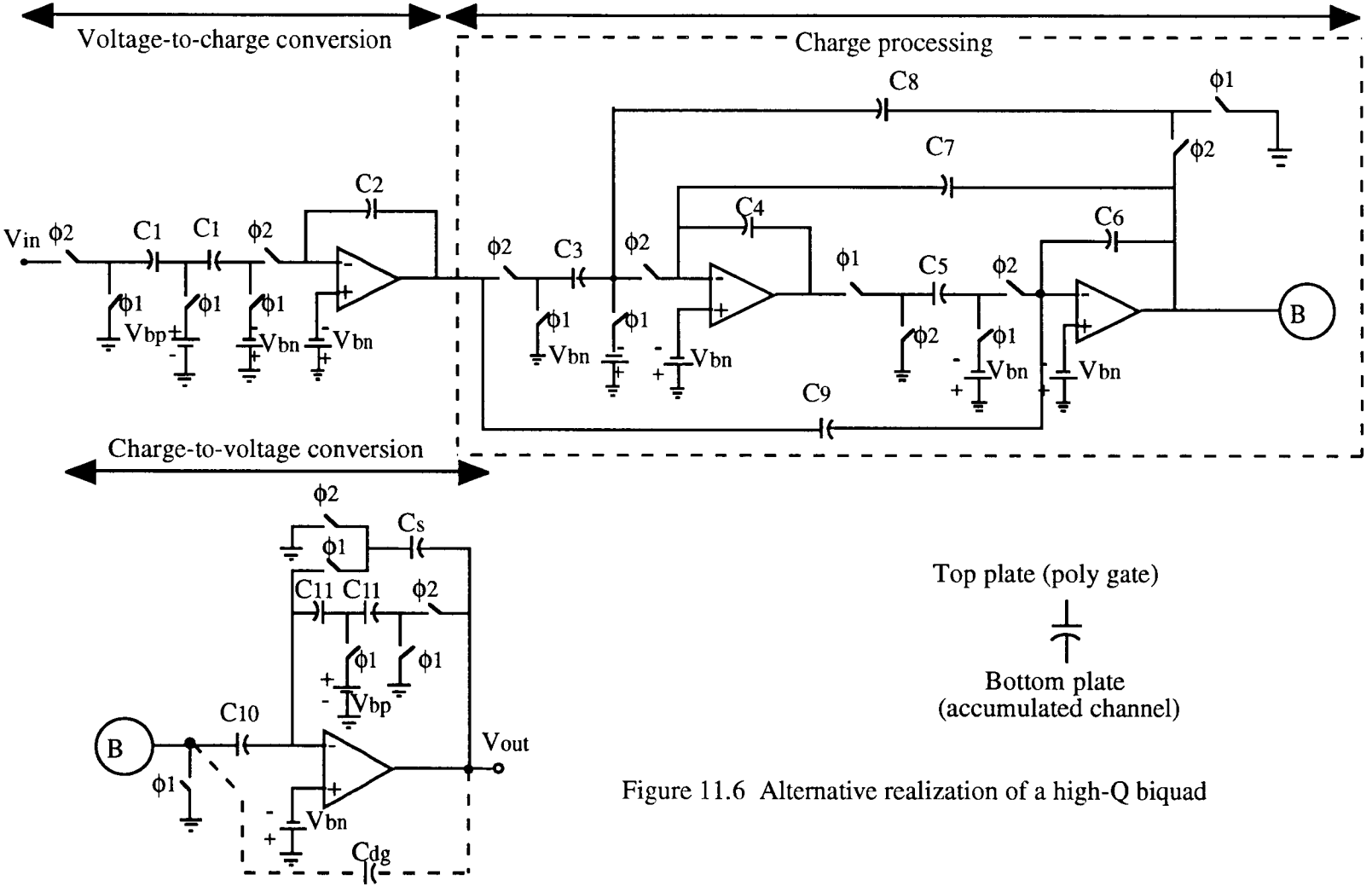

Figure 11.6 Alternative realization of a high-Q biquad

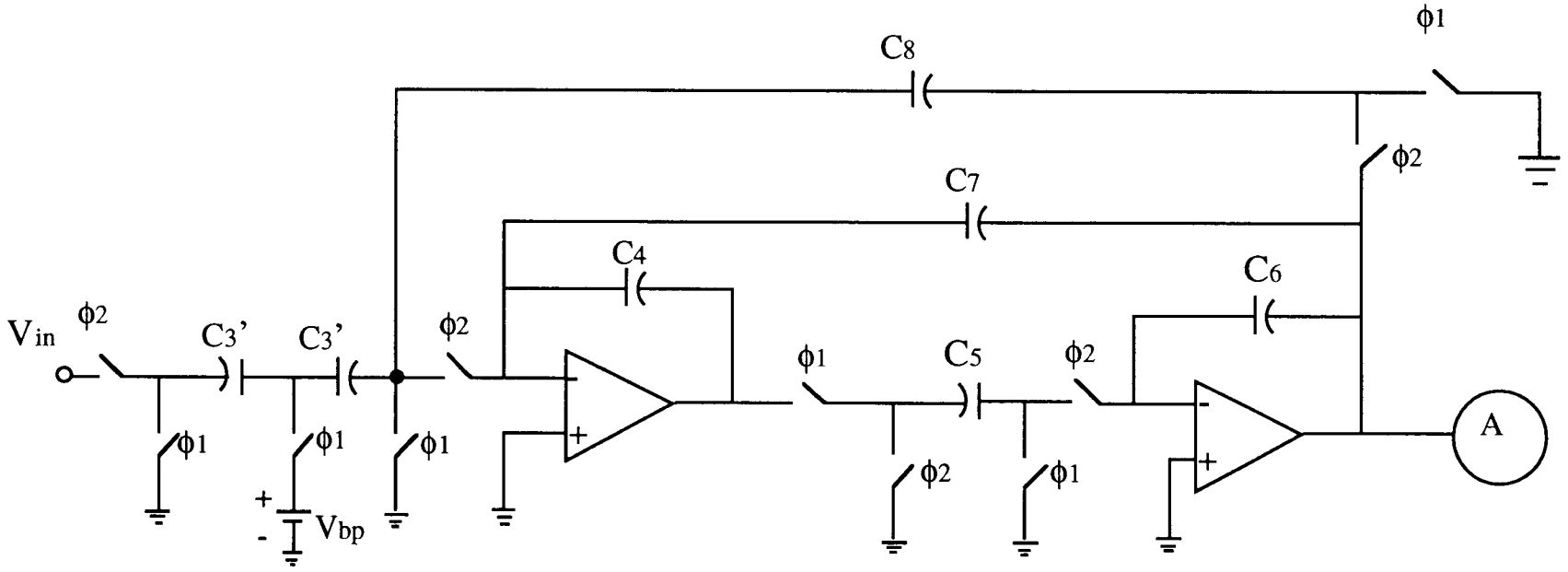

Figure 11.7 An input branch combined with a voltage-to-charge converter using series compensation

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APPENDIX

APPENDIX

SPICE Parameters for the Simulations Performed in this Thesis

```
.MODEL  n       NMOS
+(Level = 2     UO = 521.3      VTO  = 0.9175     NFS  = 5.9984E11
+ TPG = 1       TOX= 225E-10    NSUB = 5.7E16     UCRIT= 5.0E4
+ UEXP = 8.5652E-2              VMAX = 4.953E4    RSH  = 349.7
+ XJ = 3.0E-7   LD  = 2.029E-7  DELTA= 5.281
+ PB = 0.8      JS = 1.0E-5     NEFF = 3.09735    WD   = 2.2278E-7
+ CJ = 5.56037E-4                MJ   = 4.349E-1   CJSW = 3.73283E-10
+ MJSW = 3.4355E-1               CGSO = 3.1E-10    CGDO = 3.1E-10
+ CGBO = 3.4E-10                 FC   = 0.5        XQC  = 1.0 )

.MODEL  p       PMOS
+(Level = 2     UO = 167.6      VTO  =-0.9153     NFS  = 6.5023E11
+ TPG = -1      TOX= 225E-10    NSUB = 3.67E16    UCRIT= 1.0E4
+ UEXP = 9.9314E-2              VMAX = 2.8585E4   RSH  = 418.2
+ XJ = 3.0E-7   LD  = 7.093E-8  DELTA= 2.146
+ PB = 0.8      JS = 1.0E-5     NEFF = 0.93116    WD   = 4.082E-7
+ CJ = 4.4864E-4                MJ   = 4.039E-1   CJSW = 4.57E-10
+ MJSW = 3.344E-1               CGSO = 1.08E-10   CGDO = 1.08E-10
+ CGBO = 6.25E-10        FC  = 0.5     XQC  = 1.0 )
```