AN ABSTRACT OF THE DISSERTATION OF

Ruoxin Jiang for the degree of Doctor of Philosophy in Electrical & Computer Engineering presented on July 30, 2001.

Title: Design of a 1.8-V 14-bit $\Delta - \Sigma$ A/D Converter with 8X Oversampling and 4 MHz Nyquist Output Rate.

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Terri S. Fiez

In this dissertation, a new $\Delta\Sigma$ A/D converter is presented that is ideally suited for communication applications. It is based on a single-loop single-stage structure, which can realize a high maximum out-of-band quantization noise gain while maintaining stable operation and thus achieve 14-bit resolution at 8 times oversampling. A fifth-order $\Delta\Sigma$ analog-to-digital converter (A/D) has been designed and tested in a 0.18 μm CMOS process. This is the first single-stage $\Delta\Sigma$ A/D converter reported in the literature that achieves 14-bit resolution at 4 MHz equivalent Nyquist rate with a 1.8-V power supply.

Design of a 1.8-V 14-bit $\Delta - \Sigma$ A/D Converter with 8X Oversampling and 4 MHz Nyquist Output Rate

by

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1. INTRODUCTION

1.1. Motivation

The idea of delta-sigma ($\Delta\Sigma$) modulation emerged long before it was practical for integrated circuit implementation [1]. In the late 1980's, the rapid advances in VLSI technologies made $\Delta\Sigma$ modulators the most attractive way of implementing high resoultion low to medium speed A/D converters. Unlike conventional Nyquist-rate A/D converters, $\Delta\Sigma$ A/D converters can achieve 16-bit or higher resolution without imposing stringent requirements on device matching [2] .

In recent years, high speed data communications have become one of the most promising applications for the IC industry. High speed data communications, such as xDSL, require high resolution and wideband A/D converters with high dynamic range and high linearity. $\Delta\Sigma$ A/D converters can achieve high dynamic range and high linearity more readily than Nyquist-rate A/D converters such as pipelined and two-step A/D converters. In these applications, the typical *oversampling ratio* (OSR) of $\Delta\Sigma$ A/D converters varies from 32 to 256. To achieve wide bandwidth, the oversampling ratio must be reduced. Reducing the oversampling ratio will lead to a significant reduction in the *signal-to-noise ratio* (SNR). Thus, with the existing

design approaches for $\Delta\Sigma$ A/D converters, both high bandwidth and high resolution are not feasible.

Many low oversampling $\Delta\Sigma$ A/D converters have been reported [3], [4], [5], [6]. These A/D converters have up to 1.25MHz input signal bandwidth. In [3], a 2-0 MASH structure is used. The first stage is a second-order $\Delta\Sigma$ modulator with a 5-bit quantizer. The second stage is a 10-bit pipelined A/D converter with correction logic. The chip consumes 550mW with 5V power supply. And the total die size is 5.7 X 6.2 mm^2. To achieve wide bandwidth, the chip is very complex and requires excessive die area. The complexity and large area make $\Delta\Sigma$ A/D converters less attractive than Nyquist converters, because Nyquist A/D converters can achieve similar specifications with similar area and power consumption [38]. Thus, it is very important to find a simple and robust $\Delta\Sigma$ modulator structure, which is capable of implementing high resolution and wide bandwidth with low power dissipation and small die area.

1.2. Dissertation Organization

In this dissertation, the role of *Maximum out-of-band Quantization Noise Gain* ($\|H\|_\infty$) is explored in the design of high bandwidth $\Delta\Sigma$ A/D converters. It is found that high signal-to-noise ratio (SNR) with low oversampling in $\Delta\Sigma$ A/D converters can be achieved by maximizing the $\|H\|_\infty$. To realize this performance, a new $\Delta\Sigma$ modulator structure is developed that directly maps the pole and zero locations to the integrator coefficients. The final implementation is easy to design, insensitive to coefficient variation and achieves the best performance reported to date. This dissertation is organized as follows:

Chapter 2 shows that $\|H\|_\infty$ is a very important paramenter for $\Delta\Sigma$ modulators, especially when the oversampling ratio is low. By increasing $\|H\|_\infty$ from a typical value of between 1.5 and 2 to between 5 and 6, the signal-to-noise ratio of $\Delta\Sigma$ modulators can be increased greatly compared with other $\Delta\Sigma$ modulators with a low $\|H\|_\infty$. The relationships between $\|H\|_\infty$, oversampling ratio, signal band tones and SNR are provided. The minimum $\|H\|_\infty$ for a particular oversampling ratio is given, which shows that Lee's rule [8] is an approximation that is effective for only high oversampling ratios. It is shown that $\|H\|_\infty$ should be greater than 2 to avoid corrupting the *spurious free dynamic range* (SFDR) of $\Delta\Sigma$ modulators, when low oversampling is used.

Chapter 3 is a review of existing low oversampling $\Delta\Sigma$ A/D converters which describes the relationship between the A/D converter topologies and the circuit parameters. By dissecting a typical high-order $\Delta\Sigma$ modulator, it is shown that existing $\Delta\Sigma$ modulators tend to be unstable when $\|H\|_\infty$ goes up even with multi-bit quantizers.

In Chapter 4, a novel $\Delta\Sigma$ structure called a *hybrid structure* is presented. This structure provides a direct mapping from the $\Delta\Sigma$ modulator coefficients to the pole/zero locations of the *noise transfer function* (NTF). This structure can implement a high $\|H\|_\infty$ with very low sensitivity to coefficient variations and can tolerate low DC gain of the opamps. The design methodology of the hybrid $\Delta\Sigma$ modulator is also described in this chapter.

Chapter 5 describes the design of a 1.8-V 14-bit hybrid $\Delta\Sigma$ A/D with 8X oversampling and 2 MHz input signal bandwidth. Design considerations for the front-end integrator, delay blocks, comparators, charge injection, clock timing and digital-to-analog (DAC) performance are discussed in detail. The results of Monte Carlo simulations and the comparison of commonly used dynamic element match-

ing techniques (DEM) in DACs are also provided. Layout design, including the floorplan, cell design and final chip layout, is also included in this chapter.

Chapter 6 shows the measurement results and conclusions of this $\Delta\Sigma$ A/D converter. The chip is tested with a single 1.8 volt power supply and measurement results are provided. This chip achieves 81.63dB SNDR and 103dB SFDR with 8X oversampling in an active die area of 2.86 mm^2. The power dissipation is 102mW for the analog circuitry and 47mW for the digital circuitry. This is the first $\Delta\Sigma$ A/D ever reported that can achieve 14-bit resolution and 2 MHz input signal bandwidth with a single 1.8-V power supply. The results show that the hybrid $\Delta\Sigma$ A/D converter is suitable for high resolution, wide bandwidth applications.

Chapter 7 describes the design of an important block used in analog signal processing: the multiplier. A new double balanced multiplier based on the multi-input floating-gate multiplier is presented [45]. The multiplier is devised to make it suitable for down converting high frequency signals. The harmonic distortion due to systematic errors and random errors is discussed. This chip is fabricated in a 0.35μm double poly triple metal CMOS process. Measurements show that this multiplier achieves 0.25% total harmonic distortion. This linearity is difficult to achieve with conventional multipliers based on the Gilbert six transistor cell. Measurement results show that this multiplier is suitable for use in dual IF receivers.

2. THE INFLUENCE OF MAXIMUM OUT-OF-BAND QUANTIZATION NOISE GAIN ON ΔΣ A/D PERFORMANCE

2.1. Introduction to Quantization Noise of ΔΣ Modulators

A simple first-order ΔΣ modulator is shown in Fig. 2.1. The quantizer is represented by an adder which sums its input signal y and a quantization noise e_i. The variables u, y, v denote the input signal, the quantizer input and the quantizer output, respectively. At time $t = n$, the output v[n] is:

$$v[n] = u[n-1] + (e_i[n] - e_i[n-1]) \tag{2.1}$$

The corresponding Z-domain function is:

$$V = UZ^{-1} + E_i(1 - Z^{-1}) \tag{2.2}$$

The output V is a function of input, U, and quantization noise, E_i. The above equation can be expressed as:

$$V = USTF(Z) + E_iNTF(Z) \tag{2.3}$$

where STF(Z) denotes the signal transfer function and NTF(Z) denotes the quantization noise transfer function. In this example, STF(Z) is simply a delay. Thus, the input signal is passed to the output after one clock cycle delay. NTF(Z) is a first-order difference function and in the frequency domain, the amplitude response of $NTF(\omega)$ is:

$$|NTF(\omega)| = 2sin(\omega T/2) \tag{2.4}$$

where T is the period of the sampling clock, f_s. When the input signal frequency is much higher than the sampling frequency f_s, the amplitude in (2.4) will be very small at low frequencies. As a result, the baseband quantization noise will be greatly attenuated when high oversampling is used. This filtering of the noise is referred to as *noise shaping.*

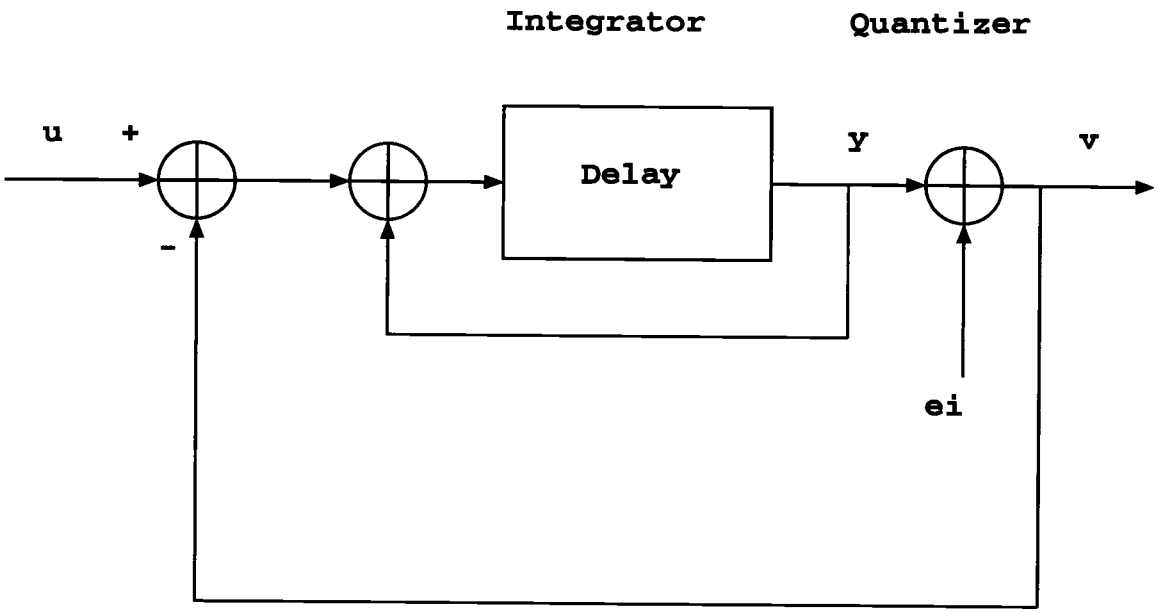


FIGURE 2.1. Block diagram of a first-order $\Delta\Sigma$ modulator.

If we assume the quantization noise is a white gaussian noise, the average quantization noise power is $\frac{\Delta^2}{12}$, where Δ is the least significant bit (LSB) of the quantizer. The output mean square baseband noise power can be obtained by integrating the noise-shaped quantization noise over the baseband:

$$P_N = \int_{-\omega_B}^{+\omega_B} |NTF(\omega)|^2 \frac{\Delta^2}{12\omega_S}\, d\omega \approx (\frac{\pi^2}{3})(\frac{1}{M^3})\frac{\Delta^2}{12},\ M >> 1 \qquad (2.5)$$

where P_N is the mean square noise power, ω_B is the signal bandwidth, $NTF(\omega)$ is the noise transfer function described in (2.4), and $M = \frac{2\omega_B}{\omega_S}$ is defined as the *oversampling ratio.* For a $\Delta\Sigma$ modulator with an N-bit quantizer, the maximum sinusoidal input has an amplitude of $\frac{(2^N-1)\Delta}{2}$. The power of the maximum sinusoidal input is then:

$$P_S = \frac{(2^N-1)^2\Delta^2}{8} \tag{2.6}$$

and the dynamic range (DR) of the first-order $\Delta\Sigma$ modulator with a multi-bit quantizer can be obtained from (2.5) and (2.6) as:

$$DR = \frac{P_S}{P_N} = \frac{3}{2}(\frac{3}{\pi^2})(2^N-1)^2M^3, \; M >> 1 \tag{2.7}$$

From (2.7), it can be seen that every doubling of the oversampling ratio, M , will result in 9 dB (i.e. 1.5 bit) dynamic range increase compared with 6 dB dynamic range increase that can be observed in Nyquist rate A/D converters. Thus increasing the oversampling ratio M is an effective way of increasing the dynamic range.

A second-order $\Delta\Sigma$ modulator is shown in Fig. 2.2. Similar to the first-order $\Delta\Sigma$ modulator, the output V is:

$$V = UZ^{-1} + E_i(1-Z^{-1})^2 \tag{2.8}$$

The noise transfer function is a second-order difference. The corresponding amplitude response of the noise transfer function is:

$$|NTF(\omega)| = (2sin(\omega T/2))^2 \tag{2.9}$$

The dynamic range of the second-order $\Delta\Sigma$ modulator is:

$$DR = \frac{3}{2}(\frac{5}{\pi^4})(2^N-1)^2M^5, \; M >> 1 \tag{2.10}$$

Comparing (2.10) with (2.7), we see that, for a second-order $\Delta\Sigma$ modulator, each doubling of M results in 15 dB increase (i.e., 2.5 bit) in dynamic range. Thus, increasing the order of a $\Delta\Sigma$ modulator is another effective way to increase the dynamic range.

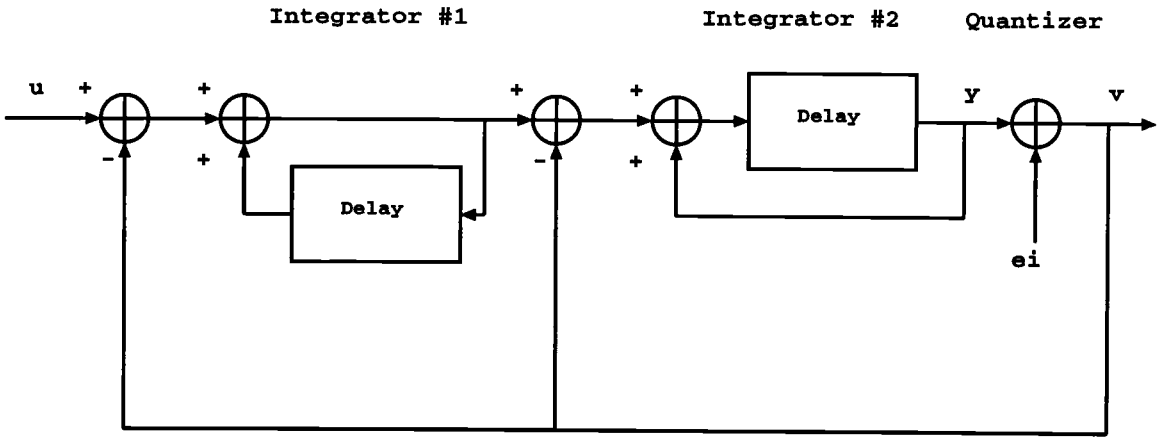


FIGURE 2.2. Block diagram of a second-order $\Delta\Sigma$ modulator.

The topology of an L-th order $\Delta\Sigma$ modulator is shown in Fig. 2.3. The output V is:

$$V = UZ^{-1} + E_i(1 - Z^{-1})^L \tag{2.11}$$

The above equation shows that the noise transfer function $NTF(Z)$ is an L-th order difference. In the frequency domain, the amplitude of the L-th order noise transfer function is:

$$|NTF(\omega)| = (2sin(\omega T/2))^L \tag{2.12}$$

For an L-th order $\Delta\Sigma$ modulator, each doubling of oversampling ratio M results in approximately $(6L + 3)$ dB dynamic range increase, which is close to

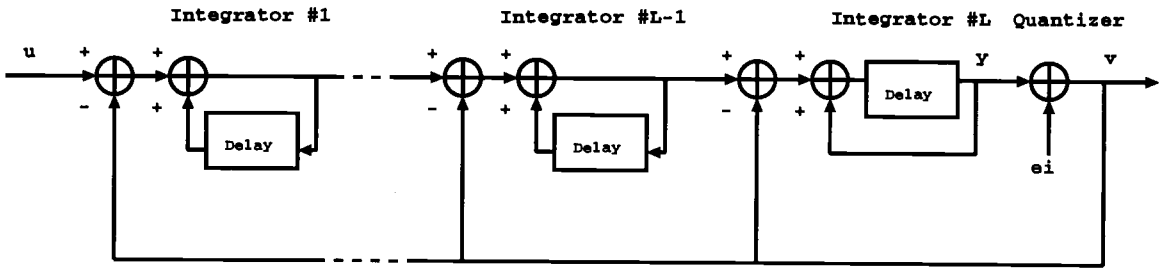


FIGURE 2.3. Block diagram of an L-th order $\Delta\Sigma$ modulator.

$(L + 0.5)$ bit/octave. If L is a large number, the modulator can achieve very high dynamic range with a high oversampling ratio M as shown below.

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 M^{2L+1}, \; M >> 1 \tag{2.13}$$

In Section 2.1, all equations are obtained based on the assumption that the quantization noise is white noise, where the quantization noise is flat over the spectrum. Actually, the characteristics of the quantization noise spectra depends on many factors such as the order of the modulator, input signal amplitude and maximum out-of-band quantization noise gain to name a few. The relationships between them are very complicated, since $\Delta\Sigma$ modulators are virtually non-linear systems. The purpose of this section is to provide an intuitive explanation of these relationships.

For a $\Delta\Sigma$ modulator, an input signal passes through each integrator before it reaches the quantizer input node. After passing through each integrator, the signal is scrambled by signals such as the DAC feedback signals, local feedback signals and feedforward signals. As a result, the output signal will be less correlated with the original input signal. If a high-order $\Delta\Sigma$ modulator is used, the signal will be

scrambled many times. It will become uncorrelated with the original quantizer input signal, and very few if any tones will be detected at the output.

If a low order $\Delta\Sigma$ modulator is employed, the input signal is not scrambled enough before it reaches the quantizer input. Thus the quantizer output code is somewhat correlated with the original input. The quantization noise will have a periodic component whose period is the same as the original input signal. As a result, the output will contain tones in the signal bandwidth due to the correlated quantization noise.

Figure 2.4 is the spectrum of the first-order $\Delta\Sigma$ modulator with a 1-bit quantizer as shown in Fig. 2.1. Due to the simple structure of the first-order $\Delta\Sigma$ modulator, there are very large tones in the baseband frequency (for an oversampling ratio of 128). The spurious free dynamic range (SFDR) is only 55dB. Thus, first-order stages are almost never used for practical applications (excluding the first-order $\Delta\Sigma$ modulators used in MASH $\Delta\Sigma$ A/D converters).

Figure 2.5 is the spectrum of the second-order single bit $\Delta\Sigma$ modulator with an OSR of 128 as shown in Fig. 2.2. It can be seen that the tones are significantly reduced compared with the tones of the first-order $\Delta\Sigma$ modulator. Thus, increasing the order of a $\Delta\Sigma$ modulator can reduce the tones in the signal band.

When the input signal is a DC signal, it will generate some tones, whose amplitude and frequency depend on the amplitude of the DC input. Let's consider the first-order $\Delta\Sigma$ modulator shown in Fig. 2.1. To simplify the problem, we assume the $\Delta\Sigma$ modulator has a 1-bit quantizer and the 1-bit DAC has an output of ± 1 volt. If the DC input signal amplitude is a rational number of the reference voltage, the output may form a periodic pattern that results in tones in the output spectrum.

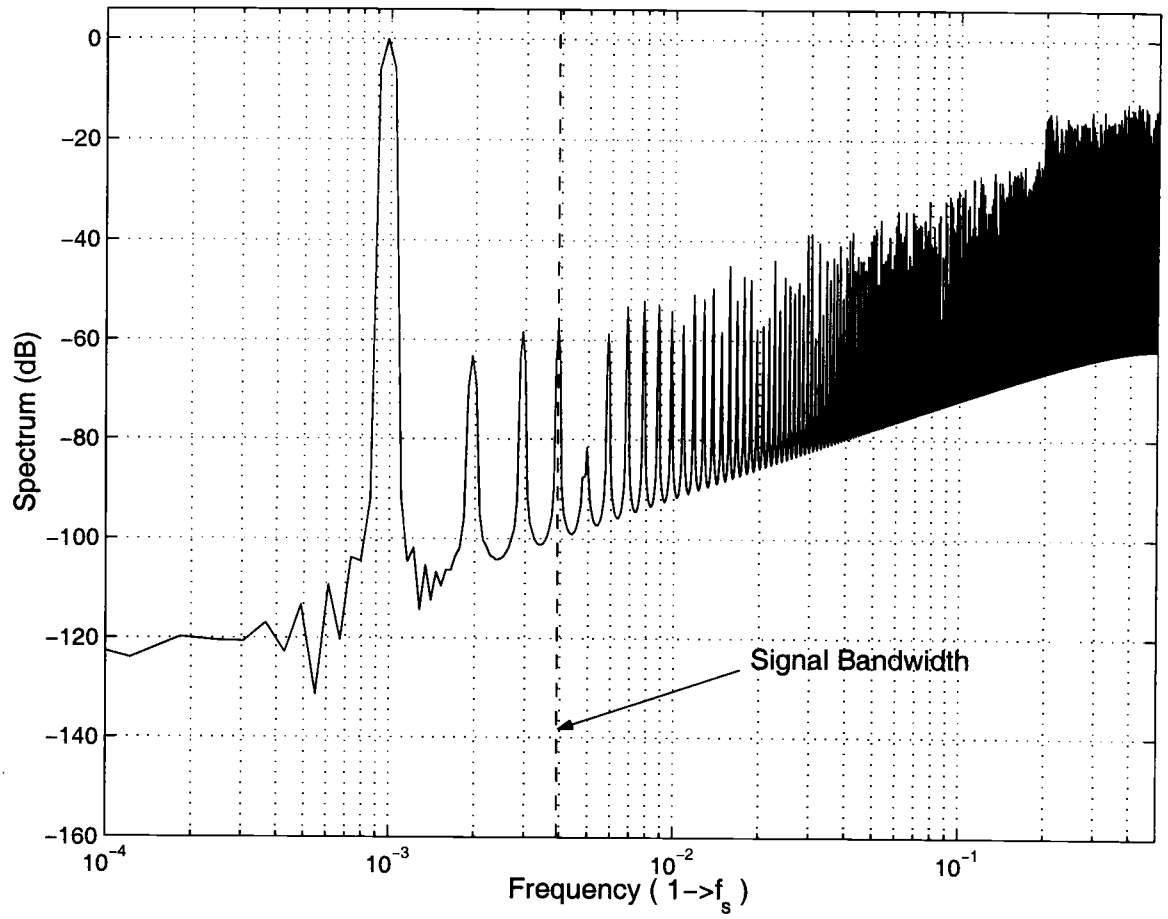


FIGURE 2.4. Spectrum of a first-order $\Delta\Sigma$ modulator with an oversampling ratio of 128.

For example, if the DC input signal is $\frac{1}{16}$ volt, on average there will be 17 (1)'s and 15 (-1)'s for each 32 clock cycles. As a result, tones will appear with a uniform spacing of $\frac{1}{32}f_s$ as shown in Fig. 2.6. The tones are very high in amplitude and the first-order noise shaping is corrupted. This kind of noise is called *pattern noise.* Pattern noise is a particularly serious issue for low order $\Delta\Sigma$ modulators.

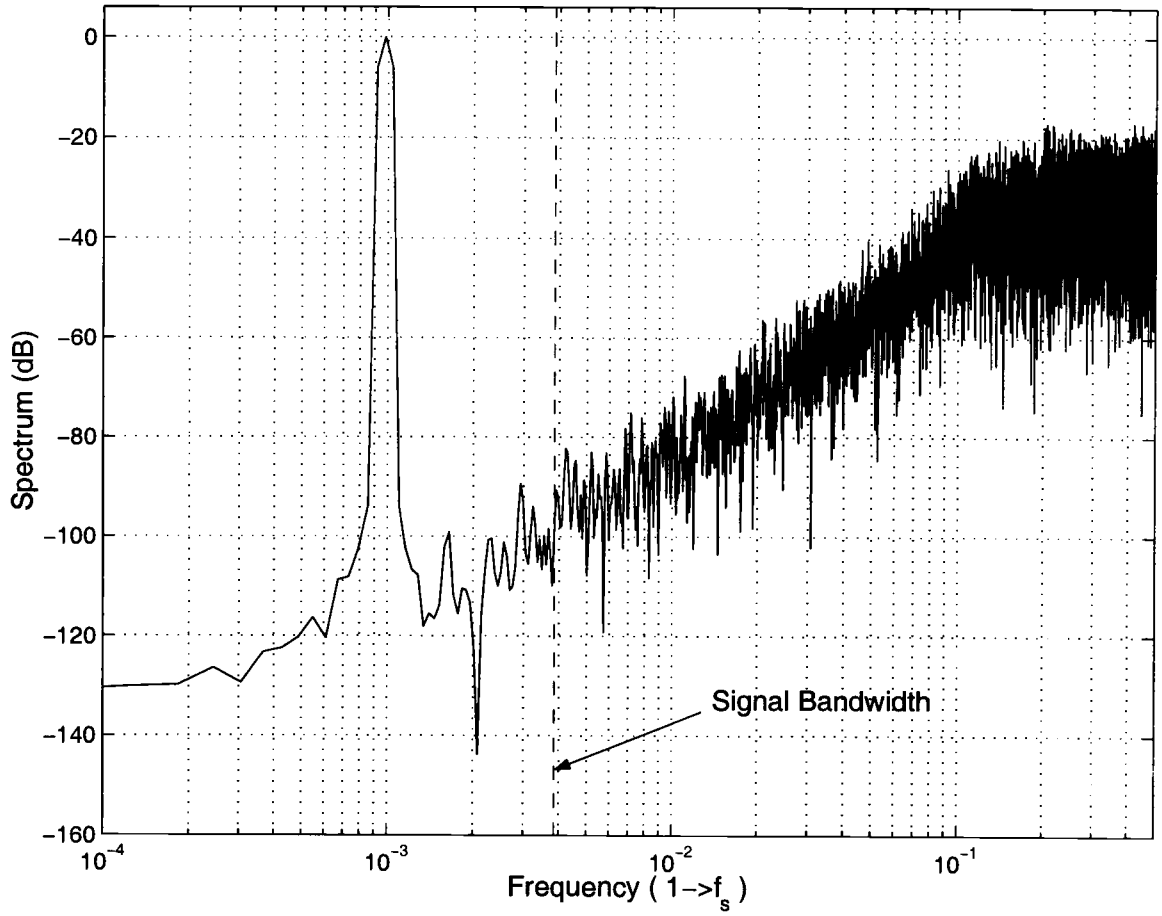


FIGURE 2.5. Spectrum of a second-order $\Delta\Sigma$ modulator with an oversampling ratio of 128.

Maximum out-of-band quantization noise gain ($||H||_\infty$) is also an important parameter of $\Delta\Sigma$ modulators. A high $||H||_\infty$ will amplify out-of-band quantization noise and attenuate signal band quantization noise. But when $||H||_\infty$ is increased, the maximum stable input range will be reduced. For a given $\Delta\Sigma$ modulator, there is an optimum $||H||_\infty$ value for which the modulator can reach the maximum SNR. If $||H||_\infty$ is above this value, the maximum stable input range decreases rapidly and the SNR decreases. On the other hand, if $||H||_\infty$ is less than this value, the

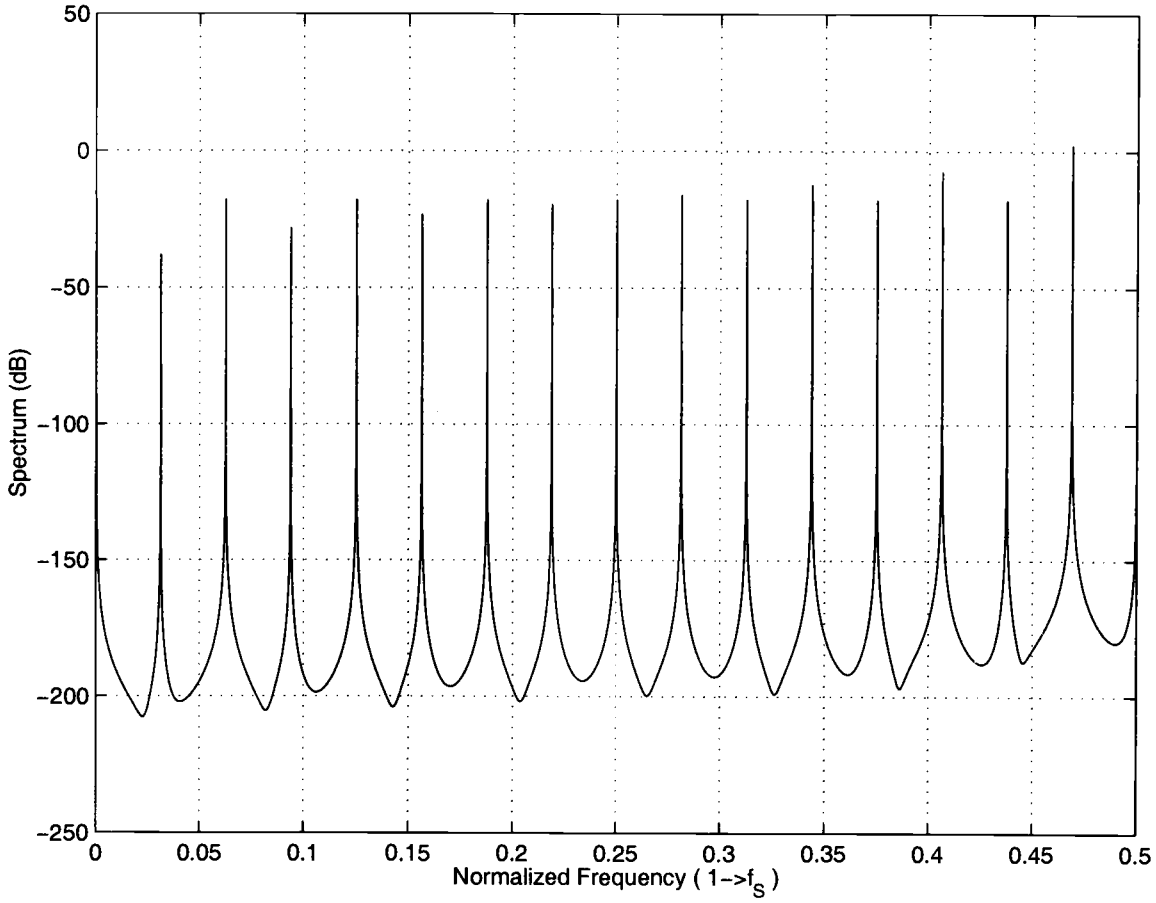


FIGURE 2.6. Pattern noise spectrum of a first-order $\Delta\Sigma$ modulator with a -24dB DC input.

signal band quantization noise shaping becomes worse and the SNR again decreases. When choosing $\|H\|_\infty$, a trade-off must be made between the stability and the aggressiveness of the noise shaping. It has also been observed that a higher $\|H\|_\infty$ can help to reduce the tones in the signal band. $\|H\|_\infty$ has a profound effect on $\Delta\Sigma$ modulators and its influence will be discussed in detail in the next section of this chapter.

2.2. The Relationship Between $\|H\|_\infty$ and $\Delta\Sigma$ Modulator System Performance

In (2.12), it was shown that the L-th order $\Delta\Sigma$ modulator shown in Fig. 2.3 has a maximum out-of-band quantization noise gain of 2^L. If a 1-bit quantizer is used for a high-order $\Delta\Sigma$ modulator, quantization noise can be greatly amplified so that the quantizer is overloaded and the $\Delta\Sigma$ modulator becomes unstable. Thus, $\Delta\Sigma$ modulators with an order of 3 or greater usually use MASH structures to suppress quantization noise power.

The second-order $\Delta\Sigma$ modulator shown in Fig. 2.2 has a $\|H\|_\infty$ of 4. Figure 2.7 is a second-order $\Delta\Sigma$ modulator proposed by B. E. Boser [7]. Compared with the circuit shown in Fig. 2.2, each integrator in this modulator has one clock cycle delay and a -6dB attenuator at the input. The noise transfer function is:

$$NTF(Z) = \frac{(1-Z^{-1})^2}{1-1.5Z^{-1}+0.75Z^{-2}} \tag{2.14}$$

The $\|H\|_\infty$ for (2.14) is 2.3093. By reducing $\|H\|_\infty$ from 4 to 2.3093, the integrator output probability density width is much smaller than that of the modulator shown in Fig. 2.2. The histograms of the two modulators are shown in Fig. 2.8. The modulator proposed by B. E. Boser has a narrower integrator output distribution than the traditional one. This is very important for practical circuit design, since a narrower integrator output distribution implies a wider input signal dynamic range.

The two second-order $\Delta\Sigma$ modulators shown in Figs. 2.2 and 2.7 have a maximum out-of-band quantization noise gain of 4 and 2.3093, respectively, and they are both stable. For higher order $\Delta\Sigma$ modulators, stability is a complicated issue. Lee's rule [8] states that high-order $\Delta\Sigma$ modulators with a 1-bit quantizer

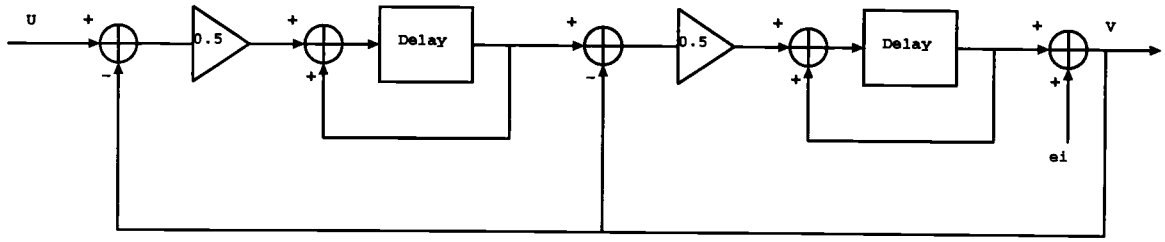


FIGURE 2.7. A second-order $\Delta\Sigma$ modulator proposed by B. E. Boser.

must have a $\|H\|_\infty$ less than 2 to remain stable. This rule of thumb is derived from simulations and is verified by practical designs [10] [12]. In high-order single stage $\Delta\Sigma$ modulator designs, typically $\|H\|_\infty$ varies from 1.5 to 2.0.

The quantizers of $\Delta\Sigma$ modulators are highly non-linear due to their discrete output levels and are overloaded if the input signal is too large. This provides a reasonable guide for high oversampling $\Delta\Sigma$ A/D converters.

To estimate the stability of $\Delta\Sigma$ modulators, a linear model with a variable gain can be used [13]. If we assume the quantizer gain is unity, a $\Delta\Sigma$ modulator can be represented by the block diagram shown in Fig. 2.9. In this figure, the loop filter has two inputs and the output, Y, is a function of input signal, U, and quantizer output, V.

$$Y(Z) = L_0(Z)U(Z) + L_1(Z)V(Z) \tag{2.15}$$

The quantizer output, $V(Z)$, can also be expressed as a function of the input, $U(Z)$, and the quantization noise, $E(Z)$.

$$V(Z) = G(Z)U(Z) + H(Z)E(Z) \tag{2.16}$$

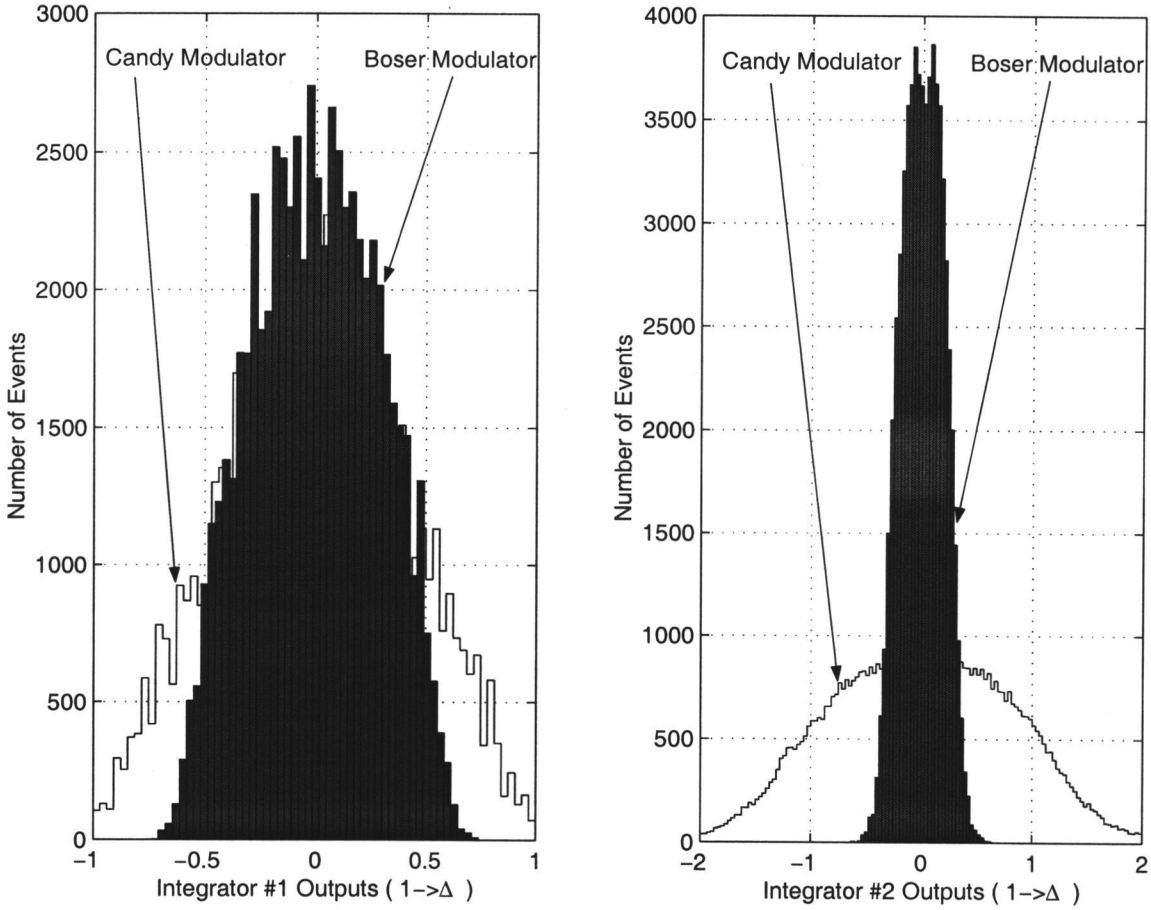


FIGURE 2.8. Comparison of integrator output histograms for the traditional and the Boser architecture with sinusoidal input 3dB below overload.

where $G(Z)$ and $H(Z)$ are the *signal transfer function* (STF) and *noise transfer function* (NTF), respectively. The relationship between $G(Z)$, $H(Z)$, L_0 and L_1 is:

$$L_0(Z) = \frac{G(Z)}{H(Z)} \tag{2.17}$$

$$L_1(Z) = \frac{H(Z)-1}{H(Z)} \tag{2.18}$$

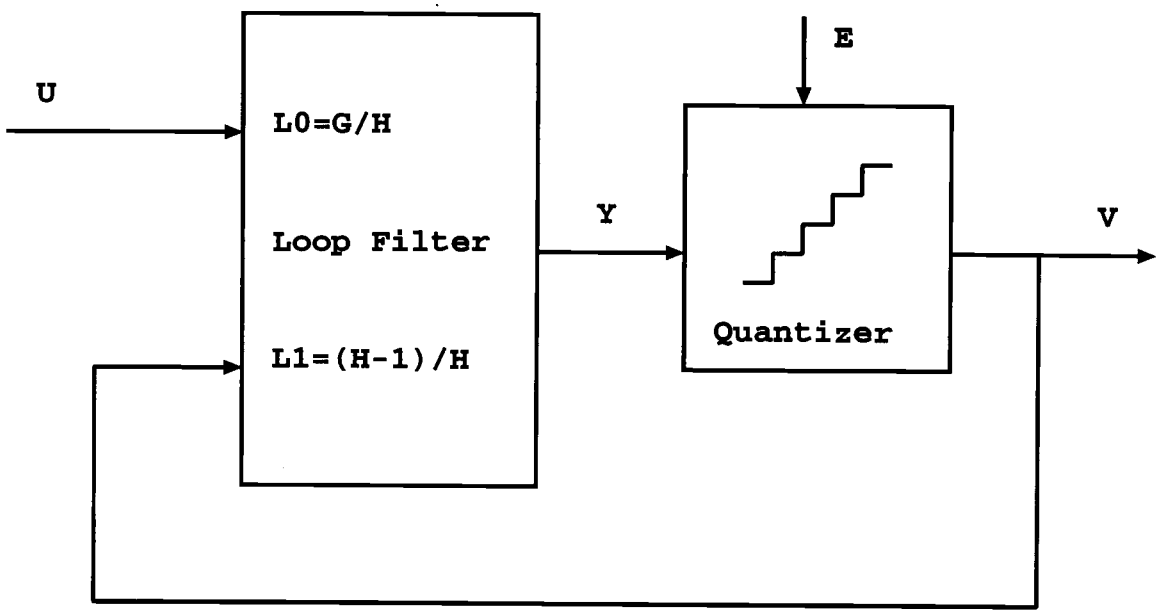


FIGURE 2.9. Block diagram of a $\Delta\Sigma$ modulator.

The above linear model has a major drawback in that it assumes the quantization noise, $E(Z)$, is not correlated with the input signal, $U(Z)$. As discussed in Section 2.1, quantization may be correlated to the input signal. To take this into account, a variable gain block is used to represent the quantizer gain as shown in Fig. 2.10. For this model, the output, $V(Z)$, can be expressed as:

$$V(Z) = G'(Z)U(Z) + H'(Z)E'(Z) \tag{2.19}$$

where

$$E'(Z) = V(Z) - KY(Z) \tag{2.20}$$

$$G'(Z) = \frac{KG(Z)}{K+(1-K)H(Z)} \tag{2.21}$$

$$H'(Z) = \frac{H(Z)}{K+(1-K)H(Z)} \tag{2.22}$$

Equation (2.22) is the *noise transfer function* (NTF) of this model. In order to make the new model more accurate than the previous model, we must choose the variable gain K such that the quantization noise, $E(Z)$, and the signal component, $V(Z)$, are uncorrelated. This effect makes the quantization noise and the input signal uncorrelated. The optimum K that satisfies this condition is:

$$K_{opt} = \frac{covariance(y,v)}{variance(y,y)} \tag{2.23}$$

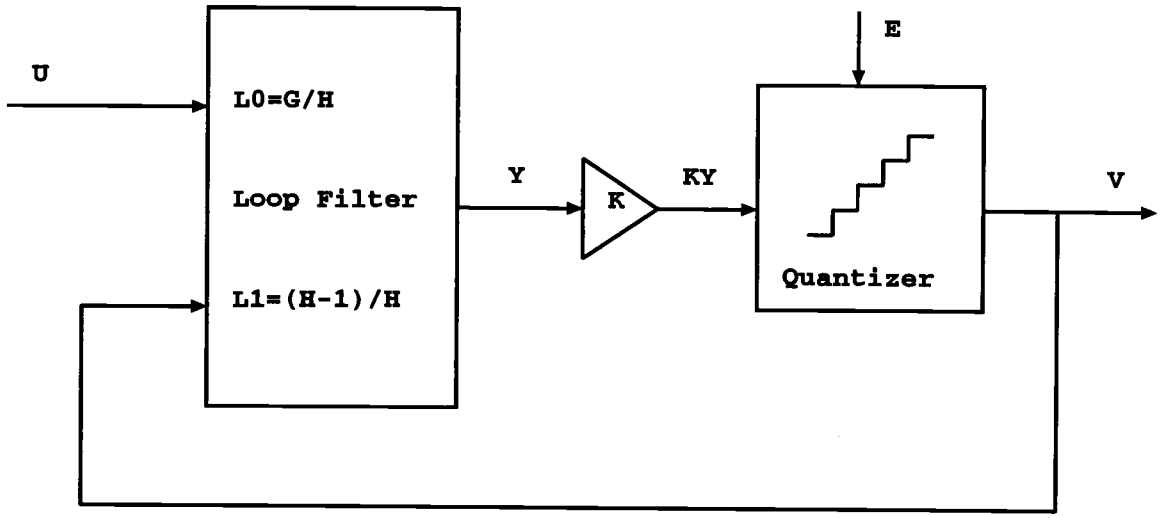


FIGURE 2.10. Block diagram of a $\Delta\Sigma$ modulator with a variable gain.

The quantizer gain depends on the modulator structure and the input signal amplitude. As the gain varies, the loop gain also varies, which causes the NTF poles to move. If the NTF poles move out of the unit circle, the quantizer will not be able to bring the modulator output back into the unit circle and the modulator becomes unstable. From (2.23), when the quantizer input y has a very large amplitude, the gain K will drop. A large signal y implies a large input signal u. Thus, $\Delta\Sigma$ modulators can be unstable if the input signal amplitude is too large. Figure 2.11

shows the NTF root locus of a third-order $\Delta\Sigma$ modulator. When K is less than the critical value 0.296, the poles are outside of the unit circle and the modulator becomes unstable.

Since the signal y is also a function of the quantization noise, stability also depends on quantization noise. If a $\Delta\Sigma$ modulator has a high $\|H\|_\infty$, the quantization noise will be amplified and fed back to the loop filter. This will result in a large signal y. If y is large enough to reduce the quantizer gain K below a certain value, the modulator can be unstable. If the $\Delta\Sigma$ modulator has a high $\|H\|_\infty$, it can be unstable even when the input signal amplitude is very small. Thus $\|H\|_\infty$ is very critical in terms of modulator stability. For this reason, the $\|H\|_\infty$ of high order $\Delta\Sigma$ modulators is typically chosen in the range of 1.5 to 2.

The two $\Delta\Sigma$ modulators shown in Fig. 2.2 and Fig. 2.7 have $\|H\|_\infty$ of 4.0 and 2.3093, respectively, and they are both stable. The corresponding root loci are shown in Fig. 2.12. When quantizer gain, K, approaches zero, the poles are still inside the unit circle and consequently, the modulators are always stable even when $\|H\|_\infty$ is as high as 4.

As previously shown, $\|H\|_\infty$ is an important factor in determining the $\Delta\Sigma$ modulator stability. To maintain stability, high order $\Delta\Sigma$ modulators with a 1-bit quantizer must have a maximum out-of-band quantization noise gain less than 2. Equation (2.13) demonstrates that $\|H\|_\infty$ has little or no bearing on the dynamic range of the $\Delta\Sigma$ modulator.

Lee's rule is appropriate for high order $\Delta\Sigma$ modulators with a 1-bit quantizer. If a multi-bit quantizer is used, quantization noise power will decrease. As a result, $\|H\|_\infty$ can be increased without compromising the stability of the $\Delta\Sigma$ modulator.

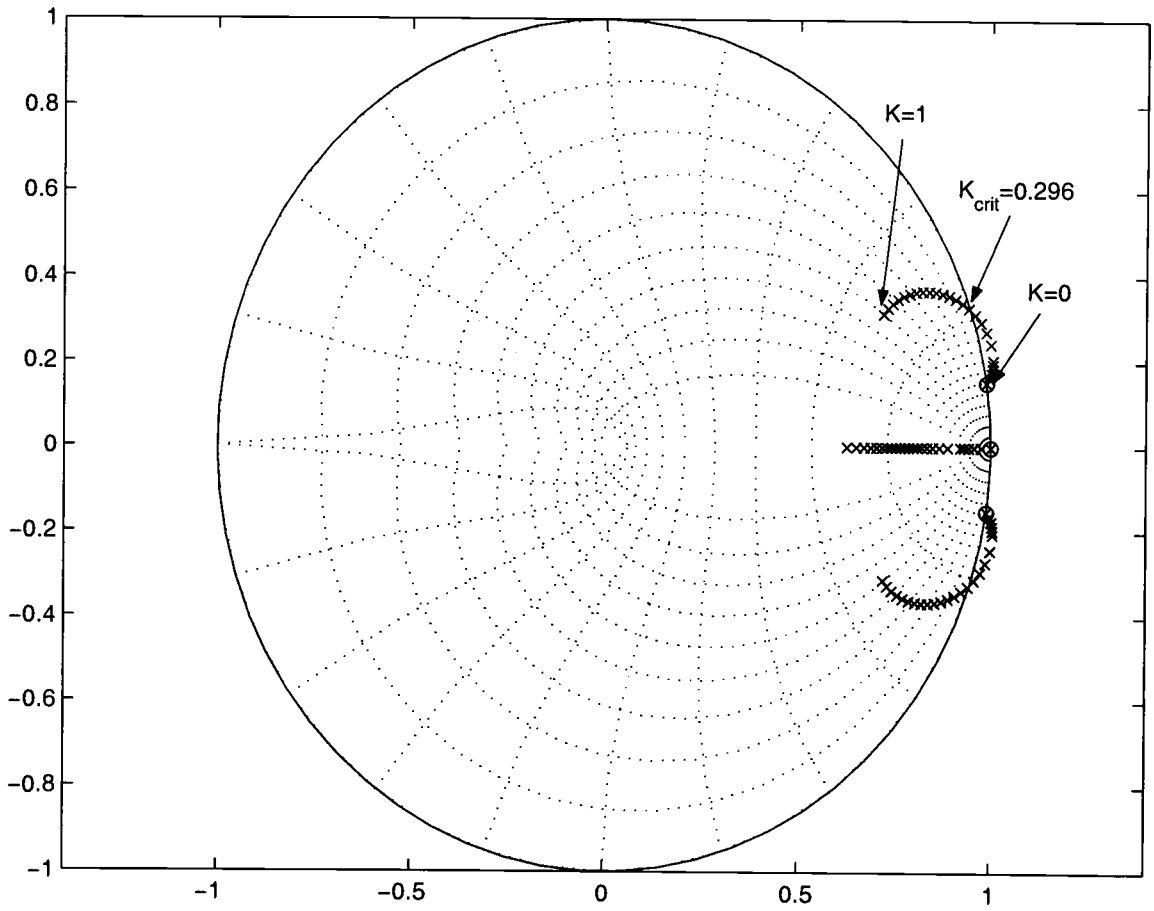


FIGURE 2.11. NTF root locus of a third-order $\Delta\Sigma$ modulator.

The influence of $||H||_\infty$ on $\Delta\Sigma$ modulators has been explored using state space simulation [11]. When the modulator has a multi-bit quantizer, it is likely that the state space simulation is stable with a high $||H||_\infty$. However, when the implementation of a high-order single-stage multi-bit $\Delta\Sigma$ modulator with a $||H||_\infty$ much higher than 2 is considered, it is found that nearly all existing high-order $\Delta\Sigma$ modulators become unstable. Thus, many implementations of high-order single-stage $\Delta\Sigma$ modulators with a multi-bit quantizer have a $||H||_\infty$ of approximately 2.

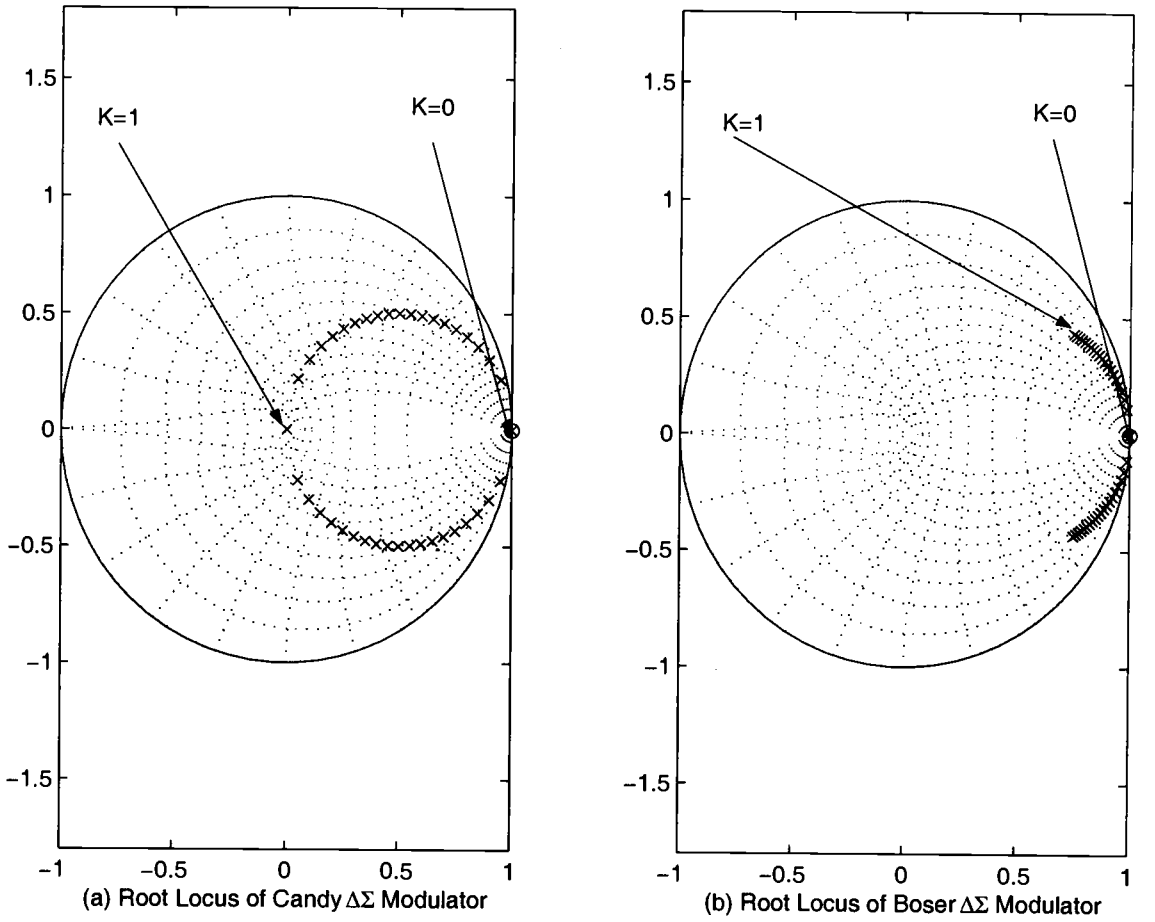


FIGURE 2.12. NTF root loci of two second-order modulators, (a) Candy modulator with $\|H\|_\infty$ =4 and (b) Boser modulator with $\|H\|_\infty$ =2.3.

To illustrate this, consider the noise transfer function shown in Fig. 2.13 of the fourth-order $\Delta\Sigma$ A/D with a 4-bit quantizer in [14]. Although the NTF peaks at 3.1886, a large portion of the NTF is less than 2 and the average out-of-band NTF is close to 2. This $\Delta\Sigma$ modulator has a 16X oversampling ratio and achieves 14-bit resolution with a 250 kHz input signal bandwidth. The dynamic range estimated by (2.13) is 103.4 dB while the measured dynamic range is 84 dB.

The dashed curve in Fig. 2.13 shows the NTF of a fifth-order $\Delta\Sigma$ modulator with a 4-bit quantizer. It has an 8X oversampling ratio and $\|H\|_\infty$ =6. Since the NTF curve is smooth and there is no peaking, the average out-of-band quantization noise gain is very close to the maximum $\|H\|_\infty$. The dynamic range estimated by (2.13) is 85.3 dB and the measured dynamic range is 83dB.

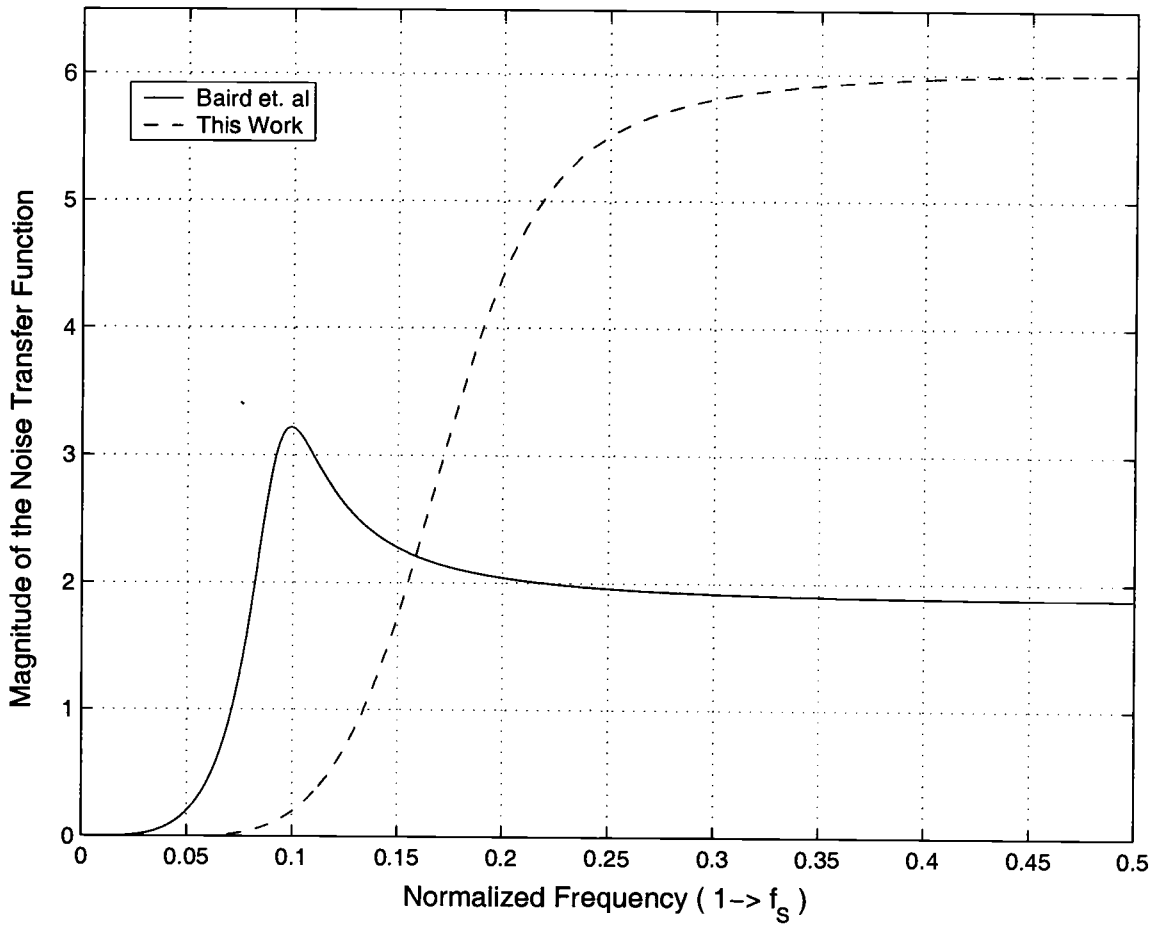


FIGURE 2.13. Comparison of two noise transfer functions, The solid line is for a 4th order $\Delta\Sigma$ modulator with a 4-bit quantizer and the dotted line is for a 5th order modulator with a 4-bit quantizer.

When $\|H\|_\infty$ is high, it can boost the signal-to-noise ratio of a $\Delta\Sigma$ modulator. The noise transfer function can be written as:

$$NTF(Z) = A\frac{\prod_i(Z-a_i)}{\prod_j(Z-b_j)} \tag{2.24}$$

where A is the coefficient, a_i and b_j are the NTF zeros and poles. A higher out-of-band quantization noise gain can be achieved by moving the poles toward the $Z = -1$ point in a Z-plane (i.e., the $\frac{\omega_s}{2}$ point in the frequency domain). This means the poles are away from the $Z = 1$ point (i.e., the DC point in the frequency domain) and the baseband quantization noise can be suppressed.

Figure 2.14 shows two fifth-order noise transfer functions with $\|H\|_\infty$ of 1.5 and 6, respectively. For the noise transfer function with a low $\|H\|_\infty$, the poles are close to the $Z = 1$ point and the baseband noise shaping is below 0.3891. If $\|H\|_\infty$ is increased to 6, the NTF poles are far away from the $Z = 1$ point, which results in aggressive noise shaping. The maximum out-of-band quantization noise gain is 6 and the baseband magnitude is below 0.0033. Thus by increasing $\|H\|_\infty$ from 1.5 to 6, the baseband noise can be reduced by about two orders of magnitude. This implies that $\|H\|_\infty$ is a very important parameter for $\Delta\Sigma$ modulators with multi-bit quantizers.

Figure 2.15 shows the signal-to-noise plus distortion ratios (SNDR) of third-, fifth-order $\Delta\Sigma$ modulators with 4-bit quantizers and 8X oversampling ratios as a function of $\|H\|_\infty$. The Matlab delta-sigma toolbox is used to generate each of these and the NTF poles and zeros are optimally placed in each case [15]. The fifth-order $\Delta\Sigma$ modulator can only achieve about 48 dB SNDR with $\|H\|_\infty$ =1.5. However, when $\|H\|_\infty = 6$, 90 dB SNDR is achieved. By increasing $\|H\|_\infty$ from 1.5 to 6, the resolution of the fifth-order $\Delta\Sigma$ modulator increases by 6 to 7 bits. Recall that the

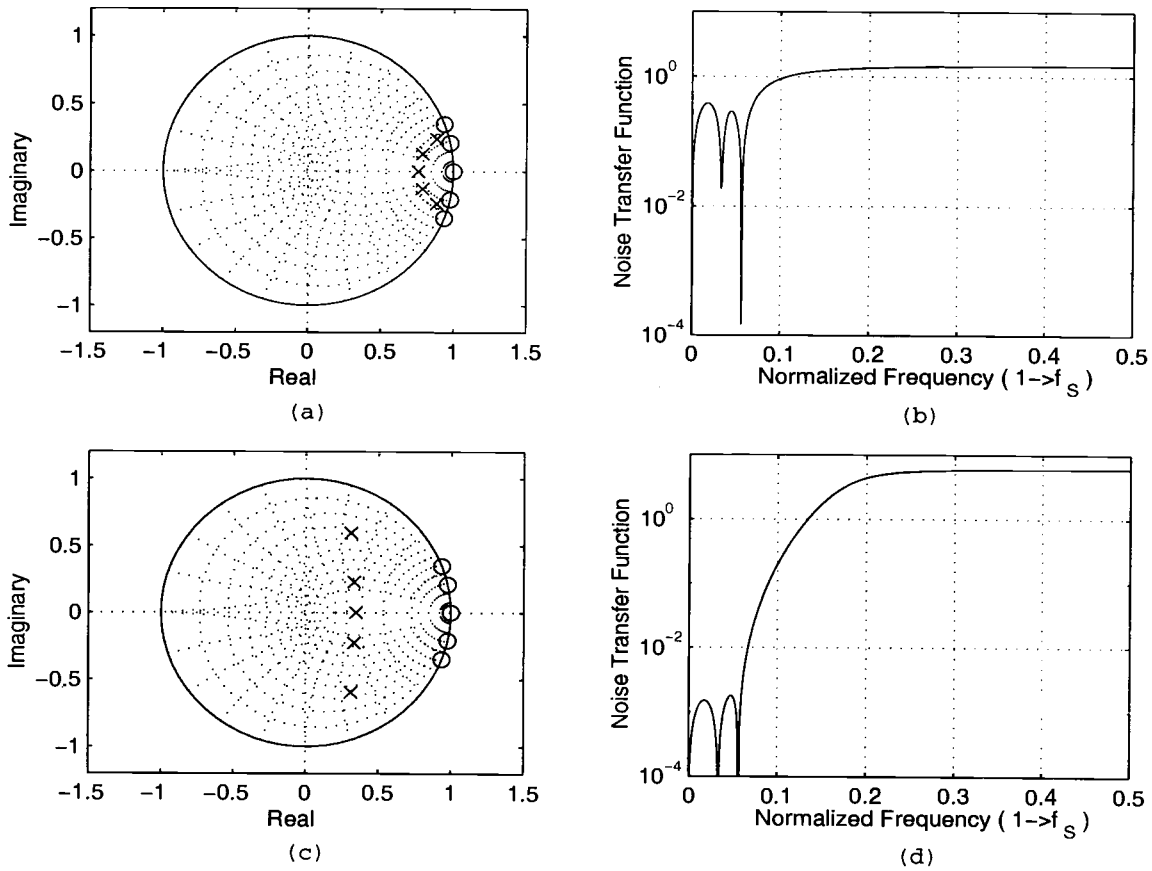


FIGURE 2.14. Comparison of two fifth-order noise transfer functions: (a) pole-zero plot of the noise transfer function with $\|H\|_\infty$=1.5, and (b) the corresponding noise transfer function of (a). (c) Pole-zero plot of the noise transfer function with $\|H\|_\infty$=6, and (d) the corresponding noise transfer function of (c).

resolution of an n-th order $\Delta\Sigma$ modulator drops about $n+0.5$ bit for each halving of oversampling ratio. For low oversampling $\Delta\Sigma$ modulators, a high $\|H\|_\infty$ can greatly amend the loss of resolution due to the reduced oversampling ratios.

The Matlab $\Delta\Sigma$ modulator toolbox uses state space matrices to represent $\Delta\Sigma$ modulators. When the implementation of the $\Delta\Sigma$ modulator is considered, the structure is usually different from the state space representation and the maximum

stable input is different from that obtained from the state space representation. Thus the maximum achievable SNDR is typically different from the curves shown in Fig. 2.15 (and usually less than that predicted in Fig. 2.15).

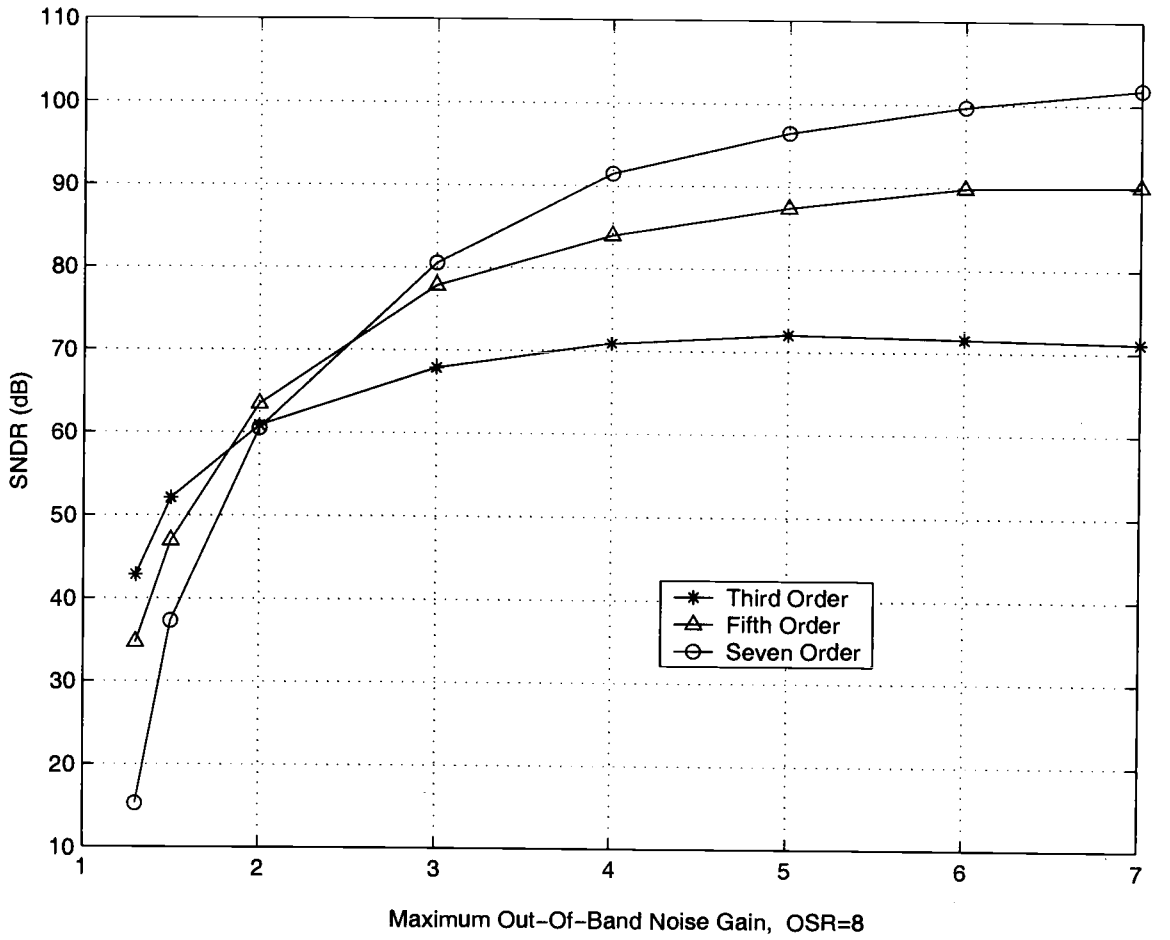


FIGURE 2.15. SNDR as a function of $\|H\|_\infty$ for third, fifth, and seventh-order $\Delta\Sigma$ modulators with a 4-bit quantizer and 8X OSR.

Another $\|H\|_\infty$ related phenomenon has also been observed when the two $\Delta\Sigma$ modulators with 8X oversampling are examined. Figure 2.16(a) is the NTF pole-zero plot of a fifth-order $\Delta\Sigma$ modulator with a 4-bit quantizer and $\|H\|_\infty$ =1.5.

Fig. 2.16(b) is the simulated output spectrum. Apart from poor noise shaping, large tones inside the baseband are also observed. The SNDR is only 40.21 dB and SFDR is only 52 dB, because the linearity is corrupted by the in-band tones. If $\|H\|_\infty$ is increased to 6 as is shown in Fig. 2.16(c), the SNDR can be increased to 83.44 dB and the baseband is tone free. This results in a SFDR of 105 dB (Fig. 2.16(d)). The solid curves in Fig. 2.16(a) and Fig. 2.16(c) denote the baseband bandwidth ($\omega = 0.0625\omega_s$ for 8X oversampling).

For the simulations shown in Fig. 2.16, idealities are included in the $\Delta\Sigma$ modulator such as no mismatch, noise, opamp finite DC gain or other non-ideal effects. Since the $\Delta\Sigma$ modulator is fifth-order, the correlation between the input signal and the quantization noise is also very weak. Thus, we would expect the baseband tones in the high-order modulator to be minimal. However, simulations show that there are large tones when $\|H\|_\infty$ is reduced to a small value. To explain this phenomenon, the Z-plane of Fig. 2.17 is considered more carefully. The natural frequency, ω, varies from 0 to π (i.e., from DC to $\frac{\omega_s}{2}$) and it is represented by the radial dotted lines in Fig. 2.17. The damping factor, ζ, varies from 0 to 1 and it is constant along circles inside the unit circle. If a complex conjugate pole pair is located at (ω ,ζ) in the Z-plane, the corresponding impulse response is:

$$h(n) = \zeta^n cos(\frac{2\pi\omega n}{\omega_s}),\ n = 0, 1, 2, 3 \ldots \tag{2.25}$$

where ω_s is the sampling frequency. The impulse response is a damped oscillation with a frequancy, ω, and a damping rate of ζ^n. For two poles located at $\omega = 0.2\omega_s$ and $\zeta = 0.9$ in the Z-plane (as shown in Fig. 2.17), the corresponding frequency domain responses are shown in Fig. 2.18. Note that the signal peaks at $f \approx 0.2f_S$. For $\Delta\Sigma$ modulators with low $\|H\|_\infty$, the NTF poles are close to DC. If

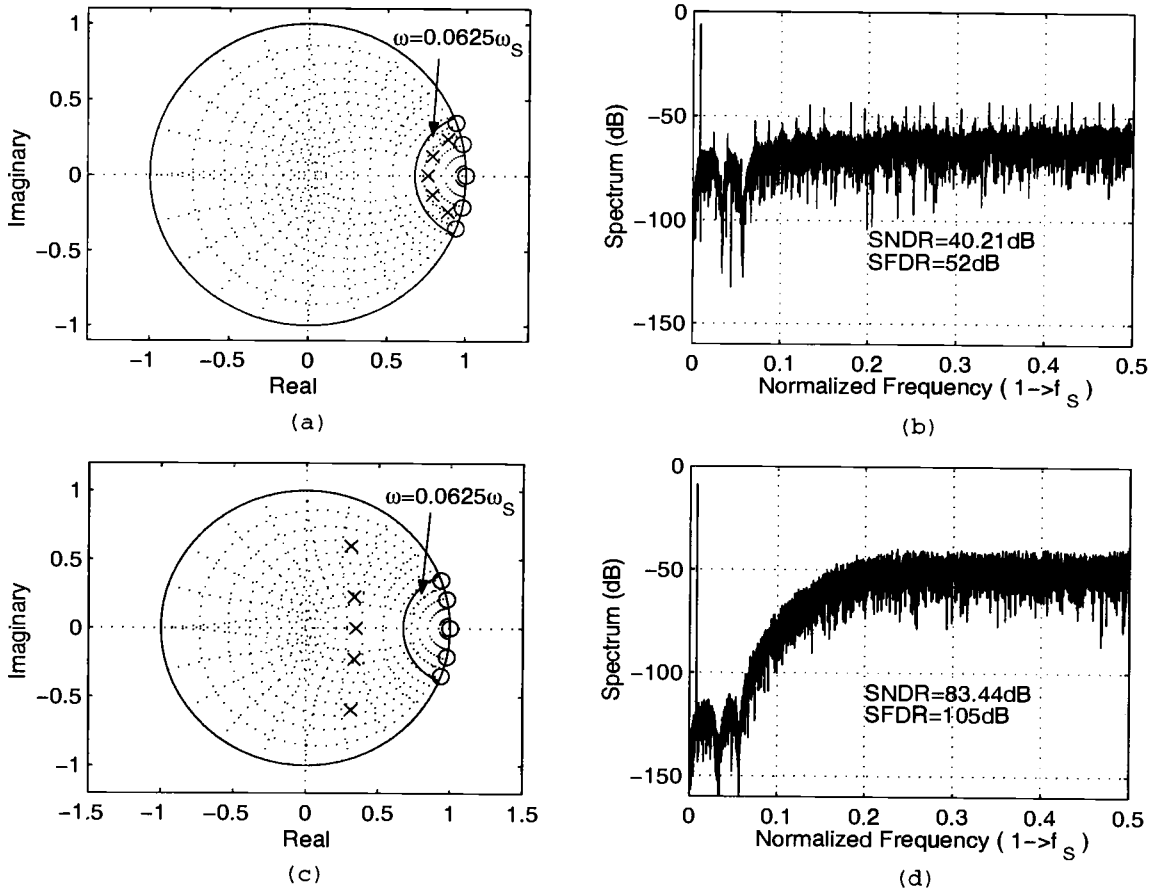


FIGURE 2.16. (a) The pole-zero plot of a fifth-order 4-bit $\Delta\Sigma$ modulator with $\|H\|_\infty$ =1.5 and 8X OSR, and (b) simulated spectrum of the modulator shown in (a). (c) The pole-zero plot of a fifth-order 4-bit $\Delta\Sigma$ modulator with $\|H\|_\infty$ =6 and 8X OSR, and (d) simulated spectrum of the modulator shown in (c).

the $\Delta\Sigma$ modulator also has a low oversampling ratio, the frequency domain peaking can be within the baseband frequency and this will generate tones in the output within the baseband bandwidth.

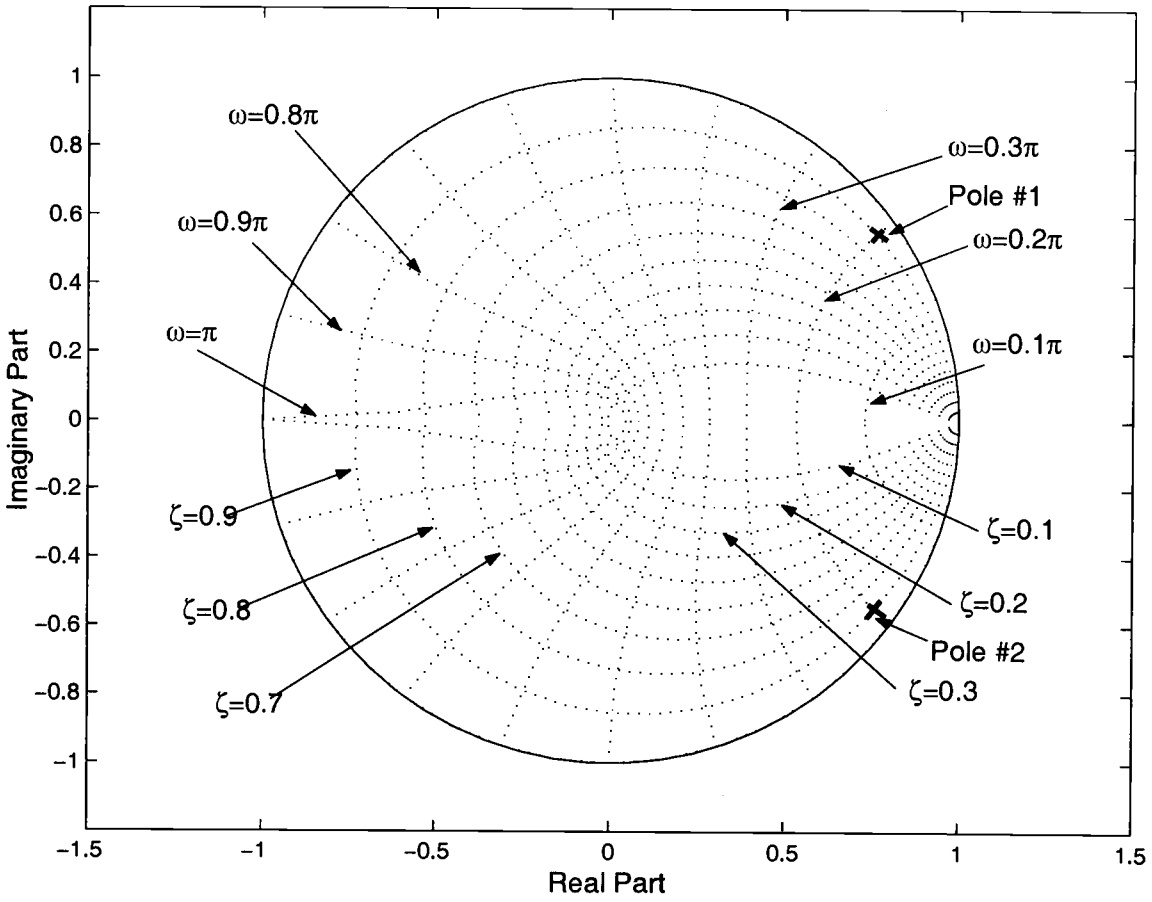


FIGURE 2.17. Constant natural frequency ω contours and constant damping rate ζ contours in a Z-plane, two poles are shown at $\omega = 0.2\pi$ and $\zeta = \pm 0.9$.

This is a simple explanation for a two-pole system. For a high-order $\Delta\Sigma$ modulator, this explanation is also valid. Figure 2.14 shows the pole-zero plots and noise transfer functions of a fifth-order $\Delta\Sigma$ modulator with $\|\mathrm{H}\|_\infty$ =1.5 and $\|\mathrm{H}\|_\infty$ =6, respectively. If a random input signal x passes through a linear time invariant system *H(f)*, the output signal y is also a random signal. The power spectral density of y is:

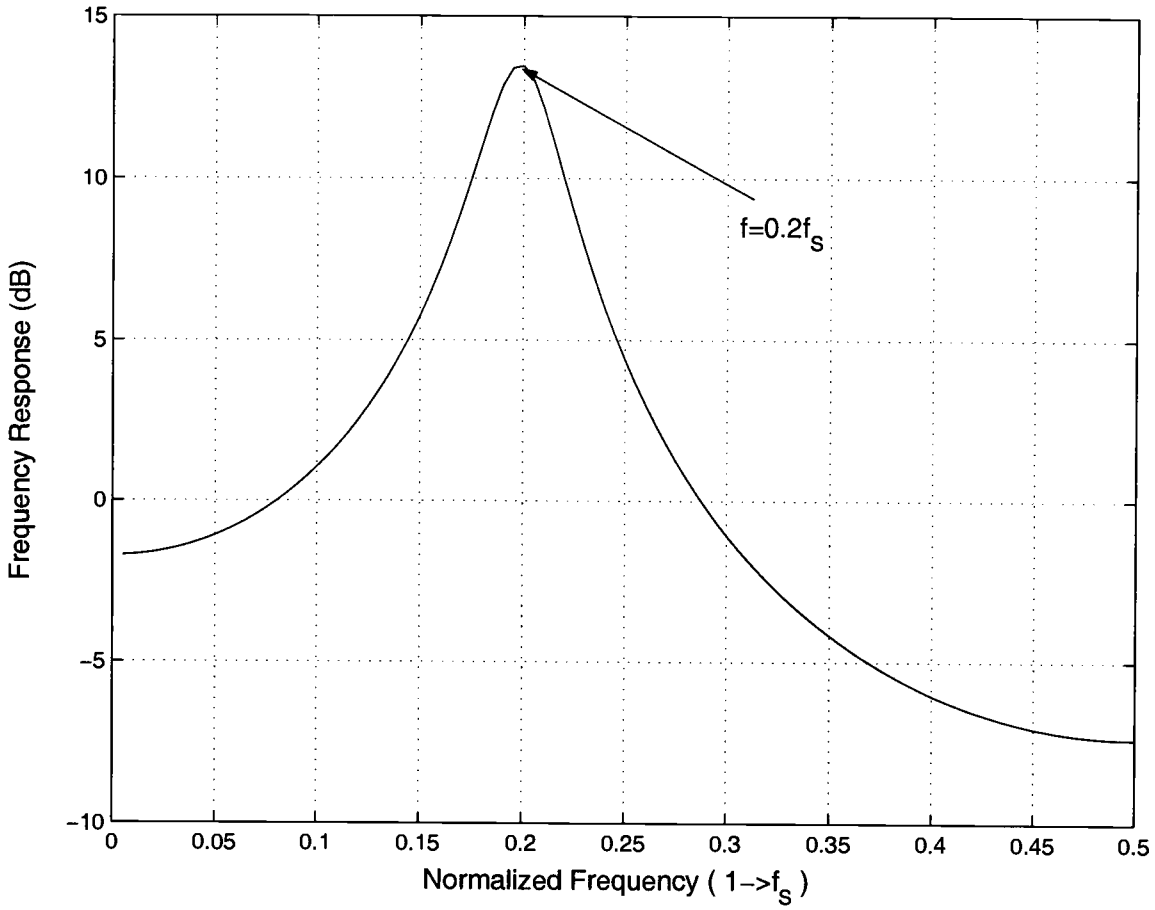


FIGURE 2.18. The frequency response of a two pole system, two poles are at $\omega \approx 0.2\pi$ and $\zeta = 0.9$ in the Z-plane.

$$S_Y(f) = |H(f)|^2 S_X(f) \tag{2.26}$$

where $S_X(f)$ is the power spectral density of x and $S_Y(f)$ is the power spectral density of y. If the quantization noise is a gaussian white noise source, the spectrum of the output signal resembles the two noise function curves shown in Fig. 2.14(b) and (d). The output does not have any tones in the baseband. But when $\|\mathrm{H}\|_\infty = 1.5$, the output spectrum has large tones as shown in Fig. 2.16.

Equation (2.26) represents the *statistical relationship* between the input and the output. It is usually approximated by a *long term averaging.* However for *short term, transient tones* may appear. Figure 2.19 shows the damped sinusoid impulse response of the noise transfer function of Fig. 2.14(a). The period of the sinusoidal wave is about 17 clock cycles. Thus, the frequency is approximately $\frac{1}{17}\omega_S$ or $0.0588\omega_S$, which is inside the baseband bandwidth. According to the convolution theorem, the output *y(n)* is:

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \tag{2.27}$$

The output *y(n)* is a superposition of impulse response functions. If the input signal is a deterministic signal such as a sinusoidal signal, the steady output will be a pure sinusiodal signal without any tones. If the input signal is a white random signal, the output has no steady state value. As a result, the output may not folllow (2.27) and tones can be found at $\omega \approx 0.0588\omega_S$. Since the tones are inside the signal band of the STF, they can interact with the input signal and eventually the output becomes tonal. This kind of $\Delta\Sigma$ modulator is *an inherently tonal* $\Delta\Sigma$ *modulator.*

Due to the tonal effect, $||H||_\infty$ of low oversampling $\Delta\Sigma$ modulators has a lower limit below which the modulator will become tonal and the SFDR starts to drop. Figure 2.20 shows the minimum $||H||_\infty$ to avoid the tonal effects as a function of the modulator order and oversampling ratio. From When OSR is high, the minimum $||H||_\infty$ can be less than 2 and Lee's rule [8] holds in this case. But when OSR is low, the minimum $||H||_\infty$ is significantly higher than 2 and Lee's rule [8] no longer holds. This relationship also applies to MASH A/D converters. The difference is that the tones of the first stage in a MASH A/D can be attenuated by the following stages and therefore tones are less significant. Multi-bit quantizers are used for the $\Delta\Sigma$

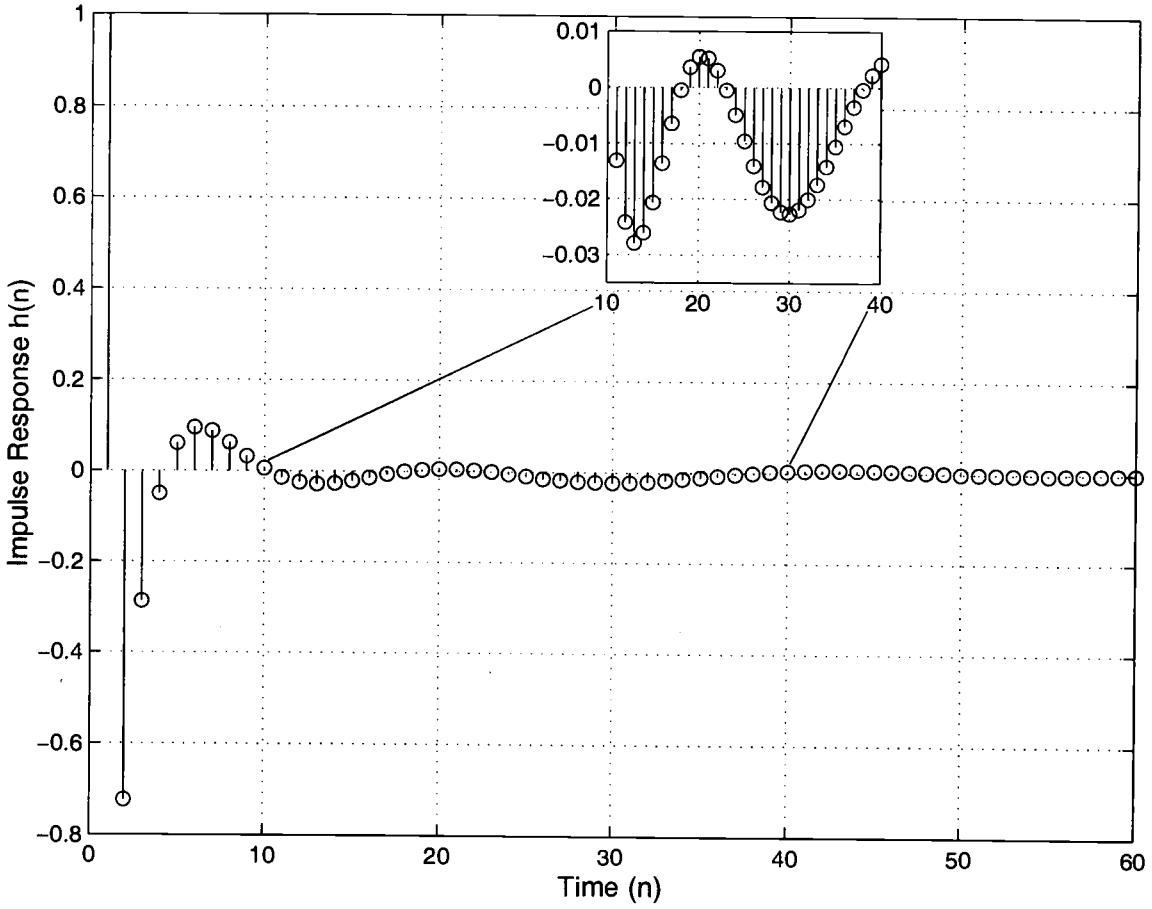


FIGURE 2.19. Impulse response of the noise transfer function shown in Fig. 2.14(a).

modulators only to ensure that the $\Delta\Sigma$ modulators are stable with high $\|H\|_\infty$. The relationship shown in Fig. 2.20 does not depend on the resolution of the quantizers.

The tones due to low $\|H\|_\infty$ are different from the tones due to limit cycle oscillations. To demonstrate this, let us consider the first-order $\Delta\Sigma$ modulator shown in Fig. 2.1. For this first-order $\Delta\Sigma$ modulator, the quantization noise is closely correlated to the input signal level and large tones can be generated. If a

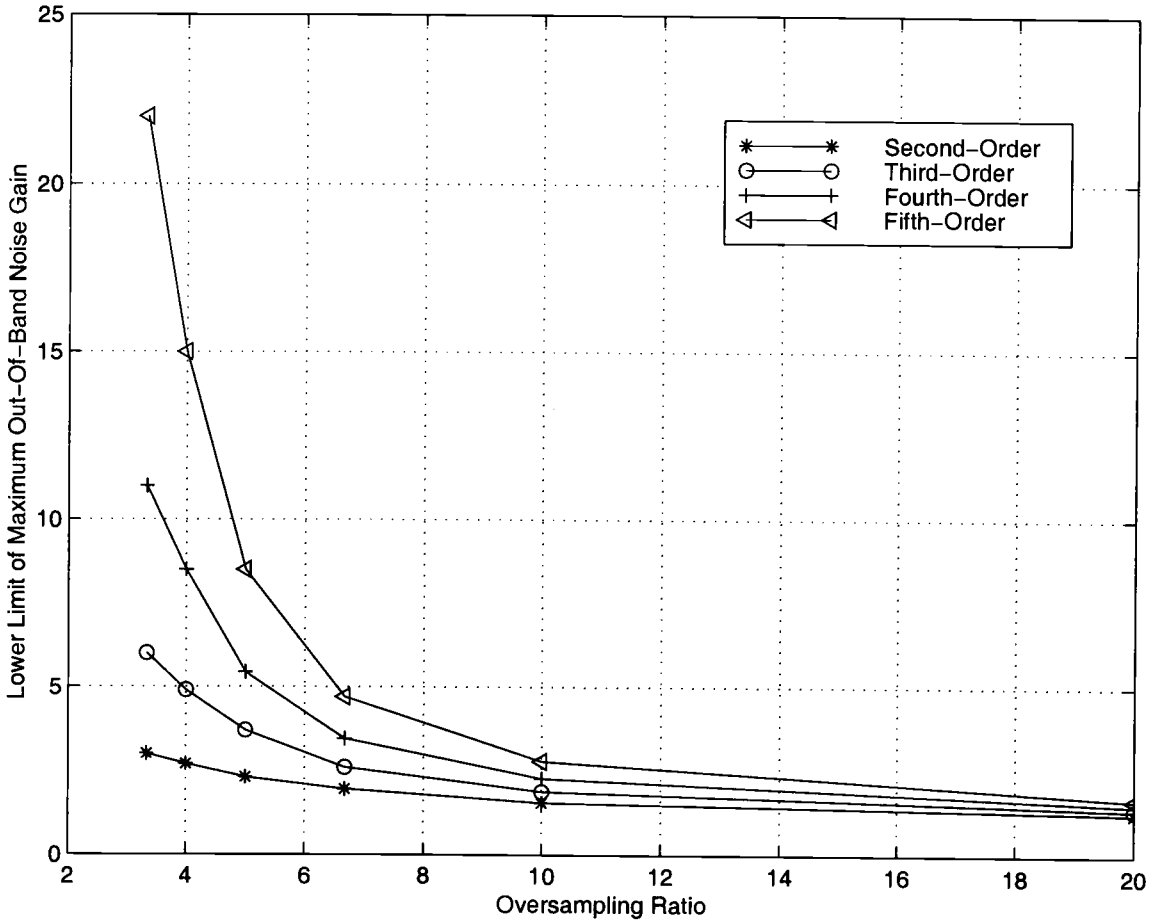


FIGURE 2.20. Minimum $\|H\|_\infty$ to avoid tones in the baseband as a function of oversampling ratio and $\Delta\Sigma$ modulator order.

small DC input is applied, pattern noise will appear at the output when the DC input is a rational number of the reference voltage [13]. If the DC input changes a small amount, the output tones can change significantly, Fig. 2.21(a) and (b). For the fifth-order $\Delta\Sigma$ modulator with a 4-bit quantizer, OSR=8 and $\|H\|_\infty = 1.5$, the tones do not change as the DC input level is changed, Fig. 2.21(c) and (d). Thus, the tones due to a low $\|H\|_\infty$ are not due to limit cycle oscillations.

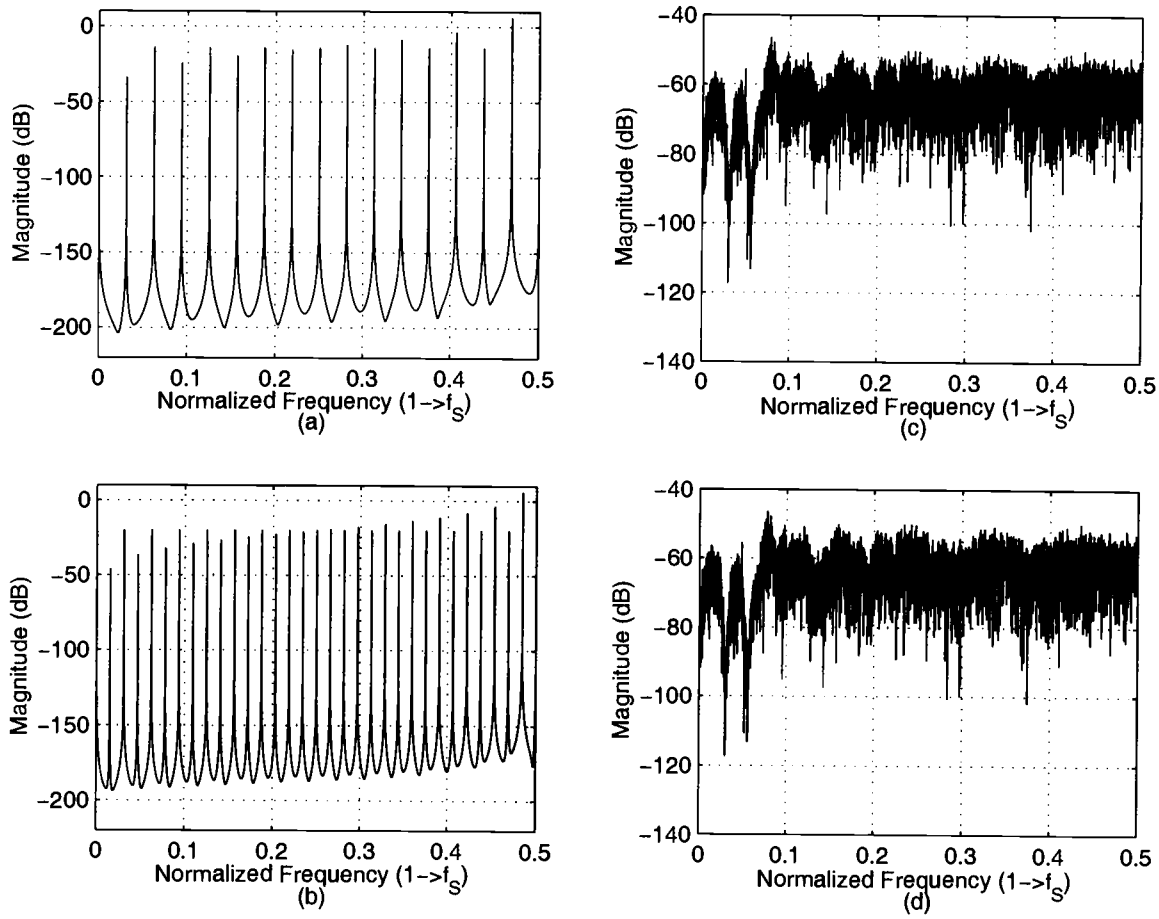


FIGURE 2.21. Spectra of two $\Delta\Sigma$ modulators with different DC input levels. First-order $\Delta\Sigma$ modulator with 1-bit quantizer (a) DC input is -24 dB relative to full scale and (b) DC input is -30 dB. Fifth-order hybrid $\Delta\Sigma$ modulator with 4-bit quantizer where OSR=8, $\|H\|_\infty$=1.5 (c) DC input is -24 dB, (d) DC input is -30 dB.

In the second example, the fifth-order $\Delta\Sigma$ modulator with $\|H\|_\infty = 1.5$ and OSR=8, large tones appear. However, when the OSR is increased to 32, there are almost no tones in the baseband, Fig. 2.22. Oversampling ratio is an important factor for these kind of tones. The tones due to limit cycle oscillations are not a strong function of the oversampling ratio [13]. Thus, the tones introduced by $\|H\|_\infty$ are not due to limit cycle oscillations.

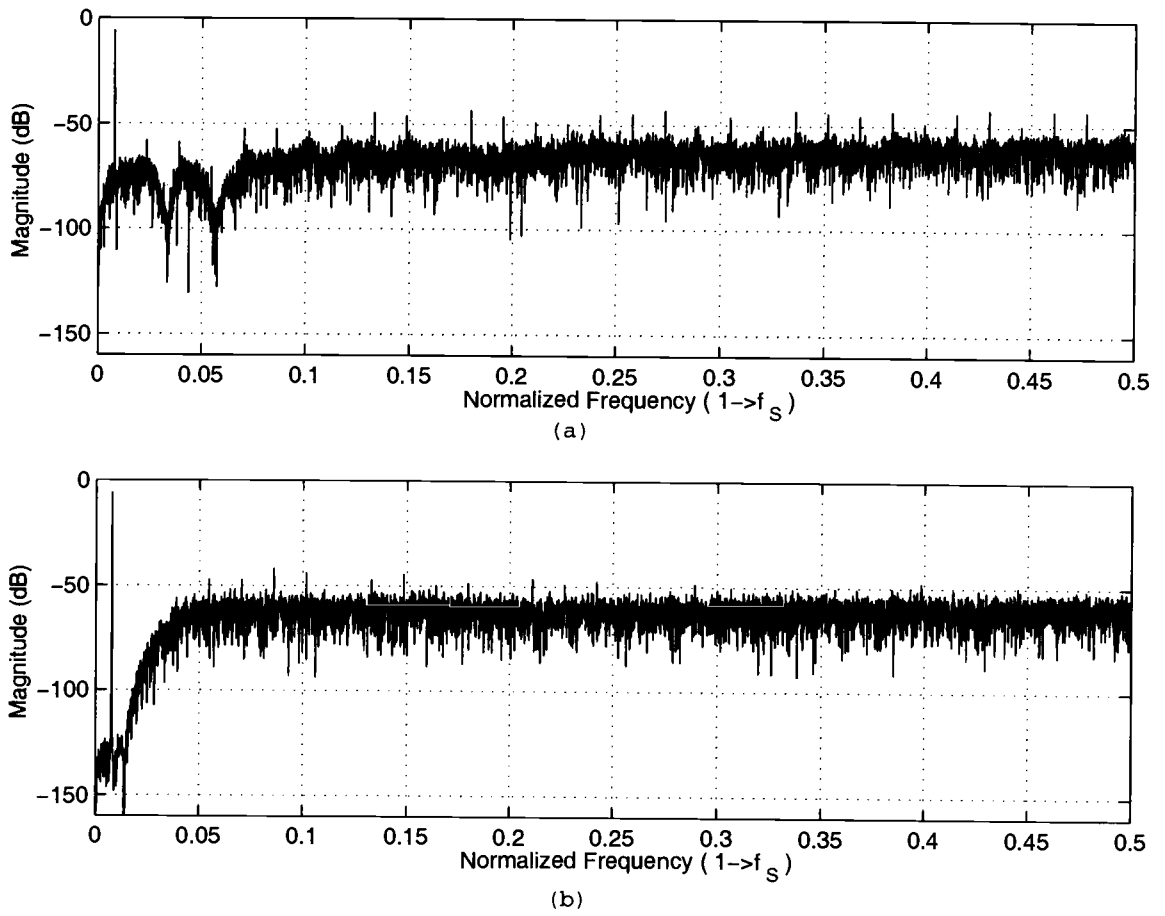


FIGURE 2.22. Spectra of two fifth-order $\Delta\Sigma$ modulators with 4-bit quantizers with (a) $\|H\|_\infty$ =1.5 and OSR=8, (b) $\|H\|_\infty$ =1.5 and OSR=32.

Another demonstration of this can be shown with the second-order $\Delta\Sigma$ modulator shown in Fig. 2.2 with $\|H\|_\infty$ of 4. According to the relation shown in Fig. 2.20, no tones will be generated in the baseband. However, the output still has tones as shown in Fig. 2.5. The tones are due to the simple second-order structure and are observable even when a high $\|H\|_\infty$ is used.

The above three examples illustrate that the two kinds of tones are due to different mechanisms. The tones due to a low $\|H\|_\infty$ are a major concern for low oversampling single-stage $\Delta\Sigma$ modulator designs. The relationship between the tones and a low $\|H\|_\infty$ is shown in Fig. 2.20. This relationship has been simulated and verified by $\Delta\Sigma$ modulators with different orders and oversampling ratios.

2.3. Conclusion

To design a single-stage low oversampling ratio $\Delta\Sigma$ A/D converter with a multi-bit quantizer, a high $\|H\|_\infty$ must be used. It is shown that a low $\|H\|_\infty$ can generate large tones in the output of low oversampling $\Delta\Sigma$ modulators and the $\Delta\Sigma$ modulators become inherently tonal. The minimum $\|H\|_\infty$ to avoid tones in the baseband frequency range is shown as a function of the oversampling ratio and the $\Delta\Sigma$ modulator order.

3. STABILITY ANALYSIS OF EXISTING ΔΣ A/D ARCHITECTURES

3.1. Analysis of a Fifth-Order Leapfrog ΔΣ Modulator

A ΔΣ modulator with a multi-bit quantizer (usually $\geq$ 3 bit) has a very small quantization noise power. As a result, it is possible to increase the out-of-band noise gain to a value greater than 2 while maintaining stable operation. Although many ΔΣ modulators with multi-bit quantizers have been implemented [3], [4], [6], [14], none of them have a $\|H\|_\infty$ significantly greater than 2. As will be described, these structures are unstable if $\|H\|_\infty$ is much higher than 2.

To gain insight into why these ΔΣ modulators tend to be unstable when $\|H\|_\infty$ is greater than 2, a fifth-order leapfrog ΔΣ modulator is analyzed [12], Figure 3.1. To optimally place the NTF poles and zeros, a *n-th* order ΔΣ modulator must have at least *2n* independent coefficients. Leapfrog ΔΣ modulators have *2n* independent coefficients where the resonator feedbacks (i.e., b1, b2,... b5) determine the zero positions of the NTF and all the coefficients (i.e. a_i, b_i, i=1,2,... 5) determine the poles of the NTF. The relationship between the coefficients and the pole-zero positions can be obtained from the circuit shown in Fig. 3.1. Mapping the coefficients to the NTF requires significant symbolic manipulation as shown in Appendix A.

Table 3.1 shows the coefficients of the leapfrog ΔΣ modulator for $\|H\|_\infty$ =1.5 and $\|H\|_\infty$ =6, respectively. When $\|H\|_\infty$ is low, the coefficient $a5$ has the minimum absolute value. The coefficient with the maximum absolute value is $a1$.

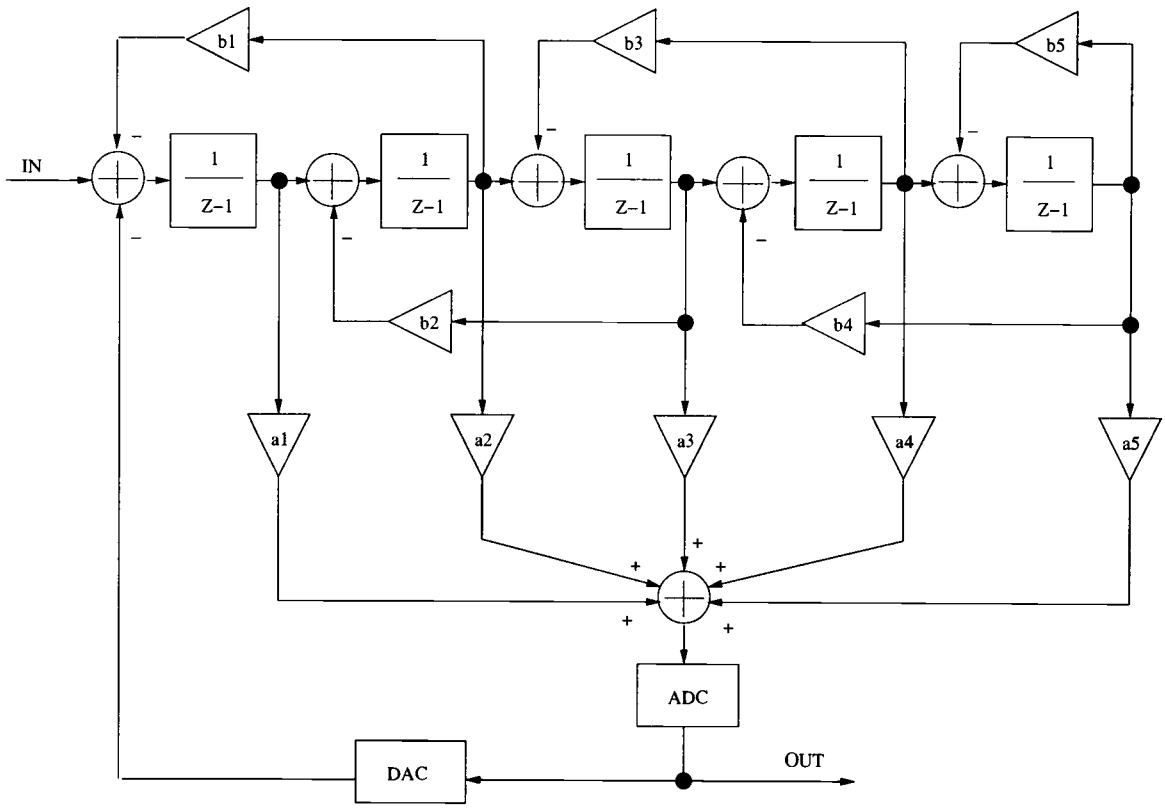


FIGURE 3.1. Structure of a fifth-order leapfrog $\Delta\Sigma$ modulator before coefficient scaling.

The *coefficient spread* is defined as the ratio of the maximum absolute coefficient value to the minimum absolute coefficient value. The leapfrog $\Delta\Sigma$ modulator has a coefficient spread of 412.6 for $\|H\|_\infty = 1.5$ and 289.3 for $\|H\|_\infty = 6$. This is a large component spread and it will result in a $\Delta\Sigma$ modulator that consumes very large area and power. The large coefficient spread also limits the maximum stable input. Thus coefficient scaling is needed to reduce the coefficient spread and increase the maximum stable input range.

The wide coefficient spread is due to the highly non-linear relationship between the circuit coefficients and the pole-zero positions of the NTF as shown in Appendix A. In general, modifying one coefficient value will change all pole-zero positions. To change one pole (pair) or one zero (pair) without changing other poles and zeros, all coefficients must be modified. This results in very high coefficient sensitivity. Thus when the poles and zeros are changed, some coefficients will rapidly increase or decrease and the coefficient spread will become very high. Scaling is one way to reduce the coefficient spread.

TABLE 3.1. The coefficients of the fifth-order leapfrog $\Delta\Sigma$ A/D converter of Fig. 3.1 with $\|H\|_\infty$=1.5 and $\|H\|_\infty$=6.

Coefficients	$\|H\|_\infty$ =1.5	$\|H\|_\infty$ =6
a1	7.227e-1	3.1941
a2	8.70133e-2	4.21372
a3	-5.41897e-2	2.5654
a4	5.25965e-3	5.88958e-1
a5	1.75135e-3	-1.38268e-1
b1	0	0
b2	5.25337e-2	5.25337e-2
b3	1.45646e-2	1.45646e-2
b4	1.08502e-1	1.08502e-1
b5	1.699e-1	1.699e-1

Using equivalent scaling, the coefficients of a switched capacitor circuit can be scaled such that the poles and zeros of the transfer function remain unchanged after scaling and the dynamic range is improved. The most commonly used scaling method [16] is to multiply all capacitors connected to the opamp outputs by a factor S. This will improve the output dynamic range of each opamp by a factor of S. For $\Delta\Sigma$ modulators, it is usually more important to improve the maximum stable input

range and reduce the coefficient spread than to simply increase the opamp dynamic range.

To scale the $\Delta\Sigma$ modulator for maximum stable input range and minimum coefficient spread, a general rule for equivalent scaling is needed. Consider a simple feedback system with a loop filter $T(Z) = \frac{N(Z)}{D(Z)}$ and a feedback factor K. The closed-loop transfer function is:

$$H(Z) = \frac{1}{1+K\frac{N(Z)}{D(Z)}} \tag{3.1}$$

If, after equivalent scaling, the loop gain $K\frac{N(Z)}{D(Z)}$ is not changed, then the poles and zeros of $H(Z)$ remain unchanged. Thus scaling can also be applied to more complicated linear systems with local resonator feedbacks, feedforwards and distributed feedbacks.

There are numerous equivalent scaling methods. One way to scale the leapfrog $\Delta\Sigma$ modulator is shown in Fig. 3.2. Each distributed feedforward path (i.e., the paths formed by $\frac{a_1}{S_1}$, $\frac{a_2}{S_1S_2}$,...) forms a feedback loop via the ADC, the DAC and the integrators. Each local resonator feedback also forms a feedback loop. The scaling method makes all feedback loop gains constant. The scaling factors $S_1, S_2, \ldots S_5$ are usually between 0 and 1. For a high oversampling ratio leapfrog $\Delta\Sigma$ modulator, the coefficients a_4 and a_5 have very small absolute values before scaling, Fig. 3.1. After scaling, the absolute values of a_4 and a_5 are increased and the coefficient spread is reduced. At the same time, the maximum stable input is also increased. In Fig. 3.2, we see that the coefficients of the leapfrog $\Delta\Sigma$ modulator are very sensitive to small variations in $S_i (i = 1, 2, \ldots 5)$.

The leapfrog $\Delta\Sigma$ modulator is stable with $\|\mathrm{H}\|_\infty = 1.5$. But when $\|\mathrm{H}\|_\infty = 6$, it is unstable with or without scaling. Comparing the two sets of coefficients in Table 3.1, the absolute values of the coefficients $a1, a2, \ldots a5$ are increased significantly

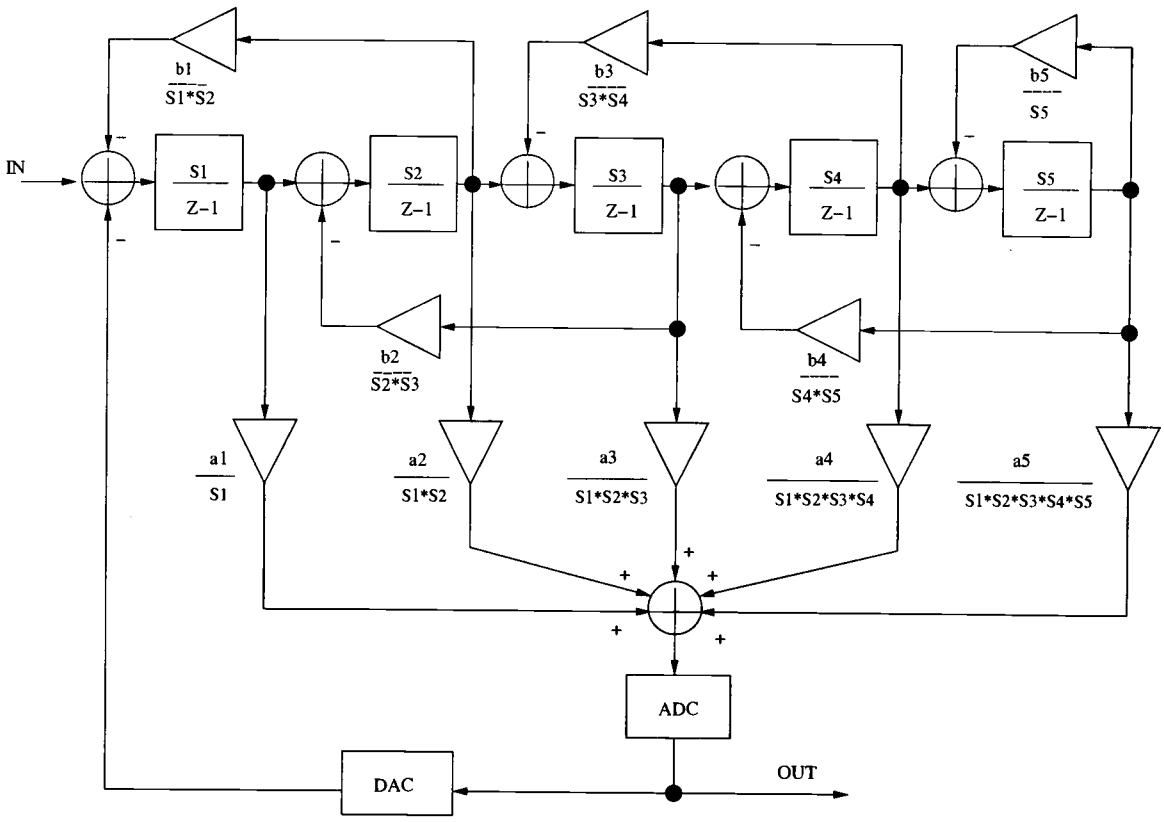


FIGURE 3.2. Structure of a fifth-order leapfrog $\Delta\Sigma$ modulator after coefficient scaling.

when $\|H\|_\infty$ is increased from 1.5 to 6. The integrator output amplitudes increase much faster than those with $\|H\|_\infty$ =6 and will overload the quantizer and make the $\Delta\Sigma$ modulator unstable. Simulation shows scaling the leapfrog $\Delta\Sigma$ modulator coefficients does not help to stabilize the modulator, when the $\|H\|_\infty$ is too high.

The leapfrog $\Delta\Sigma$ modulator has five integrators in the forward path and the amplitudes tend to build up from one integrator to the next. When $\|H\|_\infty$ is set to a high value such as 6, the absolute values of $a5$ and $a4$ become much larger than those with $\|H\|_\infty$ =1.5. The output amplitudes of the 4th and 5th integrators are

higher than those of the other integrators. If $a5$ and $a4$ have large absolute values, the two outputs will be the dominant signals at the quantizer input. The low order feedback loops formed by a1 and a2 are too weak to force stable oeration in the $\Delta\Sigma$ modulator. Simulation shows that the leapfrog $\Delta\Sigma$ modulator with $\|H\|_\infty = 6$ becomes unstable a few clock periods after power up. The higher order feedback loops formed by $a4$ and $a5$ become the dominant loops in this architecture and the $\Delta\Sigma$ modulator becomes unstable. Scaling the coefficients in the opposite direction (i.e. in the direction that the coefficient spread is *increased*) will improve stability. But the coefficient spread, which is already very high, will be even higher and this kind of coefficient spread is not feasible for a practical implementation.

If the $\Delta\Sigma$ modulator has a moderate $\|H\|_\infty$ such as 1.5, it is very stable. This is due to the fact that the absolute values of $a5$ and $a4$ are very small and the feedback loops formed by coefficients $a5$ and $a4$ are not the dominant loops. Lower order feedback loops formed by $a1$ and $a2$ are the dominant loops. Thus the $\Delta\Sigma$ modulator is very stable with a low $\|H\|_\infty$.

The high DC gain of the integrators and the highly non-linear relationship between the $\Delta\Sigma$ modulator coefficients and the NTF pole-zero positions are the two major contributors to instability. For a $\Delta\Sigma$ modulator with a high $\|H\|_\infty$ to be stable, the modulator must be able to form a dominant negative feedback as early as possible to stabilize the modulator, and some blocks must have moderate gain to avoid amplitude build-up.

3.2. Review of Other Commonly Used Structures

Since most $\Delta\Sigma$ modulators are unstable with a high $\|H\|_\infty$, a review of existing $\Delta\Sigma$ modulator structures can help to create a new structure that is stable with a

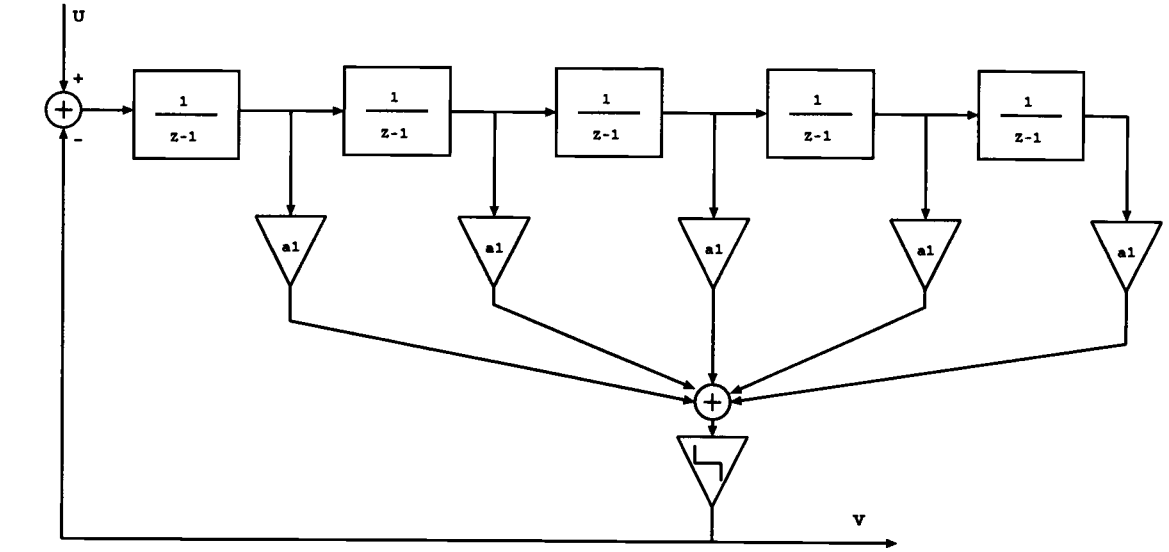
high $\|H\|_\infty$. The commonly used $\Delta\Sigma$ modulator structures can be found in [13] and [15] and include: chain of integrators with weighted feedforward summation (FFS) [13], chain of integrators with feedforward summation and local resonator feedback (FFLR) [13], chain of integrators with distributed feedback (DFB) [13], chain of integrators with distributed feedback distributed feedforward inputs (DFBFF) [13] and chain of integrators with distributed feedback distributed feedforward paths and local resonator feedback (DFBFFLR).

Figure 3.3(a) shows the FFS structure where the weighted feedforward paths determine the NTF poles. Since this structure does not have $2n$ coefficients, it cannot arbitrarily place the NTF zeros and all NTF zeros are at DC. This is a big drawback for low oversampling $\Delta\Sigma$ modulators. For low oversampling applications, if the NTF poles can be optimally placed, an extra increase in SNR (typically from a few dB to 20dB) can be achieved. This structure also has a wide coefficient spread. Because of the high DC gain requirement of the integrators, the integrator outputs can build up rapidly after power up and instability can occur.

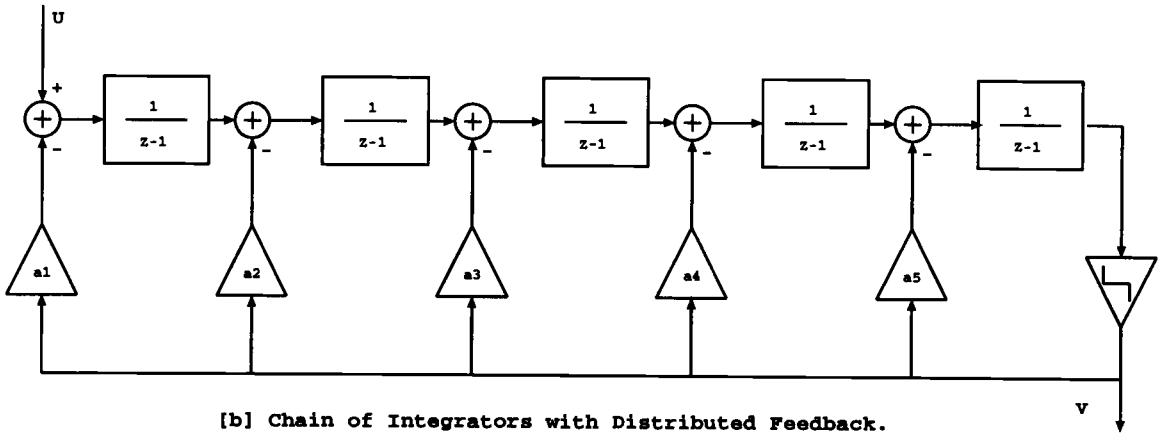
Figure 3.3(b) shows the DFB structure. The distributed feedback paths determine the NTF pole positions. Similar to the FFS structure, it does not have $2n$ coefficients and all the NTF zeros are at DC. A big drawback of this structure is that for an n-th order $\Delta\Sigma$ modulator with a DFB structure, it takes n clock periods for the input signal to reach the quantizer input after power up. Before it reaches the quantizer input, the quantizer output is independent of the input signal. Thus, in terms of the input signal, the $\Delta\Sigma$ modulator runs in open-loop mode between $t = 1$ and $t = n$. If the $\Delta\Sigma$ modulator is high order, the integrator outputs can be very large. When the input signal reaches the quantizer input at $t = n$, the large output can overload the quantizer and the modulator is unstable. For a $\Delta\Sigma$ modulator with a FFS structure, a first-order feedback loop is formed right after

the first clock period that helps to stabilize the $\Delta\Sigma$ modulator. For this reason, a high order FFS structure is generally more stable than a high order DFB structure.

The FFLR structure is similar to the FFS structure. It has some local resonator feedback loops to move the NTF zeros away from DC. The DFBFF structure is similar to the DFB structure. The extra feedforward inputs do not change the NTF. They help to give more freedom in placing the STF zeros. The DFBFFLR structure is similar to the DFBFF structure. The extra local resonator feedback loops allow the NTF zeros to be moved away from DC. The local resonator feedback can reduce the DC gain requirement of the integrators, but it does not significantly improve the stability. In this case, the local resonator feedback is very weak and the resonator feedback coefficients are typically of the same order of magnitude as $\frac{1}{OSR}$ or less. Thus, the DC gain requirement is still very high and stability is difficult to achieve.



[a] Chain of Integrators with Weighted Feedforward Summation.



[b] Chain of Integrators with Distributed Feedback.

FIGURE 3.3. Block diagrams of two typical $\Delta\Sigma$ modulators.

3.3. Conclusion

Existing high-order $\Delta\Sigma$ modulators become unstable when $\|H\|_\infty$ is greater than 2, and they also have very large coefficient spreads for low oversampling. To reduce the coefficient spread, a simple structure is needed. Additionally, to avoid instability in high-order single-stage $\Delta\Sigma$ modulators, chains of cascaded integrators should be avoided and low gain blocks in the forward path are used to help stabilize the modulator. In Chapter 4, a new $\Delta\Sigma$ modulator structure is presented which is stable for high $\|H\|_\infty$, and the coefficient spread is minimal even with low oversampling ratios.

4. Hybrid $\Delta\Sigma$ A/D CONVERTER FOR LOW OVERSAMPLING APPLICATIONS

4.1. The Derivation of Hybrid $\Delta\Sigma$ Modulator Structure

In order to design a single-stage $\Delta\Sigma$ A/D with low oversampling ratio and 14-bit resolution, a new structure must be devised which is realizable and stable for high $\|H\|_\infty$. As presented in the previous chapters, the new structure must satisfy the following conditions:

- The $\Delta\Sigma$ modulator must be realizable as a stable high-order structure.
- A high $\|H\|_\infty$ must be employed to boost SNR and to reduce tones.
- The relationship between the NTF poles-zeros and the modulator coefficients must be simple so that the coefficient spread is small.
- For high-order $\Delta\Sigma$ modulators, feed-forward paths should be used to increase stability.
- Low gain blocks should be introduced to enhance stability.
- The coefficient spread must be as small as possible reducing both the capacitor size and power dissipation.
- The front-end must be as simple as possible so that reduced noise and distortion can be achieved.

In Chapter 2, it is shown that a fifth-order $\Delta\Sigma$ A/D with a 4-bit quantizer and $\|H\|_\infty$ =6 can achieve 14-bit resolution with an 8X oversampling ratio. In order to implement a stable $\Delta\Sigma$ modulator with a high $\|H\|_\infty$, the modulator coefficients must be insensitive to variations due to quantization or mismatches. According to [32], a high-order linear system can have lower sensitivity if it is decomposed into first-order and second-order subsystems. This implies that if we can find a way to decompose a high-order $\Delta\Sigma$ modulator into first-order and second-order blocks, the $\Delta\Sigma$ modulator is likely to be stable with higher $\|H\|_\infty$. One such approach is to use a MASH structure. But the MASH structure requires very small integrator leakage and very accurate coefficients for the first stage. With a 0.18 μm CMOS process, the typical opamp DC gain is only 40-45 dB. Thus, integrator leakage is high and the error due to the leakage cannot be accurately estimated by the following stages. As a result, the performance of the MASH $\Delta\Sigma$ modulator is limited and a single-stage $\Delta\Sigma$ modulator structure is needed to avoid the problems associated with MASH $\Delta\Sigma$ modulators. To find such a structure, let us consider the noise transfer function of this modulator. The noise transfer function is:

$$NTF(Z) = \frac{(Z-1)(Z^2-1.955Z+1)(Z^2-1.875Z+1)}{(Z-0.3466)(Z^2-0.6659Z+0.1626)(Z^2-0.6238Z+0.451)} \tag{4.1}$$

Figure 4.1 shows a $\Delta\Sigma$ modulator with a simple feed-back with the quantizer gain assumed to be unity. The loop filter in the forward path is $L(Z) = \frac{N(Z)}{D(Z)}$ and the noise transfer function is:

$$NTF(Z) = \frac{1}{1+L(Z)} = \frac{D(Z)}{N(Z)+D(Z)} \tag{4.2}$$

Comparing (4.1) with (4.2), $N(Z)$ and $D(Z)$ can be obtained as:

$$N(Z) = (3.1938Z^4 - 8.02Z^3 + 8.7376Z^2 - 4.6176Z + 0.9746) \tag{4.3}$$

$$D(Z) = (Z-1)(Z^2-1.955Z+1)(Z^2-18.75Z+1) \tag{4.4}$$

The loop filter $L(Z)$ is:

$$L(Z) = \frac{3.1938}{Z-1}\frac{(Z^2-1.224Z+0.4028)}{(z^2-1.955z+1)}\frac{(z^2-1.287z+0.7576)}{(z^2-1.875z+1)} \tag{4.5}$$

Thus $L(Z)$ can be decomposed into an integrator, a gain stage and two low-Q biquad stages. A low-Q biquad has both low gain and low coefficient spread. Thus low-Q biquad blocks in the forward path can increase stability and reduce coefficient spread at the same time. There are many ways to implement a biquad. One way is to use typical biquad circuits shown in [16] [17]. However, these circuits require the use of zero delay integrators. If two zero delay biquad circuits are cascaded, the total delay is the sum of the two biquad circuits. Thus the maximum clock frequency will be limited. Many structures can be found for IIR systems [18]. Among these structures, *the direct form II structure* and *the transposed direct form II structure* are the most suitable structures for the biquad circuits.

Let us consider the transposed direct form II structure shown in Fig. 4.2. This structure can generate two poles and two zeros and the transfer function $H(Z)$ is:

$$H(Z) = \frac{b_0Z^2+b_1Z+b_2}{Z^2-a_1Z-a_2} \tag{4.6}$$

In Fig. 4.2, there is still a zero delay path from the input to the output with a gain of b_0 and consequently the maximum clock frequency of the $\Delta\Sigma$ modulator will still be limited. One way to circumvent these problems is to modify (4.5) into the following form:

$$L(Z) = \frac{3.1938}{Z-1}(1+\frac{0.731Z-0.5972}{z^2-1.955z+1})(1+\frac{0.588Z-0.2424}{z^2-1.875z+1}) \tag{4.7}$$

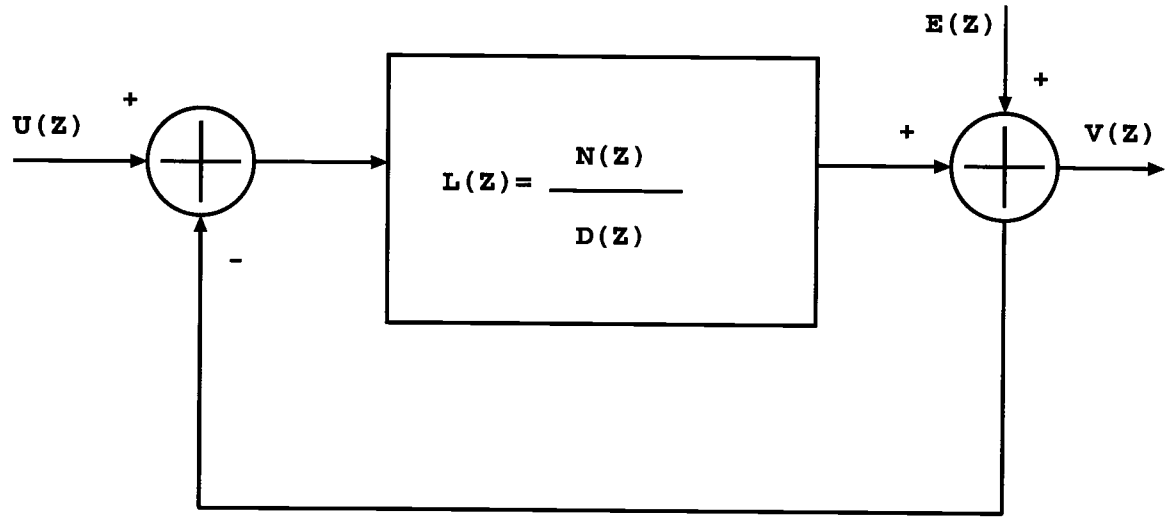


FIGURE 4.1. Block diagram of a $\Delta\Sigma$ modulator with a simple feed-back.

The block diagram of the fifth-order $\Delta\Sigma$ modulator corresponding to (4.7) is shown in Fig. 4.3. The zero delay path is avoided and feed-forward paths are formed to stabilize the $\Delta\Sigma$ modulator. A 4-bit, 17-level quantizer is used in the circuit. It has two second-order transposed direct form II blocks in the modulator. The two blocks have the same structure shown in Fig. 4.4 with the only difference between them being the coefficient values. The transfer function of the transposed direct form II block shown in Fig. 4.4 is:

$$H(Z) = \frac{b_1 Z + b_2}{Z^2 - a_1 Z - a_2} \tag{4.8}$$

Finally, comparing (4.8) with (4.7), the coefficient values in the circuit can be obtained. Table 4.1 shows the coefficients of the $\Delta\Sigma$ modulator shown in Fig. 4.3 with $\|H\|_\infty$ equal to 1.5 and 6, respectively.

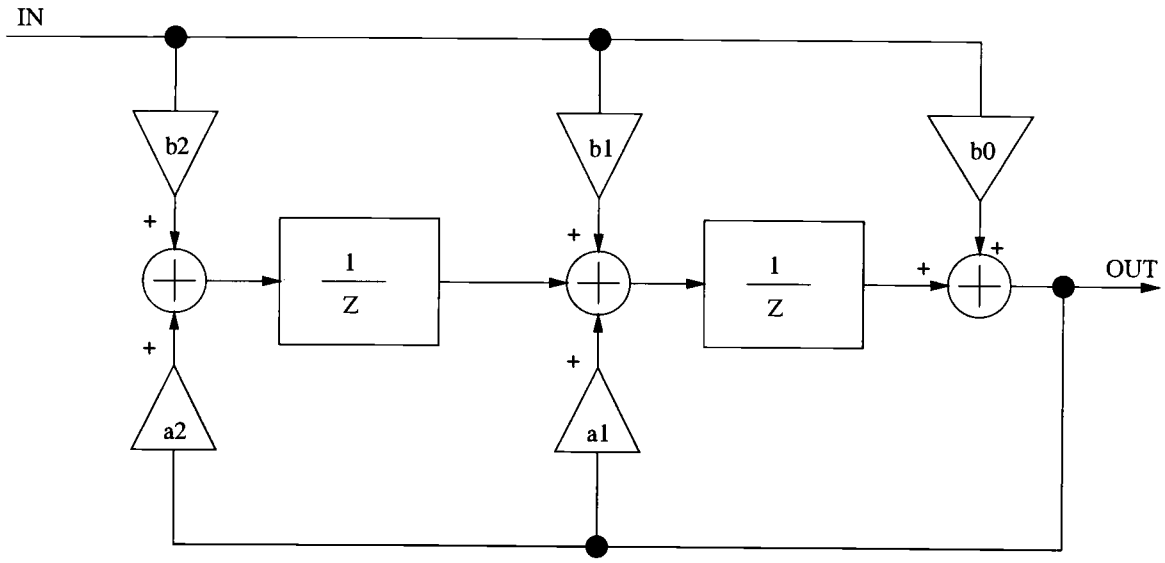


FIGURE 4.2. Block diagram of a second-order transposed direct form II structure.

In the table, a_{ij} and b_{ij} $(i, j = 1, 2)$ are the circuit coefficient values. The subscript i denotes the block number while the subscript j indicates the component in block i. Since the $\Delta\Sigma$ modulator shown in Fig. 4.3 has both integrator and delay blocks, this structure is referred to as a *hybrid structure.* The coefficient spread of the hybrid $\Delta\Sigma$ modulator is 40.73 when $\|H\|_\infty$=1.5 and it is 8.065 when $\|H\|_\infty$=6. The coefficient spread is much smaller than that shown in Table 3.1 for the leapfrog modulator. Thus with the hybrid structure, the die size and power dissipation are significantly reduced. This structure is particularly suited for high $\|H\|_\infty$, because the coefficient spread drops significantly as $\|H\|_\infty$ is increased.

Each second-order transposed direct form II block shown in Fig. 4.3 generates a complex conjugate zero pair in the Z-plane. The front-end integrator creates a zero at DC. The two transposed direct form II blocks are independent in determining the zeros of the noise transfer function. If the coefficient in one block changes,

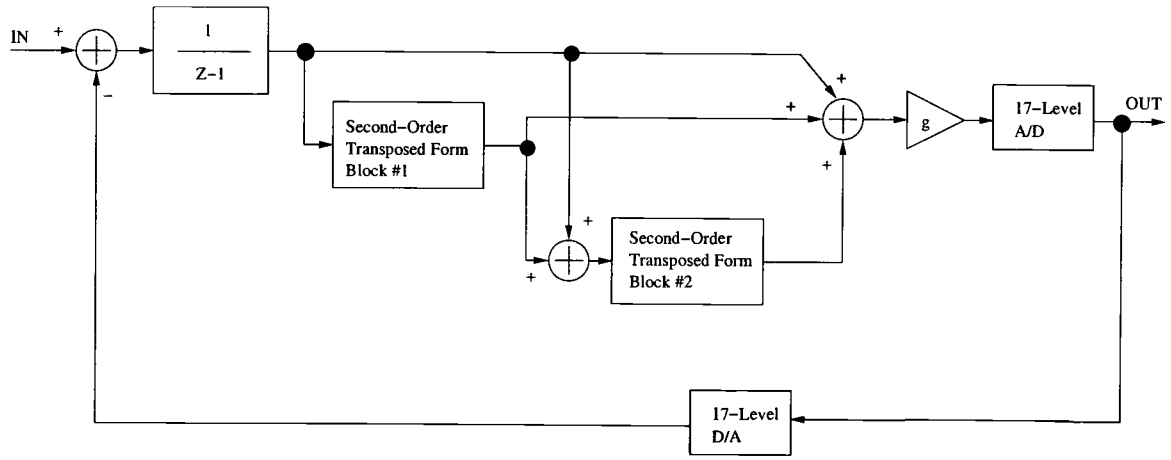


FIGURE 4.3. Block diagram of a fifth-order $\Delta\Sigma$ modulator.

only the zeros generated by this block will be changed and all other zeros remain unchanged. Thus the realtionship between the zeros and the circuit coefficients is always second-order, although the order of the $\Delta\Sigma$ modulator is more than second-order. This structure results in low coefficient sensitivity and the capacitor matching requirement is relaxed. The relationship between the NTF poles and the circuit coefficients is not as simple as that between NTF zeros and circuit coefficients. But the NTF poles are much more insensitive to coefficient variations than other structures as described in more detail in Section 4.4.

4.2. Stability of the Fifth-Order Hybrid $\Delta\Sigma$ Modulator

Stability is always an important consideration for high order $\Delta\Sigma$ modulators. Figure 4.5 shows the root locus of the noise transfer function. The $\Delta\Sigma$ modulator in this case will be unstable if the quantizer gain is less than 0.81.

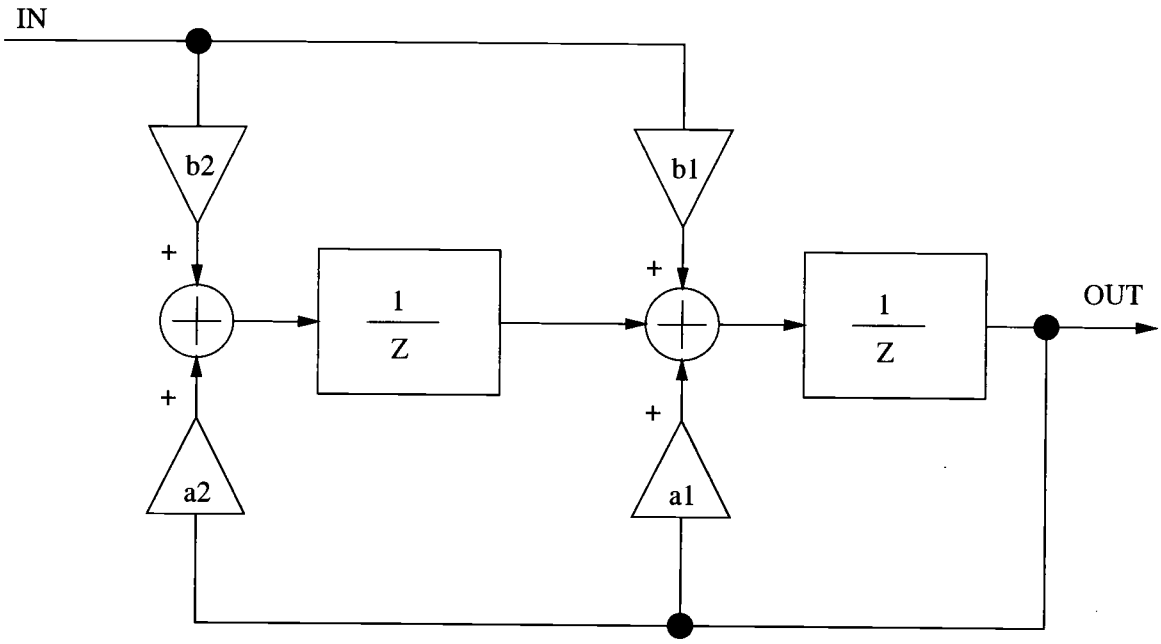


FIGURE 4.4. Block diagram of the second-order transposed direct form II structure shown in Fig. 4.3.

If a 1-bit quantizer is used, stability of a fifth-order $\Delta\Sigma$ modulator is a challenging problem. However, if a multi-bit quantizer is used, the problem can be greatly alleviated. A multi-bit quantizer reduces the quantization noise power, linearizes the $\Delta\Sigma$ modulator and simplifies the stability problem. Figure 4.6 shows the optimum quantizer gain as a function of input signal level. The variation of K_{opt} is very small before the modulator becomes unstable. Even when the input signal is less than 1 LSB, the optimum quantizer gain is still around 0.915. Thus the linearity of the quantizer is well defined (K $\approx$ 0.915) and the $\Delta\Sigma$ modulator can be approximated by the linear model shown in Fig. 2.10 with $K \approx 0.915$.

TABLE 4.1. The coefficients of a fifth-order Hybrid $\Delta\Sigma$ A/D converter (shown in Fig. 4.3) for $\|H\|_\infty$ =1.5 and $\|H\|_\infty$ =6 before coefficient scaling

Coefficients	$\|H\|_\infty$ =1.5	$\|H\|_\infty$ =6
g	0.7224	3.1938
a_{11}	1.875	1.875
a_{12}	-1.0	-1.0
b_{11}	0.048	0.588
b_{12}	-0.0889	-0.2424
a_{21}	1.955	1.955
a_{22}	-1.0	-1.0
b_{21}	0.073	0.731
b_{22}	-0.1006	-0.5972

In order to estimate the SNR as a function of the input level, a model is needed. For $\Delta\Sigma$ modulators with a 1-bit quantizer, the describing function method [19] can be used. For $\Delta\Sigma$ modulators with a multi-bit quantizer, the describing function does not work very well, since the multi-bit quantizer is more linear than a 1-bit quantizer. A simplified linear model can be used, since the quantizer optimum gain shown in Fig. 4.6 is very well defined. It only varies in a small range as the input signal level changes. Thus the $\Delta\Sigma$ modulator can be simplified and the simplified model is shown in Fig. 4.7.

The $\Delta\Sigma$ modulator becomes unstable when the quantizer gain drops to 0.81 for a DAC output range of ± 1. Referring this to the input of the linearized quantizer in Fig. 4.7, the $\Delta\Sigma$ modulator will be unstable when the signal Y is $\frac{1}{0.81}$. Signal Y can be expressed as a function of the input signal, U, and the quantization noise, E_i, if the quantization is assumed to be linear with a gain K:

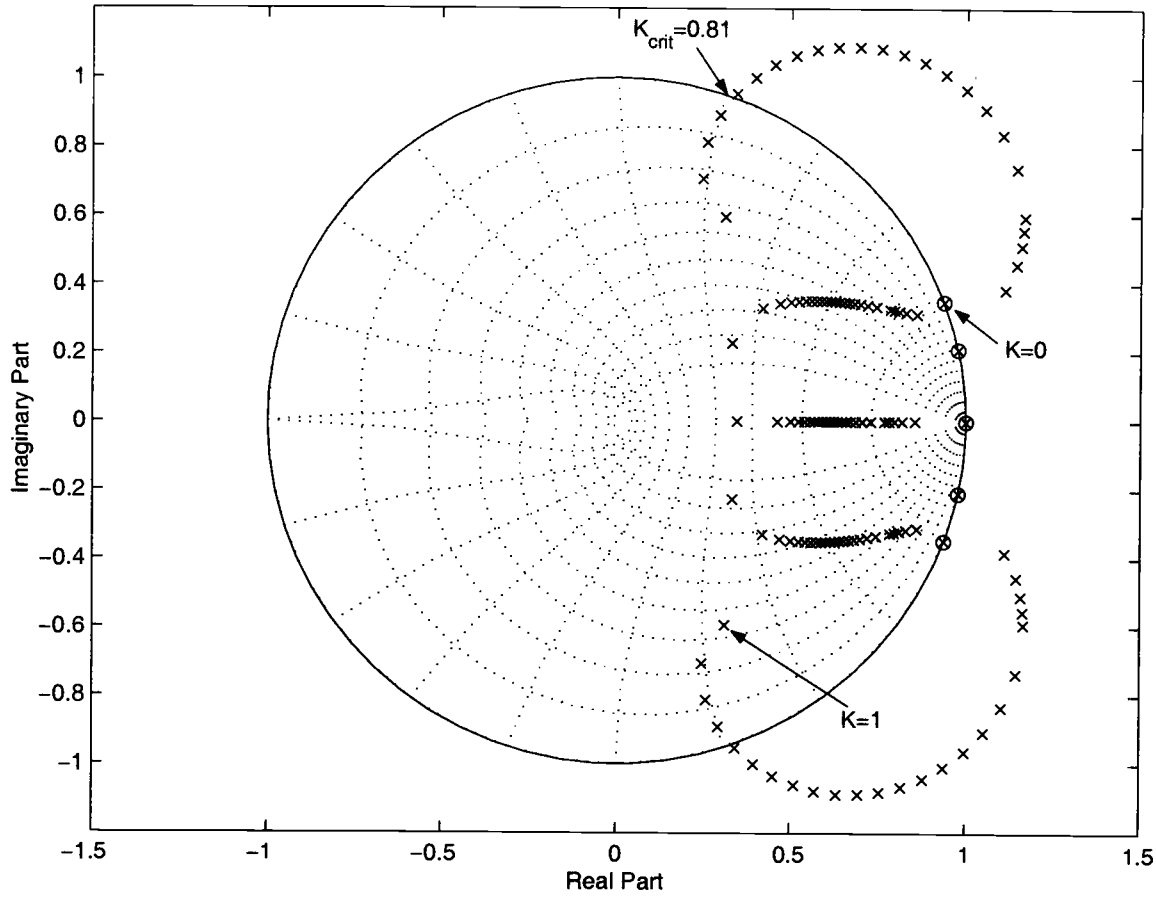


FIGURE 4.5. Root locus of a fifth-order Hybrid $\Delta\Sigma$ modulator with $\|\mathrm{H}\|_\infty$=6.

$$Y = \frac{(U-E_i)L(Z)}{1+KL(Z)} \tag{4.9}$$

where $L(Z)$ is the loop filter shown in (4.7) and K is the optimum quantizer gain. The frequency response of $L(Z)$ is shown in Fig. 4.8. The dashed line is the upper bound of the baseband frequency with 8X oversampling used. Since the input signal U is inside the baseband, the frequency response of U is almost flat inside the baseband. The baseband gain of L(Z) is $\frac{1}{0.915} \approx 1.0929$. For the quantization noise, E_i, the average gain is difficult to determine. If gaussian white noise is assumed, the

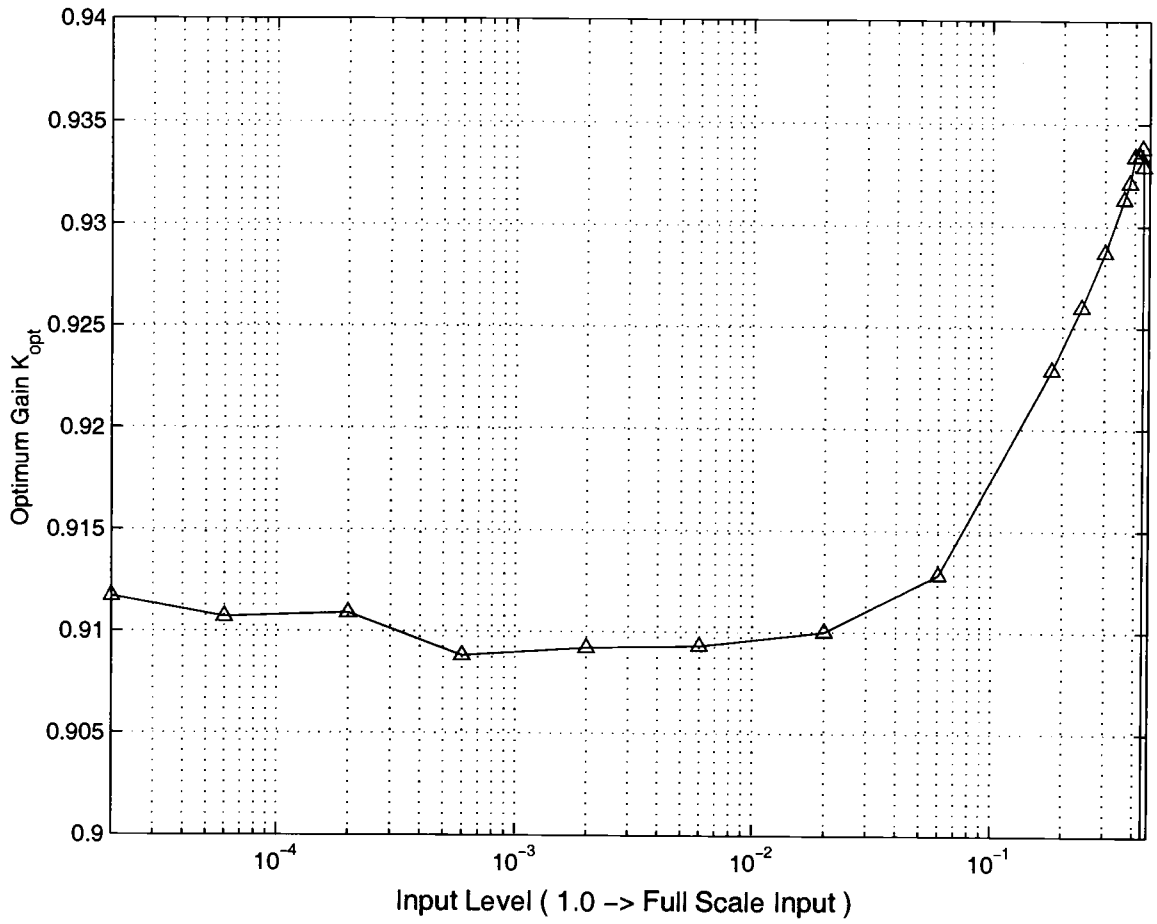


FIGURE 4.6. Optimum quantizer gain of a fifth-order hybrid $\Delta\Sigma$ modulator with $\|H\|_\infty$=6.

average gain is about 4.88 after integrating $L(Z)$ over the whole Nyquist bandwidth. Thus, the $\Delta\Sigma$ modulator becomes unstable when the quantizer input is $\frac{1}{0.81}$. Under this condition, (4.9) can be simplified into:

$$1.0929U - 4.88E_i = \frac{1}{0.81} \tag{4.10}$$

When the quantizer input Y is $\pm\frac{1}{0.81}$, E_i is approximately $\frac{1}{0.81} - 1 \approx 0.2346$. Since U and E_i are uncorrelated, (4.10) can rewritten as:

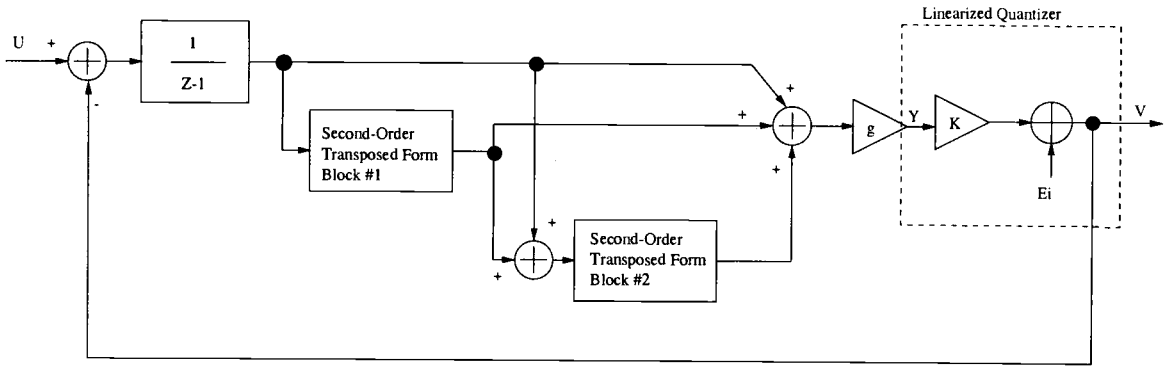


FIGURE 4.7. A simplified linear model of the fifth-order $\Delta\Sigma$ modulator.

$$(1.0929U)^2 + (4.88E_i)^2 = (\frac{1}{0.81})^2 \tag{4.11}$$

After plugging $E_i \approx 0.2346$ into (4.11), the maximum stable input U_{max} is found to be -4.98 dB.

Switcap2 simulations show that the fifth-order $\Delta\Sigma$ modulator shown in Fig. 4.3 has a maximum stable input of -8.8dB below the reference voltage. The maximum stable input, U_{max}, predicted by the linear model is 3.82 dB higher than that obtained from Switcap2 simulations. The difference is primarily from the average quantization noise gain shown in (4.10). When the $\Delta\Sigma$ modulator is on the verge of instability, the quantization noise E_i may not be white and, as a result, the gain in this case can be different from the average value. Figure 4.9 compares the two results from Switcap2 and this linear model. It shows that the linear model is a close approximation of the switcap2 simulation result. Thus, this simplified model allows us to get a quick estimate of the SNR and the maximum stable input.

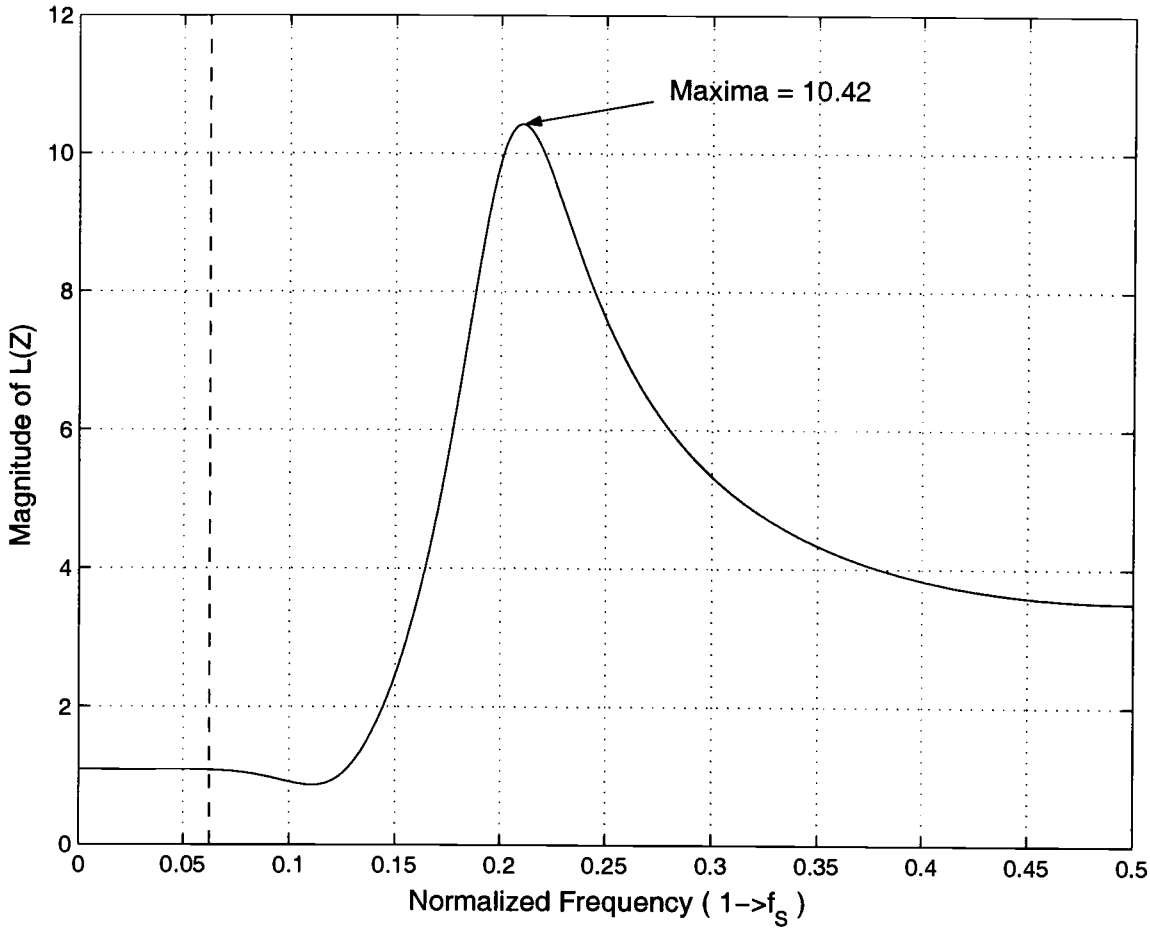


FIGURE 4.8. Frequency response of L(Z). The quantizer gain is 0.915 and the dashed line is the upper bound of the baseband frequency.

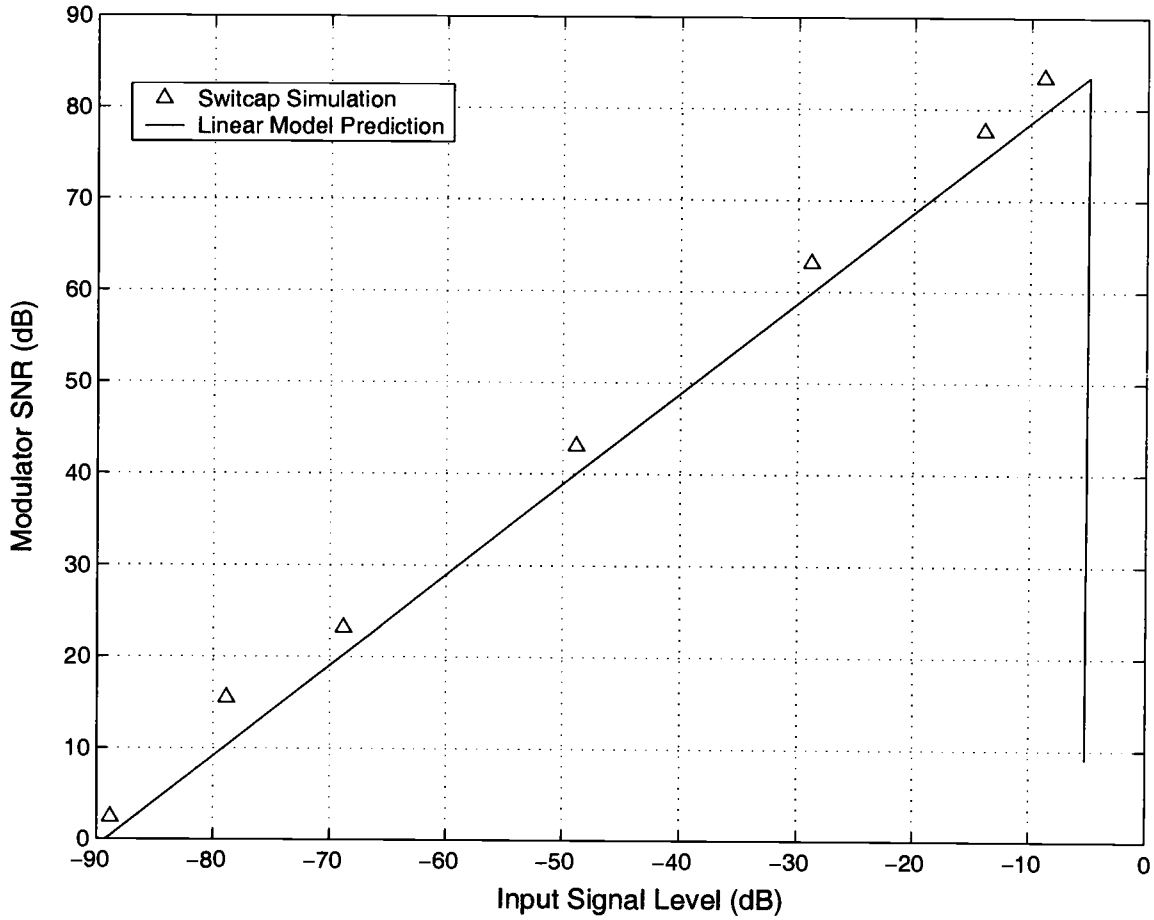


FIGURE 4.9. Comparison of the SNR as a function of input signal level obtained from Switcap2 and the linear model, respectively.

If a -6 dB attenuator is added at the input, the maximum stable input will be -2.8 dB, which is the typical input range for a $\Delta\Sigma$ modulator. For a fifth-order single-stage $\Delta\Sigma$ modulator, such an input signal range is very good.

The description of the stability of the hybrid $\Delta\Sigma$ modulator shown in Fig. 4.3 can be described in this way: The front-end integrator output has a zero delay path to the quantizer input. Thus, after the first clock period, a first-order feedback loop is formed. This loop helps to stabilize the $\Delta\Sigma$ modulator before it enters the steady state. The two second-order transposed direct form II blocks are low-Q biquad circuits with very low gain. If the inputs to these two blocks are bounded, their outputs are also bounded. Hence, if the front-end integrator output is bounded, the signal at the quantizer input is also bounded. Thus the quantizer input will not build up as do other high-order $\Delta\Sigma$ modulators, and therefore this hybrid $\Delta\Sigma$ modulator can achieve very good stability with a high $\|H\|_\infty$.

4.3. Dynamic Element Matching Algorithms

For a system with feedback, the linearity of the forward path is not very critical as long as the loop gain is high. But the linearity of the feedback path is very important. The linearity of the feedback path must be greater than the targeted system linearity to avoid corrupting the system linearity.

The hybrid modulator shown in Fig. 4.3 has a multi-bit DAC in the feedback path. The typical capacitor mismatch is about 0.1%. If the DAC is implemented by capacitor arrays, its linearity is limited to about 0.1%, which is not good enough to realize a 14-bit A/D converter.

Many methods have been developed to reduce DAC non-linearity. Digital correction techniques [20] [21] can be used to correct the errors introduced by multi-

bit DACs. The A/D converter shown in [20] uses an EPROM to store the DAC mismatch errors so that, for each quantizer output (4-bits in [20]), a high resolution output (16-bits in [20]) is used to accurately represent the actual DAC feedback. The other A/D converter shown in [21] uses a MASH structure. The error of the first stage is adaptively measured and cancelled by digital circuits. Digital correction techniques use digital circuits to minimize errors. The major advantage of digital correction is that mismatch errors are reduced instead of being noise shaped. For low oversampling applications, this is very important. For an N-bit $\Delta\Sigma$ modulator with an M-bit quantizer, the digital correction needs approximately 2^{N+M} clock periods. The digital correction is usually run before A/D conversion. If anything changes such as the temperature, the $\Delta\Sigma$ A/D must be corrected again.

Another class of techniques is *dynamic element matching* (DEM). The idea behind DEM is to select the DAC elements in such a way that DAC non-linearity error is randomized and noise-shaped. Tones caused by DAC non-linearity are suppressed and tones in the baseband are noise-shaped. There are many DEM algorithms [22], [9], [6], [23], [24], [26], [27], [28], [29], [30]. Depending on the element selecting schemes, these algorithms can provide simple randomization, first-order noise shaping or second-order noise shaping to DAC non-linear errors. Figure 4.10 shows the fifth-order hybrid $\Delta\Sigma$ modulator with dynamic element matching (DEM) control logic in the feedback path to dynamically reduce system non-linearities.

L. R. Carley proposed a random averaging algorithm [22] that randomizes DAC non-linear errors. A non-ideal multi-bit DAC can generate low frequency tones if no method is used to suppress the non-linear errors. By using a butterfly-type randomizer, the low frequency tones are smoothed and spread out throughout the whole spectrum. If the randomization is ideal (i.e., the tones are uniformly

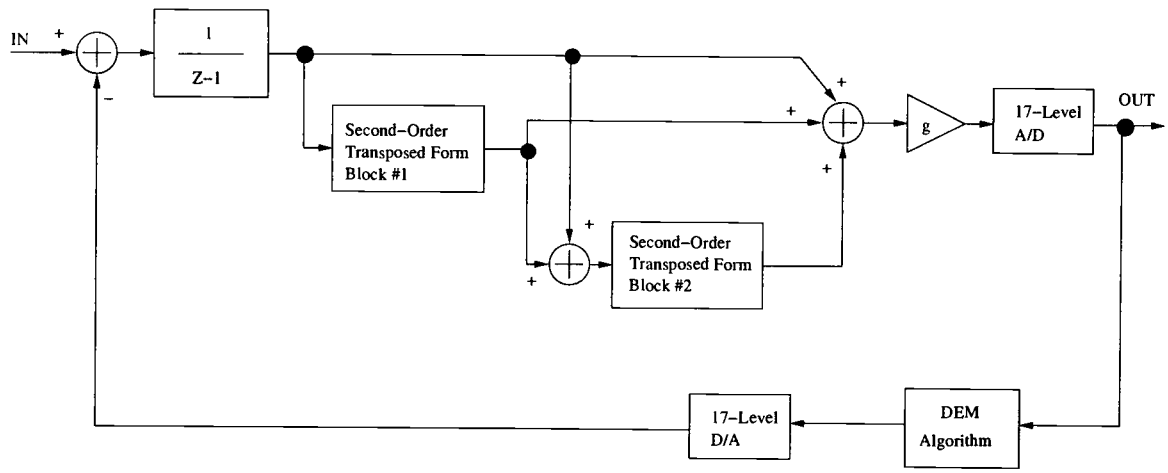


FIGURE 4.10. The fifth-order hybrid $\Delta\Sigma$ modualtor with dynamic element matching block.

smoothed), the relative baseband error N_E (i.e., the rms baseband tone amplitude divided by the DAC full scale range) is:

$$N_E = \frac{rms(\frac{\Delta E}{E})}{2\sqrt{M \times OSR}} \tag{4.12}$$

where M is the number of DAC elements, $rms(\frac{\Delta E}{E})$ is the rms value of the DAC element relative mismatch and OSR is the oversampling ratio. For a $\Delta\Sigma$ modulator with 16 DAC elements and 8X oversampling ratio, the relative baseband error $N_E \approx 0.044 \times rms[\frac{\Delta E}{E}]$. The attenuation is not high, because the oversampling ratio is low. As the oversampling ratio increases, the baseband error portion will inversely decrease. In general, this DEM algorithm is not suitable for $\Delta\Sigma$ modulators because it increases the frequency noise floor. The random averaging algorithm spreads out DAC mismatch errors over the entire spectrum which swamps out the noise shaping of the overall $\Delta\Sigma$ modulator.

By choosing the DAC elements in a particular way, the DAC mismatch errors can be noise-shaped instead of being evenly spread out over the entire spectrum. There are many algorithms [9], [23], [24], [25], [6], [26] that can provide first-order noise shaping to DAC mismatch errors. *Data weighted averaging* (DWA) [9] is a typical algorithm. DAC elements are selected in a circular fashion. If at time $t = n - 1$ some DAC elements are used and the last element used is the k-th element, at time $t = n$ the DAC elements starting from the $(k + 1)$ -th element will be used. For an N-level DAC, there are (N-1) elements. DAC mismatch errors will sum to zero in no more than (N-1) clock cycles. Thus DAC error energy is moved to high frequencies and the baseband distortion is noise shaped. Since the DAC elements are rotated through repeatedly, it is possible that DAC mismatch errors can form a periodic pattern. This can introduce tones in the baseband. To reduce the tones, a small dither sometimes is needed.

Another algorithm called *Individual Level Averaging* (ILA) is proposed by B. Leung [24]. This algorithm assigns an index to each DAC output level. For each output code k, all DAC elements are used an equal number of times. There are different methods to realize this. One way is called the "rotation approach" [24]. If the DAC elements starting from the $1st$ to the $k - th$ are used for the last DAC code of K, elements starting from the $2nd$ to the $(k + 1) - th$ will be selected for the next output code K. Another way is called the "addition approach" [24]. If DAC elements starting from the 1st to the k-th are used for the last DAC code of K, elements starting from the (k+1)-th to the 2K-th will be selected for the next output code K. Obviously, the "rotation approach" takes M times to cycle through all the DAC elements, where M is the number of DAC elements. The "addition approach" can take less time to cycle through all the DAC elements. Simulation shows that the "addition approach" can achieve higher SNR than the "rotation approach" [24].

This algorithm requires more memory than other algorithms. But this algorithm provides more choices for selecting DAC elements and it is less likely to form a periodic pattern. Thus, the tonal behavior is usually less than the DWA algorithm. One drawback of this algorithm is that this algorithm cycles through the DAC elements more slowly than the DWA algorithm, and as a result, the noise-shaping of ILA algorithm is not as aggressive as the DWA algorithm.

Double Index Averaging (DIA) [23] and *Bi-directional Data Weighted Averaging* (BiDWA) [6] are two similar algorithms. The DIA algorithm uses two indices for the positive output and the negative output, respectively. If the output is positive, one index will be used. If the output is negative, the other index will be used. Both indices move in the same direction. The BiDWA algorithm uses two indices to memorize the last DAC elements used for even samples and odd samples, respectively. For the next even sample, the even index will be used and it will move in one direction. For the next odd sample, the odd index will be used and it will move in the opposite direction. Both algorithms provide first-order noise shaping to DAC mismatch errors. By using two indices to randomize the output sequence, the possibility of forming a periodic pattern is less than that of the DWA algorithm.

All the first-order algorithms mentioned above select DAC elements in some form of a circular way. It is possible for all of them to form a periodic pattern sometimes. *Rotated Data Weighted Averaging* (RDWA) [26] is an algorithm that has multiple circles in its state diagram. When the control logic rotates within a circle, it is actually running the DWA algorithm. The finite state machine will randomly jump from this circle to another in order to avoid forming a periodic pattern. The logic control becomes very complicated as the number of levels of the DAC increases. From the simulation results of [26], this algorithm provides very good supression of tones.

To gain insight into these first-order algorithms, the number of indices is considered for each algorithm used. The DWA algorithm uses one index in a circular way. Sometimes it can form a periodic pattern. ILA algorithm with the "addition approach" uses multiple indices: One index for each DAC level. This algorithm randomizes the output sequence and it is less likely to form a periodic pattern. The DIA and BiDWA algorithms use two indices to supress tones. RDWA has only one index. But the index jumps randomly, which also helps to reduce tones. Figure 4.11 shows examples of three commonly used first-order DEM algorithms: DWA, BiDWA and ILA algorithms. The multi-bit DAC is assumed to have 8 elements. The indices of all algorithm start at the first element.

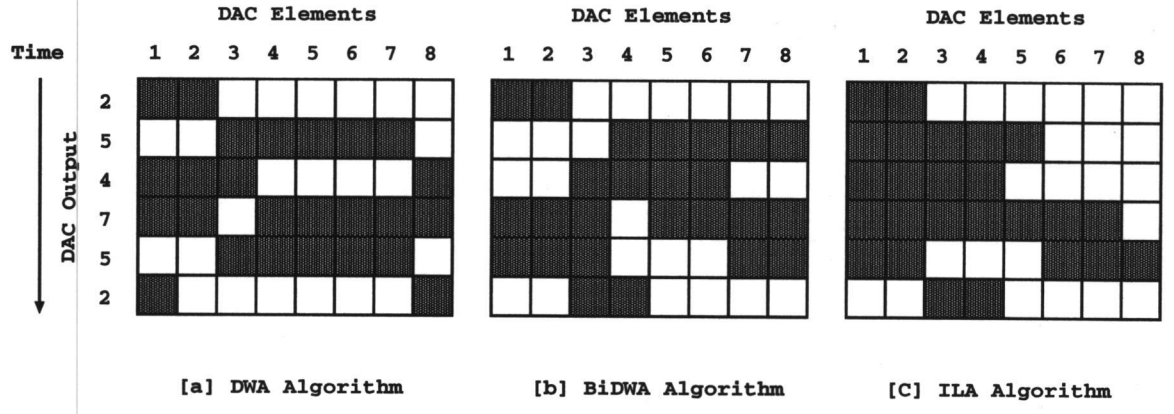


FIGURE 4.11. Examples of three first-order DEM algorithms: (a) data weighted averaging algorithm, (b) bi-directional data weighted averaging algorithm, (c) individual level averaging algorithm.

The algorithms discussed above first-order noise shape the DAC mismatch errors. Second-order noise shaping can be achieved by using different (in general more complicated) algorithms.

Schreier and Zhang proposed a new algorithm [27], [28], which provides second-order noise shaping to DAC mismatch errors. In the element selection logic, a digital second-order $\Delta\Sigma$ modulator is used to shape the DAC mismatch errors. This algorithm involves data sorting and the stability of the digital $\Delta\Sigma$ modulator is conditional. Instead of sorting data, a tree structure can be used to reduce the total number of transistors.

The $\Delta\Sigma$ modulator proposed by Yasuda demonstrates another way to achieve second-order noise shaping on DAC mismatch errors [29]. A tree structure is employed to avoid data sorting and to reduce gate count. This algorithm requires a large number of adders, registers and digital comparators.

The algorithm proposed by Galton [30] also provides second-order noise shaping to DAC mismatch errors. The element selection logic also has a tree structure. The circuit complexity of the element selection logic is similar to that of [29].

This work targets a $\Delta\Sigma$ modulator with 8X oversampling ratio and 32 MHz clock rate. The time allocated to the DEM algorithm execution is less than one clock period. Thus the DEM algorithm to be used must be fast and simple. Any algorithm that requires more than one clock period cannot be used.

The algorithm proposed in [27], [28] requires data sorting. Data sorting is usually implemented by multiple clock period schemes. Although it can be implemented by combinational logic, the complexity of the combinational logic is prohibitively high. The other two second-order algorithms [29], [30] provide simplified solutions to this problem. But both of them use tree-like topologies, which have several layers of combinational logic. The delay of the combinational logic is very large. Another issue is that when the oversampling ratio is low, the improvement obtained from the second-order algorithms over the first-order algorithms is smaller. The $\Delta\Sigma$ A/D in [30] has about 5 dB SNDR difference between the first-order and

second-order algorithms at 64X oversampling. It has been reported [28] that the SNDR difference between first-order and second-order algorithms is insignificant when the oversampling ratio is below 30. Second-order algorithms are more suitable for applications with high oversampling ratios, such as audio $\Delta\Sigma$ A/D converters and instrumentation $\Delta\Sigma$ A/D converters. Hence, second-order algorithms are not adopted for this design.

Among the first-order algorithms, ILA requires more memory than the others and the logic is also complicated. RDWA algorithm also has very complicated control logic. Thus DWA, DIA and BiDWA are possible choices for this design. As mentioned before, DWA provides the most aggressive noise shaping among first-order algorithms, but it is likely to have more tones in the baseband. DIA and BiDWA have less tones but their noise shaping is not as aggressive as DWA. Figure 4.12 shows the difference between the BiDWA algorithm and the DWA algorithm. It is evident that the tones are much less with BiDWA than with DWA. But at the same time the noise floor with BiDWA is higher than that with DWA. The DWA algorithm generates tones when a periodic pattern is formed. But if a $\Delta\Sigma$ modulator is high order, the correlation between the quantization noise and the input signal is much less and so the tones will be less. Under this condition, it is more desirable to have a more aggressive noise shaping on DAC mismatch errors than to have less tones at the expense of less aggressive noise shaping.

A C program is developed to simulate the fifth-order $\Delta\Sigma$ modulator with the different algorithms. Circuit non-idealities are considered in the simulations. The opamp DC gain is 43 dB with a unity-gain bandwidth of 280 MHz. The DAC unit capacitor mismatch is assumed to be a guassian distribution with $\sigma = 0.001$. Circuit coefficient variations are also taken into account. A standard deviation

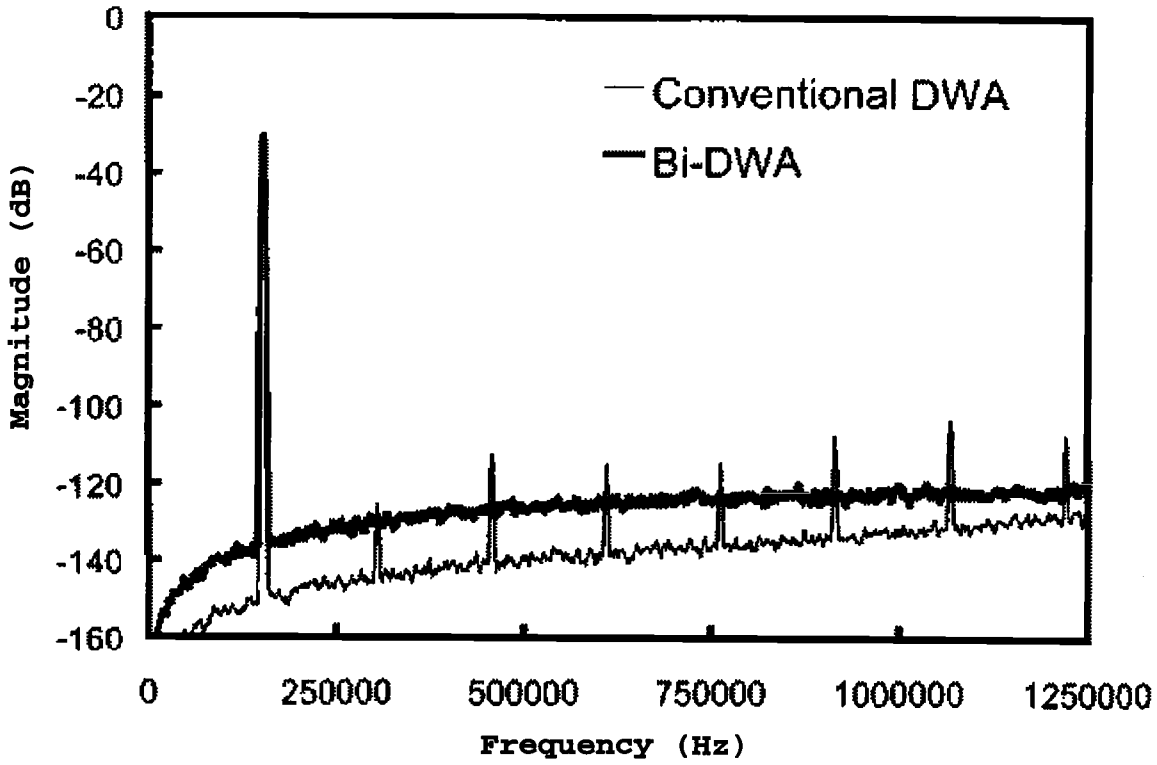


FIGURE 4.12. Spectra of BiDWA and DWA algorithms.

of 0.1% is used and the maximum clock jitter is 10 pico seconds. Figure 4.13 shows the simulation results for different algorithms. In Fig. 4.13(a), no algorithm is used and the SNDR is 77.57 dB. The tones caused by the DAC non-linearity are very large. Figure 4.13(b)(c)(d) are the results with DWA, DIA and BiDWA algorithms, respectively. It can be seen that all three algorithms have very small tones because of the high-order modulator structure. The DWA algorithm has the most aggressive baseband DAC mismatch noise shaping. Thus the baseband equi-ripple noise shaping is retained and the SNDR is 82.66dB. The DIA and the BiDWA algorithms have less aggressive noise shaping, which results in smeared baseband

DAC mismatch noise shaping. Thus the DIA and the BiDWA algorithms result in a little lower SNDR than the DWA algorithm. For this reason, this $\Delta\Sigma$ modulator achieves the best result with the DWA algorithm instead of the DIA or the BiDWA algorithm. The SNDR with the DIA algorithm is very close to that with the BiDWA algorithm, because both algorithms use two indices and the DAC mismatch noise shaping curves are very similar.

It should be noted that the $\Delta\Sigma$ A/D converters shown in [25] and [6] use simple second-order structures. For a second-order $\Delta\Sigma$ modulator, the quantization noise is likely to be correlated with the input signal and the DAC mismatch tends to generate tones. That is the reason these A/D converters get better results with the ILA and the BiDWA algorithms than with the DWA algorithm. For high order $\Delta\Sigma$ modulators, tones are unlikely to be generated and aggressive DAC mismatch noise shaping is more important for suppressing the tones.

Figure 4.14 shows the SNDR as a function of DAC unit capacitor mismatch for different algorithms. Each point in Fig. 4.14 is the average of 100 simulations. The four curves correspond to the SNDR without any algorithm, the SNDR with the DWA algorithm, the SNDR with the DIA algorithm and the SNDR with the BiDWA algorithm. Without any algorithm, the SNDR starts to roll off as the capacitor mismatch increases. With the DWA algorithm, the SNDR remains greater than 80 dB for DAC unit capacitor mismatches $\sigma < 0.33\%$ and the roll off of the SNDR is the the most gradual. The DIA and BiDWA algorithms have a similar effect on SNDR. They are better than without any algorithm, but they roll off faster than that with the DWA algorithm. The difference between the DWA algorithm and the DIA and BiDWA algorithms becomes larger as the DAC unit capacitor mismatches

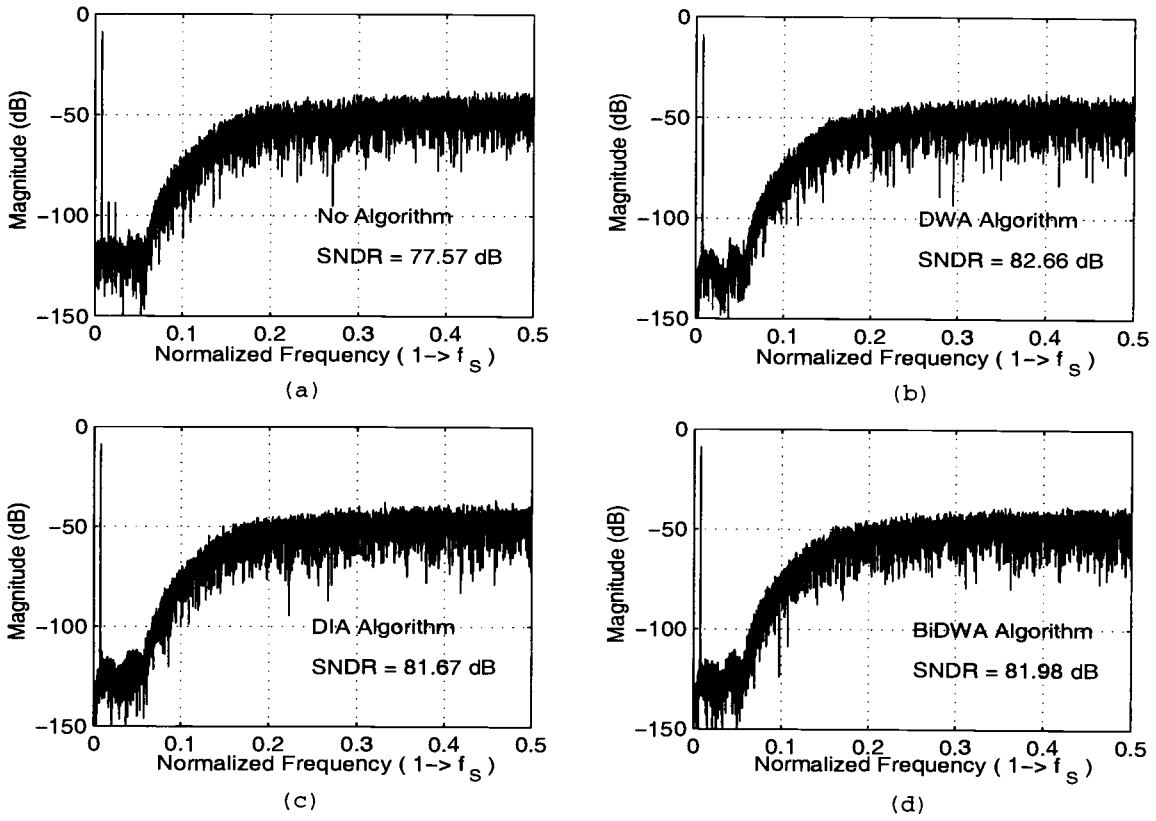


FIGURE 4.13. Comparison of different DEM algorithms with DAC capacitor mismatch $\sigma = 0.1\%$, opamp DC gain $\approx$ 43dB, and the maximum clock jitter of 10 ps. (a) No DEM algorithm is used, (b) DWA algorithm is used, (c) DIA algorithm is used, (d) BiDWA algorithm is used.

increase. From all these simulation results, it can be seen that the DWA algorithm is the most suitable one for this $\Delta\Sigma$ modulator.

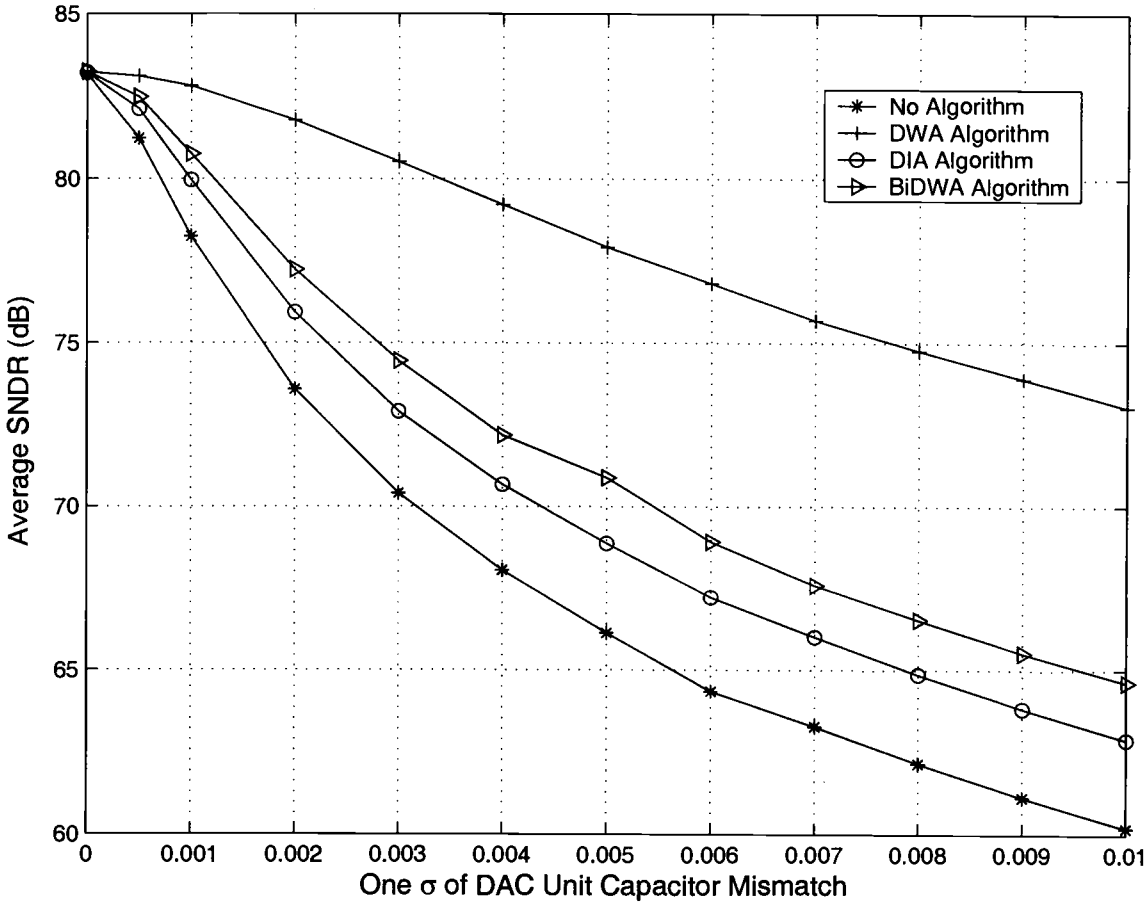


FIGURE 4.14. SNDR as a function of DAC unit capacitor mismatch for different algorithms. Each point is the average of 100 simulations.

4.4. Coefficient Quantization

The ideal coefficients of the fifth-order $\Delta\Sigma$ modulator are shown in Table 4.1. In practical design, the values are quantized to $\frac{n}{m}$, where m, n are integers so that the coefficients can be realized by unit capacitors. Unit capacitor implementations of coefficients can be more accurate and less sensitive to process variations. Additionally, ideally m and n will be as small as possible without degrading system

performance. Small m and n results in less overall capacitance and, consequently, reduced die area and power consumption.

To quantize circuit coefficients, the sensitivity of coefficients must be analyzed. Sensitivity is defined as [31]:

$$S_x^y = \frac{\Delta y/y}{\Delta x/x} \tag{4.13}$$

where x denotes a coefficient value and y denotes the circuit parameter being considered. To determine the overall performance, the sensitivity of the SNR to circuit coefficients is needed. Since other $\Delta\Sigma$ modulators are unstable with $\|\mathrm{H}\|_\infty = 6$, we are unable to make comparisons between the hybrid $\Delta\Sigma$ modulator and other $\Delta\Sigma$ modulators with respect to SNR. An alternative is to compute the sensitivity of the pole-zero positions to circuit coefficient variations. If the pole-zero positions of a $\Delta\Sigma$ modulator are very sensitive to coefficient variations, the SNR of the $\Delta\Sigma$ modulator (if the modulator is stable) is probably very sensitive to coefficient variations. Figure 4.15 shows the poles and zeros of the fifth-order $\Delta\Sigma$ modulator. The distance between the pole P_3 and DC is L. If a coefficient x varies a small amount Δx, the pole will move to P_3'. The distance between P_3 and P_3' is ΔL. Then the sensitivity of P_3 to the coefficient x is:

$$S_x^{P_3} = \frac{\Delta L/L}{\Delta x/x} \tag{4.14}$$

The noise transfer function of the fifth-order hybrid $\Delta\Sigma$ modulator is:

$$NTF(Z) = \frac{1}{1+L(Z)} \tag{4.15}$$

$$L(Z) = \frac{g}{Z-1}\left[\frac{Z^2+(b_{21}-a_{21})Z+(b_{22}-a_{22})}{Z^2-a_{21}Z-a_{22}}\right]\left[\frac{Z^2+(b_{11}-a_{11})Z+(b_{12}-a_{12})}{Z^2-a_{11}Z-a_{12}}\right] \tag{4.16}$$

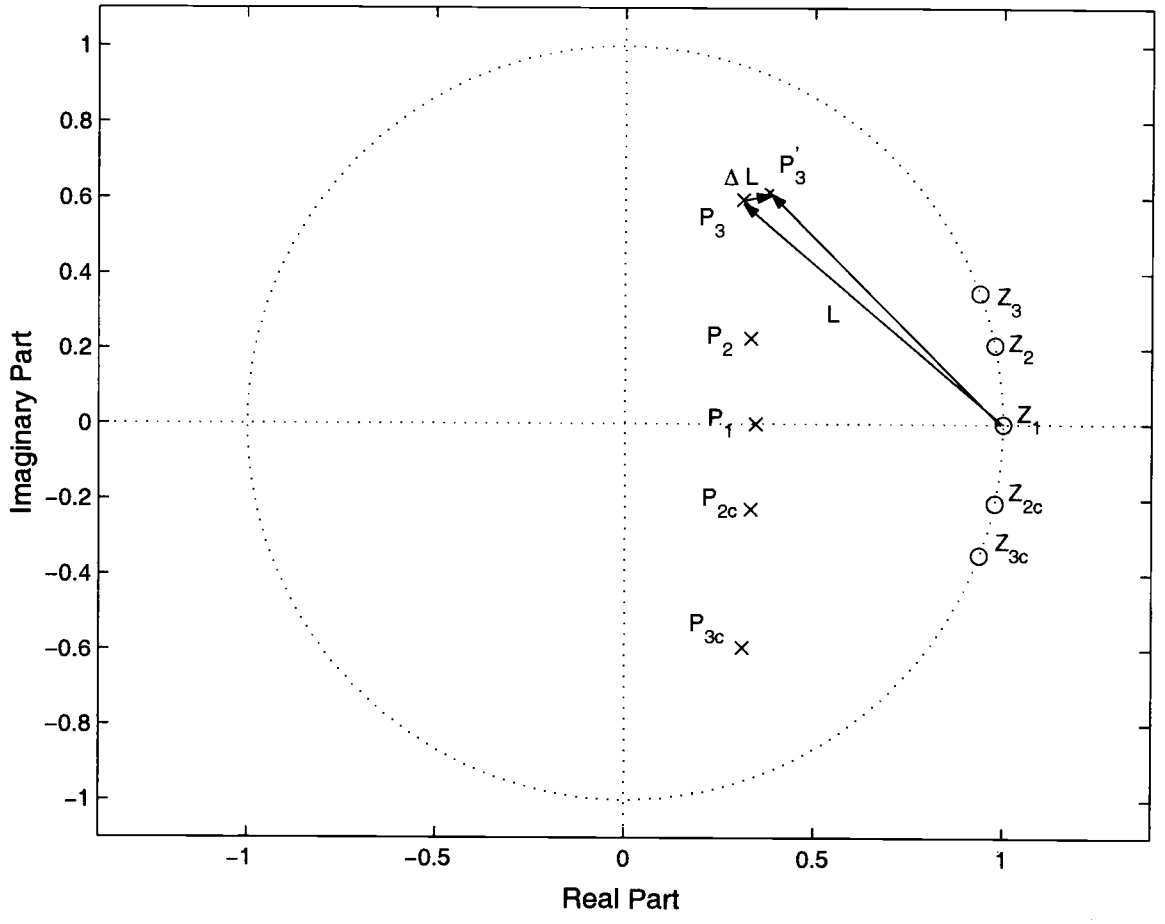


FIGURE 4.15. The illustration of pole/zero sensitivity to coefficient variation.

where the subscripts have the same meaning as in Table 4.1. The sensitivity of the pole/zero positions to coefficient variations is shown in Table 4.2. Zero Z_1 is generated by the front-end integrator and does not change as g, a_{ij} and b_{ij} change. Thus the sensitivity of Z_1 is not shown in Table 4.2.

As a comparison, the sensitivity of the pole/zero positions to coefficient variations of the leapfrog $\Delta\Sigma$ modulator shown in Fig. 3.1 are shown in Table 4.3 The coefficient b_1 shown in Fig. 3.1 is always zero. Thus b_1 is not included in Table 4.3.

TABLE 4.2. The pole/zero sensitivity of the fifth-order hybrid $\Delta\Sigma$ A/D converter shown in Fig. 4.3 to circuit coefficient variations with $\|H\|_\infty$ =6.

Sensitivity	P_1	P_2	P_3	Z_2	Z_3
g	19.8	8.3	2.6	0	0
a_{11}	1.3	4.6	4.5	0	7.9
a_{12}	3.1	5.5	3.1	0	4.0
b_{11}	5.7	4.4	2.6	0	0
b_{12}	5.2	4.6	1.8	0	0
a_{21}	43.1	47.7	5.3	24.9	0
a_{22}	40.8	22.9	4.1	10.61	0
b_{21}	17.8	13.4	3.3	0	0
b_{22}	57.8	42.7	5.0	0	0

Comparing Table 4.2 with Table 4.3, we see that the sensitivity of the hybrid $\Delta\Sigma$ modulator is much lower than that of the leapfrog $\Delta\Sigma$ modulator.

The maximum sensitivity of the NTF zeros of the hybrid $\Delta\Sigma$ modulator is 24.90 and for the NTF poles, it is 57.76. Each zero pair is controlled by one transposed direct form II block. This ensures that the NTF zeros are shifted very little after coefficient quantization. The sensitivity of the poles is a little higher than that of the zeros, since $\|H\|_\infty$ is very high. All NTF poles are far away from DC in the Z-plane. A little pole shift does not have a significant effect on the noise shaping. Thus, the noise shaping of the hybrid $\Delta\Sigma$ modulator is not affected by coefficient quantization.

The maximum zero sensitivity of the leapfrog $\Delta\Sigma$ modulator is 2517 and it is very difficult to obtain accurate baseband noise shaping. The maximum pole sensitivity is 411 which also makes it very difficult to control the poles after coeffi-

TABLE 4.3. The pole/zero sensitivity of the fifth-order leapfrog $\Delta\Sigma$ A/D converter (shown in Fig. 3.1) to circuit coefficient variations with $\|H\|_\infty$ =6.

Sensitivity	P_1	P_2	P_3	Z_1	Z_2	Z_3
a_1	68.85	38.74	9.636	0	0	0
a_2	410.63	334.87	15.36	0	0	0
a_3	101.99	53.208	9.1548	0	0	0
a_4	22.512	14.371	2.403	0	0	0
a_5	11.362	6.214	0.709	0	0	0
b_2	5.045	3.008	0.526	2516.95	0.4808	0.06705
b_3	1.485	0.9016	0.14099	419.066	0.1135	0.0979
b_4	9.510	5.012	0.4528	712.092	0.1886	0.4386
b_5	0.6611	0.6131	0.1005	1938.580	0.1239	0.2054

cient quantization. The leapfrog $\Delta\Sigma$ modulator analyzed here is a typical example, however, all the $\Delta\Sigma$ modulators mentioned in Chapter 3 have the same limitation.

From the above comparison, it is clear that the hybrid $\Delta\Sigma$ modulator has very low sensitivity. This allows the aggressive quantization of the circuit coefficient and produces a modulator that is also tolerant of manufacturing variations.

In order to optimize power consumption, the coefficients must be simple and easy to realize. It is better to use unit capacitors to implement these coefficients because the total number of capacitors will be as small as possible. Since the poles and zeros have very low sensitivity to coefficient variations, aggressive coefficient quantization is used to simplify the layout. The original coefficient and the final quantized coefficient values are shown in Table 4.4.

b_{12} has the maximum relative quantization error of 3.135%. This is because b_{12} has very low sensitivity. Such high quantization error can corrupt a $\Delta\Sigma$ modu-

TABLE 4.4. The coefficient values of the fifth-order hybrid $\Delta\Sigma$ modulator before and after coefficient quantization with $\|H\|_\infty$ =6.

Coefficients	Before Quantization	After Quantization
g	3.2	3.2
a_{11}	1.9	1.9
a_{12}	-1.0	-1.0
b_{11}	0.59	0.59
b_{12}	-0.24	-0.25
a_{21}	1.9	1.9
a_{22}	-1.0	-1.0
b_{21}	0.73	0.73
b_{22}	-0.60	-0.60

lator with high coefficient sensitivity, but for this hybrid $\Delta\Sigma$ modulator, the effect is very small.

Figure 4.16 shows the pole/zero positions before and after coefficient quantization. After coefficient quantization, the NTF zeros change very little. The pole on the real axis moves closer to DC, but at the same time, the pole pair far away from the real axis also move further away from DC. The combined effect results in an output spectrum very close to that before coefficient quantization.

Figure 4.17 shows the spectra of the hybrid $\Delta\Sigma$ modulator before and after coefficient quantization. The noise shaping envelope is almost unchanged after coefficient quantization. The difference in SNDR is 82.42dB compared to 82.37dB.

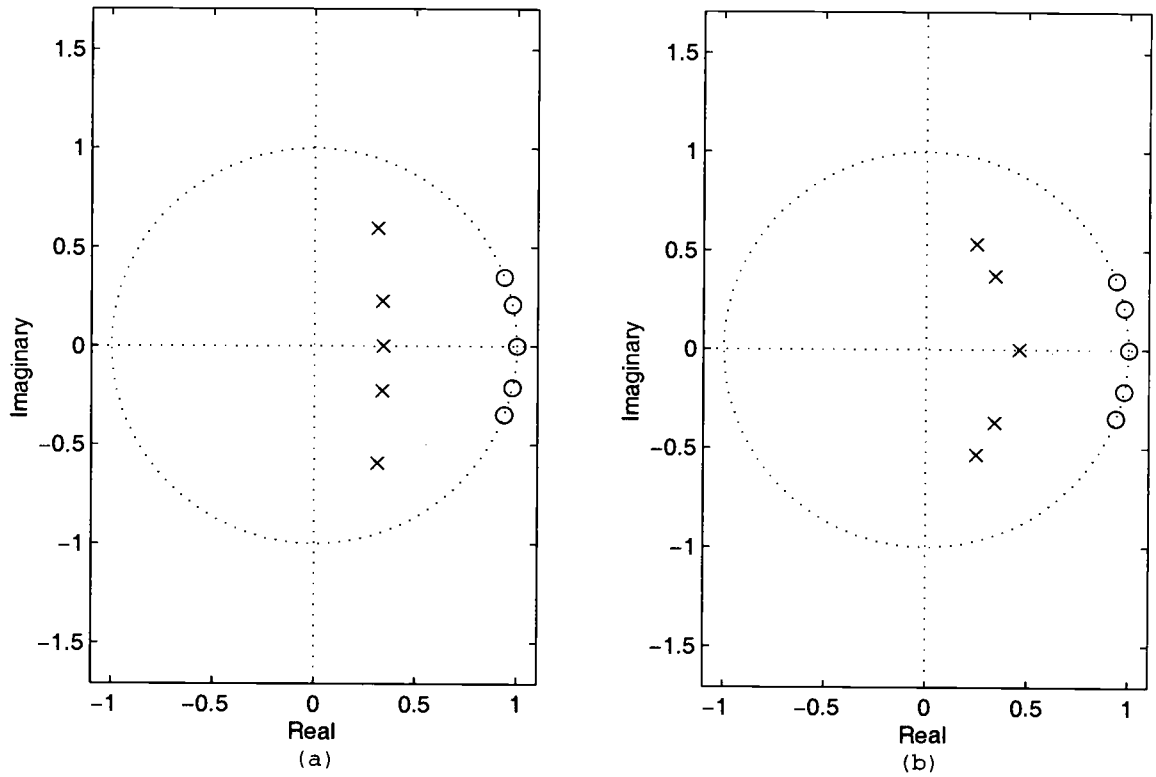


FIGURE 4.16. Pole/zero positions of the fifth-order hybrid $\Delta\Sigma$ modulator, (a) pole/zero positions before coefficient quantization, (b) pole/zero positions after coefficient quantization.

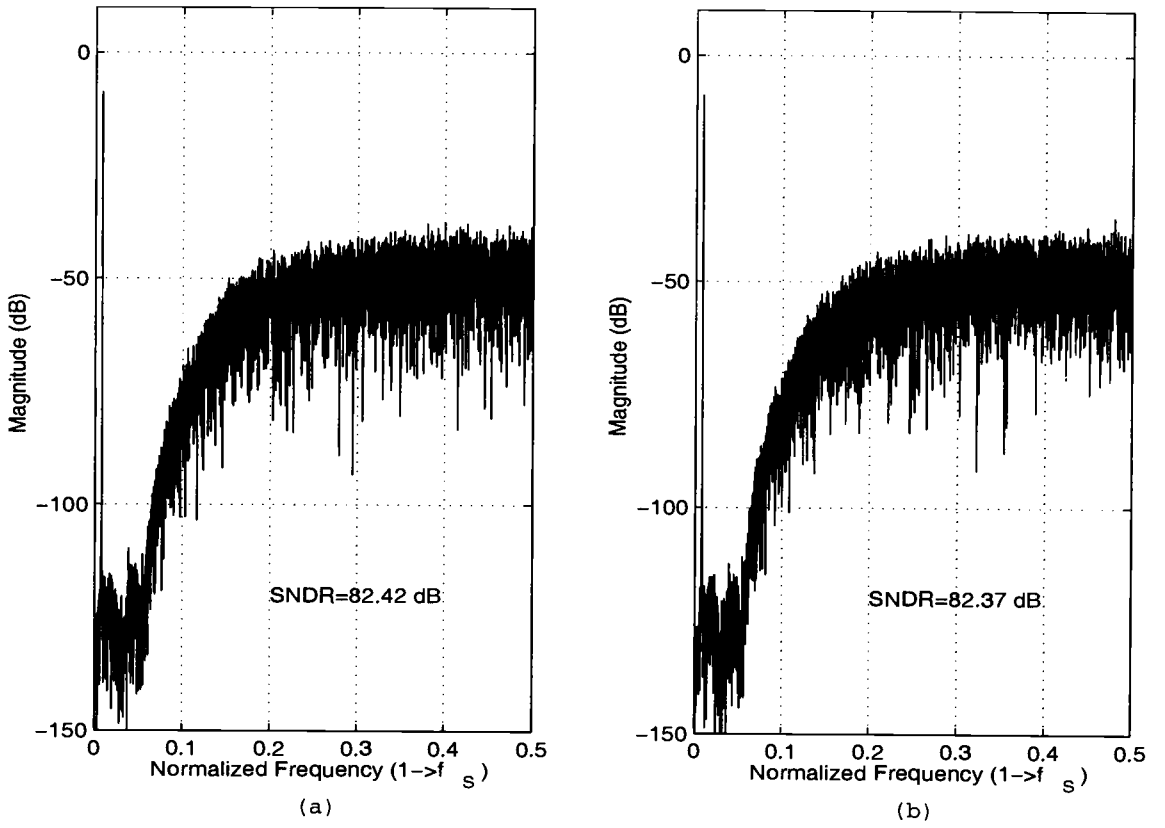


FIGURE 4.17. Spectra of the fifth-order hybrid $\Delta\Sigma$ modulator, (a) before coefficient quantization, (b) after coefficient quantization.

4.5. Simulation Results

A C program is used to run Monte Carlo simulations of the $\Delta\Sigma$ modulator under various conditions. The modulator coefficients are quantized and device errors such as KT/C noise, capacitor mismatch, finite opamp DC gain, clock jitter and comparator offset voltage and hysterisis are taken into account. All error terms have Gaussian distributions with all standard deviations set to the typical values of a 0.18 μm CMOS process.

Figure 4.18 shows the Monte Carlo simulation results for 1024 simulations. The DAC unit capacitors have 0.1% mismatch and the DWA algorithm is used. The mean SNDR is 82.78 dB with a standard deviation of only 0.45dB and all simulated SNDRs are greater than 81 dB.

In Fig. 4.19 everything is the same as in Fig. 4.18 except that no DEM algorithm is used. The mean SNDR is only 78.20 dB, which is 4.5 dB less than that with the DWA algorithm. Another interesting result is that the standard deviation is now 2.01 dB, which is much higher than that with the DWA algorithm. Thus the DEM algorithms not only increase SNDR but also reduce the standard deviation of the SNDR.

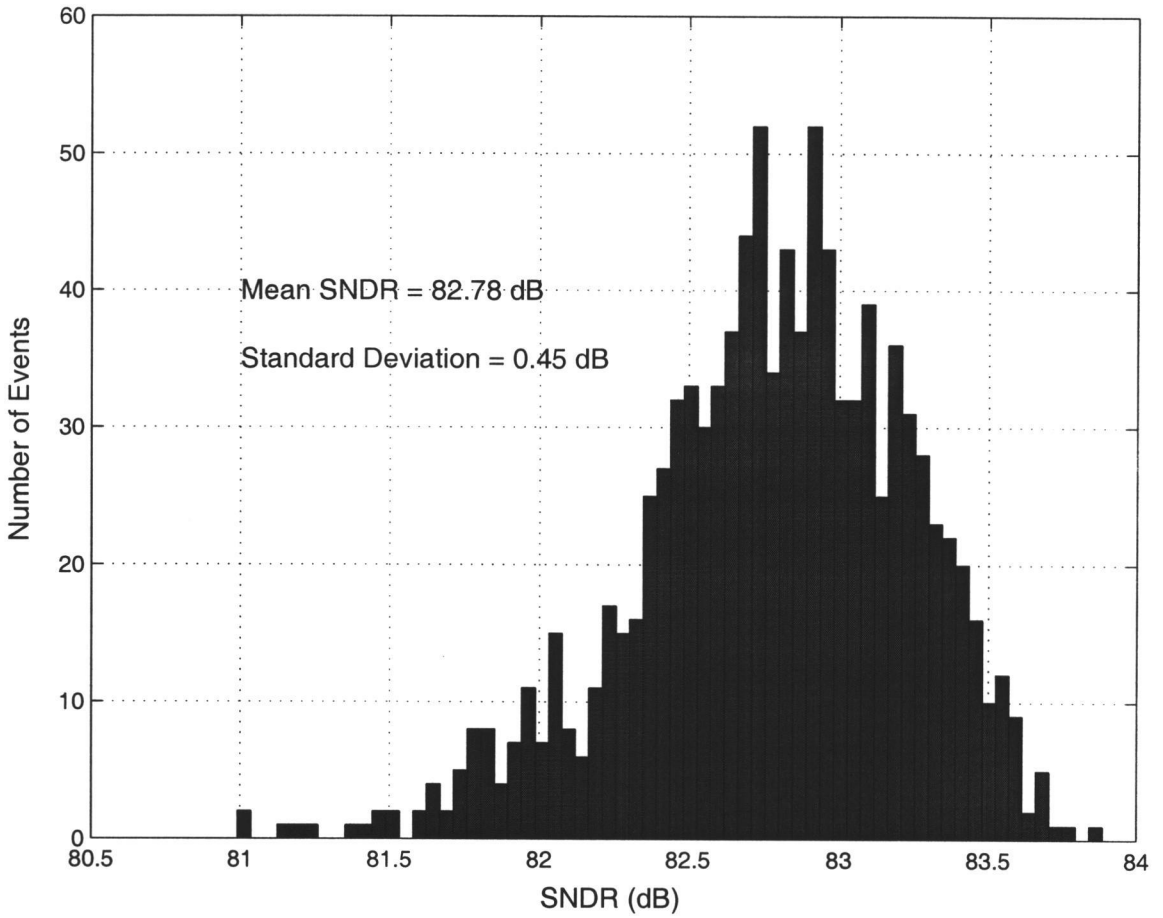


FIGURE 4.18. Monte Carlo simulation of the $\Delta\Sigma$ modulator with the DWA algorithm after coefficient quantization. The DAC capacitor mismatch is $\sigma = 0.1\%$, the opamp DC gain $\approx$ 43dB, and the maximum clock jitter is 10 ps.

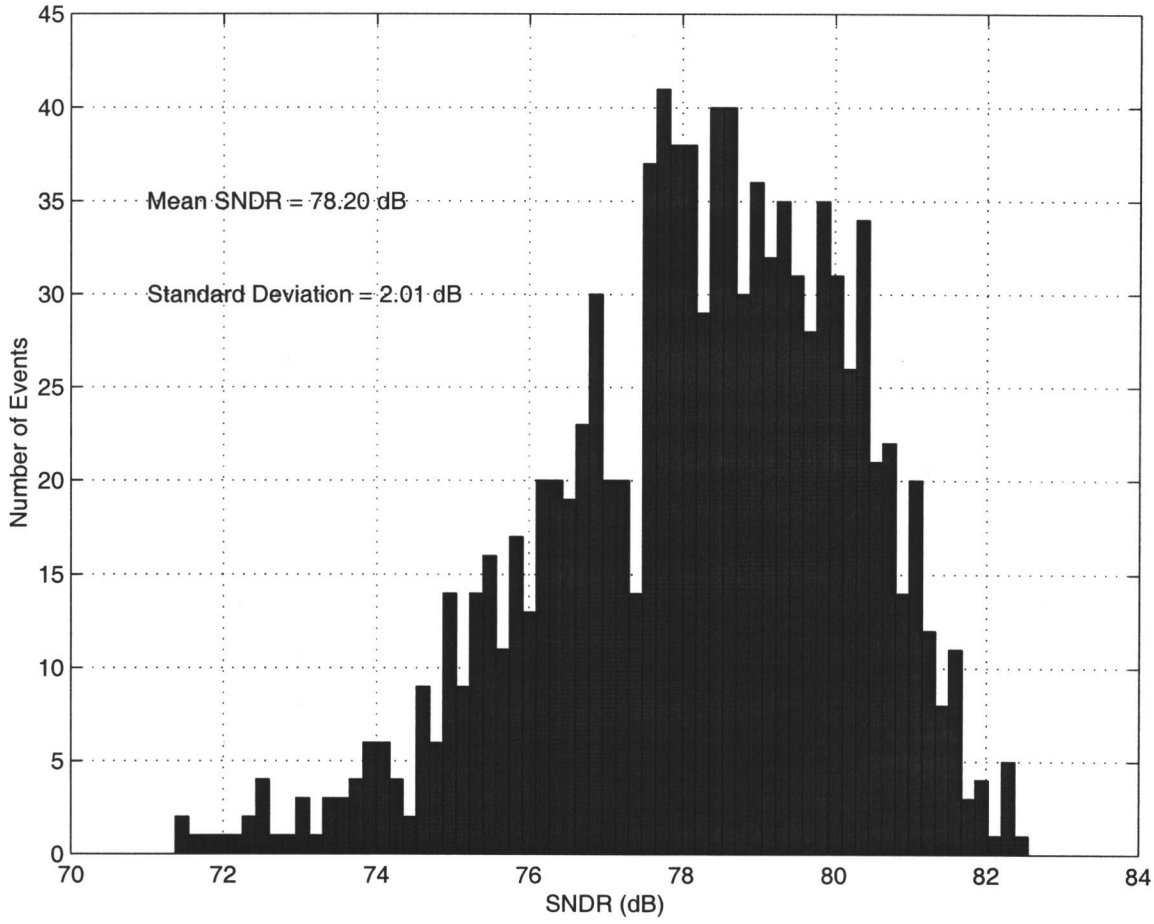


FIGURE 4.19. Monte Carlo simulation of the $\Delta\Sigma$ modulator after coefficient quantization without a DEM algorithm. The DAC capacitor mismatch is $\sigma = 0.1\%$, the opamp DC gain $\approx$ 43dB, and the maximum clock jitter is 10 ps.

4.6. Conclusion

This hybrid $\Delta\Sigma$ modulator provides a direct mapping between the NTF pole-zero locations and the modulator coefficients. By using this structure, a high $\|H\|_\infty$ can be used to boost the signal-to-noise ratio and remove tones in the baseband. The simple relationship also allows aggressive coefficient quantization. Simulations show that the fifth-order hybrid $\Delta\Sigma$ modulator does not have noticeable SNDR degradation with coefficient quantization errors up to 3%. As a result, fewer and smaller capacitors can be used without corrupting the modulator performance. Monte Carlo simulations demonstrate that the hybrid $\Delta\Sigma$ modulator structure is a very stable and robust architecture.

This hybrid structure also has a very simple front-end. There is no distributed feedback or feedforward paths at the front-end. This helps reduce the die size and the power consumption, since the front-end usually consumes more power and area than the circuits that follow. There is only one feedback loop, which helps to avoid the use of multiple multi-bit DACs [4] or a current-mode multi-bit DACs [14].

A comparison between several DEM algorithms is presented in this chapter. Second-order algorithms are not employed in this design due to circuit complexity and speed limitations. Among the first-order DEM algorithms, DWA has been shown to be the most suitable for the low oversampling high-order $\Delta\Sigma$ modulator. It can provide the most aggressive DAC mismatch noise shaping when compared to other first-order algorithms. Additionally, the baseband tones with the DWA algorithm are also very small due to the high-order structure.

5. DESIGN OF A 1.8-V 14-BIT ΔΣ A/D CONVERTER WITH 8X OVERSAMPLING AND 2 MHZ INPUT SIGNAL BANDWIDTH

5.1. Block Diagram of the A/D Converter

The block diagram shown in Fig. 4.3 and the implementation described in Chapter 4 has approximately -8.85 dB maximum stable input. Typically, the maximum stable input of a ΔΣ A/D is about -3dB. To achieve the -3 dB level, a -6 dB attenuator is employed at the front-end. Thus the input referred maximum stable input is increased to -2.85 dB. A DWA algorithm is used in the DAC feedback path and the entire block diagram of the ΔΣ modulator is shown in Fig. 5.1. To ensure the ΔΣ modulator is stable, switches are used to discharge all integrating capacitors during power up.

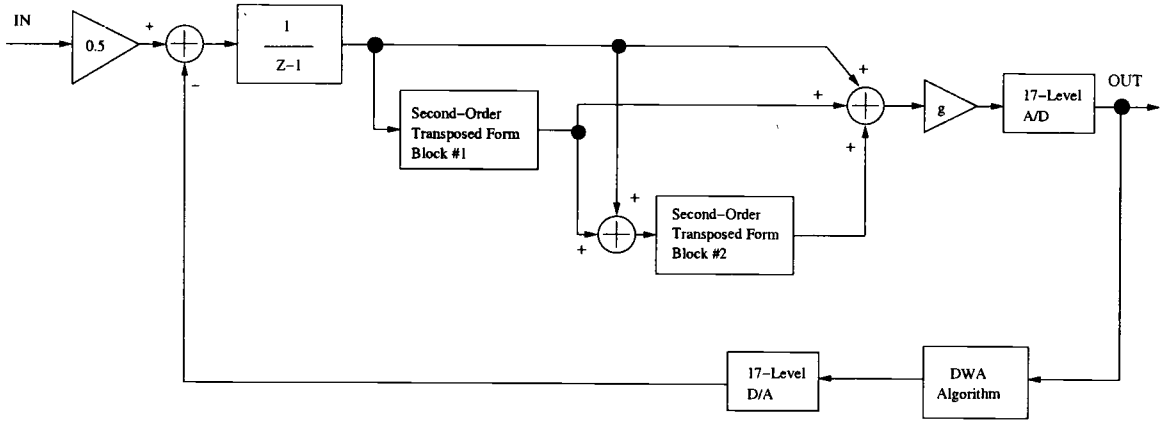


FIGURE 5.1. Block diagram of the fifth-order ΔΣ A/D converter.

This block diagram has an integrator at the front-end, two second-order transposed direct form II blocks, a summing amplifier with a gain of 3.5, a 4-bit flash A/D and DWA control logic in the feedback path. Thermal noise, flicker noise and KT/C noise at the front-end integrator are usually the dominant sources of noise. Power consumption of the front-end integrator is usually much higher than the following blocks. Thus we need to design a front-end integrator with good linearity, small input-referred noise and moderate power consumption.

In the following sections, the design considerations and details about the front-end integrator, the two second-order transposed direct form II blocks, the summing-amplifying block, the 4-bit flash A/D and the data weighted averaging logic circuit will be discussed.

5.2. Front-End Integrator Design

The front-end integrator is the most important part of the $\Delta\Sigma$ A/D converter. The KT/C noise, flicker noise and thermal noise must be characterized and the non-linearity of the DAC unit capacitors must be controlled so that it is not the limiting factor of the A/D converter. To successfully design such a front-end integrator, the transistor circuit design must take all the process variations and limits into account. A 0.18 μm, 1.8 V CMOS process is used for this A/D converter and as a result, the output dynamic range of the front-end opamp is only $\pm 0.6 V_{P\_P}$. Thus, the opamp must have large input transistors to reduce the flicker and thermal noise. The size of the DAC unit capacitors must be carefully chosen so that it achieves good linearity and the power consumption is moderate.

Due to the fast development of CMOS processes, the minimum channel length of MOS transistors keeps decreasing. This leads to a trend toward reduced power

supply voltage. Thus designing an amplifier with a wide bandwidth becomes more challenging with each new generation of fabrication technology.

For wideband amplifiers, the typical structures used are folded-cascode [33], [17] and telescopic [17], [34]. Folded-cascode amplifiers provide a wide unity gain bandwidth and the input common-mode range is wider than that of a telescopic amplifier. Telescopic amplifiers typically have higher DC gain than folded-cascode amplifiers and the unity gain bandwidth is wider, because telescopic-cascode amplifiers have less source and drain P-N junction capacitance. To achieve the same slew rate, a telescopic amplifier usually consumes less current than a folded-cascode amplifier.

Although telescopic amplifiers have many advantages, they also have a smaller output swing than a folded-cascode amplifier. This is a serious limitation for the design of this $\Delta\Sigma$ modulator, because the power supply is limited to 1.8 volts. For folded-cascode amplifiers, it is possible to achieve $\pm 0.6 V_{P\_P}$ output swing. For telescopic amplifiers, the output swing will be limited to between $\pm 0.3 V_{P\_P}$ and $\pm 0.4 V_{P\_P}$. When the output swing becomes small, KT/C noise, charge injection and clock feedthrough are the limiting factors of a A/D converter. If an A/D is limited by KT/C noise, the realtionship between the sampling capacitor C , the resolution of the A/D converter expressed in bit N and the output swing V_{max} is:

$$C \propto \frac{2^{2N}}{V_{max}^2} \tag{5.1}$$

Thus the capacitance will increase drastically as the output swing is reduced. High swing telescopic amplifiers have been proposed [34], in which the tail current transistors are biased in the deep triode region. But this kind of a high swing telescopic amplifier uses a regulated cascode and replica-tail current feedbacks to compensate the low differential gain and common-mode rejection ratio (CMRR).

This will limit the maximum achievable bandwidth for a given process and at the same time increase the amplifier complexity, since three auxiliary amplifiers are needed for the regulated cascode and replica tail currents. Thus the folded-cascode structures are more suitable for this work.

The structure of the front-end amplifier is shown in Fig. 5.2. It is a conventional folded-cascode amplifier. A PMOS input differential pair is used for better input referred noise. In order to make the amplifier more insensitive to process variations, a standard transistor finger is chosen. Each transistor has an integer number of fingers. The W/L of each finger is $5.2\mu m/0.34\mu m$. This is based on the consideration of gate noise, the gate RC time constant, the transistor matching [35] and process constraints.

The PMOS input differential pair in Fig. 5.2 has 96 fingers each. The $(V_{GS} - V_T)$ for PMOS transistors and NMOS transistors are 0.23 V and 0.205 V, respectively. The transconductance of the input PMOS transistor is $2.33 \times 10^{-2} S$. The corresponding thermal noise power density is $v_{n,1}^2(f) = \frac{8}{3} KT \frac{1}{g_m} = 47.54 \times 10^{-20} V^2/Hz$. For M9 and M3 shown in Fig. 5.2, the corespond thermal noise power densities are $51.58 \times 10^{-20} V^2/Hz$ and $24.63 \times 10^{-20} V^2/Hz$, respectively. The input-referred thermal noise is given by:

$$V_n^2 \approx (V_{n,1}^2(f) + \frac{g_{m9}^2 V_{n,9}^2(f)}{g_{m1}^2} + \frac{g_{m3}^2 V_{n,3}^2(f)}{g_{m1}^2}) \times 2 \tag{5.2}$$

From (5.2), the input referred noise is $v_n \approx 1.913 nV/\sqrt{(Hz)}$. The CADENCE Spectre simulation is shown in Fig. 5.3. The simulation result is $2.127 nV/\sqrt{Hz}$, which is very close to hand calculations. For a 2 MHz input signal band, the total thermal noise is approximately $3\mu V$.

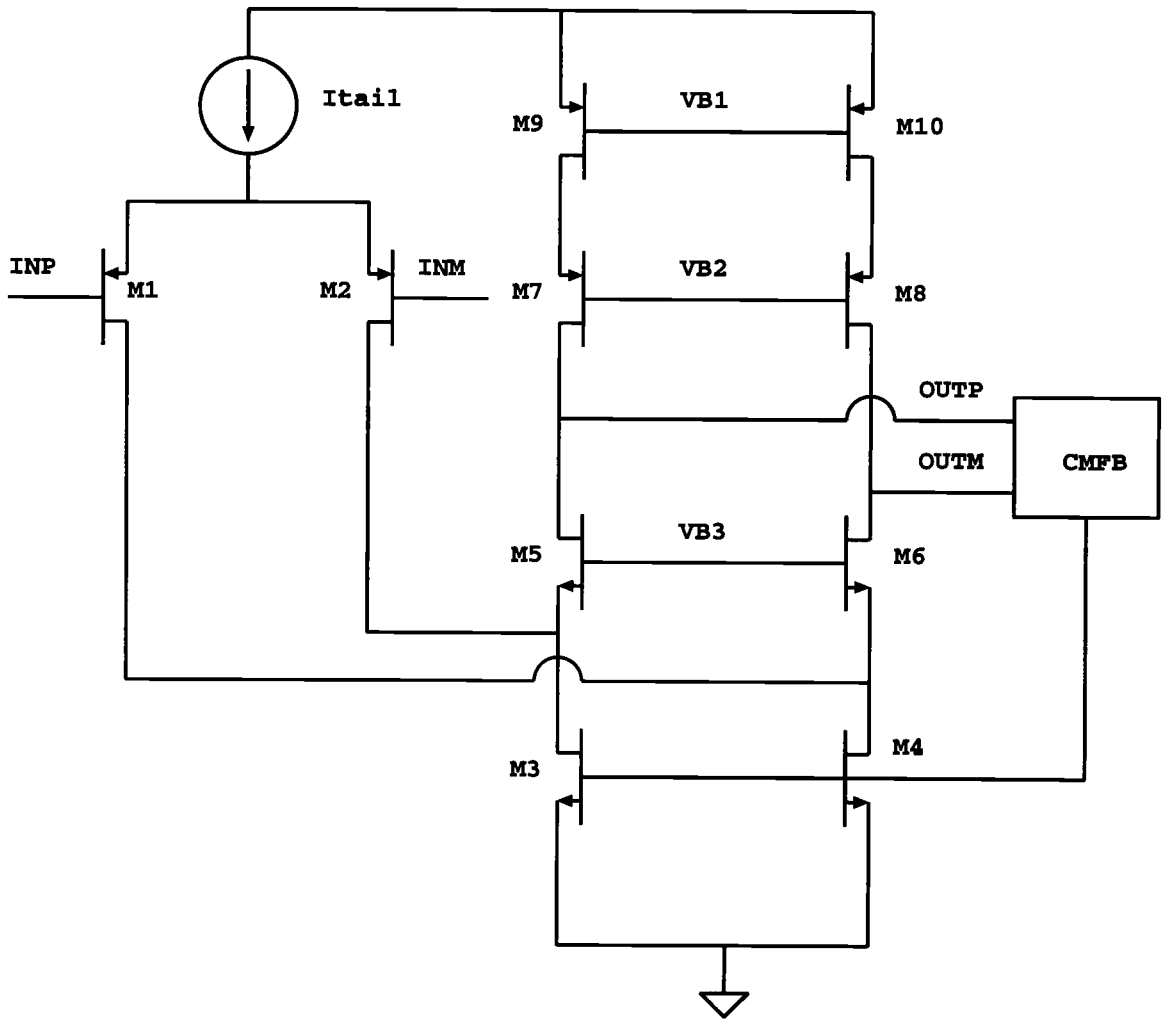


FIGURE 5.2. The front-end folded-cascode amplifier.

Flicker noise parameters are not available in the model files given. However, the flicker noise can be etimated from known processes. For the TSMC 0.35 μm process, the flicker noise corner frequency is about 2 MHz for a small transistor. If this 0.18 μm process has the same corner frequency, the rms flicker noise greater than 10 Hz is 1.34 μV. Actually, the flicker noise corner frequency is probably

much lower than 2 MHz, because the input transistors are very large. The $\Delta\Sigma$ modulator has an LSB amplitude of about 23 μV. The input-referred flicker noise is much less than one LSB. Even if the actual flicker noise is higher than 2 MHz, the $\Delta\Sigma$ modulator is not likely to be limited by the input referred flicker noise of the front-end opamp.

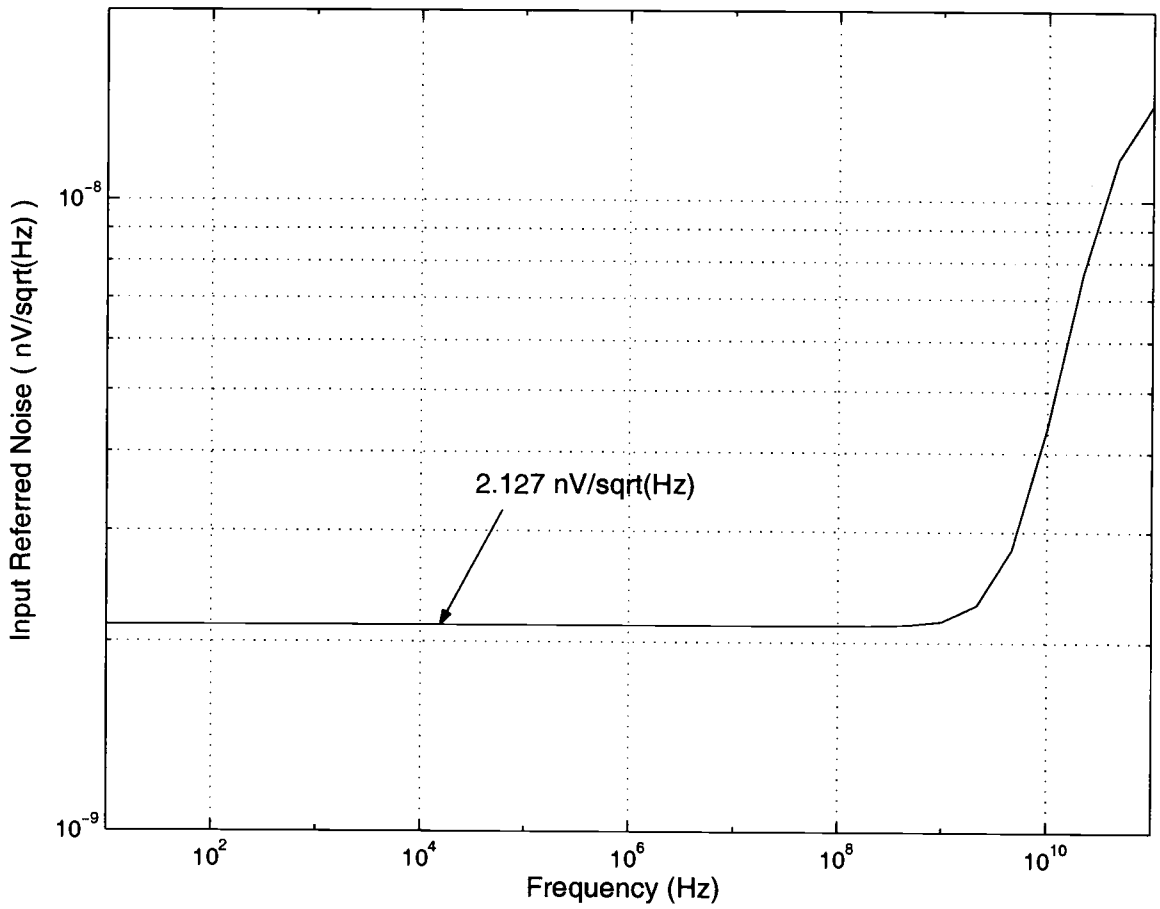


FIGURE 5.3. Input-referred noise of the main Opamp.

The DC gain is shown in Fig. 5.4 as a function of the output swing. When the differential output swing is $\pm 0.5 V_{P-P}$, the DC gain is greater than 110. The

reference voltage of the $\Delta\Sigma$ A/D converter is chosen to be 0.5 V. The histograms of the outputs are almost always within $\pm 0.4 V_{P-P}$. Thus an average gain of 140 is reasonable for this modulator. The DC gain is also a function of the output voltage. The gain non-linearity is included in the C program in Chapter 4. The simulation results of the C program show that low DC gain and gain non-linearity of the opamps do not have noticeable influence on the $\Delta\Sigma$ modulator.

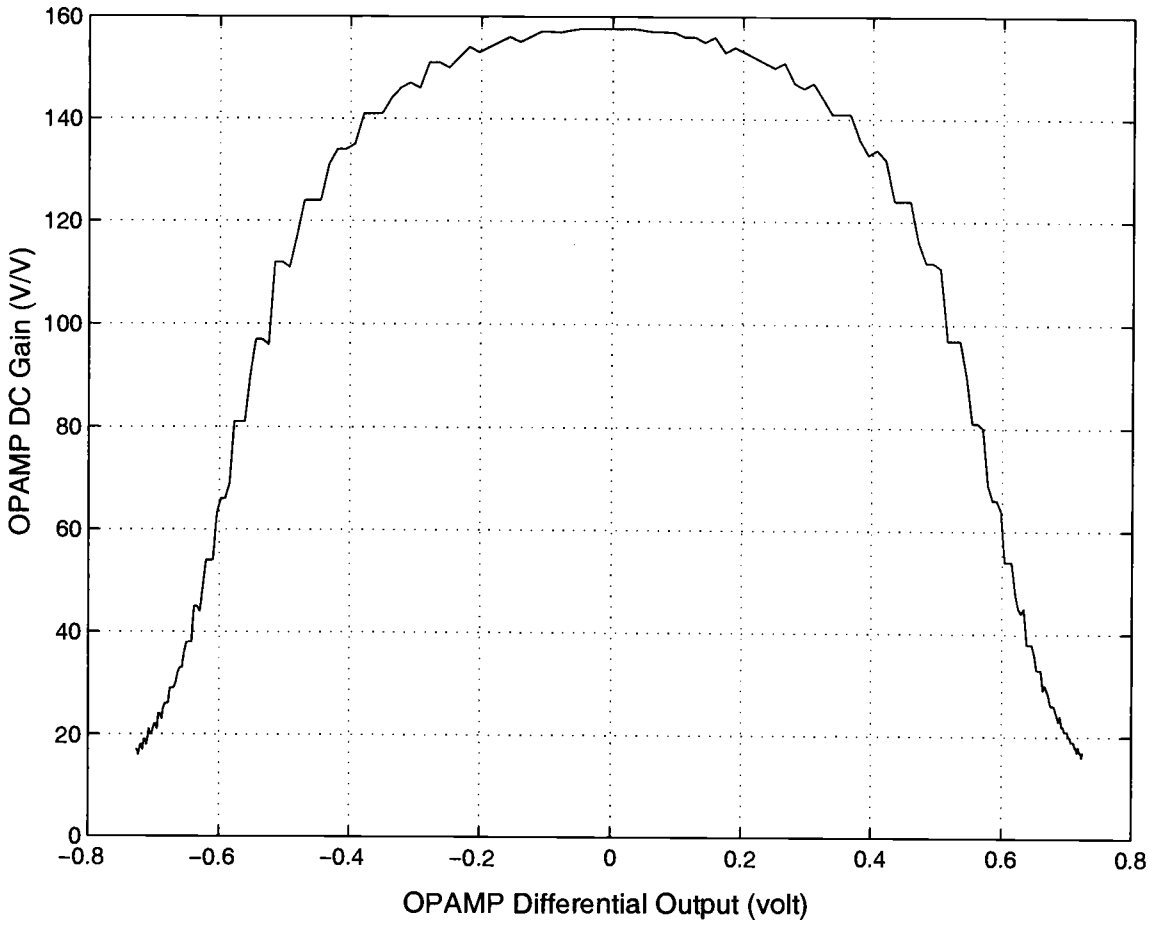


FIGURE 5.4. The front-end opamp DC gain as a function of the differential output.

Since the modulator is clocked at 32 MHz, charge injection and clock feedthrough have a significant effect on the output. Switched capacitor type common-mode feedback circuits inject charge to the biased nodes, when the switches are turned off. As a result, there are small common-mode voltage variations at the biased nodes. These common-mode voltage variations can translate into a differential error voltage at the output. For low clock frequencies, this is not a serious problem. But for high clock frequencies, it can cause more than 1 LSB differential error voltage at the output. For example, the common-mode voltage shift due to charge injection and clock feedthrough is about 10 mV with a 32 MHz clock. This results in about 80 μV differential error at the output, which is about 3.5 LSBs. Thus, a continuous-time common-mode feedback circuit is used for this opamp. Simulation shows that the continuous-time common-mode feedback is better than the switched capacitor common-mode feedback with 32 MHz clock.

In order to guarantee that the common-mode feedback circuit always works with a 1.8 V supply, both NMOS differential pairs and PMOS differential pairs are used as input transistors. The common-mode feedback circuit is shown in Fig. 5.5. M15-M18 are part of the cascode circuit of the main opamp. If OUTP is very high and OUTM is very low, M2, M4, M6, M8 will be turned off. But M1, M3, M5, M7 are still in saturation and the common-mode feedback loop still has high gain to stabilize the main opamp. The common-mode feedback amplifier (CMA) is a two-stage amplifier. From the input of the CMA to node A is the first gain stage. From node A to the outputs of the main opamp is the second gain stage. The two capacitors labeled C_C in Fig. 5.5 are the Miller compensation capacitors and each capacitor is 1.8 pF. The compensation capacitors also help to stabilize the main opamp, when the main opamp has very small capacitive load during some clock phases. The CMA has 258 MHz unity gain bandwidth with 63.5 degrees of phase

margin. The loop gain of the common-mode feedback is 75.8 dB. Another advantage of this CMA is that, since M11 and M14 are biased in class-AB mode, smaller sizes for M11 and M14 can be used to drive the two big transistors M15 and M16. This helps to reduce the power consumption of the CMA.

The whole opamp has very good frequency response. With an 8 pF load (excluding the compensation capacitors shown in Fig. 5.5), the unity gain bandwidth is 281 MHz with a phase margin of 85.3 degree, the DC gain is 43 dB and the slew rate is $640V/\mu s$. Table 5.1 is the summary of the specifications of the front-end opamp.

TABLE 5.1. Specifications of the front-end opamp with a capacitive load of 8 pF.

Specs	Minimum	Typical	Fast
DC Gain (dB)	42.67	43.53	44.44
Slew Rate (V/us)	577	638	684
UGB (MHz)	259	281	311
PM (degree)	85.0	85.3	85.5
Input Referred Themal Noise (nV/sqrt(Hz))	2.003	2.127	2.234
Power Dissipation (mW)	28.3	32	34.7

The integrator is shown in Fig. 5.6. The DAC is implemented with sixteen 0.45 pF capacitors. According to Pelgrom [36], the variance of parameter ΔP of a pair of devices with an area of $W \times L$ is:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \tag{5.3}$$

where A_P and S_P are two process-dependent coefficients and D_x is the distance between the two devices. This equation tells us the mismatch variance is inversely proportional to the device size. In order to achieve good linearity, the

DAC capacitor cannot be too small. A 0.45pF poly-poly capacitor for this process is about 560 μm^2. Capacitors of this size are expected to achieve 0.1% mismatch. Another matching factor from (5.3) is the distance between two devices. By using common centriod layout techniques and putting these capacitors close to each other, this mismatch can be greatly reduced.

It is shown in Fig. 5.6 that eight capacitors out of sixteen are used to sample the input signal. This provides -6 dB attenuation to the input signal and the maximum stable input is -2.85 dB. The switches connected to ground or virtual ground are NMOS switches and they are $1.2\mu m/0.18\mu m$. The switches connected to other nodes are CMOS switches where the sizes are $5.2\mu m/0.18\mu m$ for the NMOS transistors and 15.6um/0.18um for the PMOS transistors. The typical charge injection is about 2.5 μV. Simulation shows that this integrator can settle to 14 bits in about 11ns for the worst case. Conventional two phase non-overlapping clocks are used. The integrator samples the input during $\phi 1$ and transfers the charge to the integrating capacitors during $\phi 2$. During $\phi 2$, the sixteen capacitors are chosen by the DAC output to connect either to vref+ or vref-. The layout of the integrator is shown in Fig. 5.7.

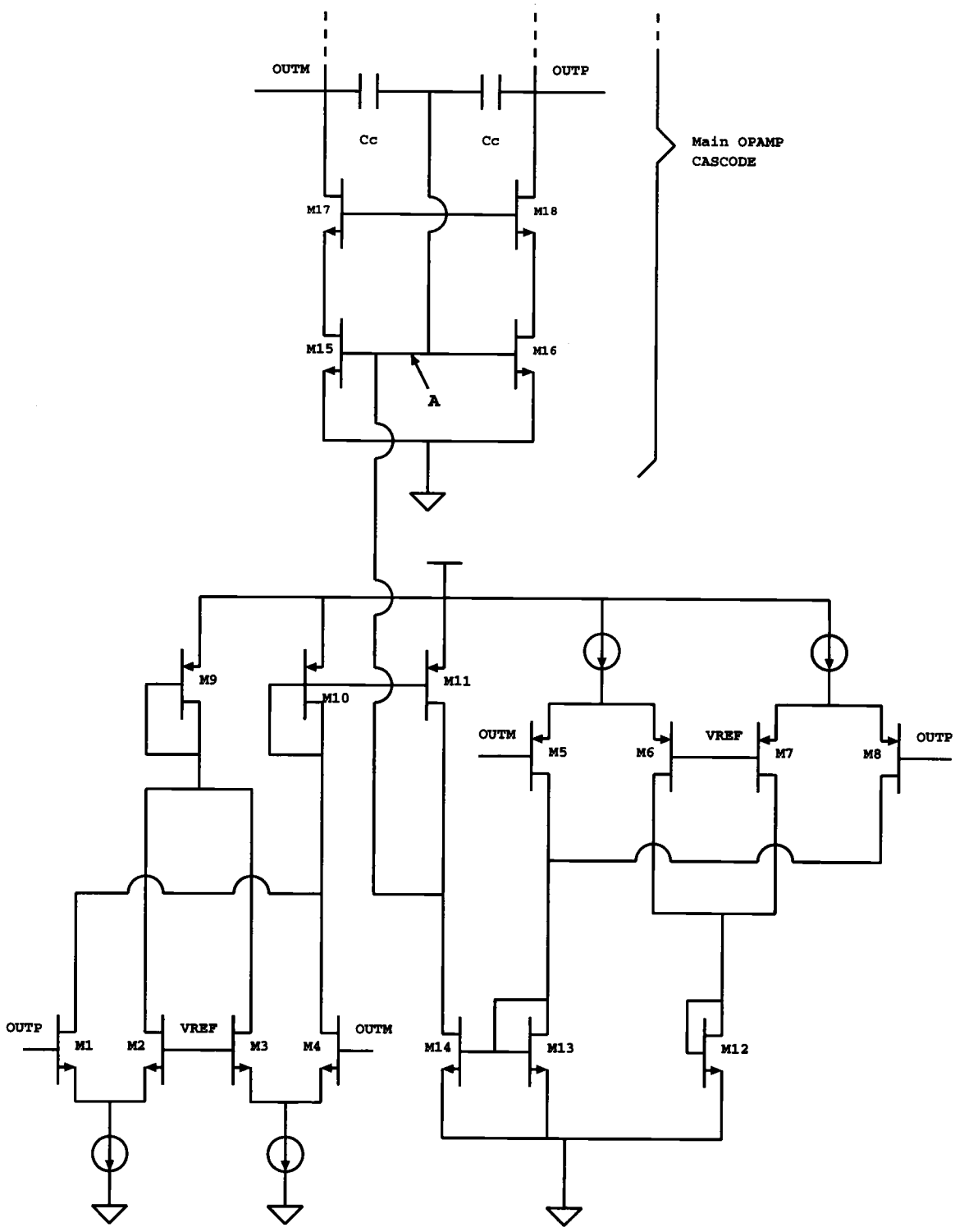


FIGURE 5.5. Common-mode feedback circuit used in the front-end Opamp.

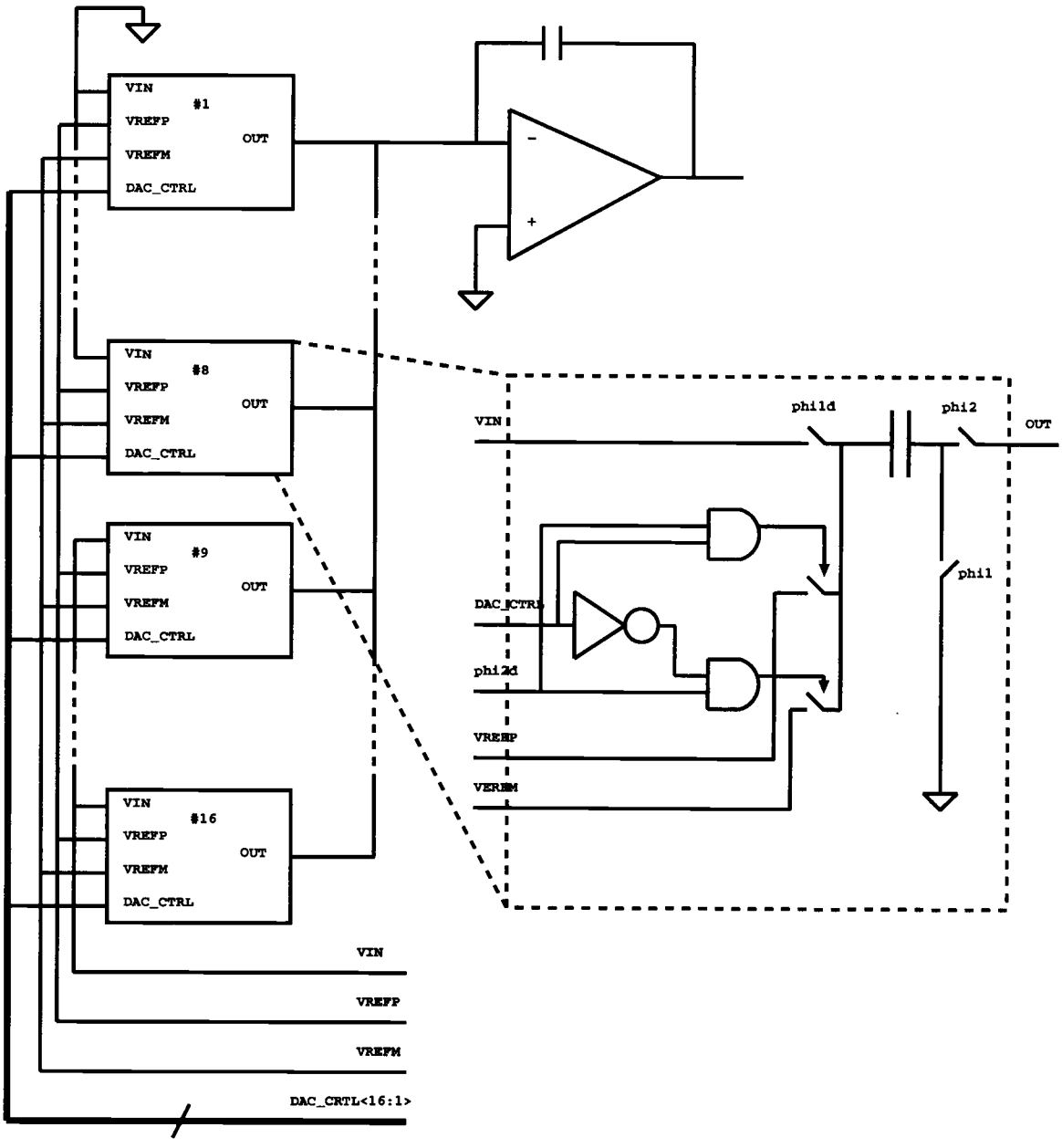


FIGURE 5.6. Block diagram of the front-end integrator.

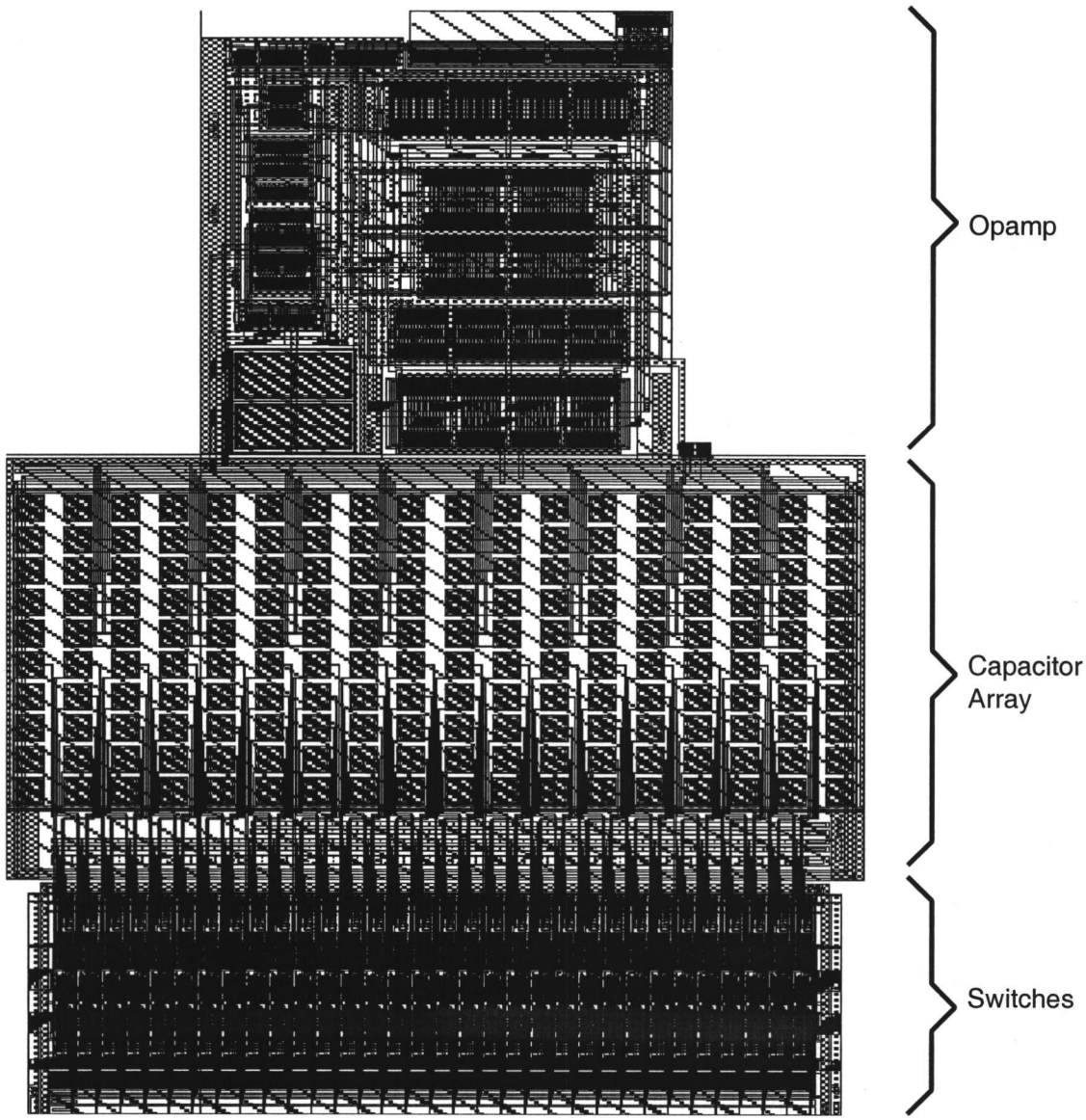


FIGURE 5.7. Layout of the front-end integrator.

5.3. Design of the Second-Order Transposed Direct Form II Blocks

The second-order transposed direct form II block shown in Fig. 4.4 has two delay blocks. It is not a problem to implement a delay block in the digital domain. But in the analog domain, it is difficult to implement a delay block close to an ideal delay, because there is always some leakage introduced by the finite DC gain of the opamps. Switched capacitor settling error must also be considered. The non-idealities mentioned above will be attenuated by the loop gain. Thus the effect of a non-ideal delay block on a $\Delta\Sigma$ modulator is much less than that of the error feedback structure, in which delay blocks are in the feedback path instead of in the forward path.

One way to implement the delay is shown in Fig. 5.8. It is an integrator with an extra switched capacitor, C_3 , which is used to sample the previous output and cancel the previous output during $\phi 2$. Assume the DC gain of the amplifier is A and there is no settling error. The transfer function of the delay block is:

$$H(Z) = \frac{C_1 Z^{-1}}{C_2}\left[\frac{1}{(1+\frac{C_1+C_2+C_P}{AC_2})-(\frac{C_2+C_P}{AC_2})Z^{-1}}\right] \tag{5.4}$$

The non-ideal delay block has a pole very close to the origin at:

$$P(Z) \approx (\frac{C_2+C_P}{AC_2}) \tag{5.5}$$

When the DAC feedback is formed, this pole in the forward path will become a zero very close to the origin in the noise transfer function. A zero close to the origin does not change the noise transfer function much. At the same time, the pole in (5.5) slightly changes the poles of both the noise transfer function and the signal transfer function. These effects have been taken into account in the C program mentioned in Chapter 4. The simulation results in Chapter 4 show that the delay block shown in Fig. 5.8 is a suitable implementation for this work.

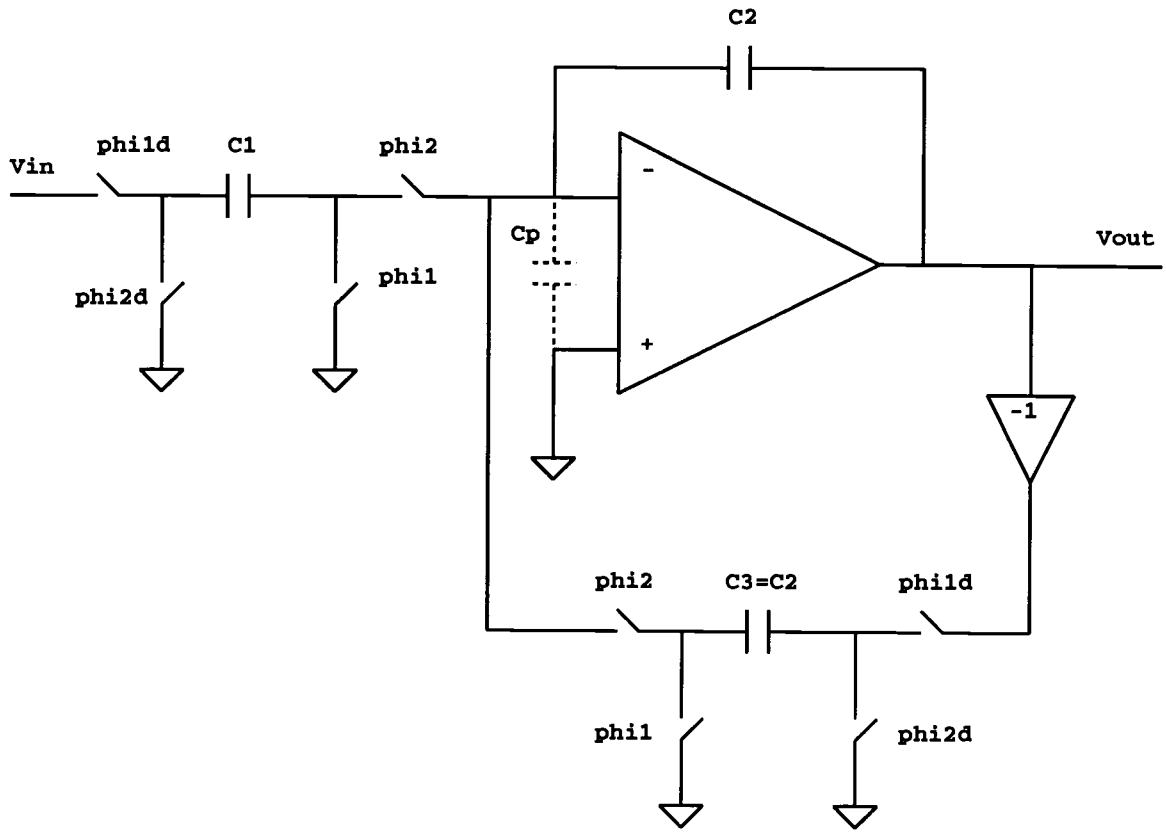


FIGURE 5.8. Analog implementation of one clock period delay.

Since the front-end integrator has high DC gain, the noise and distortion of the following blocks are greatly attenuated. This allows aggressively scaling the transistor sizes of the following stages. All other opamps are scaled down to 25% the size of the front-end opamp. The typical power consumption of this opamp is 8 mW. Thus the total power consumption can be greatly reduced.

One way to reduce the area and to increase the speed is to reduce the redundant capacitors. The delay block shown in Fig. 5.8 has a feedback switched capacitor C_3 with a coefficient of -1. The second-order transposed direct form II block shown in Fig. 4.4 has a feedback a_1. Table 4.1 shows that a_1 is 1.875 and 1.955 for the two

second-order transposed direct form II block shown in Fig. 4.10. Thus coefficients a_1 and -1 can be reduced to a single coefficient $(a_1 - 1)$. In this chip, signals are sampled during $\phi 1$ and charge is transferred to the integrator capacitors during $\phi 2$. If we ignore switch resistance, the switched-capacitor integrator during $\phi 2$ can be simplified as in Fig. 5.9. C_S is the sampling capacitor, C_P is the opamp parasitic input capacitance, C_F is the integrating capacitor and C_L is the capacitive load. The capacitors corresponding to coefficients a_1 and -1 are part of the capacitor C_S during $\phi 2$ and the closed-loop unity-gain bandwidth at this point in time is [37]:

$$\omega_{CL} \approx \frac{g_m}{[C_S + C_P + \frac{C_L(C_F + C_S + C_P)}{C_F}]} \tag{5.6}$$

where ω_{CL} is the closed-loop unity gain bandwidth of the opamp and g_m is the transconductance of the opamp. By merging the two coefficients a_1 and -1 into one coefficient, the capacitor C_S is reduced by 30-40%. Thus the feedback factor β is increased by 40-60% and the closed loop bandwidth can be increased by 60.8% and 44.2% for the first and second blocks, respectively.

5.4. Design of the Summing-Amplifying Block

As shown in Fig. 4.10, the summing-amplifying block is used to sum three input signals, amplify it by a factor of about 3 and feed it to the input of the 4-bit A/D converter. This block is a zero delay switched-capacitor circuit. There are two possible approaches for this block as shown in Fig. 5.10. In the single stage approach shown in Fig. 5.10(a), the summing and amplifying are implemented with one opamp. The feedback factor β is approximately 0.08 and the closed-loop bandwidth is too small for this application. If the function is implemented in a two stage configuration shown in Fig. 5.10(b), the feedback factors for the first and the

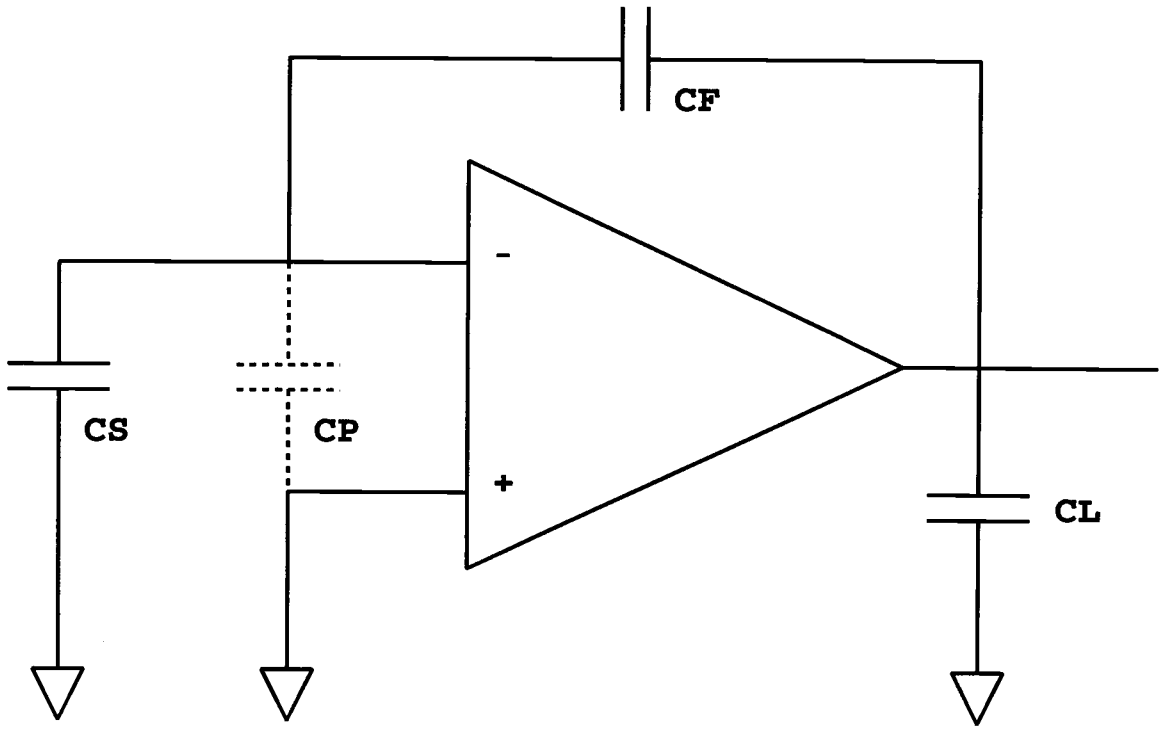


FIGURE 5.9. A simplified schematic of the switched-capacitor integrator during $\phi 2$.

second opamps are 0.20 and 0.192, respectively. The total time constant of the two stage approach is about 82% of the time constant of the single stage approach. Thus the two stage approach can achieve higher closed-loop bandwidth than the single stage approach and it is used in this design as the summing-amplifying block.

The DC gain of the opamps used in this A/D is about 43 dB. Low DC gain opamps can make integrators leaky and the poles and zeros of the NTF and STF will drift away from their ideal locations. From Chapter 4, it is known that this hybrid $\Delta\Sigma$ modulator has very low sensitivity to coefficient variations. However, special attention should be paid to the summing-amplifying block. Since this block

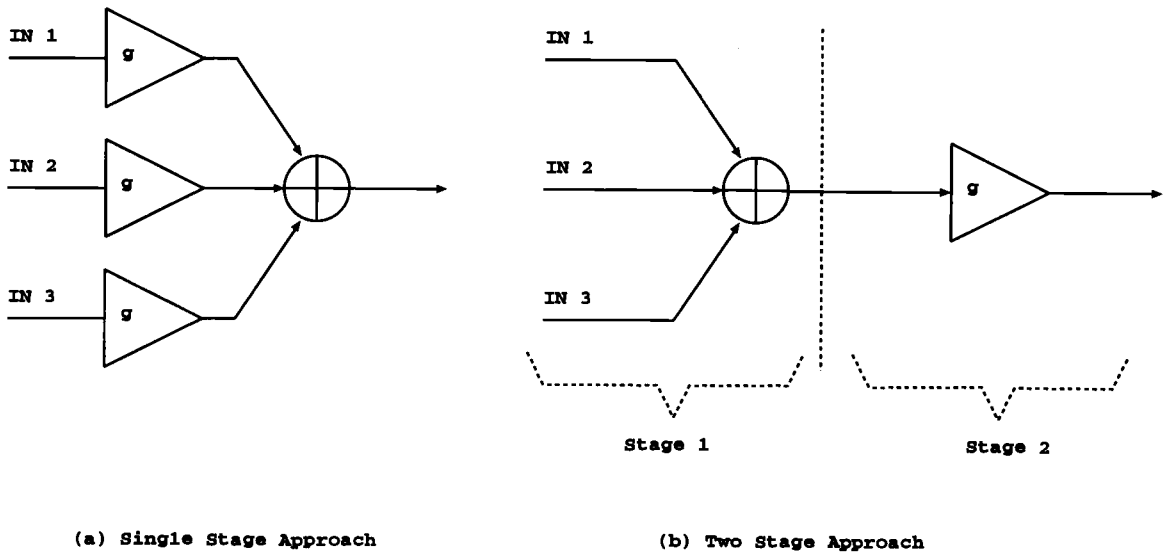


FIGURE 5.10. Two approaches to the summing-amplifying block.

sums three input signals, the non-idealities can affect all preceding blocks. Let us consider the two stage approach shown in Fig. 5.10(b). If the feedback factor is small and the opamp DC gain is also low, the closed-loop gain will be small. For opamps with 43 dB DC gain, the first stage in Fig. 5.10(b) has a loop gain of only 25.3 which reduces the gain by about 3.95%. The second stage has a loop gain of 25.97 and this reduces the gain by 3.85%. The resulting total gain error is about 7.8%. If the gain g is set to the nominal value of 3.2, the effective g is only 2.95. The NTF poles will move far from the ideal positions and this will degrade the SNDR of the modulator. To compensate the gain error, a higher value of g is needed. Since the coefficient g has very low sensitivity to pole/zero positions as shown in Table 4.2, g can be quantized aggressively to an easy-to-implement value without significant influence on the final performance. To simplify the layout implementation, $g = 3.5$ is used compared with the ideal value of 3.47. Figure 5.11 show the results with

and without the coefficient compensation. If g is set to 3.2, the noise shaping is distorted and the SNDR is only 80 dB. If g is increased to 3.5, the noise shaping is very smooth and the SNDR is 83.41 dB.

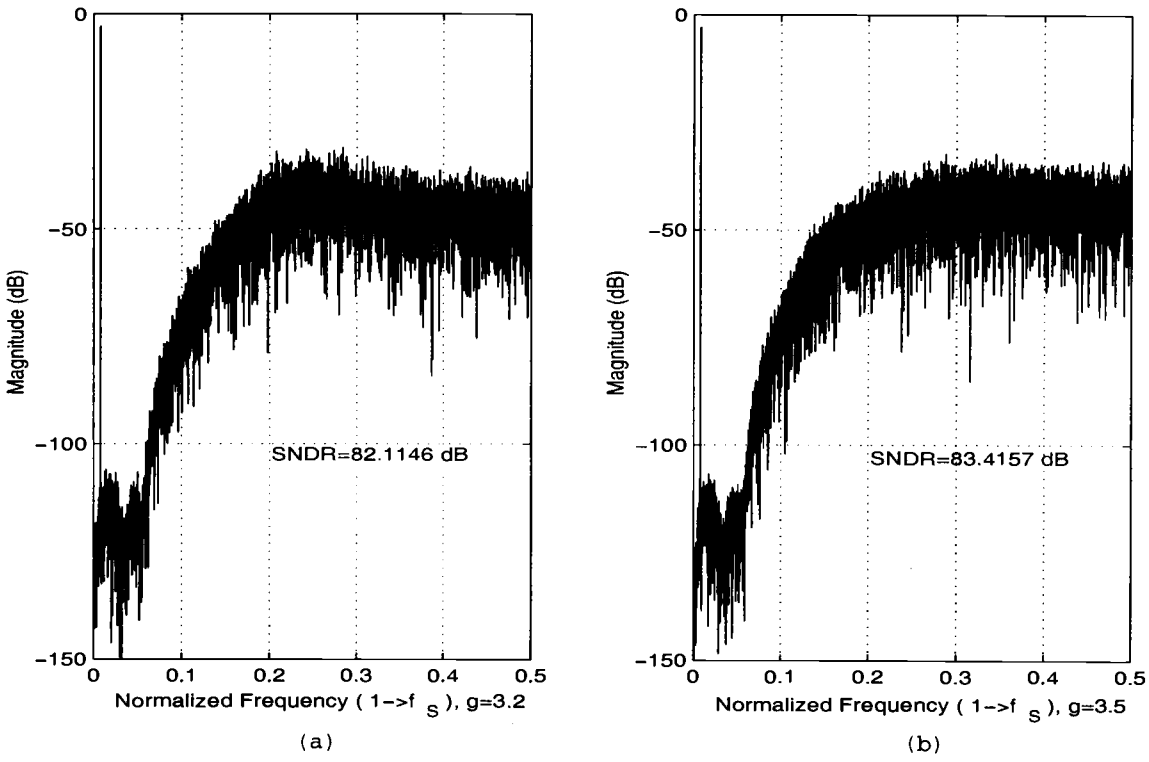


FIGURE 5.11. Comparison of coefficient compensation effect on the hybrid $\Delta\Sigma$ modulator, (a) no coefficient compensation (g=3.2), (b) with coefficient compensation (g=3.5).

5.5. Design of the 17-Level 4-Bit Flash A/D

For a fifth-order $\Delta\Sigma$ modulator, the quantizer input is subjected to fifth-order noise shaping. Thus designing a multi-bit quantizer for a $\Delta\Sigma$ modulator is

much easier than that for a Nyquist-rate A/D converter. The offset voltages of the comparators are not important, since they are DC signals.

The effect of comparator hysteresis on the $\Delta\Sigma$ modulator is difficult to estimate by hand. Comparator hysteresis is simulated by a C program. Figure 5.12 shows the error bar of the modulator SNDR as a function of comparator hysteresis. The comparator hysteresis has a negligible effect on the $\Delta\Sigma$ modulator. The standard deviation of the SNDR is about 0.5 dB, which is very close to the standard deviation of the SNDR shown in Fig. 4.18. Figure 4.18 shows a standard deviation of 0.45 dB without taking comparator hysteresis into account. When the hysteresis is as high as 13mV, the SNDR drops only about 0.4 dB. A properly designed comparator will have hysteresis much less than 13mV. Hysteresis influence can be further reduced by using democratic logic to reduce thermometer code bubbles caused by comparator hysteresis.

The comparator core is shown in Fig. 5.13. It has a biasing circuit, a preamplifier, a master latch and a slave latch. The preamplifier is a single stage class-A amplifier. This simple structure has only one pole. Thus it is absolutely stable and very fast when the output and input of the preamplifier are shorted for offset cancellation. This preamplifier has a gain of 8 to 15. Thus the offset voltage of the master latch will be attenuated by 20 dB. This is good enough for this $\Delta\Sigma$ modulator because of the fifth-order noise shaping. The master latch has a typical structure. The slave latch is formed by digital gates. When the comparator is in the offset cancellation phase, the master latch output will be reset. But the slave latch output will not be changed. All transistors have $0.18\mu m$ channel length. At 32 MHz clock rate, the comparator core consumes 0.72mW.

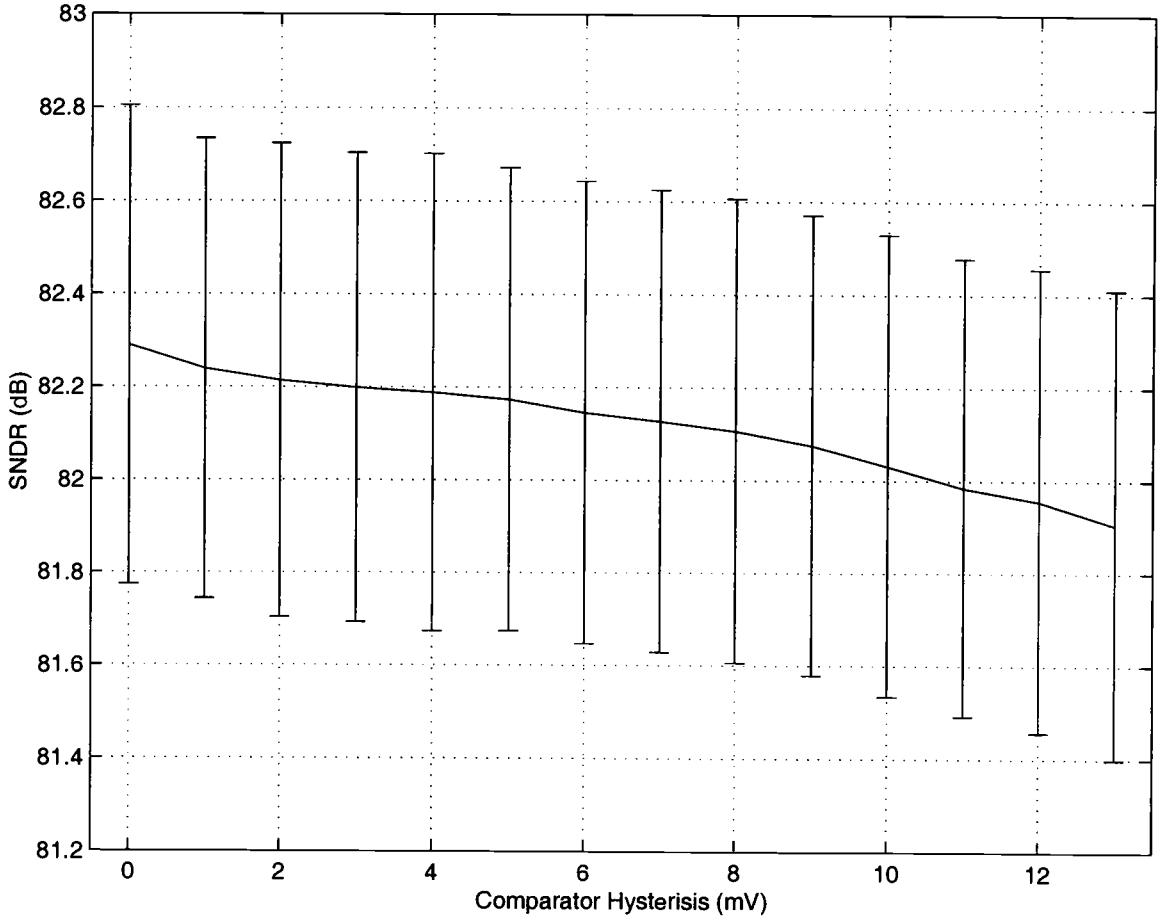


FIGURE 5.12. Error bar of the SNDR of the $\Delta\Sigma$ modulator as a function of comparator hysteresis.

Since the power supply is only 1.8 V, the comparator core has very limited common-mode input range. The input signal cannot be directly connected to the input of the comparator core. Thus a switched-capacitor circuit is needed to compare the opamp output with the reference voltage. The schematic of the comparator is shown in Fig. 5.14. Two switches S_5 and S_6 are used to prevent the comparator core input from being affected by the switch noise of S_1, S_2, S_3 and S_4. S_5, S_6 are

turned off when $S1$ and $S4$ are turned off or S_2, S_3 are turned on. Thus switch noise will not dump charge on the offset cancellation capacitors.

Sixteen comparators are used to build the 4-bit 17-level A/D. A poly resistor ladder is used to generate the reference voltages. The total resistance is 640 Ω. The voltage across the resistor ladder is 0.5 volt. Each comparator has two 50 fF capacitors for offset compensation. The layout of a comparator cell is shown in Fig. 5.15.

5.6. Design of the Clock Generator

The switched capacitor circuits use conventional two phase non-overlapping clocks. Due to the clock timing of the 4-bit A/D, the clock generator is somewhat complicated. Figure 5.16 shows the schematic of the clock generator. The output signal *offset_ca* is used to drive the input *reset* of the comparator shown in Fig. 5.14. Outputs *g1, g2* are used to drive the summing-amplifying block. Outputs *phi1, phi1d, phi2, phi2d* are non-overlapping clock signals that are used to drive the front-end integrator and the two transposed direct form II blocks. The signal *reset_switches* is used to discharge all integrating capacitors during power up. The corresponding clock diagram is shown in Fig. 5.17.

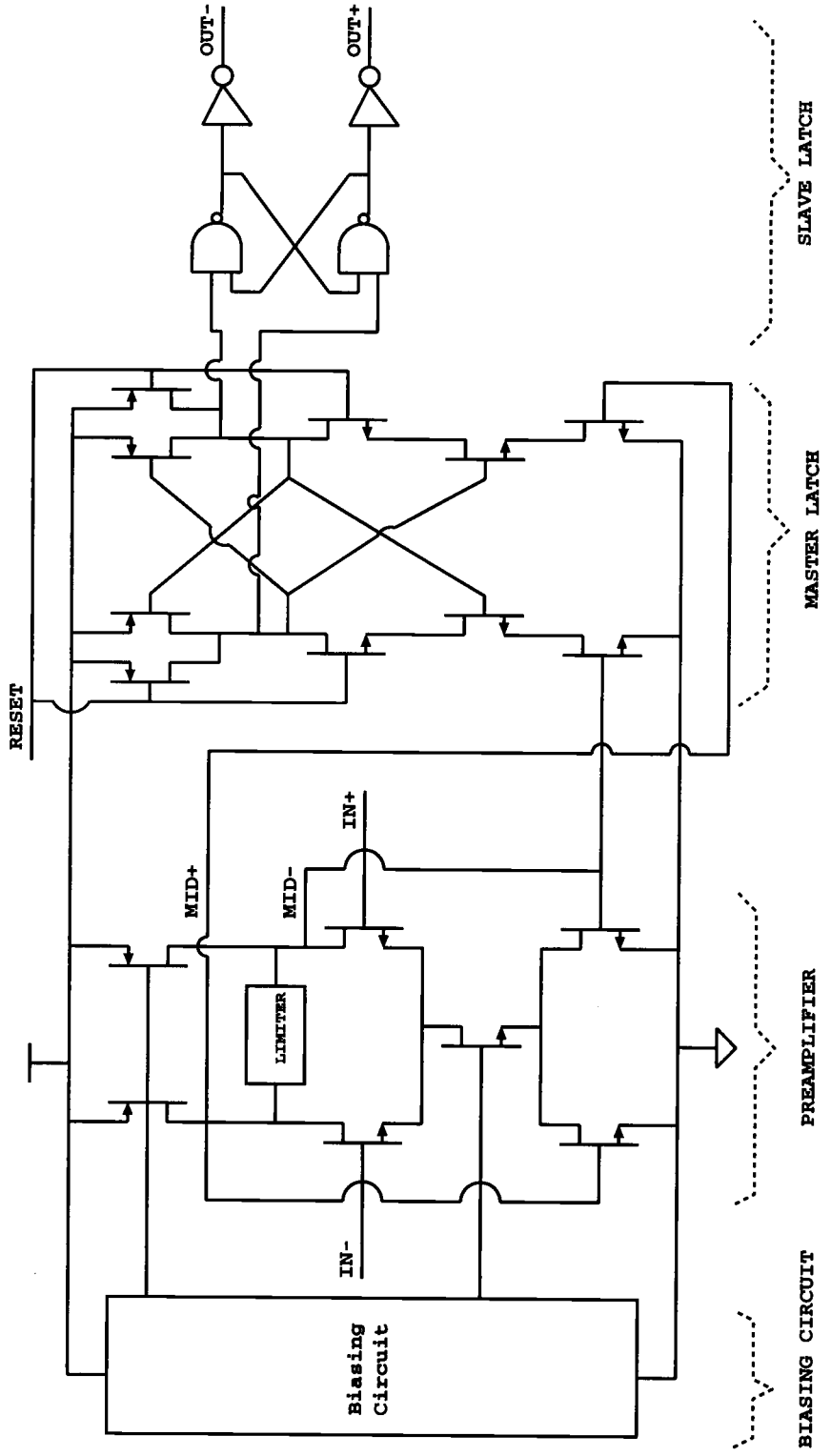


FIGURE 5.13. Comparator core of the 4-bit A/D used in the $\Delta\Sigma$ modulator.

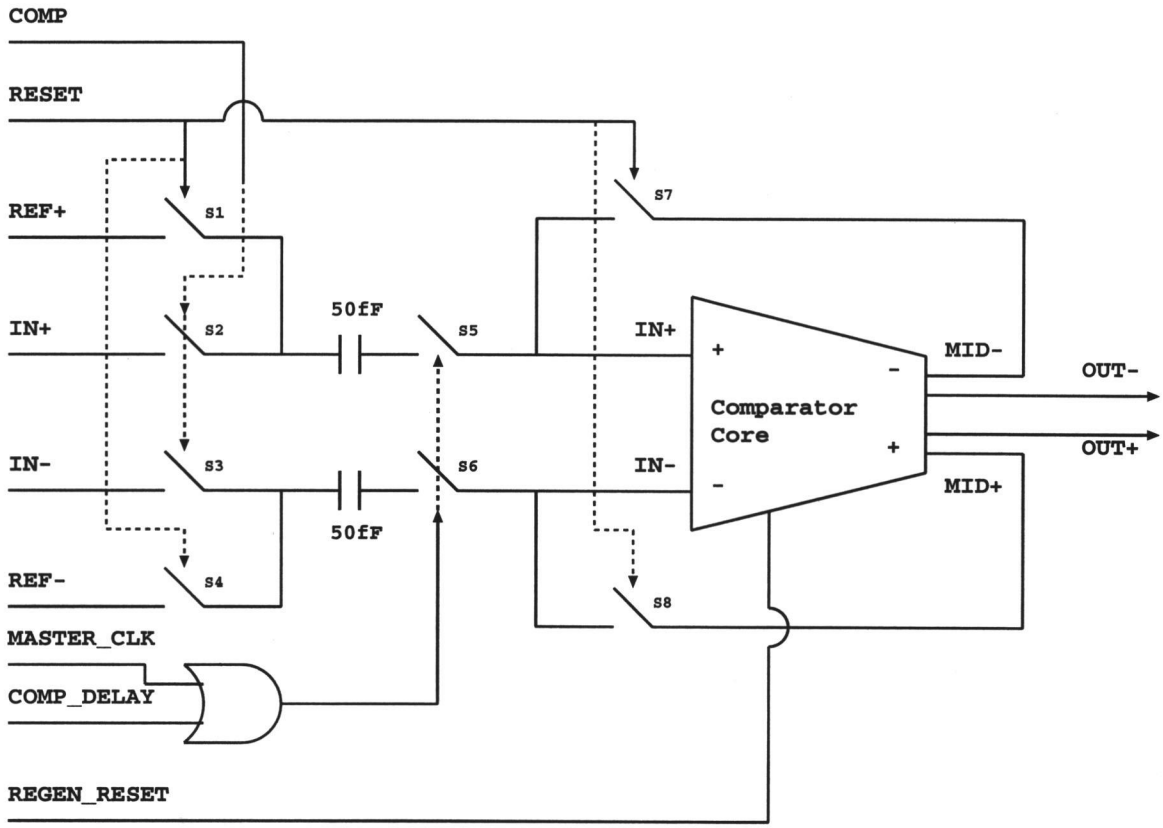


FIGURE 5.14. Schematic of the comparator cell.

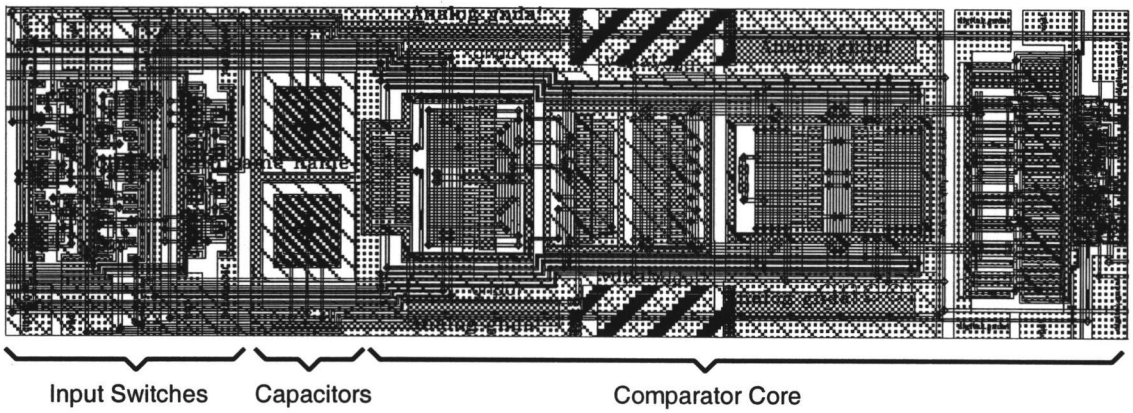


FIGURE 5.15. Layout of the comparator cell.

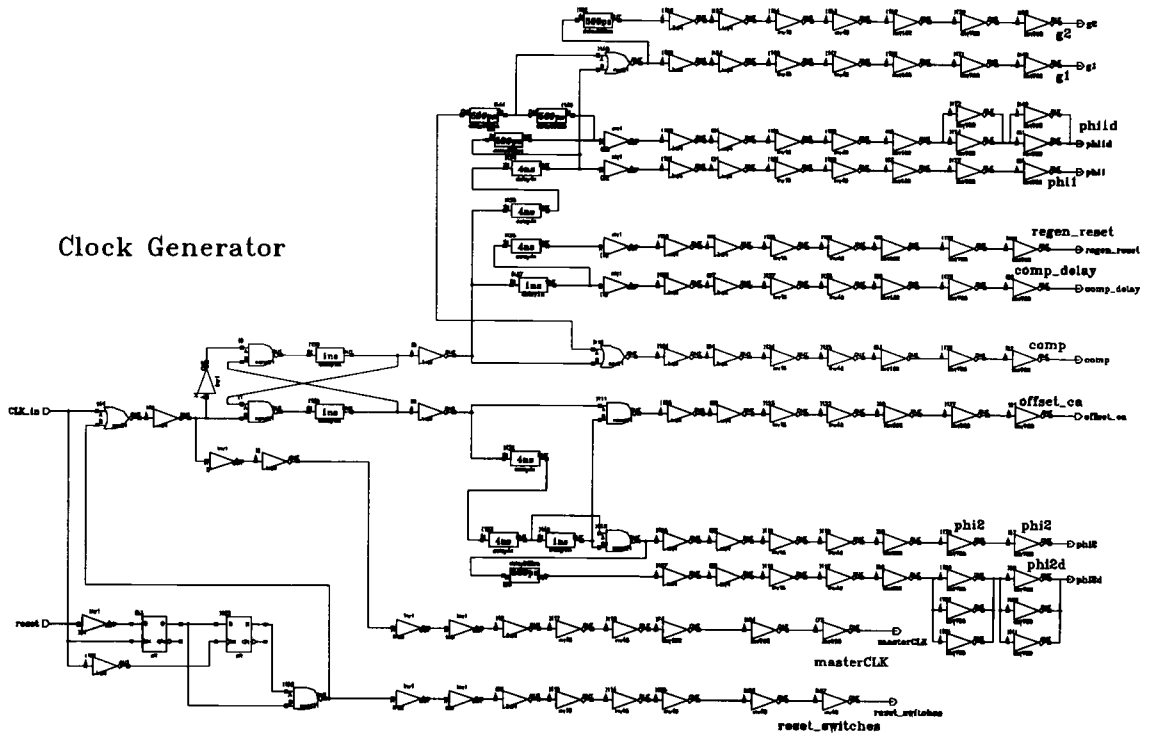


FIGURE 5.16. Schematic of the clock generator.

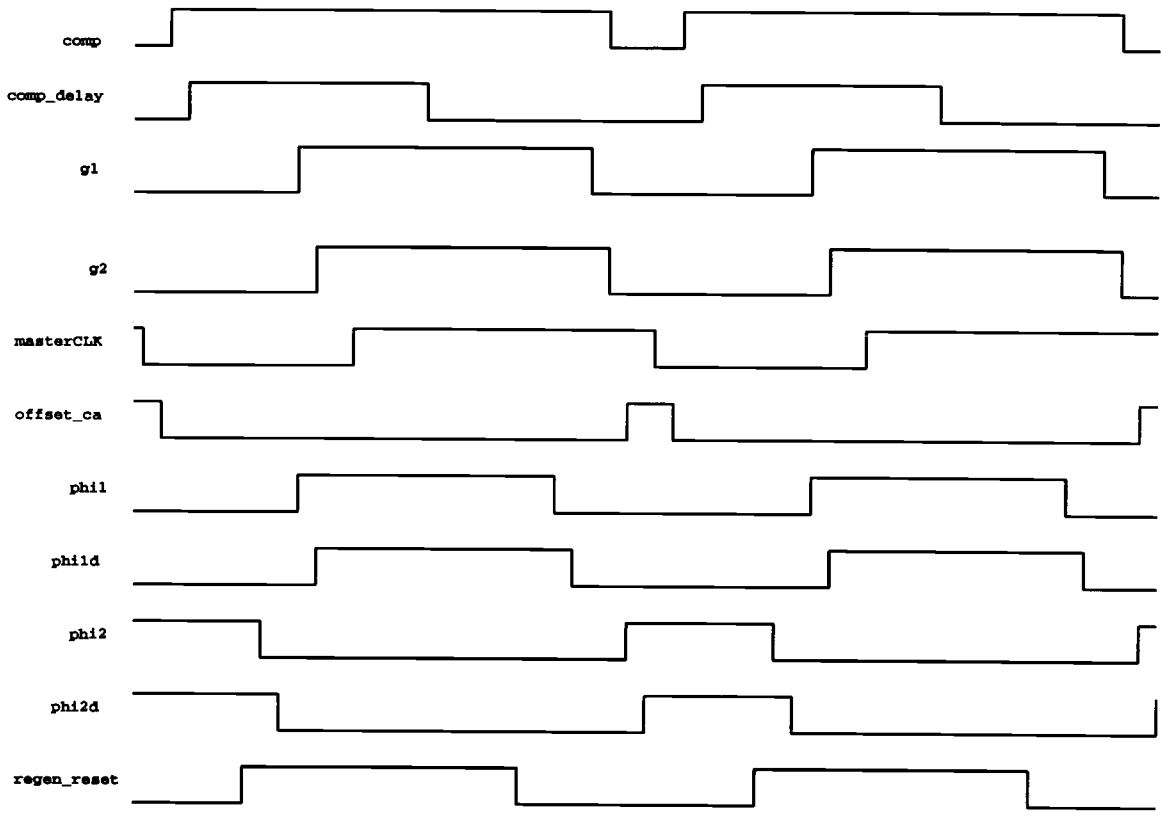


FIGURE 5.17. Timing diagram of the clock generator.

5.7. Logic Design of the Data Weighted Averaging Algorithm

The data weighted averaging algorithm is implemented in this $\Delta\Sigma$ A/D. The block diagram of the DWA algorithm is shown in Fig. 5.18. The 16-bit logarithmic shifter and the accumulator are the key blocks in the diagram. Democratic logic is used to reduce bubbles in the thermometer code. However, there may be some bubbles that the democratic logic cannot eliminate (the possibility is very small). If the thermometer code at the democratic logic output is directly converted to a binary code, a very large error can occur when the democratic logic cannot eliminate all bubbles. The large error can easily make the fifth-order $\Delta\Sigma$ modulator unstable. This problem can be greatly reduced by converting the thermometer code to gray code first and then converting the gray code to a binary code.

A 16-bit logarithmic shifter is used instead of using a barrel shifter, because a 16-bit barrel shifter has very complicated wiring. The accumulator is 4-bit and when the accumulated value is greater than 15, it will be automatically truncated to 4 bits (MSB is truncated). The binary output of the accumulator is decoded to a thermometer code and the thermometer code is used to control the 16-bit logarithmic shifter. The shifter will circularly shift the 16-bit input exactly the same bits as the total number of 1's in the shift control signal. A comprehensive verilog simulation has been performed to verify the functions of the DWA logic. It shows that the logic design can implement data weighted algorithm under all kinds of circumstances.

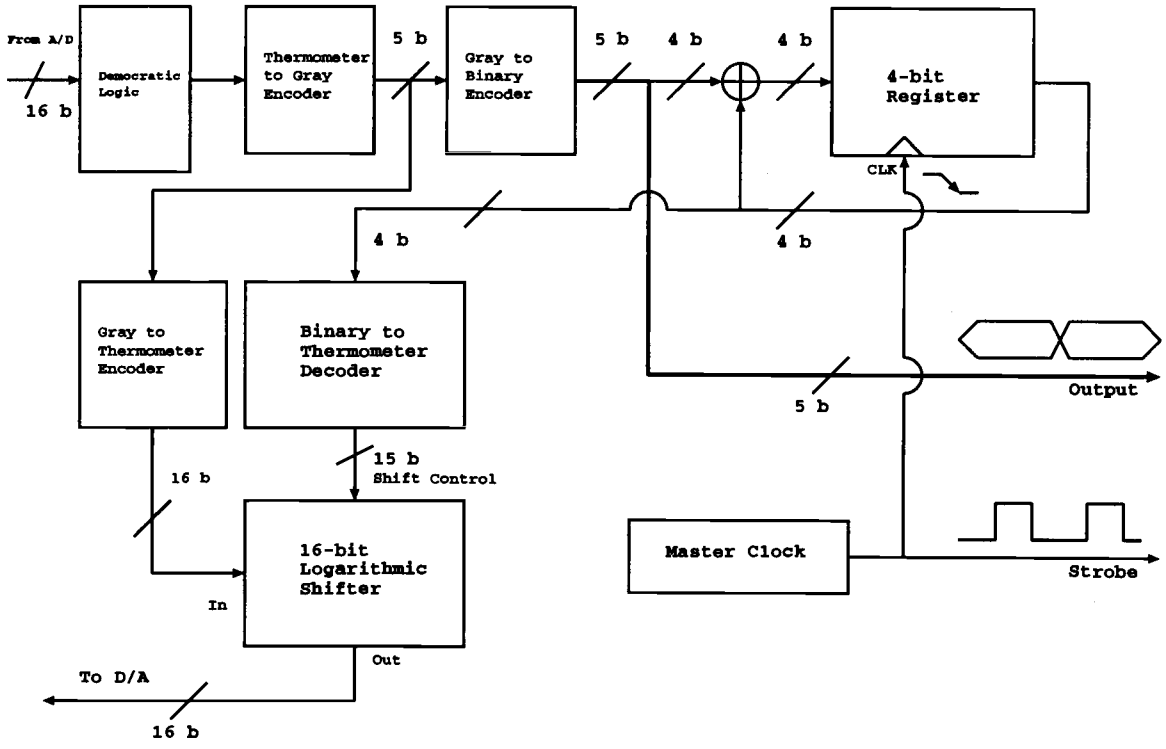


FIGURE 5.18. Block diagram of the data weighted averaging logic.

5.8. Layout Design

For high performance analog mixed-signal circuits, layout is a very important issue. A bad layout can degrade system performance. In order to make a good layout, a floorplan is needed. Fig. 5.19 shows the floorplan of this chip. The front-end opamp is in the upper left corner, where substrate noise will be the smallest. The global biasing circuit is also in this corner. Capacitors are placed between the opamps and the switches so that switch noise can be attenuated before it reaches the opamps. Guard rings and shielding N-WELLs are placed all over the chip to

reduce substrate noise coupling. The 4-bit A/D is between the analog and the digital circuit. The DWA logic and the clock generator are placed at the bottom of the die.

Common centroid layout techniques, dummy transistors, dummy capacitors and dummy resistors are used to improve matching. To avoid cross talk, the delay blocks of the clock generator have seperate power and ground lines. These lines have the same tie points only at the power and the ground pads. This can help to reduce clock jitter. A large number of power and ground pads are used to reduce the supply noise due to current surges. Poly-poly capacitors are used on chip as decoupling capacitors and the total decoupling capacitance is 106 pF. Each decoupling capacitor has a damping resistor to avoid ringing on the power and ground lines. The chip has 52 pins and the total active die area including the power and ground rails is about 2.86 mm^2. The die photo of the $\Delta\Sigma$ A/D is shown in Fig. 5.20.

5.9. Simulation Results

Each block of the fifth-order $\Delta\Sigma$ modulator has been simulated with Spectre. Simulation shows that the front-end integrator and the two second-order transposed direct form II blocks can settle to within 14 bits in 12 ns under the worst case. The summing-amplifying block is a cascade of two zero delay switched capacitor gain blocks. The total time constant is the sum of the two blocks. Under the worst case, it can settle to 10 bits. It can settle to 12 bits and 14 bits for the typical case and the fast case, respectively. Although the settling error is likely to be greater than 14 bits, the summing-amplifying block is subjected to fifth-order noise shaping. If the noise shaping effect is taken into account and the settling is assumed to be linear,

the 10 bit settling error will not have noticeable effect on the SNDR. This is verified by the C program. Linear settling is a reasonable assumption, because the opamps have about 85 degree phase margin. Thus the settling is close to exponential and linearity is very good. Whole chip simulation including the digital part and the pad frame has been done with Spectre. The simulation of each clock cycle takes 70 minutes. To estimate the spectrum, typically 16K data are needed. Thus the Spectre simulation is too slow to get enough data for estimating the spectrum.

In order to make sure the clock timing is correct and the modulator behaves in the same way as expected, a Switcap2 program has been developed to simulate the whole $\Delta\Sigma$ modulator. The opamp input capacitance is included in the simulation. The Switcap2 code is shown in APPENDIX B. Figure 5.21 shows the simulation results. The simulated SNDR is 83.42 dB, which is very close to the result predicted by the C program. It should be noted that the DAC unit capacitor mismatch is not included due to the great difficulty in implementing the DWA logic with Switcap2. Thus the simulated SNDR is a little higher than the average SNDR shown in Chapter 4. The main purpose of Switcap2 simulation is to verify that the $\Delta\Sigma$ modulator is functionally correct. Thus ignoring DAC unit capacitor mismatch will not undermine the viability of the hybrid $\Delta\Sigma$ modulator structure. Spectre transient analysis and Switcap2 transient analysis of the whole chip have been done and compared. Both transient analyses generate the same results. Thus this $\Delta\Sigma$ A/D converter is verified.

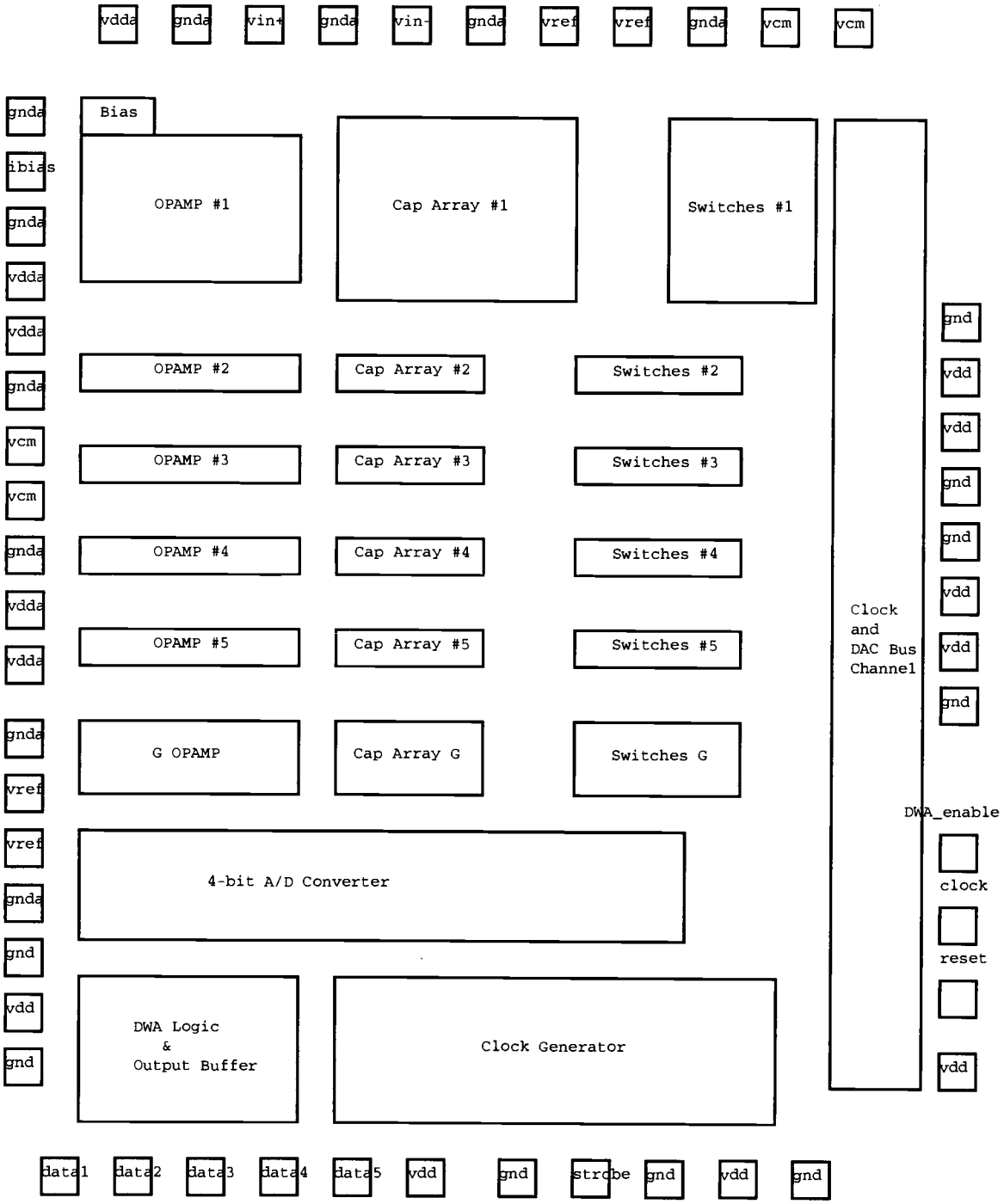


FIGURE 5.19. Floorplan of the fifth-order $\Delta\Sigma$ modulator.

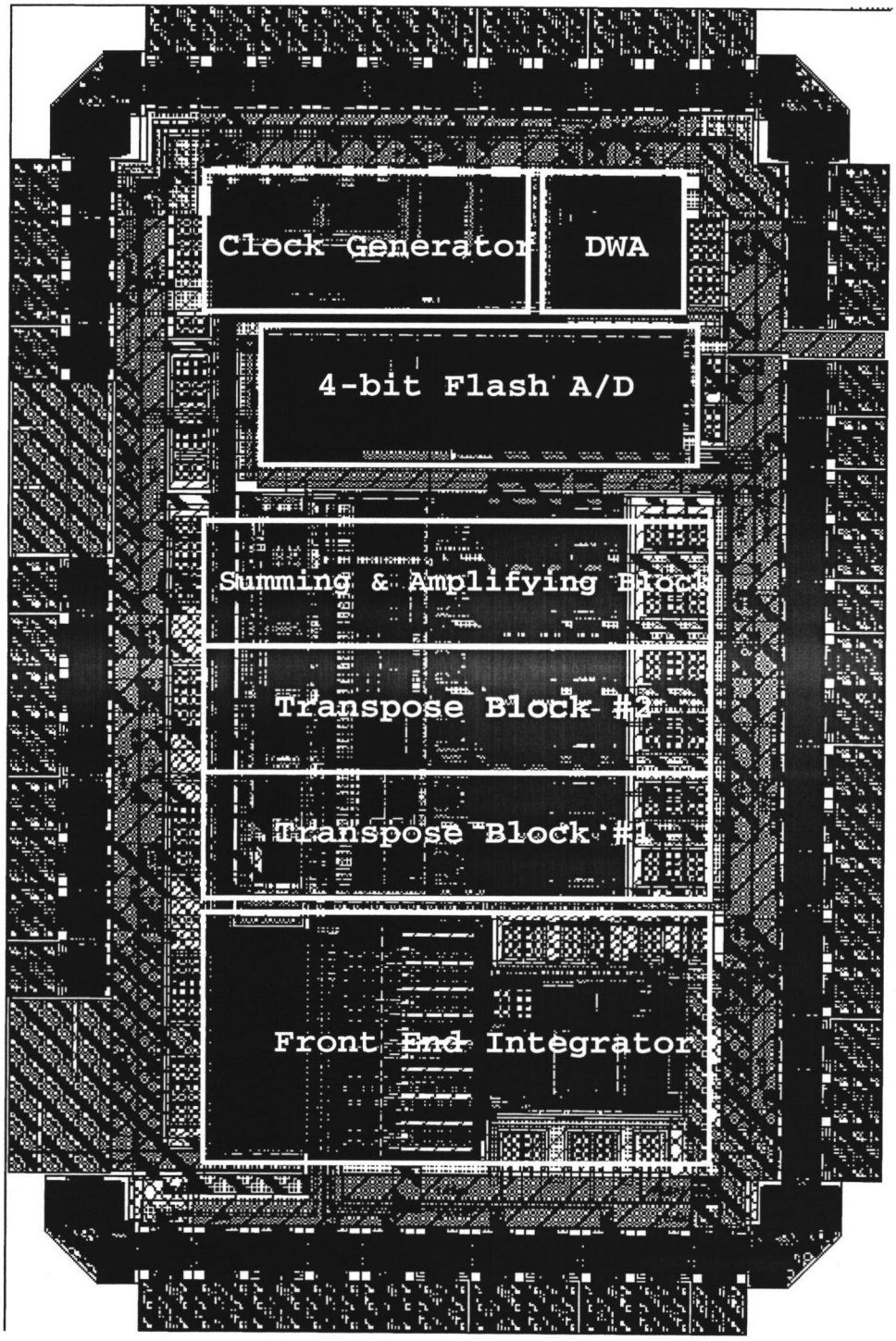


FIGURE 5.20. Layout of the fifth-order hybrid $\Delta\Sigma$ A/D converter.

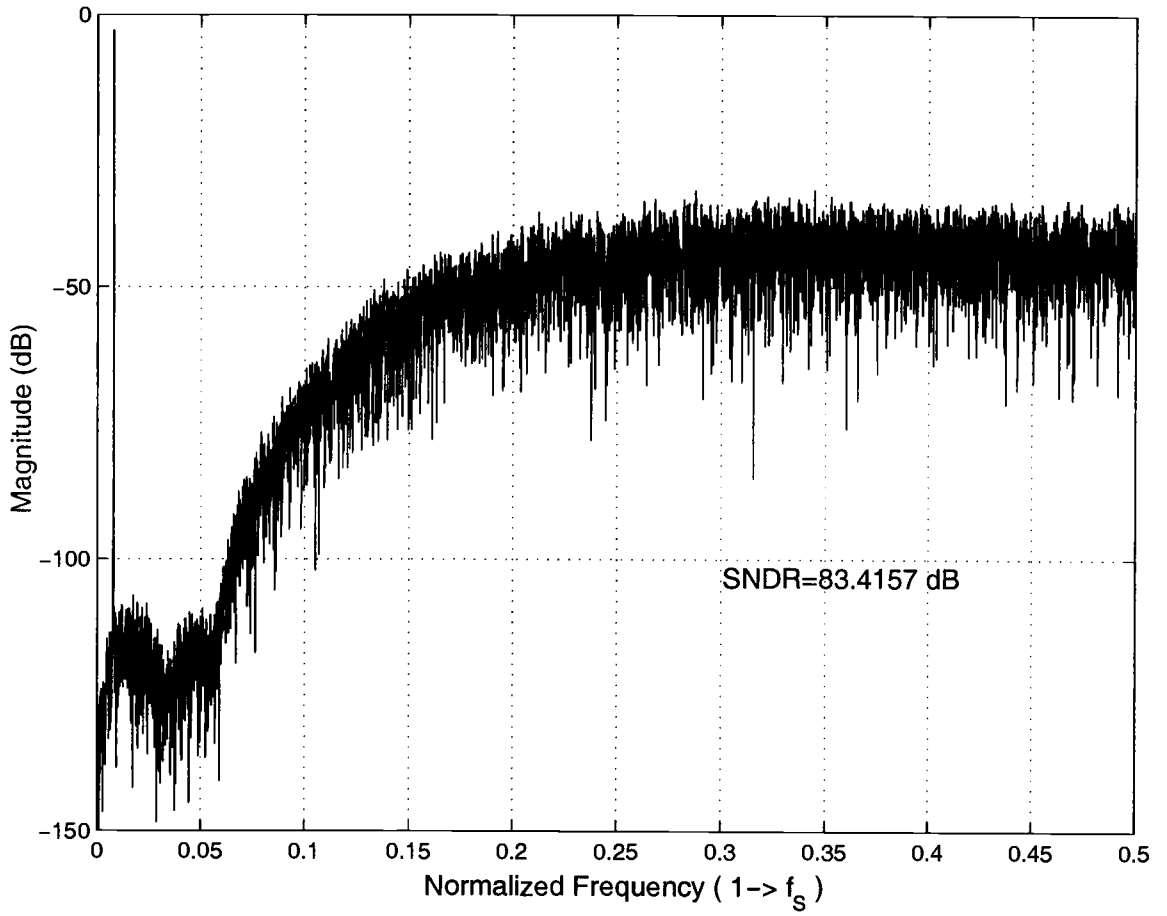


FIGURE 5.21. Simulated spectrum of the fifth-order $\Delta\Sigma$ modulator obtained from Switcap2.

6. MEASUREMENT AND CONCLUSION

6.1. Test Circuit Setup

A four layer printed circuit board has been designed to test the chip. The schematic of the PCB is shown in Appendix D. This $\Delta\Sigma$ A/D converter is designed to achieve 14 bit resolution with 2 MHz input signal bandwidth. Thus, a low noise highly linear signal source is need. The *Audio Precision system two 2322* is used as the signal source. This signal source can achieve an SNDR of 104dB. The *Tektronix TLA 720* logic analyzer is used to acquire the A/D output. The *SONY/Tektronix AWG 520* arbitrary waveform generator is used to generate the clock signals. The test circuit setup is shown in Fig. 6.1.

A four layer printed circuit board is designed. Separate layers are used for ground and power supplies to provide a low noise low interference environment for the $\Delta\Sigma$ A/D chip. The test circuit board generates the reference voltages and the biasing current as shown in Appendix D.

The *Audio Precision system two 2322* achieves the maximum SNDR at approximately $6 - 8V_{P\_P}$ output swing. The $\Delta\Sigma$ A/D has only $0.73V_{P\_P}$ input dynamic range. If the outputs of the *Audio Precision system two 2322* are applied directly to the A/D inputs, it can only provide input signals with about 84 dB SNDR. This will limit the accuracy of the measurement. Thus the input signal needs to be attenuated before it is applied to the A/D input. Figure 6.2 shows

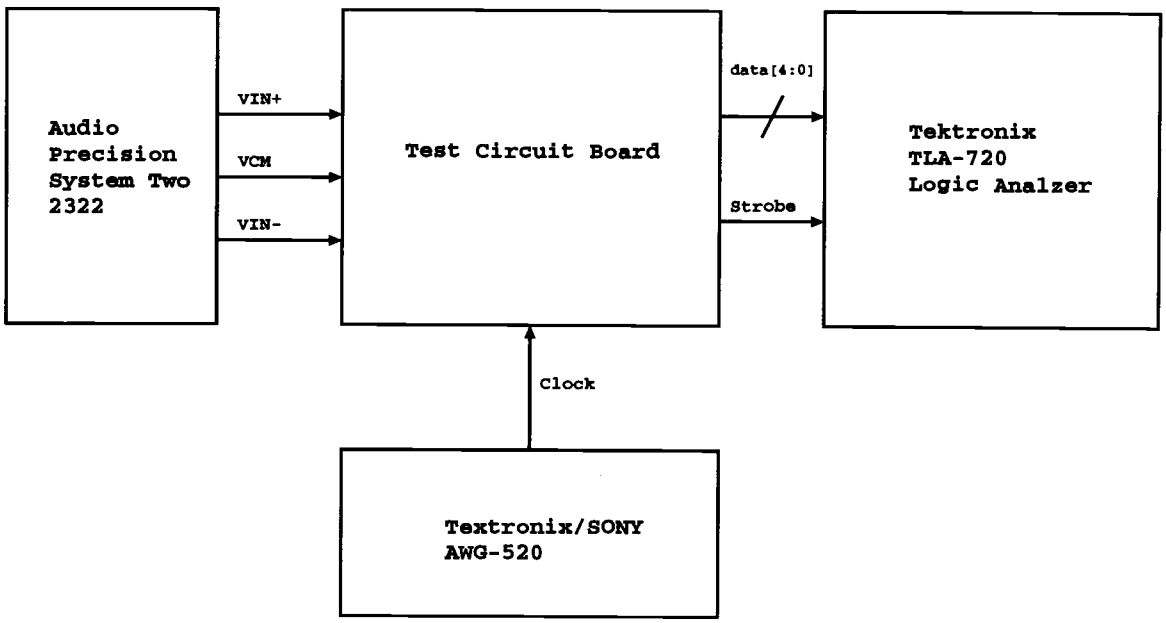


FIGURE 6.1. Block diagrm of the $\Delta\Sigma$ A/D test circuit setup.

the schematic of the attenuator. It provides -20.8dB attenuation and limits the bandwidth to about 3MHz.

6.2. Measured Results

Since the A/D converter uses only a single 1.8 V power supply, the dynamic range is very small. Special care is taken in shielding the circuit board from external noises. The Agilent E3631A power supply has large tones at 120KHz and its harmonics. It results in about $100\mu V - 200\mu V$ tones in the baseband, which is about 4-8 LSBs. To overcome this problem, two 6-V batteries are used as the power supply and the tones disappear. The circuit board is put inside a metal box.

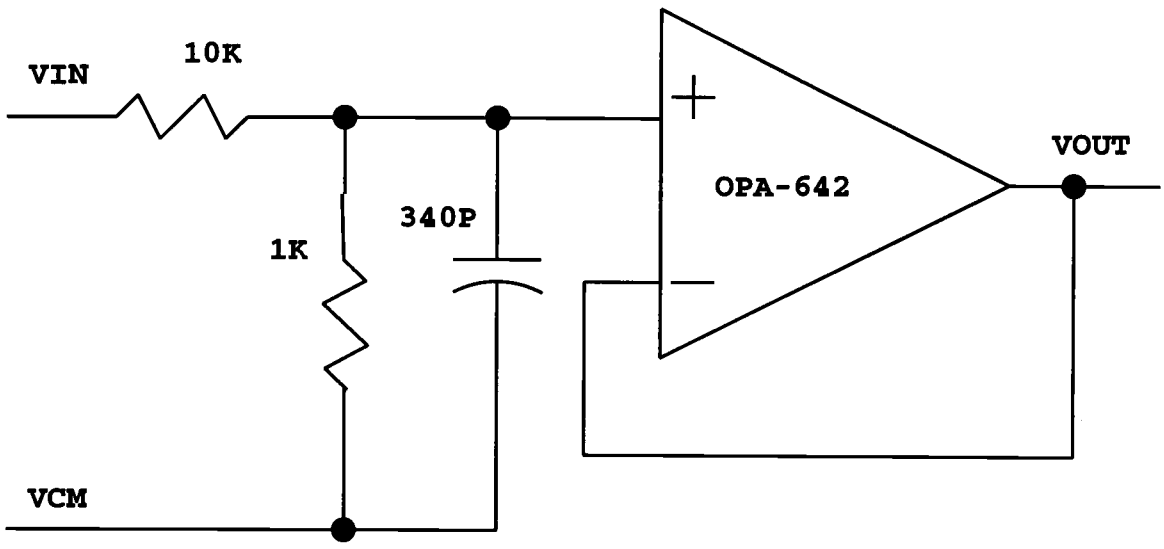


FIGURE 6.2. The attenuator at the input of the A/D converter.

The ground of the circuit board is connected to the metal box. Measurement also shows that multi-point grounding between the circuit board and the box can help to reduce baseband noise. The photo of the test equipment is shown in Fig. 6.3. Figure 6.4 shows the test circuit board with the $\Delta\Sigma$ A/D converter.

The A/D is measured with and without the DWA algorithm, and a clock frequency of 32MHz as shown in Fig. 6.5. The input signal frequency is 125KHz. The SNDR is 81.63dB with 103dB SFDR. The linearity is very good and there are almost no noticeable tones. Without the DWA algorithm, the SNDR is 76.80dB with 83.09dB SFDR. From Fig. 6.5, it can be seen that the equi-ripple baseband noise shaping is smeared because of noise. And the out of band noise shaping envelope has a small peaking. This is due to capacitor mismatch. A small deviation

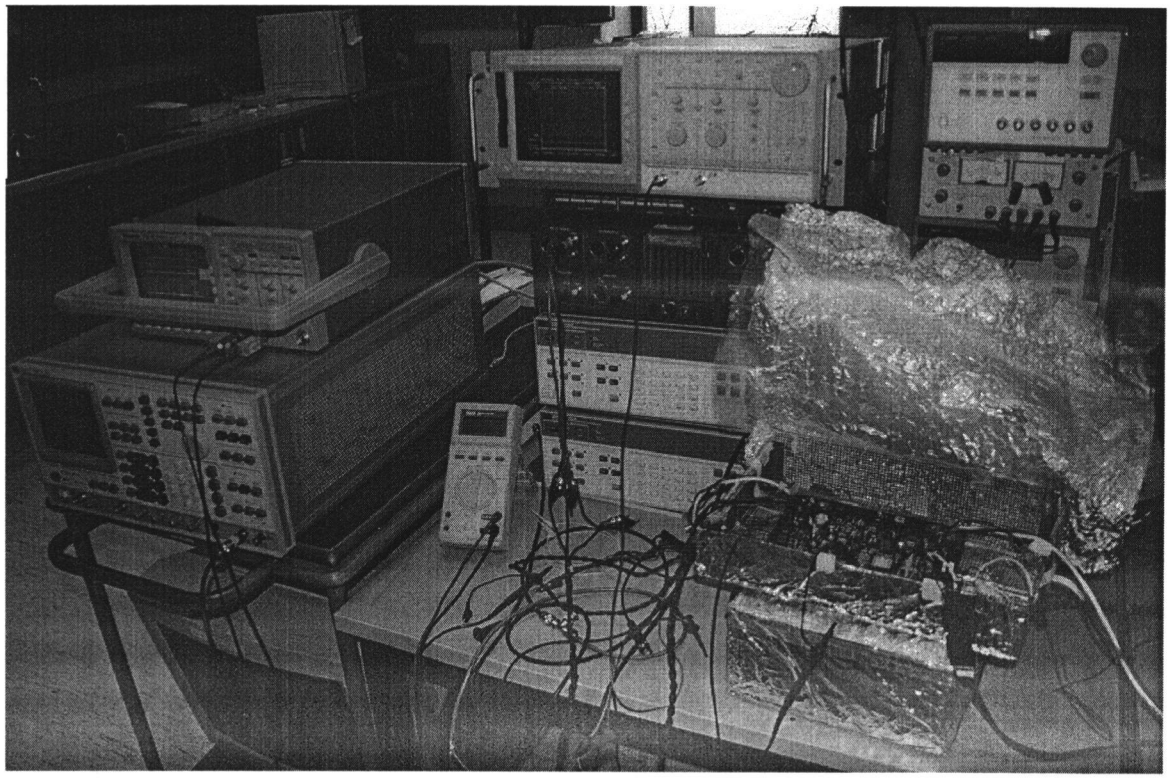


FIGURE 6.3. Photo of the test equipment of the $\Delta\Sigma$ A/D converter.

of the capacitance will move the NTF poles and zeros away from their ideal positions and the Q of the second-order transposed direct form II blocks will change correspondingly. Due to the low coefficient sensitivity, the overall performance is still very good. This result also proves that DWA can effectively suppress the DAC non-linearity for this $\Delta\Sigma$ modulator structure.

The input signal level is swept and the output is measured. Figure 6.6 shows the SNDR and SFDR of the $\Delta\Sigma$ A/D converter as a function of input signal level. The maximum SNDR drops by about 6 dB if no algorithm is used. The maximum

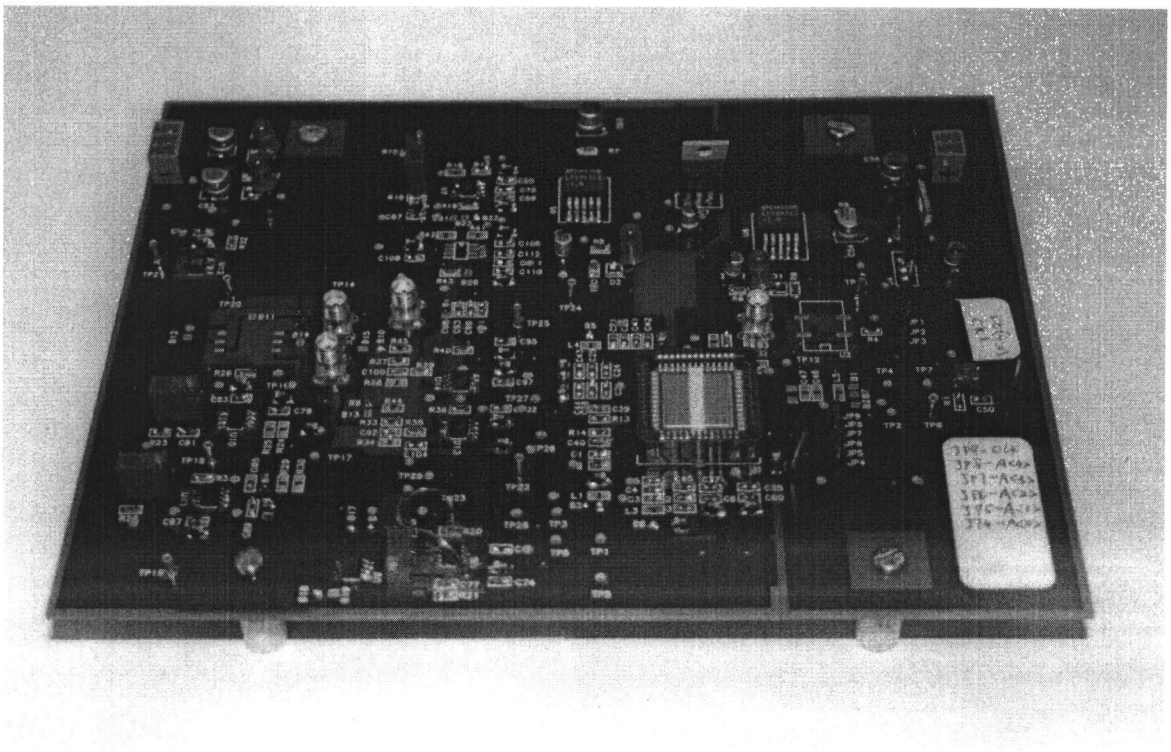


FIGURE 6.4. Photo of the test circuit board with the $\Delta\Sigma$ A/D converter.

SFDR drops by about 20 dB without the DWA algorithm. As the input signal level decreases, the difference becomes smaller. When the input signal level is -40 dB or less, the difference is negligible. The dynamic range of the $\Delta\Sigma$ A/D converter is about 83dB.

Different clock frequencies are used to test the A/D performance. Figure 6.7 shows the maximum SNDR and maximum SFDR with various clock frequencies. The A/D performance is very stable for clock frequencies less than approximately 34 MHz. Beyond this frequency, incomplete settling will severely degrade the A/D performance. The speed bottle neck is the zero delay summing and amplifying

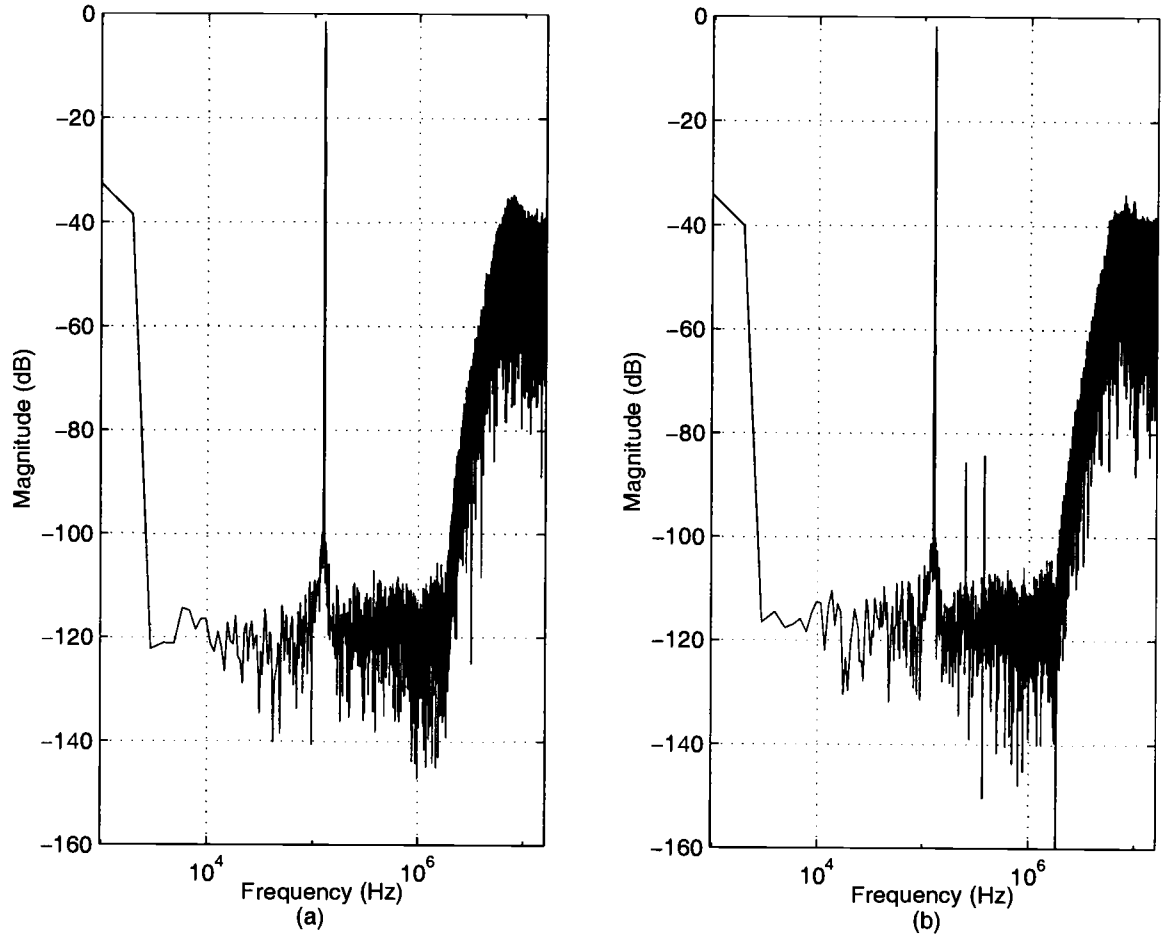


FIGURE 6.5. Measured spectra of the $\Delta\Sigma$ modulator with a clock frequency of 32 MHz and an input signal frequency of 125KHz. (a) SNDR=81.63dB with the DWA algorithm, and (b) SNDR=76.80 dB without the DWA algorithm.

block shown in Fig. 4.10. Different frequency input signals are measured with a 32MHz clock. Figure 6.8 shows the measured spectra with a input signal frequency of 500KHz and 1MHz, repsectively. Figure 6.9 shows the SNDR and SFDR as a function of the input signal frequency. The measured result of the A/D converter are summarized in Table 6.1.

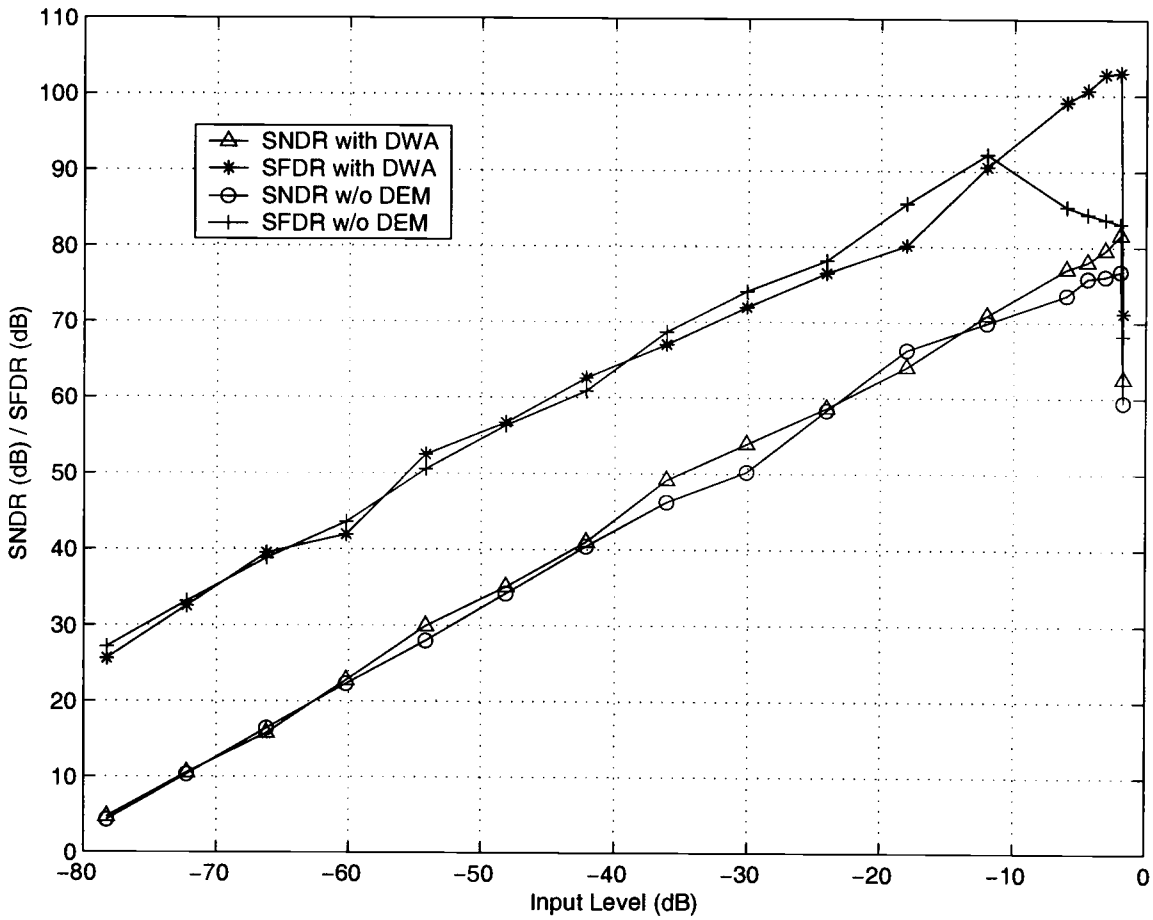


FIGURE 6.6. Measured SNDR and SFDR as a function of the input signal level with a clock frequency of 32 MHz and an input frequency of 125KHz.

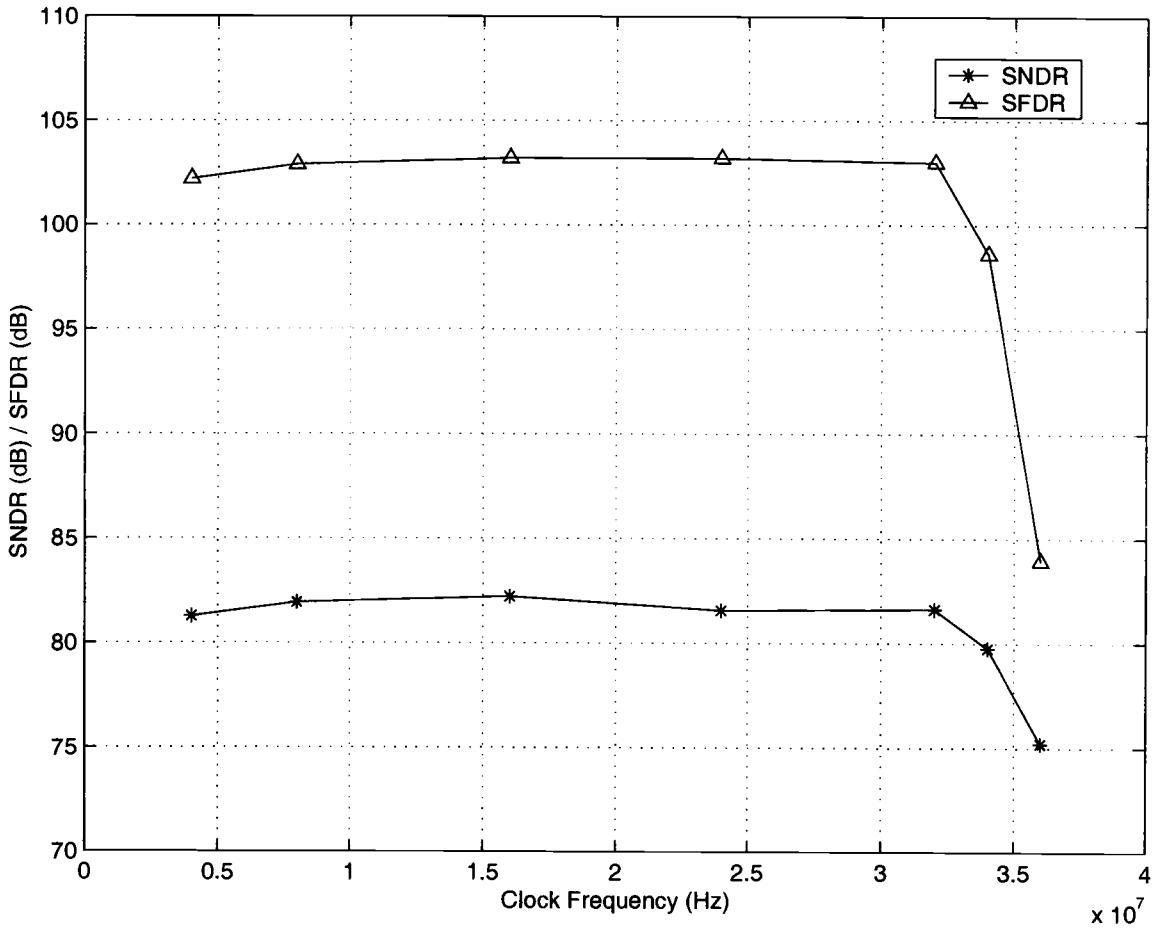


FIGURE 6.7. Measured maximum SNDR and maximum SFDR as a function of clock frequency, the input signal is 125KHz.

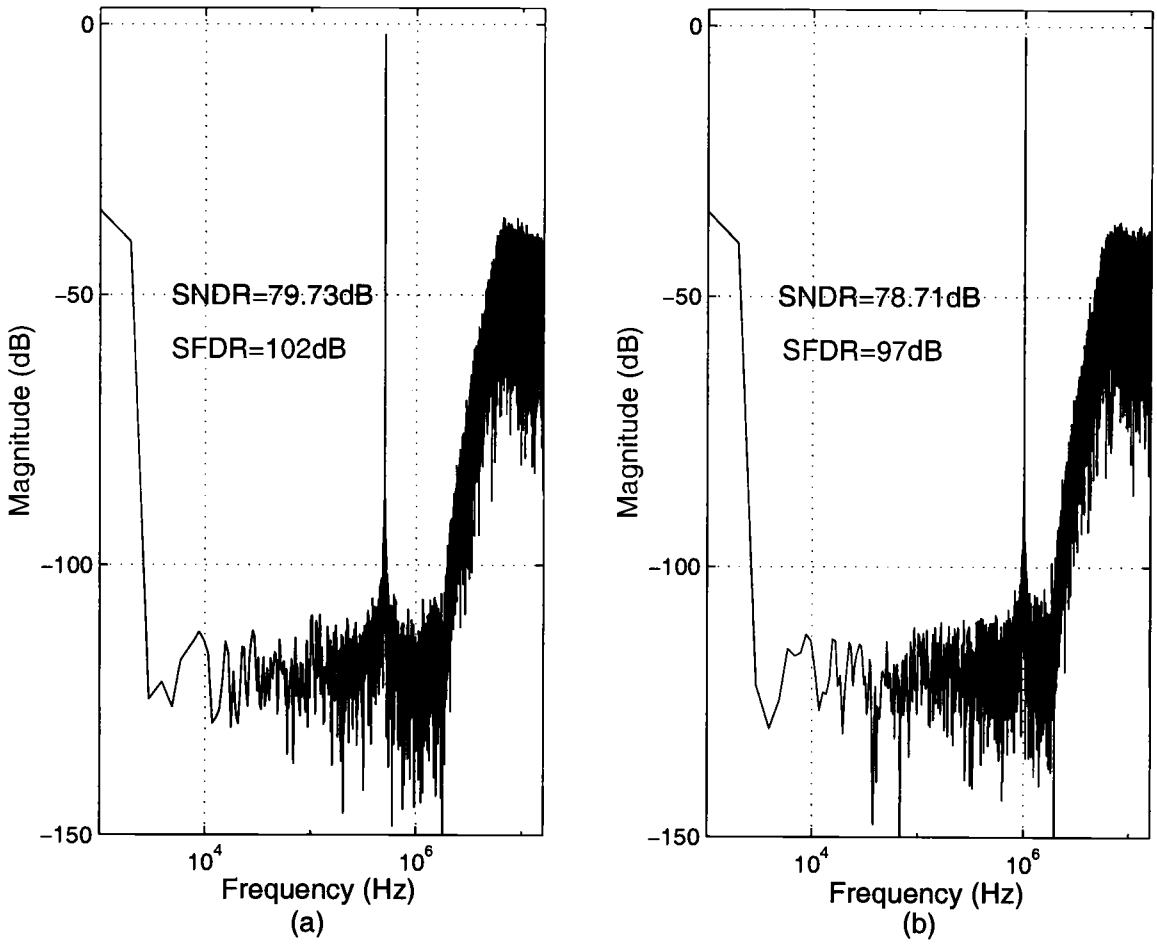


FIGURE 6.8. Measured spectra of the $\Delta\Sigma$ A/D converter with different input signal frequencies and a 32MHz clock, (a) f_{in}=500KHz, (b) f_{in}=1MHz.

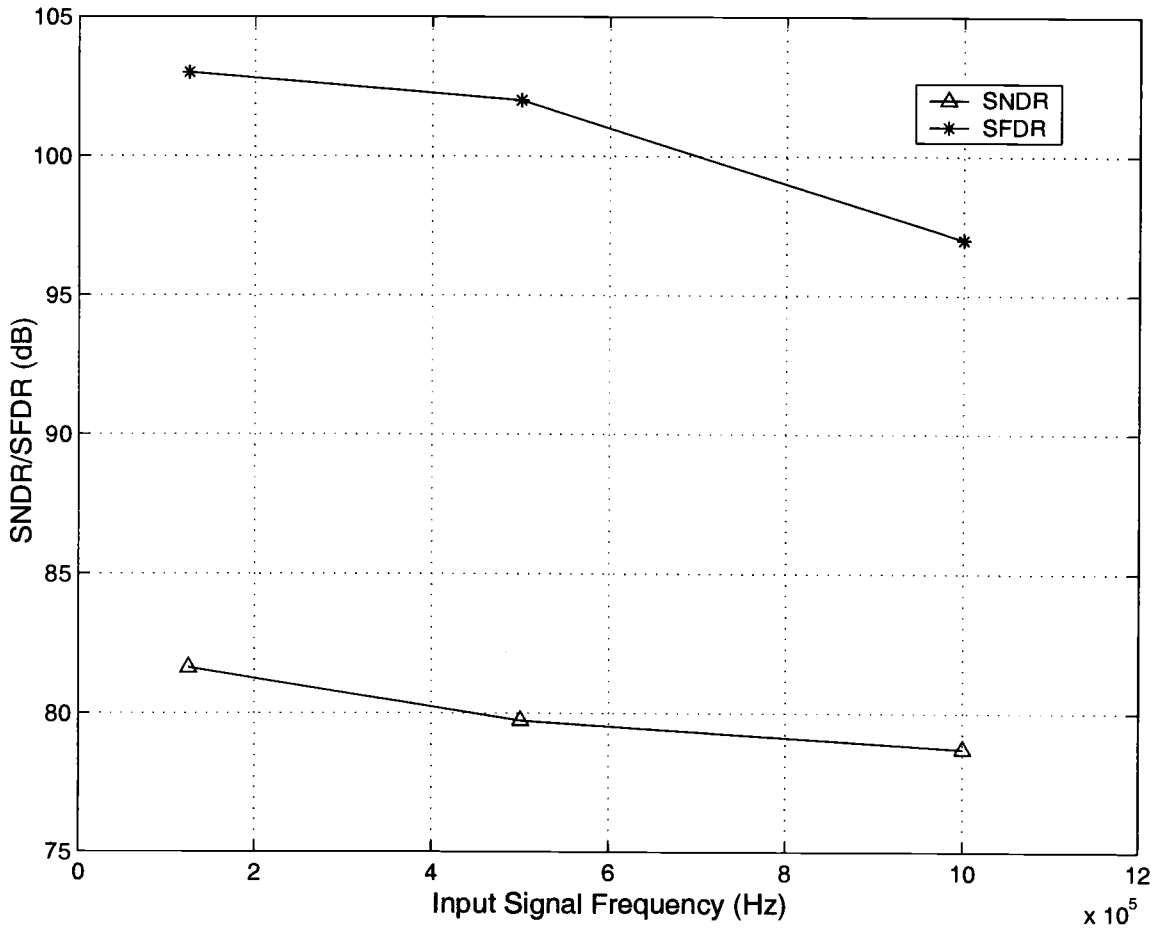


FIGURE 6.9. Measured SNDR and SFDR as a function of input signal frequency with a 32MHz clock.

TABLE 6.1. Specifications of the Fifth-Order Hybrid $\Delta\Sigma$ A/D Converter with a Clock Frequency of 32 MHz and an Input Signal Frequency of 125 KHz.

Specification	Value
Max. SNDR	81.63dB
Max. SFDR	103dB
Dynamic Range	83dB
OSR	8
Input Signal BW	2 MHz
Power Supply	1.8 V
Analog Power	102mW
Digital Power	47mW
Die Area (w/o Pads)	1.3mm X 2.2mm
Die Area (w/ Pads)	1.8mm X 2.6mm
Process	0.18 μm 2-poly 5-metal CMOS

6.3. Comparison of This Work with Existing Designs

There are some existing low oversampling $\Delta\Sigma$ A/D converters [3], [4], [5], [6], [14]. Table 6.2 compares the specifications of this design with some previous designs. It can be seen that all other designs (except [5]) use 5 volt power supplies. This can greatly increase the signal dynamic range. Thus KT/C noise and thermal noise are much less and the opamp gain can be very high. This design uses a single 1.8 V power supply with a full scale input of $\pm 0.5V$ and the opamp DC gain is only 43 dB - 45 dB. Thus designing such an A/D converter becomes very difficult, because the relative noise floor is much higher than others and the integrator leakage is also greater.

Due to the use of the hybrid structure, a stable fifth-order single loop $\Delta\Sigma$ A/D is implemented. The single loop structure greatly supresses the leakage and the high-order structure helps to achieve 14-bit resolution with only 8X oversampling. The power and area of this chip are only slightly higher than [14]. But it achieves the widest input signal bandwidth. With a single 1.8 V power supply, this A/D has a maximum stable input of $\pm 0.36V$. The input signal dynamic range is much smaller than those with 5 V or 3.3 V power supplies. The overall performance of this chip is better than all other designs shown in Table 6.2.

Figure of merit is a commonly used method to evaluate different A/D converters. To take the low supply voltage into account, the figure of merit (FM) is defined as:

$$FM = \frac{4KTD_rF_N}{P_tLSB} \tag{6.1}$$

where D_r is the dynamic range, F_N is the Nyquist frequency, P_t is the total power consumption and LSB is the least significant bit expressed in volt. The figure of merits of some existing low oversampling $\Delta\Sigma$ A/D converters are shown in

TABLE 6.2. Comparison of this design and some previous designs.

Refs	SNDR	Bandwidth	OSR	Topology	Quantizer(s)	Process	Power
[3]	88 dB	1.25 MHz	8	2-0	5b, 10b	0.6u 5V	550mW
[4]	89 dB	1.25 MHz	24	3rd	6b X 3	0.65u 5V	152mW
[5]	82 dB	1.1 MHz	24	2-1-1	1b X 3	0.5u 3.3V	200mW
[6]	87 dB	1.25 MHz	8	2-1-1	4b X 3	0.5u 5V	105mW
[14]	78 dB	0.25 MHz	16	4th	4b	1.2u 5V	58mW
This Work	81.63dB	2 MHz	8	5th	4b	0.18u 1.8V	149mW

Fig. 6.10. This design achieves the highest figure of merit and the highest output Nyquist rate. The overall performance of this chip is the best.

6.4. Conclusion and Future Work

In this dissertation, the relationship between $\|H\|_\infty$ and the $\Delta\Sigma$ modulator performance is discussed. It has been found that, for a low oversampling single stage $\Delta\Sigma$ modulator, a low $\|H\|_\infty$ can generate tones in the baseband. Increasing $\|H\|_\infty$ is an effective way to increase the SNR and to reduce the baseband tones. Existing single stage $\Delta\Sigma$ modulators become unstable with a high $\|H\|_\infty$. A new $\Delta\Sigma$ modulator structure is proposed, which can implement a stable high-order single-stage $\Delta\Sigma$ modulator with a high $\|H\|_\infty$. This new structure has very small coefficient spread and is insensitive to coefficient variations. A fifth-order 8X oversampling $\Delta\Sigma$ A/D has been designed and tested. This chip achieves a maximum SNDR of 81.63dB and a dynamic range of 83dB. The spurious free dynamic range is 103dB. The measured results show that this new structure is very suitable for low oversampling high order

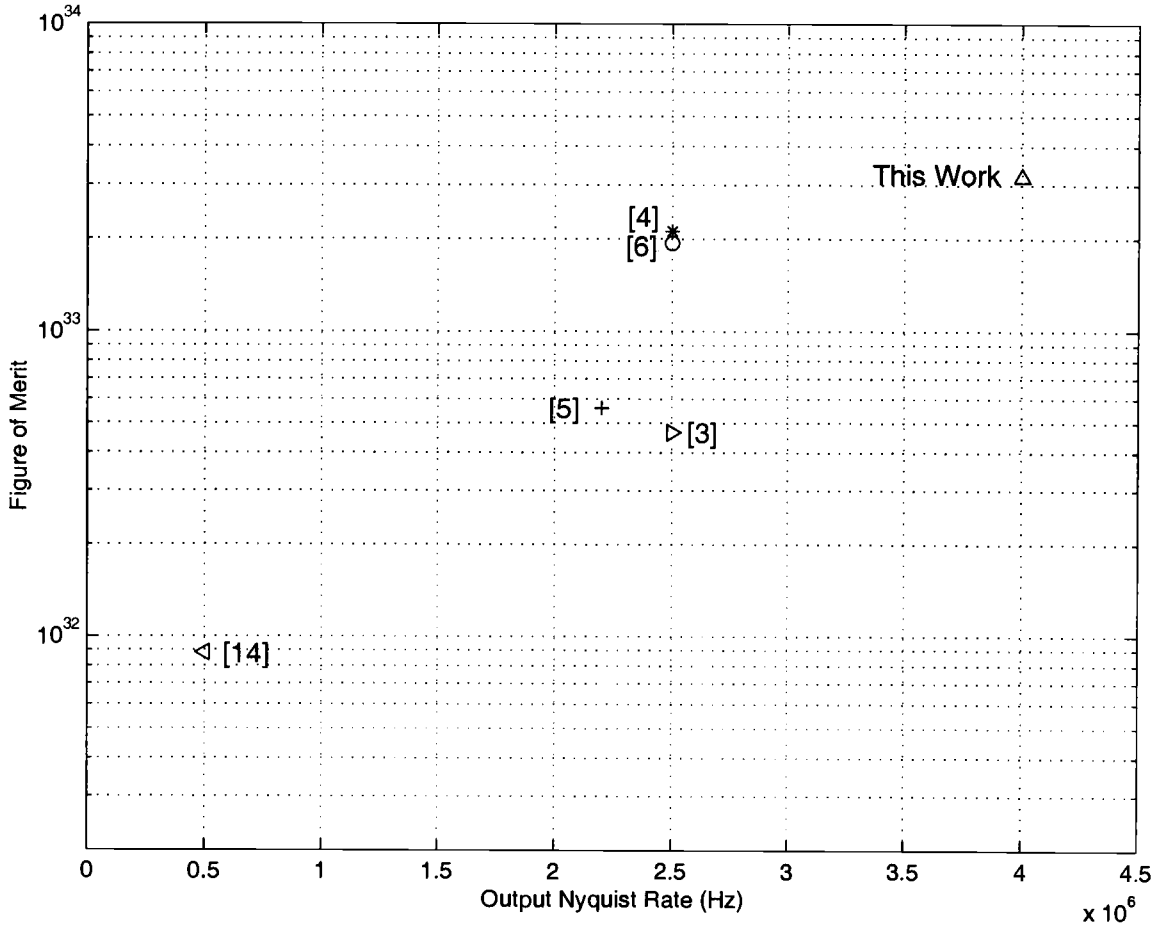


FIGURE 6.10. Figure of merits of some low oversampling $\Delta\Sigma$ A/D converters.

high resolution applications. This is the first single stage $\Delta\Sigma$ A/D reported that can achieve 14 bit resolution, 2 MHz input signal bandwidth with a 1.8 V power supply.

However, there are still more issues to work on in the future. In this dissertation, it is shown that a low $\|H\|_\infty$ can generate extra tones in the baseband. These tones are not due to limit cycles and are very important for low oversampling single stage $\Delta\Sigma$ A/D converters. The reason behind it is very complicated. This

dissertation only gives an intuitive explanation. Future work is needed to clearly find the relationship between $\|H\|_\infty$ and the baseband tones. The hybrid structure used in this design shows that embedding analog delay blocks in the forward path of a $\Delta\Sigma$ modulator is a good way of designing high-order single stage $\Delta\Sigma$ modulators. Further research should focus on finding the best *delay-based* $\Delta\Sigma$ modulator structures.

7. DESIGN OF A MULTI-INPUT DOUBLE BALANCED CMOS MULTIPLIER

7.1. Introduction

In this chapter, the design of a multi-input double balanced CMOS multiplier is described. Previous floating-gate multi-input multipliers require special processing for the floating-gate and the implemented floating multiplier can operate at tens of kilo hertz frequency. As a result, it is only suitable for instrumentation applications [45]. This design uses multiple capacitors in a standard CMOS process instead of specialized floating gates and the output frequency range is from 1 MHz to 100 MHz. This multiplier is suitable for communication applications such as up conversion and down conversion of signals.

The multiplier is an important component in analog circuit design. There are many kinds of multipliers. Most of them [46], [47] are derived from the Gilbert six transistor multiplier core. For these kinds of multipliers, the output is a linear approximation of the product of the input signals. When the input signal amplitude is high, harmonic distortion increases considerably. Predistortion circuits can be used to increase the linearity, but the harmonic distortion of a Gilbert multiplier is typically limited to 0.7% - 2%.

Some CMOS multipliers use the square law of MOS transistors to increase the linearity [46]. Mehrvarz and Kwok [45] proposed a novel multiplier with multi-input floating-gate inputs. Two input signals are capacitively coupled at the floating gates of the input MOS transistors. If short channel effects, mobility degradation

and channel length modulation effects are negligible, the output is a pure product of the two input signals. The total harmonic distortion (THD) is typically 0.3% - 0.5%. In this chapter, a new multiplier based on [45] is developed. This multiplier operates in the frequency range of 1MHz to 100MHz and can be used for data communication applications.

7.2. Principles of Multi-Input Multipliers

Figure 7.1 shows the schematic of the multi-input floating-gate multiplier proposed by Mehrvarz and Kwok [45]. Each input transistor has a floating gate and three top gates. The top gates are put along the channel length direction. This is shown in Fig. 7.2. In [45], to accommodate the three top gates, the channel length of each input MOS transistor is $20\mu m$. Thus the bandwidth of the multiplier is usually less than 1 MHz and it is suitable only for instrumentation applications.

Figure 7.3 shows all the capacitors connected to the floating gate. The total capacitance C_T at the floating gate node is [45]:

$$C_T = \sum_{i=1}^{3} C_i + \frac{2}{3}C_{OX} + C_{FD} + C_{FS} + C_{FB} \tag{7.1}$$

where C_{FD} is the capacitance between the floating gate and the drain, C_{FS} is the capacitance between the floating gate and the source and C_{FB} is the capacitance between the floating gate and the substrate. Since the floating gate is capacitively coupled, the voltage of the floating gate is a weighted sum of the three input signals V_i, the substrate voltage V_B, the source voltage V_S and the threshold voltage V_T. The drain current I_D of the input transistors is [45]:

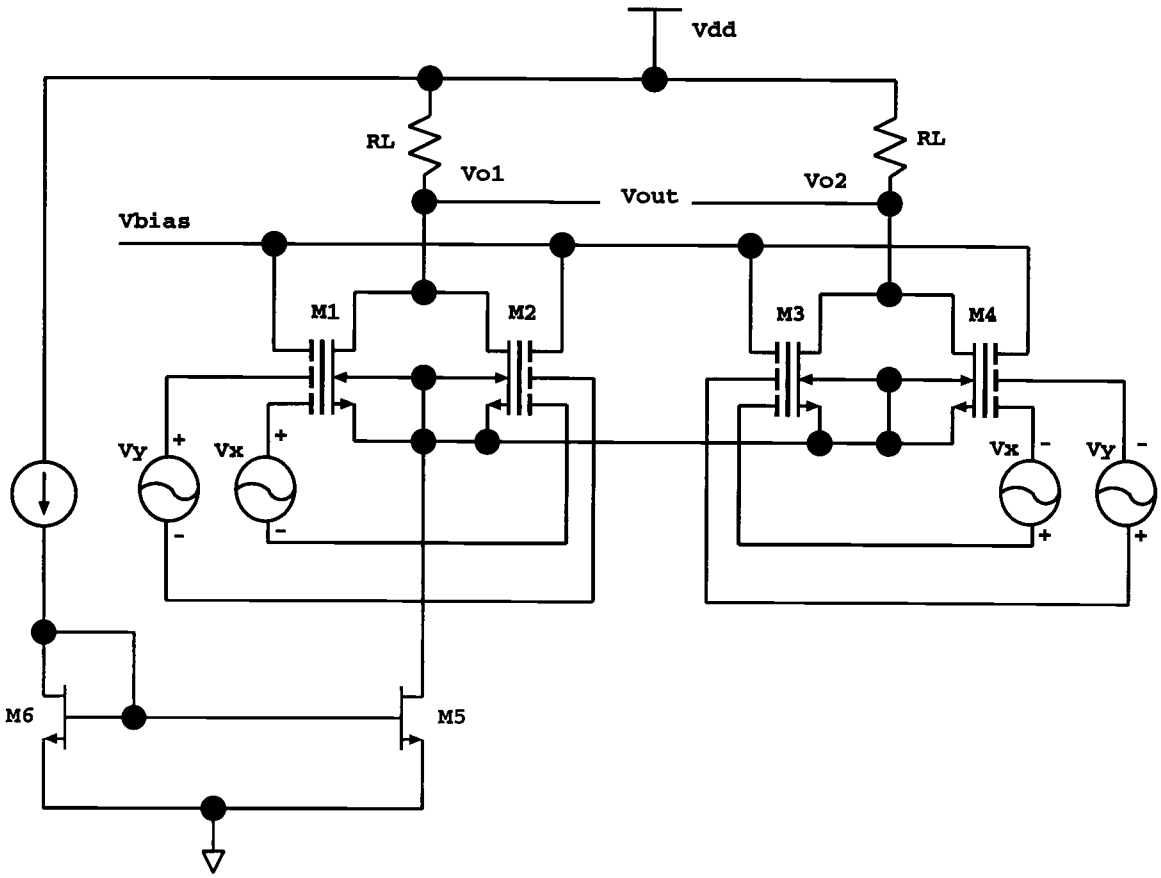


FIGURE 7.1. Schematic of the multi-input floating-gate multiplier.

$$I_D = \tfrac{1}{2}K(\textstyle\sum_{i=1}^{3} W_i V_i + W_B V_B - W_S V_S - W_T V_T)^2 \tag{7.2}$$

where $W_i = \frac{C_i}{C_T}$ is the coupling ratios of the input signals, $W_B = \frac{C_{FB}}{C_T}$ is the coupling ratio of the substrate voltage, $W_S = 1 - \frac{2C_{OX}}{3C_T} - \frac{C_{FS}}{C_T}$ is the coupling ratio of the source voltage, and $W_T = 1 - \frac{2C_{OX}}{3C_T}$ is the coupling ratio of the threshold voltage. For the multiplier shown in Fig. 7.1, the output voltage V_o is [45]:

$$V_o = (I_{o1} - I_{o2})R_L$$

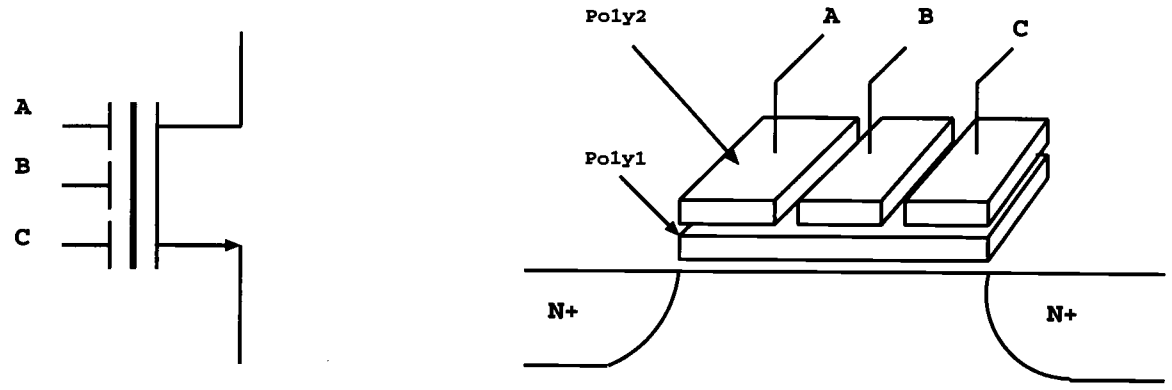


FIGURE 7.2. Illustration of a multi-input floating-gate MOSFET.

$$
\begin{aligned}
&= \frac{1}{2}KR_L\left\{\left[(\frac{1}{2}W_iV_X + \frac{1}{2}W_iV_Y + W_{iB}V_{Bias} + W_BV_B - W_SV_S - W_TV_T)^2\right.\right. \\
&\quad \left.+(-\frac{1}{2}W_iVX - \frac{1}{2}W_iV_Y + W_{iB}V_{Bias} + W_BV_B - W_SV_S - W_TV_T)^2\right] \\
&\quad - \left[(\frac{1}{2}W_iV_X - \frac{1}{2}W_iV_Y + W_{iB}V_{Bias} + W_BV_B - W_SV_S - W_TV_T)^2\right. \\
&\quad \left.\left.+(-\frac{1}{2}W_iV_X + \frac{1}{2}W_iV_Y + W_{iB}V_{Bias} + W_BV_B - W_SV_S - W_TV_T)^2\right]\right\} \\
&= KR_LW_i^2V_XV_Y \qquad (7.3)
\end{aligned}
$$

From (7.2), the output V_o is an ideal product of the input signal V_X and V_Y. Thus it is a double balanced multiplier and the potential linearity can be very high.

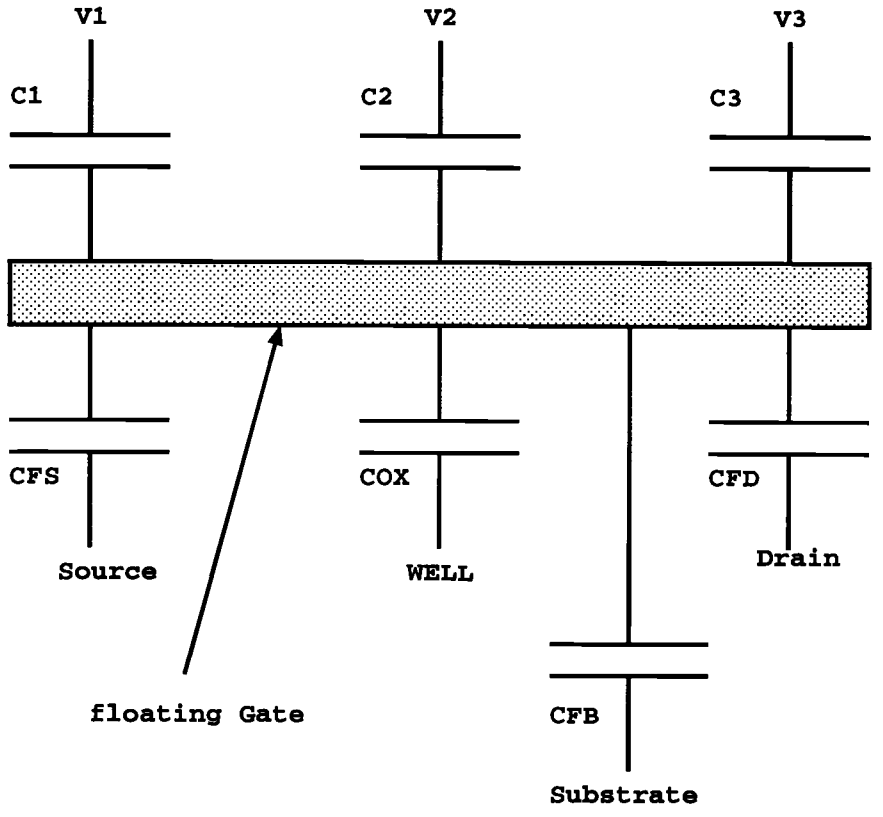


FIGURE 7.3. Illustration of all capactiors connected to the floating gate.

7.3. Design of a CMOS Multi-Input Multiplier

The multi-input floating-gate multiplier proposed by Mehrvarz and Kwok [45] has very low bandwidth and is not suitable for up conversion or down conversion of high speed signals. The two resistive loads R_L in Fig. 7.1 introduce extra mismatch errors and the floating gate process is not a standard CMOS process.

In order to overcome these limitations, a new multiplier is derived from the multi-input floating-gate multiplier. The schematic of the new multiplier is shown in Fig. 7.4. Poly-poly capacitors are used to sum the input signals at the gates of the input differential pairs $M_1 - M_4$. PMOS input transistors are used in order to connect the substrate to the source. Four long channel length transistors $M_7 - M_{10}$ biased in the triode region are used to bias the DC operating point of the input transistors. A high swing current mirror is used to generate a single-ended output and to drive the 50 ohm load. The cascode output provides high output resistance, which allows the use of shorter channel length transistors without significantly reducing the linearity of the multiplier. M_{11} is used to reduce the capacitive load at the drain of M_5.

Table 7.1 shows the channel widths and lengths of the transistors shown in Fig. 7.4. Large transistors are used to reduce the mismatch and to drive the 50 ohm load. The drain currents of M_5 and M_6 are both 2.4mA. By driving a 50 ohm load, the multiplier has an output swing of 0.2 V_{P-P}, $C_1 - C_4$ are 5.6 pF each, and $C_{P1} - C_{P4}$ are the parasitic capacitances at the input node. These parasitic capacitances are usually very small compared with $C_1 - C_4$.

TABLE 7.1. The W/L of the Transistors Shown in Fig. 7.4

Transistors	$W/L(um/um)$
M1-M4	576/0.8
M5,M6	1152/0.8
M7-M10	1.2/48
M11	384/0.8

7.4. Harmonic Distortion Analysis and Simulation Results

Systematic and random errors will both effect the performance of the multiplier. There are two types of errors: Systematic errors, including mobility saturation and channel length modulation effects and they result in odd harmonics. Random errors are due to threshold mismatch, channel length/width mismatch, and capacitance mismatch. Random errors create both odd and even harmonics. However, random errors can be reduced greatly if transistor sizes and capacitor sizes are carefully chosen and laid out.

When V_{GS} is high, the mobility of the MOSFET will decrease. The relationship is given by [48]:

$$\mu = \frac{\mu_0}{1-\theta(V_{GS}-V_T)} \tag{7.4}$$

Where $\theta \approx \frac{2\times10^{-9}m/V}{t_{OX}}$ is a process dependent parameter. A 0.35 μm CMOS process is used for this chip. For this process, $\theta \approx 0.22V^{-1}$. If the signal $V_X = V_{AC}sin(\omega t)$ and we substitute (7.4) into (7.2), the third-order harmonic distortion due to mobility saturation is [45]:

$$|H_{D3}| \approx \frac{3\theta W_i^2 V_{AC}^2}{16\sqrt{\frac{2I_{SS}}{K}-W_i^2V_Y^2}} \tag{7.5}$$

In this design, $\theta \approx 0.22V^{-1}$, $W_i \approx 0.4$, $V_{AC} \approx 0.4V$, $I_{SS} \approx 2.4mA$, $K \approx 4.4mA/V^2$, $V_Y \approx 0.4V$, then $|H_{D3}| \approx 0.099\%$.

Channel length modulation effects are another important systematic error source. In the multiplier shown in Fig. 7.1, the drains of the input transistors are connected to the resistive load. The third order harmonic distortion due to channel length modulation is [45]:

$$|H_{D3}| \approx \frac{\lambda W_i^2}{16W_S\sqrt{\frac{2I_{SS}}{K} - W_i^2 V_Y^2}} V_{AC}^2 \tag{7.6}$$

But for the new multiplier, the resistance seen at the drains of the input transistors is approximately $\frac{1}{g_{m5}} \approx 58\ ohm$. The voltage swing at the drains of the input transistors is less than the output swing (about 50% at the maximum output swing). Thus the third-order harmonic distortion due to the channel length modulation of the input transistors is less than that predicted by (7.6). However, the resistance at the drains of the input transistors is non-linear. Thus, we use the estimate of (7.6) for the harmonic distortion. For this design, $\lambda \approx 0.175V^{-1}$, $W_S \approx 0.15$ and $|H_{D3}| \approx 0.175\%$.

The cascode current mirror output (shown in Fig. 7.4) also has finite output impedance which will also introduce distortion. The cascode output impedance is 187K ohm, while the resistive load is only 50 ohms. About $\frac{50}{187K} = 0.0267\%$ current will not flow to the 50 ohm load. The harmonic distortion caused by the finite output impedance is less than 0.0267%, because only a portion of the 0.0267% current is non-linear. Thus, the finite output impedance is not a significant source of distortion for this design.

The above distortions are due to systematic errors and usually they are correlated. Thus the total distortion due to systematic errors (assuming $|H_{D3}|$ is the dominant term) is approximately $0.099\% + 0.175\% + 0.0267\% = 0.3007\%$. Figure 7.5

shows the simulation results of the new multiplier. The two input signals are 64 MHz and 70 MHz, respectively with amplitudes of 0.8 Vp-p. All systematic errors are included in the simulation. The simulated THD is 0.29% for the down conversion. This is very close to the estimated distortion. Ideally the output should only have 6MHz and 134MHz components. But due to harmonic distortion, tones appear at 12MHz, 18MHz, 30MHz, etc. The two high frequency input signals also feedthrough to the output and the isolation is about -54dB. Tones also appear at $134MHz \pm 6MHz$, $134MHz \pm 12MHz$, etc. This is due to the intermodulation of the 6MHz and 134MHz signals. For this reason, this mulitpier is suitable for down conversion and not for up conversion.

Random errors such as input capacitor mismatch, threshold voltage mismatch and transconductance, K, mismatch also introduce extra harmonic distortion. According to [36], the random mismatch of a parameter x of a rectangular object (width=W, length=L) is:

$$\sigma^2(x) = \frac{A_X^2}{WL} + S_X^2 D^2 \tag{7.7}$$

where A_X and S_X are process dependent parameters and D is the distance between two matching objects. Equation (7.7) implies that the error of x has a random term and a gradient term. By using large geometries, the random error term can be reduced. By putting two matching objects close to each other and making them symmetrical, the gradient error can also be reduced. The input transistors $M_1 - M_4$ are very large (576 μm/0.8 μm each). For the 0.35 μm process, there are no data on device mismatch. From [36], it is estimated that, for this process, $A_{VTO} \approx 7mV \times \mu m$, $A_K \approx 8.3\mu m \times \mu A^{1/2} \times V^{-1}$, $S_{VTO} \approx 4\mu V/\mu m$ and $S_K \approx 4 \times 10^{-6} V^{1/2}/\mu m$. For transistors $M_1 - M_4$ in Fig. 7.4, $D \approx 2\mu m$. Thus $\sigma_{VT} \approx 0.326mV$,

$\sigma_K \approx 0.15\mu A/V^2$. By using the $3-\sigma$ rule, the variations of V_T and K for $M_1 - M_4$ are less than $0.978mV$ and $0.45\mu A/V^2$, repsectively. The second harmonics due to V_T and K variations are given by [45]:

$$|H_{D2}| \approx \frac{W_T \sigma V_T}{8V_Y \sqrt{\frac{2I_{SS}}{K} - W_i^2 V_Y^2}} V_{AC} \tag{7.8}$$

$$|H_{D2}| \approx \frac{\sigma K}{K}\left(\frac{W_T \sigma V_T}{16\sqrt{\frac{2I_{SS}}{K} - W_i^2 V_Y^2}}\right) \tag{7.9}$$

Thus, $|H_{D2}|$ due to K mismatch is about 3.0×10^{-6} and $|H_{D2}|$ due to V_T mismatch is about 5.0×10^{-6}. The distortion due to the mismatch of M_{14}, M_{15} is about the same magnitude. Thus the harmonic distortion due to V_T mismatch and K mismatch is negligible.

The input capacitor mismatch also introduces harmonic distortion. A large capacitance is used (5.6 pF each) and common-centriod layout techniques are employed. The mismatch is typically 0.1% - 0.2%. To avoid underestimating the mismatch, 0.5% capacitor mismatch is assumed. The second harmonic distortion $|H_{D2}|$ is about 0.12% and $|H_{D3}|$ is about 0.02%.

The joint total harmonic distortion due to systematic errors and random errors is:

$$THD \approx \sqrt{(0.3007\%)^2 + (0.12\%)^2 + (0.02\%)^2} \approx 0.324\% \tag{7.10}$$

Thus the systematic errors are the major source of distortion for this multiplier. If other factors, such as substrate noise coupling, power supply noise, are taken into account, the total harmonic distortion will increase. But it is still possible for this multiplier to achieve 0.5% THD.

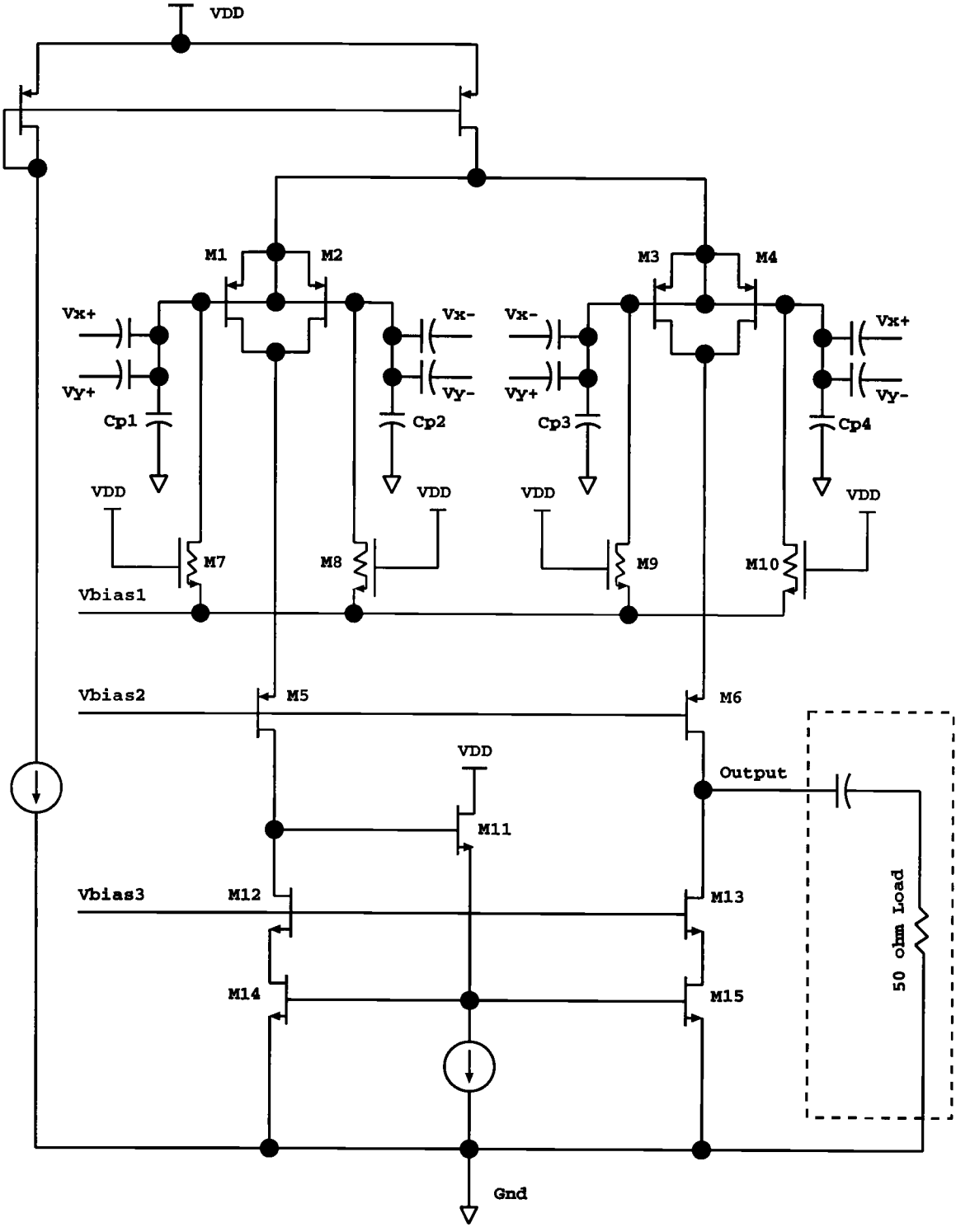


FIGURE 7.4. Schematic of the new multiplier.

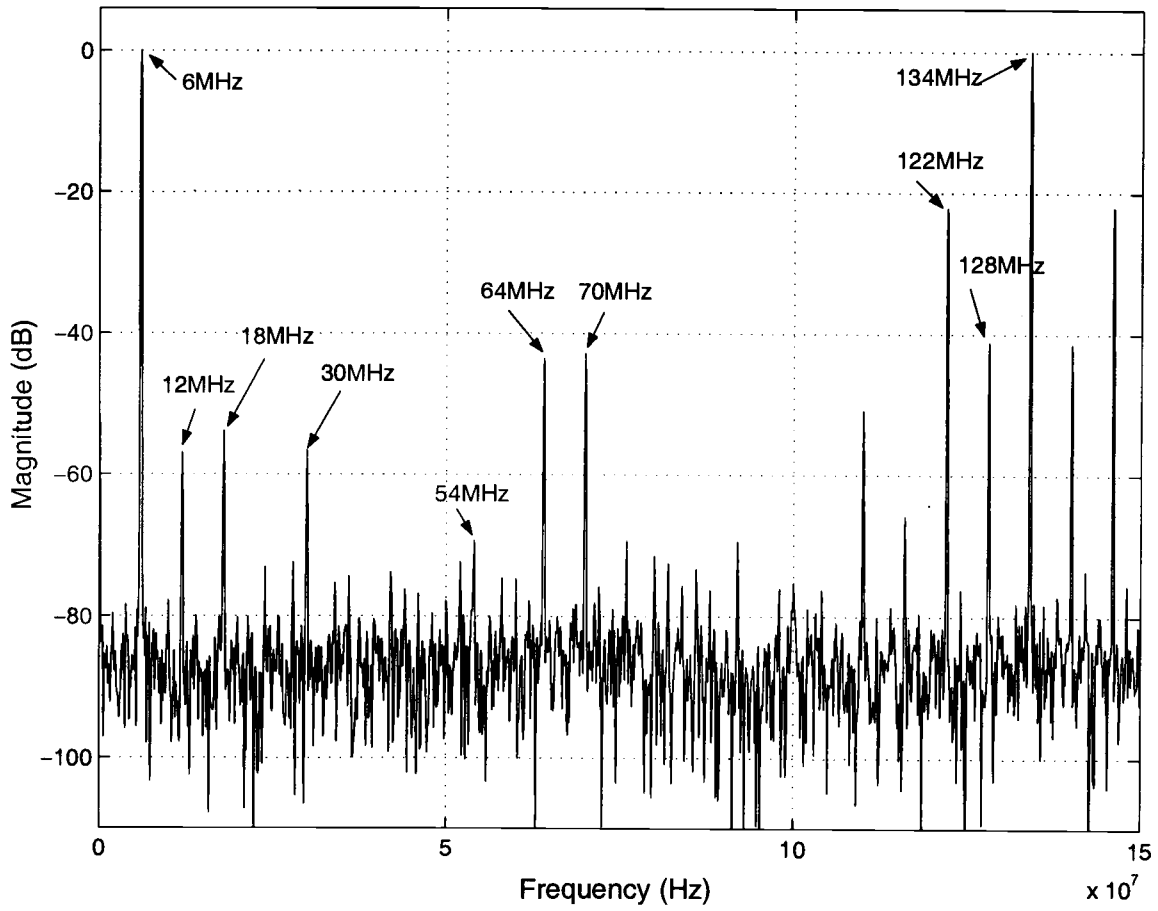


FIGURE 7.5. Simulated down conversion output spectrum of the multiplier where one input is 64MHz $0.8V_{P-P}$ and one input is 70MHz 0.8Vp-p. The output THD is 0.290%.

7.5. Measurement

This multiplier is implemented in a $0.35\mu m$ 3.3 V double poly triple metal CMOS process. Figure 7.6 shows the layout. The eight input coupling capacitors are 5.6pF each. All capacitors are laid out so that they are symmetrical. All transistors requiring matching are laid out using interdigitated techniques. The output and the ground pads are also shown in the layout.

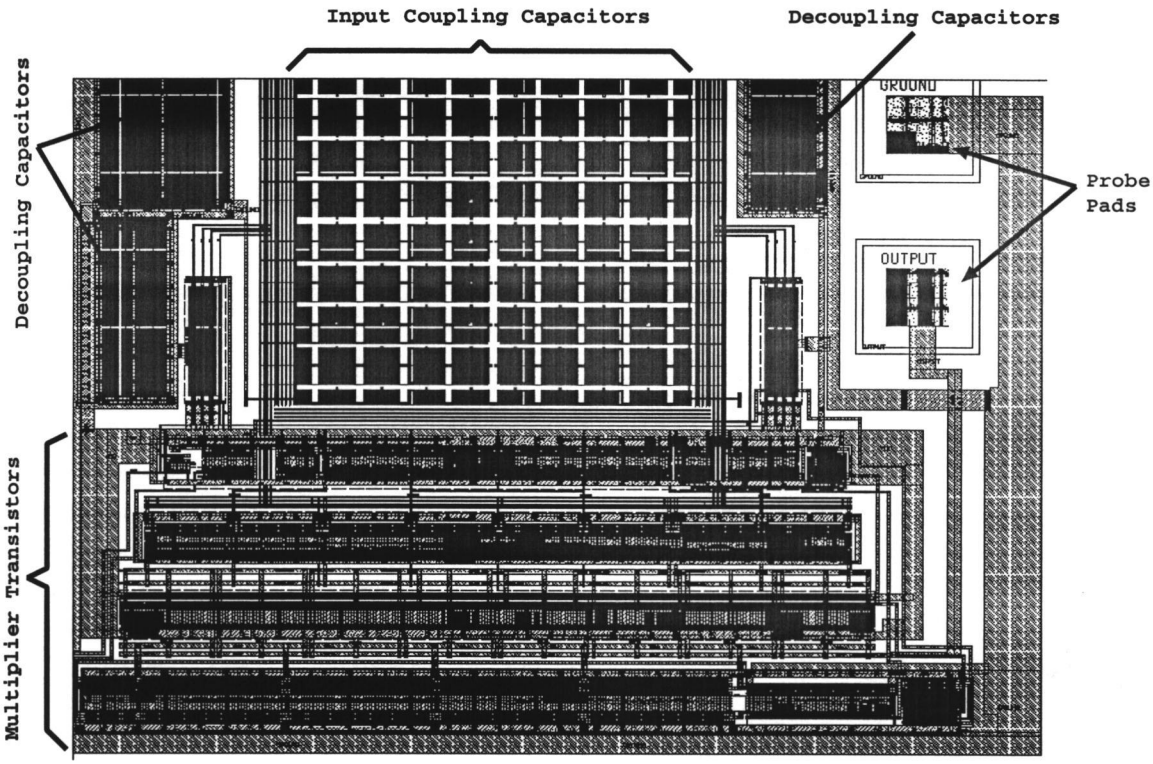


FIGURE 7.6. Layout of the multiplier.

The SONY/Tektronix AWG520 arbitrary waveform generator is used to generate two input signals. Allen Avionics high Q 16-bit bandpass filters are used to filter out the input signal tones. A Cascade Microtech probe station is used to host

the test circuit board. The output signal is obtained using a Cascade Microtech ACP40-W probe. A HP 3585B spectrum analyzer is used to analyze the output signal. This spectrum analyzer has 50 ohm input resistance, which is driven by the current output of the multiplier. A 0.1 μF capacitor is used to isolate the DC signal between the multiplier output and the spectrum analyzer input. The test equipment setup is shown in Fig. 7.7.

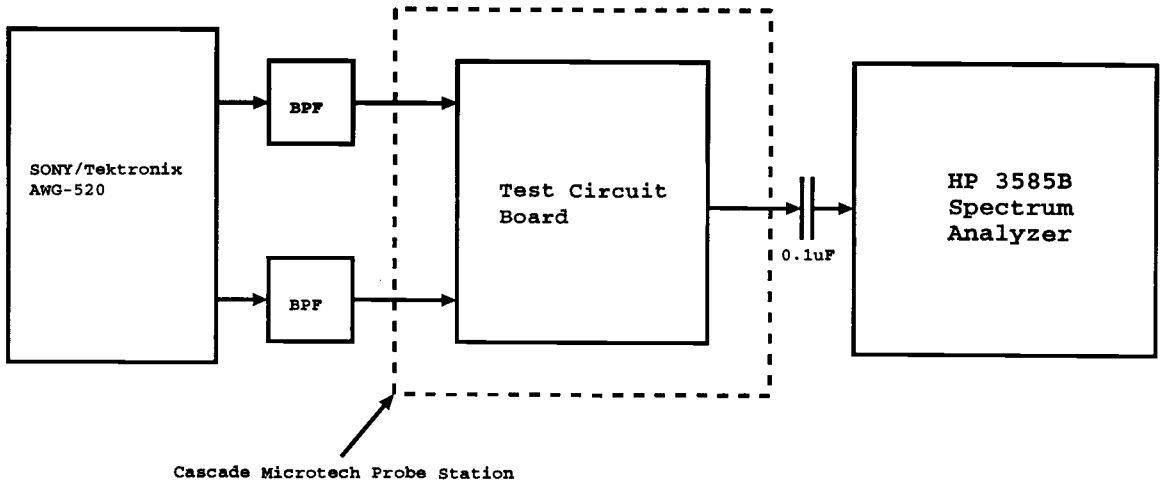


FIGURE 7.7. Test equipment setup of the multiplier.

The test circuit board is powered by two 6-V batteries and the test circuit board is attached to the probe station for probing. The photo of the probe station and the test circuit board is shown in Fig. 7.8.

The HP 3585B spectrum analyzer can analyze frequencies from 20Hz to 40MHz. Thus the maximum frequency that can be used in the measurement is limited by the spectrum analyzer. To measure the down-conversion result, two signals at frequencies of 17MHz and 18MHz are used. The signal is down-converted

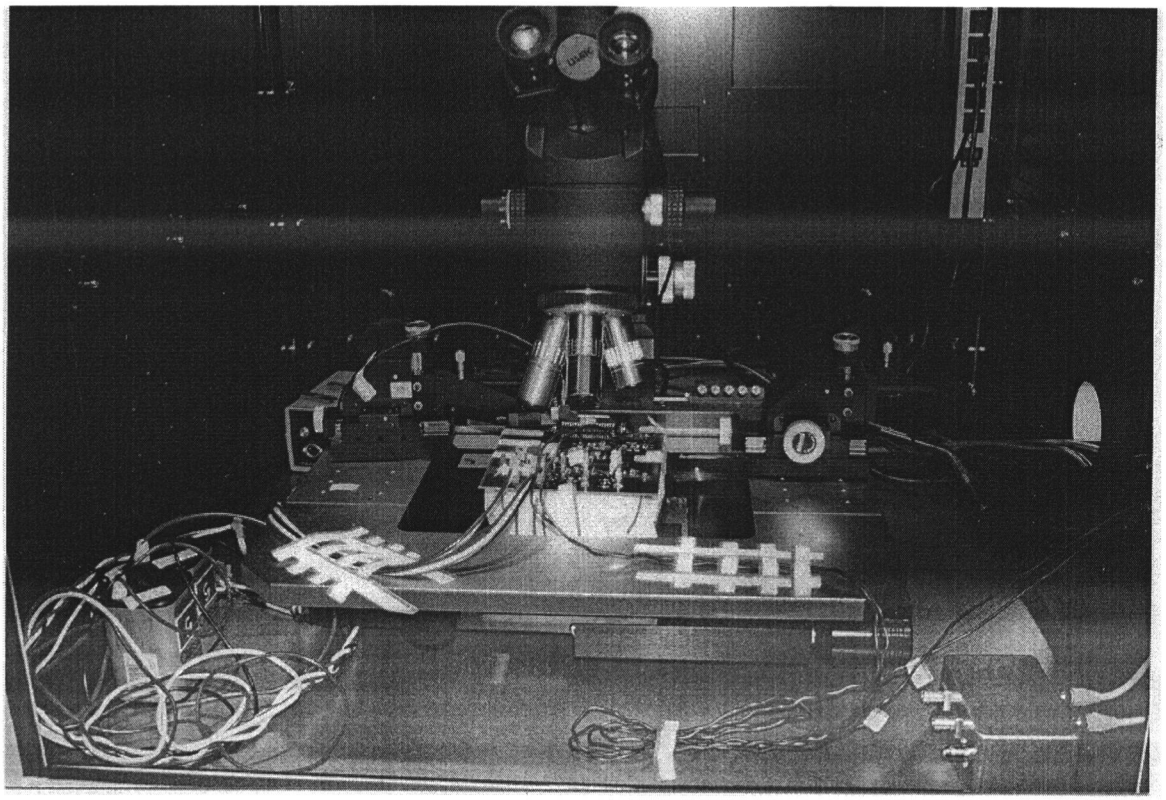


FIGURE 7.8. Photo of the probe station and the test circuit board.

to 1 MHz. The measured spectrum is shown in Fig. 7.9. The third harminic at 3 MHz is -52.5 dB lower than the fundamental frequency amplitude. The second harmonic is much lower than the third harmonic. The total harmonic distortion is about 0.25%. This result is very close to the estimated value and generally is difficult to achieve with conventional Gilbert six transistor cell structures.

The up-conversion is also measured. The two input signals are at 1 MHz and 30 MHz, respectively. Similar to the simulation results, the measured results show large signal feedthrough and the total harmonic distortion is only 2.4%. This is

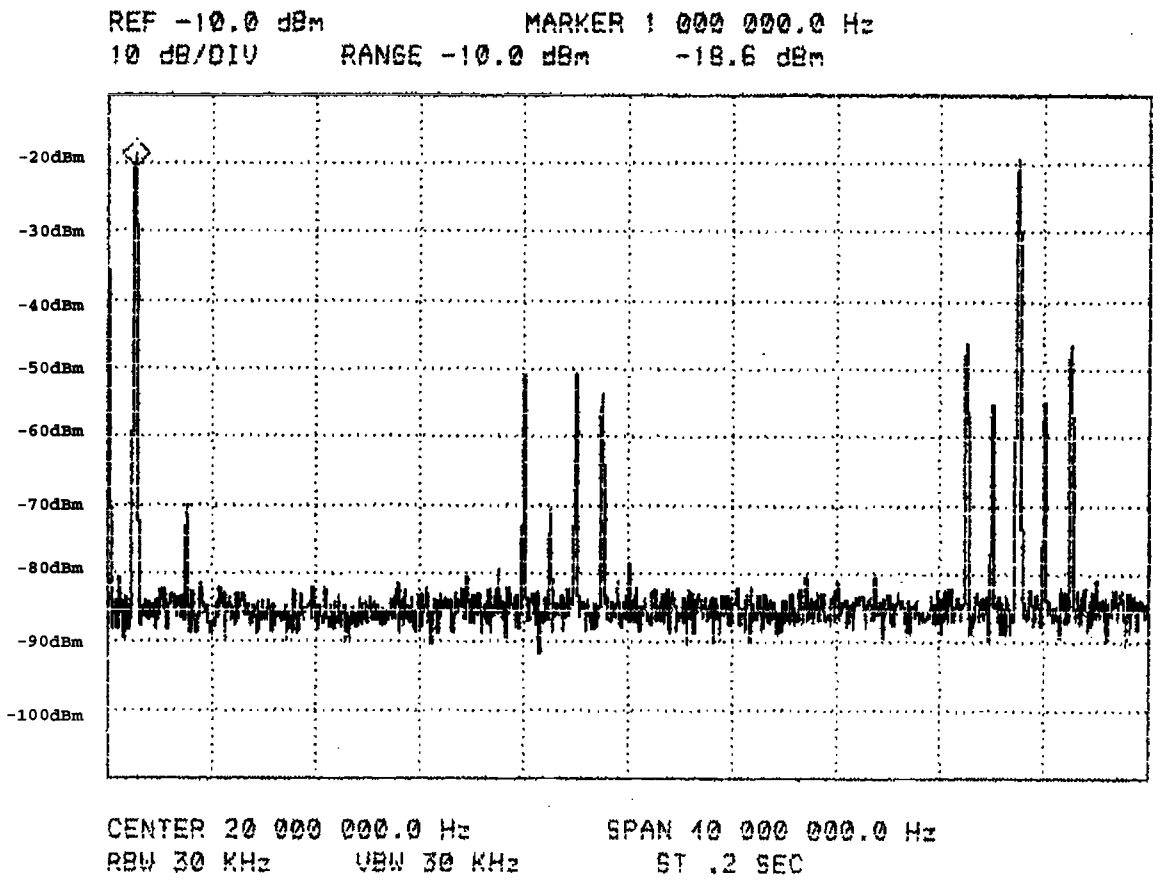


FIGURE 7.9. Measured spectrum of the down conversion with two input signals at 17 MHz and 18 MHZ, respectively.

because this multiplier uses capacitors to couple the input signals and the isolation is poor. Thus the output signal has significant input signal components due to feedthrough. For down-conversions, this is not a problem, because the frequency of the down-converted signal is far away from the input signal frequencies. But for up-conversions, the frequency up-converted signal is very close to the carrier frequency and they can intermodulate with each other and generate more tones. The measured

up conversion spectrum is shown in Fig. 7.10. The carrier frequency is 30 MHz and the input signal frequency is 1 MHz.

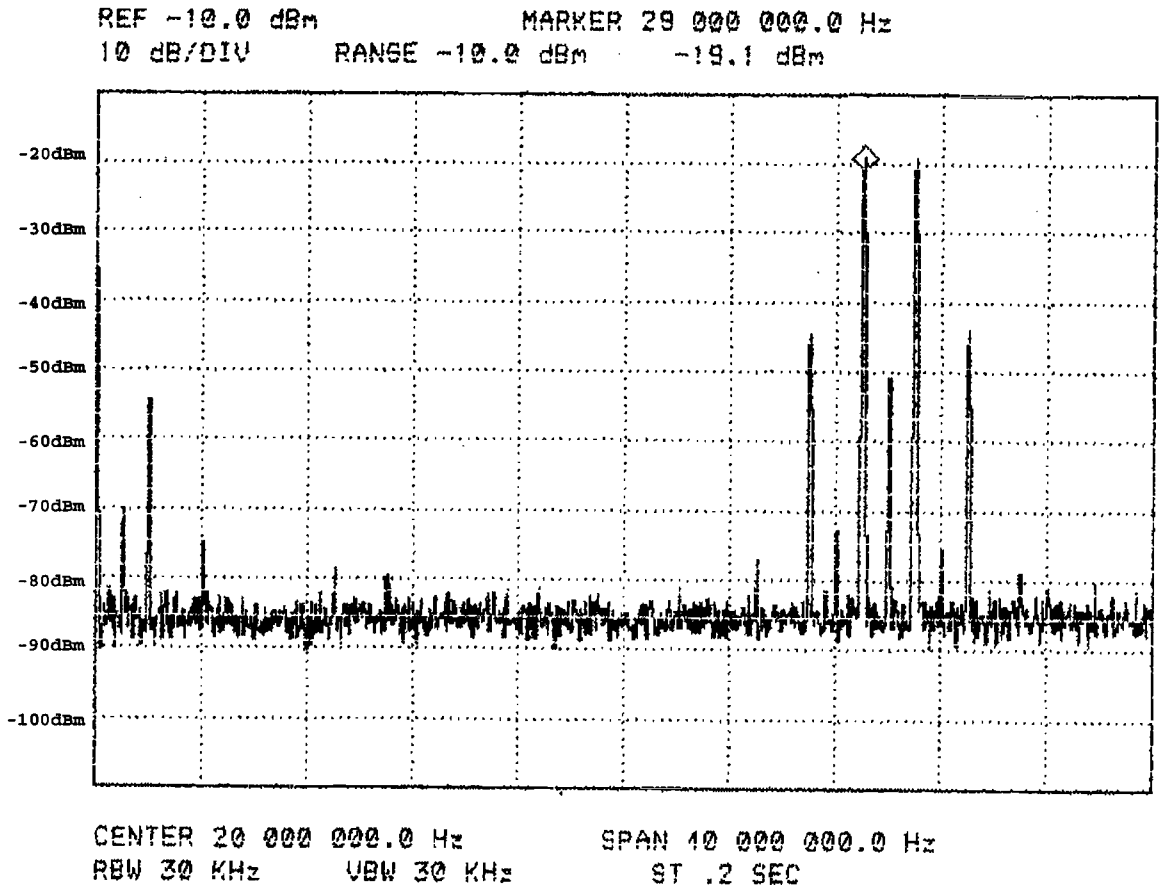


FIGURE 7.10. Measured spectrum of the up conversion with two input signals at 1 MHz and 30 MHZ, repsectively.

On the PCB, Burr-Brown OPA642 opamps are used to convert the single-ended input signals to differential signals. When the signal frequencies are high, the harmonic distortions of the opamps will increase rapidly. Figure 7.11 is the measured spectrum of the down conversion with two input signals at 30 MHz and 36 MHz, respectively. The total harmonic distortion is about -44 dB of which 30%

is from the opamps. The harmonic distortion introduced by the opamps increases rapidly as the input signal frequencies increases. Thus, the measurement is limited by the opamps.

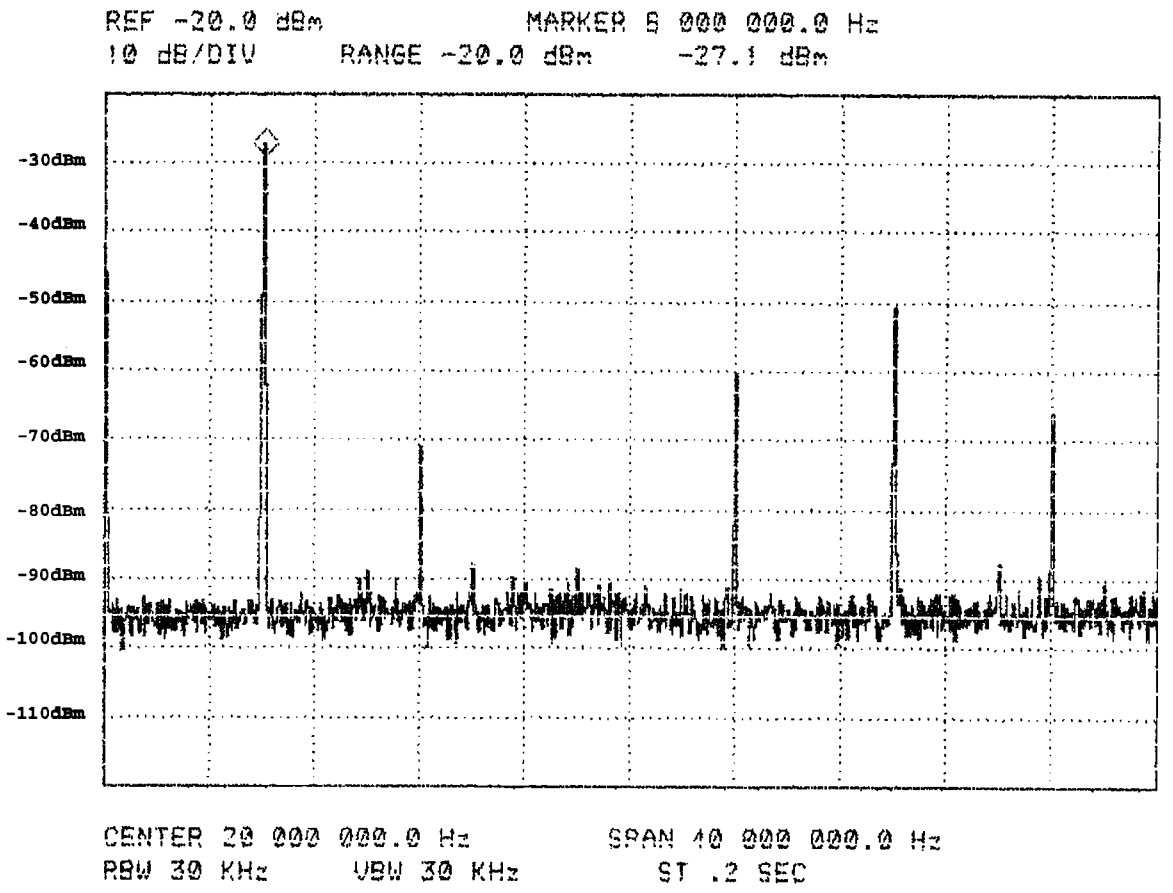


FIGURE 7.11. Measured spectrum of the down conversion with two input signals at 30 MHz and 36 MHZ, repsectively.

The TSMC 0.35 μm 2-poly 3-metal CMOS process is used for this multiplier. The active area including the two probe pads is 2mm X 1.6mm. The specifications of the multiplier are summarized in Table 7.2.

TABLE 7.2. Specifications of the multiplier. For the up conversion, the two input signals are 1MHz and 30MHz, respectively. For the down conversion, the two input signals are 17MHz and 18MHz, respectively.

Specification	Value
THD (Down Conversion)	0.25%
THD (Up Conversion)	2.4%
SFDR (Down Conversion)	-53 dB
SFDR (Up Conversion)	-33 dB
IP3 (Down Conversion)	32.9 dBm
IP3 (Up Conversion)	18.63 dBm
Max. Output Swing	0.2 V_{P-P}
Input Capacitance	5.6 pF
Power Supply	3.3 Volt
Power Dissipation	24 mW
Active Area	2mm X 1.6mm
Process	0.35 um 2-poly 3-metal CMOS

7.6. Conclusion

This multiplier uses the square-law property of MOS transistors. Ideally the output is a pure product of the two input signals. Simulations and measured results show that this multiplier has very low total harmonic distortion for down conversions. This multiplier can be used in dual IF receivers [49] to down-convert signals from high frequency IF to low frequency IF. Measured results show that the total harmonic distortion is as low as 0.25% for down conversion with an IP3 of 32.9 dBm. Thus this multiplier is very suitable for communication applications.

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APPENDICES

APPENDIX A. Mathematica Solutions of the Coefficients of the Fifth-Order Leapfrog $\Delta\Sigma$ Modulator for Different $\|H\|_\infty$

Solving the coefficients of the leapfrog 5th order 4-bit delta-sigma A/D Converter NTFMAX=1.5

```
num1 = (b5);
num2 = (b1 + b2 + b3 + b4);
num3 = (b1 * b5 + b2 * b5 + b3 * b5);
num4 = (b1 * b3 + b1 * b4 + b2 * b4);
num5 = (b1 * b3 * b5);

denom1 = (a1 + b5);
denom2 = (a1 * b5 + a2 + b1 + b2 + b3 + b4);
denom3 = (a1 * (b2 + b3 + b4) + a2 * b5 + a3 + (b1 + b2 + b3) * b5);
denom4 = (a4 + a3 * b5 + a2 * (b3 + b4) + a1 * b5 * (b2 + b3));
denom5 = (a5 + a4 * b5 + a3 * b4 + a2 * b3 * b5 + a1 * b2 * b4 + b1 * b3 * b5);

eqn1 = -5 + num1;
eqn2 = 10 - 4 * num1 + num2;
eqn3 = -10 + 6 * num1 - 3 * num2 + num3;
eqn4 = 5 - 4 * num1 + 3 * num2 - 2 * num3 + num4;
eqn5 = -1 + num1 - num2 + num3 - num4 + num5;

eqd1 = -5 + denom1;
eqd2 = 10 - 4 * denom1 + denom2;
eqd3 = -10 + 6 * denom1 - 3 * denom2 + denom3;
eqd4 = 5 - 4 * denom1 + 3 * denom2 - 2 * denom3 + denom4;
eqd5 = -1 + denom1 - denom2 + denom3 - denom4 + denom5;

Solve[{eqn1 == -4.8301, eqn2 == 9.4960, eqn3 == -9.4960,
        eqn4 == 4.8301, eqn5 == -1, eqd1 == -4.1074, eqd2 == 6.8150,
        eqd3 == -5.7017, eqd4 == 2.4030, eqd5 == -0.4078}, {a1, a2, a3,
        a4, a5, b1, b2, b3, b4, b5}]

{{a5 → 0.00175135, a4 → 0.00525965, a3 → -0.0541897, a2 → 0.0870133,
  b4 → 0.108502, b1 → 0., b2 → 0.0525337, a1 → 0.7227, b3 → 0.0145646, b5 → 0.1699}}
```

Solving the coefficients of the leapforg 5th order 4-bit delta-sigma A/D Converter NTFMAX=6.0

```
In[22]:= num1 = (b5);
         num2 = (b1 + b2 + b3 + b4);
         num3 = (b1 * b5 + b2 * b5 + b3 * b5);
         num4 = (b1 * b3 + b1 * b4 + b2 * b4);
         num5 = (b1 * b3 * b5);

         denom1 = (a1 + b5);
         denom2 = (a1 * b5 + a2 + b1 + b2 + b3 + b4);
         denom3 = (a1 * (b2 + b3 + b4) + a2 * b5 + a3 + (b1 + b2 + b3) * b5);
         denom4 = (a4 + a3 * b5 + a2 * (b3 + b4) + a1 * b5 * (b2 + b3));
         denom5 = (a5 + a4 * b5 + a3 * b4 + a2 * b3 * b5 + a1 * b2 * b4 + b1 * b3 * b5);

         eqn1 = -5 + num1;
         eqn2 = 10 - 4 * num1 + num2;
         eqn3 = -10 + 6 * num1 - 3 * num2 + num3;
         eqn4 = 5 - 4 * num1 + 3 * num2 - 2 * num3 + num4;
         eqn5 = -1 + num1 - num2 + num3 - num4 + num5;

         eqd1 = -5 + denom1;
         eqd2 = 10 - 4 * denom1 + denom2;
         eqd3 = -10 + 6 * denom1 - 3 * denom2 + denom3;
         eqd4 = 5 - 4 * denom1 + 3 * denom2 - 2 * denom3 + denom4;
         eqd5 = -1 + denom1 - denom2 + denom3 - denom4 + denom5;

         Solve[{eqn1 == -4.8301, eqn2 == 9.496, eqn3 == -9.496, eqn4 == 4.8301, eqn5 == -1,
           eqd1 == -1.636, eqd2 == 1.476, eqd3 == -0.7584, eqd4 == 0.2126, eqd5 == -0.02542},
          {a1, a2, a3, a4, a5, b1, b2, b3, b4, b5}]

Out[22]= {{a5 → -0.138268, a4 → 0.588958, a3 → 2.5654, a2 → 4.21372,
           b4 → 0.108502, b1 → 0., b2 → 0.0525337, a1 → 3.1941, b3 → 0.0145646, b5 → 0.1699}}
```

APPENDIX B. Switcap2 Simulation Source Code of the Fifth-Order Hybrid $\Delta\Sigma$ Modulator

```
TITLE: FIFTH-ORDER DELTA-SIGMA A/D CONVERTER WITH HYBRID STRUCTURE

/* Created by:  Ruoxin Jiang
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                Corvallis, OR 97331
                email: jiang@ece.orst.edu
                June 2000 - June 2001

   Vref+ and Vref- are 0.25 and -0.25 respectively.
   This A/D has a 17-level quantizer, one integrator,
   four delay circuits and a gain=3.x circuit.
   A high out-of-band quantization noise gain is used.
   Feedback DAC is implemented by 16 unit capacitors.
   At OSR=8, this A/D has an SNDR of about 83dB.
   It can be used for applications that requires
   1-6MHz and 14-bit resolution. Some examples are
   ADSL and WCDMA. */

  TIMING;
    PERIOD 31.25E-9;
    CLOCK phi1 1 (0 1/2);
    CLOCK phi2 1 (1/2 1);
  END;


/* fully differential amp,
   if you want DC gain of 100,
   let p1=50
*/

  SUBCKT (outp outm inp inm) DIFAMP (p1);
    E1(outp 0 inp inm) p1;
    E2(0 outm inp inm) p1;
  END;


/* 4 switches and a cap */
```

```
  SUBCKT (in1 in2 out1) SWCAP (p1 p2 c1);
    sw1 (in1 4) p1;
    sw2 (4 in2) p2;
    sw3 (5 out1) p2;
    sw4 (5 0) p1;
    csample (4 5) c1;
  END;


/* similar to SWCAP, but have two feedback
   inputs for DAC output signals.
   It is used in the first stage of this design */

  SUBCKT (in1 f1 f2 out1) DACCAP (p1 p2 sel c1);
   yg1 NOT (sel seln);
   yg2 AND (p2 sel selck);
   yg3 AND (p2 seln selckn);
   sw1 (in1 1) p1;
   sw2 (f1 1) selck;
   sw3 (f2 1) selckn;
   sw4 (2 0) p1;
   sw5 (2 out1) p2;
   csample (1 2) c1;
  END;


/* integrator: one opamp with two feedback caps.
   two extra SWCAPs are needed to fufill the
   integrator function */

  SUBCKT (inp inm outp outm) INTEGRATOR (c1 cin gain);
    cap1 (inp outm) c1;
    cap2 (inm outp) c1;
    cin1 (inp 0) cin;
    cin2 (inm 0) cin;
    x1 (outp outm inp inm) DIFAMP (gain);
  END;


/* one clock delay: similar to integrator.  But
   with two SWCAP, previous outputs are cancelled.
   The following stage must sample on "p1" for
```

```
   this circuit to have one clock delay */

  SUBCKT (inp inm outp outm) DELAY1 (p1 p2 c1 c2 cin gain);
    x1 (inp inm outp outm) INTEGRATOR (c1 cin gain);
    xsw1 (outp 0 inp) SWCAP (p1 p2 c2);
    xsw2 (outm 0 inm) SWCAP (p1 p2 c2);
  END;


/* The switched-capacitor used to implement zero-delay */
  SUBCKT (in1 out1) SWZERO (p1 p2 c1);
    sw1 (in1 1) p2;
    sw2 (1 0) p1;
    sw3 (2 out1) p2;
    sw4 (2 0) p1;
    csample (1 2) c1;
  END;


/* Convert logic output to analog output, because sw2
   cannot print logic values directly. sw2 is really bad */
  SUBCKT (in1 out1) LOGICVOLT (vrefp vrefm);
    yg1 NOT (in1 in1m);
    sw1 (vrefp out1) in1;
    sw2 (vrefm out1) in1m;
  END;


/* 17-level A/D  with latched output.
   In sw2, resistors are realized by a switched cap with
   a high frequency clock.  This requires more simulation time.
   In this file, the resistor ladder is realized by a
   capacitor ladder.  It cannot be implemented in reality,
   but is OK and simple for the simulation.
   This A/D has a single-ended input. The 16-bit
   output will directly drive the DAC capacitors */

  SUBCKT (inp vrefp vrefm) adc17 (clk out1 out2 out3 out4
    out5 out6 out7 out8 out9 out10 out11 out12 out13 out14
    out15 out16 out1m out2m out3m out4m out5m out6m out7m
    out8m out9m out10m out11m out12m out13m out14m out15m
    out16m);
```

```
c1 (vrefp 1) 2; /* represents 0.5*R */
c2 (1 2) 1; /* represents R */
c3 (2 3) 1;
c4 (3 4) 1;
c5 (4 5) 1;
c6 (5 6) 1;
c7 (6 7) 1;
c8 (7 8) 1;
c9 (8 9) 1;
c10 (9 10) 1;
c11 (10 11) 1;
c12 (11 12) 1;
c13 (12 13) 1;
c14 (13 14) 1;
c15 (14 15) 1;
c16 (15 16) 1;
c17 (16 vrefm) 2;

ycmp1 cmplat (inp 16 clk out1);
ycmp2 cmplat (inp 15 clk out2);
ycmp3 cmplat (inp 14 clk out3);
ycmp4 cmplat (inp 13 clk out4);
ycmp5 cmplat (inp 12 clk out5);
ycmp6 cmplat (inp 11 clk out6);
ycmp7 cmplat (inp 10 clk out7);
ycmp8 cmplat (inp 9 clk out8);
ycmp9 cmplat (inp 8 clk out9);
ycmp10 cmplat (inp 7 clk out10);
ycmp11 cmplat (inp 6 clk out11);
ycmp12 cmplat (inp 5 clk out12);
ycmp13 cmplat (inp 4 clk out13);
ycmp14 cmplat (inp 3 clk out14);
ycmp15 cmplat (inp 2 clk out15);
ycmp16 cmplat (inp 1 clk out16);

yg1 NOT (out1 out1m);
yg2 NOT (out2 out2m);
yg3 NOT (out3 out3m);
yg4 NOT (out4 out4m);
yg5 NOT (out5 out5m);
yg6 NOT (out6 out6m);
yg7 NOT (out7 out7m);
```

```
      yg8 NOT (out8 out8m);
      yg9 NOT (out9 out9m);
      yg10 NOT (out10 out10m);
      yg11 NOT (out11 out11m);
      yg12 NOT (out12 out12m);
      yg13 NOT (out13 out13m);
      yg14 NOT (out14 out14m);
      yg15 NOT (out15 out15m);
      yg16 NOT (out16 out16m);
  END;


  CIRCUIT;
    vrefp (90 0);
    vrefm (91 0);
    vinp (1 1000);
    vinm (2 1001);

/* voffp and voffn are the input referred offset
   voltages.  If we assume the opamps have no
   DC offset, KT/C noise or opamp input
   referred noise (which is impossible),
   the modulator will have approximately 3 LSB
   dead zone centered at zero input.
   Simulations show that offset voltages and
   KT/C noise are enough to eliminate the dead zone.
   They also help to reduce tones in baseband when
   the input signal is very small */

    voffp (1000 0);
    voffm (1001 0);

/* The 17-level A/D */
    xadc (33 90 91) adc17 (phi2 out1 out2 out3 out4 out5 out6
      out7 out8 out9 out10 out11 out12 out13 out14 out15 out16
      out1m out2m out3m out4m out5m out6m out7m out8m out9m
      out10m out11m out12m out13m out14m out15m out16m);

/* Convert the logic outputs of the comparators for printing */
    xb1 (out1 volt1) LOGICVOLT (90 91);
    xb2 (out2 volt2) LOGICVOLT (90 91);
    xb3 (out3 volt3) LOGICVOLT (90 91);
```

```
    xb4 (out4 volt4) LOGICVOLT (90 91);
    xb5 (out5 volt5) LOGICVOLT (90 91);
    xb6 (out6 volt6) LOGICVOLT (90 91);
    xb7 (out7 volt7) LOGICVOLT (90 91);
    xb8 (out8 volt8) LOGICVOLT (90 91);
    xb9 (out9 volt9) LOGICVOLT (90 91);
    xb10 (out10 volt10) LOGICVOLT (90 91);
    xb11 (out11 volt11) LOGICVOLT (90 91);
    xb12 (out12 volt12) LOGICVOLT (90 91);
    xb13 (out13 volt13) LOGICVOLT (90 91);
    xb14 (out14 volt14) LOGICVOLT (90 91);
    xb15 (out15 volt15) LOGICVOLT (90 91);
    xb16 (out16 volt16) LOGICVOLT (90 91);

/* The first stage integrator and DAC capacitors */
    xint1 (6 7 9 8) INTEGRATOR (5.0E-12 1.0E-12 70);
    xdacp1 (1 90 91 6) DACCAP (phi1 phi2 out1 0.3125E-12);
    xdacp2 (1 90 91 6) DACCAP (phi1 phi2 out2 0.3125E-12);
    xdacp3 (1 90 91 6) DACCAP (phi1 phi2 out3 0.3125E-12);
    xdacp4 (1 90 91 6) DACCAP (phi1 phi2 out4 0.3125E-12);
    xdacp5 (1 90 91 6) DACCAP (phi1 phi2 out5 0.3125E-12);
    xdacp6 (1 90 91 6) DACCAP (phi1 phi2 out6 0.3125E-12);
    xdacp7 (1 90 91 6) DACCAP (phi1 phi2 out7 0.3125E-12);
    xdacp8 (1 90 91 6) DACCAP (phi1 phi2 out8 0.3125E-12);
    xdacp9 (0 90 91 6) DACCAP (phi1 phi2 out9 0.3125E-12);
    xdacp10 (0 90 91 6) DACCAP (phi1 phi2 out10 0.3125E-12);
    xdacp11 (0 90 91 6) DACCAP (phi1 phi2 out11 0.3125E-12);
    xdacp12 (0 90 91 6) DACCAP (phi1 phi2 out12 0.3125E-12);
    xdacp13 (0 90 91 6) DACCAP (phi1 phi2 out13 0.3125E-12);
    xdacp14 (0 90 91 6) DACCAP (phi1 phi2 out14 0.3125E-12);
    xdacp15 (0 90 91 6) DACCAP (phi1 phi2 out15 0.3125E-12);
    xdacp16 (0 90 91 6) DACCAP (phi1 phi2 out16 0.3125E-12);
    xdacm1 (2 90 91 7) DACCAP (phi1 phi2 out1m 0.3125E-12);
    xdacm2 (2 90 91 7) DACCAP (phi1 phi2 out2m 0.3125E-12);
    xdacm3 (2 90 91 7) DACCAP (phi1 phi2 out3m 0.3125E-12);
    xdacm4 (2 90 91 7) DACCAP (phi1 phi2 out4m 0.3125E-12);
    xdacm5 (2 90 91 7) DACCAP (phi1 phi2 out5m 0.3125E-12);
    xdacm6 (2 90 91 7) DACCAP (phi1 phi2 out6m 0.3125E-12);
    xdacm7 (2 90 91 7) DACCAP (phi1 phi2 out7m 0.3125E-12);
    xdacm8 (2 90 91 7) DACCAP (phi1 phi2 out8m 0.3125E-12);
    xdacm9 (0 90 91 7) DACCAP (phi1 phi2 out9m 0.3125E-12);
    xdacm10 (0 90 91 7) DACCAP (phi1 phi2 out10m 0.3125E-12);
```

```
    xdacm11 (0 90 91 7) DACCAP (phi1 phi2 out11m 0.3125E-12);
    xdacm12 (0 90 91 7) DACCAP (phi1 phi2 out12m 0.3125E-12);
    xdacm13 (0 90 91 7) DACCAP (phi1 phi2 out13m 0.3125E-12);
    xdacm14 (0 90 91 7) DACCAP (phi1 phi2 out14m 0.3125E-12);
    xdacm15 (0 90 91 7) DACCAP (phi1 phi2 out15m 0.3125E-12);
    xdacm16 (0 90 91 7) DACCAP (phi1 phi2 out16m 0.3125E-12);

/* The second-order transpose block 1 */
    xd2 (10 11 13 12) DELAY1 (phi1 phi2 1.0E-12 1.0E-12 0.5E-12 80);

/* I merged the delay cap to increase speed.  Thus c2=1.0e-19,
   which means c2 is set to zero */
    xd3 (14 15 17 16) DELAY1 (phi1 phi2 1.0E-12 1.0E-19 0.5E-12 80);

    xswd21 (16 0 11) SWCAP (phi1 phi2 1.0E-12);
    xswd22 (8 0 11) SWCAP (phi1 phi2 0.25E-12);
    xswd23 (9 0 10) SWCAP (phi1 phi2 0.25E-12);
    xswd24 (17 0 10) SWCAP (phi1 phi2 1.0E-12);

/* Originally was 32/17, merged with delay cap, -> 15/17 */
    xswd31 (16 0 14) SWCAP (phi1 phi2 0.882353E-12); /* 15/17 */

    xswd32 (8 0 14) SWCAP(phi1 phi2 0.5882353E-12); /* 10/17 */
    xswd33 (12 0 14) SWCAP (phi1 phi2 1.0E-12);
    xswd34 (13 0 15) SWCAP (phi1 phi2 1.0E-12);
    xswd35 (9 0 15) SWCAP (phi1 phi2 0.5882353E-12);
    xswd36 (17 0 15) SWCAP (phi1 phi2 0.882353E-12);

/* The second-order transpose block 2 */
    xd4 (18 19 21 20) DELAY1 (phi1 phi2 1.0E-12 1.0E-12 0.5E-12 80);

/* merged with delay cap, c2=1.0E-19 , same as xd3 above */
    xd5 (22 23 25 24) DELAY1 (phi1 phi2 1.0E-12 1.0E-19 0.5E-12 80);

    xsw41 (8 0 19) SWCAP (phi1 phi2 0.60E-12);
    xsw42 (24 0 19) SWCAP (phi1 phi2 1.0E-12);
    xsw43 (16 0 19) SWCAP (phi1 phi2 0.60E-12);
    xsw44 (17 0 18) SWCAP (phi1 phi2 0.60E-12);
    xsw45 (25 0 18) SWCAP (phi1 phi2 1.0E-12);
    xsw46 (9 0 18) SWCAP (phi1 phi2 0.60E-12);
    xsw51 (8 0 22) SWCAP (phi1 phi2 0.727272E-12); /* 16/22 */
    xsw52 (24 0 22) SWCAP (phi1 phi2 0.954545E-12); /* 21/22 */
```

```
    xsw53 (16 0 22) SWCAP (phi1 phi2 0.727272E-12);
    xsw54 (20 0 22) SWCAP (phi1 phi2 1.0E-12);
    xsw55 (21 0 23) SWCAP (phi1 phi2 1.0E-12);
    xsw56 (17 0 23) SWCAP (phi1 phi2 0.727272E-12);
    xsw57 (25 0 23) SWCAP (phi1 phi2 0.954545E-12);
    xsw58 (9 0 23) SWCAP (phi1 phi2 0.727272E-12);

/* The gain stage before the 17-level A/D */
/* Two OPAMPs are used. One sums three inputs. One amplifies by 3.x */
/* SNDR=82.5dB.  Less than one 'g' stage */
    xg1 (26 27 29 28) DELAY1 (phi1 phi2 1.0E-12 1.0E-12 0.57E-12 80);
    xswg1 (8 26) SWZERO (phi1 phi2 1.0E-12);
    xswg2 (16 26) SWZERO (phi1 phi2 1.0E-12);
    xswg3 (24 26) SWZERO (phi1 phi2 1.0E-12);
    xswg4 (25 27) SWZERO (phi1 phi2 1.0E-12);
    xswg5 (17 27) SWZERO (phi1 phi2 1.0E-12);
    xswg6 (9 27) SWZERO (phi1 phi2 1.0E-12);

    xg2 (30 31 32 33) DELAY1 (phi1 phi2 1.0E-12 1.0E-12 0.83E-12 80);
    xswg7 (28 30) SWZERO (phi1 phi2 3.5E-12);
    xswg8 (29 31) SWZERO (phi1 phi2 3.5E-12);

  END;


/* Due to the use of comparators, only time-domain simulation
   can be run.  Frequency domain simulation is not allowed. */

  ANALYZE NTRAN;
    TIME 0+ 16484 1;
    INIT L(out1)=1 L(out2)=1 L(out3)=1 L(out4)=1 L(out5)=1
         L(out6)=1 L(out7)=1 L(out8)=1 L(out9)=0 L(out10)=0
         L(out11)=0 L(out12)=0 L(out13)=0 L(out14)=0 L(out15)=0
         L(out16)=0;
    SET vrefp DC +0.25;
    SET vrefm DC -0.25;
    SET vinp COSINE 0.0 +0.18 250000 0 0 3.8;
    SET vinm COSINE 0.0 -0.18 250000 0 0 3.8;
    SET voffp DC 2.0e-5;
    SET voffm DC -2.0e-5;

/* The cmd below is used to watch the output histograms of all OPAMPs */
```

```
/*    PRINT v(8,9) v(16,17) v(24,25) v(33,32);  */

/* The cmd below is used to get the DAC output
   You need to sum the 16 outputs below to get the
   quantizer output */

      PRINT v(volt1) v(volt2) v(volt3) v(volt4) v(volt5) v(volt6)
      v(volt7) v(volt8) v(volt9) v(volt10) v(volt11) v(volt12)
      v(volt13) v(volt14) v(volt15) v(volt16);
  END;

END;
```

APPENDIX C. Schematic of the Front-End Opamp and the Comparator Core

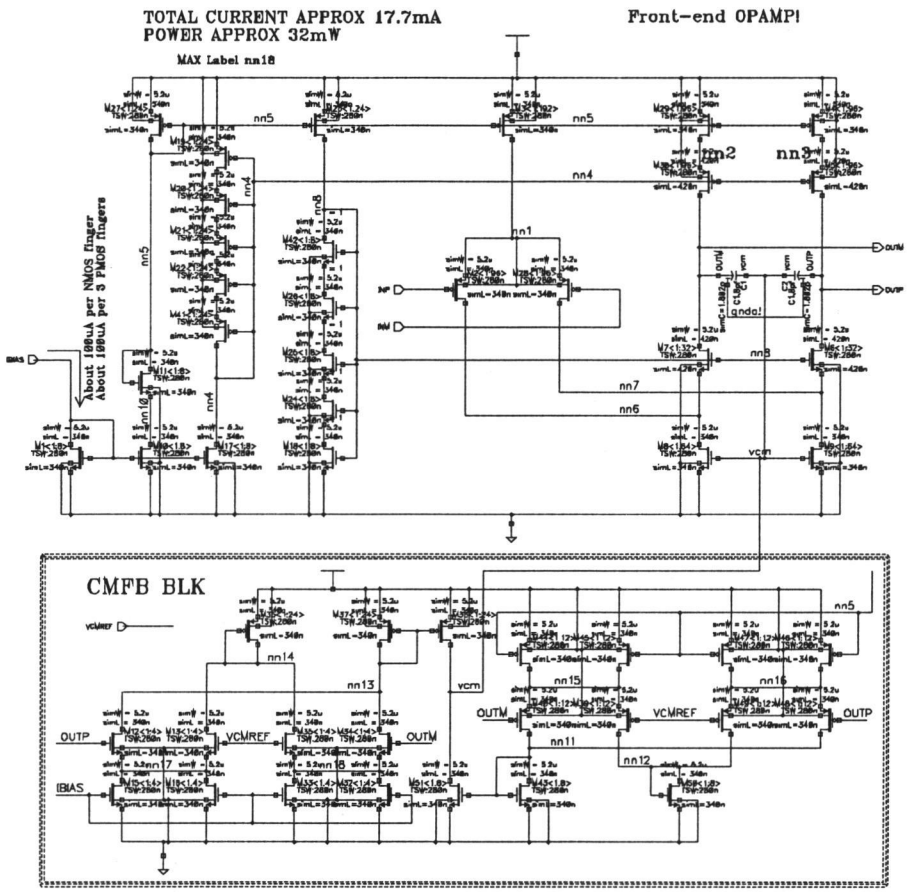

FIGURE C.1. Schematic of the front-end opamp.

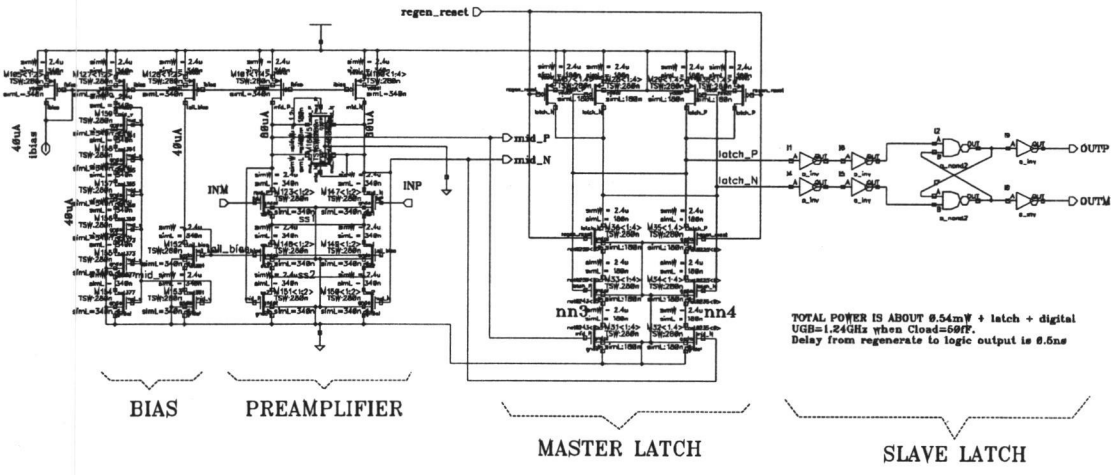

FIGURE C.2. Schematic of the comparator core.

APPENDIX D. Schematic of the Printed Circuit Board for the Hybrid $\Delta\Sigma$ A/D Testing

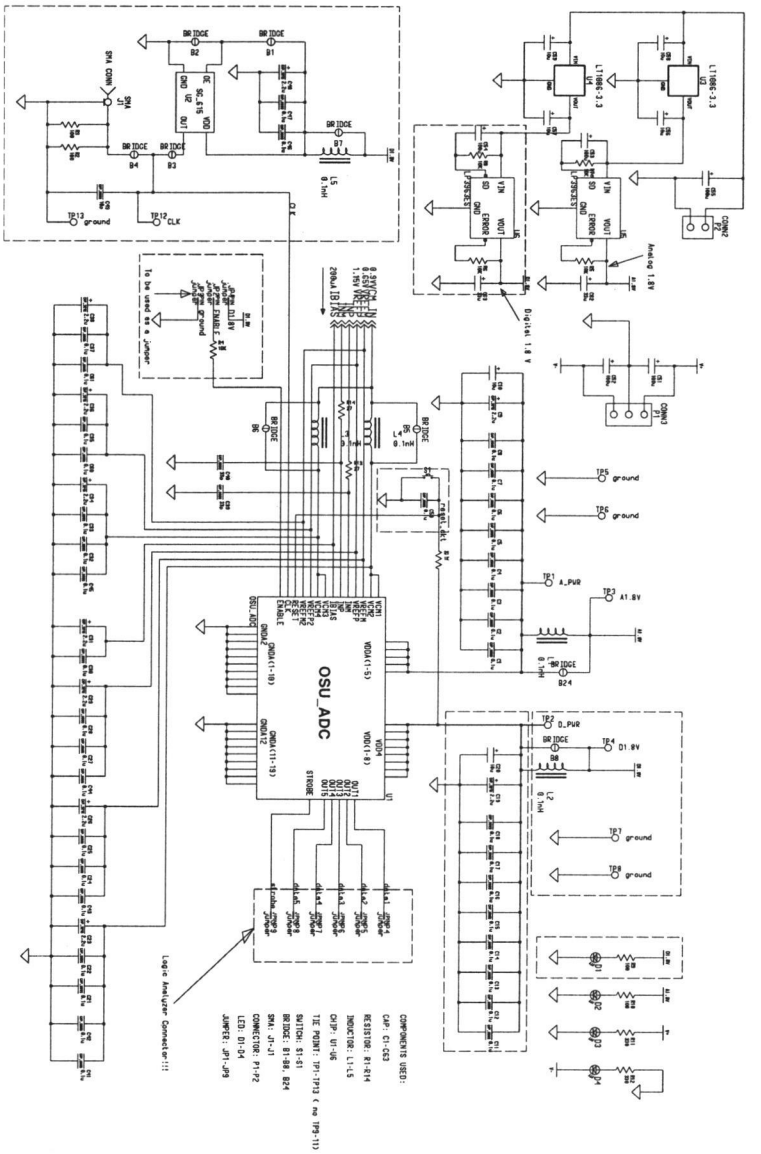

FIGURE D.1. Main schematic of the PCB.

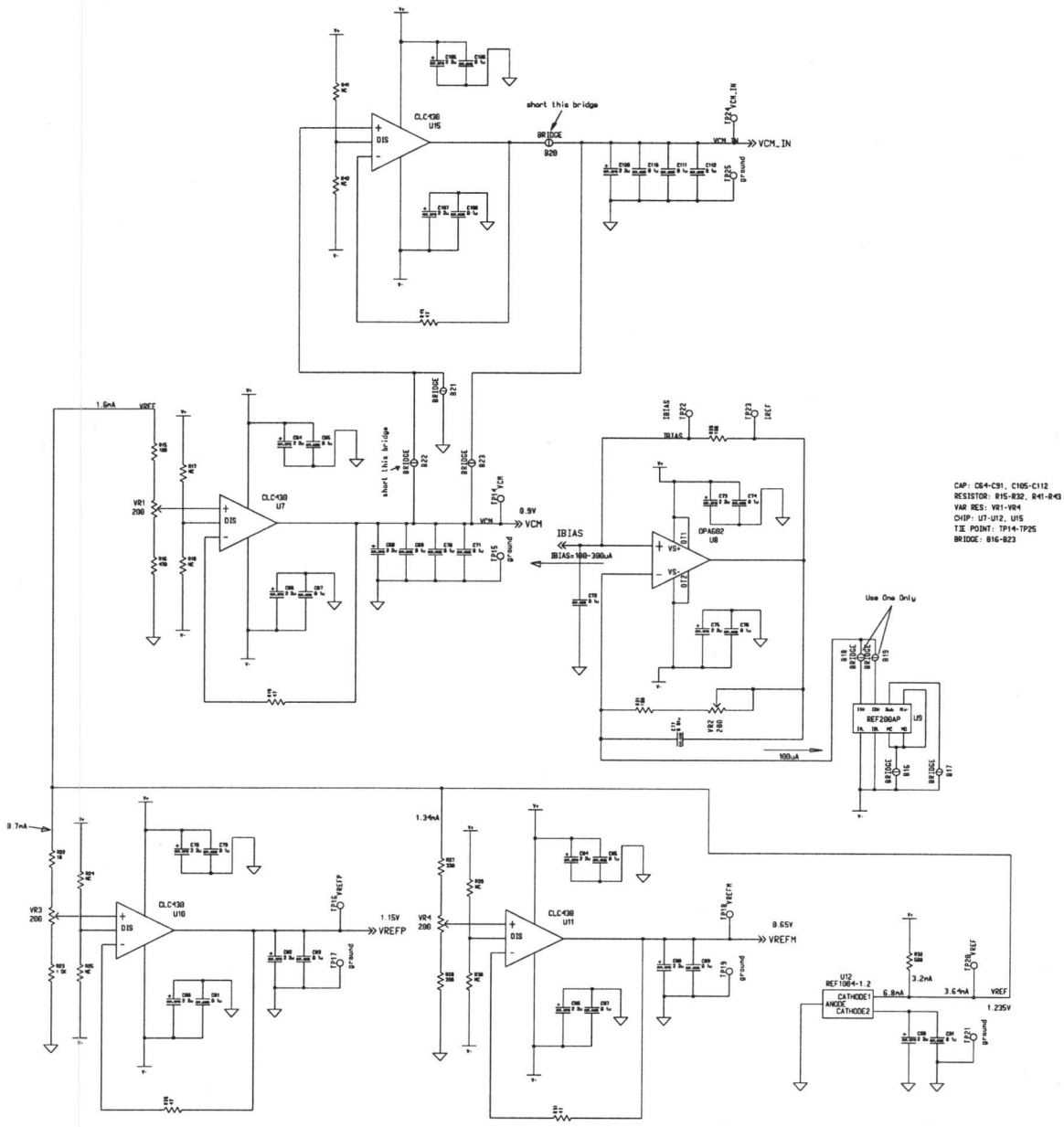

FIGURE D.2. Biasing and reference circuits of the PCB.

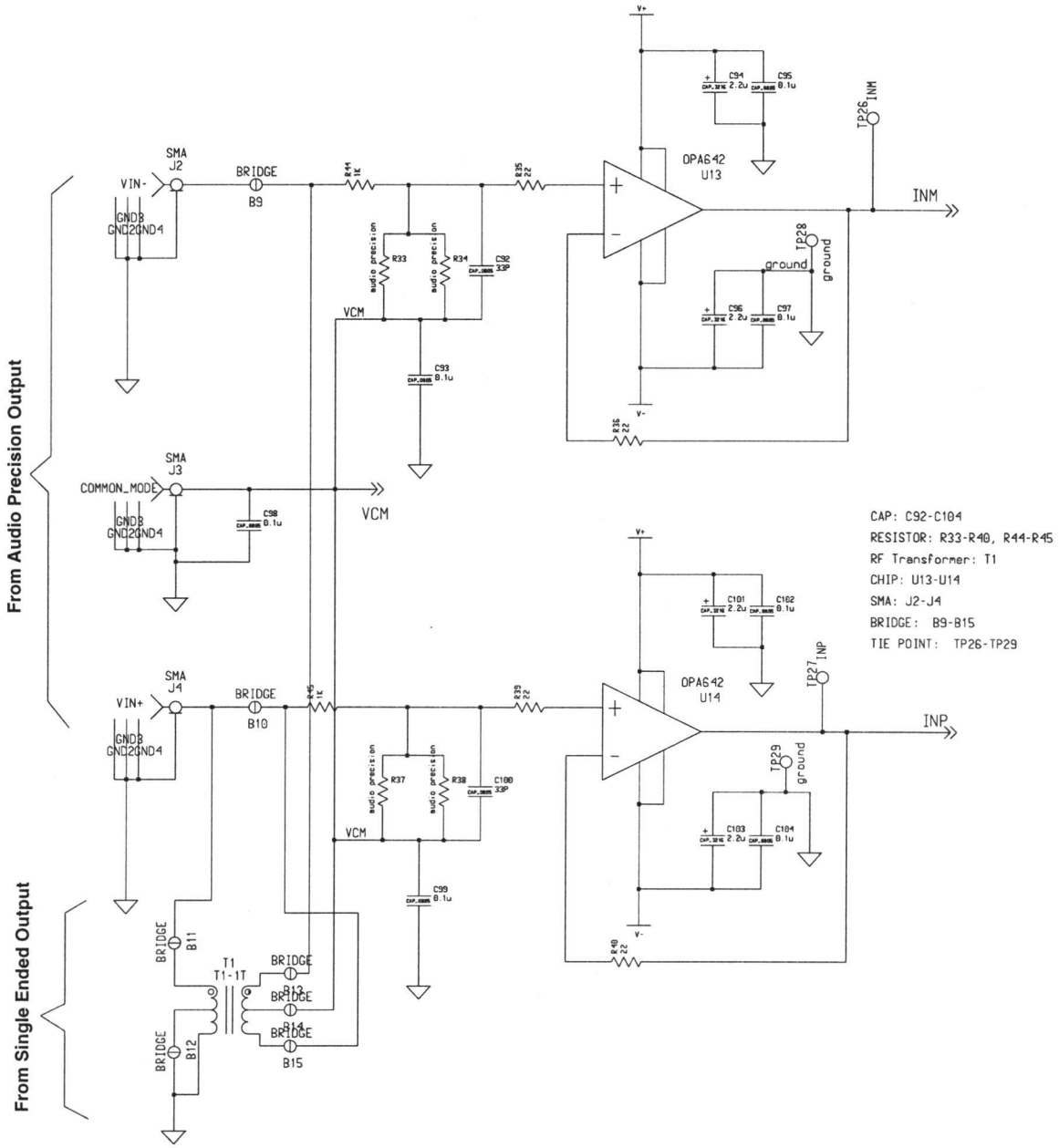

FIGURE D.3. Input amplifiers of the PCB.