AN ABSTRACT OF THE THESIS OF

John Jian Yang for the degree of Master of Science in Electrical and Computer engineering presented on February 2, 1988. Title: A High-Swing CMOS Operational Amplifier Topology.

Abstract approved: Redacted for privacy

David J. Allstot

A circuit topology for high-swing, high-linearity CMOS operational amplifiers has been developed. The technique uses parallel-connected p- and n-channel input pairs to realize an input common-mode voltage range nearly equal to the total power supply voltage. High linearity is achieved by summing the DC bias and AC small-signal currents so that the small voltage gain is, to a first order, constant over the full common-mode voltage range. The technique has been applied to two-stage and cascode CMOS operational amplifiers.

A HIGH-SWING CMOS OPERATIONAL AMPLIFIER TOPOLOGY

By

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A THESIS

Submitted to

Oregon State University

in partial fulfillment of

the requirements for the

degree of

Master of Science

Completed February 2, 1988

Commencement June 1988

APPROVED:

Redacted for privacy

Professor of Electrical & Computer Engineering
in charge of major

Redacted for privacy

Head of Department of Electrical & Computer Engineering

Redacted for privacy

Dean of Graduate School

Date thesis is presented February 2, 1988

Typed by John J. Yang for John Jian Yang

To:

the people who helped and encouraged me.

ACKNOWLEDGEMENT

I would like to express my deep appreciation to Dr. David J. Allstot, my major professor, for his help, patience, advice, and continued encouragement. I am grateful to Prof. V.K. Thipathi, Prof. D.L. Amort, and Prof. A.H. Love for serving on my graduate committee.

Thanks to all my fellow students for their friendship, support, and shared experiences that surfaced in so many ways. A special thanks to Ms. Elaine Almgren for her help in reading the manuscript of this thesis. Magnavox Government and Industrial Electronics Company provided partial support for this project.

I would like to take this opportunity to express my hearty thanks to Prof. Chen Yuen and his family for their help and encouragement since I came to the United States.

Sincere thanks are due to my aunt and uncle, Mr. & Mrs. Laurence Moh. The support, understanding, and encouragement from them are gratefully appreciated.

Last, but not least, the most important goes to my parents. Throughout my life, no matter what I attempted to undertake, they each been there to offer their love and support. To them I can only say thank you and I love you.

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I. INTRODUCTION

Since the mid 1970's, Metal Oxide Semiconductor (MOS) technology has been widely used in Very Large Scale Integrated (VLSI) design. Because of its advantages such as low power dissipation, high packing density, and low cost, CMOS has in fact become the dominant VLSI technology. With the increase in chip complexity has come a strong requirement for the complete integration of analog-digital subsystems on the same chip. Therefore, the implementation of analog functions in CMOS technology has become increasingly necessary, and combined analog and digital CMOS designs are now a major area of interest.

The development of CMOS analog circuit designs is usually constrained by the fabrication technology used for digital CMOS applications. This often means that the available MOSFET devices are not optimum for analog applications. Furthermore, CMOS VLSI technology is not

only being scaled down to ever-smaller feature sizes, it is also being operated with reduced power supply voltages. In terms of available dynamic range, analog CMOS designs suffer more from scaling than do digital CMOS designs [3],[10]. The reduced supply voltage range without reduced device threshold voltages eliminates the use of many proven analog circuit configurations. Therefore, new topologies must be developed that operate over a much higher percentage of the total available power supply voltage range.

As it is a key element of many integrated analog subsystems, an operational amplifier topology has been developed using a scaled CMOS technology. The purpose of this thesis is to investigate this new topology for high-swing, high-linearity, power efficient CMOS operational amplifiers.

II. BASIC PRINCIPLES OF MOS OPERATIONAL AMPLIFIER DESIGN

1. General Performances of an MOS Operational Amplifier

P.R. Gray and R.G. Meyer stated in their tutorial paper that the most important difference between MOS and traditional stand-alone bipolar operational amplifiers is their application [1]. Most MOS amplifiers are used in monolithic analog subsystems having well-defined load impedances which are often purely capacitive. Several of the most important performance parameters for MOS operational amplifiers are [4]:

(1) Power dissipation;

(2) Maximum allowable capacitive load;

(3) Open-loop low-frequency voltage gain;

(4) Output voltage swing;

(5) Equivalent input noise spectral density;

(6) Power Supply Rejection Ratio (PSRR);

(7) Die area for integration;

(8) Unity-gain bandwidth;

(9) Closed-loop gain and phase margins;

(10) Input common mode range;

(11) Common-Mode Rejection Ratio (CMRR);

(12) Input-referred DC offset voltage.

In this thesis, the discussion will focus on the output voltage swing and common-mode input range. These parameters are significantly impacted by CMOS technology and power-supply scaling.

For the commonly-used unity-gain buffer amplifier shown in Fig. 1, input common-mode range and output swing are important parameters. In order to handle large signal amplitudes without gross distortion, the input signal amplitude must be smaller than the minimum of either the common-mode input range of the amplifier, or the output swing. From the amplifier dc transfer characteristic shown in Fig. 2, the limitations of input common-mode range and output swing give important information on the small-signal gain calculation and on the distortion performance of the stages [6].

Consider the circuit of Fig. 3(a). For all devices designed to operate in the saturation region, the large-signal common-mode transfer characteristic is derived. First, the input pair stage is split into a common-mode half circuit as in Fig. 3(b). Assuming $|V_{T3}|=V_{T1}$, the maximum and minimum common-mode input voltage V_{ic} are determined as

$$V_{ic}^{+} = V_{DD} - V_{DS(SAT)3} \tag{1}$$

$$\begin{aligned} V_{ic}^{-} &= V_{SS} + V_{GS1} + V_{DS(SAT)5} \\ &= V_{SS} + (V_{T1} + V_{DS(SAT)1} + V_{DS(SAT)5}). \end{aligned} \tag{2}$$

$$V_{DS(SAT)} = V_{GS} - V_{T} \tag{3}$$

where V_T is the threshold voltage, $V_{DS(SAT)}$ is drain-source saturation voltage, and V_{GS} is gate-source voltage. If by design $V_{DS(SAT)1}=V_{DS(SAT)3}=V_{DS(SAT)5}=V_{DS(SAT)}$, and $V_{T1}=V_T$, then the input common-mode range extends from $V_{DD}-V_{DS(SAT)}$ to $V_{SS}+V_T+2*V_{DS(SAT)}$. The useful peak range about zero volts is therefore about $\pm(V_{DD}-2*V_{DS(SAT)}-V_T)$, assuming $V_{DD}=|V_{SS}|$.

Next, consider that the output swing of the circuit of Fig. 3(a) is limited by the output stage as shown in Fig. 3(c). The maximum and minimum output voltages are derived as

$$V_{out}^{+} = V_{dd} - V_{DS(SAT)6} \tag{4}$$

$$V_{out}^{-} = V_{ss} + V_{DS(SAT)8} \tag{5}$$

Therefore, the output swing is in the range of V_{dd}-$V_{DS(SAT)6}$ to V_{ss}+$V_{DS(SAT)8}$. For a conventional CMOS operational amplifier, the common-mode input range is less than the output voltage swing [6].

Another widely used CMOS operational amplifier configuration using p-channel input devices has the same limitation, but in the opposite direction as shown in Fig. 4. It has a linear common-mode input range extending from V_{SS}+$V_{DS(SAT)}$ to V_{DD}-(V_T+2*$V_{DS(SAT)}$).

2. Impact of Scaled CMOS Technology

CMOS VLSI technology scaling seriously impacts CMOS analog performance [10]. As the total power supply

voltage range scales down from 10 volts to 5 volts, and even to 3.3 volts in future, the dynamic range is also reduced because of the fixed threshold voltages of the MOSFETs based on digital noise margin considerations. For practical considerations, the typical enhancement-mode threshold voltages are ± 0.75 volts for the NMOS and PMOS devices, respectively. For the circuit of Fig 3(a), and assume that the saturation voltage, $V_{DS(SAT)}=0.25$ volts, is chosen for all devices, and that the power supply is 10 volts, the efficiency of the voltage swing (linear range) over the total power supply voltage is 75% from Eq. 2. If the total power supply voltage is reduced to 5 volts, the efficiency decreases to 50%. If it is further shrunk to 3.3 volts in the future, the efficiency will drop to only 24%. Thus, we must consider how to design the analog circuits to operate over a much higher percentage of total power supply voltage in order to maintain a given output voltage level. Y.P. Tsividis stated in a recent paper, "Much more (MOS analog circuits) must be achieved by future design cleverness, especially in the face of shrinking power supply voltages and fabrication processes driven by the digital technology" [5].

3. Basic MOS Model Parameters

In analog circuits, the transistors are designed to operate in the saturation region. For an MOS transistor, we express the drain current in the saturation region as:

$$I_{DS}=\frac{\mu C_{OX}}{2} * \frac{W}{L} * (V_{GS} - V_T)^2 * (1 + \lambda V_{DS}); \quad (6)$$

$$V_T = V_{T0} + \gamma * [(V_{SUB} + 2 \phi_F)^{\frac{1}{2}} - (2 \phi_F)^{\frac{1}{2}}] \quad (7)$$

where

μ ---- the mobility of the carriers in the channel region;

C_{OX} --- the gate oxide capacitance per unit area;

KP ---- the transconductance parameter;

(in SPICE MOS model, defined as KP= $\mu * C_{OX}$)

W,L --- the actual channel width and length of the MOS transistor;

V_{SUB} --- the substrate bias voltage;

$2 \phi_F$ --- the surface potential (PHI, in SPICE);

V_{T0} --- the zero-bias threshold voltage V_{SUB}=0

(VTO,in SPICE);

γ --- the body-effect coefficient (GAMMA, in SPICE);

λ --- the channel length modulation factor (LAMBDA, in SPICE) where

$$\lambda \doteq 1 / [L * (N_{SUB})].$$

If we neglect the body effect and channel length modulation, the first-order drain current equation is expressed as

$$I_{DS} = \frac{\mu C_{OX}}{2} * \frac{W}{L} * (V_{GS} - V_{T0})^2 \qquad (8)$$

For analog circuit applications, the small-signal transconductance, g_m, and output conductance, g_{ds}, are particularly important:

$$\begin{aligned} g_m &= dI_{DS} / dV_{GS} = 2 * I_{DS} / (V_{GS}-V_T) \\ &= 2I_{DS} / V_{DSAT} \\ &= (2 * KP * W/L * I_{DS})^{\frac{1}{2}} \end{aligned} \qquad (9)$$

$$\begin{aligned} g_{DS} &= dI_{DS} / dV_{DS} \doteq \lambda * I_{DS} \\ &= I_{DS} (\lambda_0 * L_0) / L \end{aligned} \qquad (10)$$

The saturation voltage is expressed as a function of the drain bias current and the ratio of the channel width and length as

$$V_{DSAT} = \{ 2 * Id / [KP * W / L] \}^{\frac{1}{2}} \qquad (11)$$

where λ_0 is the channel length modulation factor for a given channel length L_0.

An important difference between MOS and bipolar technology is the fact that the maximum transistor open circuit low-frequency voltage gain, g_m / g_{ds}, is much lower for an MOS transistor because the MOS device exhibits smaller g_m [1],[6],[7].

4. Basic Design of a CMOS Operational Amplifier

The primary function of the operational amplifier described in this paper is to drive a capacitive load with large voltage swing and with minimal distortion.

To design an operational amplifier, we must achieve specifications determined by the application requirements. The most important performance parameters

are open-loop voltage gain, bandwidth, slew-rate, input common-mode range, voltage swing, and input referred RMS noise [6].

The cascode operational amplifier is shown in Fig. 11. The unity-gain bandwidth, w_T, is a key factor in determining the amplifier speed. For this single dominant pole amplifier,

$$BW = w_T = a_v * W_1 \tag{12}$$

where w_1 is the frequency of the dominant pole, p_1, and a_v is the low-frequency open-loop voltage gain expressed as

$$a_v = K * g_{m1} / g_{out} \tag{13}$$

where g_{m1} is the small-signal transconductance of the first-stage of the amplifier, and g_{out} is the output conductance of the amplifier [12]. The dominant pole, p_1, is associated with the high impedance output node and has a frequency of

$$w_1 = g_{out} / C_L \tag{14}$$

Therefore, the unity-gain bandwidth is equal to

$$BW = a_v * w_1 = K * g_{m1} / C_L \cdot \qquad (15)$$

The slew-rate is the maximum rate of change of the output voltage, dV_0/dt, and is directly related to the input stage tail current which is $2I_d$:

$$SR = 2I_d / C_L \quad (V / \text{micro sec}) \qquad (16)$$

From equations (13)-(16), we calculate the device width (W), length (L), and bias current (I_d) given the desired unity-gain bandwidth, slew-rate, open-loop voltage gain, and voltage swing.

In this thesis, for the design of both two-stage and cascode operational amplifiers, $V_{D(SAT)}$ is set to 0.35 volts based on the device size considerations and avoiding subthreshold region of operation. The quiescent current, I_d, is designed to be 20 μA based on minimum power consumption, maximum slew-rate, and also practical device sizes.

For a two-stage operational amplifier shown in Fig. 3(a), the most commonly used frequency compensation technique is "pole splitting" which is used to create an approximate single-pole frequency response. The pole-splitting model is illustrated in Fig. 5 for the use of two gain stages. The feedback capacitor, C_f, is on-chip and connected across an inverting gain stage to realize a very large effective capacitance according to the Miller Effect. A dominant low-frequency pole is created at node (a) because of this very large effective capacitance. Simultaneously, the pole associated with node (b) is moved to a higher frequency. The transfer function after compensation is given by

$$a(S) = \frac{a_v\ (1 + S/Z)}{(\ 1 + S/P_1\ )(\ 1 + S/P_2\ )(\ 1 + S/P_3\ )} \qquad (17)$$

where

$$Z \doteq 1\ /\ (\ C_f/g_{m2} - r_f\ C_f\ )\ ; \qquad (18)$$

$$P_1 \doteq -1\ /\ (\ g_{m2}\ r_1\ r_2\ C_f\ ) \doteq -g_{m1}\ /\ (\ a_v\ C_f\ )\ ; \qquad (19)$$

$$P_2 \doteq -g_{m2}\ C_f\ /[C_1\ C_L + C_f(\ C_1 + C_L)] \doteq -g_{m2}/C_L\ ; \qquad (20)$$

(assuming $C_L >> C_1$)

$$P_3 \doteq -1 / (r_f C_1) . \qquad (21)$$

For an amplifier to maintain acceptable closed-loop stability, only the dominant pole p_1 is placed below the unity-gain frequency, w_u. Any nondominant poles can exist below the unity-gain frequency only as doublets, which means one left-half-plane (LHP) pole and one LHP zero at nearly identical frequencies. Compensation details are given in [8]. If the capacitive load is small then when $R_f = 1/g_{m2}$, the zero is at infinity. For further increases in the value of R_f, the zero will be moved from the RHP into the LHP, and ideally located on the top of second pole, p_2 to cause pole-zero cancellation. This technique both reduces the required compensation capacitance and increases the unity-gain bandwidth of the amplifier [9].

III. DESIGN CONSIDERATIONS FOR HIGH SWING CMOS OPERATIONAL AMPLIFIER

1. Basic Requirements of High-Swing Operational Amplifier Design

As shown in the previous section, the output swing and input common-mode range of a general purpose operational amplifier are substantially less than the power supply range and are not symmetric about the mid-supply value. For example, a two-stage CMOS operational amplifier with an n-channel input pair is shown in the Fig. 3(a). With a proper choice of the DC bias voltages, the positive input common-mode range (V_{dd}-$V_{DS(SAT)}$) nearly equals V_{dd}. Unfortunately, the negative input common mode range is at least one gate-source voltage and one saturation voltage above V_{ss}, the negative power supply. From Fig. 3(d) which is a plot of $I_t = 2I_d$ versus common-mode input voltage, the tail current I_t is decreased and MN5 is turned off when the common-mode input voltage is more negative than V_{ss} + (V_{gs} + V_{DSAT}). A similar situation occurs with the CMOS op amp with the p-channel input pair shown in Fig. 4, but in the opposite direction. The negative common-

mode input range ($V_{SS}+V_{DS(SAT)}$) nearly equals the negative power supply voltage, V_{SS}. However, device MP5 is turned off when the common-mode input voltage exceeds $V_{dd} - (V_{gs} + V_{DSAT})$. as shown in Fig. 4(b).

If two amplifiers with n- and p-channel input pairs are connected in parallel, the composite amplifier achieves nearly a rail-to-rail common-mode input range. Unfortunately, there are serious problems involved in realizing these apparent swing advantages in a real circuit. The op amp must over the entire swing range maintain high linearity, controlled quiescent output current, and closed-loop stability, and must exhibit no cross-over distortion. These requirements present a difficult design task [2], [11].

2. Conceptual Solution

One version of a composite CMOS amplifier consists of two amplifiers with n- and p-channel input pairs as shown in Fig. 6 [4]-[5]. The amplifier with n-channel input pair operates over the positive portion of voltage signal. Conversely, the amplifier with p-

channel input pair operates over the negative portion of the signal. Unfortunately, there are many practical problems with this kind of connection. First of all, the voltage gain cannot be maintained at a constant value over the input common-mode range, which causes significant signal distortion. The reason for the variable voltage gain is that in the output stage, each device (MP6 and MN8) is controlled by one op amp. This is similar to two voltage controlled current sources connected in series. When the common-mode signal is close to the positive power supply, only the n-amplifier is active, and it controls the upper device MP6 to conduct a current, I_S. Similarly, when the common-mode input signal is close to the negative power supply, only the p- amplifier is active and it controls the lower device MN8 to conduct a current also designed as I_S. Moreover, when the common-mode input signal is in the mid-range of the power supplies, both n- and p-amplifiers are active and both output devices are conducting. Unfortunately, the output current becomes unpredictable because of the two devices that are driven by unrelated bias voltages. This causes the voltage gain linearity and hence the distortion problem, and unpredictable DC offset voltages.

Secondly, the composite op amp may become unstable after connecting stable n- and p-amplifiers assuming local compensation. The overall poles and zeros position are changed, and therefore, more compensation elements (capacitors and resistors) are needed in order to make the composite operational amplifier stable. This not only makes the circuit more complex, but also costs more chip area and reduces the speed of the amplifier. Finally, the cross-over discontinuity problem has also been reported for this kind of configuration [2].

3. Practical Solution

i. A two-stage CMOS op amp implementation

In one very promising composite CMOS operational amplifier topology, problems are avoided by summing the DC bias and AC small signal currents of the complementary input stage into a shared NMOS current mirror load as shown in Fig. 7. This composite input stage is then followed by a common-source second gain stage including only one conventional pole-splitting frequency compensation network.

For a common-mode input signal near V_{dd}, the NMOS differential pair is active and the PMOS pair is turned off. For a common-mode input voltage close to V_{ss}, the PMOS pair is active and the NMOS pair is turned off. In the mid-range of power supply, both pairs are active. Therefore, this CMOS amplifier exhibits a very wide common-mode input voltage range as shown by the simulated unity-gain DC transfer curve of Fig. 8.

The significant difference between this circuit and previous circuits is that the bias currents are accurately controlled. At the extremes near V_{dd} or V_{ss} when only one input pair is active, the DC bias current is approximately halved as compared to the mid-range value. Thus, the input stage transconductance is also halved. A very important result of these bias current controls is that the output conductance of the first stage is also halved when only one pair is active. Thus, the ratio of the small-signal transconductance to the output conductance is kept nearly constant. Therefore, the small-signal gain is also kept very constant over the entire voltage range as shown in Fig. 9.

The quiescent current in the NMOS current source load versus input common-mode voltage range is shown in Fig. 10. The very constant nature of this current for the mid-range common-mode voltage is obtained as a result of the cancellation of the channel-length modulation effects by summing the bias currents from the p- and n-channel tail current sources.

Furthermore, as the NMOS input stage is not required to operate near V_{ss}, and the PMOS input stage is not required to operate near V_{dd}, cascode tail current sources may be used not only to increase the bias current linearity, but also to increase the Common Mode Rejection Ratio (CMRR).

ii. A cascode CMOS op amp implementation

A high-swing cascode operational amplifier employing the new design principle has also been developed and is shown in Fig. 11. The main advantage of this topology over the two-stage topology is that the load capacitance serves as the frequency compensation capacitance, and eliminates the pole-splitting network. The cascode op amp output stage may also increase the op amp open-loop low-frequency

voltage gain in comparison to a two-stage op amp. A disadvantage of the cascode op amp is that the output swing is slightly reduced by the presence of the cascode structure as shown in Fig. 11b. As before, the input stage is the same as with the two-stage implementation. The bias and signal currents are summed into a shared current source load preceding the output stage. The quiescent current of Fig. 12 is similar to that of Fig. 10 for the two-stage composite amplifier. The output quiescent current is very well controlled and very linear over mid-range of common-mode input voltage. The well controlled quiescent current behavior ensures that the overall voltage gain linearity is excellent as shown in Fig. 13 [13].

IV. SIMULATION RESULTS

The two operational amplifiers are being fabricated in a 3-μm p-well CMOS process using the MOSIS[1] fabrication service. Fig. 14 shows a plot of the layout of the two-stage operational amplifier and Fig. 15 shows a plot of the layout of the cascode operational amplifier. Device sizes are listed in the Table I. Actual experimental results will be published at later date. The process parameters of the MOSIS 3-μm CMOS P-well technology used in all SPICE simulations are listed in Appendix I.

The well-controlled bias current ensures the very high linearity of voltage gain through the entire common mode input range. For the two-stage op amplifier, the linear range of voltage gain from the 79dB to the 85dB is calculated as 95% of total power supply range. For the cascode op-amplifier, the linear range from 90dB to 93db is about 90% of power supply range. Therefore, both amplifiers have a significantly higher linear range over a very high percentage of

1. MOS Implementation Service -- an organization that provides university communities with IC fabrication services.

total power supply range as compared to previously reported designs.

This high swing topology is well-suited for a small power supply range which is a future goal. Without changing any design considerations, the SPICE2 simulations were done with the total power supply range of 5 volts, as in Fig. 16. This topology is also very promising for use at 3.3 volts of total power supply voltage.

The SPICE input files of the high-swing two-stage op amp is listed in Appendix II and cascode op amp is listed in Appendix III.

V. CONCLUSIONS.

In this thesis, a new high-swing, high-linearity CMOS operational amplifier topology has been studied. The topology uses a different approach for high-swing performance than any previous configuration. It significantly improves the op amp common-mode input range and output swing with very high linearity. Circuits details and simulation results have been given. This topology is well-suited for designing analog subsystems working in small voltage supply ranges. The topology also can be implemented in different operational amplifier configurations such as class-AB [14] and adaptive-biased configurations [15].

TABLE I. COMPONENT SIZES (μm, pF).

1. High-Swing Two Stage Op Amp

M1P	110/12	M11	80/4
M2P	110/12	M12	80/4
M1N	18/4	M13	168/8
M2N	18/4	M14	168/8
M5P	168/8	M15	168/8
M5PA	168/8	M16	168/8
M5N	80/4	R_f	2.9K ohm
M5NA	80/4	C_f	8
M6P	160/4	C_L	10
M8P	1008/8		

2. High-Swing Cascode Op Amp

M1P	110/12	M11	80/4
M2P	110/12	M12	80/4
M1N	18/4	M13	168/8
M2N	18/4	M14	168/8
M5P	168/8	M15	168/8
M5PA	168/8	M16	168/8
M5N	80/4	M9	336/8
M5NA	80/4	M7	80/4
M3	336/8	M8	80/4
M4	336/8	M10	80/4
M6	336/8	M20	80/4
C_L	10		

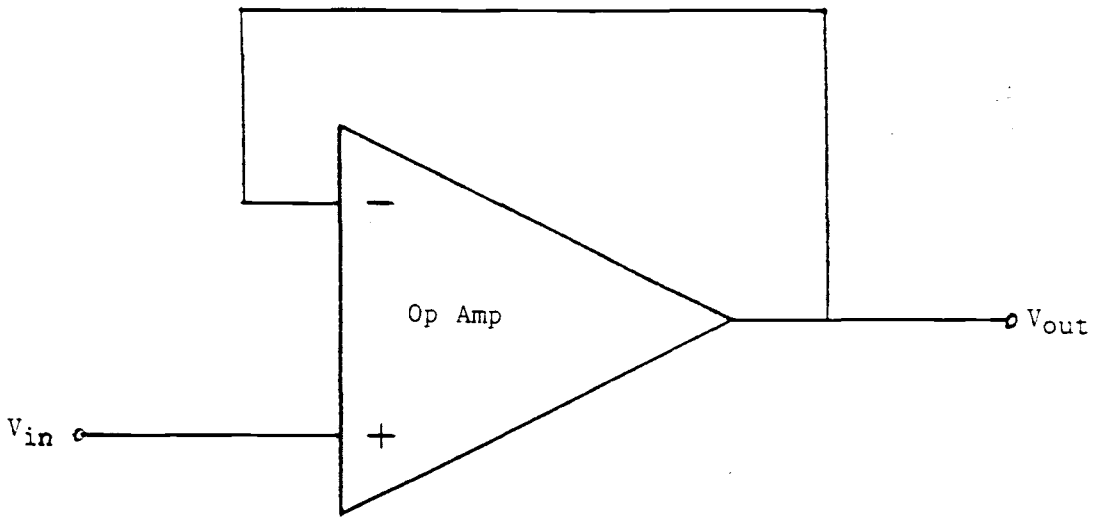


Fig. 1 A operational amplifier in a unity-gain buffer configuration.

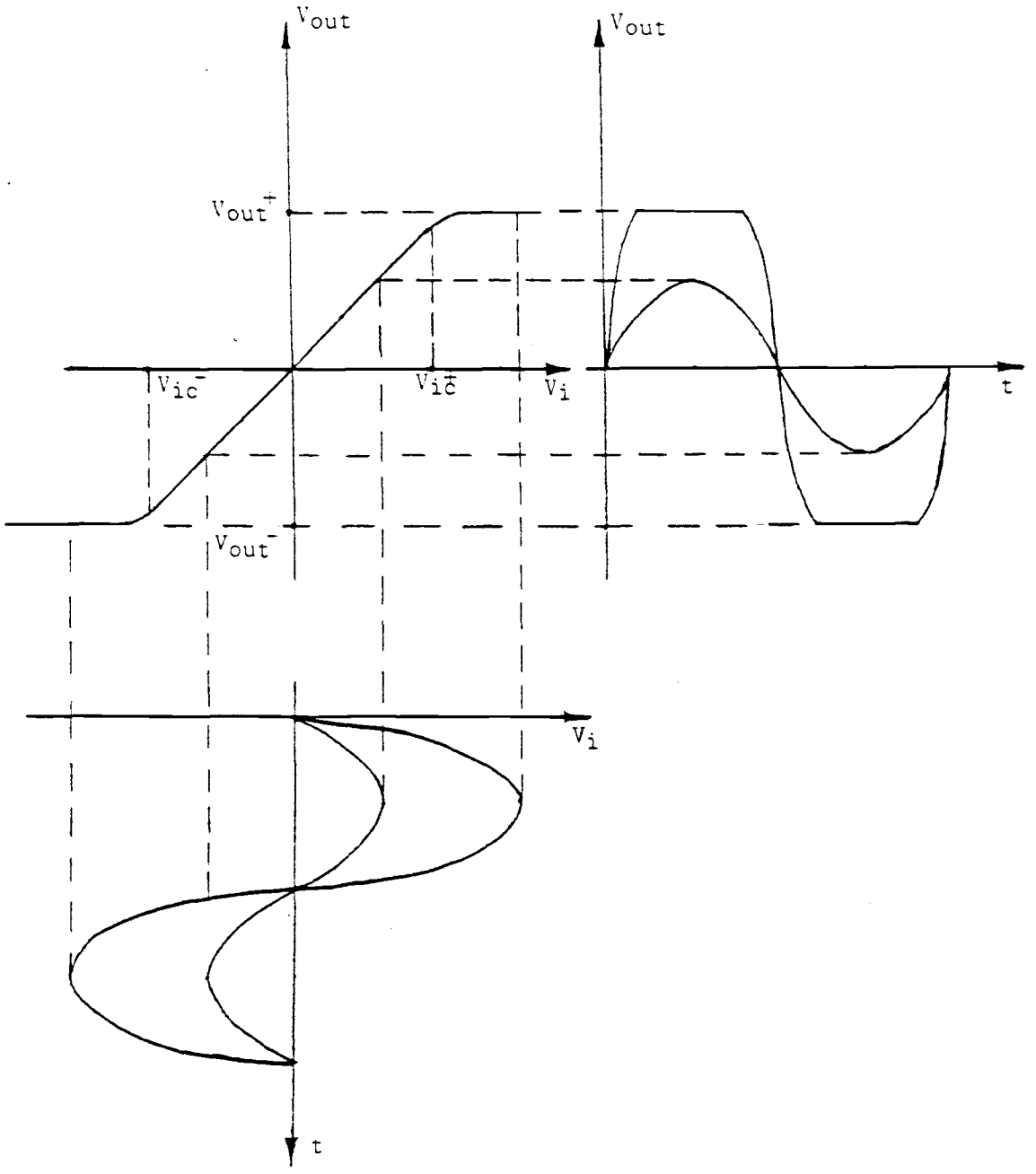


Fig. 2 Output waveforms for various amplitude common-mode input signals applied to the unity-gain buffer amplifier.

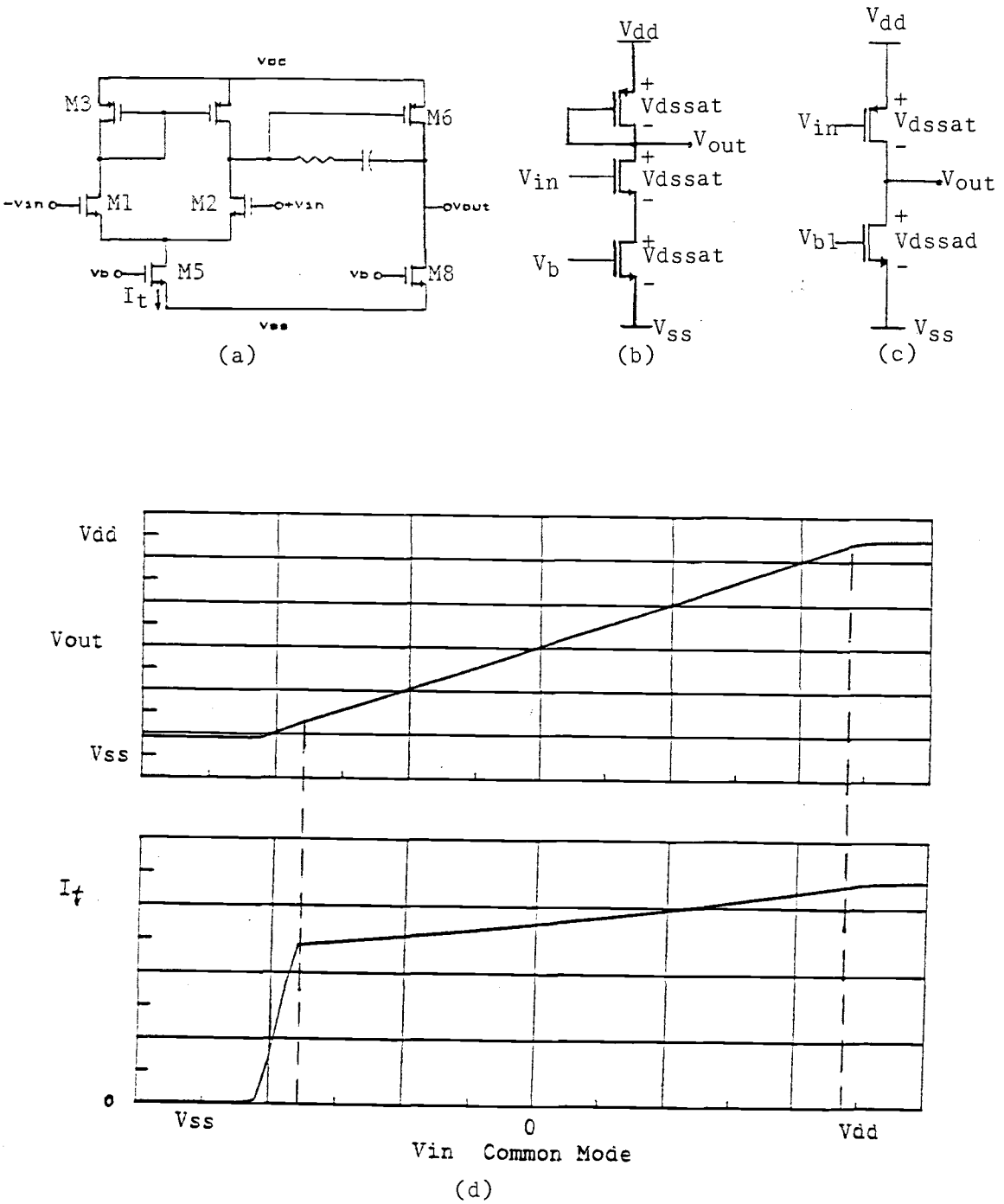
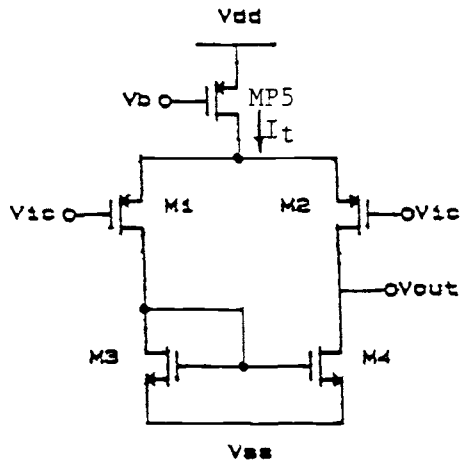


Fig. 3 A two-stage CMOS op amp with n-MOS input pair. (a) Schematic; (b) Common-mode half-input pair; (c) Output stage; (d) Common-mode input range and output swing.



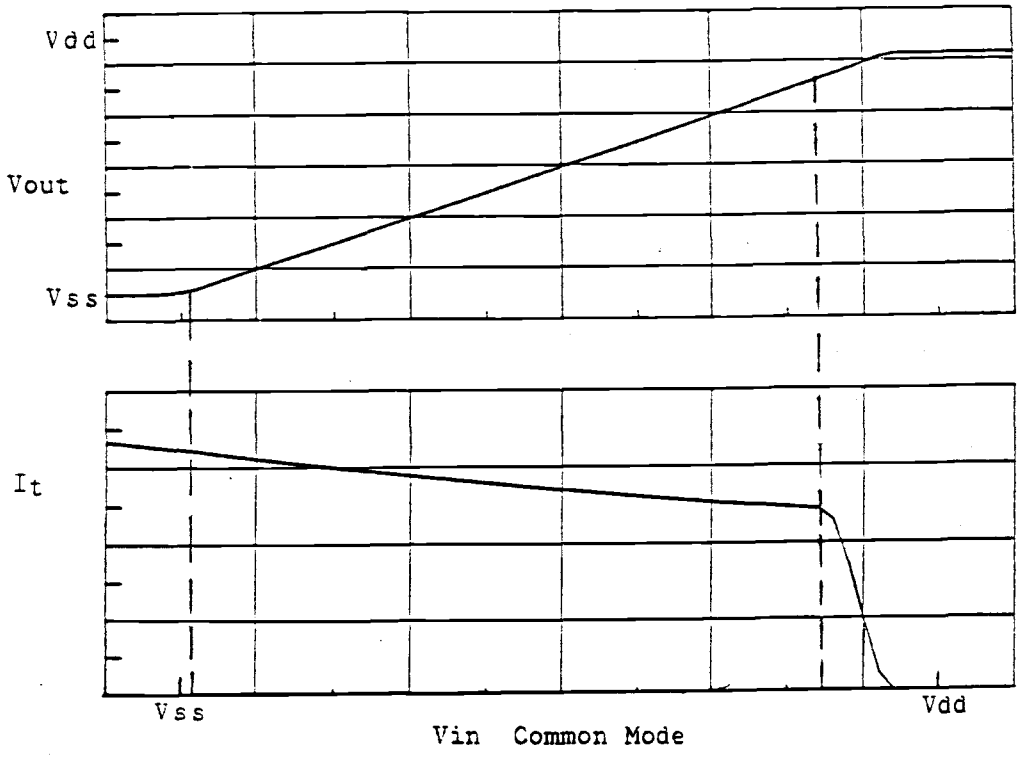


Fig. 4 A p-MOS input pair with its simulated input common-mode range.

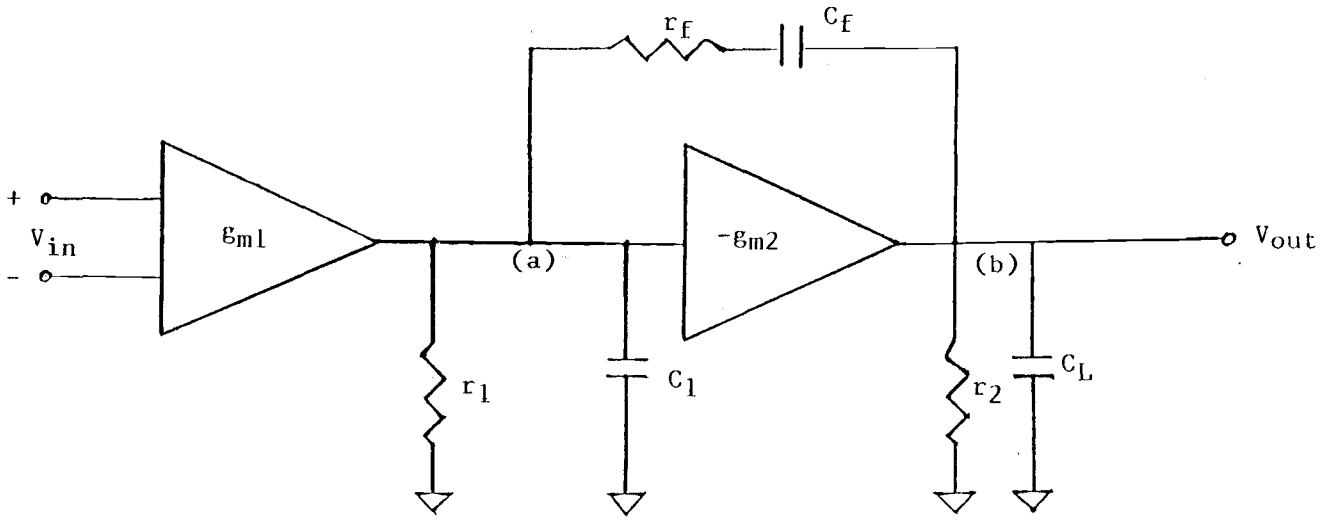


Fig. 5 Pole-splitting compensation. Small-signal equivalent circuit model.

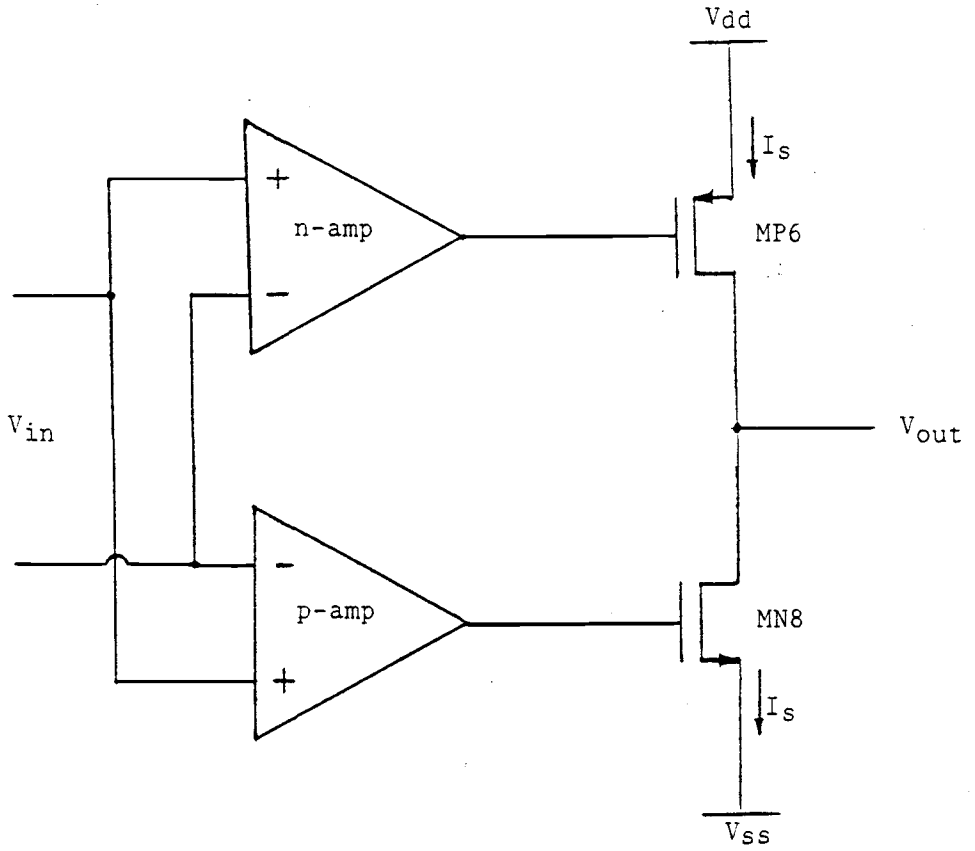


Fig. 6 One possible composite CMOS amplifier configuration.

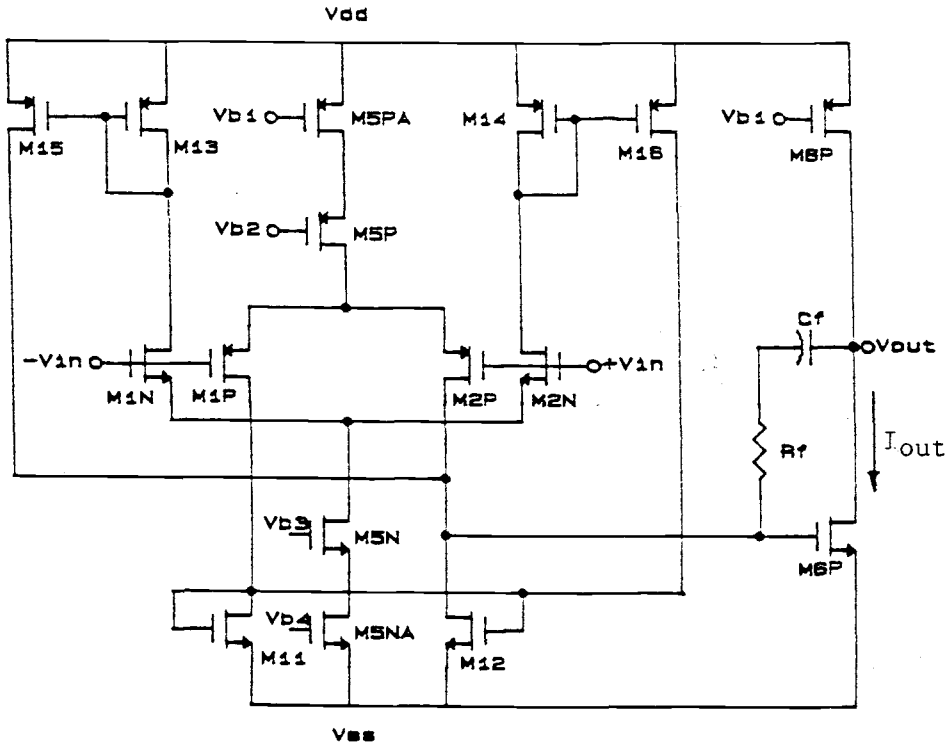


Fig. 7 Schematic of high-swing two-stage op amp.

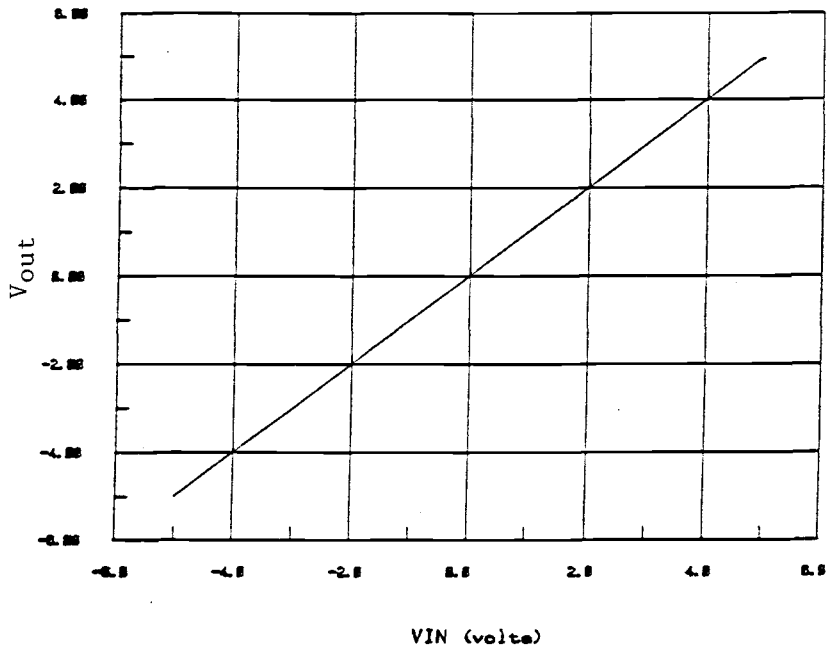


Fig. 8 Common-mode input and output ranges of high-swing two-stage op amp.

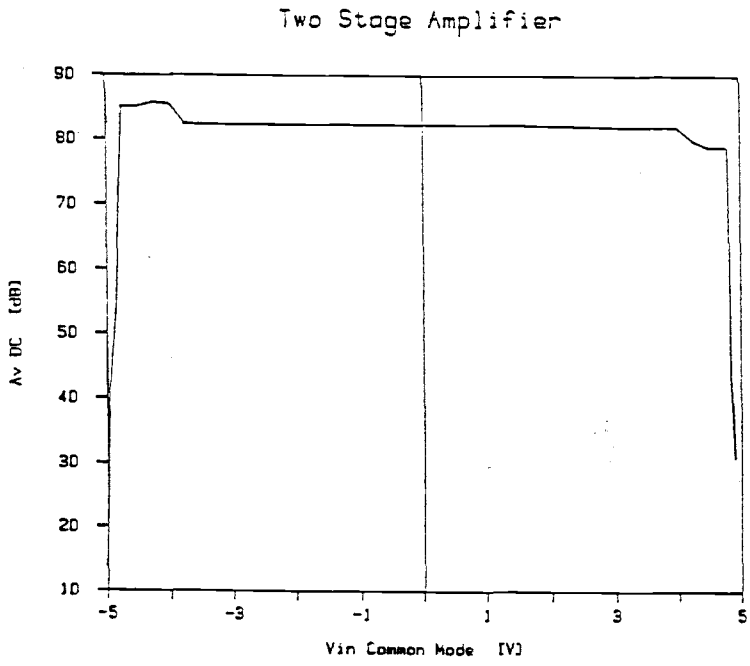


Fig. 9 Small-signal voltage gain versus input common-mode voltage(two-stage op amp).

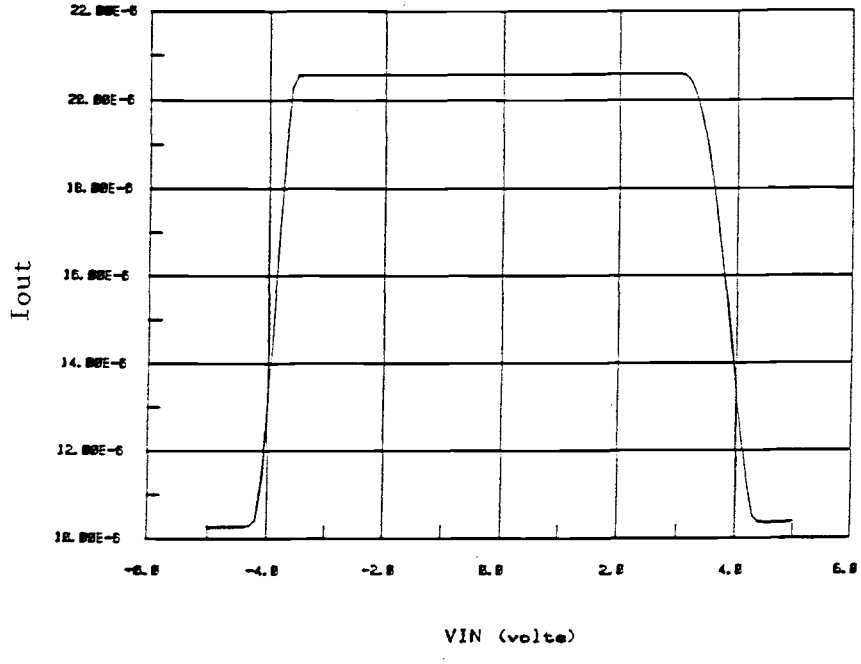


Fig. 10 Quiescent bias output current versus input common-mode voltage.

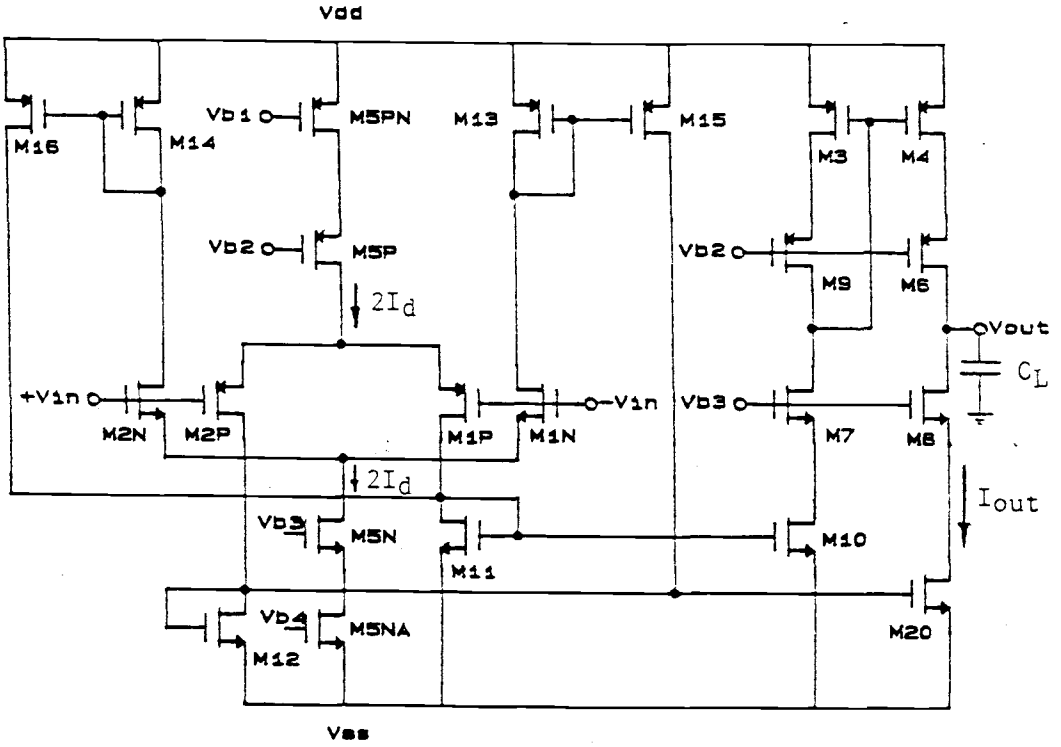


Fig. 11 Schematic of the high-swing cascode op amp.

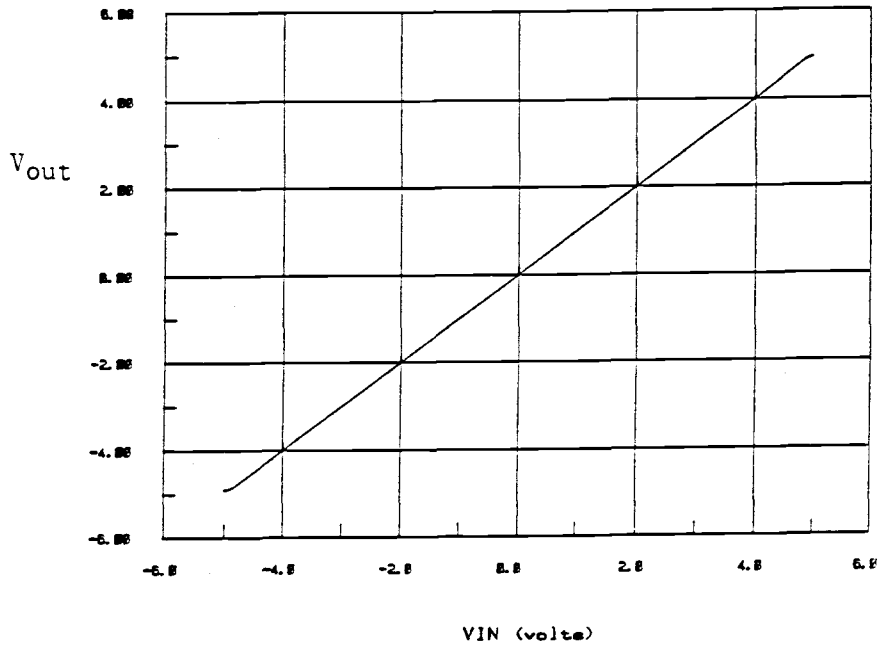


Fig. 11b Common-mode input and output range of high-swing cascode op amp.

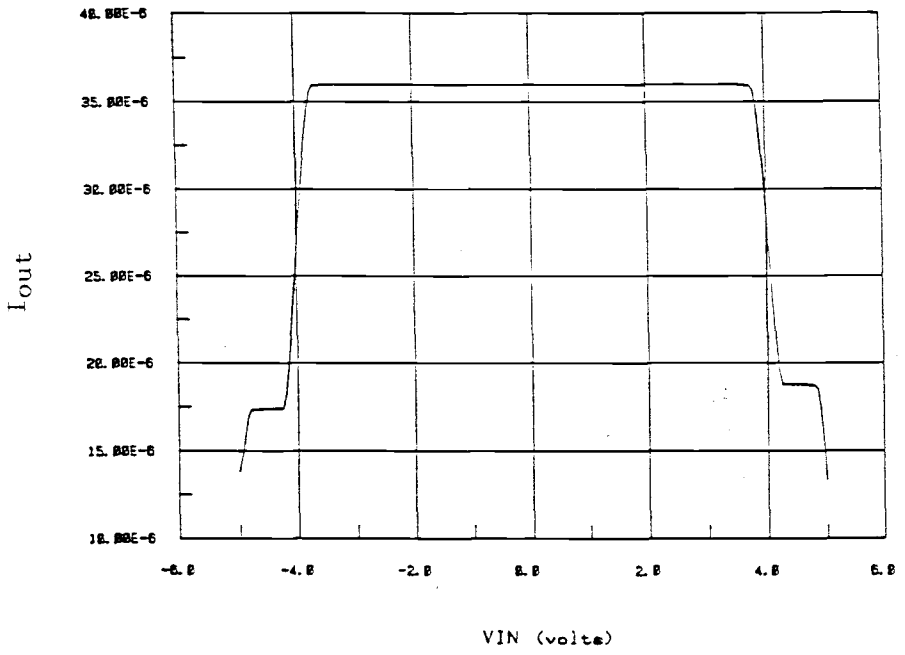


Fig. 12 Quiescent bias output current versus input common-mode voltage.

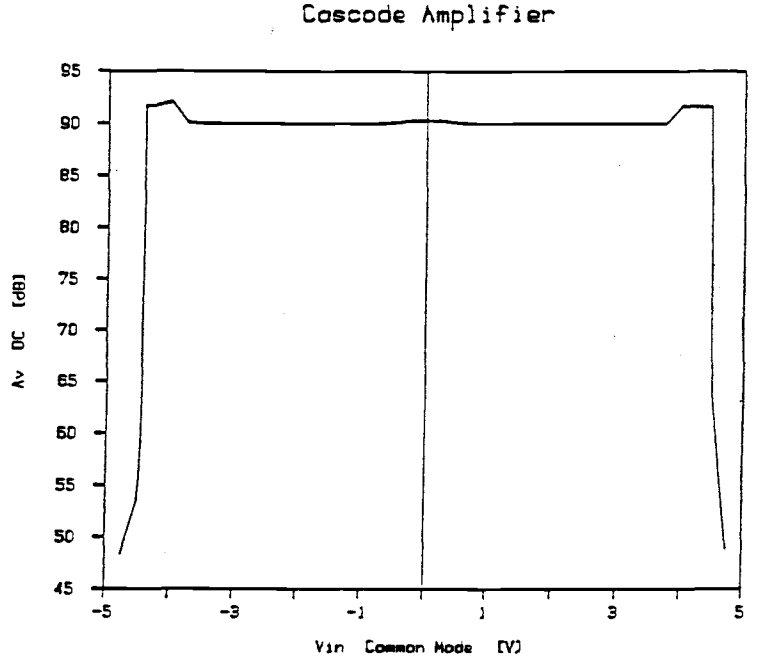


Fig. 13 Small-signal voltage gain versus input common-mode voltage (cascode op amp).

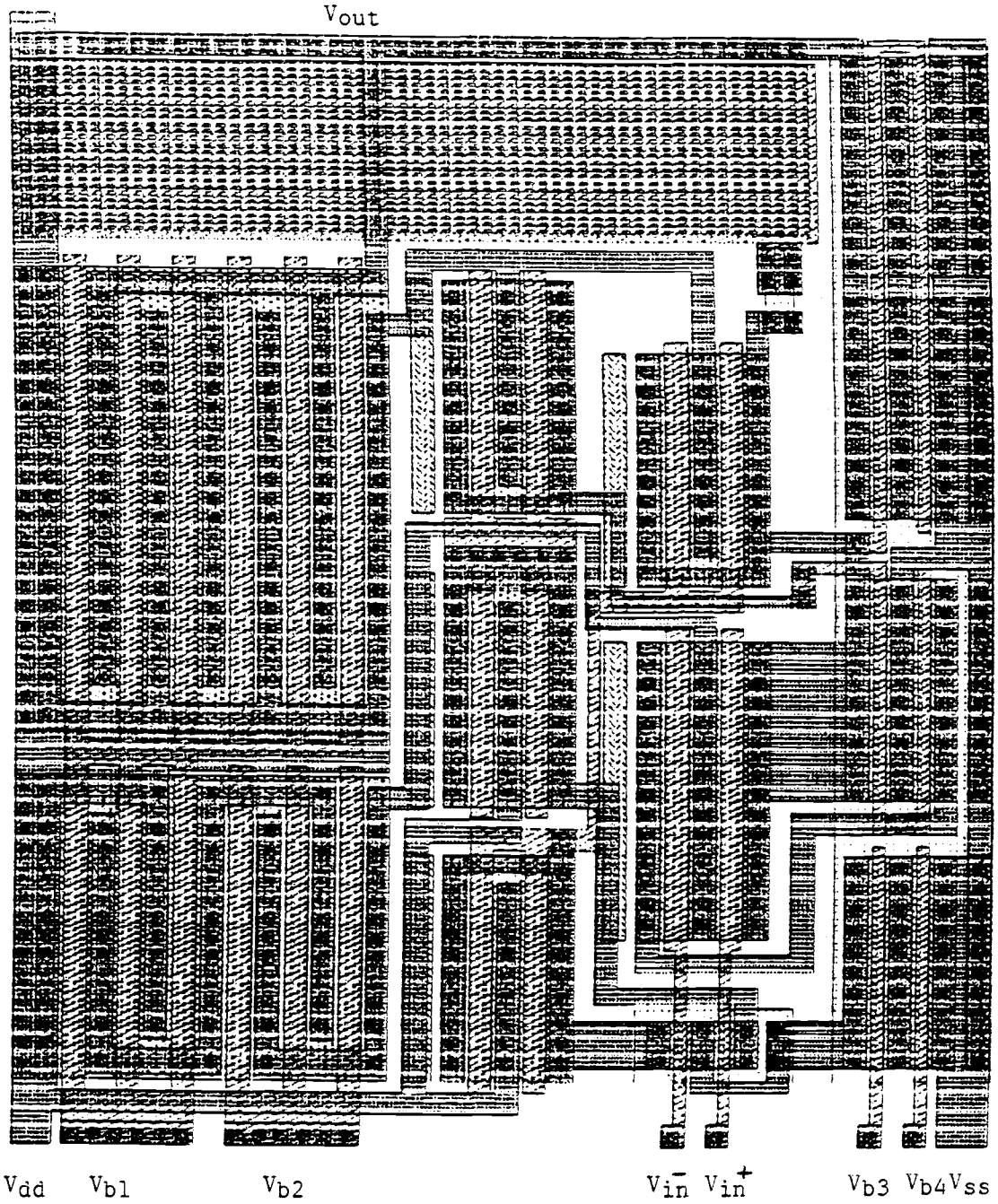


Fig. 14 Layout of the high-swing two-stage op amp.

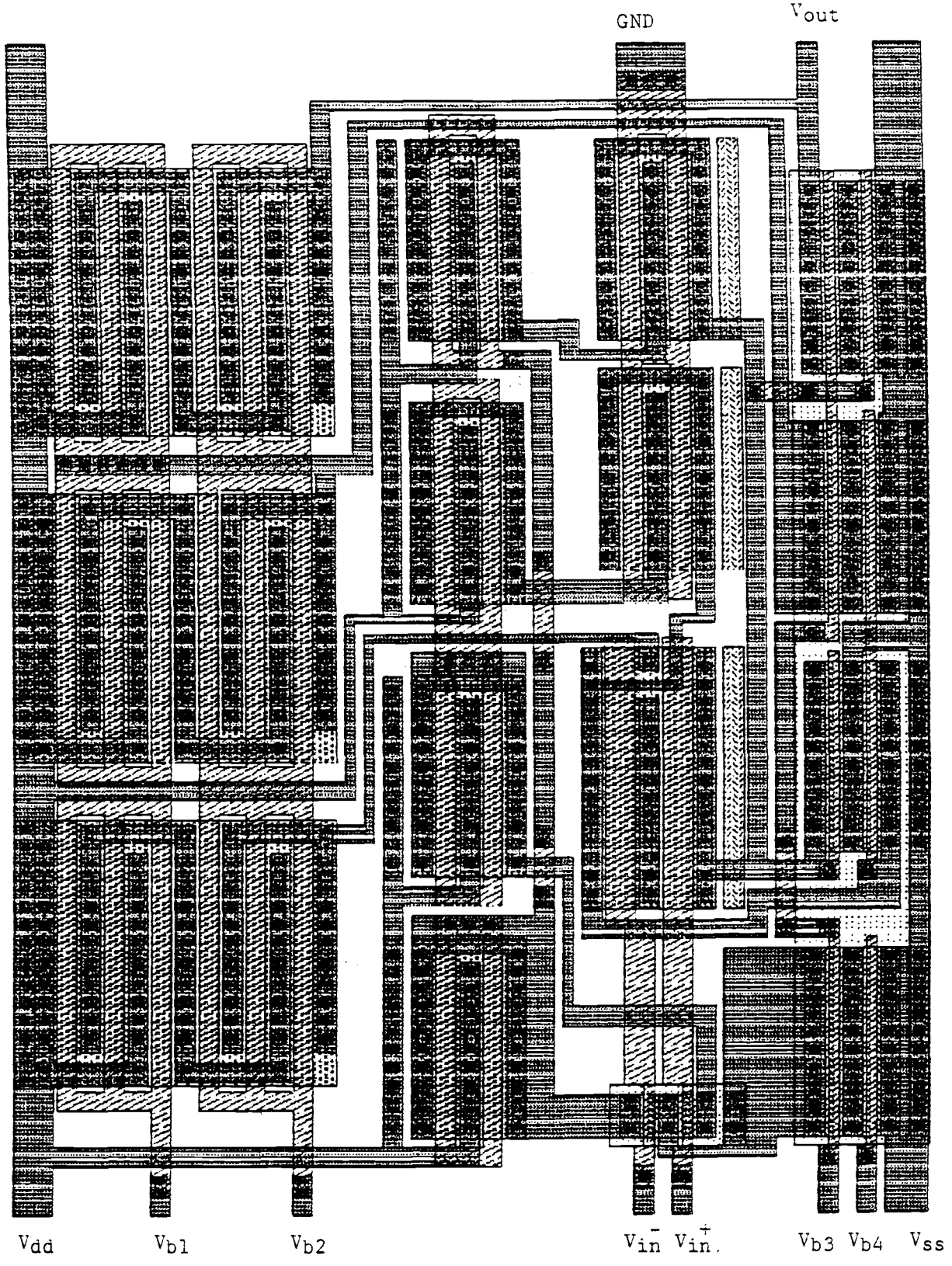


Fig. 15 Layout of the high-swing cascode op amp.

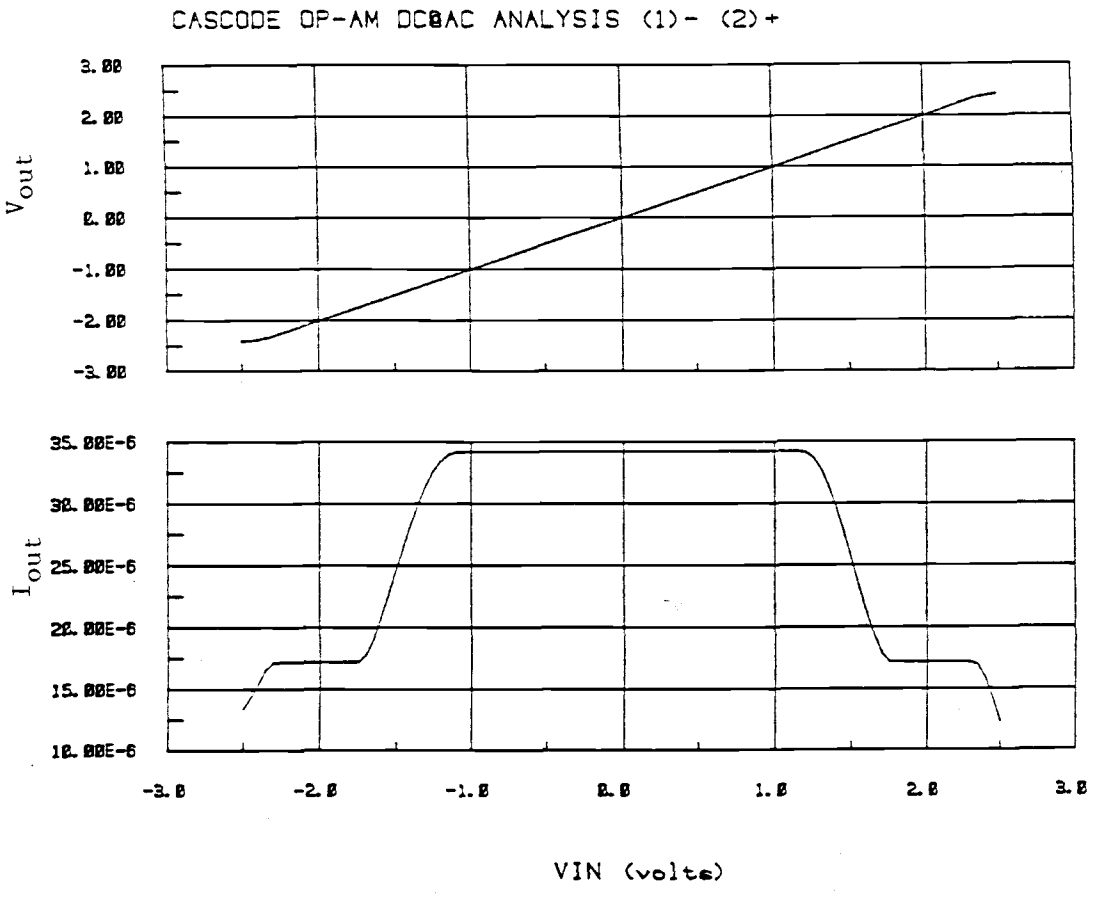


Fig. 16 Simulated results of the cascode op amp at 5 volts power supply.

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APPENDICES

APPENDIX I. MOSIS Process Parameters

```
*         MOSIS STANDARD 3-μm P-WELL CMOS PROCESS PARAMETERS

*         NOMINAL N-CHANNEL MODEL ( L=3 MICRONS )

.MODEL    N03  NMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.0E+16  VTO=0.827125  KP=3.286649E-05
+         PHI=0.6  UO=200  UEXP=1.001E-03  UCRIT=999000
+         DELTA=1.2405  VMAX=100000  XJ=0.4U
+         NFS=1.234795E+12  NEFF=1.001E-02  TPG=1.0
+         RSH=25  CGSO=5.2E-10  CGDO=5.2E-10  CJ=3.2E-04
+         CJSW=9.0E-10  MJSW=0.33  AF=1.25  KF=1.0E-27
+         GAMMA=1.3596 LAMBDA=1.604983E-2 MJ=0.5

+
.MODEL    N04  NMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.0E+16  VTO=0.827125  KP=3.286649E-05
+         PHI=0.6  UO=200  UEXP=1.001E-03  UCRIT=999000
+         DELTA=1.2405  VMAX=100000  XJ=0.4U
+         NFS=1.234795E+12  NEFF=1.001E-02  TPG=1.0
+         RSH=25  CGSO=5.2E-10  CGDO=5.2E-10  CJ=3.2E-04
+         CJSW=9.0E-10  MJSW=0.33  AF=1.25  KF=1.0E-27
+         GAMMA=1.3596 LAMBDA=1.203737E-2 MJ=0.5

*         NOMINAL P-CHANNEL MODEL ( L=3 MICRONS )

.MODEL    P03  PMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.121088E+16 VTO=-0.894654 KP=1.526452E-05
+         PHI=0.6  UO=100  UEXP=0.153441 UCRIT=16376.5
+         DELTA=1.93831 VMAX=100000 XJ=0.4U
+         NFS=8.788617E+11 NEFF=1.001E-02  TPG=-1.0
+         RSH=95  CGSO=4E-10  CGDO=5.2E-10  CJ=2E-04
+         CJSW=4.5E-10  MJSW=0.33 AF=1.25  KF=1.5E-27
+         GAMMA=0.879003  LAMBDA=4.708659E-02  MJ=0.5

.MODEL    P08  PMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.121088E+16 VTO=-0.894654 KP=1.526452E-05
+         PHI=0.6  UO=100  UEXP=0.153441 UCRIT=16376.5
+         DELTA=1.93831 VMAX=100000 XJ=0.4U
+         NFS=8.788617E+11 NEFF=1.001E-02  TPG=-1.0
+         RSH=95  CGSO=4E-10  CGDO=5.2E-10  CJ=2E-04
+         CJSW=4.5E-10  MJSW=0.33 AF=1.25  KF=1.5E-27
+         GAMMA=0.879003  LAMBDA=1.810000E-02  MJ=0.5
```

APPENDIX II. SPICE Input File of Two-Stage Op Amp

```
MOSAMP(OAADA) DC&AC ANALYSIS (1)- (2)+
++++++++++++++++++++++++++++++CIRCUIT 1
N1  1  2  3  4 54 53  5  6       100 200 NAMP
P1  1  2  3  4  8 51 52 12 9 10 100 200 PAMP
****************************************
IN          2  7  DC AC
VIN         2  7  PULSE(0  4.7)
BIAS        7  0  0
DC VIN      5 -5  0.25
************************************3.9K
IY    10  200
****************************************
COM    4  11    2.9K
COM   11   8    8P
I1     8  13
LOAD  13   0    25P
LLOAD  8   0    1
.PR    DC  V(6)    V(12) V(5) V(9)
.PR    DC  V(4)    V(3)
GR     DC  V(8)    I(VIY)
GR     AC  VDB(8)  VP(8)
.PR     AC  VDB(8)  VP(8)
.GR TRAN   V(2)    V(8)   I(VI1)
NODESET   V(1)=0   V(2)=0    V(8)=0    V(4)=-3.8126
          V(6)=-4.5098 V(12)=2.3474 V(5)=-1.3219
          V(3)=-3.8126 V(9)=4.5705
************************************++++END OF 1
DD    100   0   5
SS    200   0  -5
************************************************
AC  DEC  5   10 10MEG
.TRAN 100NS 5US
.FOUR  1K V(8,0)
OPTIONS  NOPAGE  LIMPTS=1001 NOMOD
OP
****************************************
SUBCKT NAMP 1 2 10 7 9 15 5 6 100 200
INCLUDE NAAST
ENDS   NAMP
SUBCKT PAMP  51 52 53 54 58 59 75 55 60 70
             100  200
INCLUDE PAAST
ENDS   PAMP
INCLUDE DCBIAS
INCLUDE MDEL3
END
```

APPENDIX II.(Cont.1)

```
* N-CH(NAAST) CMOSAMP STRUCTURE-FILE(REDESIGN)
M1N  3  1  5  5   N04  W=18U    L=4U
+          AD=240P   AS=240P   PD=46U   PS=46U
M2N  4  2  5  5   N04  W=18U    L=4U
+          AD=240P   AS=240P   PD=46U   PS=46U
M3N  3  3 100 100 P12  W=252U   L=12U
+          AD=6N     AS=6N     PD=430U  PS=430U
M4N  4  4 100 100 P12  W=252U   L=12U
+          AD=6N     AS=6N     PD=430U PS=430U
M5N  6  9 200 200 N04  W=80U    L=4U
+          AD=1.26N  AS=1.26N  PD=114U PS=114U
M55N  5 15  6 200 N04  W=80U    L=4U
+          AD=1.26N  AS=1.26N  PD=114U PS=114U
M7N  7  3 100 100 P12  W=252U L=12U
+          AD=36N    AS=36N  PD=2430U PS=2430U
M10N 10 4 100 100 P12  W=252U L=12U
+          AD=5.04N  AS=5.04N  PD=366U PS=366U
*IM9N 100  9   20U
D8P  8  100 DMOD
D8N  200  8 DMOD
D5P  5  100 DMOD
D5N  200  5 DMOD
D4N  200  4 DMOD
D4P  4  100 DMOD
D3P  3  100 DMOD
D3N  200  3 DMOD
*****************************************************
```

APPENDIX II.(Cont.2)

```
*P-CH(PAAST) CMOSAMP STRUCTURE(REDESIGN) (70 200)
************************ BEGIN.
M1P   53   51   55 100 P12 W=110U L=12U
+                       AD=930P AS=930P PD=92U PS=92U
M2P   54   52   55 100 P12 W=110U L=12U
+                       AD=930P AS=930P PD=92U PS=92U
M3P   53   53   70 200 N04 W=80U L=4U
+                       AD=630P AS=630P PD=72U PS=72U
M4P   54   53 200 200 N04 W=80U L=4U
+                       AD=630P AS=630P PD=72U PS=72U
M5P   60   59 100 100 P12 W=504U L=12U
+                 AD=1.875N AS=1.875N PD=155U PS=155U
M55P 55   75   60 100 P12 W=504U L=12U
+                 AD=1.875N AS=1.875N PD=155U PS=155U
M6P   58   54 200 200 N04 W=160U L=4U
+                       AD=630P AS=630P PD=72U PS=72U
M8P   58   59 100 100 P12 W=1008U L= 8U
+                       AD=630P AS=630P PD=72U PS=72U
*IM9P 59   200   20U
D58P 57   100   DMOD
D58N 200   57   DMOD
D53P 53   100   DMOD
D53N 200 53    DMOD
D54N 200 54    DMOD
D54P 54   100   DMOD
D55P 55   100   DMOD
D55N 200 55    DMOD
****************************** END.
```

APPENDIX III. SPICE Input File of Cascode Op Amp

```
ASCODE OP-AMP (CAADA) DC ANALYSIS (1)- (2)+
 REDESIGN
++++++++++++ CIRCUIT 1
1 1 2 3 4 5 6 7 8 9 10 20 11 13 14 1 2 15 18
  100 200 0 AMP
**********************************************
BIAS   2  12   0
**********************************************
VUFB    1   8
IY     8   18
LOAD   8    0   25P
LOAD  8   0    1
GR   DC  V(8)   I(VIY)
GR   AC  VDB(8) VP(8)
.PR   DC V(3) V(4) V(5) V(6) V(7) V(8)
.PR   DC V(9) V(10) V(20)
.PR   DC V(15)
.PL   DC V(8)
PR  AC  VDB(8) VP(8)
.NOISE V(8)  VIN  5
.GR NOISE   INOISE(DB)
.GR    TRAN V(8) V(2)
NODESET  V(1)=0 V(2)=0 V(8)=0 V(4)=4.5851 V(3)=4.5849
 V(6)=-4.4826 V(7)=3.7245 V(9)=-4.4826  V(11)=3.7245
 V(15)=-1.2868 V(10)=-3.8459 V(20)=-3.8459 V(14)=3.7394
 V(5)=2.3163 V(13)=3.7394
**************************POWER SUPPLY VOLTAGE
DD   100  0   5
SS   200  0  -5
**********************************************************
IN     12  0  D   AC
VIN      12  0  PULSE(0  4.75 0  0.15US)
OP
DC VIN     5  -5   0.1
AC    DEC  5   1   5MEG
.NOISE V(8)  VIN  5
.TRAN    20NS   2U
OPTIONS NOPAGE LIMPTS=1001 NOMOD
        NODE  LIST
******************************************
SUBCKT AMP 1 2 3 4 5 6 7 8 9 10 20 11 13 14 21 22
  25 88 100 200  500
INCLUDE DCBIAS
INCLUDE CAAST
INCLUDE MDEL3
END
```

APPENDIX III.(Cont.1)

```
*     OP-AMP CASCODE STRUCTURE FILE
*     REDESIGN
***   MAIN CIRCUIT (7,10) SHOULD BE BIASED    8-88
**************************************************
M5PA    56    51    100    100     P08    W=336U  L=8U
+             AS=4.536N AD=4.536N PS=522U  PD=522U
M5P      5    52     56    100     P08    W=336U  L=8U
+             AS=4.536N AD=4.536N PS=522U  PD=522U
M2P     20     2      5    100     P12    W=110U L=12U
+             AS=990P   AD=990P   PS=128U  PD=128U
M1P     10     1      5    100     P12    W=110U L=12U
+             AS=990P   AD=990P   PS=128U  PD=128U
M1N     13    21     25     25     N04    W=18U  L= 4U
+              AS=162P   AD=162P   PS=36U   PD=36U
M2N     14    22     25     25     N04    W= 18U  L=4U
+              AS=162P   AD=162P   PS=36U   PD=36U
M5N     25    53     58     58     N04    W= 80U  L=4U
+                 AS=720P  AD=720P  PS=98U  PD=98U
M5NA    58    54     200   200     N04    W= 80U  L=4U
+                 AS=720P  AD=720P  PS=98U  PD=98U
M3       3    11     100    100     P08    W=336U  L=8U
+             AS=4.536N AD=4.536N PS=522U  PD=522U
M4       4    11     100    100     P08    W=336U  L=8U
+             AS=4.536N AD=4.536N PS=522U  PD=522U
M9       7    52      3     100     P08    W=336U  L=8U
+              AS=4.536N AD=4.536N PS=522U PD=522U
M6       8    52      4     100     P08    W=336U  L=8U
+              AS=4.536N AD=4.536N PS=522U PD=522U
M7       7    53      6      6      N04    W= 80U  L= 4U
+                  AS=720P  AD=720P PS=98U   PD=98U
M8      88    53      9      9      N04    W= 80U  L= 4U
+                 AS=720P  AD=720P PS=98U    PD=98U
M10      6    10     200    200     N04    W= 80U  L= 4U
+                 AS=720P  AD=720P PS=98U    PD=98U
M20      9    20     200    200     N04    W= 80U  L= 4U
+                 AS=720P  AD=720P PS=98U    PD=98U
M11     10    10     200    200     N04    W= 80U  L= 4U
+                 AS=720P  AD=720P PS=98U    PD=98U
M12     20    20     200    200     N04    W= 80U  L= 4U
+                 AS=720P  AD=720P PS=98U    PD=98U
```

APPENDIX III.(Cont.2)

```
M13     13    13    100    100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
M14     14    14    100    100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
M15     15    13    100    100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
M16     16    14    100    100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
M17     20   500    15     100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
M18     10   500    16     100     P08    W=168U  L=8U
+           AS=2.268N AD=2.268N  PS=270U  PD=270U
*****************************  DC BIAS
*IBIAS     100      54     10U
RTEST     100   54    1MEG
MBD     54   54    200     200     N04    W=20U    L=4U
+             AS=180P    AD=180P    PS=38U    PD=38U
MB1     51   54    200     200     N04    W=20U    L=4U
+             AS=180P    AD=180P    PS=38U    PD=38U
MBA     51   51    100     100     P08    W=104U  L=8U
+            AS=1.404N AD=1.404N PS=174U  PD=174U
MB2     52   54    200     200     N04    W=20U    L=4U
+             AS=180P    AD=180P    PS=38U    PD=38U
MBB     52   52    100     100     P08    W=21U   L=8U
+             AS=288P    AD=288P    PS=50U    PD=50U
MB3     53   51    100     100     P08    W=104U  L=8U
+            AS=1.404N AD=1.404N PS=174U  PD=174U
MBC     53   53    200     200     N04    W=4U     L=4U
+             AS=36P     AD=36P     PS=22U    PD=22U
VSHORT   7    11
```