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Adam C. Heiberg for the degree of Master of Science in

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Title: An Ultra Low Voltage Micropower GPS Receiver RF Front-End for Wildlife Tracking

Abstract approved: _____

Terri S. Fiez Kartikeya Mayaram

A fully integrated CMOS GPS receiver RF front end optimized for low power operation is presented. The system operates with a supply voltage down to 250 mV. A prototype has been fabricated in a 0.13μm CMOS process and includes a low voltage LNA, quadrature oscillators, and quadrature mixers. It exhibits an order of magnitude lower power consumption than the best previously published work. The system has a measured gain of 42 dB, a noise figure of 8.6 dB, and an oscillator phase noise of -113.8 dBc/Hz at a 1 MHz offset while consuming a maximum of 580 μW of power and requiring no external components.

An Ultra Low Voltage Micropower GPS Receiver RF Front-End for Wildlife Tracking

by

Adam C. Heiberg

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Adam C. Heiberg, Author

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Academic

I wish to extend my sincere thanks to Thomas Brown for assistance related to a number of facets of my work. These include but are not limited to helpful discussions related to circuit design, PCB design, and Latex usage. In addition, I had the opportunity to serve as Tom's IC layout assistant for a significant amount of time, which provided me with vital experience for my own IC layout during the following year. Another person I wish to thank is James Ayers for a number of useful conversations related to RF circuits and assistance in the lab. Napong Panitantum cannot be thanked enough for the invaluable assistance he provided fixing problems with both Cadence and Mentor Graphics software. I also wish to extend thanks to Farhad Farahbakshian for a number of useful discussions related to oscillators. Steve Meliza, Hector Oporta and the other residents of KEC3040 are very deserving of gratitude for helping to create a wonderful working environment in our office. Finally, I cannot overstate the appreciation I have for my two Major Professors, Terri Fiez and Karti Mayaram. They gave me the opportunity to complete the work discussed here and tirelessly encouraged me to create innovative and unique solutions to the challenges I faced along the way.

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Personal

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1 INTRODUCTION

Consumer electronic devices using global positioning system (GPS) have proliferated the market. Hand held GPS receivers are now a standard consumer electronic device, and many cell phones offer GPS capability. The current generation of low power GPS receivers is used in GPS enabled wrist watches with lithium ion batteries that must be charged daily. Applications requiring prolonged GPS operation in compact, low cost packages still elude commercial designs. The recent rise to prominence of RF CMOS techniques and technology opens new doors in the design of fully integrated, low power receiver front ends for GPS [1]. This new breed of receiver enables long term remote sensing and other isolated applications where long battery life and small size are paramount.

There are two distinct approaches to achieving low power. The first of these is to utilize stacked circuits with current shared by multiple circuit blocks. A common example of current reuse in front end circuits is stacking the LNA and mixer [2, 3]. Another current reuse technique is stacking the mixer and oscillator [4]. The ultimate example of this technique is a GPS receiver front end with close to 100% current reuse and a stacked mixer, oscillator, and LNA [5]. The second technique is to use ultra low voltage circuit designs. Low voltage RF circuit blocks are shown in [6], and a 0.5 V receiver design without an oscillator is presented in [7]. The low supply voltage of these circuits reduces power consumption to a level that is comparable to current reuse designs.

Low voltage design techniques may lack some of the elegance of current reuse, but they ensure compatibility with future low voltage CMOS processes. This is because threshold voltage does not track the reduction in supply voltage with process scaling, making it more difficult to stack transistors with each new process generation [8]. In addition, stacking multiple circuits may require access to the body terminal of NMOS devices. If possible, it is preferable to eliminate this requirement to realize a design that is inexpensive

and portable from one process to the next.

To address the need for a fully integrated low power GPS receiver, this paper presents an ultra low voltage RF front end in standard CMOS. The front end is fully integrated, requiring no external components. It is optimized for low power consumption, allowing use with small, inexpensive batteries. The combination of complete integration and low power consumption provides a solution that is both compact and inexpensive. The RF front end consists of a variable gain LNA, quadrature double balanced mixers, and quadrature oscillators. All of the circuits are optimized for low voltage operation, functioning properly with a power supply of only 250 mV. No supply boosting is required on chip because all of the circuits have been designed for ultra low voltage operation. All biasing is integrated into the IC. As a result, there are only 2 ports, an IF output and a RF input.

The paper is organized as follows. Chapter 2 includes a summary of the requirements of GPS systems and describes the architecture of the front end. Design of the LNA, oscillator, and mixer is described in Chapters 3, 4, and 5, respectively. In Chapter 6, experimental results are presented and compared with recently published work. The paper is concluded in Chapter 7.

2 SYSTEM REQUIREMENTS AND ARCHITECTURE

2.1 Unique Requirements of GPS

The specifications of the L1 GPS band create a unique set of requirements when compared to other common wireless communication systems [9]. Phase noise and linearity are usually two of the most important specifications in a wireless communication system. However, by inspecting Table 2.1 it is clear that phase noise and linearity are of minor importance. Since the signal power is extremely low, a GPS receiver needs to have the highest possible gain as opposed to high linearity. The fact that there are no close-in blockers relaxes the requirements for both linearity and phase noise. The noise figure should be minimized to obtain the best possible SNR. However, the noise figure requirement is not stringent due to the processing gain of the spread spectrum GPS signal [10].

TABLE 2.1: L1 GPS Specifications [11]

Channel Power [dBm]	-128
Processing Gain [dB]	43.1
Center Frequency [GHz]	1.57542
Signal Bandwidth [MHz]	2.046
Closest Blocker [MHz]	9 [10]

2.2 Quadrature Operation

One common method of improving spectral efficiency in communication systems is to utilize a quadrature modulation scheme. In a quadrature scheme, the output is composed

of two terms. One of these terms is generated by modulation with an in-phase carrier while the other term is generated by modulation with a carrier at the same frequency with a 90° phase shift. In this case, the transmitted signal is given by:

$$S(t) = A\cos(\omega t)[data_I(t)] - A\sin(\omega t)[data_Q(t)] \tag{2.1}$$

where $data_I(t)$ is the data stream transmitted on the I channel and $data_Q(t)$ is the data stream transmitted on the Q channel. A quadrature receiver can separate the two terms in (2.1), allowing $data_I(t)$ and $data_Q(t)$ to be resolved from each other and processed separately by the receiver.

The in-phase component of the carrier is modulated by the P code and the quadrature component is modulated by the C/A code. The C/A code is the coarse acquisition code, which is used in typical civilian GPS receivers. The P code, which stands for precise code, is used for high accuracy GPS and may be reserved for military use. GPS uses quadrature modulation to separate the C/A and P codes from each other. Appendix II includes a detailed description of these codes. The implication of quadrature modulation is that a GPS receiver front end must have quadrature oscillators and mixers.

2.3 Additional Requirements

As stated in Section 1, size, power consumption, and cost are key requirements. To ensure the most compact possible solution, a fully integrated design must be realized. Eliminating external components will reduce cost and size. Power consumption is an important consideration because reduced power consumption means that a smaller and less expensive battery can be used, further reducing both size and cost. Also, many GPS receivers utilize an active antenna [9, 12], which integrates the low noise amplifier (LNA) into the antenna module. To create a fully integrated solution, all external components need to either be implemented on the GPS receiver IC or eliminated from the system.

Figure 2.1 illustrates that a typical GPS receiver has a number of external components. In addition to the previously mentioned active antenna, there is often a matching network or balun [13] and external decoupling capacitors. To realize a fully integrated solution, the LNA must be moved from the active antenna into the GPS receiver. The external matching network must also be moved into the receiver, and the design must be implemented with a single-ended input to eliminate the need for an external balun and to reduce pin count. Large on chip decoupling capacitors eliminate the need for external decoupling capacitors. In addition, fully differential circuits with minimal supply noise sensitivity ensure proper operation with minimal decoupling.

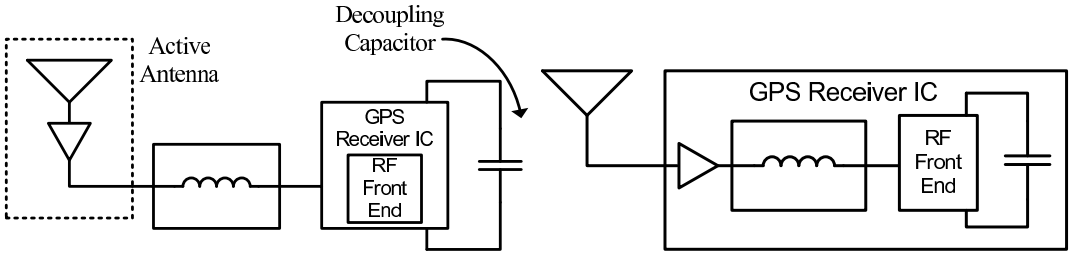


FIGURE 2.1: (a) Typical receiver implementation. (b) Fully integrated receiver.

2.4 Performance Requirements for the Receiver Front End

The key performance specifications for the RF portion of the receiver are gain and noise figure. Image rejection, which is often a critical requirement for receivers, is of minor importance due to the relatively empty spectrum that surrounds the L1 GPS carrier. In addition, linearity is also of minor importance due to the small signal power and the fact that there are no close-in blockers. Finally, phase noise performance is also of only moderate importance [9].

Having high gain in the RF portion of the GPS receiver is important because it

minimizes the noise contribution of all circuit blocks further down the receive chain. The input referred power of noise sources following the front end will be attenuated by the gain of the front end. Thus, their contribution to the system noise figure is drastically reduced [14]. To improve flexibility and immunity to noisy baseband circuitry, the gain of the RF portion of the system should be greater than 30 dB. This means that noise generated in the baseband portion of the system will be attenuated by at least a factor of 1000 when referred to the system's input. If this is the case, it is possible to safely use the RF front end discussed here with any baseband system without worrying about reduced sensitivity due to baseband noise.

Another important consideration related to gain is the dynamic range of the front end. Receivers typically have an automatic gain control (AGC) system to ensure that the receiver's output is near full scale at all times [15]. AGC is generally implemented in the baseband portion of the receive chain using variable gain amplifiers [9, 11]. However, the flexibility of the front end can be improved if it incorporates variable gain. This will improve the overall dynamic range of the system by supplementing the gain adjustment range of the baseband system. In addition, in the unlikely event that a large blocker appears near the carrier frequency or if the carrier itself has significantly more power than expected, the gain can be dynamically reduced to avoid excessive nonlinearity in the front end [16].

Noise figure is one of the most critical considerations in a receiver design because it limits the sensitivity of the receiver. Table 2.2 lists the parameters of L1 band GPS that are relevant to determining the noise figure of the front end. N_0 is the thermal noise power present at the input of the circuit and $\frac{E_b}{N_0}$ is the energy per bit relative to the thermal noise floor. R_b is the data rate in bits per second. The desired sensitivity is taken to be 10 dB below the channel power to ensure reliable operation. The required noise figure for

a receiver can be calculated using [9]:

$$NF_{rec} < sensitivity - \frac{E_b}{N_0} - 10\log(R_b) - N_0 \tag{2.2}$$

From this equation, the maximum noise figure of the entire receive chain must be less than 11 dB.

TABLE 2.2: Sensitivity Parameters

Channel Power [dBm]	-128
Sensitivity [dBm]	-138
R_b [bps]	50
N_o [dBm]	-174
$\frac{Eb}{No}$ [dB]	8

Given that the maximum noise figure for the whole receive chain is 11 dB, it is clear that the RF front end portion of the chain must have a noise figure below 11 dB. An approximate noise budget for a GPS receive chain is given in Table 2.3. If the RF front end has a noise figure of 8 dB, then the overall receive chain noise figure is 9 dB if a 2 bit ADC is used. Since the gain of the RF front end is so high, a receive chain using a 2 bit ADC will have a noise figure of approximately:

$$NF_{rec} \approx NF_{RF} + 1 \tag{2.3}$$

where NF_{RF} is the noise figure of the RF front end and the 1 represents the quantization noise of the ADC.

From (2.3), it can be seen that as long as the noise figure of the RF front end is below 10 dB, the system noise figure will be less than 11 dB. However, to provide some margin for error, the value of NF_{RF} will have an upper bound of 8 dB as shown in Table 2.3, ensuring that the noise figure of the receive chain is never greater than 9 dB.

TABLE 2.3: Noise Budget of GPS Receive Chain

	RF	**Analog Baseband**	**2 bit ADC**
Noise Figure [dB]	8	10	1*
Cascaded NF [dB]	8	8	9
Gain [dB]	30	80	
Cascaded Gain [dB]	30	110	

* ADC quantization noise

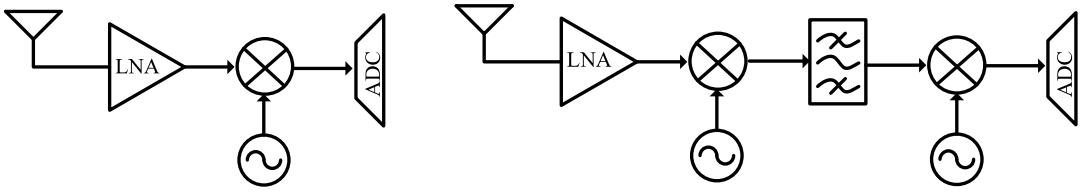
There are a number of other requirements that should be defined to ensure proper operation of the receiver. One of these is tuning range. To compensate for process variations, the LO must have a tuning range of at least 10%. In addition, the power consumption must be as low as possible. A reasonable target for power consumption in this case is 1 mW. One more specification that requires attention is LO phase noise. Phase noise performance better than -80 dBc/Hz in band ensures no compromise in performance [9]. To realize a robust design, the in-band phase noise is specified as -90 dBc/Hz. Finally, to ensure that the system does not radiate an excessive amount of LO noise through the input, the maximum acceptable LO leak through is specified as -70 dBm. These design specifications are summarized in Table 2.4.

TABLE 2.4: Front End Performance Requirements

Noise Figure [dB]	8
Gain [dB]	30
Phase Noise @ 1 MHZ offset $[\frac{dBc}{Hz}]$	-90
LO Tuning Range [%]	10
LO Leakage at input [dBm]	-70

2.5 Receiver Architecture

The L1 GPS band does not require significant channel selectivity, making a direct conversion receiver architecture an attractive option. In addition, a direct conversion architecture is well suited to low power applications due to its simplicity when compared to the more commonly used superheterodyne architecture [17]. Figure 2.2 includes simplified diagrams of superheterodyne and direct conversion receiver architectures. It is clear that the superheterodyne architecture includes significant added complexity in the form of additional mixers and oscillators. This added complexity means that the direct conversion architecture has an inherent advantage in terms of power consumption.



(a) (b)

FIGURE 2.2: (a) Direct conversion architecture. (b) Superheterodyne architecture.

True direct conversion receivers have two major practical problems, flicker noise and DC offset. To mitigate these problems, it is possible to slightly alter the operation of the basic direct conversion topology and create a low intermediate frequency (IF) receiver. In a low IF receiver, the IF frequency is centered at a high enough frequency that flicker noise can be avoided. The IF is still low enough that it can be directly applied to a baseband ADC without any additional frequency translation [17]. By using a low IF receiver, it is possible to obtain the simplicity and efficiency of a direct conversion architecture without the severe practical difficulties.

A block diagram of the front end architecture is shown in Figure 2.3. The area in the dotted line is the focus of this work. The LNA is integrated on chip, eliminating the

need for an active antenna. Note that there are two mixers and a quadrature oscillator to satisfy the previously mentioned requirement for quadrature operation.

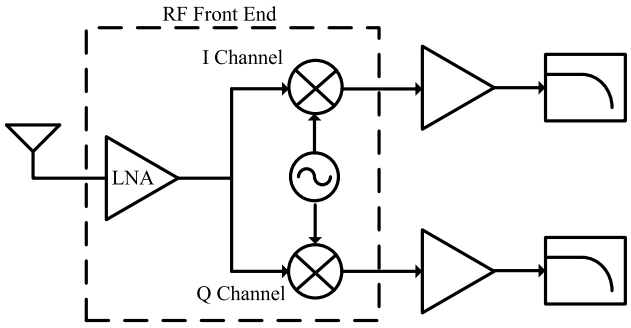


FIGURE 2.3: Receiver topology.

3 LNA DESIGN AND ANALYSIS

An LNA is one of the most important elements in a wireless receiver. It is responsible for providing an input match, which is typically 50 Ω. In addition, the LNA must provide enough gain to make the noise contribution of the mixer and all other components in the receive chain negligible. The LNA is also responsible for reducing the LO leakage present at the input of the system.

Figure 3.1 shows a circuit schematic of the LNA used in this design. The LNA has a number of key design features that enable system integration and low voltage operation. A single ended 50 Ω input port provides a matched input without requiring any external components and using only a single pin. Transformer feedback (L_{in}) is utilized to realize the input match and double the effective transconductance of the first stage. Parasitic feedthrough in the first stage is neutralized by C_{N1} [18], allowing high gain and stability without using the common cascoded LNA structure [19]. A resonant load, consisting of L_1 and C_1, is utilized in the first stage of the LNA as a zero headroom current source, minimizing the supply voltage required for proper operation.

A second gain stage is included in the LNA to increase the gain. As in the first stage, the load is a zero headroom resonant circuit, giving the best possible low voltage operation. In addition, the second stage is neutralized by C_{N2} [16], eliminating the need for a cascode device to further improve low voltage performance. A center tapped inductor (L_2) is used in the load of the second stage, providing a differential output. This reduces sensitivity to common mode noise on the chip and allows the LNA to interface easily with a double balanced mixer. The second stage of the LNA implements a variable gain feature with a cross coupled pair formed by M_3 and M_4. This maximizes the flexibility of the front end as discussed in Chapter 2.

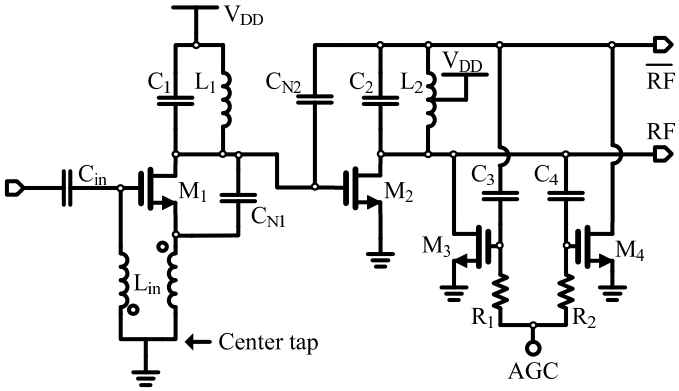


FIGURE 3.1: LNA circuit schematic.

3.1 Input Matching

In the interest of creating a fully integrated system, it is vital to realize the desired input match without using any external capacitors or inductors. One very attractive means of creating a match is to use transformer feedback [18, 20].

One benefit of transformer feedback is that the input impedance is not significantly affected by parasitic impedance connected to the center tap of L_{in}. Consider the circuits in Figure 3.2. The commonly used dot notation signifies the flow of power through the transformer. This means that current flows into the dot on the primary side and it flows out of the dot on the secondary side into a load [21]. In this case, L_{in} is used as a transformer with a turns ratio of 1. L_{in} does not have clearly defined primary and secondary coils. However, it is still possible to deduce the direction of current flow by inspecting the polarity of the voltage at its terminals. The following relationships result from this analysis if the turns ratio is assumed to be 1:

$$I_1 = -I_2 \tag{3.1}$$

$$I_x = I_1 + I_2 = 0 \tag{3.2}$$

Equation (3.2) shows that $I_x = 0$, meaning that no AC current flows through the center tap of L_{in}. As a result, the circuit is insensitive to impedance in series with the center tap. This means that the behavior of the match is not severely affected by bondwire impedance to ground. As a result, the match offers consistent behavior with widely varying bondwire length, eliminating the need to use external components to tune the match frequency.

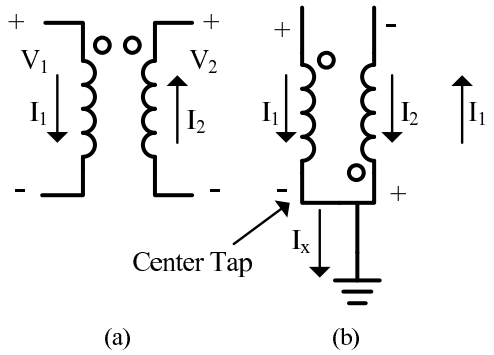


FIGURE 3.2: (a) Voltage and current in a transformer. (b) Voltage and current in a center tapped inductor.

Figure 3.3 illustrates an AC model of the LNA's input. The two inductors in the figure act as a transformer with coupling that is assumed to be perfect. Equations (3.3) and (3.4) describe the operation of the transformer.

$$I_1 = I_2 + \frac{v_g}{j\omega L_{in}} \tag{3.3}$$

$$I_2 = I_1 + \frac{v_s}{j\omega L_{in}} \tag{3.4}$$

where I_1 and I_2 are the currents through the transformer coils, v_g and v_s are the gate and source voltages, L_{in} is the self inductance of each coil, and ω is the frequency in radians per second.

The transformer action effectively doubles the g_m of the input stage by applying

twice the voltage v_{in} across the gate and source terminals of the input transistor M_1 [18]. However, the most important function of the transformer coupling is input matching. Using Figure 3.3 it is possible to evaluate the input impedance, which is given by:

$$Z_{in} = \frac{(4L_{in}\omega^2 C_{gs} + L_{in}\omega^2 C_{in} - 2jg_m L_{in}\omega - 1)j}{\omega C_{in}(2jg_m L_{in}\omega + 1 - 4L_{in}\omega^2 C_{gs})} \tag{3.5}$$

where g_m is the transconductance of M_1. For a matched input condition, the following must be true:

$$Re(Z_{in}) \approx R_{ref} \tag{3.6}$$

$$Im(Z_{in}) \approx 0 \tag{3.7}$$

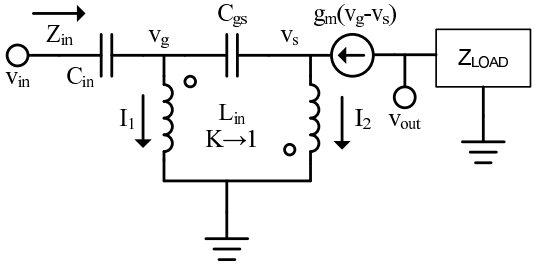


FIGURE 3.3: AC model of the LNA input.

Figure 3.4 is a schematic diagram of the commonly used inductively degenerated LNA. This circuit provides a relatively narrow band match and is generally tuned by an external inductor, which is denoted L_1 in the figure. Because of its narrow bandwidth, the match must be tuned to compensate for variations in process and packaging parasitics. One of the key requirements of this system's input matching is that it must be realized without the use of an external inductor or capacitor. As a result, the match must have very wide bandwidth to eliminate the need for external tuning components.

The transformer feedback matching that is used in this implementation has considerably better wideband behavior than the traditional inductively degenerated LNA. To

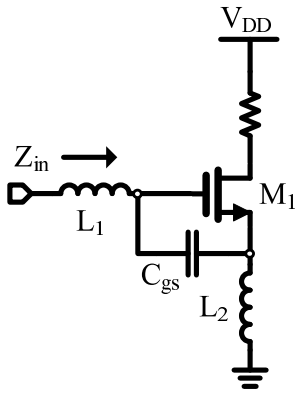


FIGURE 3.4: Inductively degenerated LNA.

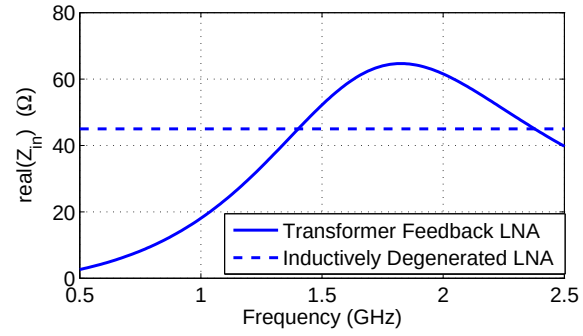
understand why transformer feedback offers significantly better wideband matching than inductive degeneration, it is possible to evaluate the input impedance of both designs and compare the two. The input impedance of the transformer feedback implementation discussed here is given in (3.5). Previous research has focused on the inductively degenerated LNA design, and its input impedance is given by [19]:

$$Z_{in} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}L_2}{C_{gs}} \tag{3.8}$$

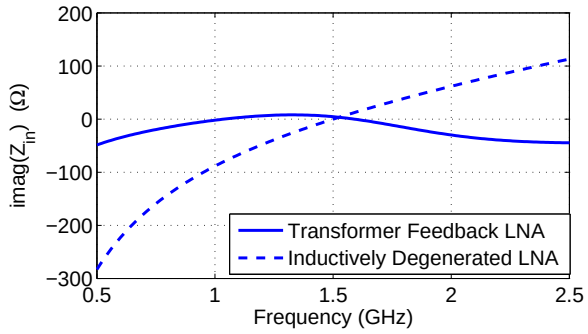
where g_{m1} is the transconductance of transistor M_1, which is shown Figure 3.4.

A plot of the real and imaginary components of the input impedance of both matching schemes is given in Figure 3.5. The requirements for a matched condition are given in (3.6) and (3.7). It is important to note that in a matched condition the imaginary component of the input impedance is very small. The improved wideband performance of the transformer feedback match used in this implementation becomes apparent by inspecting the imaginary component of Z_{in}. In the case of the inductively degenerated LNA, the imaginary component of the input impedance has a single zero crossing, corresponding to a matched condition. It rapidly diverges as the frequency shifts away from resonance.

The opposite occurs in the transformer feedback match. The imaginary component



(a)



(b)

FIGURE 3.5: (a) Real component of Z_{in}. (b) Imaginary component of Z_{in}.

of its input impedance is approximated by:

$$Im(Z_{in}) \approx \frac{L_{in}}{\frac{1}{\omega} - 4\omega C_{gs} L_{in}} \tag{3.9}$$

where C_{gs} is the gate to source capacitance of M_1 and L_{in} is the inductance of the transformer as shown in Figure 3.1. It has three zero crossings and evaluates to a relatively small value for a wide range of frequencies. As a result, the bandwidth of the match is extended because it's imaginary component does not rapidly diverge from zero as in the case of the inductively degenerated LNA. Note that one of the zero crossings is not shown in the figure because it occurs at a higher frequency than is shown in the graph.

Figure 3.6 is a plot of the predicted $|S11|$ for each of the two matching schemes. Both input matches are dependent on device transconductance, which is a function of

power. To ensure an accurate comparison, the curves have been generated with both matching schemes using the same transconductance and tuned to the same frequency. The -10 dB bandwidth of the transformer feedback match is approximately twice as large as the -10 dB bandwidth of the inductive degeneration match. The wide bandwidth of the transformer feedback match eliminates the need for external tuning components, making it an excellent choice to realize a fully integrated solution.

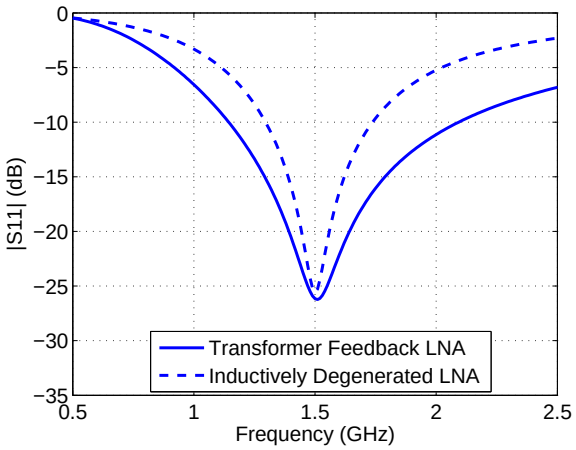


FIGURE 3.6: $|S11|$ for inductive degeneration and transformer feedback input matching.

3.2 C_{gd} Cancellation

The low voltage operation of the receiver means that input isolation cannot be achieved by cascoding as is often done. However, excellent input isolation can be realized by using neutralization [16, 18]. The principle of neutralization is to cancel the parasitic C_{gd} path with an equal and opposite transfer of charge. Figure 3.7 illustrates the concept of neutralization. A voltage applied at v_g will cause a charge Q_{gd} to flow out of the gate and into C_{gd} to satisfy conservation of charge. If a capacitor called C_N is connected between the gate and an inverted replica of the drain voltage, then a charge with opposite polarity, denoted by Q_N will flow into the gate node. If C_N and C_{gd} are equal, then Q_{gd}

and Q_N must also be equal and no net charge will flow into the gate, effectively eliminating the effect of the C_{gd} signal path.

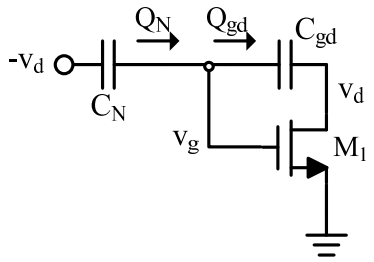


FIGURE 3.7: Basic concept of neutralization.

It is important to note that this cancellation will not be perfect, even if C_{gd} and C_N are perfectly matched. This is due to the finite gain of the gain stage. The error can be calculated in the following way where A is the gain and C_N and C_{gd} are assumed to be identical:

$$Q_{gd} = C_{gd}(V_g - V_d) \tag{3.10}$$

$$Q_N = C_N(V_g + V_d) \tag{3.11}$$

$$V_d = -AV_g \tag{3.12}$$

$$Q_{gd} = C_{gd}(V_g + AV_g) \tag{3.13}$$

$$Q_N = C_N(V_g - AV_g) \tag{3.14}$$

$$\frac{Q_{gd}}{Q_N} = \frac{C_{gd}(V_g + AV_g)}{C_N(V_g - AV_g)} = \frac{(V_g + AV_g)}{(V_g - AV_g)} \tag{3.15}$$

For large A, (3.15) will evaluate to -1, providing perfect neutralization. As the gain is reduced, significant mismatch will occur and the neutralization will become less effective. However, in this case, both gain stages have adequate gain to realize effective neutralization. In addition, to ensure the best possible cancellation, both C_{N1} and C_{N2} are implemented with dummy MOSFETs, providing excellent matching.

To maximize LNA stability and reduce LO leakage at the input, both stages of the LNA utilize neutralization. Figure 3.8 illustrates how neutralization is implemented in each of the two gain stages. Stage 1 has a single ended output, meaning that the simple neutralization scheme presented in Figure 3.7 cannot be implemented since it depends on an inverted output. However, the transformer used for input matching insures that the voltage at the source of M_1 is always 180° phase offset from the gate voltage. As a result, the desired charge flow can be realized by connecting C_{N1} across the drain and source terminals of M_1 [18]. This capacitor provides a path to deliver the appropriate neutralizing charge to the gate terminal of C_{gd1}. The movement of positive charge is denoted by Q. The exchange of charge between C_{gd1} and C_{N1} ensures that the total charge at both the gate and drain terminals of M_1 remains unchanged, effectively eliminating the signal path associated with C_{gd1}.

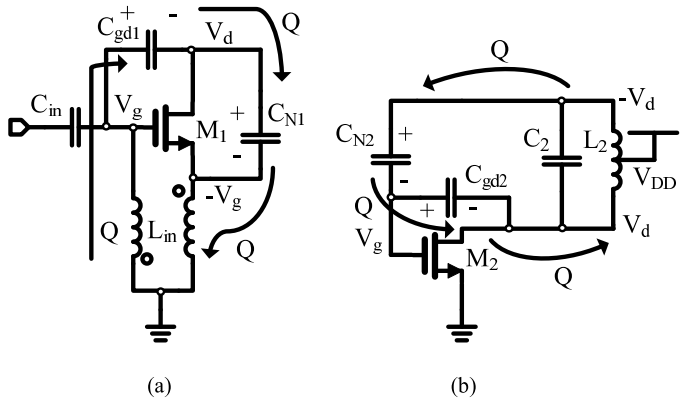


FIGURE 3.8: (a) Stage 1 neutralization. (b) Stage 2 neutralization.

The output of the LNA's second stage is differential, meaning the neutralization

scheme described in Figure 3.7 can be used. As in the case of the first stage, Q denotes movement of positive charge through the circuit. An exchange of charge between C_{gd2} and C_{N2} ensures that there is zero net charge transferred to any terminal of M_2 or to the load. As a result, the affect of the C_{gd2} path is eliminated.

3.3 Gain and Noise Figure of the First Stage

The first stage of the LNA is the most critical part of the system in terms of noise performance. High gain in the first stage will ensure that other noise sources in the system have marginal impact. In addition, any noise sources in the first stage will not be attenuated when referred to the input, meaning that they have a severe effect on the system noise figure [22]. As a result, for the best possible noise performance, the first stage of the LNA should have both high gain and low noise.

Figure 3.3 can be utilized to determine the input to output gain of the LNA's first stage. The load is assumed to be some arbitrary impedance, although in this case a parallel resonant network is used. Using KCL, it is possible to obtain the result found in (3.16). It is important to note from this equation that the effective transconductance, G_m, is equal to $2g_m$ where g_m is the transconductance of M_1. As expected, the gain is directly proportional to the product of G_m and Z_{LOAD}.

$$A = \frac{-2g_m Z_{LOAD} L_{in} C_{in} \omega^2}{L_{in} C_{in} \omega^2 - 2g_m L_{in} j\omega - 1 + 4L_{in} C_{gs} \omega^2} \tag{3.16}$$

Evaluating the noise figure of the first stage requires defining which noise sources should be considered. In the interest of simplicity, only two noise sources will be accounted for. These are the thermal noise of transistor M_1 and the thermal noise of the load.

The load must be defined to determine its noise contribution. As shown in Figure 3.1, the load is a parallel LC network consisting of L_1 and C_1. The primary noise

source in this circuit is thermal noise from the inductor's series resistance. This resistance and its noise generator are shown in Figure 3.9 and are denoted RL_{LOAD} and $\overline{V_{NL}^2}$, respectively. The noise power of this noise generator is amplified by the load's Q squared, so the noise power at the output from this source can be much larger than expected. The noise generator associated with the inductor's series resistance is defined as [23]:

$$\overline{V_{NL}^2} = 4K_BTR \tag{3.17}$$

In the above equation, K_B is the Boltzmann constant, T is the absolute temperature, and R is the resistance. In this case, the resistance is the series resistance of L_1.

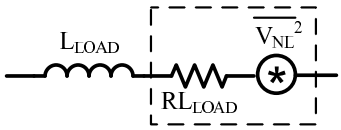


FIGURE 3.9: Inductor noise model.

The classic thermal noise model for MOS transistors is given by [24, 25]:

$$\overline{I_N^2} = 4K_BT\gamma g_{d0} \tag{3.18}$$

where g_{d0} is the drain conductance with zero bias and γ represents excess thermal channel noise. A considerable amount of research has focused on γ [26, 27], however it is still not well understood [28] and is highly process dependent.

Figure 3.10 includes a schematic of the first stage of the LNA with the previously discussed noise sources. In addition, the noise of the source resistance is shown. This circuit can be used to evaluate the approximate noise figure of the LNA:

$$F = 1 + \frac{(Z_{in} + R_s)^2}{4(\omega\ L_{in}g_m)^2\ \overline{V_{Nin}^2}} \left[\left| \frac{\overline{I_N^2}}{(2jg_m\omega L_{in} + 1)^2} \right| + \overline{P_{Nload}^2} \right] \tag{3.19}$$

where Z_{in} is the input impedance of the LNA, R_s is the source resistance connected to the input, and g_m is the transconductance of M_1. In the above equation, $\overline{I_N^2}$ is the thermal noise generator of M_1, $\overline{V_{Nin}^2}$ is the noise generator of the source, and $\overline{P_{Nload}^2}$ is

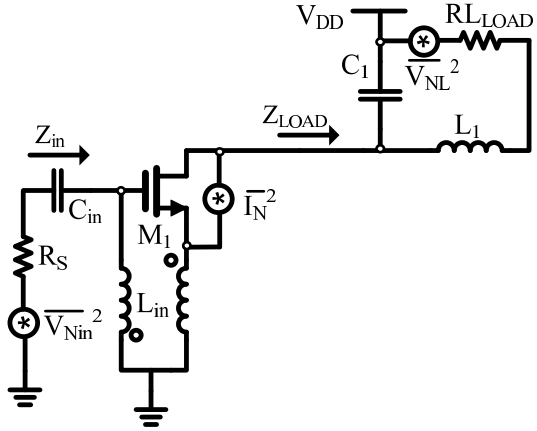


FIGURE 3.10: Schematic of the LNA input stage with noise sources.

the noise power of the load. It is possible to simplify this relationship with the following approximation:

$$F \approx 1 + \left(\overline{I_N^2} + \overline{P_{Nload}^2}\right) \frac{(z_{in} + R_s)^2}{4(\omega L_{in} g_m)^2 \ \overline{V_{Nin}^2}} \tag{3.20}$$

The second term in (3.20) is the output noise power due to the MOS thermal noise generator and the third term is the noise due to the parasitic load resistance. It is important to note that increasing the g_m of M_1 will reduce the noise contribution of both the MOS thermal noise and the load thermal noise.

Equations (3.21) and (3.22) describe the noise behavior of the load. In (3.21), $\overline{V_{NL}^2}$ is the noise generator of the load, which is described in Figure 3.9 and given by (3.17).

$$\overline{P_{Nload}^2} = \left| \frac{Q^2 \ \overline{V_{NL}^2} \ L_{load}}{Z_{LOAD}^2} \right| \tag{3.21}$$

$$Q = \frac{\sqrt{\frac{L_1}{C_1}}}{RL_{LOAD}} \tag{3.22}$$

3.4 Variable Gain

The second stage of the LNA includes a variable gain capability. A differential output is used on this stage, making a negative conductance cross coupled pair a convenient way to adjust the gain. Figure 3.11(a) is a schematic of the variable gain circuit. It looks very much like a conventional NMOS cross coupled oscillator. As a result, it is important to consider how the variable gain circuit affects the LNA's stability.

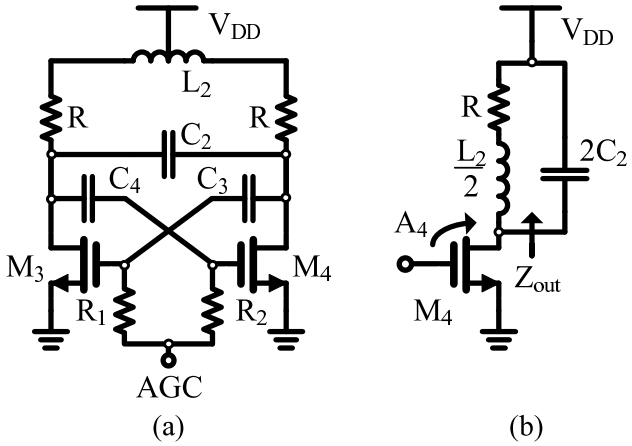


FIGURE 3.11: (a) Variable gain circuit in second stage of LNA. (b) AC half circuit of variable gain circuit.

Figure 3.11(b) is a half circuit representation of the variable gain system. This half circuit can be used to determine the loop gain and stability of the system. The half circuit is a common source amplifier with a resonant load. The gain of this amplifier configuration is:

$$A_4 = -g_{m4} Z_{out} = A_3 \tag{3.23}$$

where g_{m4} is the transconductance of M_4 and Z_{out} is the output impedance. A_4 is shown in Figure 3.11(b), and it represents the gate to drain gain of transistor M_4. A_3 is the gate to drain gain of M_3 and is equal to A_4 due to the symmetrical nature of the circuit. Z_{out}

is the output impedance, which is shown in Figure 3.11(b) and is given by:

$$Z_{out} = \frac{R + j\omega\frac{L_2}{2}}{1 + 2j\omega C_2(R + j\omega\frac{L_2}{2})} \tag{3.24}$$

where R represents the parasitic series resistance of the inductor L_2.

The loop gain of the variable gain circuit can be determined by inspecting Figure 3.11(a). If the signal path is traced around the loop formed by the gate and drain terminals of M_3 and M_4, it can be seen that the loop gain is:

$$A_{LOOP} = A_3A_4 = g_{m3}g_{m4}\left(\frac{R + j\omega\frac{L_2}{2}}{1 + 2j\omega C_2(R + j\omega\frac{L_2}{2})}\right)^2 \tag{3.25}$$

To ensure that oscillation does not occur and stability is maintained, the loop gain of the cross coupled pair must be less than 1, resulting in the following requirement:

$$|A_{Loop}| < 1 \tag{3.26}$$

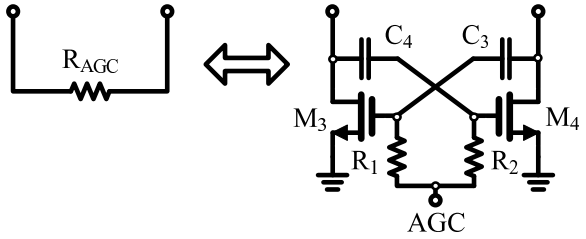


FIGURE 3.12: (a) Simple negative resistor representation of the variable gain circuit. (b) Negative resistance generated by M_3 and M_4 for variable gain.

The gain of the second stage of the LNA can be determined by representing the cross coupled pair consisting of M_3 and M_4 as a negative resistance. Figure 3.12 shows this relationship. The value of this resistance is:

$$R_{AGC} = \frac{-2}{g_m} \tag{3.27}$$

where g_m=g_{m3}=g_{m4}. The value of R_{AGC} is adjusted by tuning the voltage denoted AGC in Figures 3.11(a) and 3.12(b). By tuning this voltage and adjusting R_{AGC}, it is possible to adjust the gain of the LNA.

A simplified schematic of the second stage of the LNA with the adjustable gain circuit represented as a simple resistance is shown in Figure 3.13(b). The gain of this circuit is given by:

$$A = 2g_{m2}Z_{out2} \tag{3.28}$$

where Z_{out2} is the impedance to common mode at the drain of M_2 as shown in Figure 3.13(a). The additional factor of 2 represents the voltage doubling of the signal across differential inductor L_2. Z_{out2} is determined by L_2, C_2, the parasitic resistor R, and the negative resistance R_{AGC} and is given by:

$$Z_{out2} = \frac{R_{AGC}(2R + j\omega L_2)}{2R + 2R_{AGC} + 4j\omega R_{AGC}RC_2 - 2\omega^2 R_{AGC}L_2C_2 + j\omega L_2} \tag{3.29}$$

The above equation can be rewritten in terms of transconductance as follows by substituting (3.27):

$$Z_{out2} = \frac{2(2R + j\omega L_2)}{4 + 8j\omega RC_2 - 4\omega^2 L_2C_2 - 2g_mR - j\omega g_mL_2} \tag{3.30}$$

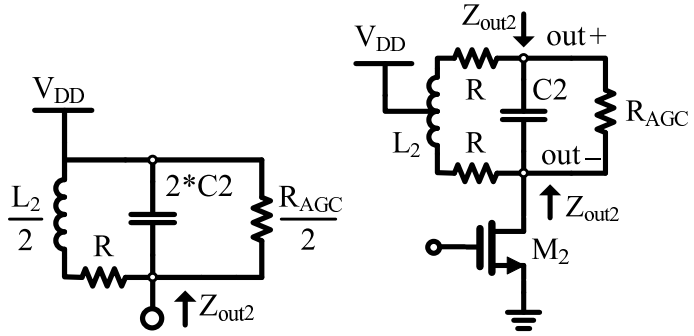


FIGURE 3.13: (a) Output impedance to common mode. (b) Simplified schematic to analyze gain of stage 2.

The gain can be increased by increasing the tuning voltage applied at node AGC. However, it is important to ensure that the AGC voltage is not increased to the point that g_{m3} and g_{m4} are large enough to destabilize the circuit, which will occur if Z_{out2} is

negative. This condition can be avoided by ensuring that the condition specified in (3.26) is not violated.

3.5 Summary of LNA Design

The key design requirements for the LNA are low voltage operation and high gain. To meet the requirement for high gain, a 2 stage LNA topology with resonant loads on both stages has been chosen. Figure 3.1 includes a schematic of the LNA used in this implementation. The first stage of the LNA provides a 50 Ω input match and a significant amount of gain. The second stage of the LNA provides additional gain and creates an interface to a balanced mixer.

A number of key innovations have been included in the design of the LNA. One is that both stages have been neutralized. Due to the low voltage requirement of the system, cascoding cannot be used to provide reverse isolation in the LNA's gain stages. As a result, to achieve both high gain and good reverse isolation, a novel LNA design with multistage neutralization, implemented with capacitors C_{N1} and C_{N2}, has been created. The development of a wideband input match based on inductor L_{in} is another innovative feature. This wideband match eliminates the need for external components to tune the match frequency. Another key innovation of the LNA design is the inclusion of a variable gain capability, which is realized by the AC cross coupled pair formed by transistors M_3 and M_4. This maximizes the dynamic range of the front end. In addition, it drastically improves the LNA's flexibility by allowing the LNA to be tuned for either high gain or high linearity depending on the signal present at the system's input.

4 VCO DESIGN AND ANALYSIS

The VCO generates a frequency tone which is used to down convert the RF input to a desired IF or baseband frequency. Proper operation of the VCO is crucial to ensuring that the RF input can be converted to a lower baseband frequency for analog and digital signal processing. In many cases, the VCO is one of the largest consumers of power [29]. As a result, it is one of the most critical blocks due to the power constraints in this design.

The basic topology that has been chosen for the oscillator is a differential Colpitts design [20, 29]. Colpitts oscillators have an inherent advantage in terms of noise performance over traditional cross coupled VCOs [30] because noise is injected into the LC tank when the magnitude of the impulse sensitivity function is relatively small [31]. The differential nature of the structure has some key benefits. In this case, a differential output is needed to drive a balanced mixer. In addition, a differential structure has excellent immunity to common mode noise and supply or ground impedance [20]. The differential Colpitts structure has another important benefit over a traditional single ended Colpitts design. Colpitts oscillators often have problems with reliable startup, which means that ensuring reliable operation requires additional power. The complementary nature of the signals present in a differential topology implies that the effective G_m and loop gain can be increased without significantly increased power consumption [20].

A schematic of the VCO design used in this implementation is shown in Figure 4.1(a). A traditional single transistor Colpitts topology is shown in Figure 4.1(b) for comparison. Transistors M_1 and M_2 are the core active devices of the oscillator, corresponding to transistor M_c in the traditional Colpitts implementation. Capacitors C_{FB} and C_G provide the feedback that defines the Colpitts topology. Inductor L_2 acts as a zero headroom current source, corresponding to I_{DC} in the traditional Colpitts implementation. The area is minimized and differential operation is assured by utilizing center tapped

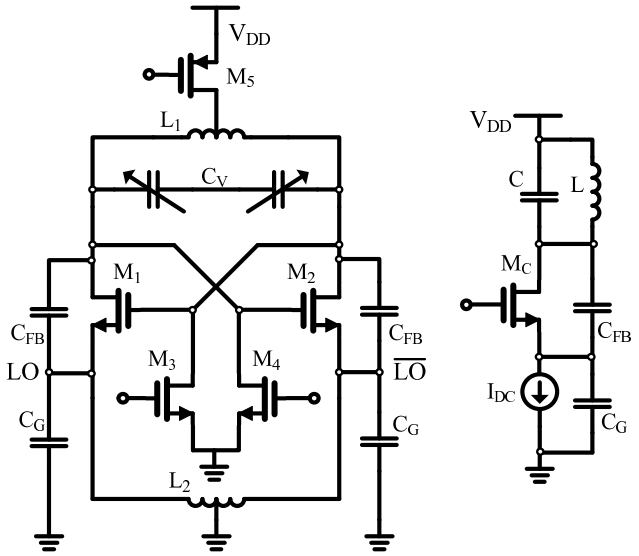


FIGURE 4.1: (a) Circuit schematic of VCO. (b) Traditional Colpitts oscillator.

inductors for L_1 and L_2. Frequency tuning is realized with a pair of MOS varactors, which are denoted C_V in the schematic.

A method for coupling two differential Colpitts oscillators is described in [20]. However, this method is not optimal for low voltage operation because it involves stacking multiple transistors. To solve this problem, an alternate solution consisting of transistors M_3 and M_4 has been used to force quadrature operation. This method has been described in [32, 33] for standard cross coupled oscillators, but this is the first time it has been used in a Colpitts design.

Low voltage oscillators typically have very poor supply noise rejection because their sensitive LC tanks couple directly to the supply. In addition, these types of circuits generally have no means of amplitude and power control. In this application, limiting power and robust performance in the presence of a varied and noisy supply are key design requirements. Supply noise rejection is particularly important because one goal of the design is to eliminate the requirement for large external decoupling capacitors. Transistor M_5 provides a solution to both of these concerns. It limits the oscillator's power and it

provides isolation from supply noise.

To reduce the severity of the mixer's loading on the oscillator, the LO output is taken to be the capacitively divided feedback nodes denoted LO and $\overline{LO}$ in Figure 4.1(a). Nodes LO and $\overline{LO}$ are only moderately sensitive to loading due to the low Q of the resonant circuit at the bottom of the oscillator. This is a very unique feature of the design since the LO output is exclusively taken to be the drain terminals of M_1 and M_2 in conventional Colpitts oscillators. This change reduces the amplitude of the LO signal applied to the mixer and necessitates the use of the passive LO peaking network described in Chapter 5. However, this is a critical change to make because it eliminates the need to use an LO buffer, which is typically used to isolate the sensitive oscillator nodes from the mixer. The importance of eliminating the LO buffer is twofold. A LO buffer requires a significant amount of power when running at high speed. In addition, it is very difficult to realize a functional LO buffer with a low supply voltage. As a result, eliminating the LO buffer reduces power consumption and improves low voltage operation.

4.1 Low Voltage Considerations

As discussed previously, the GPS receiver described here must be able to operate at extremely low voltages. As a result, the oscillator's swing must be very large relative to the supply voltage. The resonant components in the oscillator allow it to float between the supplies, effectively increasing the supply voltage. Consider the source terminals of M_1 and M_2. These nodes can actually float below ground since their ground connection is made through an inductor. A similar situation occurs at the drain terminals of M_1 and M_2, the presence of L_1 allowing them to float above the drain of the current source, M_5. This means that extremely low voltage functionality can be realized without compressing the V_{SD} of M_5 and compromising its operation.

Another consideration related to low voltage operation is whether to use NMOS or

PMOS transistors in the oscillator. It is possible to realize better low voltage operation with NMOS transistors. NMOS transistors typically have a lower threshold voltage than comparable PMOS transistors. In addition, carrier mobility in NMOS transistors is generally significantly higher than in PMOS transistors. The result of these factors is that the V_{gs} of M_1 and M_2 can be reduced if NMOS devices are used, permitting lower voltage operation. One final benefit of NMOS devices is that they generally have higher g_m. This increases the startup loop gain in the oscillator, ensuring reliable startup.

4.2 Loop Analysis

An analysis of the oscillator loop is very important because it provides insight into the frequency range over which the oscillator will function properly. In addition, since there are two resonant circuits, it is important to analyze the loop to ensure that only one of the resonant circuits peaks when the loop gain is greater than 1. If both networks resonate when the loop gain is greater then 1, then the oscillator will have two resonant frequencies for a given tuning voltage. As a result, the Q of the bottom tank circuit must be relatively low to ensure that the oscillator behaves in a predictable manner.

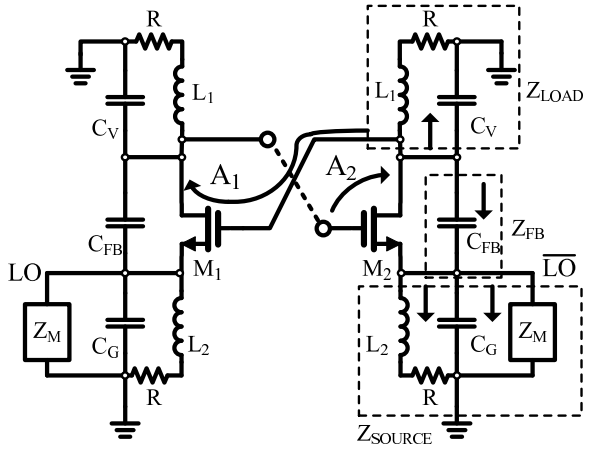


FIGURE 4.2: VCO loop analysis.

Figure 4.2 shows the oscillator with the loop broken for analysis. Z_M is the load presented by the mixer. It is important to include this loading in the analysis to ensure that it doesn't have a detrimental effect on the performance of the oscillator. Transistors M_3 and M_4 are neglected because they are not part of the oscillator's core. The gate to drain gain of M_1 and M_2 is given by A_1 and A_2, respectively.

$$A_1 = A_2 = A_N \tag{4.1}$$

The total loop gain is the product of A_1 and A_2.

$$A_{LOOP} = A_N^2 = A_1 A_2 \tag{4.2}$$

A_N can be determined by analyzing a half circuit of the oscillator.

$$A_N = \frac{-g_m Z_{LOAD} Z_{FB}}{g_m Z_{FB} Z_{SOURCE} + Z_{FB} + Z_{LOAD} + Z_{SOURCE}} \tag{4.3}$$

where g_m is the transconductance of M_1 and M_2 and the impedances are defined in Figure 4.2. In this case, the parasitic resistor R has been added in series with each inductor to increase the accuracy of the analysis. If this resistance is neglected, then the Q of the resonant circuits is infinitely high and the results are very inaccurate.

The startup gain and the resonant frequency of the oscillator can be obtained from (4.2) and (4.3). In theory, a loop gain greater than unity should ensure startup [16]. However, to realize a robust design the minimum loop gain should be at least 1.5. The resonant frequency can be determined by evaluating the phase of the loop response. The oscillator will find a steady state operating point when the loop phase shift is 0° [34].

4.3 Phase Noise Considerations

The Colpitts topology does an excellent job reducing the effect of noise sources in transistors M_1 and M_2. However, the tail current source M_5 can cause significant noise

problems. Noise from the tail source at even harmonics of f_0 will appear at the output. To eliminate noise at higher order even harmonics a capacitor is connected to AC ground at the drain of M_5 [30] as shown in Figure 4.3. This leaves flicker noise as the primary noise source of concern in M_5. Properly sizing M_5 significantly reduces its flicker noise contribution.

Another key noise consideration is ensuring that significant noise is not coupled into the oscillator through the gate of M_5. This means that special care must be taken to ensure that the bias circuits associated with the oscillator have excellent noise performance. Noise in the bias can be reduced by increasing device size and reducing transconductance. This is particularly important if a high gain current mirror is used to reduce power in the bias network. Noise power from the bias circuit is multiplied by the gain of the current mirror squared as shown in Figure 4.3. Of particular concern is flicker noise since high frequency noise can be reduced by the presence of C_T and by simply bandlimiting the bias circuits.

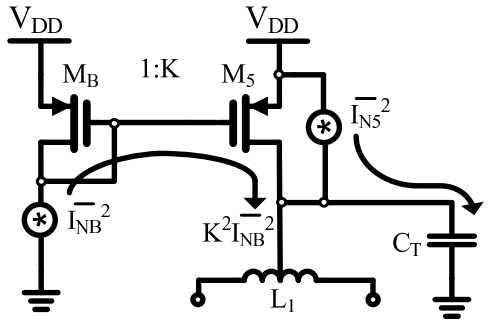


FIGURE 4.3: Effect of tail capacitor and bias noise.

One very important practical benefit of the presence of M_5 is isolation of the oscillator from supply noise. Without M5, supply noise can couple directly into the tank of the oscillator. In this case, one design goal is to eliminate the need for large decoupling capacitors, so immunity to power supply noise is a very important consideration.

4.4 Summary of VCO Design

The VCO has been optimized for robust operation with minimal power consumption at very low voltages. To achieve the best possible noise performance, a Colpitts oscillator topology has been chosen [31]. The oscillator is fully integrated, using a pair of differential inductors for reduced area and MOS varactors for frequency tuning.

A number of innovative design features can be found in the oscillator. Low voltage oscillators typically have a direct connection between the sensitive LC tank and either the power supply or ground, making them very sensitive to supply noise. Low supply noise sensitivity and minimal power consumption are both key requirements of this design, requiring the presence of transistor M_5, which is shown in Figure 4.1(a). Low voltage quadrature operation is achieved by adapting a scheme commonly used in cross coupled oscillators to the Colpitts topology. The design utilizes a direct connection between the VCO and mixer. This eliminates the need for a LO buffer, reducing power consumption and improving low voltage operation.

5 MIXER DESIGN AND ANALYSIS

As in the case of the LNA and the VCO, low power consumption and low voltage operation are the two defining requirements for the mixer. Low voltage mixers are very challenging because traditional mixers generally rely on stacking multiple transistors as illustrated in Figure 5.1(a). To ensure proper operation, the V_{DS} of the transconductor must be at least 200 mV, whereby the peak LO voltage is at least 500 mV. To avoid limiting the minimum supply voltage in the mixer an alternative topology is needed.

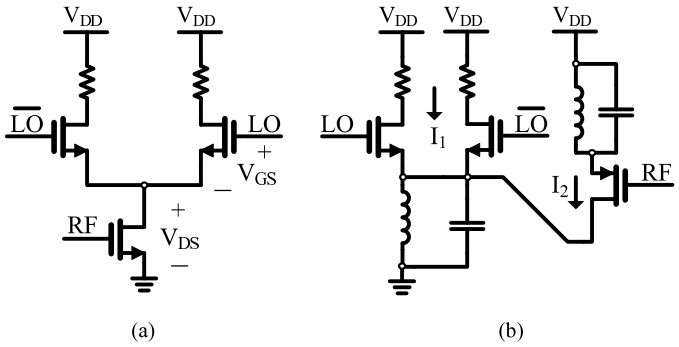


FIGURE 5.1: (a) Traditional single-balanced mixer. (b) Folded single-balanced mixer.

To improve linearity and low voltage operation, folded mixers have become popular. It is possible to avoid stacking transistors with a folded mixer [6], however, folding the circuit adds additional current branches. Figure 5.1(b) shows an example of this technique. The total current is now the sum of I_1 and I_2. I_1 is considerably less than I_2 in most cases. Regardless, there is an additional current flowing in the circuit when compared with the standard single-balanced mixer shown in Figure 5.1(a).

For the best possible low voltage and low power operation, a switched transconductor mixer [35] has been selected for this design. Figure 5.2 provides a schematic of the mixer. The switched transconductor mixer addresses the concerns related to the standard stacked mixer and the folded mixer discussed previously. Low voltage operation is assured

to be excellent since there is no transistor stacking, and current draw is minimized because there is only a single current path.

It is evident from the schematic that the mixer has a double-balanced implementation. In this case, it is convenient to utilize a double-balanced design since complementary RF and LO signals are available. A double-balanced mixer offers the benefit of high isolation between the IF output and both the RF input and the LO input [16]. As a result, the signal appearing at the IF port is very clean, helping to ensure the most accurate possible baseband signal. One other important note is that the mixer is loaded resistively, meaning that the output common mode voltage and output impedance are easily defined.

In the interest of reducing power, the design does not use a LO buffer as in a traditional switched transconductor mixer. Instead, a passive peaking network, consisting of L_{PEAK} and C_{PEAK}, is used. This network has a relatively low Q of approximately 3, so it provides some voltage gain without causing a significant change in the oscillator's loop behavior. The presence of this peaking network is required by the relatively small amplitude of the LO signal, which is a result of the LO signal being taken at a different node than in a typical Colpitts oscillator as described in Section 4. The innovative interfacing of the mixer and oscillator eliminates the need for a LO buffer, reducing power consumption and improving low voltage operation.

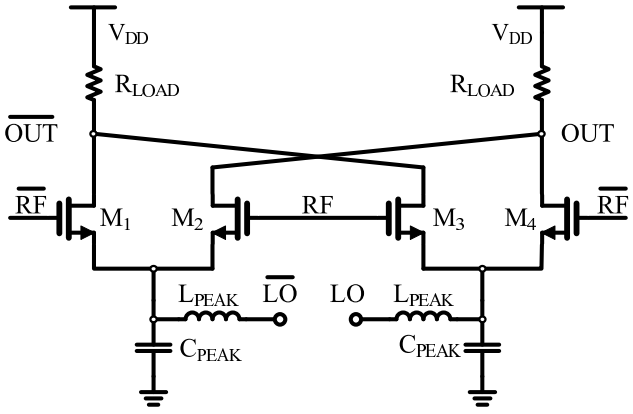


FIGURE 5.2: Double-balanced switched transconductor mixer circuit schematic.

5.1 Low Power Performance Optimization

As discussed previously, the switched transconductor mixer has some inherent advantages for low voltage, low power applications. However, to ensure the best possible performance, it is important to consider optimizing transistors M_1-M_4.

According to [35], the conversion gain of the switched transconductor mixer is proportional to the transconductance of M_1-M_4. As a result, the mixer should have the highest possible transconductance for a given amount of current. The quantity $\frac{g_m}{I_D}$ is maximized in weak inversion [36, 37], so using weakly inverted devices will allow the desired transconductance to be realized in the most efficient way.

The mixer's gain was simulated with constant current and a wide variety of transconductor device sizes to verify that the prediction made in the previous paragraph is correct. By inspecting the simulation results in Figure 5.3, it becomes clear that properly sizing the switched transconductors such that they are in weak inversion yields a gain improvement of 6+ dB when compared to conventional strong inversion biasing.

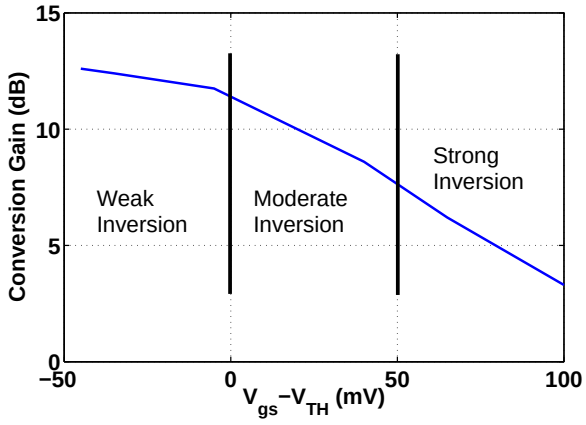


FIGURE 5.3: Simulated conversion gain vs. transconductor operating region.

There is another benefit to operating the switched transconductors in weak inver-

sion. Assuming constant g_m in the switched transconductors, the noise performance will be improved significantly in weak inversion when compared to an implementation using devices in strong inversion. Flicker noise is inversely proportional to device size, and a weakly inverted device will be considerably larger than a strongly inverted device with identical g_m. In addition, the thermal noise, which is given in (3.18), will be reduced because the value of γ will be approximately 25% smaller in weak inversion [37].

5.2 Summary of Mixer Design

For the best possible low voltage and low current operation, a switched transconductor mixer is used in this implementation. It differs from a traditional switched transconductor realization in two important ways. The LO buffer has been eliminated and replaced by inductor L_{PEAK} and capacitor C_{PEAK} as shown in Figure 5.2. This improves the low voltage operation of the circuit and reduces power consumption. Additionally, the transconductors in the mixer have been optimized for low power operation. This results in a significant performance improvement with reduced power consumption.

6 EXPERIMENTAL RESULTS

The GPS RF front end has been fabricated in a standard 1 poly 8 metal 0.13μm CMOS process with MIM capacitors. Figure 6.1 is a photo of the die. No isolated NMOS devices were used, eliminating the need for a triple well process. All pins are fully ESD protected. In addition, on-chip RC clamps are used on all supplies to maximize ESD survivability. A conventional pad ring occupies the perimeter of the chip, ensuring that there are no special considerations related to the wirebonding. The chip was bonded in a MLF48 package, which is a standard leadless QFP type package.

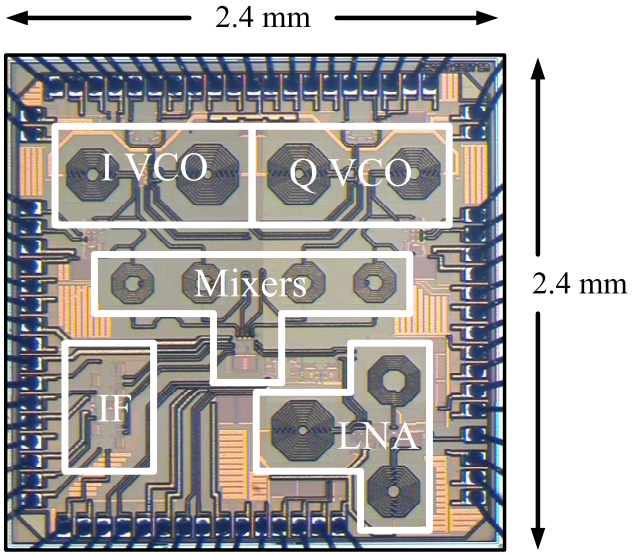


FIGURE 6.1: Die photo.

A conventional FR4 circuit board was used for lab testing. FR4 is the least expensive and most commonly used PCB dielectric, so it is vital to verify that the design works properly with this material. Large decoupling capacitors are located on the die, and the input matching network is fully integrated. As a result, no external components are required by the chip, reducing overall system size and cost. All RF signals on the board are routed as 50 Ω transmission lines to ensure the best possible signal integrity. In

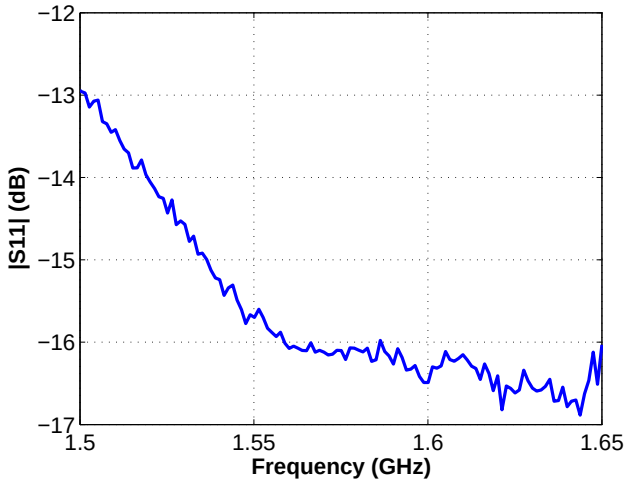
addition, differential signals are used everywhere except the RF input to further improve signal integrity and improve immunity to common mode interference. All connections utilize SMA connectors to ensure excellent noise performance and good high frequency characteristics.

Three supply voltages have been used to verify the functionality of the front end. The nominal supply voltage is 400 mV. However, the system exhibits excellent performance with the supply reduced to only 250 mV. The figures in this section provide measured data with supply voltages of 400 mV, 300 mV, and 250 mV. If the supply is reduced below 250 mV, the oscillator's startup behavior becomes erratic. In addition, there is a constant transconductance bias in the LNA which has trouble functioning properly below 250 mV.

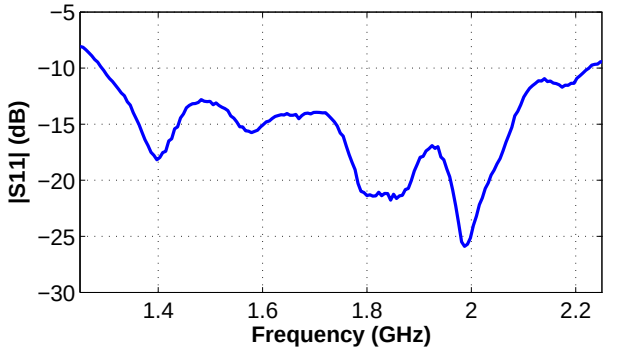
Input matching was tested using an HP8720ES S parameter network analyzer. The measured $|S11|$ is shown in Figure 6.2(a). At the L1 band center frequency, the input matching is approximately -16 dB. It is important to note that no external components are used to tune the match. Figure 6.2(b) includes a wider bandwidth plot of the measured $|S11|$. It is interesting to note that the input matching is better than -10 dB for a bandwidth of nearly 1 GHz. This wideband behavior makes this match very attractive for an integrated multiband receiver. With some further development, it may be possible to extend the match bandwidth to cover the 900 MHz and 2.4 GHz ISM bands.

The noise figure was measured with an IF frequency of 10 MHz. As a result, there is no flicker noise contribution to the noise figure. It is possible to reduce the IF center frequency to 4 MHz with no significant change in the measurements. A Tektronix RSA3308A spectrum analyzer was used to obtain the results. The measured noise figure is shown in Figure 6.3. Measured results are reported for the single sideband (SSB) noise figure since it is the most relevant measure of noise in this system.

The gain of the front end was measured at a 10 MHz IF frequency as in the noise figure measurement. As in the case of the noise figure, the IF frequency can be reduced to 4 MHz with no appreciable change in performance. The gain response is very flat in



(a)



(b)

FIGURE 6.2: (a) Measured input matching in L1 GPS band. (b) Measured wideband behavior of input match.

the signal band, with a maximum ripple of only 0.25 dB. The variable gain circuit in the LNA allows system gain to be adjusted between 15 and 45 dB. Figure 6.4 shows results measured with a gain setting of approximately 42 dB.

Phase noise measurements of the oscillator were obtained using an Agilent E4440A spectrum analyzer and buffered outputs from both the I and Q channel oscillators. The phase noise mismatch between the I and Q channels is approximately 1 dB. Figure 6.5

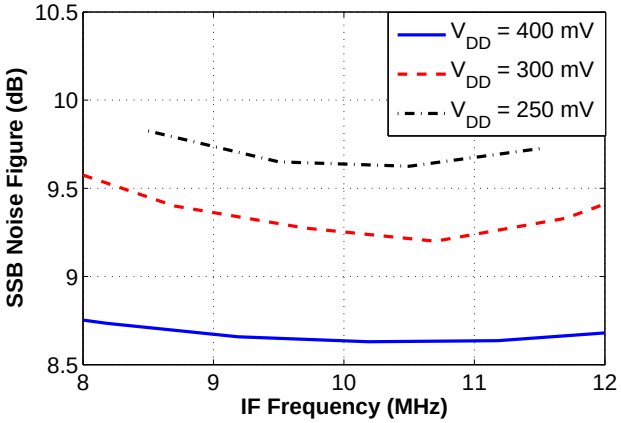


FIGURE 6.3: Measured noise figure.

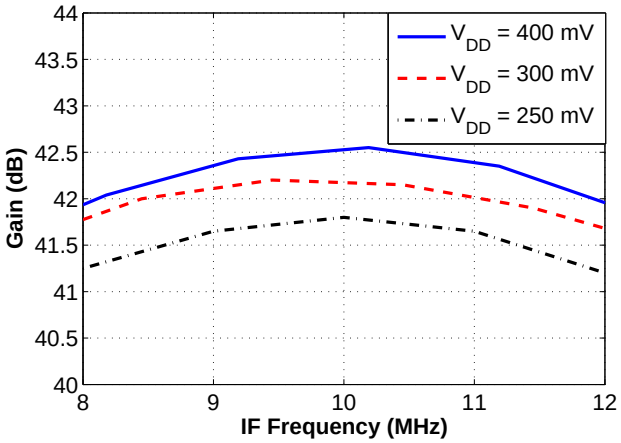


FIGURE 6.4: Measured gain.

is a plot of the measured phase noise of the Q channel oscillator. Note that the phase noise performance at a 1 MHz offset is only weakly dependent on power supply voltage, illustrating the robustness of the design in the presence of a changing power supply.

One common measure of oscillator performance is the figure of merit (FOM) [29]. The oscillator is operated in the current limited regime, so reducing the supply improves the figure of merit since power consumption is reduced without significantly changing the amplitude of oscillation. Table 6.1 shows the calculated figure of merit and measured phase noise for three different power supply voltages. The oscillator offers excellent phase

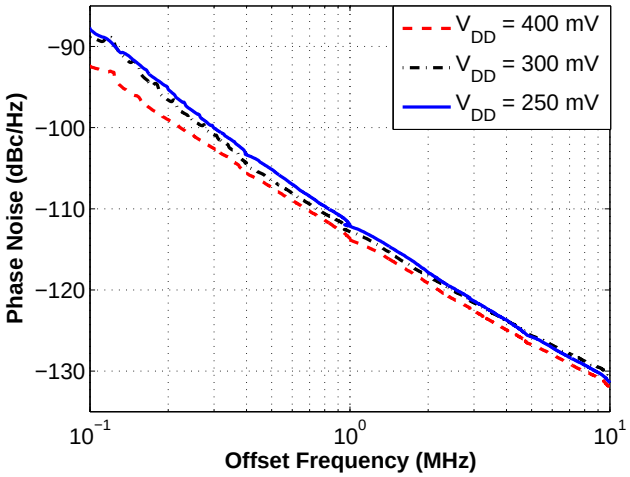


FIGURE 6.5: Measured phase noise of Q channel oscillator.

noise performance given its power consumption. The figure of merit is competitive with some of the best recently published low voltage CMOS VCOs and the supply voltage is 30% lower than in previous designs [29, 38].

TABLE 6.1: Phase Noise and Figure of Merit for VCO

	Phase Noise @ 1 MHz [dBc/Hz]	**FOM [dB]**
V_{DD} = 400 mV	-113.8	186.4
V_{DD} = 300 mV	-112.5	187
V_{DD} = 250 mV	-112.4	187.4

It is important to note that the oscillator discussed here is a quadrature design unlike the circuits discussed in [29, 38]. As a result, there is additional noise due to transistors M_3 and M_4 shown in Figure 4.1(a). If the design was presented as a stand alone VCO without quadrature outputs, these transistors could be eliminated, improving phase noise performance. In addition, further optimization of the bias circuit and transistors M_1, M_2, and M_5 through simulation suggests that phase noise performance can be improved by

approximately 3 dB with no increase in power. With some minor changes, the oscillator should offer a measured figure of merit in excess of 190 dB.

The linearity of the front end was characterized by measuring both IIP3 and 1 dB gain compression. These measurements were obtained with a Tektronix RSA3308A spectrum analyzer and an Agilent E4433B signal generator. The measured IIP3 is -35 dBm and 1 dB compression is -45.7 dBm with the system gain set to 35 dB. To improve linearity, the system gain can be dynamically reduced to 15 dB, providing a significant linearity improvement. With the gain adjusted to its minimum setting, the measured IIP3 is -10 dBm and 1 dB gain compression is -21 dBm.

Table 6.2 provides the complete characterization of the system as well as a comparison with some recently published integrated RF front ends [5, 39, 40]. Power measurements include all bias circuits for the entire front end. The low power design techniques employed result in the power consumption being an order of magnitude lower than the lowest previously published work [5]. Additional novel features of the design include variable gain and

TABLE 6.2: Summary of Performance and Comparison to Prior Work

	[5]	**[39]**	**[40]**	This Work		
				V_{DD}: 400 mV	V_{DD}: 300 mV	V_{DD}: 250 mV
VCO Phase Noise @ 1 MHz [dBc/Hz]	-104	-118	-122*	-113.8	-112.5	-112.4
VCO Tuning Range [%]				11	11	11
Nominal Conversion Gain [dB]	36	25.8	16	42.5	42.2	41.8
Gain Adjustment Range [dB]				27.5	27.2	26.8
SSB Noise Figure [dB]	4.8**	2.7 (DSB)	6**	8.6	9.2	9.6
|S11| @ Center Frequency [dB]	-20	-30		-16	-16	-16
-10 dB Bandwidth of |S11| [MHz]	210	250		935	935	935
IIP3 [dBm]	-19	-14.5	-6	-35	-35.2	-35.8
1 dB Compression Point [dBm]	-31	-27.6	-18	-45.7	-47	-48
LO to RF Leakage [dBm]	-55	-105		-80.7	-81	-81.75
Process Technology	0.13μm CMOS	0.35μm BiCMOS	0.25μm CMOS	0.13μm CMOS	0.13μm CMOS	0.13μm CMOS
Power Consumption [mW]	5.4	41.3	9.6	0.586	0.405	0.352

* 600 KHz Offset ** Not Specified as DSB or SSB

a fully integrated input match. These features provide unprecedented levels of flexibility and integration. Additionally, there is no requirement for access to the body terminal of NMOS transistors, eliminating the need for special processing steps associated with this requirement and reducing cost. The resulting design offers a revolutionary combination of ultra low power consumption, excellent performance, and compact size.

7 CONCLUSION

A new ultra low power GPS RF front end with the lowest supply voltage and power consumption reported to date has been presented. Ultra low voltage circuit design techniques have been used to reduce power consumption by an order of magnitude over any previously reported work. Several new ultra low voltage circuits have been developed for the front end. An ultra low voltage two stage LNA with a fully integrated input match and variable gain improves system integration and flexibility. The down conversion mixers utilized in the system have been optimized for low power operation through the elimination of the LO buffer and by biasing the switched transconductors in the mixers in weak inversion, maximizing the conversion gain at low power levels. A low voltage quadrature oscillator with immunity to supply fluctuation and excellent phase noise performance provides an efficient and robust LO signal to the mixers without using a LO buffer.

These new circuits combine to provide a compact, efficient, and highly flexible receiver front end with excellent performance. Unlike most low voltage designs, access to the body terminal of NMOS transistors is not required, eliminating the need for a triple well process. This front end's high degree of integration and order of magnitude reduction in power consumption opens the door to the development of compact, inexpensive precision location sensors using GPS technology.

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APPENDICES

A Wildlife Tracking

Tracking the location of organisms has long been a desire of scientists. Location tracking can be used to study migratory habits, reproductive behavior, and other key animal activities. For many years, scientists have used visual sightings of animals that are either tagged or have some other uniquely identifying characteristic to track wildlife movement. Obvious drawbacks exist with this method. Tracking large numbers of organisms is nearly impossible due to the difficulty of locating the organisms and uniquely identifying them once they are found [41]. An ideal solution to this problem is an accurate location sensor with the intelligence required to uniquely identify the organism that it is responsible for tracking.

One of the most challenging and important behaviors to track is migration. This is a key behavior because one glitch in a migration pattern can affect the health of a population for many subsequent years. Migration can be found in an incredibly wide range of animals. The incredible diversity of migratory animals can be understood by considering two of the most well known migratory animals: humpback whales and monarch butterflies.

Birds are some of the most prolific of all migratory animals. At the present time there are a couple commonly employed methods of tracking birds. One method involves tagging birds with a small, primitive transmitter which can be tracked by a nearby receiver. This method allows somewhat accurate tracking of small birds over very short distances. The range of this technique is generally limited to a few hundred yards [42]. In nearly all cases, migration tracking requires significantly longer range than this solution offers. An alternative method, which can be used on large birds, is to tag the bird with a tracking collar. These collars use satellite communications for location information and data transmission. The benefit of this system is that it offers global tracking range. At the present time, the collars are far too large and heavy to track anything smaller than a large bird of prey. Global tracking of small organisms requires the creation of a new

position sensing device that is both compact and efficient.

For migratory bird tracking, global range is an absolute requirement. This makes a satellite based tracking method a very attractive option [43]. Two of the primary satellite tracking systems that exist today are ARGOS [43, 41] and GPS.

ARGOS based services have been used for bird tracking for many years. ARGOS has two serious drawbacks. ARGOS operates with a carrier frequency of 406.5 MHz [43]. This equates to a whip antenna approximately 7 - 8 inches in length [42]. The physical size of the antenna may be of marginal importance on a large bird, but it is a significant problem if smaller birds are to be tracked. The other problem with ARGOS is the inconsistent accuracy. The average error is only 350m, but the maximum error can be greater than 500 km [44]. In many cases, this much error and uncertainty is intolerable. In addition, ARGOS services require a subscription to a monthly service, which makes access more difficult and increases cost [42].

TABLE A.1: Comparison of GPS and ARGOS

	GPS	**ARGOS**
Whip Antenna Length (inches)	1.75-2	7-8
Typical Accuracy (m)	100	350
Transmit/Receive	Receive	Transmit
Subscription Cost ($ per month)	0	6.00

One excellent alternative to ARGOS, which addresses all of the previously stated problems, is GPS. The carrier frequency of GPS is 1.575 GHz [9], meaning that a simple quarter wave whip will have a length of 1.75 - 2 inches [42], which is significantly smaller than a comparable ARGOS antenna [42]. In addition, the accuracy of GPS is significantly better than that of ARGOS. Typical error in a GPS system is around 100 m [45]. In addition, GPS doesn't suffer from the maximum error issues associated with ARGOS.

One other benefit that GPS has over ARGOS is that there is no fee associated with using it. In a small study this may be a minor concern. However, if a large population is studied, the subscription cost of ARGOS may become prohibitive.

The drawback of GPS is that it is considerably more complex than ARGOS. ARGOS simply transmits a signal that indicates the ID of the tag. All of the difficult work, like detecting and processing the transmitted signal, is done by the ARGOS satellites [43]. GPS moves much of the complexity to the GPS receiver. In spite of this, GPS offers the possibility of lower power because GPS doesn't transmit, meaning that the GPS system doesn't require a power hungry power amplifier. The advantages of GPS over ARGOS make it the clear choice to create a compact and accurate mobile location sensor. Table A.1 summarizes the key differences between GPS and ARGOS.

B GPS Overview

The GPS system, which is also known as the NAVSTAR global positioning system, is operated by the United States Department of Defense [45]. A total of 24 satellites are used in the system. The satellites are organized into 6 orbital planes with 4 satellites in each plane [46, 47]. Location can be accurately calculated by measuring the distance from the receiver to 4 or more satellites [46]. This distance is calculated by determining the time delay associated with the data being sent by each visible satellite. Triangulation is then used to precisely determine the location of the receiver [45].

GPS is well known for its accuracy. The useful accuracy of standard GPS is approximately 100 m. Interestingly, the accuracy of the system is actually intentionally limited to this degree of precision. The GPS signal that is available to civilians is called C/A code, which stands for coarse acquisition [45]. The 100 m accuracy of the C/A code is intentionally limited for civilian usage. Maximum precision signals are encoded with another code and may be reserved for military use. This code is called the P code, which stands for precise code.

Two GPS bands are commonly used. These bands are referred to as the L1 and L2 bands [48]. The L1 band is used in most commercial GPS receivers. It carries both the C/A code and P code with a center frequency of 1.57542 GHz. The L2 band, which is centered at 1.2276 GHz, carries only the P code. Some commercial receivers support both the L1 and L2 bands. However, the P code content is not guaranteed to be available, making the L2 band of limited use.

In a typical GPS communication system, the receiver sees a channel power of approximately -130 dBm [9, 48]. Typical receivers begin to have difficulty in reliably resolving signals with a power level below -100 dBm. Considering the power of the GPS carrier, it is clearly impractical to directly receive unencoded data. Fortunately, the data rate of GPS is very low. In the case of the L1 band, the data rate is 50 bps [48], and in the case of the

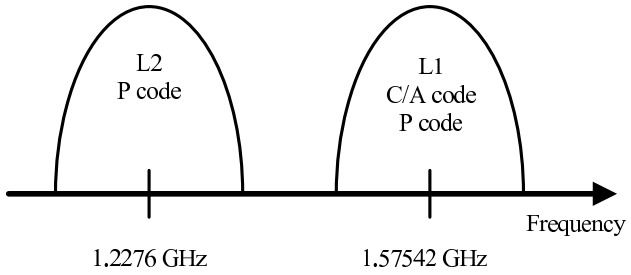

FIGURE B.1: Typically used GPS bands.

L2 band it is 25 bps [9]. This low data rate means that it is possible to transmit many symbols for each bit of data. These symbols are called chips. This allows the receiver to integrate the received signal over a long period of time, effectively increasing the amount of energy associated with each received bit [9]. This technique is called spread spectrum coding. There is a processing gain associated with spread spectrum coding, and it allows the receiver to resolve signals that have very low signal power. The processing gain is given by [49]:

$$G = 10 \log \left(\frac{chip\_rate}{data\_rate} \right) \tag{B.1}$$

The spread spectrum scheme utilized in GPS is called direct sequence spread spectrum (DSSS). In a DSSS system, the transmitter modulates the transmitted signal by a series of values called pseudo random noise (PRN) [48]. The PRN sequence is chosen to evenly spread the energy of the transmitted data over the desired spectrum. As a result, the signal appears to be white noise in the spectrum over which it is spread. Figure B.2 illustrates the relative relation of bits, chips, and spectral bandwidth for a signal before and after spreading. In L1 band GPS, the PRN sequence has a length of 1023 chips [10]. As stated previously, many symbols (or chips) are sent for each bit of data, so the chip rate is much higher than the actual bit rate. In the case of L1 band GPS, the chip rate is 1.023 Mcps [9], meaning that 20460 chips are transmitted for each bit.

Receiving DSSS coded data requires that the receiver has prior knowledge of the

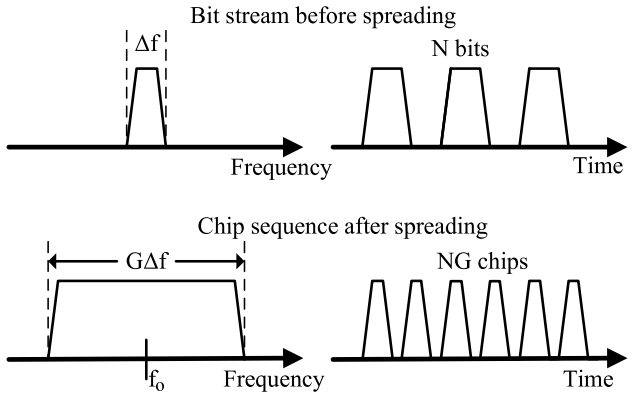

FIGURE B.2: Relative effect of spreading in time and frequency domains.

PRN sequence. The receiver must despread the received chips to obtain the desired bits of data that are hidden in the spread spectrum signal. This process encompasses applying the PRN code that was used to modulate the bit sequence at the transmitter to demodulate the received chip sequence and obtain the desired data stream. In essence, the PRN sequence is applied in reverse at the receiver to undo the spreading action that occurred in the transmitter [50].

To properly process the received chips, the receiver must synchronize itself very precisely with the transmitter to ensure that the PRN code is applied at precisely the correct location in the received chip sequence [50]. Without proper synchronization, the receiver has no way of resolving the data from the PRN encoded noise. At first glance, this may seem like a problem, however, it can be used in GPS to obtain the precision timing information that is required to calculate the receiver's distance from a satellite. All of the satellites of the GPS system are precisely synchronized with each other. This means that the receiver can simply determine the difference in time between received data sent by different satellites to determine its position. Figure B.3 gives a simple example of this. Assuming that the positions of the two satellites are known, which is the case in a GPS system, the receiver calculates the difference between the time delays associated with the transmissions from satellites 1 and 2 to find its position. If the difference is zero, then the

receiver is located precisely between the two satellites. If $t_{d1} > t_{d2}$, then the receiver is located closer to satellite 2. It's important to keep in mind that in a real GPS system the receiver must compare timing information from at least 4 satellites.

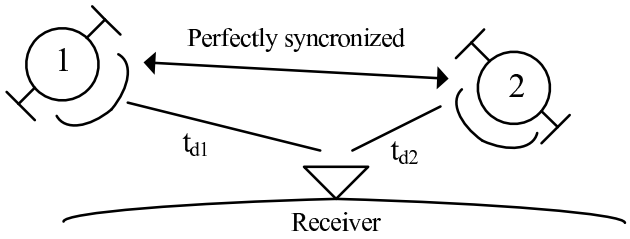

FIGURE B.3: Satellite position and timing.

Another unique property of spread spectrum coding is that it permits multiple transmitters to simultaneously send data within the same portion of the frequency spectrum [51]. GPS satellites use a set of PRN codes called gold codes [48]. Gold codes have perfect orthogonality [52], meaning that there is zero correlation between the data transmitted by any two satellites. This means that both the C/A and P code transmissions from each satellite are unique. As a result, all of the GPS satellites can simultaneously transmit within the same portion of the frequency spectrum. Therefore, the GPS receiver can tune itself to the transmission of any desired satellite that is in range by selecting the correct code.

Another benefit of using orthogonal gold codes is that the code itself carries the ID of the satellite. This is because an orthogonal code will always give a data value of 0 unless it is used to demodulate a signal that was modulated with the same code [51]. As a result, any time the demodulated signal has a nonzero value, it must have come from a satellite using the same PRN code as the receiver.