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Donald L. Amort

A fluorescence anisotropy spectrophotometer known by the acronym GUS has been in use at Oregon State University in the department of biochemistry and biophysics for several years under the supervision of Dr. Irvin Isenberg. Dr. Isenberg wished to improve the accuracy, versatility, speed of data acquisition, and ease of operation by using a PDP-8/E computer to control the apparatus, collect data, and compute the desired results. Formerly the apparatus was controlled manually and data conditioning was done primarily by analog means.

The author was given the task of designing the interface between GUS and the PDP-8/E computer given the following conditions:

I. Two analog signals from GUS must be conditioned and connected to the AD01 analog to digital converter

supplied with the PDP-8/E computer.

II. A reference signal is available from the mechanical light chopper of GUS, and data sampling must be synchronized with this reference.

III. A simulator must be built to provide controllable test signals with noise for purposes of testing the computer operation under known input conditions.

IV. An automatic control must be built for initiating the computer program periodically at a preselected time interval for the purpose of observing time varying samples.

V. In addition the AD01 analog to digital converter needs substantial modification to make it compatible with the rest of the system.

This paper describes the implementation of the system as outlined above.

Interfacing a Fluorescence Anisotropy Spectrophotometer to a PDP-8/E Computer

by

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TABLE OF CONTENTS

1. Introduction: The Basic Instrument... 1

2. The Synchronization Problem..... 6

3. AD01 Modifications..... 12

4. The Periodic Mode..... 21

5. PDP-8/E Buss Interface Circuit..... 24

6. Simulating GUS Signals..... 30

7. Signal Conditioning..... 35

8. Concluding Remarks..... 37

Bibliography..... 38

Appendix..... 39

Interfacing a Fluorescence Anisotropy Spectrophotometer to a PDP-8/E Computer

Chapter 1

Introduction: The Basic Instrument

This paper describes the interface between a PDP-8/E computer and a fluorescence anisotropy spectrophotometer known as GUS. This chapter will familiarize the reader with the basic instrument and the type of signals that must be handled.

The apparatus is shown in schematic form in figure 1. A light source emits a beam of light that passes through a mechanical light chopper. This chopped beam of light then passes through a polarizing filter and strikes a chemical sample (such as Rhodamine B or a Histone).

The sample fluoresces and the emitted light is measured by two photomultiplier tubes, one with a vertical polarizing filter and the other with a horizontal polarizing filter. The photomultiplier outputs are amplified by electrometers and preamplifiers. Since the signal levels are extremely small there is a large amount of noise superimposed on the actual signal. The signal to noise ratio varies widely depending on the nature of the sample under test, but in general the signal cannot be read on an oscilloscope

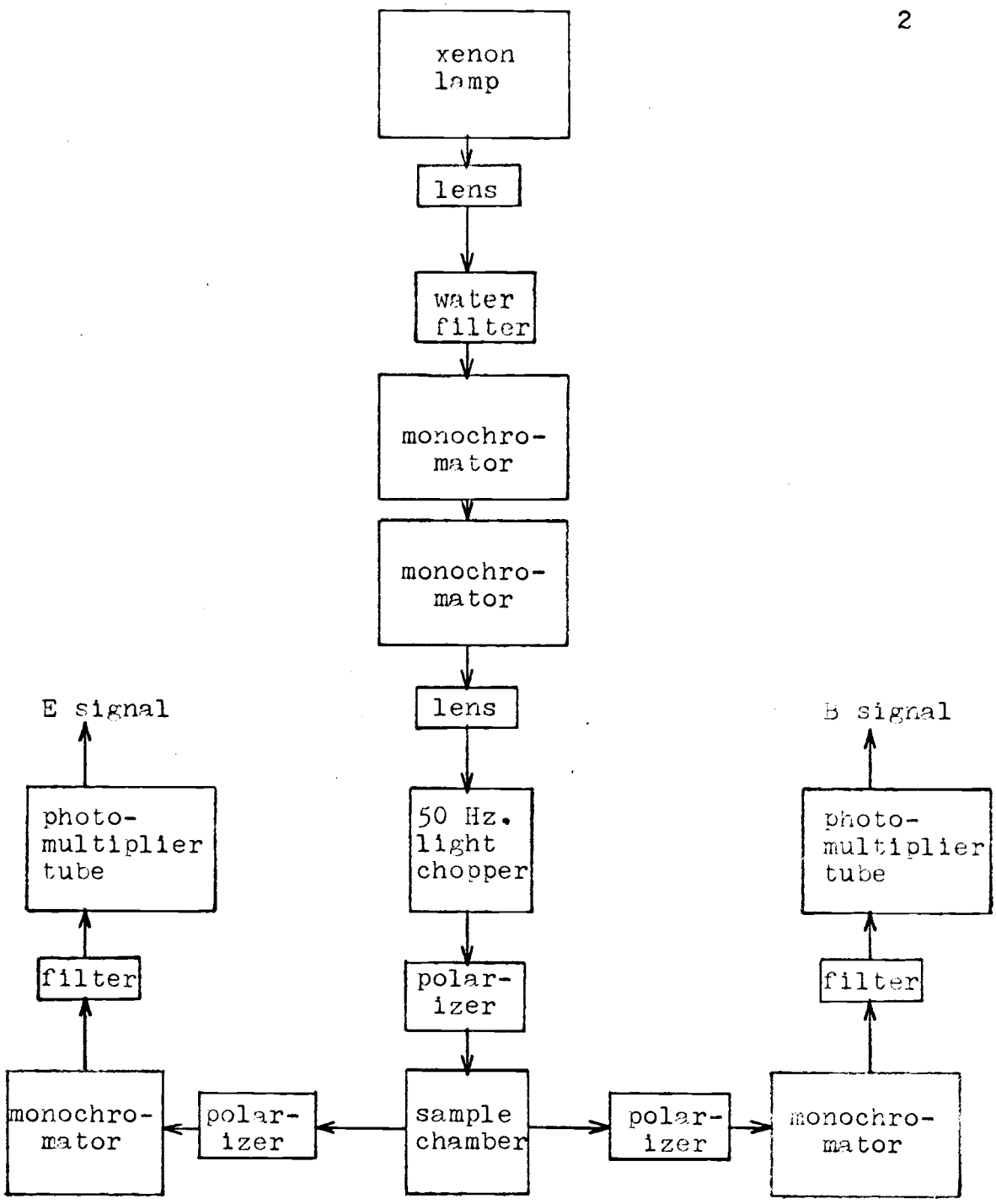

Figure 1. Basic GUS Instrument

with any degree of accuracy, and for the worst cases no signal can even be seen with the eye.

Since the signals are so small, DC offset and drift become a problem. To avoid these problems the light source is chopped and it is necessary to measure the signal twice during each cycle of the chopper, once when the chopper is closed and again when it is opened. Offset and drift are eliminated by taking the difference between these two readings. The present chopper runs at 50 Hz and the resulting light intensity is approximately a square wave as a function of time.

The two signals from GUS are denoted E and B and the final desired results are E+2B and (E-B)/(E+2B). The data was previously handled by lock-in amplifiers and a small analog computer. This arrangement proved unsatisfactory and the analog computer was replaced by a summing digital voltmeter and a counter. E and B were then measured and averaged separately and the final calculations done manually. This system required considerable care in use to insure that the two channels used for E and B were properly adjusted. The system had to be aligned by measuring E and B with the initial polarizing filter rotated 90°. A variable gain control on the B channel allowed adjustment of the B amplitude and had to be set such that B and E were

of equal amplitude in this cross polarized configuration.

The system was quite cumbersome to use and required a highly trained operator to achieve accurate results. However it should be noted that this apparatus was one of only a very few in existence capable of measuring the desired results to accuracy in the third significant digit.

Dr. Irvin Isenberg (department of biochemistry and biophysics) wished to improve the system by computerizing it. If the apparatus could be interfaced with a computer, several simplifications would result. For example, channel sensitivity would no longer need to be adjusted because the computer could calculate a numerical sensitivity correction before beginning an actual data run. All incoming data for B could then be multiplied by this correction factor. In addition all calculations could be done by the computer rather than manually. The computer would also allow greater flexibility limited only by the ingenuity of the programmer and the amount of available core storage for holding various routines.

With this in mind a PDP-8/E computer and an AD01 analog to digital converter system were acquired from Digital Equipment Corporation. In addition a teletype was purchased to provide input/output capabilities to the computer.

The proposed scheme involved connecting the E and B signals from GUS to two of the four available multiplexed input channels of the AD01 analog to digital converter. All data could then be converted to digital form and be processed by the computer. In addition it was decided to add a third photomultiplier tube to GUS for monitoring the source lamp intensity. This signal is denoted as L and will use one of the two remaining multiplexer inputs.

Chapter 2

The Synchronization Problem

As mentioned earlier the light source for GUS is turned on and off with a mechanical chopper. The resultant waveforms are represented in figure 2. (Noise has been omitted for clarity.) The necessary data is $\overline{(E-E_o)}$ and $\overline{(B-B_o)}$ where the overbar denotes an average value. The chopping is necessary to eliminate problems associated with DC offset and drift in the amplifiers.

It is necessary to synchronize the sampling process to the chopper in order to guarantee that the A/D converter samples the signals only at times that correspond to the flat regions of the waveform. Furthermore the computer must know for each sample whether the chopper is open or closed.

The circuit shown in simplified form in figure 3 accomplishes these objectives. The circuit can be divided into two sections; one section generates sync pulses while the other section is a control section. In the following explanation refer to the waveforms of figure 4. The reference signal from the chopper is amplified and clamped at TTL levels. This signal triggers two monostable multivibrators, one on the rising edge and the other on the

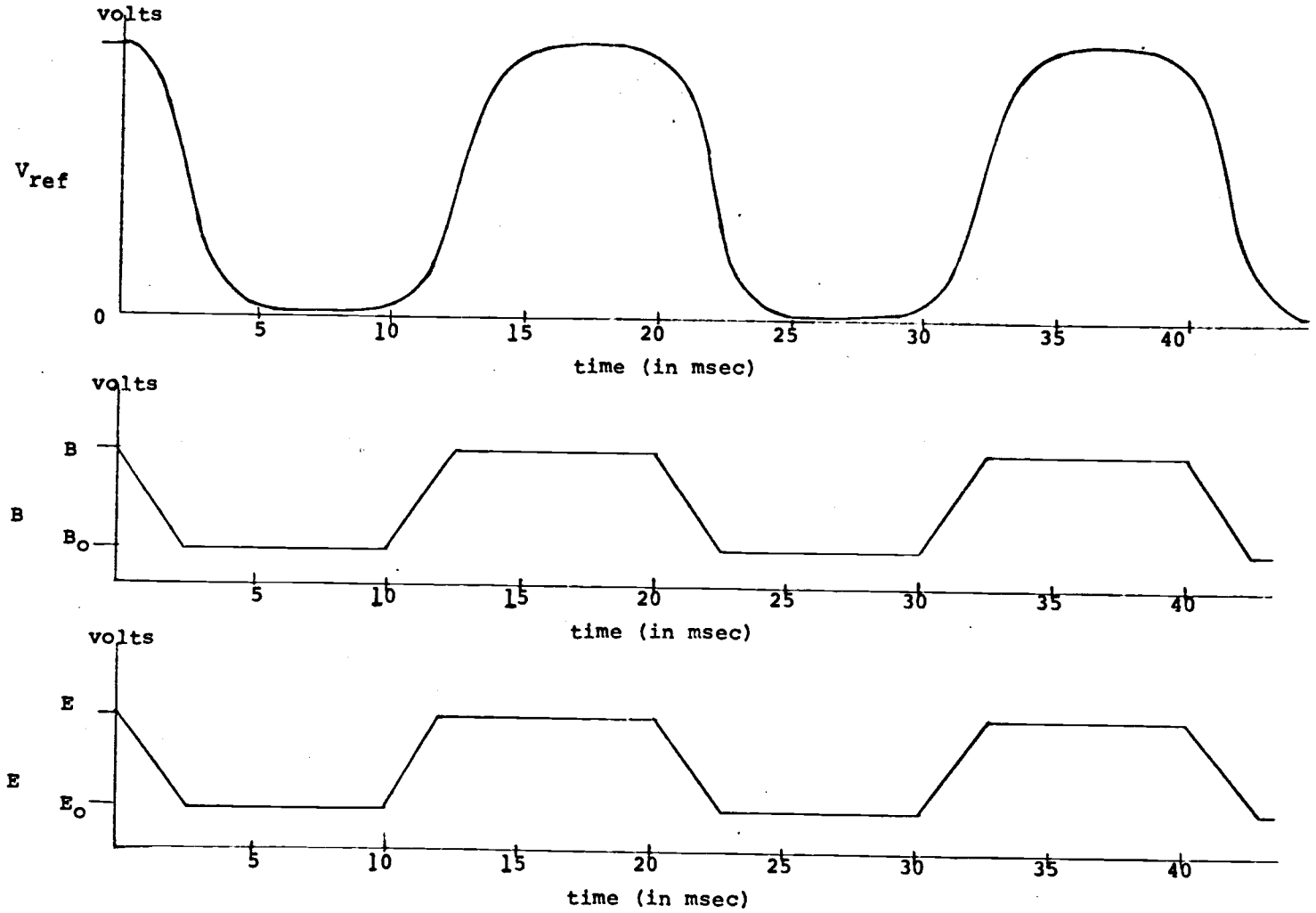

Figure 2. Basic GUS Signals

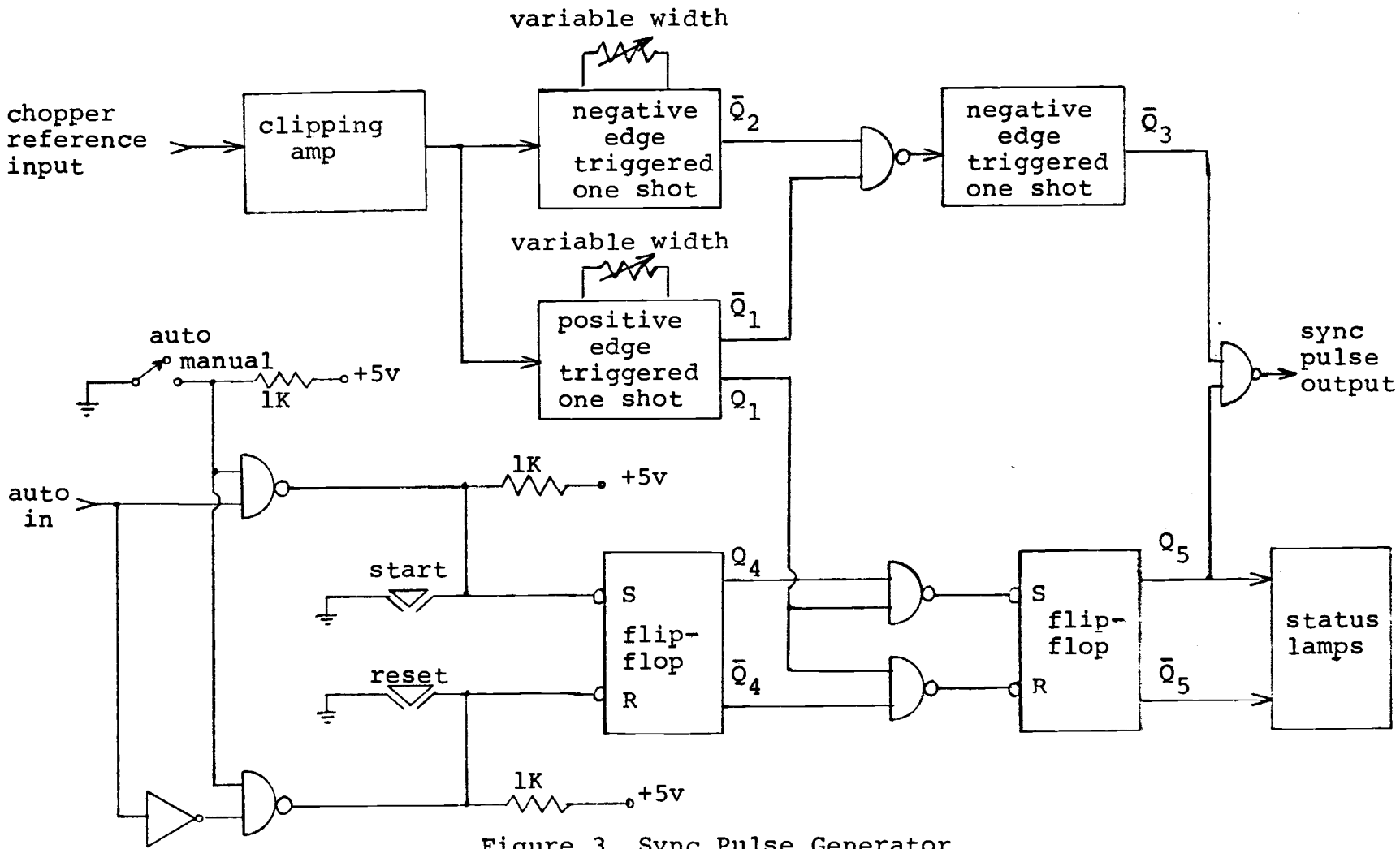

Figure 3. Sync Pulse Generator

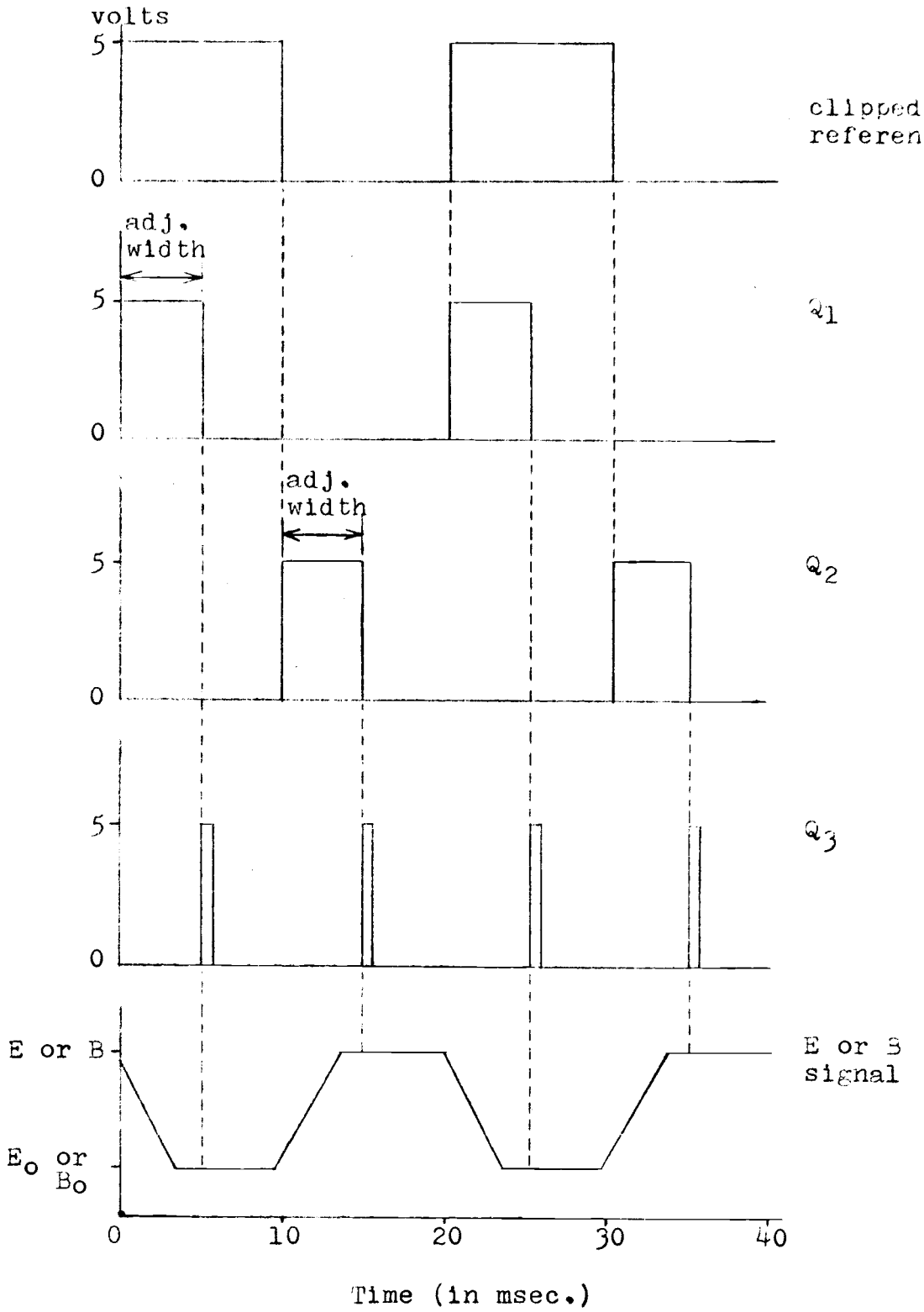

Figure 4. Sync Pulse Generator Waveforms

falling edge. The outputs of these two monostables are Q_1 and Q_2 respectively. Q_1 and Q_2 are logically "OR"ed and the resulting signal triggers monostable Q_3 on the falling edge.

The Q_3 pulses are about one μsec in width and these form the desired sync pulses. Q_1 and Q_2 have separately adjustable pulse widths. By adjusting trimpots the sync pulses may be positioned at any point in time relative to the reference waveform. This allows the system to be adjusted for nonsymmetrical data waveforms and phase lag between the chopper reference and the actual chopper movement.

We must still address the problem of keeping track of whether the chopper is open of closed for each sync pulse. This problem is solved by the control section. Q_3 is gated to the output connector through a NAND gate controlled by flip-flop Q_5. Flip-flop Q_4 stores any request to turn the sync pulses off or on. The two gates connecting the outputs Q_4 and $\overline{Q}_4$ to the inputs S and R of Q_5 perform the function of transferring the state request from Q_4 to Q_5 at the appropriate time such that the following situation always is true: Whenever the sync pulses are turned on the first pulse to be gated out always corresponds to the high reference state, and conversely whenever the sync

pulses are turned off the last pulse to go out always corresponds to the low state of the reference. In this manner the computer can easily keep track of the position of the chopper simply by toggling a two state counter in the program each time a sync pulse is received.

Q_4 may be set and reset either manually by means of two pushbutton switches or automatically by an external logic signal. A switch disables the external automatic input when the manual mode is desired. Two lights on the front panel indicate the state of Q_5 and hence show whether the sync pulses are on or off.

Chapter 3

AD01 Modifications

The AD01 analog to digital converter system supplied with the PDP-8/E computer had to be modified for use with GUS. The original system is shown in block form in figure 5. It consisted of a program controlled four channel analog multiplexer followed by a programmable gain amplifier with gains of 1, 2, 4 or 8. The analog signal then went to a successive approximation type analog to digital converter. Conversion was initiated by a program instruction. When the conversion was completed an end of conversion signal set the flag. The flag could be interrogated by the program and an instruction skip occurred if the flag was set at the time of interrogation. This allowed the programmer to wait for the conversion to end before executing an instruction to read the result.

The system had two main drawbacks. First of all there was no way to synchronize the sampling with the sync pulses from the sync pulse generator. The second difficulty arose because of the successive approximation method of conversion. A successive approximation analog to digital converter requires a nonvarying analog input signal during the time of conversion. This particular system required 29 μsec to make a conversion and thus any noise on the signal with frequency

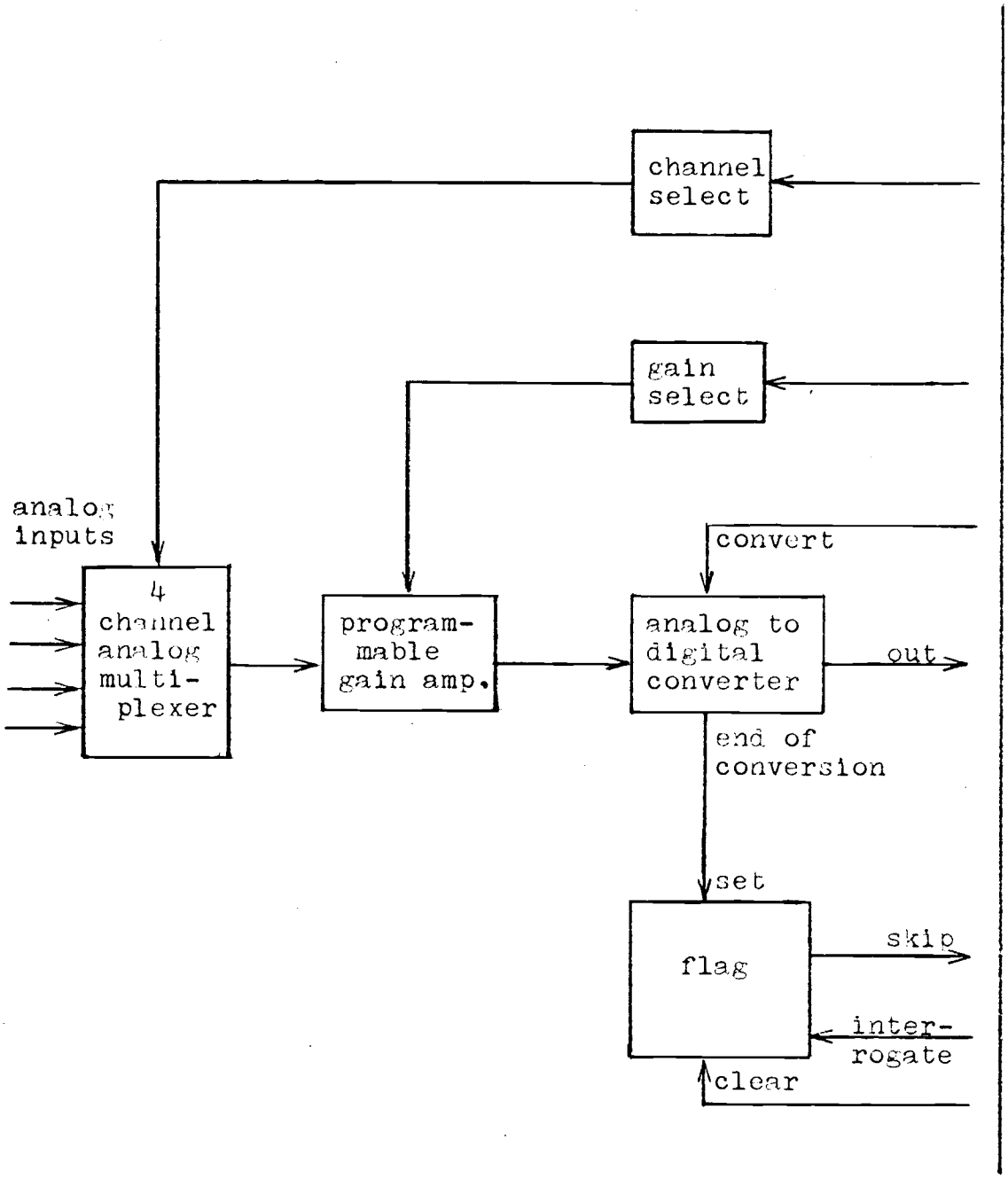

Figure 5. Original AD01 System

content in the neighborhood of 10 KHz or higher would cause erroneous results. Since the signals from GUS can be extremely noisy this presents a nontrivial problem.

These deficiencies were corrected by modifying the system as shown in figure 6. The main change was the addition of an integrate and hold circuit. This was designed around a Philbrick-Nexus 4850 three mode integrator. The 4850 includes a low-bias-current operational amplifier, two FET analog switches and a reset circuit. It was necessary to supply the integrating resistor and capacitor as well as the logic functions to control the mode (reset, integrate or hold) of the 4850.

An integrate and hold circuit was selected instead of a sample and hold circuit to take advantage of the noise cancelling properties of the integration process. If integration is begun at each sync pulse and is terminated before the chopper begins to change state (see figure 7) then the process is essentially one of integrating a DC level with noise. If the length of time of integration is held constant then the result at the end of each integration is a component directly proportional to the DC level and a reduced noise component. By numerically averaging over many integrations the noise component will tend towards zero.

The timing of the integration interval is fixed by a crystal controlled 300 KHz clock and a counter. The counter

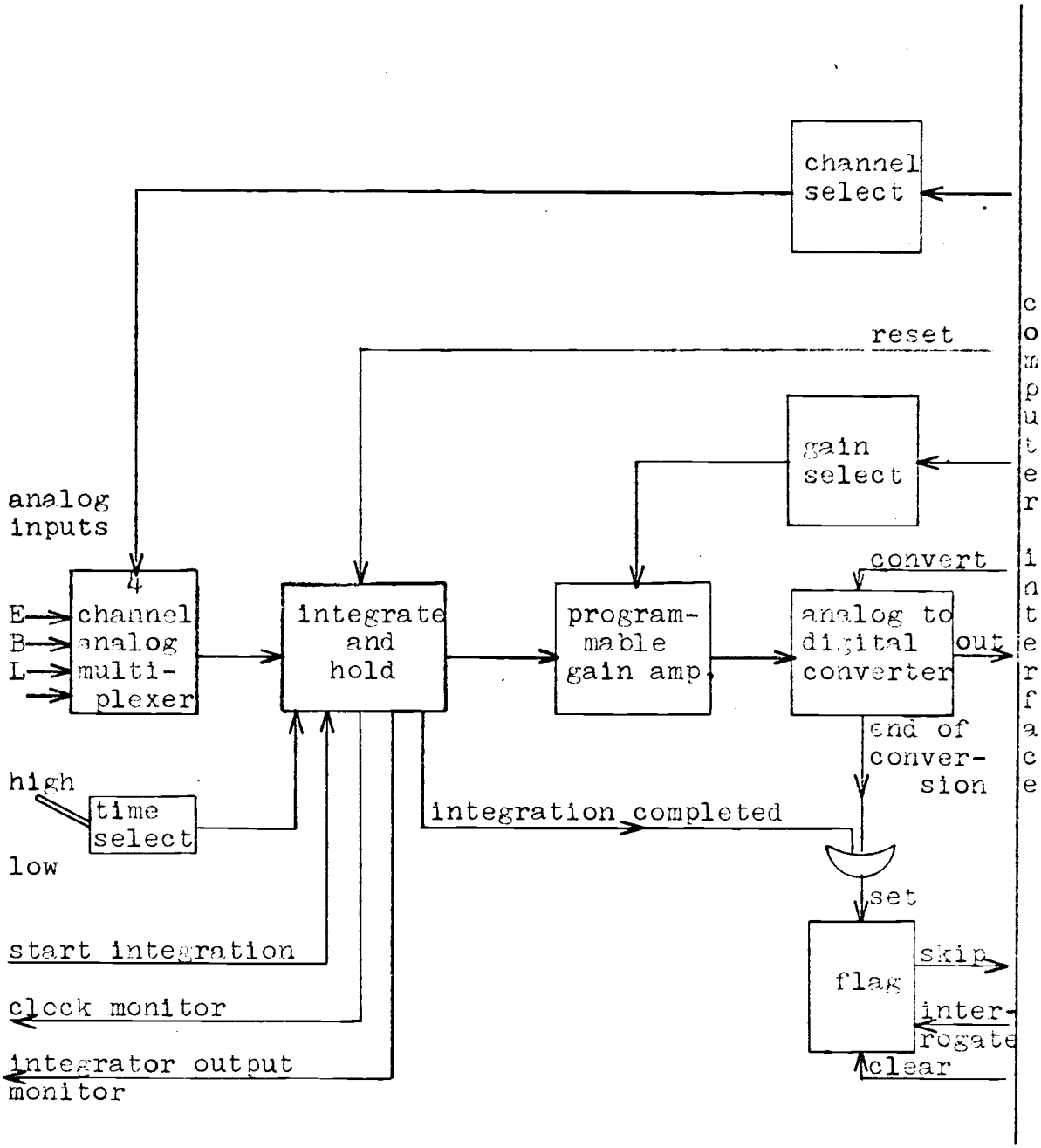

Figure 6. Modified AD01 System

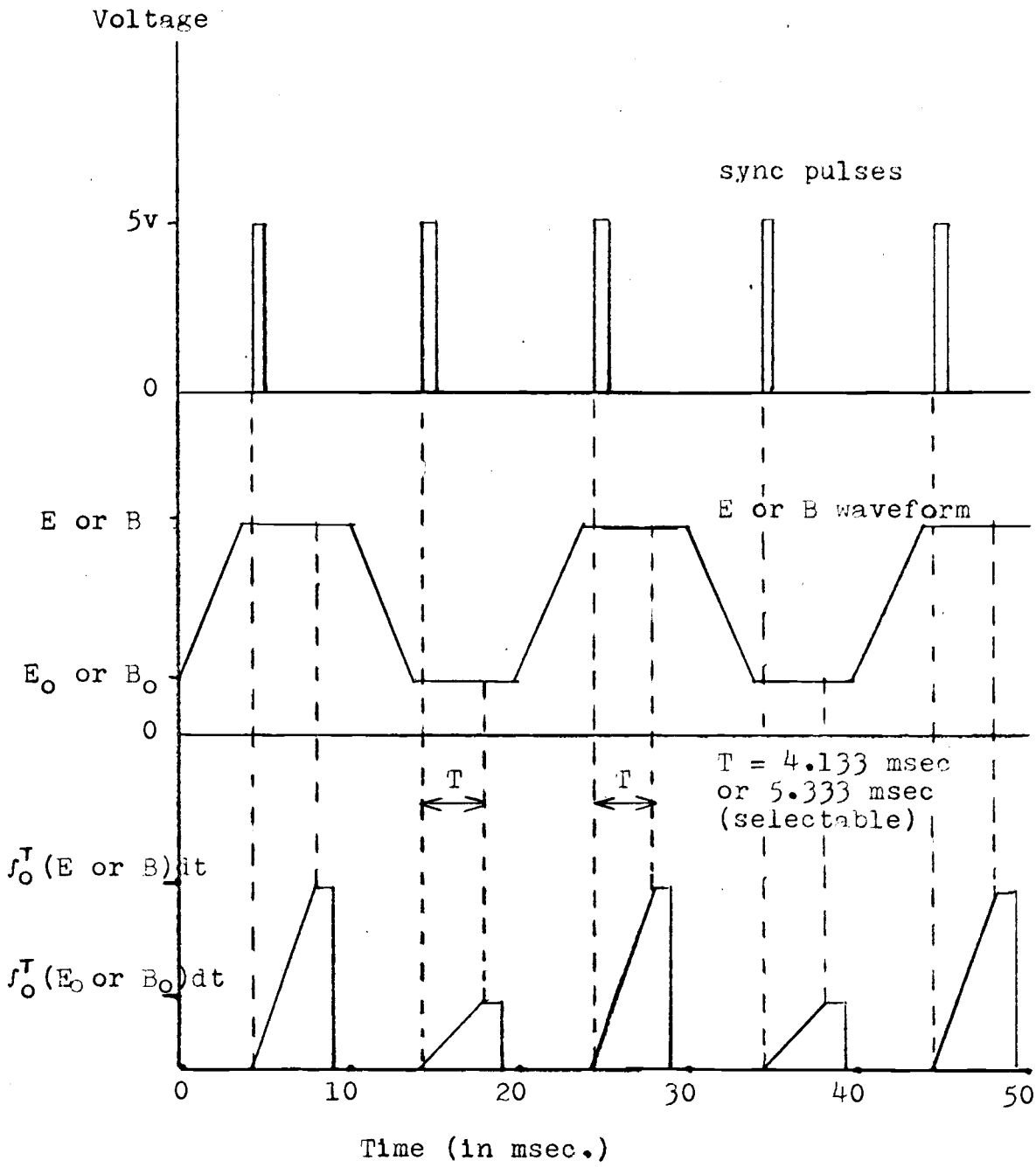

Figure 7. Integration of the E or B Waveform

begins counting clock pulses when integration begins and integration terminates when the counter reaches 1600. The counter may be preset to either zero or 360 (selectable by a toggle switch) and the corresponding lengths of integration are 5.33... msec or 4.133 msec. Integration always begins on the rising edge of the first clock pulse following the sync pulse and thus there is no $\pm\frac{1}{2}$ clock period uncertainty in the length of the integration interval.

The output of the integrator has the mathematical form

$$-V_{out} = V_o + \frac{1}{RC}\int_0^T V_{in}dt$$

where R is the input resistor, C is the feedback capacitor, T is the length of integration, V_{in} is input voltage, V_{out} is output voltage and V_o is the reset voltage. V_o can be arbitrarily set by controlling the current to the reset input of the 4850. V_o was chosen at approximately -9 volts for the following reason: The range of the analog to digital converter is -10 v to +10 v, but the signals from GUS are unipolar (positive voltage only). Hence to take advantage of the full range of the ADC it is necessary for the integrator to be reset close to -10 v because the integration will always proceed in a positive direction.

R and C determine a multiplicative constant on the integral and were chosen such that the largest signals expected on the inputs of the system would not overdrive

the integrator. The capacitor has polystyrene dielectric material for low leakage and good stability.

In the modified configuration, the programmable gain amplifier follows the integrate and hold circuit and this is followed by the ADC. (See figure 6.) The system operates as follows:

1. The circuitry is initialized by the computer for the E input of the four channel multiplexer, the reset mode of the integrator and a gain of 1.
2. The sync pulse generator is activated by command from the computer.
3. The first sync pulse occurs and integration begins.
4. When the integration is complete the 4850 enters the hold mode and the flag is set.
5. The computer senses the flag, clears the flag and initiates an analog to digital conversion.
6. When the conversion is complete the ADC sets the flag.
7. The computer senses the flag, clears it, and executes a read instruction to transfer the results to the computer.
8. The program checks the data entry for an over-driven input condition by noting whether or not the data is at the positive or negative limit of the ADC.

9. The program then checks to see if the gain of the programmable amplifier can be increased.

10. The optimum gain having been determined above, the program resets the gain and initiates a new conversion, keeping track of the gain in the form of an exponent. This process insures that all readings will have as many significant bits as possible.

11. When the conversion is complete, the flag is set, sensed, cleared, and data transferred to the computer as in steps 6 and 7 above.

12. The integrator is switched from hold to reset and the gain reset to 1. This completes the E reading.

13. Steps 3 through 12 are repeated to measure E_o. (See figure 2.)

14. The computer then switches the multiplexer to the B channel and repeats steps 3 through 13 to obtain B and B_o data.

15. The program may branch at this point and either repeat steps 3 to 13 to obtain data from the L channel or skip the L channel entirely, whichever the operator has chosen to do.

The entire integrate and hold circuit along with its clock, counter, and controls was constructed on a DEC circuit card and plugged directly into a blank socket on the AD01 frame.

An additional change was made to give the data one more bit of resolution. The ADC itself has a twelve bit output. However only eleven of these bits were originally transferred to the computer. The twelfth bit (the least significant) was ignored. By rewiring the interface, all twelve bits were made available to the computer.

To aid the operator in verifying proper operation of the integrating system, two monitor outputs are available. One allows the integrator output to be displayed on an oscilloscope. The other allows the operator to verify the frequency and stability of the timing clock.

Chapter 4

The Periodic Mode

One of the new capabilities envisioned for GUS is time variation studies; i.e. how the fluorescence properties of a sample vary as a function of time. To realize this capability an accurate time base is needed. Since a Beckman counter unit was available the author chose to use its crystal oscillator as a time base. The Beckman unit contains a decade type countdown system and its time output may be set for a period of 10^{-6}, 10^{-5}, 10^{-4}, 10^{-3}, 10^{-2}, 10^{-1} or 1 second with a front panel selector switch. Since even one second is too short for the intended application, an external countdown unit was designed and built.

The countdown unit is capable of multiplying the period of pulses applied to its input by 200, 500 or 1000 and is switch selectable. The unit consists of a single stage pulse amplifier, to bring the Beckman time pulses up to TTL logic levels, followed by three decade counters. Texas Instruments SN7490 integrated circuits were used for the decade counters. These consist of a separate divide-by-two counter and a divide-by-five counter. By switching one divide-by-two counter and one divide-by-five counter in and out of the

circuit, the 200, 500 or 1000 ratio is achieved. The output pulses from this unit go to a special flag and skip circuit added to the PDP-8/E. Thus the computer program can wait for a timing pulse, take a burst of samples, analyze the data, and then wait for the next timing pulse.

The countdown unit also has a count/reset switch that allows the operator to initialize the experiment. In the reset position the output is inhibited. When the switch is changed from reset to count an output pulse corresponding to t = 0 occurs. This allows the computer to take a set of readings at t = 0. The output pulses then arrive at the selected interval of between 0.2 sec and 1000 sec depending on the combination of switch settings. (0.2 sec is not the fastest setting possible, but probably the fastest setting of any practical use.)

There is an additional reason for using the Beckman counter. The counter section may be used to count the pulses at the output of the countdown unit and thus it serves as a visual clock for the operator.

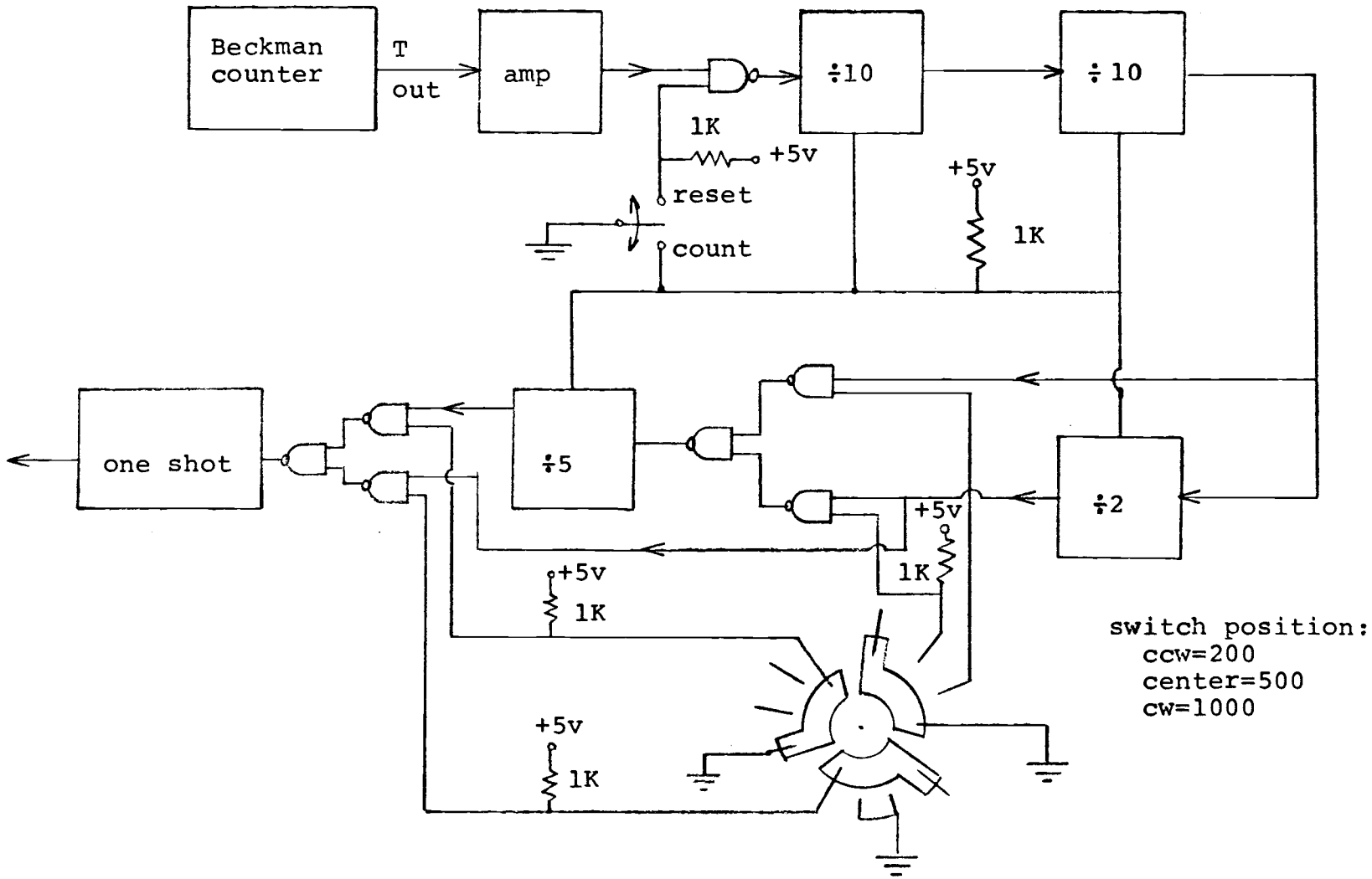

Figure 8. Periodic Timing System

Chapter 5

PDP-8/E Buss Interface Circuit

The PDP-8/E uses a common buss system called the Unibuss to connect all the subsystems of the computer together and also to interface with all outside devices. It was necessary to design a circuit to interface with the Unibuss to provide three needed functions. A flag and skip system was needed for the periodic mode described in the previous chapter. A means was needed for turning the sync pulse generator off and on (see Chapter 2) by program control. In addition a control circuit was needed for rotating the initial polarizing filter upon command from the computer.

The PDP-8/E computer has single word instructions and a twelve bit word length. All instructions for external devices take the following form;

bit	0	1	2	3	4	5	6	7	8	9	10	11
	OP code = 6			6 bit address code for device select						3 bit device instruction code		

where bits 0, 1, and 2 are always octal 6 to indicate an operation on an external device. Bits 3 through 8 form an address code. Each external device has its own unique address code. Bits 9, 10 and 11 form an instruction code that tells the device what operation to perform.

All of these bits are available on the Unibuss. In addition there are two other signals on the Unibuss that will be of importance here. The I/O Pause signal serves as a strobe signal for strobing the decoding of the six bit device select code. The other important signal is called the skip line. Whenever the skip line is asserted the program will skip the next program instruction. This feature is useful when it is desired to synchronize some part of a computer program to the status of an external device or event.

The schematic of the buss interface circuit is shown in figure 9. A seven input NAND gate serves as a decoding gate to detect the device code selected for this circuit. (14 octal.) The device selected signal from this gate then strobes the instruction code from bit lines 9, 10 and 11 to a set of gates that decode the six codes used in this circuit. The six codes and their corresponding instructions are listed in table 1. All input and output signals are negative true logic functions. This is done to permit wire-oring with open collector logic on the buss lines. All loads placed on the buss lines (I/O Pause and MD-3 through MD-11) have been designed to keep the loading effect on these lines to a minimum.

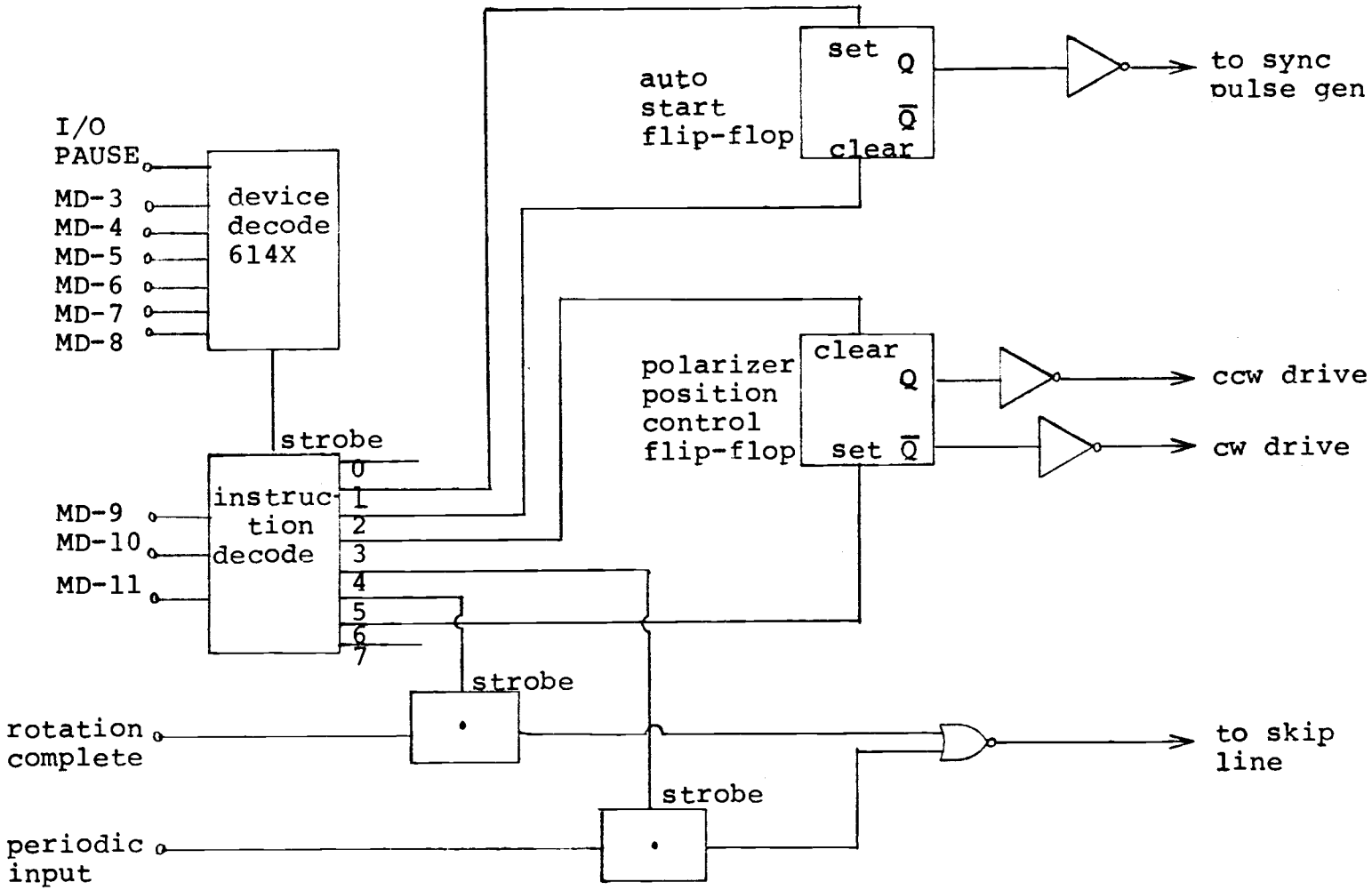

Figure 9. PDP-8/E Buss Interface Circuit

Table 1. Buss Interface Instruction Set

instruction code	complete instruction word	function
1	6141	turn sync pulse generator off
2	6142	turn sync pulse generator on
3	6143	rotate filter counterclockwise
4	6144	skip if periodic input is true
5	6145	skip if rotate completed input is true
6	6146	rotate filter clockwise

Instructions 1 and 2 set or reset a flip-flop and the status of the flip-flop is routed to the sync pulse generator (see Chapter 2). In a similar fashion instructions 3 and 6 reset or set a second flip-flop to control the filter position. Both the true and complement sides of this flip-flop are buffered out for use as necessary. The actual rotating controls have not been implemented as of this writing. This is a non-essential feature of the system and it will be implemented when funds are available.

Instructions 4 and 5 both strobe external input lines and cause a program skip if the corresponding input is true. Instruction 4 strobes the input line from the countdown circuit described in the previous chapter. Instruction 5 strobes a line for the purpose of determining when the

execution of a filter rotation instruction has been completed. (One line suffices for both CCW and CW rotations.)

To illustrate the usefulness of the skip feature to the programmer, consider the following programming example. Suppose the instrument is in the periodic mode and we wish to wait for a pulse from the timer - countdown system of Chapter 4. The following instructions accomplish this function:

address	instruction	function
1252	...	...
1253	...	...
1254	6144	skip if periodic input is true
1255	5254	jump to previous instruction
1256	...	...
1257	...	...

When the programmer wishes to wait he simply executes a 6144 which causes a program instruction skip if the periodic input is true. This is followed by a jump to previous location instruction. Hence if the periodic input is not true the program is trapped in an endless two instruction loop. It can only escape from this loop when the periodic input goes true and causes the program to skip the jump

instruction. The program then proceeds to whatever instruction occurs in address location 1256. Thus, a simple two instruction subroutine can be used to synchronize the computer program to some external event.

Chapter 6

Simulating GUS Signals

With any new data acquisition system it is desirable to have a means of checking the performance under known and controllable conditions prior to spending any large amount of time and money analyzing actual data. For this reason a simulating system was devised. The two areas of primary concern are 1) proper functioning of all software routines, and 2) linearity of the signal path. As discussed earlier, DC offset and offset drift are not critical factors due to the chopping system. Absolute magnitudes are not critical either since the primary result is in the form of a ratio.

Figure 10 shows in block form the simulator circuit. Since all signals must be synchronized with the light chopper, the reference signal from the chopper is used to derive the simulated signals. This reference is amplified and clamped to assure a uniform square wave. This signal then passes through a variable gain amplifier to simulate lamp variations. An L output signal is derived by passing the variable square wave through a summing amplifier to add in DC offset and noise.

The E output and B output are derived in a similar manner. Additional variable gain amplifiers in the E and

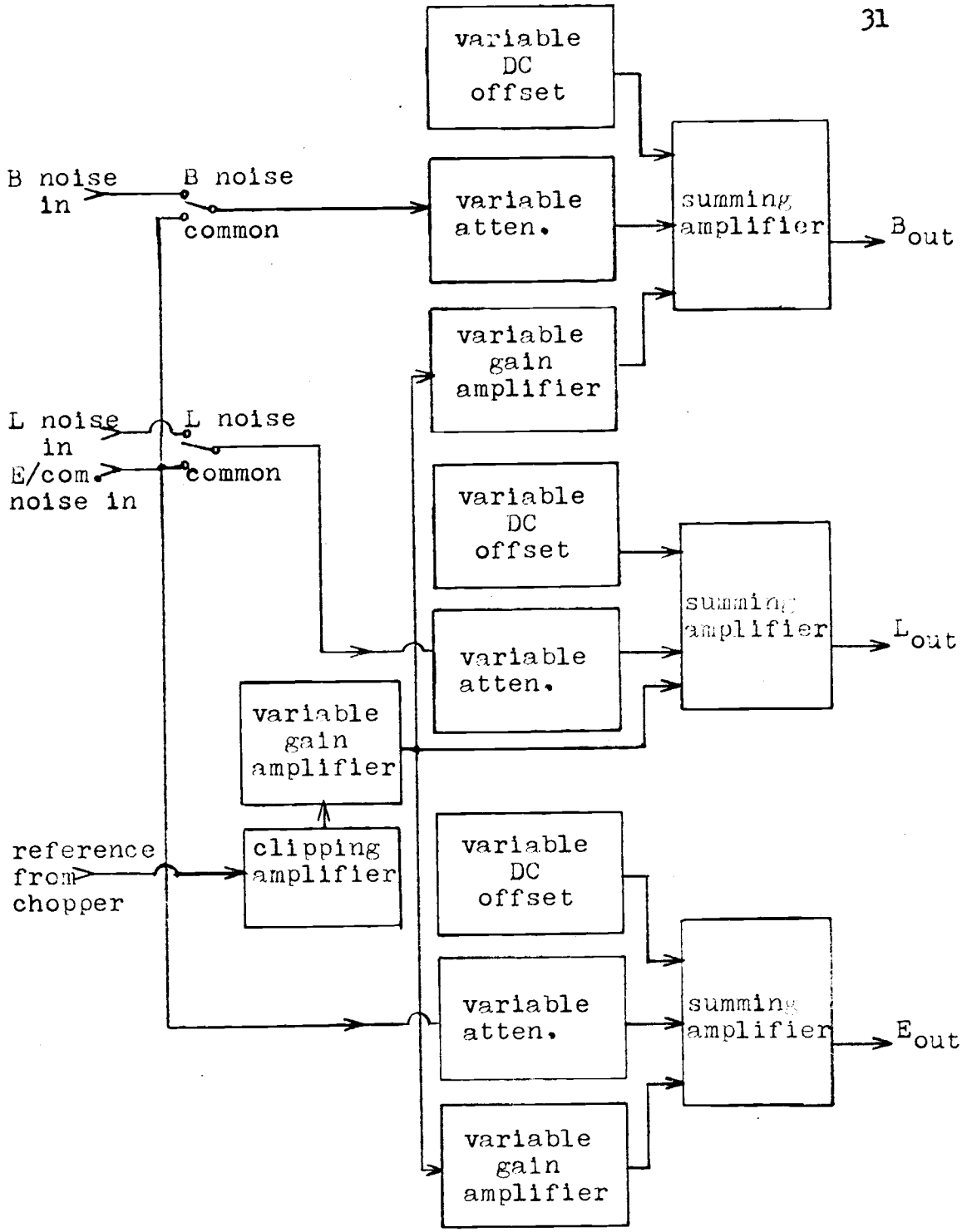

Figure 10. GUS Simulator

B paths allow independent adjustment of these signals. Noise and offset are added in with summing amplifiers. The three noise signals are independently variable and they may be derived from three separate inputs or one common input as desired. All three offsets are also independently variable.

This system can be used to adequately exercise the software by varying the offests, noise levels, simulated lamp intensity, and so forth. It also serves as a check on linearity since the ratio of $E - E_o$ to $B - B_o$ (see figure 2) should remain constant as simulated lamp intensity is varied.

Since no noise sources were conveniently available for use with the simulator, a dual noise source was designed to fulfill this need. A block diagram of the noise generator is shown in figure 11. Zener diodes are used for the source of the noise. A zener diode biased right at the knee where the zener effect begins is a good source of relatively white noise. This was verified by a spectral analysis. The zener sources are followed by two stages of amplification to increase the amplitude.

Some concern was expressed about 60 Hz noise especially in view of the fact that the chopper operates at 50 Hz, giving rise to the possibility of a 10 Hz beat frequency. For this reason it was decided to add a variable amount of

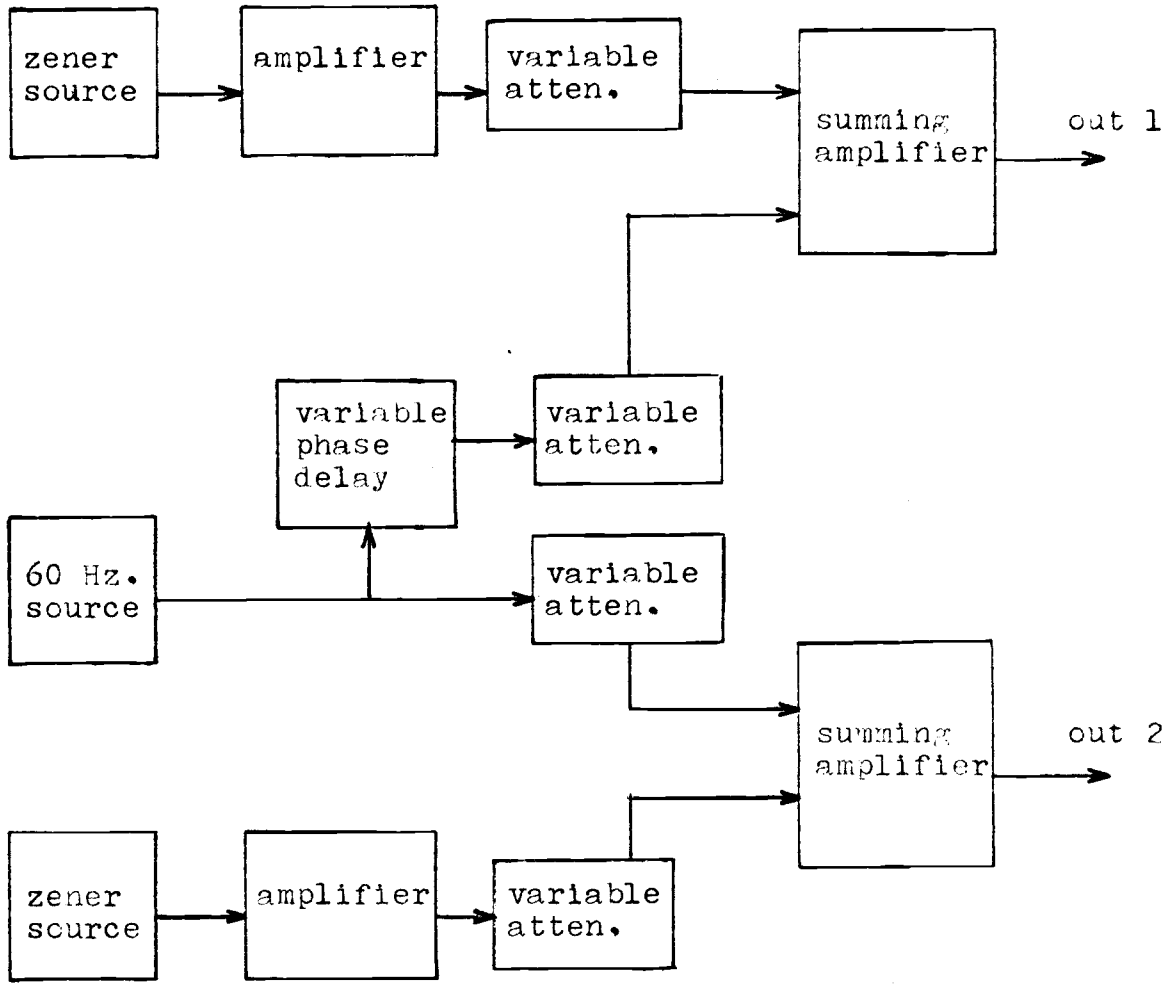

Figure 11. Dual Noise Generator

60 Hz, derived from the power line, to the noise sources via summing amplifiers. In addition, to add even more flexibility, a variable phase delay allowing adjustment over a 180° range was added to one of the 60 Hz noise signals. This arrangement allows thorough testing of the computer's ability to properly average out the noise.

Chapter 7

Signal Conditioning

In passing from the photomultiplier tubes to the computer, the GUS signals pass through two amplifying stages. The first stage is an electrometer. The electrometers change output current from the photomultipliers into voltage. The electrometer gains may be varied by switch selection of the feedback resistor. Following the electrometers are 100x preamps. The signals then pass from the preamp outputs to the multiplexer inputs on the computer. In addition the overall system gain may be changed by varying the supply voltage to the photomultiplier tubes. By properly setting the photomultiplier supplies and the electrometer gains, appropriate signal levels may be obtained for a wide range of sample fluorescence levels.

The electrometers and preamps were part of the GUS system that existed previous to this project and hence are not part of this thesis per se. However one problem does exist in this area. For extremely noisy signals it is possible to saturate the output of the preamp with noise while still having a very small component of true signal. Any amplifier saturation will cause erroneous data readings and therefore must be prevented. With this in mind it was

proposed that filters be placed between the electrometers and the preamps to reduce the noise entering the preamps.

To meet this need a Butterworth two pole active low pass filter was designed. A single feedback operational amplifier type was selected from the literature. Switch selectable cutoff points at 1 KHz, 2 KHz, 5 KHz and 100 KHz provide flexibility for the operator. The design equations were programmed on a small computer and several runs were made in an attempt to find readily available component values. As it turned out, for optimum filter performance the component tolerances are quite critical. Trimmer capacitors were added to the design to provide individual adjustment for each switch position. Since the filters invert the signal, an additional inversion must be inserted to maintain proper signal polarity (see page 17).

Chapter 8

Concluding Remarks

The system described in this paper was implemented gradually over the year of September 1971 through August 1972. With the exception of the polarizer rotation mechanism (to be added later) the entire system is operational and is in use.

A linearity check was performed by Enoch W. Small in the following manner. Wire mesh screens of different mesh size were placed between the lamp and the sample to vary the intensity of the light incident on a Rhodamine B sample. $E - E_o$ and $B - B_o$ were measured and printed out by the computer for the various lamp intensities. The results were linear to three significant figures over an amplitude range of 2500:1 and when extrapolated the data passed through the origin coordinates (0,0). Thus the overall system linearity appears to be excellent.

Initial sample runs exhibit excellent agreement with results collected by other investigators. However GUS is now believed to be the most advanced instrument of its type in existence and as confidence in its accuracy grows it may become the standard of comparison by which other instruments and methods are gauged.

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1. Ayres, William A., Enoch W. Small and Irvin Isenberg. A computerized fluorescence anisotropy spectrophotometer. Corvallis, Oregon, Oregon State University, Dept. of Biochemistry and Biophysics, 1972. (In preparation)

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7. Graeme, Jerald G., Gene E. Tobey and Lawrence P. Huelsman (eds.). Operational amplifiers - design and applications. New York, McGraw-Hill, 1971. 473 p.

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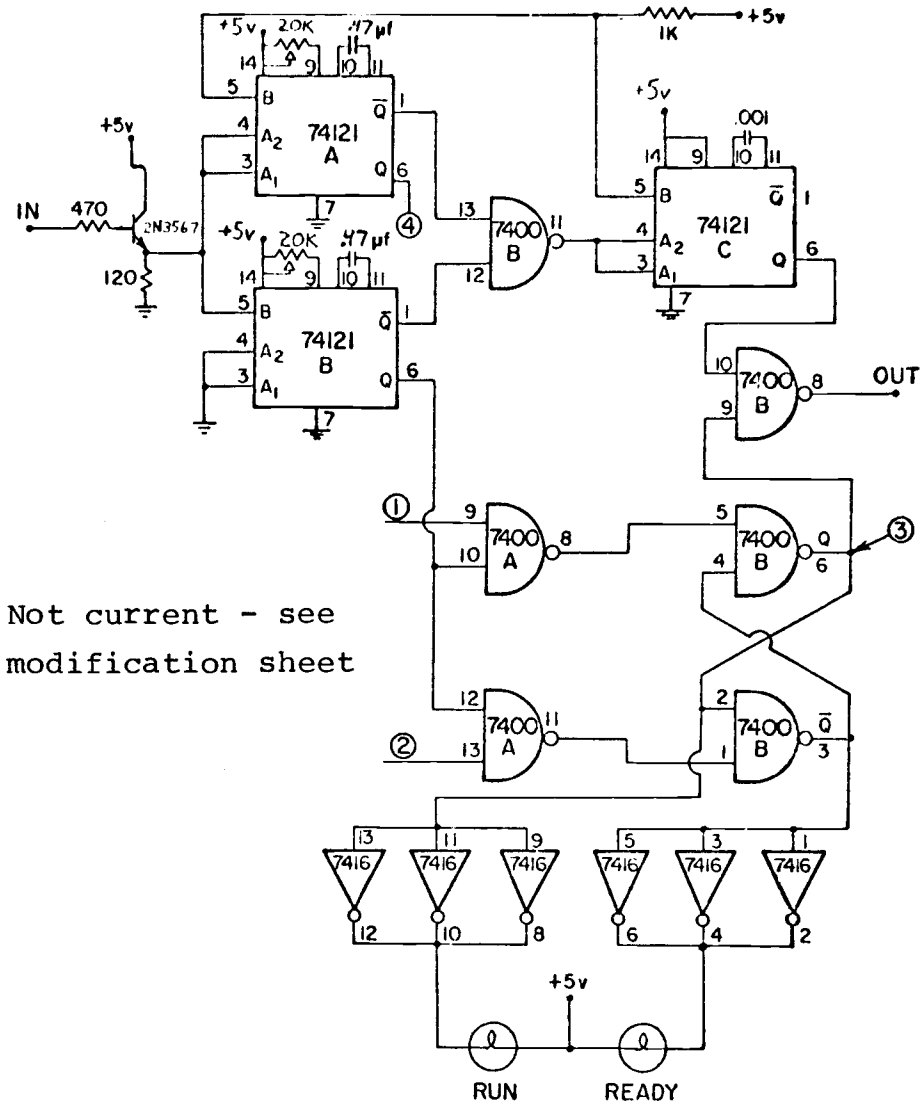
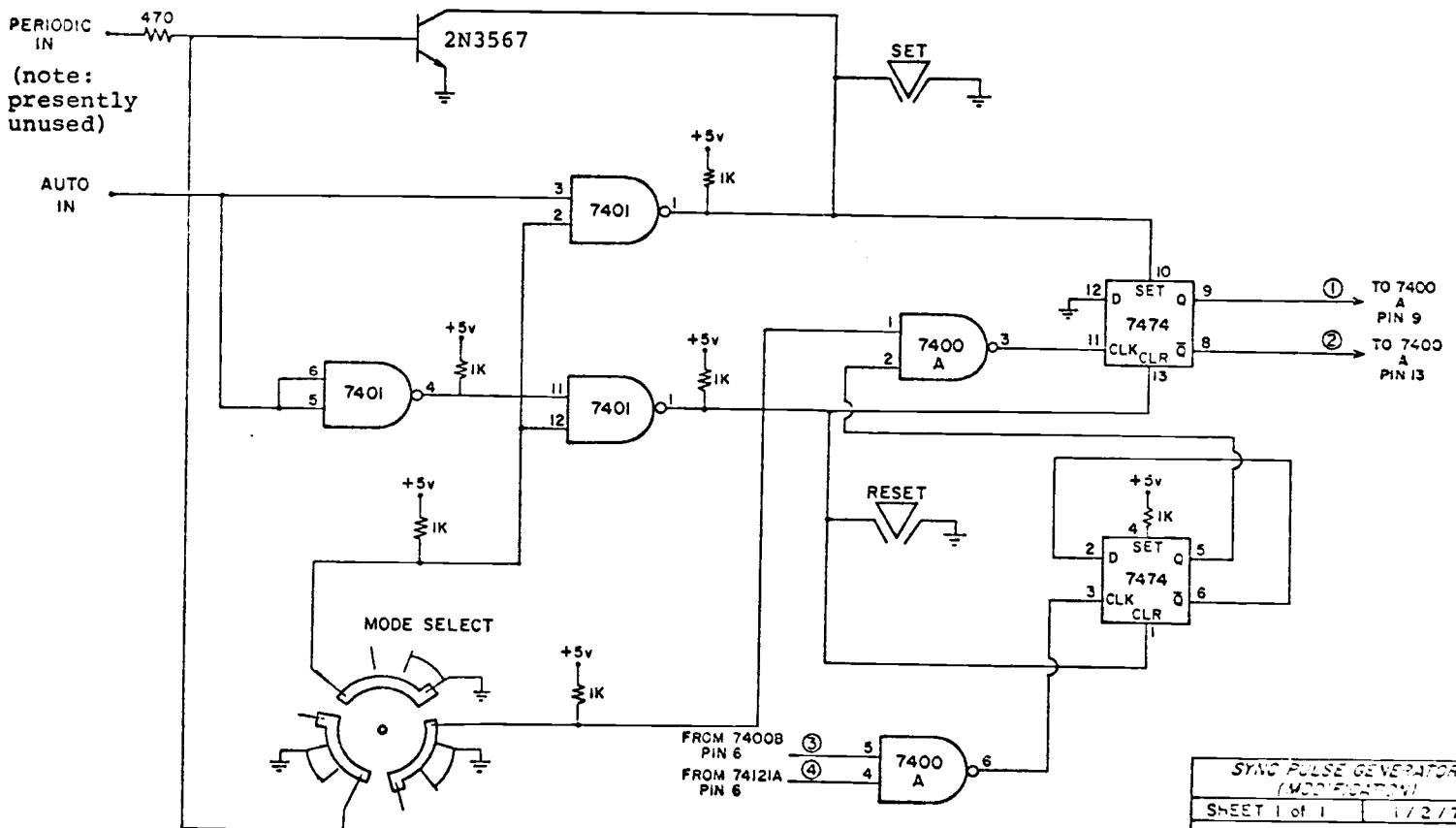
APPENDIX



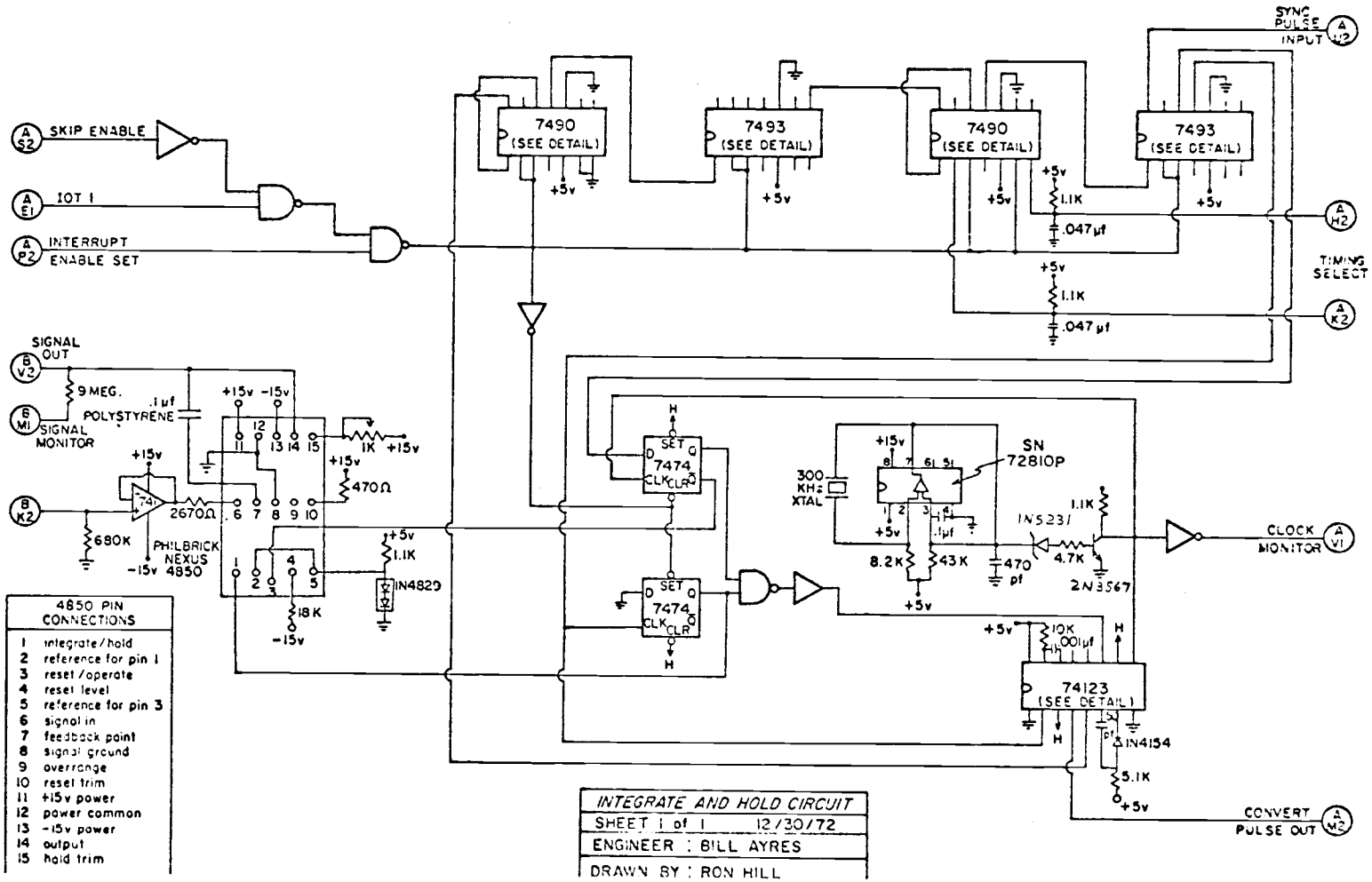
Not current - see modification sheet

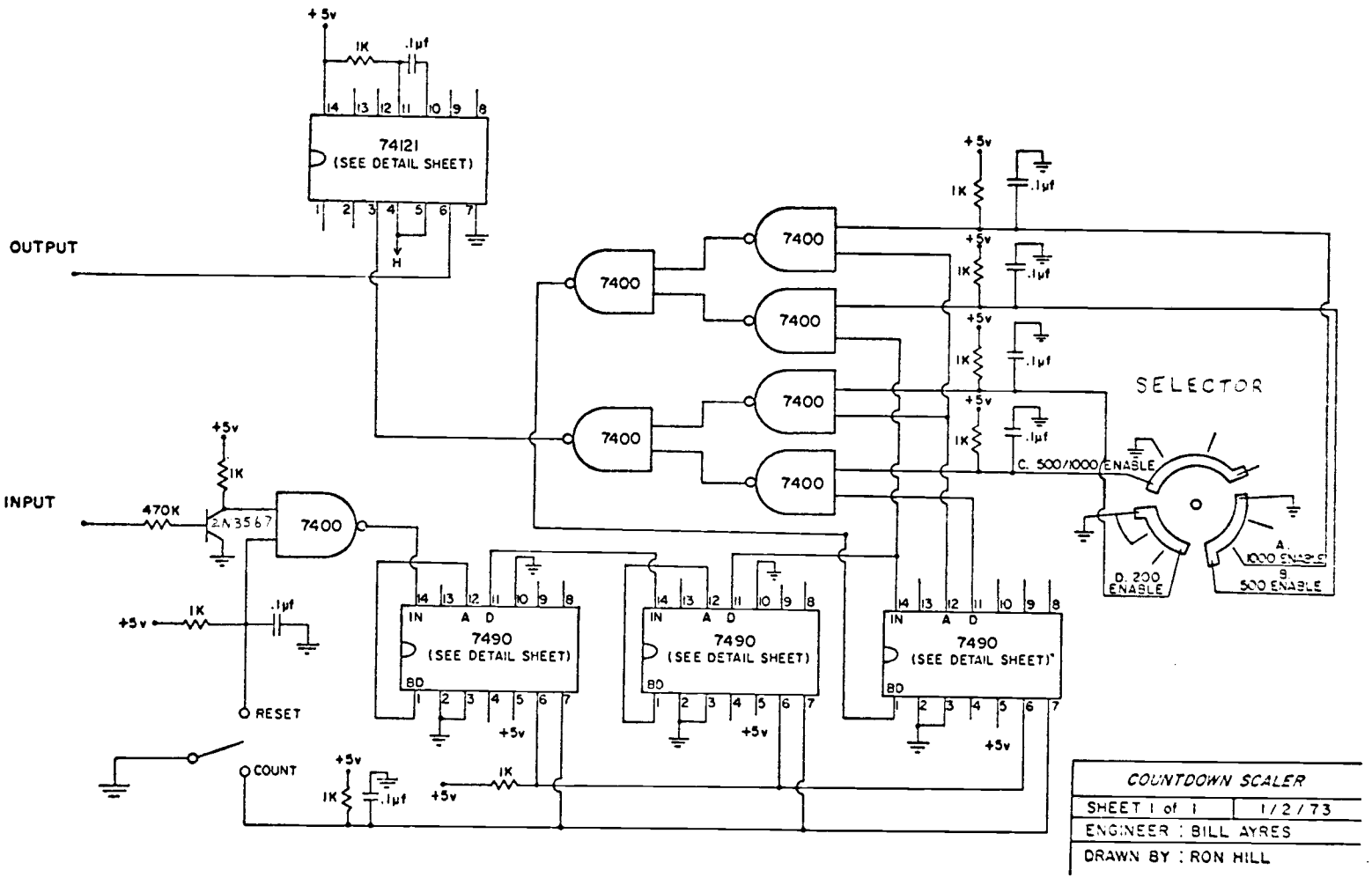
All IC's have +5v on pin 14 and ground on pin 7

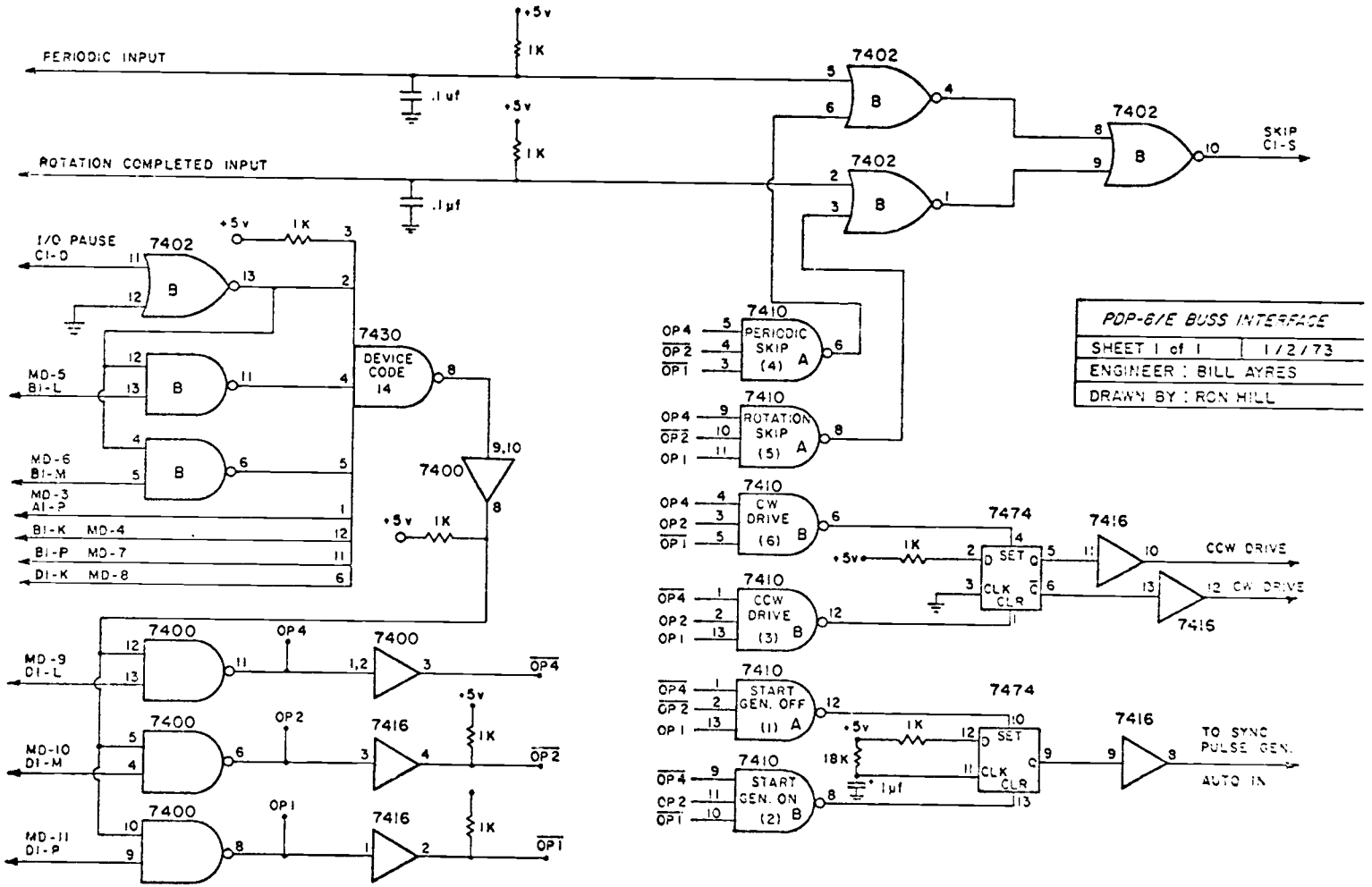
SYNC PULSE GENERATOR	
SHEET 1 of 1	12/2/1971
ENGINEER : BILL AYRES	
DRAWN BY : RON HILL	

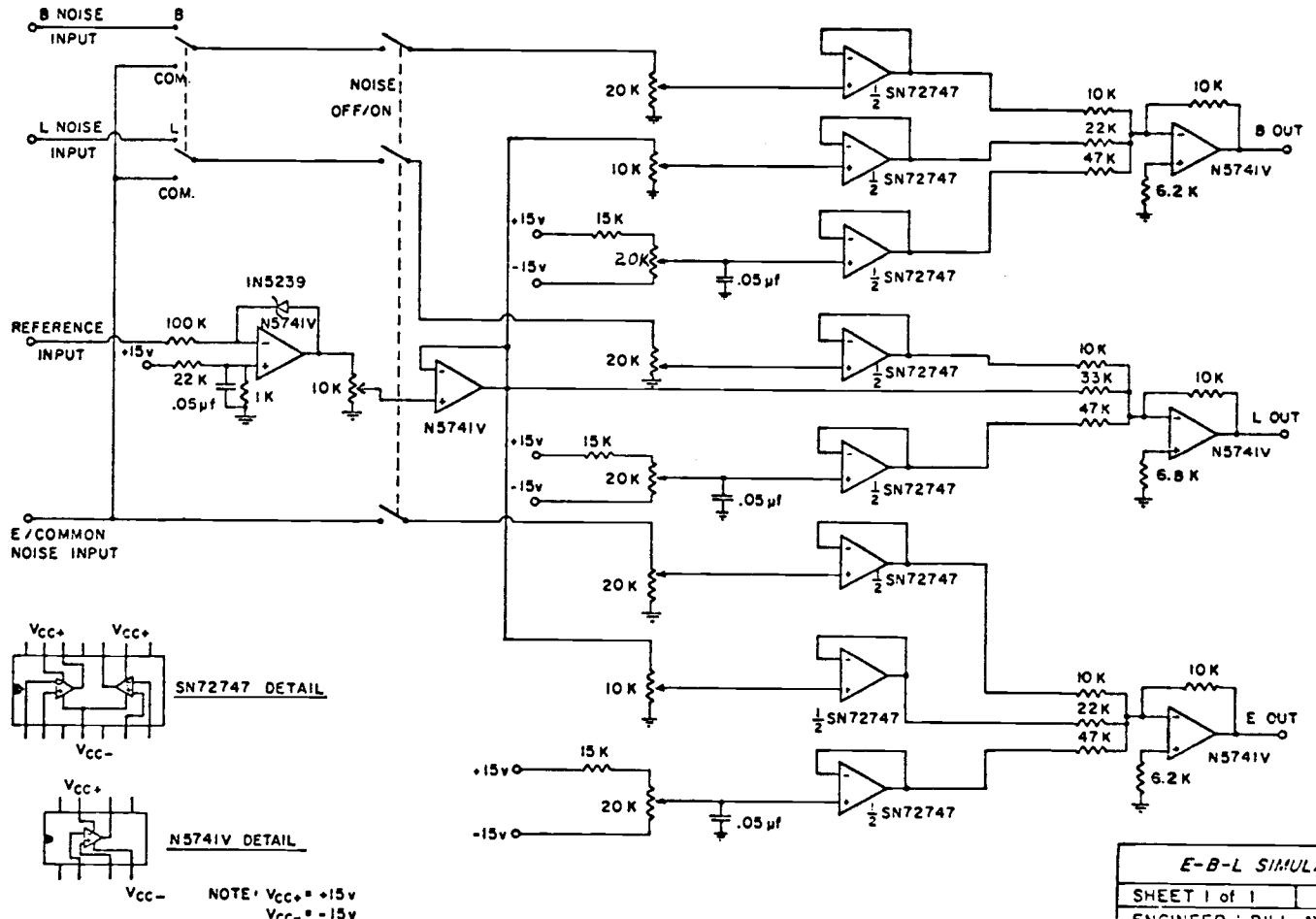


SYNC PULSE GENERATOR (MODIFICATION)	
SHEET 1 of 1	1/2/73
ENGINEER : BILL AYRES	
DRAWN BY : RON HILL	

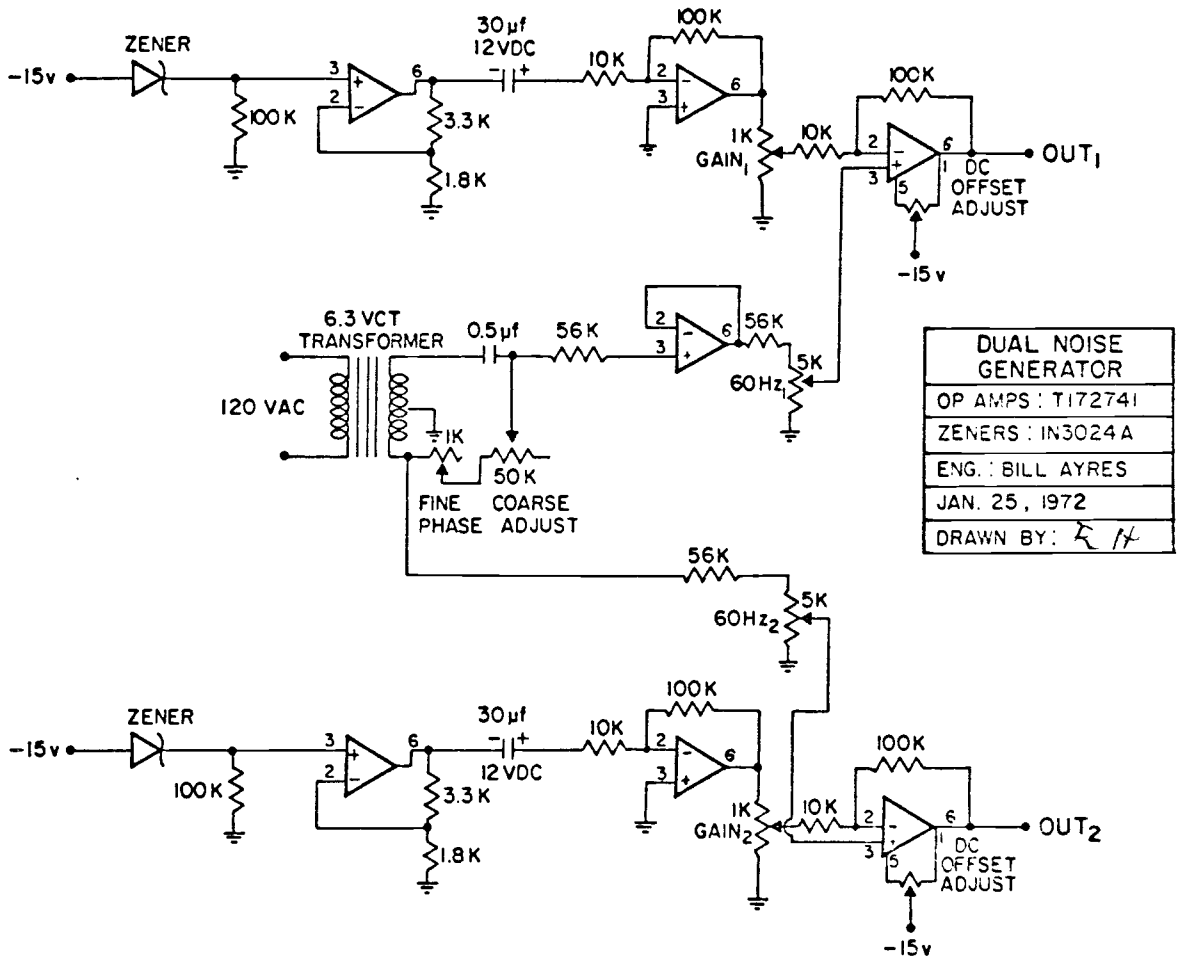

SYNC PULSE INPUT
A M2
SKIP ENABLE
A S2
IOT 1
A E1
INTERRUPT ENABLE SET
A P2
7490 (SEE DETAIL)
7493 (SEE DETAIL)
7490 (SEE DETAIL)
7493 (SEE DETAIL)
+5v
1.1K
.047 µf
A H2
TIMING SELECT
A K2
SIGNAL OUT
B V2
9 MEG.
.1 µf POLYSTYRENE
B M1
SIGNAL MONITOR
+15v -15v
1K +15v
470Ω
B K2
2670Ω
680K
PHILBRICK NEXUS 4850
-15v
18K
IN4829
7474
SET
CLR
H
300 KHz XTAL
SN 72810P
.1µf
IN5231
8.2K
43K
470 pf
4.7K
2N3567
CLOCK MONITOR
A V1
10K
.001µf
74123 (SEE DETAIL)
IN4154
5.1K
CONVERT PULSE OUT
A M3
4850 PIN CONNECTIONS
1 integrate/hold
2 reference for pin 1
3 reset/operate
4 reset level
5 reference for pin 3
6 signal in
7 feedback point
8 signal ground
9 overrange
10 reset trim
11 +15v power
12 power common
13 -15v power
14 output
15 hold trim
INTEGRATE AND HOLD CIRCUIT
SHEET 1 of 1 12/30/72
ENGINEER : BILL AYRES
DRAWN BY : RON HILL

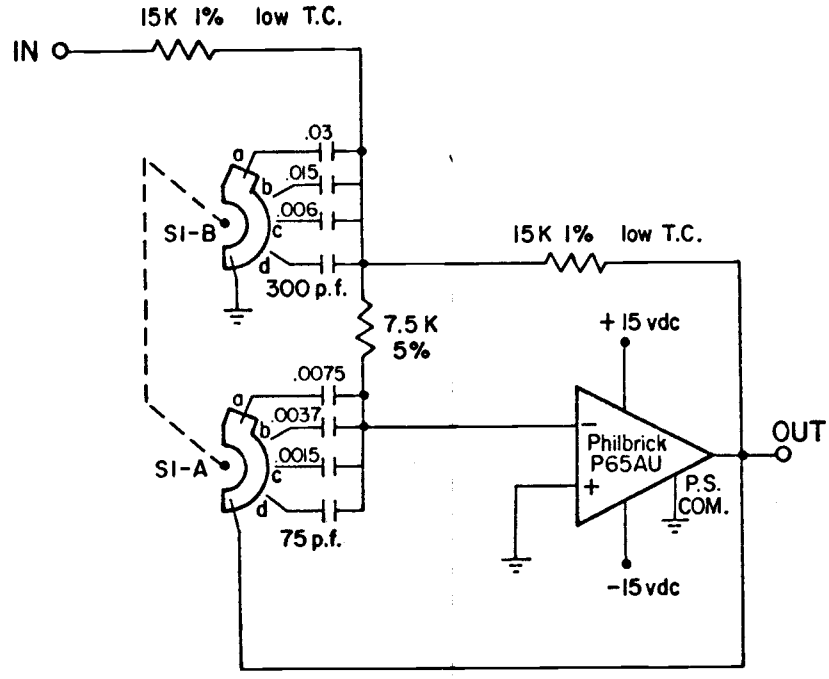

+5v
1K
.1µf
74121
(SEE DETAIL SHEET)
OUTPUT
H
7400
7400
7400
7400
7400
7400
SELECTOR
C. 500/1000 ENABLE
D. 200 ENABLE
A 1000 ENABLE
B 500 ENABLE
INPUT
470K
2N3567
RESET
COUNT
7490
(SEE DETAIL SHEET)
IN
A
D
BD
COUNTDOWN SCALER
SHEET 1 of 1
1/2/73
ENGINEER : BILL AYRES
DRAWN BY : RON HILL


FERIODIC INPUT
ROTATION COMPLETED INPUT
+5v
1K
.1 uf
.1µf
7402
7410
7430
7400
7474
7416
SKIP CI-S
I/O PAUSE CI-O
DEVICE CODE 14
PERIODIC SKIP (4) A
ROTATION SKIP (5) A
CW DRIVE (6) B
CCW DRIVE (3) B
START GEN. OFF (1) A
START GEN. ON (2) B
MD-5 BI-L
MD-6 BI-M
MD-3 AI-P
BI-K MD-4
BI-P MD-7
DI-K MD-8
MD-9 DI-L
MD-10 DI-M
MD-11 DI-P
OP4
OP2
OP1
CCW DRIVE
CW DRIVE
TO SYNC PULSE GEN.
AUTO IN
18K
1µf
PDP-6/E BUSS INTERFACE
SHEET 1 of 1
1/2/73
ENGINEER : BILL AYRES
DRAWN BY : RON HILL



E-B-L SIMULATOR	
SHEET 1 of 1	1/2/73
ENGINEER : BILL AYRES	
DRAWN BY : RON HILL	


-15v
ZENER
100K
3
2
6
3.3K
1.8K
30µf
12VDC
10K
100K
2
3
6
1K
GAIN1
10K
100K
2
3
6
1
5
DC
OFFSET
ADJUST
OUT1
-15v
6.3 VCT
TRANSFORMER
120 VAC
0.5µf
56K
2
3
6
56K
5K
60Hz1
1K
50K
FINE
PHASE
COARSE
ADJUST
56K
5K
60Hz2
DUAL NOISE GENERATOR
OP AMPS : T172741
ZENERS : IN3024A
ENG. : BILL AYRES
JAN. 25, 1972
DRAWN BY:
-15v
ZENER
100K
3
2
6
3.3K
1.8K
30µf
12VDC
10K
100K
2
3
6
1K
GAIN2
10K
100K
2
3
6
1
5
DC
OFFSET
ADJUST
OUT2
-15v

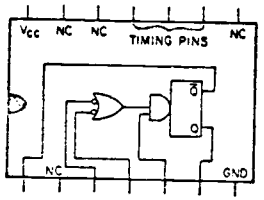


SWITCH POSITION	FILTER CUTOFF
a.	1000 Hz
b.	2000 Hz
c.	5000 Hz
d.	100 KHz

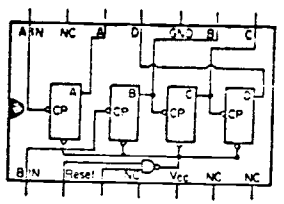
All capacitors in μf unless otherwise noted

All capacitors are nominal values. Trimming is required for optimum performance.

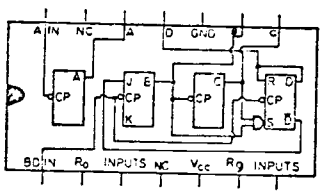
UNITY GAIN LOW PASS FILTER (INVERTING)	
SHEET 1 of 1	11/18/1971
ENGINEER : BILL AYRES	
DRAWN BY : RON HILL	



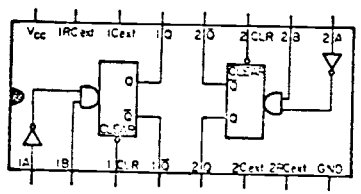
74121



7493



7490



74123

DETAIL SHEET	
SHEET 1 of 1	1/2/73
ENGINEER : BILL AYRES	
DRAWN BY : RON HILL	