In this thesis, a novel Direct-Charge-Transfer (DCT) integrator structure is proposed, which can settle much faster than regular switch-capacitor integrators. A new Spread-Spectrum Dynamic Element Matching (SS-DEM) algorithm is also introduced, which can effectively spread or shape the nonlinearity error of multi-bit DAC in the feedback path, thus improve the SNDR and THD performance of overall delta-sigma modulators. A three-bit quantizer design example is presented, which is embedded in a MASH2-0 structure delta-sigma modulator prototype and has been fabricated in AMI CMOS 1.5µm technology. Testing results indicate this quantizer works well.
A Study of Basic Building Blocks of Analog-to-Digital Delta-Sigma Modulators

by

Yuhua Guo

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Yuhua Guo, Author
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A STUDY OF BASIC BUILDING BLOCKS OF ANALOG-TO-DIGITAL DELTA-SIGMA MODULATORS

1 INTRODUCTION

1.1 Background and Motivation

Analog-to-digital conversion transforms a continuous-time, continuous-amplitude input into a discrete-time, discrete-amplitude output. Analog-to-digital converters (ADC) are very important building blocks as front ends in many digital processing systems [1]-[3]. Due to different applications, there are different ADC architectures to satisfy speed and accuracy requirements posed by whole systems. Oversampling analog-to-digital converter architectures become popular with the rapid advances in CMOS VLSI technologies because they offer high accuracy while avoiding the difficulty of implementing complex high-precision analog circuits in digital VLSI technology.

The basic idea of oversampling ADC is that it exchanges resolution in time for resolution in amplitude by modulating the analog signal into a low resolution code at a frequency much higher than the Nyquist rates, then removing the excess quantization noise by the following digital filters. So, oversampling ADCs is very suitable for CMOS VLSI digital technology because it is easier to realize high-speed digital circuit
with less power and area in modern VLSI technology, where high resolution analog components are not available, or hard to implement.

In the late 1980’s, the oversampling ADCs have found use in such applications as digital audio, digital telephony, and high-accuracy instrumentation, where the input analog signal bandwidth is not very high, usually below 100k Hz [4]. In recent years, high-speed data communications have become one of the most promising applications for IC industry. High-speed data communications, such as xDSL, require high resolution and wideband A/D converters with high dynamic range and high linearity [5]. Delta-sigma ADC can achieve high dynamic range and high linearity more readily than Nyquist-rate ADC such as pipelined and two-step ADCs. But the problem is that in these applications, the input signal bandwidth is in the range of several hundred kHFs to several MHzs. Therefore, we either need to increase the sampling frequency or reduce the oversampling ratio (OSR). However, reducing OSR will lead to a significant reduction in the signal-to-noise ratio and increasing the sampling frequency will introduce a lot of difficulties into circuit design. The other possible way is to increase the order of the modulators or the resolution of the quantizer. But increasing the order of modulators may introduce the stability issue, while in the case of multibit quantizer, the nonlinearity of multibit DAC in the feedback path may limit the performance of overall delta-sigma modulators. Hence, there must be some new circuit techniques to be invented to conquer these challenges.
1.2 Thesis Organization

The thesis is organized as follows: The basic concepts of delta-sigma ADCs are reviewed in Chapter 2; In Chapter 3, a novel direct-charge-transfer integrator is introduced, the advantage and drawback of which are also discussed in Chapter 3; in Chapter 4, a new method of dynamic element matching is described; next, we give a design-example of a 3-bit quantizer in Chapter 5, in which the process of circuit and layout design is presented and the chip is fabricated in AMI CMOS 1.5μm process; Finally, the conclusions and a summary of research are given in Chapter 6.
2 REVIEW OF DELTA-SIGMA MODULATION

2.1 Delta-Sigma Modulators Fundamentals

In this section, we will review some basic concepts and building blocks of delta-sigma modulators. A simple linear model of delta-sigma modulators is shown in Fig. 2.1.

\[ L_0(z) = \frac{G(z)}{H(z)} \]  
\[ L_1(z) = \frac{[H(z) - 1]}{H(z)} \]

where \( G(z) \) and \( H(z) \) are actually signal transfer function (STF) and noise transfer function (NTF) of delta-sigma modulators, which will further be explored below.

The output of the loop filter is
\[ Y(z) = L_0(z)U(z) + L_1(z)V(z) \]  

(2.3)

By modeling the error signal of quantizers \( e \) as \( E(z) = V(z) - Y(z) \), we can get the output of the modulator in terms of its input \( u \) and the error signal \( e \):

\[ V(z) = G(z)U(z) + H(z)E(z) \]  

(2.4)

Hence, Eq.(2.4) shows that a delta-sigma modulator’s output consists of independently filtered signal and noise components. Therefore, by choosing proper NTF and STF, we can reduce quantization noise in signal band while let STF be unity gain to pass the signal unchanged to get a good overall SNR performance of analog to digital converters. That’s the essence of noise shaping of delta-sigma modulation.

In general, the NTF and STF can be described by the loop filter parameters as follows:

\[ H(z) = \frac{1}{1 + L_1(z)} \]  

(2.5)

\[ G(z) = \frac{L_0(z)}{1 + L_1(z)} \]  

(2.6)

From the above equations, we easily see that we should make \( L_1(z) \) have high gain in the band of interest, and thus make it responsible for attenuating the quantization noise. Normally the desirable STF is flat over the band of interest. From the circuit design standpoint, it is convenient to use integrators as the fundamental active building block, especially for switched-capacitor realizations.
Next, we shall use a second-order delta-sigma modulator as an example to show the basic building blocks and some properties of delta-sigma modulators.

A simple second-order delta-sigma modulator is shown in Fig. 2.2. The modulator consists of two integrators and one quantizer in its forward path and the DAC in its feedback path. The quantizer is modeled as an adder, which sums its input signal and a quantization noise $e_i$. We can easily find the output $v[n]:$

$$v[n] = u[n-1] + (e[n] - 2e[n-1] + e[n-2])$$

The corresponding $z$-domain function is:

$$V(z) = z^{-1}U(z) + (1 - z^{-1})^2 E(z)$$

Comparing (2.8) with (2.4), we find that the signal transfer function is simply a delay, thus, the input signal is passed to the output after one clock cycle delay; but the noise transfer function is a second-order difference function, so the modulation noise now is the second difference of the quantization noise. In the frequency domain, the spectral density of this noise is
\[ N(f) = E(f)(1 - e^{i\omega T})^2 = E(f)(4\sin^2(\omega T / 2)) \] (2.9)

Hence, we can easily get the noise power in signal band as [6]:

\[ P_n = \frac{\pi^4}{5} \frac{1}{\Delta^2} \frac{\Delta^2}{12} \] (2.10)

Here we assume that the quantization noise is a white noise, the average quantization noise power is \( \Delta^2 / 12 \), where \( \Delta \) is the least significant bit (LSB) of the quantizer. From (2.10), we see that for a second-order delta-sigma modulator, each doubling of OSR results in 15 dB increase in dynamic range, which is 2.5 extra bits of resolution.

Actually this technique can be extended to higher order predictions by adding more feedback loops. For an L-th order delta-sigma modulator with a similar structure, the output is given by:

\[ V(z) = z^{-1}U(z) + (1 - z^{-1})^L E(z) \] (2.11)

The above equation shows that the noise transfer function NTF(z) is now an L-th order difference. In the frequency domain, the spectral density of noise is given by:

\[ N(f) = E(f)[2\sin(\omega T / 2)]^L \] (2.12)

For an L-th order delta-sigma modulator, each doubling of oversampling ratio OSR results in approximately \((6L+3)\) dB dynamic range increase, which is corresponding to \((L+0.5)\) bit/octave.
From above discussion, we find that via integrators in the forward path, delta-sigma modulators shape the spectrum of the quantization noise, placing most of the energy outside the signal band. Therefore, we can achieve a very good SNR performance and a very large dynamic range. From (2.12), it seems that we can get as large dynamic range as we want just by increasing the order of delta-sigma modulators or the oversampling ratio or the resolution of quantizer to reduce the quantization noise, but the modulator will suffer from a number of problems such as stability, nonlinearity introduced by the multi-bit DAC, slew-limited integrator settling etc. We discuss each of these issues below.

2.2 Design Issues of Delta-Sigma Modulators

In this section, we will discuss some design issues related with delta-sigma modulators, especially when a wide-bandwidth and high-resolution delta-sigma ADC is required. For each problem, we will review some solutions published in recent years and analyze the advantages and drawbacks of those solutions.

2.2.1 Stability

If the order of delta-sigma modulators is very large, the modulator can achieve very high dynamic range even at relatively low oversampling ratio, which is very attractive for broadband communications applications. However, the reality is that if the modulator’s order is greater than 2, the modulator may exhibit large and unbounded states and a poor SNR performance because the input to the quantizer goes
beyond the quantizer’s normal range, which means the quantizer is overloaded and the modulator becomes unstable. The potential to go unstable is a big drawback of high-order delta-sigma modulators. Because of the quantizer is a highly nonlinear element, the stability of higher-order modulators is not well understood. Some of the empirical principles have to be introduced to direct the design. One of the rule of thumb is keeping the peak frequency response gain of the noise transfer function NTF(z) less than 2. This often results in a stable delta-sigma modulator [7]. It should be noted that this stability criterion is often too conservative, as it eliminates many actually stable modulators.

Since single stage higher-order modulators have stability issues, especially when large input signals are present, another approach for realizing higher-order modulators is to use a cascade-type structure, which consists of lower-order modulators only. Such an arrangement has been called MASH (Multi-stAge noise Shaping) structure, as shown in Fig.2.3.

In this structure, the overall delta-sigma modulator is not a single loop, but consists of several lower-order single-loop modulators, each with its own quantizer. Each single-loop modulator in the cascade converts the quantization noise from the preceding modulator. The errors of all but the last single-loop modulator are then digitally canceled.
Fig. 2.3 Block diagram of MASH structure modulator

Cascaded delta-sigma (MASH) data converters offer a good compromise between high accuracy, robust stability and speed. However, they are very sensitive to analog circuit imperfection, because they rely on the accurate matching of the transfer functions of two internal signal paths, which means that the opamp gain could not be so relaxed as in the single-stage modulator, and the capacitor ratio defining the gain of integrators should be very accurate, too.

2.2.2 Nonlinearity of Multibit DACs

One-bit noise shaping modulators usually are popular because of the fact that they employ a one bit internal DAC that is inherently linear, and thus does not require precision component matching [4] [8]-[10]. However, in the case of wide-bandwidth and low OSR, the resolution that a 1-bit delta-sigma modulator can achieve is limited. One solution to the above problems is to use a multibit quantizer in the oversampled
converter loop. The primary advantage of noise-shaping modulators employing multibit quantizers is that the ratio of the total quantization noise power to the signal power at the modulator’s output is drastically reduced from that of a 1-bit modulator; typically by 6 dB per additional bit. Also, much more aggressive NTF may be used, further reducing the inband noise. Therefore, we can increase the overall resolution of any oversampled data converter without increasing the oversampling ratio, simply by increasing the number of levels in the internal data converters. Equivalently, the multibit noise-shaping coder can achieve resolution comparable to that of a single-bit modulator at a lower sample rate.

Although the multibit topologies offer a good improvement of the resolution, even at a low oversampling ratio, they impose severe linearity requirements on the DAC in the feedback path [11][12]. In [4][13][14], they point out that the integral linearity of a noise-shaping conversion system is no better than the integral linearity of the multibit internal DAC. Therefore, a number of techniques have been developed to achieve high linearity while requiring only modest component matching. These techniques include Dynamic Element Matching (DEM)[11][12], digital correction [15]-[17] and dual-quantizer architectures [18]. But some technique is still too complicated or need to consume more hardware or power, so we still need to find some simple and efficient way to solve this problem.
2.2.3 Settling and Slewing of Integrators

When dealing with wide-bandwidth delta-sigma modulator design, people may think “why not just increase the sampling frequency to keep OSR the same high as that in audio applications.” That’s because with the increase of clock frequency, it is more and more difficult to design a high-speed operational amplifier to make integrators fully settle in such a short period of time. For example, in ADSL application, the input signal bandwidth is about 1.1 MHz. If we still let the OSR be 128, then the sampling frequency should be about 281 MHz. If we use switched-capacitor circuit to implement this modulator, we need to make the opamp’s unity-gain-bandwidth about five times larger than the clock frequency [19], that’s about 1.4 GHz. It is a great challenge to design such a high bandwidth opamp, especially with a reduced voltage supply from 5 V to 3.3 V or even 1.8 V.

And more importantly, if the integrator is slew-limited, it will introduce an increase in both quantization noise and harmonic distortion at the output of delta-sigma modulators [6], which adds more difficulty to opamp design because of the high slew-rate requirements.

Hence, in order to achieve high-speed and high resolution, people have to decrease the oversampling ratio and use higher-order modulators and multibit quantizer in the feedback loop to alleviate the stringent requirements posed on the opamp design. However it is still necessary to increase the sampling frequency of the converter, as well as to reduce the oversampling ratio to maximize the signal
bandwidth of an delta-sigma converter. Therefore, some new integrator design
techniques need to be developed to meet the settling and slewing requirements with a
simple and low power opamp.
3 DIRECT-CHARGE-TRANSFER INTEGRATORS

In delta-sigma modulators, the integrators in the forward path play an important role, serving to accumulate the large quantization noise that result from the quantizer. Ideally for an delaying integrator, the output \( v(kT) \) is the sum of the previous output \( v(kT-T) \) and the previous input, \( u(kT-T) \):

\[
v(kT) = g_o u(kT - T) + v(kT - T)
\]  

(3.1)

The constant \( g_o \) represents the gain scaling the input to the integrator. The above equation corresponds to the following transfer function for an ideal integrator:

\[
H(z) = \frac{g_o z^{-1}}{1 - z^{-1}}
\]  

(3.2)

3.1 Conventional Parasitic Insensitive Integrators

A popular switched-capacitor implementation of the integrators is shown in Fig.3.1.

![Fig. 3.1 A parasitic insensitive switched-capacitor integrator](image)
This topology allows switched-capacitor circuits to be designed in a parasitic-
insensitive manner, with the integrator virtual ground receiving the charge stored on a
variety of capacitors. The transfer function of this integrator is given as below:

\[ H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \] 

(3.3)

Comparing Eq.(3.3) with Eq.(3.2), we can see that the integrator’s gain \( g_0 \) is
determined by the ratio of sampling capacitor \( C_1 \) and the integrating capacitor \( C_2 \),
which can be set quite precisely in an integrated circuit (on the order of 0.1 percent).
Actually gain variations of as much as 10 percent of nominal value has only a minor
impact on the performance of single-stage delta-sigma modulators [6]. However, in
cascaded delta-sigma modulators, they are more sensitive to the gain mismatch
because they rely on the accurate matching of the transfer functions of two internal
signal paths. Hence, the nonidealities in integrators will introduce mismatch between
the analog NTF and the digital NTF, which will cause quantization noise leakage, and
degrade the SNR performance of the overall delta-sigma converter. Besides the
capacitor mismatches, there are some other very important issues related to opamp
design, which need to be taken care of:

1) Finite Gain of Opamp

The dc gain of the ideal integrator described by (3.3) is infinite, however, in
practice, the gain is limited by circuit constraints. Assuming the opamp’s dc gain is
denoted by \( A \), the integrator transfer function is given by [20]:
\[ H(z) = \frac{(C_1 / C_2)z^{-1}[1-1/A-C_1/(AC_2)]}{1-[1-C_1/(AC_2)]z^{-1}} \] (3.4)

From (3.4), we find that the finite gain of the opamp will make the integrator lossy, and introduces a gain error into integrator’s transfer function. Usually, the gain error related to finite opamp gain is smaller than that of capacitor mismatch and is negligible. But the phase error caused by finite opamp gain shifts poles horizontally, which is more important because it introduces noise leakage to the band of interest. If we ignore the gain error introduced by finite opamp gain and simplify (3.4), we can get

\[ H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1-\alpha z^{-1}} \quad (0 < \alpha < 1) \] (3.5)

The dc gain is finite and given by:

\[ H_{dc} = H(1) = \frac{C_1 / C_2}{1 - \alpha} \] (3.6)

The limited gain at low frequency reduces the attenuation of the quantization noise in the baseband, and consequently results in an increase of the in-band quantization noise for the delta-sigma modulators. In Boser’s structure [6], he pointed out that the performance penalty incurred is on the order of 1dB when the integrator dc gain is comparable to the oversampling ratio (OSR). So the dc gain of opamps should be at the order of 40-60 dB to meet this requirement. Though a pole error doesn’t have too much effect on the performance of a single-loop modulator, for cascaded delta-sigma modulators, it turns out that a pole error will cause a leakage of noise to the
overall modulator output [21]. Therefore the dc gain of opamps used in cascaded modulators usually is far above 60 dB.

2) Finite Bandwidth of Opamp

As well known, in typical switched-capacitor circuits, a general rule of thumb is that the unity gain bandwidth of the operational amplifier should be at least five times larger than the clock frequency [19]. This requirement is more and more difficult to meet because the clock frequency keeps increasing with the increase of input signal bandwidth, though some low-OSR structures of delta-sigma modulators alleviate the problem a little. Considering the requirements of finite gain of opamps in subsection 1, it is really hard to achieve a low-power opamp with both high gain and large bandwidth.

Actually, the settling time depends both on the unity gain bandwidth of opamp and the feedback factor $\beta$, which is defined as in the case of Fig. (3.1)

$$\beta = \frac{C_2}{C_1 + C_2}$$

(3.7)

If we use a first-order opamp model, which has a 90-degree phase margin, we find that the time constant of the closed-loop amplifier $\tau$ is given by

$$\tau = \frac{1}{\beta \omega_{UGB}}$$

(3.8)

where $\omega_{UGB}$ is the unity gain bandwidth of the opamp. So the step response for the closed-loop amplifier is given by:
\[ V_{\text{out}}(t) = V_{\text{step}}(1 - e^{-t/\tau}) \]  

From (3.9), we find that if \( \beta \) is very small, the settling time will be prohibitively long, which will limit the accuracy the integrator can achieve at the sampling instant.

3) Finite Slew-Rate of Opamp

Actually, the settling issue is not the most critical, because for delta-sigma modulators, inaccurate settling will not impair the performance too much as long as the settling process is linear; in another word, the settling must not be slew-rate limited. But if the settling is slew-limited, it will introduce distortion and degrade the performance of the overall delta-sigma modulator. Therefore, we must make the opamp’s slew rate high enough to avoid slew-limited settling, which adds more difficulty to design a low power opamp to meet all the requirements of regular parasitic insensitive integrators.

3.2 Direct-Charge-Transfer Integrators

From the discussion above, we found that there are many difficulties to design a low-power opamp with high gain and large bandwidth and slew rate. So we will introduce a novel direct-charge-transfer integrator here to overcome all the difficulties by just adding a simple buffer to the circuit. The topology is shown in Fig.3.2.
Fig. 3.2 A direct-charge-transfer integrator

The circuit basically works in this way. In the sampling phase $\phi_1$, the charge stored on the capacitance $C_1$ is $C_1(V_{in}[kT - T] + V_{out}[kT - T])$; the charge stored on the capacitance $C_2$ is $C_2V_{out}[kT - T]$. When $\phi_2$ goes high, the circuit enters its integrating mode. At the end of $\phi_2$, the charges on the capacitance $C_1$ and $C_2$ is $C_1V_{out}[kT - T/2]$ and $C_2V_{out}[kT - T/2]$ respectively. We can write the charge conservation equation:

$$C_1(V_{in}[kT - T] + V_{out}[kT - T]) + C_2V_{out}[kT - T] = (C_1 + C_2)V_{out}[kT - T/2]$$

(3.8)

Also note that:

$$V_{out}[kT] = V_{out}[kT - T/2]$$

(3.9)

We can combine (3.7) and (3.8) to write:
\[ V_{out}[kT] = \frac{C_1}{C_1 + C_2} V_{in}[kT - T] + V_{out}[kT - T] \]  
(3.10)

Taking the z-transform of (3.9), we also have

\[ V_{out}(z) = \frac{C_1 z^{-1}}{C_1 + C_2} V_{in}(z) - z^{-1} V_{out}(z) \]  
(3.11)

From (3.10), we can finally find the transfer function \( H(z) \) given by

\[ H(z) = \frac{C_1}{C_1 + C_2} \frac{z^{-1}}{1 - z^{-1}} \]  
(3.12)

Comparing (3.12) with (3.2), we notice that the transfer function realizes its gain coefficient still as the ratio of two capacitances, and thus the transfer function can be accurately defined in an integrated circuit, the same advantage as that in regular integrator structure. And what’s more, this new structure has some other advantages over the regular structure in its settling behavior.

First, in this direct-charge-transfer integrator, the feedback factor is always 1 both in sampling phase and integrating phase, not like in the case of regular integrator, where the feedback factor is smaller than 1 in integrating phase, which means we can fully make use of the bandwidth of opamp and let the integrator settle much faster than regular ones.

Second, the more important thing is that we don’t need to worry too much about the slew rate of opamp because in direct-charge-transfer integrator, the charges in \( C_1 \) and \( C_2 \) are actually redistributed between themselves. To verify this, just
observe the negative input of opamp (virtual ground) when sampling capacitor C1 flips over the opamp. There is no current flow into or out this node because this is a high impedance node. So the opamp doesn’t need to provide large current to charge the integrating capacitors, which makes the opamp’s slew rate requirement much relaxed compared with regular switched-capacitor integrators. Therefore, we can easily design a low power opamp to meet the settling and slewing requirements of integrators for the small price of a buffer. As to the negative sign associated with the buffer, we don’t need to really design a inverter buffer because in practical design, we usually have use fully differential topology, the negative sign actually just means cross coupling of the opamp’s output.

Fig. 3.3 An inverting direct-charge-transfer integrator
Fig. 3.3 also shows an inverting version of direct-charge-transfer integrator, whose operation is very similar to the non-inverting version.

Though the DCT integrators have the advantages on settling and slewing, there are some other issues we need to pay attention to with this new structure. First of all, in the sampling phase, we need to sample the input signal between the input and the output buffer instead of ground, which means if the input signal changes very fast, we also need to design a high-speed buffer to meet the requirements of sampling. Second, if the buffer’s gain is smaller than one, the pole of the DCT integrator will move into the unit circle, which means the integrator will become lossy.

Fig. 3.4 A fully differential DCT switched-capacitor integrator
To overcome this, we can move the buffer into the feedback loop to compensate the buffer's gain, as shown in Fig.3.4. In this case, the buffer actually can be looked upon as a part of the opamp.

3.3 Simulations and Comparison

To verify the above observation, we will simulate these two integrator structures in HP CMOS 5V 0.5μm process and compare their performances.

Fig. 3.5 Simplified schematic of a two-stage opamp
In switched-capacitor circuits, opamps usually are realized by folded-cascode structure or telescopic structure because of the purely capacitive loads of opamps. In our simulation, we choose telescopic structure because it consumes less power than folded-cascode structure. The buffer is just a simple source-follower to drive the output load. The simplified schematic is shown in Fig.3.5.

From Fig.3.5, we can actually consider the overall circuit as a two-stage opamp, in which the telescopic first stage provides a high DC gain, and the second buffer stage provides current in the sampling phase of DCT integrator. Because the first stage is no longer driving the output load, the power consumption in the telescopic portion can be made negligible to the second buffer stage.

The frequency compensation is contained within the first stage. Also note that a Common-Mode-FeedBack (CMFB) circuit should be included in the opamp to stabilize the opamp’s output common-mode voltage. A more detailed schematic of this two-stage opamp is shown in Appendix A.

Using HP 0.5μm CMOS model and Spectrel of Cadence, we can get the frequency response of the opamp as shown in Fig.3.6. The simulated opamp DC gain is about 70dB, the unity-gain-bandwidth is about 250MHz and phase margin is about 60 degree.
To compare the performance of DCT integrators and regular integrators, we choose $C_1=C_2=1\mu F$ for the DCT structure and $C_2=2C_1=2\mu F$ for the conventional one, to make the transfer functions the same. We choose the clock frequency 100 MHz to make the settling behavior of these two structures more obvious.

From the simulation results shown in Fig.3.7, we find that DCT integrators can settle much faster than the regular ones. At the end of integrating clock phase, the regular structure only just finish slewing and enter linear settling mode, but for DCT structure, it already fully settles to the final value.
Hence, DCT integrators have the superior settling behavior than regular structure integrators, especially in the case that the clock frequency is very high and the opamp bandwidth is relatively small.

Fig. 3.7 Comparison of the output signals of a DCT integrator and a conventional integrator

But we also need to notice that in the sampling phase, the output of DCT integrators will have some small glitches because the opamp has to provide the current to charge the sampling capacitor. We should make sure the opamp output has enough time to settle back to the original value.
4 SPREAD-SPECTRUM DYNAMIC ELEMENT MATCHING

One-bit noise-shaping modulators were popular because of the inherently linearity of one-bit DAC in the feedback path of modulators. However, as shown in Chapter 2, the resolution that a one-bit delta-sigma modulator can achieve at a given oversampling ratio is limited. One solution is to use a multibit quantizer in the delta-sigma converter loop, but the linearity of the overall system will be limited by the linearity of the multibit internal DAC. Therefore, achieving high linearity and low total harmonic distortion (THD) appears to require precisely matched components, which need element trimming and thus increase the manufacturing costs. The other possible approaches are digital calibration or dynamic element matching (DEM).

In general, digital calibration is based on converting the noise due to nonlinear DAC error into a digital form, and then canceling it in the digital domain. Dynamic element matching is to convert a dc error into a wide-bandwidth noise by choosing different elements to represent a digital input code at different time. Digital calibration will not be covered in this thesis. We will briefly review several DEM algorithms and afterwards we will introduce a novel algorithm, which can do the DEM with very simple circuitry as compared with conventional DEM methods.

4.1 Conventional DEM Algorithm

The idea behind DEM is to select the DAC elements in such a way that DAC’s nonlinearity error is randomized or even noise-shaped. Tones caused by DAC nonlinearity are suppressed and noise in the baseband is filtered. There are many DEM
algorithms [11] [22]-[28]. Depending on the element selecting schemes, these algorithms can provide simple randomization, first-order noise shaping or second-order noise shaping of the DAC non-linear error. Fig. 4.1 shows a very simple 3-bit thermometer-coded DAC using a randomization DEM algorithm as an example.

![Diagram of a three-bit dynamic element matching DAC](image)

**Fig. 4.1 A three-bit dynamic element matching DAC**

As shown in Fig. 4.1, the randomizer block determines which unit capacitances will be used, which effectively spreads the nonlinearity of DAC over the whole frequency range. Therefore, the mismatch error has been converted into a white noise. Note that although the delta-sigma modulator shapes the quantization noise, the internal DAC mismatch noise is not affected by the feedback loop and is not shaped.
However, in oversampling analog-to-digital converters with high OSRs, nearly all the mismatch noise power is out of signal band, and hence can be filtered out.

Although the randomization DEM approach described above reduces the effective nonlinearity of DAC, it increases the noise floor in the signal band, and thus decreases the in-band SNR. By choosing the DAC elements in a particular way, the DAC mismatch errors can be noise-shaped instead of being evenly spread out over the entire spectrum. Data weighted averaging (DWA) is a typical algorithm [11] [25], as shown in Fig.4.2.

In the diagram shown in Fig.4.2, by placing a barrel shifter between the thermometer decoder and the unit elements, DAC elements are selected in a circular fashion. Hence, we can see that the DWA algorithm actually modulates the nonlinearity error around sub harmonics of the sampling clock frequency by making the mismatch noise a periodic signal instead of making the element mismatch noise white. It is easy to show that the mismatch shaping transfer function is \((1-z^{-1})\) for this barrel shifter type DWA algorithm. But since the DAC elements are rotated through repeatedly, it is possible that DAC mismatch errors can form a periodic pattern, which can introduce tones in the signal band. To reduce the tones, sometimes a small dither is needed.
4.2 Spread-Spectrum DEM Technique

This new idea is borrowed from spread-spectral communication. In spread-spectral communication, people first modulate the input signal with a pseudorandom number to spread the signal energy over the whole spectral range before transferring it to a channel. Though the channel will introduce all kinds of noise, we still can use the same pseudorandom code to extract the signal because the noise introduced by the channel is uncorrelated with the signal. The block diagram of spread-spectral communication is shown in Fig. 4.3.

![Fig. 4.3. Diagram of spread-spectrum communication](image)

So we can use the similar approach to turn the DAC nonlinearity into white noise. As shown in Fig. 4.4, we use a one-bit pseudorandom number to modulate the input signal to the DAC, and then with the same pseudorandom number, we demodulate the
signal from the output of DAC. The nonlinearity error of DAC is spread over the whole sampling frequency range, most of which will be removed by the subsequent decimation filter. We call this spread-spectrum dynamic element matching (SS-DEM).

Fig. 4.4 A new randomization DEM algorithm

Using Simulink, we build a simple model to simulate the performance of a classical second-order modulator with or without SS-DEM algorithm. The resolution of internal quantizer and DAC is 5 bits. To match the precision the state-of-the-art process can achieve, the DAC is 10-bit linear. We choose the clock frequency to be 100MHz and the oversampling ratio to be 64. The input signal $u$ is a 24.4 kHz 0.9V sine wave. The simulation results with SS-DEM are shown in Fig. 4.5.
Fig. 4.5 Spectra of a second-order delta-sigma modulator with SS-DEM algorithm:
(a) Spectrum and histogram of $y_{i1}$, the input to the DAC;
(b) Spectrum and histogram of $y_{i2}$, the output of the DAC;
(c) Spectrum and histogram of $v_m$, the output of the overall modulator;
(d) Power Spectra Density and histogram of $d_i$, the one-bit dither signal
Fig. 4.6 and Fig. 4.7 show the second-order delta-sigma modulator without DEM and the corresponding simulation results. Comparing Fig. 4.5 with Fig. 4.7, we can find that the spectra of the input and output of DAC with SS-DEM now looks like white noise, which means the nonlinearity of the internal DAC has been spreaded over the whole frequency range. The SNDR performance with and without SS-DEM is 69.5 dB and 65.6 dB, respectively. Therefore, there is about 4 dB improvement of SNDR with SS-DEM algorithm.

Note that we only use very simple circuitry to achieve this. For the modulation part, because it is applied in digital domain, it is very easy to implement one-bit multiplication. For the demodulation part, though it’s in analog domain to do the multiplication, we only need to exchange the clock phase on the switch to reference voltage in circuit implementation.

![Fig. 4.6 A regular second-order delta-sigma modulator without DEM](image_url)
Fig. 4.7 Spectra of second-order delta-sigma modulator without DEM:
(a) Spectrum and histogram of $y_1$, the output of the first integrator;
(b) Spectrum and histogram of $y_2$, the output of the second integrator;
(c) Spectrum and histogram of $v_m$, the output of the overall modulator;
In the case of high-speed application, the time allocated to DEM algorithm execution sometimes is less than one clock period. Thus, the DEM algorithm to be used must be fast and simple. Therefore, SS DEM is a very attractive choice compared with other complicated DEM algorithm.

Like in the DWA algorithm, we can also make the dither’s power spectral density first-order shaped to reduce the nonlinearity introduced by the DAC in the signal band, and further improve the overall delta-sigma modulator’s performance. The first-order noise-shaping SS DEM algorithm is shown in Fig. 4.8.
Fig. 4.9. Spectra of a second-order delta-sigma modulator with first-order SS-DEM algorithm:
(a) Spectra and histogram of $y_{i1}$, the input to the DAC;
(b) Spectra and histogram of $y_{i2}$, the output of the DAC;
(c) Spectra and histogram of $v_m$, the output of the overall modulator;
(d) Power Spectra Density and histogram of $d$, the one-bit dither signal

The first-order pseudorandom generator is actually a one-bit first-order digital delta-sigma modulator. Because it is only one bit, the circuit complexity doesn’t increase too much. The simulation results of 1st order SS DEM are shown in Fig. 4.9.
From Fig. 4.9. we can find that the spectrum of the input and output of DAC with SS-DEM now is first order noise-shaped and there is another 3 dB improvement of SNDR compared with no noise-shaping SS DEM algorithm. For different DAC accuracy values, the SNDR performance is summarized in Fig. 4.10. With 1st-order noise shaping SS DEM, the SNDR performance usually can improve 7 to 12 dB depending on the DAC accuracy.

![SNDR vs. DAC Linearity for no DEM, SS DEM, 1st order SS DEM](image)

**Fig. 4.10 SNDR vs. DAC nonlinearity for no DEM, SS DEM, 1st order SS DEM**

Actually we can easily implement second-order noise-shaping SS DEM in a similar way to further improve the SNDR performance. But one should notice that the
SNDR difference between first-order and second-order DEM algorithm is insignificant when the oversampling ratio is low (below 32) [29]. Hence, second-order algorithm is more suitable for applications with high oversampling ratio. In the case of low OSR, we need to use more advanced and complicated digital correction algorithm to estimate and then cancel it in digital domain [17].
5 MULTI-BIT QUANTIZER DESIGN

The quantizer is also an important building block in delta-sigma modulators, because it serves to quantize an analog signal in the loop and provides the digital output of the modulator. But since the quantizer appears after the loop gain block and before the output terminal, nonidealities associated with it are shaped by the loop in the same way that the quantization noise is shaped. This means that, at the frequencies of interest, the quantizer nonidealities are reduced the most.

Even though the quantizer nonidealities are reduced by the noise shaping properties of the loop, there are still some circuit design issues to take care of. The most important issues are comparator metastability and hysteresis, which will be discussed in this chapter. And since quantizers are mixed-signal circuits and their outputs are actually digital signals, we need to reduce the coupling from the digital part to the analog signal when we lay out and route the circuits on the chip.

In this chapter, we will present an example of 3-bit quantizer’s circuit and layout design, which is used in the first stage of a MASH 2-0 delta-sigma modulator prototype. The design issues of both circuit and layout are discussed in detail.

5.1 Three-bit Quantizer Circuit Design Example

The multi-bit quantizer in delta-sigma modulators is usually realized by flash structure ADCs, because the resolution of the multi-bit quantizer is usually less than 5-
bits, which can be easily implemented by flash architecture with a high conversion speed and reasonable power consumption.

Fig. 5.1 is a block diagram of an n-bit flash ADC. The circuit consists of $2^n$ comparators, a resistor string comprising $2^n$ equal segments and a decoder.

![Block diagram of an n-bit flash A/D converter](image)

The string subdivides the main reference into $2^n$ equally spaced voltages, and the comparators compare the input signal with these voltages. Consequently, the comparator outputs constitute a thermometer code, which is converted to binary by the decoder. Usually, flash ADC only needs one clock period to finish the analog to digital conversion, hence typically achieve higher speed than other ADC structures.
The most important and crucial blocks of flash ADCs are the comparators. They are often the limiting components in the design of high-speed data conversion systems, due to their finite accuracy, comparison speed and power consumption. However, in delta-sigma modulators, the quantizer input is subject to noise shaping, thus designing a comparator of a multi-bit quantizer for a delta-sigma modulator is much easier than that for a Nyquist rate ADC. The offset voltages of the comparators in delta-sigma modulators are not very critical since they only contribute to dc offsets or nonlinearity error of quantizer, which will both be noise-shaped out of signal band by the overall delta-sigma loop.

Therefore in this 3-bit quantizer design example, we only chose a regular high-speed switched-capacitor comparator structure, in which offset canceling techniques are not employed.

![Switched-capacitor comparator structure](image)

Fig. 5.2 The switched-capacitor comparator structure
As shown in Fig. 5.2, the comparator stage is implemented with the differential switched-capacitor structure. This switched-capacitors sample reference voltages during clock phase of \( \phi_1 \) and compare the difference of 
\[
(V_{in+} - V_{in-}) - (V_{ref+} - V_{ref-})
\]
during clock phase of \( \phi_2 \). Though the design of this 3-bit quantizer can be very relaxed due to the noise shaping property, we still don’t want to increase the quantization noise too much because it will reduce the dynamic range of the delta-sigma loop. If the nonlinearity of a quantizer is worse than its resolution, the quantizer will be non-monotonic, causing problems in delta-sigma loop. Hence, we choose the size of capacitors used in the switched-capacitor comparator to be 1 pF for good matching. The comparator must resolve the magnitude of 1/2 LSB, in this case, 125mV \( (V_{LSB}=V_{ref}/8, \text{ where } V_{ref}=2V) \), which will be not too difficult to achieve.

In this design, we chose a low-power, high-speed dynamic latch comparator appropriate for use in conventional and delta-sigma ADCs [30]. The comparator circuit is depicted in Fig. 5.3.

As shown in Fig. 5.3, the comparator includes three stages: a preamplifier, a CMOS latch circuit, and an S-R latch. The preamplifier is just a simple differential input pair M1 and M2, which not only amplifies the input signal but also suppresses the kick-back noise from the regeneration latches. The CMOS latch is composed of a NMOS flip-flop M4 and M5 with a pair of NMOS transfer gates M8-M9 for strobing, an NMOS switch M12 for resetting, and a PMOS flip-flop M6-M7 with a pair of
PMOS precharge transistors M10-M11. The output S-R latch will hold the comparison result during the whole clock period for the convenience of following encoding logic.

![Schematic of the CMOS latch comparator](image)

**Fig. 5.3 Schematic of the CMOS latch comparator**

This comparator has two working modes: reset mode and regeneration mode:

During $\phi_2$, the comparator is in the reset mode. Current flows through the closed resetting switch M12, which forces the previous two logic state voltages to be equalized. After the input stage settles on its decision, a voltage proportional to the input voltage difference is established between node a and b. This voltage will act as the initial imbalance for the following regeneration time interval. In the meantime, as
the NMOS flip-flop is reset, the PMOS one is also reset by the two closed precharge transistors, which charge nodes c and d to the positive power supply voltage.

When $\phi_1$ goes low, the comparator enters its regeneration mode. The first step of regeneration is within the time slot between $\phi_2$ getting low and $\phi_1$ getting high, in which the NMOS flip-flop regenerate the voltage difference between nodes a and b. The second regeneration step starts when $\phi_1$ gets high and M8 M9 are closed. The NMOS flip-flop, together with the PMOS ones regenerates the voltage differences between nodes a and b and between nodes c and d. The voltage difference between node c and d is rapidly amplified to a voltage swing nearly equal to the power supply voltages. The following S-R latch is driven to full complementary digital output levels at the end of regeneration mode, and remains in the previous state in the reset mode.

As discussed at the beginning of this chapter, flash ADCs are susceptible to metastability errors. Since metastability error is one of limitation in the design of flash ADCs, we need to analyze the comparison mechanism closely in order to prevent its occurance.

The comparison process can be approximately analyzed using a small-signal model as shown in Fig.5.4. In this model, $g_{m1}$, $g_{m4}$ are the transconductances of M1 or M2, M4 or M5; Ron is the on-resistance of reset switch M12; $C_a$ represents the capacitance at node a or b. All mismatches are ignored in this simple model.
We can derive two differential equations as follow:

\[ \frac{1}{2} V_{in} g_{m1} = C_a \frac{dV_a}{dt} + g_{m4} v_b + \frac{(v_a - v_b)}{R_{on}} \]  

(5.1)

\[ -\frac{1}{2} V_{in} g_{m1} = C_a \frac{dV_b}{dt} + g_{m4} v_a - \frac{(v_a - v_b)}{R_{on}} \]  

(5.2)

In (5.1) and (5.2), \( V_a \) and \( V_b \) stand for the increments relative to the voltage at nodes a and b with zero input difference. Subtracting (5.1) from (5.2) and solving it, we have:

\[ v_{ab} = [v_{ab0} - \frac{g_{m1}}{2g_{on} - g_{m4}} v_{in}]e^{\frac{-t}{\tau}} + \frac{g_{m1}}{2g_{on} - g_{m4}} v_{in} \]  

(5.3)

where \( g_{on} = 1/R_{on} \), \( \tau = C_a/(g_{m4} - 2g_{on}) \).

In (5.3), \( V_{ab} \) represent \( V_a - V_b \) and \( V_{ab0} \) is the initial voltage difference at nodes a and b. Expression (5.3) shows that when \( g_{on} \) is smaller than half of \( g_{m4} \), the time
constant $\tau$ becomes positive and the regeneration process starts. Note that if $V_{ab0}$ is very small at the sampling instant, the time for $V_{ab}$ to reach a certain value, which is interpreted as a valid logic level, will be very long. This is so called “Metastability” phenomenon.

From (5.3), we can conclude that the most efficient way to prevent metastable error occur is to minimize the time constant $\tau$. When M12 is turned off, the time constant only depends on the capacitance at node a or b and the transconductance of M4 or M5. The capacitance is related to the sizes of M1, M2, M4, M5, M8, M9, and M12. So there is a trade-off to choose these sizes, because if M4 and M5 are made wider to increase $g_m$, the capacitance at nodes a and b will also increase. Note that the size of M12 also directly affects the resetting speed, which is related to another very important issue in comparator design: hysteresis.

It is shown in (5.3) that the initial voltage difference $V_{ab0}$ is very important in the decision of the regenerative direction. Imperfect resetting will make $V_{ab}$ retain its polarity before the regeneration is activated, so the comparator output will follow residues left from the previous cycle. This phenomenon is so called “hysteresis”.

From above discussion, we conclude that in order for a comparator to respond correctly, we need to allow two phenomena to complete: regeneration of logic levels and resetting of the preamplifier output.

In this specific design example, the clock frequency is about 2 MHz, which means that one clock phase is about 250 ns long. Though the process is AMI CMOS
1.5 µm, a very slow process, we still can meet the requirements very easily. With the help of SPICE simulations, we can choose the transistor sizes as follow:

\[
\begin{align*}
W_1 &= W_2 = 16\mu m, & W_4 &= W_5 = 4\mu m, & W_6 &= W_7 = 5.6\mu m, & W_{12} &= 4\mu m \\
W_8 &= W_9 = 4\mu m, & W_{10} &= W_{11} = 5.6\mu m, & W_{13} &= 40\mu m, & I_b &= 30\mu A
\end{align*}
\]

All the transistors’ lengths are \(L=1.6\mu m\) to minimize parasitic capacitances.

Fig. 5.5 Simulation results of comparator’s internal node a and b

Fig. 5.5 shows the simulation results of the comparator in this design. The simulated transient analysis shows that the comparator can still perform correct comparison with a 1-mV input signal for a sampling rate of 20 MHz with a reference current 30\(\mu A\).
From Fig. 5.5, we can find that the comparator can fully regenerate to valid logic values even for input signal much smaller than 1 LSB and clock frequency much higher than 2MHz. So the probability for metastability occurring is very small. And also note that node a and b’s voltages can be reset in 5 ns, which can meet the requirement for preventing comparator hysteresis.

5.2 Three-bit Quantizer Layout Design

For high performance analog mixed-signal circuits, layout is a very important issue. A bad layout will introduce unnecessary large parasitic capacitances in signal paths or large mismatches between components, etc, thus degrading the overall system performance.

Therefore, in order to make a good layout, several important issues must be taken considered carefully:

1) On-chip noise coupling

It is very important to avoid on-chip noise coupling through the substrate into the signal and reference paths of delta-sigma modulators. For example, if the noise at multiples of the sampling clock frequency gets on the input lines or feedback DAC lines, this noise will be aliased down to near dc, and will be indistinguishable from the low-frequency input signal. So, guard rings and shielding N-wells should be placed all over the chip to reduce substrate noise coupling.
2) Symmetry

Even by doing all these shielding, it is still very difficult to shield a circuit entirely from noise coupling. So the best way is the use of differential circuitry. It is very important for the layout of a differential circuit to be as symmetric as possible because in this case both sides will be disturbed by the substrate in a symmetrical fashion, thus the noise just appears as a common-mode disturbance.

3) Matching

Common-centroid layout techniques, dummy transistors, dummy capacitors and dummy resistors are often used to improve the matching of analog components. It may add extra area and interconnects to do so, but it will greatly reduce the offset, gain error and nonlinearity introduced into the systems.

Besides all these, there are a lot of other layout techniques to suppress the noise coupling and improve the matching, which will not be discussed here in detail.

The 3-bit quantizer’s layout is shown in Fig. 5.6. The layout size is about 2000μm×1000μm. As shown in Fig. 5.6, the bias and the resistor string are placed as far as from the digital output of the comparators and the bubble correction part. Notice that the n-well shield is being used under the capacitors and resistor strings to minimize noise coupling. Notice also that the clock lines are placed at the top of the layout and a separate well is placed under the clock lines as a shield, too.
5.3 Experimental Results

An experimental prototype MASH 2-0 structure delta-sigma modulator was designed and fabricated, in which this 3-bit quantizer was embedded inside the first stage of the delta-sigma modulator prototype. As mentioned before, a 1.5μm double-poly n-well CMOS technology was used. Fig. 5.7 shows the microphotograph of the
experimental chip, in which the bubble correction part of the quantizer was removed because of limited die area.

Fig. 5.7 Microphotograph of the experimental chip
The measured output signal of the overall delta-sigma modulator is shown in Fig. 5.8. The clock frequency we used for test is 1 MHz and the input signal is a 10 kHz sine-wave signal. We collected totally 65536 points, only part of which is shown in Fig. 5.8.

The frequency spectrum of the first stage output is also shown in Fig. 5.9, in which we can clearly see the noise-shaping property of the delta-sigma modulator. Note that the output of the delta-sigma modulator is also the output of the internal quantizer. Hence, the experimental chip proves that this 3-bit quantizer can work correctly and meet the requirement of the whole system.
Fig. 5.9 Frequency spectrum of the first-stage output of the ΔΣ modulator
6 CONCLUSIONS

6.1 Summary

In this thesis, the design issues of basic building blocks (integrators, DACs, quantizers) in oversampling delta-sigma modulators are discussed. A novel Direct-Charge-Transfer (DCT) integrator structure is proposed, which can settle much faster than regular switched-capacitor integrators. The DCT integrator can be implemented with an opamp having just a moderate bandwidth and low slew rate, which is very advantageous for low-voltage and low power design. A new Spread-Spectrum Dynamic Element Matching (SS-DEM) algorithm is also introduced, which can effectively spread or shape the spectrum of the nonlinearity error of multi-bit DAC in the feedback path, and thus improve the SNDR and THD performance of the overall delta-sigma modulators. A three-bit quantizer design example is also presented, in which the design issues of comparators, like metastability and hysteresis, are explored closely. The layout consideration is discussed briefly and the three-bit quantizer is embedded in a MASH 2-0 structure delta-sigma modulator prototype, which has been fabricated and proved to work well.

6.2 Future work

In Chapter 3, we show that the DCT integrators have superior settling behavior over regular switched-capacitor integrators. However, there are still some issues in the sampling phase of this DCT integrator because we have to include a high-speed buffer
to provide large current to charge the sampling capacitors. Though the opamp’s slewing and settling requirements become relaxed and power consumption is thus reduced, the power consumption of the buffer make this idea less attractive because sometimes the buffer’s power consumption dominates. Therefore, we still need to find some new circuit technique to solve this problem.

For SS-DEM algorithm, we have proved its feasibility in theory and verified its function through MATLAB system-level simulation. Future work is needed to further verify this algorithm by some circuit-level simulations, or even silicon-level testing.
BIBLIOGRAPHY


APPENDICES
APPENDIX A. Schematics for the Simulation of DCT and Conventional Switched-Capacitor Integrators

Fig. A.1 Schematic of the two-stage opamp used in simulations

Switched-Capacitor Integrators

APPENDIX A. Schematics for the Simulation of DCT and Conventional

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Fig. A.2 Schematic of the conventional switched-capacitor integrator
Fig. A.3 Schematic of the DCT integrator
APPENDIX B. Schematics of 3-bit Quantizer

Fig. B.1 Schematic of the 3-bit flash ADC
Fig. B.2 Schematic of the switched-capacitor comparator
Fig. B.3 Schematic of a latched comparator