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Terri. S. Fiez Kartikeya Mayaram

Analog-to-digital converters (ADCs) are the key building block for sensor applications, such as wireless communications and digital electronics. These applications require ADCs to have medium to high accuracy (normally from 10-14 bits) and relatively low signal bandwidth (ranging from 100Hz-150kHz). Since these applications are often powered by batteries, high power efficiency of the ADCs is one of the biggest challenges of the design. Recently, noise-shaping SAR ADCs have been used inside of a delta-sigma modulator to achieve relatively high resolution while maintaining excellent power efficiency. However, the passive noise shaping from the SAR ADC can cause low frequency quantization noise leakage, which degrades the ADC accuracy. Additionally, the maximum noise shaping order has been limited to second order in reported passive noise shaping SAR ADC works.

To achieve a higher order noise transfer function (NTF) and reduce the in-band quantization noise leakage, a single opamp-based third-order delta-sigma modulator with a 4-bit noise-shaping SAR quantizer is proposed in this work. Designed with a

65nm CMOS technology, the simulated prototype modulator attains 84.5dB SNDR over 50kHz signal bandwidth sampled at 3.2MH. The power consumption of the ADC is 50.7μW. The simulation results demonstrate the power efficiency of the proposed modulator for sensor network and portable device applications.

Power Efficient Hybrid Architecture for High Resolution Analog-to-Digital Converters

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APPROVED:

Co-major Professor, representing Electrical and Computer Engineering

Co-major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Hui Zhang, Author

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Life at Oregon State University has been a significant part of my life. When I first came to OSU for college, I had no idea what I wanted to do as my career. Seven years passed by and I am so grateful that I have met so many friends and mentors. Now I'm ready to graduate and start my career as a circuit designer. I wish to take a moment to express gratitude to some of these important individuals.

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I want to say thank you to all my peer researchers. I would like to thank Ankur, Siladitya, Hossein, Hamid, Justin, Kyle, Ramin, and Ravi. Being around them made

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DEDICATION

I would like to express my deepest gratitude to my family for their sacrifices and support over the years. I would like to dedicate this thesis to my parents, Guanxiang Zhang and Yunhua Yin. Despite being far away in China, they provided unconditional support and understanding no matter what I want to pursue in my life. I want to thank my uncle, Ruming Yin, my aunt, Xiaolan Chen, and my lovely cousins Jared and Owen for treating me as a family member and taking great care of me while I was in the United States. I can't express enough appreciation in words and I wouldn't be standing here as I do today without their love and support.

Chapter 1. Introduction

1.1 Motivation

As semiconductor technology evolves, more functions can be integrated onto a system-on-chip (SoC). This is particularly true for sensor applications that may integrate sensors, an analog interface, and digital processing. As shown in Figure 1.1, typical sensor applications range from environmental monitoring to medical diagnoses [1]-[5]. In a wireless sensor network, hundreds of sensor nodes are capable of self-organizing into a collaborative network, and subsequently benefit from spatial diversity through data sharing and multi-hop connectivity. The analog-to-digital converter (ADC) is a key building block in the system to convert physical signals in the environment to digital signals that can be processed later by computers. These applications require ADCs that have medium to high accuracy (normally from 12 to 16 bits) and relatively low signal bandwidth (ranging from 100 Hz-150 kHz) [5]. Power efficiency is one of the biggest challenges because the sensors nodes and devices are often battery powered with the requirement that they last for a long period of time. Usually, a power consumption of less than 100 μW from the ADC is desired. SAR ADCs have excellent power efficiency since they avoid power-hungry analog circuitry. However, the best power efficiency is achieved for 10-12 bit accuracy [6]-[8]. For resolutions beyond 12 bits, the capacitor size increases exponentially, which increases the area and power dramatically [18], [24]. Delta-Sigma (ΣΔ) modulators, on the other hand, are often utilized in designs that require an accuracy higher than 12 bits [9]-[14]. The high resolution can be achieved by optimizing the loop filter order, quantizer levels, and the oversampling ratio (OSR). ΣΔ ADCs require traditional analog building blocks, such as operational amplifiers. In

general, ΣΔ ADC consumes more energy in each conversion step and they are less process-scaling friendly than SAR ADCs.

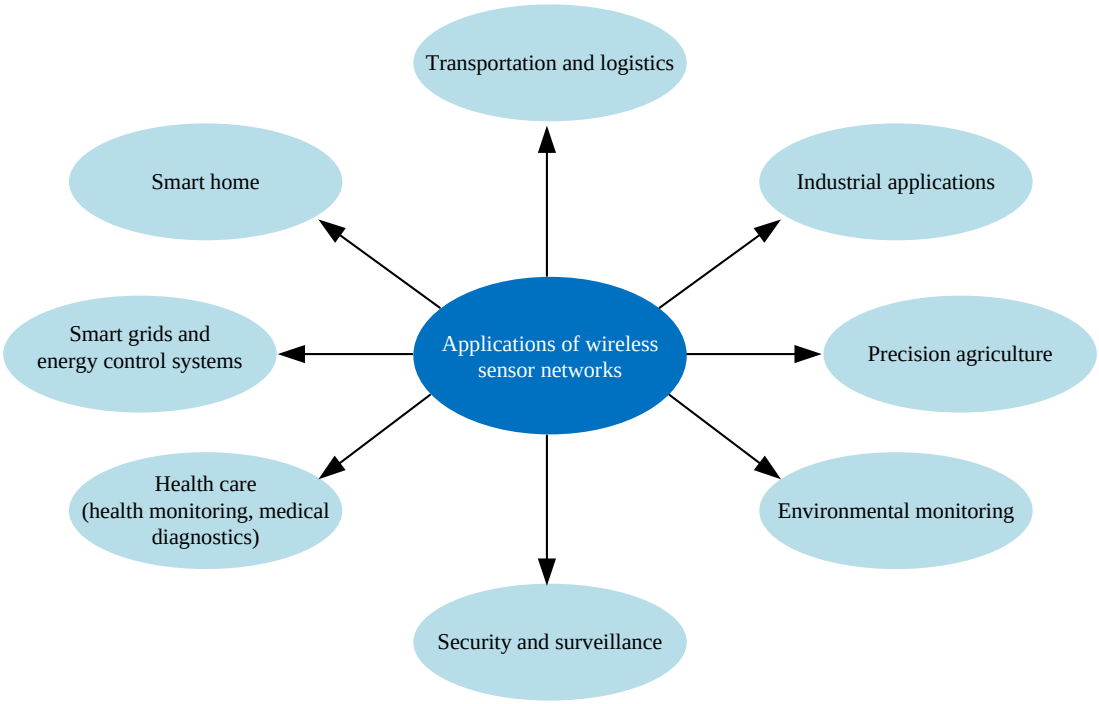

Figure 1.1 Applications of wireless sensor networks.

In this research, we have developed a novel ADC architecture to achieve both high resolution and good power efficiency. Based on previous research [15]-[17], a hybrid architecture is proposed, which embeds a noise-shaping SAR ADC into a ΣΔ modulator. The single opamp used in the loop filter not only provides a second-order noise transfer function (NTF), but also acts as an active adder for the SAR residue feedback. The proposed architecture not only achieves high accuracy but it is also power efficient.

1.2 Contributions of this Research

The major development and innovation of this research can be summarized as follows:

- A 4-bit noise shaping SAR ADC replaces the flash ADC as the quantizer for the ΣΔ modulator. Compared to traditional flash ADCs, a SAR ADC only needs one comparator instead of $2^n - 1$ comparators, where n is the number of quantizer bits. This not only reduces the power consumption, but also simplifies the design of the digital circuitry.
- The architecture takes advantage of the nature of a SAR ADC which generates a residue voltage at the end of its internal cycle. The residue voltage, which is also known as quantization noise, can be fed back to provide first-order noise shaping. The opamp in the loop filter is also used as an active adder.

1.3 Organization of this Thesis

In this thesis, Chapter 2 briefly reviews the existing noise shaping SAR ADC architecture. Chapter 3 demonstrates the design technique to enhance the NTF of a second-order modulator with a noise-shaping (NS) SAR quantizer. Circuit design details of each building block are also presented. Chapter 4 presents the simulation results in both Cadence and Matlab. Chapter 5 concludes this thesis.

Chapter 2. Literature Review

2.1 Architecture Comparison

Traditionally, SAR ADCs and ΔΣ ADCs are two candidates for sensor applications. In low speed applications, SAR ADCs achieve excellent power efficiency below 12 bits of resolution [6]-[8]. The circuit implementation for SAR ADCs is simple and the majority of the circuits are digital. Thus, SAR ADCs are more process-scaling friendly. For resolution beyond 12 bits, exploiting the oversampling and noise shaping can give rise to more effective low power implementations [9]-[14], [16]-[22]. ΔΣ ADCs are preferred for high resolution applications thanks to the oversampling and noise shaping. High resolution can be achieved by optimizing the loop filter order, quantizer levels, and the oversampling ratio (OSR). ΔΣ ADCs require traditional analog building blocks, such as opamps.

Typically, ΔΣ modulators use a number of opamp-based integrators equal to their order. In addition, an opamp-based adder might be needed in a modulator, depending on the architecture of the modulator. The power consumption of the modulator increases with the loop filter order due to the use of additional opamps. Therefore, one way to reduce the power consumption is to reduce the number of opamps.

Figure 2.1 shows the basic structure of a 2nd-order ΔΣ modulator. The architecture consists of a discrete-time filter, H(z), and a flash ADC quantizer enclosed in a feedback loop by a digital-to-analog converter (DAC). The output, V_{OUT}, is subtracted from the input signal, V_{IN}, which has been sampled at a rate much higher than the Nyquist rate. The result, after passing through the discrete-time filter, H(z), serves as an

input to the quantizer, which usually has a reduced number of levels. If the gain of the filter is high in the interval of frequency of interest (F_B) and low in the out of band, the quantization error (defined as the difference between the output of the filter and that of the quantizer) is attenuated in band due to the feedback loop. This phenomenon is called noise-shaping. The transfer function of this model in z-domain can be represented by

$$V_{OUT}(z) = V_{IN}(z) \cdot STF(z) + Q(z) \cdot NTF(z) \tag{2.1}$$

where $V_{IN}(z)$ and $Q(z)$ are the Z-transform of the input signal and quantization noise, respectively; and $STF(z)$ and $NTF(z)$ are the signal transfer function and noise transfer function, respectively. In Figure 2.1, a second-order NTF of $(1 - z^{-1})^2$ can be achieved. Thus, the in-band quantization noise is significantly suppressed and the out-of-band noise spectrum presents a 40dB/dec slope.

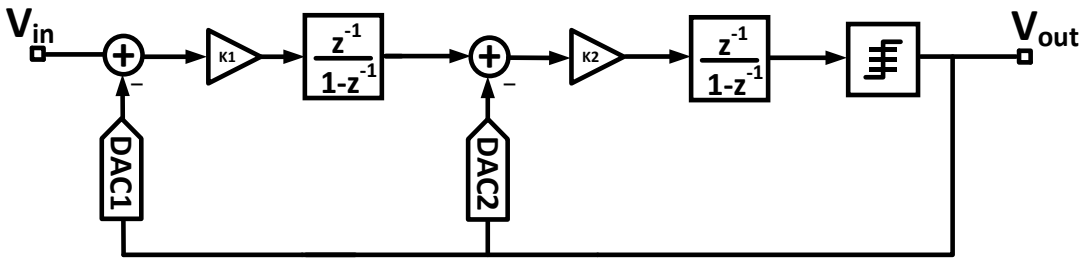

Figure 2.1 A conventional 2nd-order ΔΣ modulator with feedback structure.

SAR ADCs are often used in low power, medium resolution applications. The basic operation of the SAR ADC architecture is shown in Figure 2.2. During the first phase of operation, an input voltage is sampled onto the bottom plate of the binary weighted capacitor array. After the sampling period, each of the capacitor array bottom plates is initialized to a common-mode voltage, and the ADC performs a binary search under

the control of the SAR logic. In this architecture, the SAR algorithm performs sign-magnitude encoding of the sampled input voltage, and the capacitor DAC uses bipolar reference voltages during the binary search. Therefore, after the DAC references are initialized to the common-mode reference voltage, the comparator tests the sign of the sampled voltage, and the sign decision is fed back to the bottom plate switches of the MSB capacitor in the DAC. When the subtraction of the voltage is required, only the MSB switches move from the common-mode reference voltage to a lower reference voltage, and when addition of voltage is required, only the MSB switches move from the common-mode reference voltage to a higher reference voltage. The switches for the rest of the capacitor array are left at the common-mode reference voltage after this first decision. The rest of the bit comparison follows the same principle until the LSB comparison.

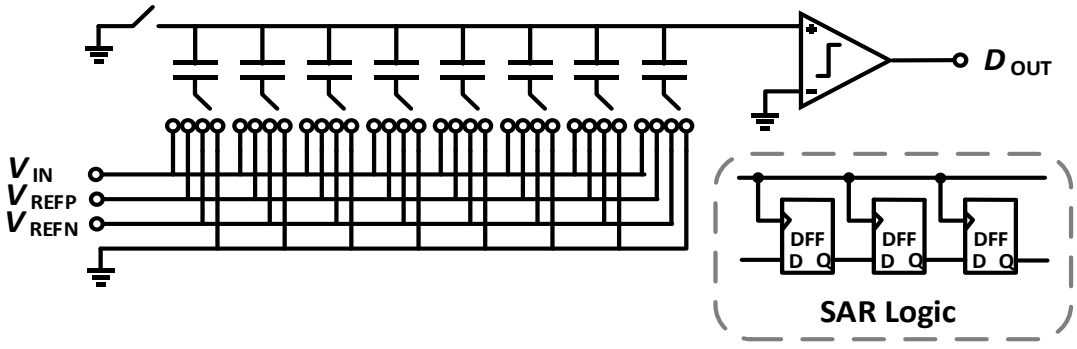

Figure 2.2 Basic operation of the SAR ADC.

A SAR ADC is a Nyquist-rate system, which means that to avoid signal aliasing, the sampling frequency is twice the bandwidth of the system. Generally, SAR ADCs suffer from mismatches in its capacitor array. Since the resolution of a SAR ADC mainly depends on the number of bits in the capacitor DAC, the capacitor size grows

exponentially as the resolution increases. Also, to reduce the *kT/C* noise, a large capacitor size is necessary. This leads to a large switching power and the need for a strong buffer to drive the capacitor array.

Recently, several papers have added new features in SAR ADCs, such as noise shaping using a residue feedback technique to improve the resolution without using a large a number of capacitors [24-27]. The existing noise shaping (NS) -SAR ADC architectures will be reviewed in the following section.

2.2 Noise Shaping SAR ADC

Oversampling and noise shaping are useful techniques to reduce the in-band quantization noise of ΔΣ modulators. Those techniques are now adopted for SAR ADCs [24]-[28]. To avoid increasing the size of the capacitor array while increasing the resolution, a low oversampling ratio can be introduced in the SAR ADC. However, without noise shaping, oversampling is usually unattractive. The question that remains is how to achieve noise shaping in SAR ADCs.

A. Residue Generation

If one follows the operation of a SAR ADC, it is seen that by the end of its internal bit cycle, a small amount of charge remains across the capacitor array and generates the residue voltage on the top plate of the capacitor arrays. This residue voltage can be treated as the quantization noise of the ADC. When the SAR ADC conversion is complete for an n-bit ADC, the magnitude of the residue voltage produced at the top plate of the DAC is shown in Equation (2.2)

$$V_{RES} = V_{IN} - \frac{V_{REF}}{2} * B_1 - \frac{V_{REF}}{4} * B_2 - \frac{V_{REF}}{8} * B_3 - \frac{V_{REF}}{16} * B_4 - \cdots - \frac{V_{REF}}{2^n} * B_n \quad (2.2)$$

In conventional SAR ADCs, the final residue information produced by the SAR DAC is discarded when a new input voltage is sampled onto the capacitor array for the next analog-to-digital conversion. The utilization of this residue voltage is demonstrated in the following section.

B. Noise Shaping SAR ADCs

With a proper feedback technique, a first-order noise shaping is possible in SAR ADCs. Noise shaping had not been efficiently demonstrated in SAR ADCs until [24]. In [24], a passive FIR filter and an opamp-based IIR filter are used to form the residue feedback path in order to achieve first-order noise shaping. Figure 2.3 shows the signal flow diagram for the noise shaping scheme that incorporates this new loop filter. The residue voltage $V_{res}(z)$ is processed by the cascade of the FIR and IIR filters to form $V_{OUT}(z)$. $V_{OUT}(z)$ is then summed with the fed-forward input and fed to the quantizer. The FIR filter is a two-tap filter with coefficients α_1 and α_2. If the IIR filter formed with the integrator has a quality factor k_A, then the overall transfer function is

$$D_{OUT}(z) = V_{IN}(z) + \frac{1-k_A z^{-1}}{1-k_A(\alpha_1-1)z^{-1}+k_A\alpha_2 z^{-2}} Q(z) \quad (2.3)$$

The signal transfer function is all-pass, but the noise is shaped and α_1, α_2, and k_A give flexibility in the form of the noise transfer function.

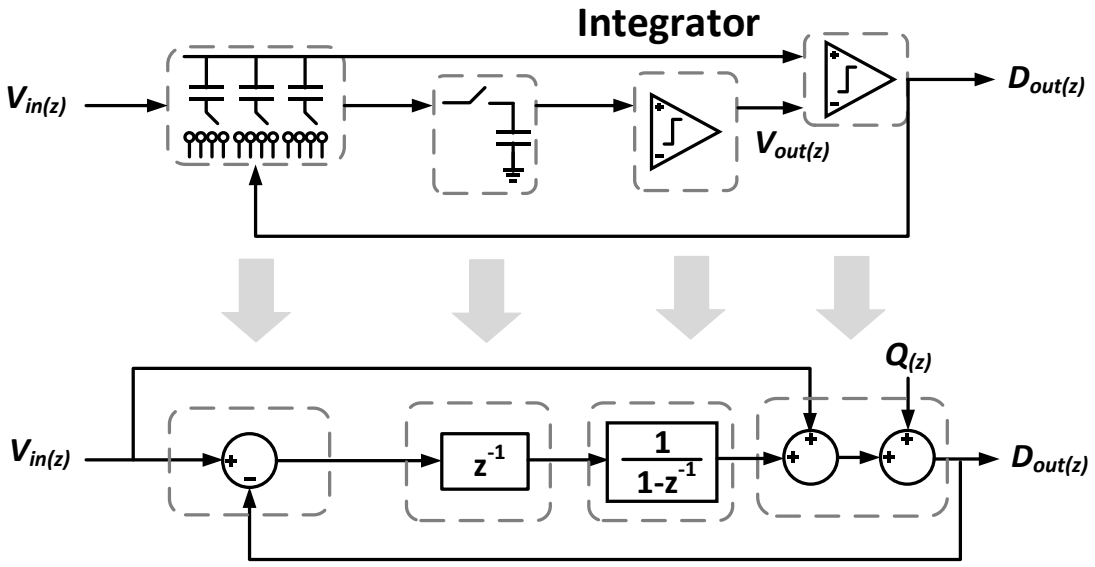

Figure 2.3 Functional representation and the equivalent signal flow diagram of the noise-shaping SAR ADC in [24].

The circuit implementation of the cascaded FIR-IIR filter is shown in Figure 2.4. The FIR filter is a two-tap filter constructed as a pair of two-capacitor arrays. Alternate DAC residue voltages are sampled onto each array at the end of a bit comparison cycle. The FIR tap coefficients α_1 and α_2 are determined by the sizes of C_A and C_B. The IIR filter is implemented with a simple, single-stage opamp along with a feedback capacitor C_F, which sums and integrates the FIR filter tap charges onto a feedback capacitor. The overall filtered residue is given as

$$V_{OUT}(z) = \left[\frac{C_A}{C_F}z^{-1} + \frac{C_B}{C_F}z^{-2}\right]\frac{k_A}{1-k_A z^{-1}}V_{RES}(z) \tag{2.4}$$

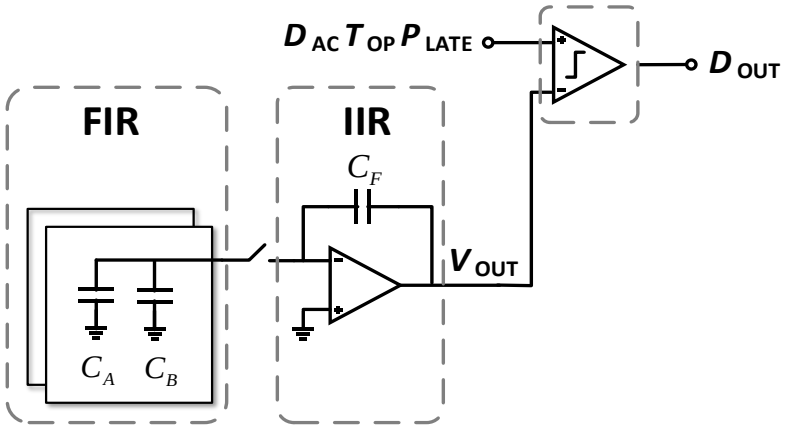

Figure 2.4 Circuit implementation of the cascaded FIR-IIR filters in [24].

Although this architecture can provide first-order noise shaping, there are several drawbacks of such a scheme. The first drawback is the thermal noise introduced by the passive sampling FIR filter. Another drawback is the residue charges that are transferred from one capacitor to another. The NTF of the noise shaping SAR ADC is $(1 - \alpha z^{-1})$, where α is determined by the ratio of the two capacitors. Thus, exact first-order noise shaping is not achieved, which leads to the out-of-band noise slope being less than 20dB/dec.

C. Second-Order Fully Passive Noise Shaping SAR ADC

The architecture in [24] can only achieve first-order noise shaping, limiting its maximum SNDR to 69 dB. Moreover, it needs to use an opamp based IIR filter, which degrades the power efficiency. To address these issues, opamp-free noise shaping (NS) SAR ADCs have been proposed [25]. In [25], an opamp-free second-order NS-SAR ADC uses two passive integrators to integrate the residue of a 9-bit SAR twice and feed

the first and second integrated results to a 3-path comparator for dynamic summation and quantization.

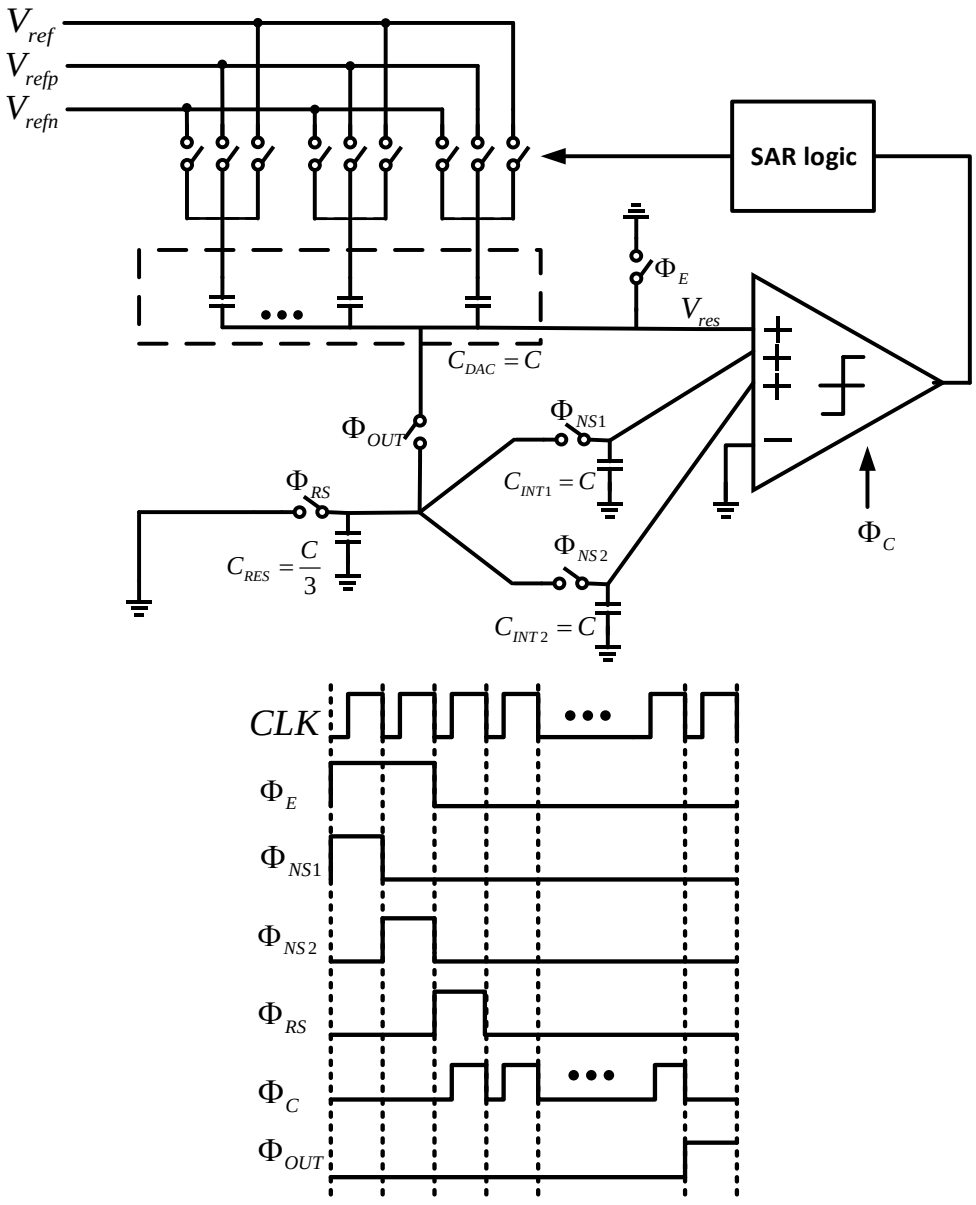

Figure 2.5 Architecture and timing control of the fully passive noise-shaping SAR presented in [25].

Fig. 2.5 shows the passive second-order noise shaping SAR ADC presented in [23]. The external clock *CLK* is divided into 20 phases. During the first 2 phases Φ_E, the input signal V_{in} is sampled onto the SAR capacitor array C_{DAC} = C. After sampling, the capacitor starts to work from phase #3 to phase #19 (Φ_C). The comparator is employed 4 times for each bit in the last 2 bits to reduce the comparator noise. After all bit comparisons, in Φ_{OUT}, a capacitor C_{RES}= C/3, is merged with C_{DAC} to get a fractional residue voltage, 0.75 V_{res}. When a new sampling starts, C_{RES} dumps its charge onto the capacitor C_{INT1}= C during phase Φ_{NS1}. The voltage on C_{RES} and C_{INT1} becomes V_{int1} = $0.1875V_{res}/(1-0.75z^{-1})$. During Φ_{NS2}, C_{RES} further dumps its charge onto another capacitor C_{INT2} = C. Similarly, the voltage on C_{RES} and C_{INT2} becomes V_{int2} = $0.25V_{INT1}/(1-0.75z^{-1})$. Hence, second-order passive integration is realized with two poles at 0.75. The gain is compensated in the comparator by sizing the input transistor properly to achieve the overall NTF of $(1-0.75z^{-1})^2$. During phase Φ_{RS}, the charge on C_{RES} is cleared to be ready for a new V_{res} in the next clock cycle. Both V_{int1} and V_{int2} are fed back to the comparator input, resulting in a 3-path input comparator as shown in Fig. 2.5.

Chapter 3. A Single-Opamp Third-Order Delta-Sigma Modulator with NS-SAR Quantizer

In Chapter 2, the state of the art NS SARs were discussed. Among all the fabricated chips [24-28], the best SNDR that was achieved by an NS-SAR is 80 dB. However, modern medical applications often require higher ADC resolution (sometimes above 14 bits). The highest NTF order found in prior work is second-order. To increase the NTF further, the low frequency quantization noise leakage increases due to the passive FIR filter. Another possible solution to improve the resolution is to increase the OSR. However, this will increase the overall power consumption dramatically and the speed requirement of the SAR internal bit cycling becomes challenging as well. Thus, other ADC architectures have been developed to achieve a higher resolution. In [28], an opamp is introduced into the system to increase the system NTF to third-order. A fully passive noise shaping (FPNS) SAR ADC is used as the quantizer in the ΔΣ modulator. Although the system is claimed to have a third-order NTF, the FPNS SAR still introduces quantization noise leakage. This causes the effective NTF to be less than third-order, and the overall SNDR is limited to only 75 dB.

In this work, we propose a novel technique to feedback the SAR residue voltage. A single opamp is used to form a second-order loop filter in the multiplexing operation. A 4-bit SAR ADC is used as the quantizer in the modulator. The loop filter opamp is then reused as an active adder to add the delayed feedback path from the SAR quantizer to form one extra-order of noise shaping. In this manner, the system is able to achieve a third-order NTF of $(1 - z^{-1})^3$. The simulation results show that the proposed

architecture can reduce the low frequency quantization noise level and therefore improve the SNDR.

3.1 NTF Enhancement Technique

The scheme in Figure 3.1 shows a system with a second-order ΔΣ loop filter and the noise-shaping SAR quantizer. As discussed earlier, an adder block is required to subtract the residue feedback signal from the output signal of the loop filter. This means that an additional opamp needs to be used to implement the adder. In order to further reduce the power consumption of the system, the adder before the NS-SAR quantizer should be eliminated.

Figure 3.2 is a behavioral model that enhances the NTF by one order without using an adder in front of the quantizer. Here only the second integrator and the NS SAR quantizer are shown. Instead of feeding the residue signal to the adder, which is after the integrator, it is fed to the input of the second integrator and the adder after the integrator is eliminated. In this case, the quantization noise from the SAR ADC is fed back to the input of the integrator through an NTF enhancement term, H(z). The overall relationship between V_b and V_{out} is shown in Equation (3.1). The derived NTF of this model is shown in Equation (3.2). The ideal NTF for a second order system is expressed as (3.3). Thus, by mapping (2) and (3), the NTF enhancement term H(z) can be found as $(1 - z^{-1})$. This means that the residue signal needs to be fed back through two paths with certain delay and polarity changes to give an extra order of noise shaping.

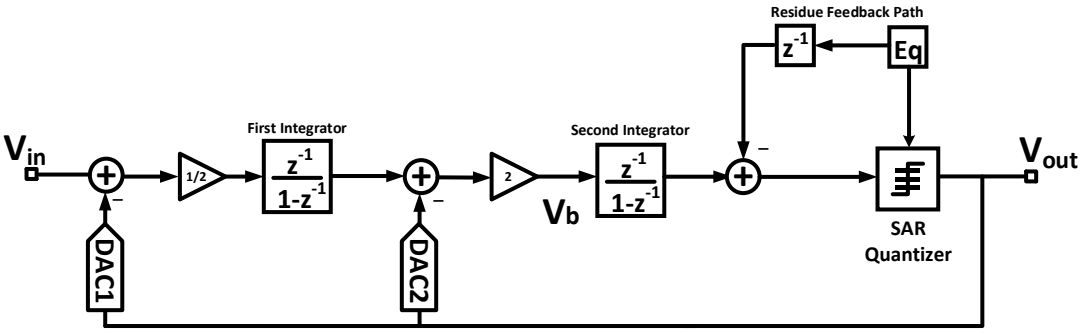

Figure 3.1: Third-order ΣΔ modulator with noise-shaping (NS) SAR quantizer

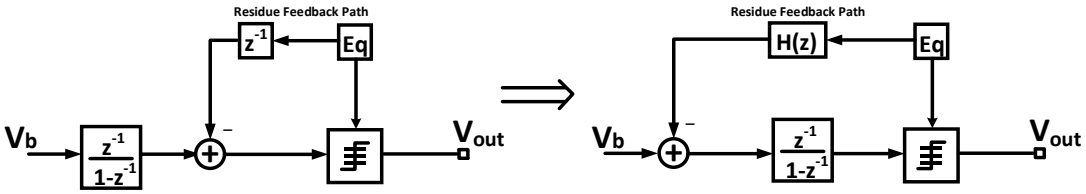

Figure 3.2: Behavioral model to enhance the NTF without an adder block.

The remodeled system is shown in Figure 3.3. A gain of ½ is added in the residue feedback path to cancel the gain in the second integrator to make a unity gain for the third-order term. The overall input and output relationship of the system is shown in Equation (3.4). Finally, the NTF is derived and shown in (3.5), which is an exact third order NTF from a ΔΣ modulator.

An input direct feedforward path is added to the output of the first integrator. In this way, the first opamp only processes the quantization noise, which has a much smaller

amplitude than the input signal. Thus, the first opamp output swing requirement is relaxed.

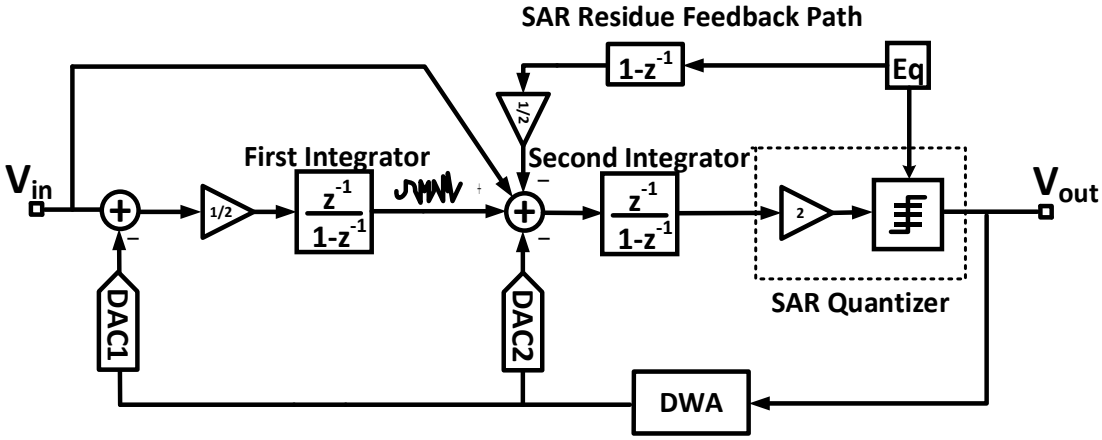

Figure 3.3: The adder before the NS-SAR quantizer is removed and the input is fed forward to relax the opamp swing requirement.

$$V_{out} = \left[V_b - V_{out} - E_q H(z)\right]\frac{z^{-1}}{1-z^{-1}} + E_q \tag{3.1}$$

$$NTF = \left[1 - H(z)\frac{z^{-1}}{1-z^{-1}}\right](1-z^{-1}) \tag{3.2}$$

$$NTF_2 = (1-z^{-1})^2 \tag{3.3}$$

$$V_{out} = \left[(V_{in} - V_{out})\frac{1}{2}H(z) + V_{in} - V_{out} + \frac{1}{2}(1-z^{-1})E_q\right]2H(z) + E_q \tag{3.4}$$

$$NTF_3 = (1-z^{-1})^3 \tag{3.5}$$

As mentioned earlier, a fully passive noise shaping SAR ADC was used in a single opamp based third-order ΣΔ modulator in [28]. To demonstrate the difference of the effective NTF between the proposed scheme and the one in [28], macro models were

built in Matlab and Simulink with the same loop filter order, quantization level, OSR, and input signal amplitude. Figure 3.4 shows the power spectral density of two simulation results. The SQNR from this work can be improved up to 10 dB compared to the one from [28] thanks to the improved third-order NTF.

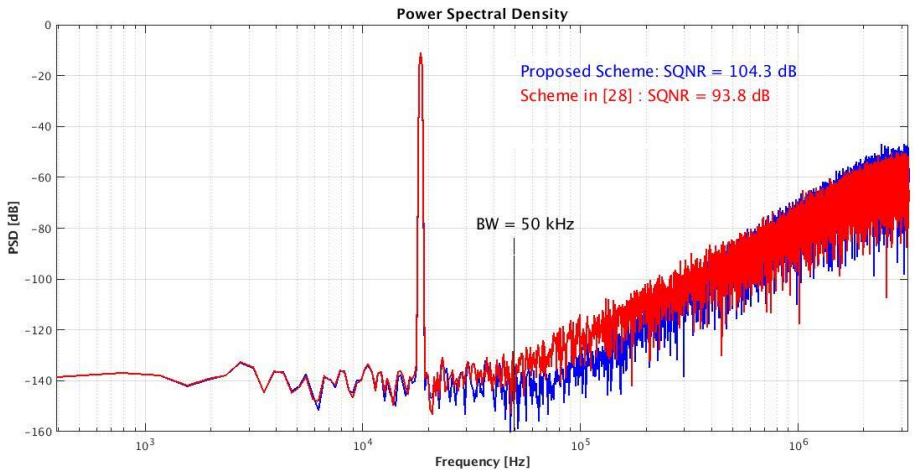

Figure 3.4: Simulated PSD with -4.4 dBFS input signal and Fs = 3.2 MHz, BW = 50 kHz.

3.2 Circuit Implementation of the Third-Order ΔΣ Modulator

The switched-capacitor (SC) implementation of the modulator is discussed in this section. Then the design details of the input sampling switch, operational amplifier, dynamic comparator, SAR logic circuit, and DAC element mismatch shaping technique are explained.

The multiplexing operation interleaves the output of the single opamp, the first stage, and the second stage [15]. Figure 3.5 shows the SC implementation of the proposed third-order ΔΣ modulator. The single opamp serves the first integrator during one phase. During the complementary phase, the opamp and the additional connected network operate as the second integrator. During Φ1, the input signal is sampled onto Cs1. During Φ2, the DAC1 signal is subtracted from the sampling capacitor, and the charges are transferred onto the feedback capacitor, Cf1. In the meantime, the output of the opamp is connected to the sampling capacitor, Cs2, in the second stage. When Φ1 starts again in the next clock cycle, the DAC2 signal is subtracted in Cs2 and the charge is transferred to the feedback capacitor, Cf2, in the second stage. By the end of Φ1, the second-order loop filter output signal is ready and is sampled onto the capacitor array in the SAR quantizer. Notice that the input direct feedforward path shares the timing with the second integrator. The kT/C noise requirement determines the size of the capacitors in the first integrator. In this design, to achieve an SNDR over 84 dB, Cs1 is chosen as 1 pF and Cf1 is 2 pF. The capacitor size in the second integrator can be relatively small due to the fact that any noise source and nonlinearity in the second

integrator will be reduced by the first integrator. In this design, Cf2 is chosen to be 150 fF.

Φ_1 is the operation period for the SAR quantizer. The output signal from the loop filter will be ready by the end of Φ_1. At the same time, the loop filter output signal is also sampled onto the SAR quantizer capacitor array in Φ_{SAR}. In this design, Φ_{SAR} is turned off before Φ_1 to give the comparator and SAR logic circuit enough time to make decisions on the internal bit cycling. During Φ_1, the signal is sampled on the top plate of the capacitor array. The bottom plate of the capacitor array is connected to ground. When Φ_1 is off, the bottom plate will be switched to V_{ref} if the digital bit is 1 and remains at ground if the digital bit is 0. Thus, after the LSB operation, the voltage on the top plate of the capacitor array will be,

$$V_{residue} = V_{in} - \frac{V_{ref}}{2} * B_1 - \frac{V_{ref}}{4} * B_2 - \frac{V_{ref}}{8} * B_3 - \frac{V_{ref}}{16} * B_4 \qquad (3.6)$$

where V_{in} is the input signal of the SAR quantizer and $V_{residue}$ is the quantization noise in the current stage. Then $V_{residue}$ is fed back to the input of the second integrator using two paths, one with a one clock cycle delay and the other with a two clock cycle delays. Because the integrator itself has a one clock cycle delay, the third-order residue feedback path is shown as $(1 - z^{-1})$ instead of $(z^{-1} - z^{-2})$.

The residue feedback path $(1 - z^{-1})$ is implemented using capacitors to hold the charge and transfer the charge back to the feedback capacitor C_{f2} with a certain number of clock delays. This requires two capacitors and three capacitors to realize the delay, respectively. The detailed clock information of Φ_{1a} , Φ_{1b}, Φ_{2a}, Φ_{2b}, Φ_{2c} is shown in Figure 3.7.

The Φ_{SAR} pulse width is chosen to be 87.5% of the pulse width of Φ_1. The op-amp in the second integrator needs to have a slightly higher unity gain bandwidth to settle faster. The op-amp design details will be shown later. The SAR ADC internal bit cycle takes only 12.5% of Φ_1. This period of time is enough for the operation of the digital logic circuitry and the comparator.

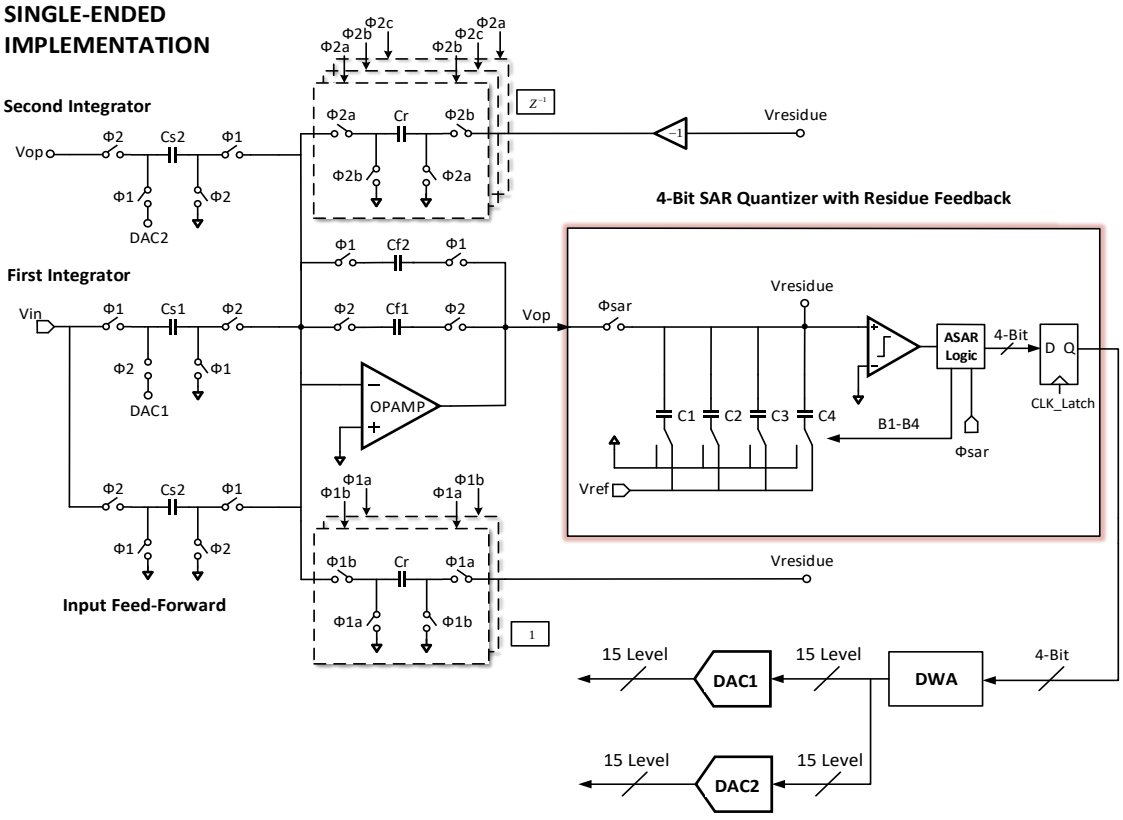

Figure 3.5 Schematic diagram of the proposed third-order ΔΣ modulator.

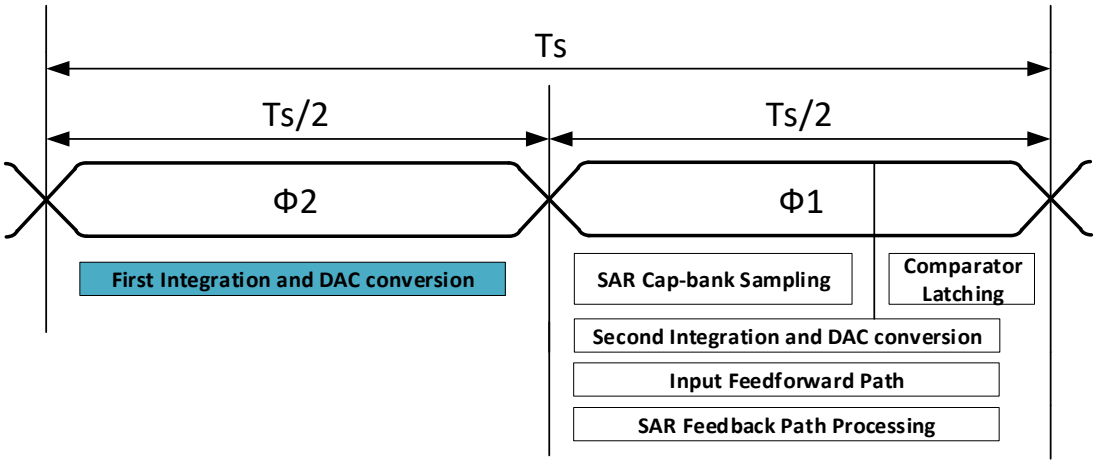

Figure 3.6. System timing control for the time-interleaved modulator and NS-SAR quantizer.

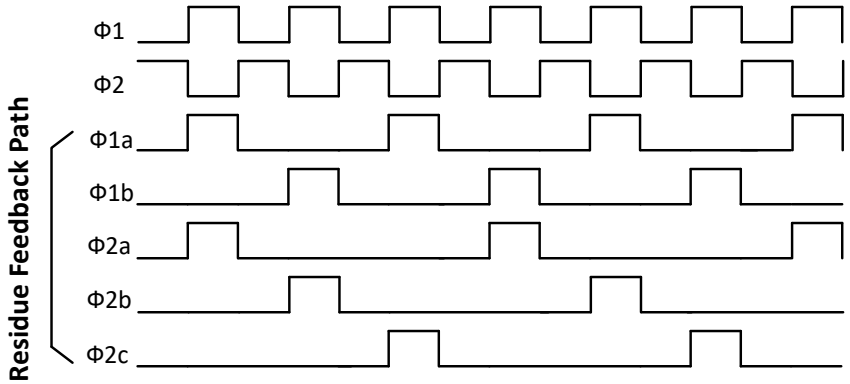

Figure 3.7. Clock phases of the integrators and feedback paths.

3.2.1 Bootstrap Switch

The input sampling switch is critical to the ADC linearity. Since the input signal is constantly changing during the sampling phase, the V_{GS} of the switch transistor also changes with the input signal amplitude. This leads to a variable on-resistance, R_{ON}, which causes the nonlinearity of the ADC. To reduce the nonlinearity, the bootstrapped switch shown in Figure 3.8 is used to perform the S/H function. With the bootstrapped

switch, the gate-source voltage of the sampling transistor is fixed at the supply voltage (V_{DD}), which makes R_{ON} a small constant value and thus improves the switch linearity. The operation of the bootstrapped switch is described as follows. During Φ_2, S1, S2 are off and S5 is on, turning the bootstrapped switch off. Meanwhile, S3 and S4 are on, and the voltage across C_{boot} is V_{DD}. During Φ_1, MN3, MP4 and MN5 are off, MN1 and MP2 are on. The voltage at node G is $V_{DD} + V_{in}$ while the voltage at node S is V_{in}. Thus, the V_{GS} of MNSW during the sampling phase is a constant at V_{DD}. As the input signal increases to V_{DD}, the voltage at node G can be as high as $2V_{DD}$, which is also the drain-source voltage of S5. This high voltage can cause reliability problems for S5, such as dielectric breakdown, hot electron effect, and reverse breakdown. To reduce the drain-source voltage of S5, an additional transistor MNT5 is used to distribute the

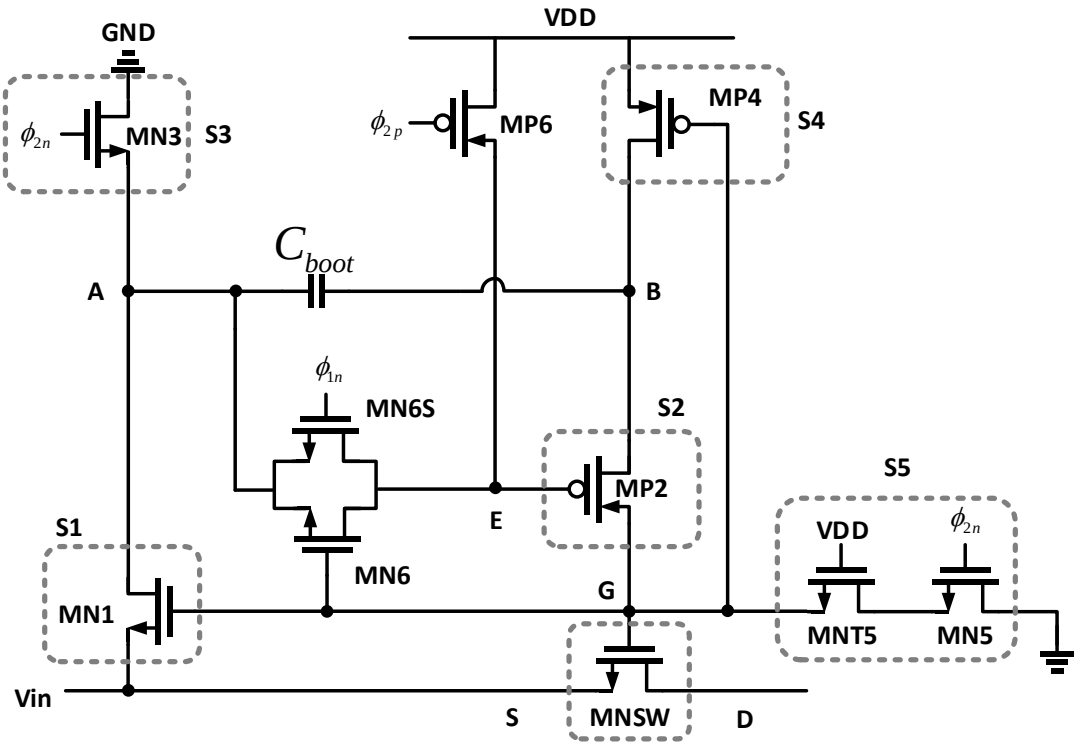

Figure 3.8 Bootstrapped switch.

boosted voltage. Transistor MN6, MN6S, and MP6 are used to trigger the switch S2. At the beginning of Φ_1, MN6S triggers S2 on. As the input voltage rises to V_{DD}, MN6S is no longer on but MN6 keeps S2 on. This operation keeps S2 on during the entire sampling phase. After the sampling phase, MP6 is on, pulling the voltage at node E to V_{DD} and S2 will be turned off. In this design, C_{boot} is chosen to be 100 fF.

3.2.2 Operational Amplifier

The single op-amp is configured for three different operations, integration during both Φ_1 and Φ_2 as well as driving the NS-SAR capacitor-array. Hence, it experiences a varying output loading condition. A two-stage architecture was selected because the dominant pole is determined by the Miller compensation capacitor, instead of the output loading capacitor as in the single-stage topology. In this design, the telescopic cascode structure is used in the first stage to achieve high gain and a common-source amplifier is adopted in the second stage to maximize the output swing to as high as possible. The op-amp employs the cascode Miller compensation technique [17] for excellent phase margin. This technique blocks the feedforward path and therefore eliminates the left-hand plane zero. The fully differential opamp is shown in Figure 3.9.

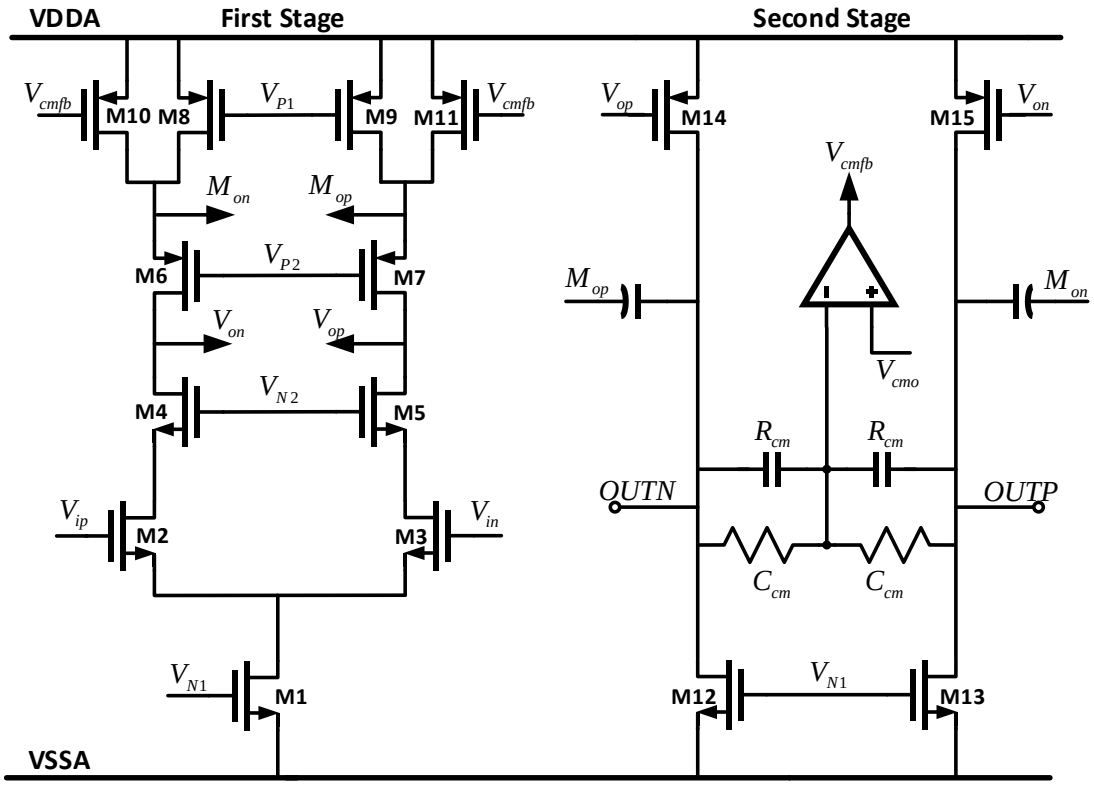

Figure 3.9 Two-stage operational amplifier.

The op-amp is tested in the simulation with a DC gain of 60 dB and a gain-bandwidth product of 25 MHz. With a supply voltage of 1.2 V, the op-amp consumes 39 μW of power.

3.2.3 Comparator Design and Asynchronous Logic and Timing

Figure 3.10 shows a schematic of the comparator in the NS-SAR quantizer. To reduce power consumption, a dynamic comparator is chosen in this design because it does not consume static current [18]. When *CLKc* is high, the comparator outputs OUT_P and OUT_N are reset to high. When *CLKc* goes to low, the differential pair, M_1 and M_2

compares the two input voltages. The latch regeneration forces one output to high and the other to low according to the comparison results. Consequently, the *Valid* signal is pulled to high to enable the asynchronous control clock.

In general, the offset voltage of the comparator can degrade the ADC performance dramatically. The offset voltage of this comparator can be expressed as

$$V_{OS} = \Delta V_{TH1,2} + \frac{(V_{GS}-V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta \mathrm{R}}{\mathrm{R}}\right) \tag{3.7}$$

where $\Delta V_{TH1,2}$ is the threshold voltage offset of the differential pair M_1 and M_2, $(V_{GS} - V_{TH})_{1,2}$ is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2, and ΔR is the loading resistance mismatch induced by M_3 - M_6. The first term is a static offset which does not affect the performance of a SAR quantizer. The second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the SAR quantizer input common-mode voltage. The dynamic offset degraded the performance of the prototype in [15].

There are several possible approaches to improve the dynamic offset. The comparator size can be increased, which increases the power consumption. In this work, a simple and reliable way is to cascode a biased MOS (M_8) at the top of the switch MOS (M_7). Because M_8 is in the saturation region, the change of its drain-source voltage has only a slight influence on the drain current. Thus, M_8 keeps the effective voltage of the input pair near a constant value when the common-mode voltage changes. Also, since the NS-SAR quantizer is placed inside a ΔΣ modulator, any non-idealities will be further reduced by the loop filter. Thus, the dynamic offset from the comparator has a minor influence on the overall system linearity.

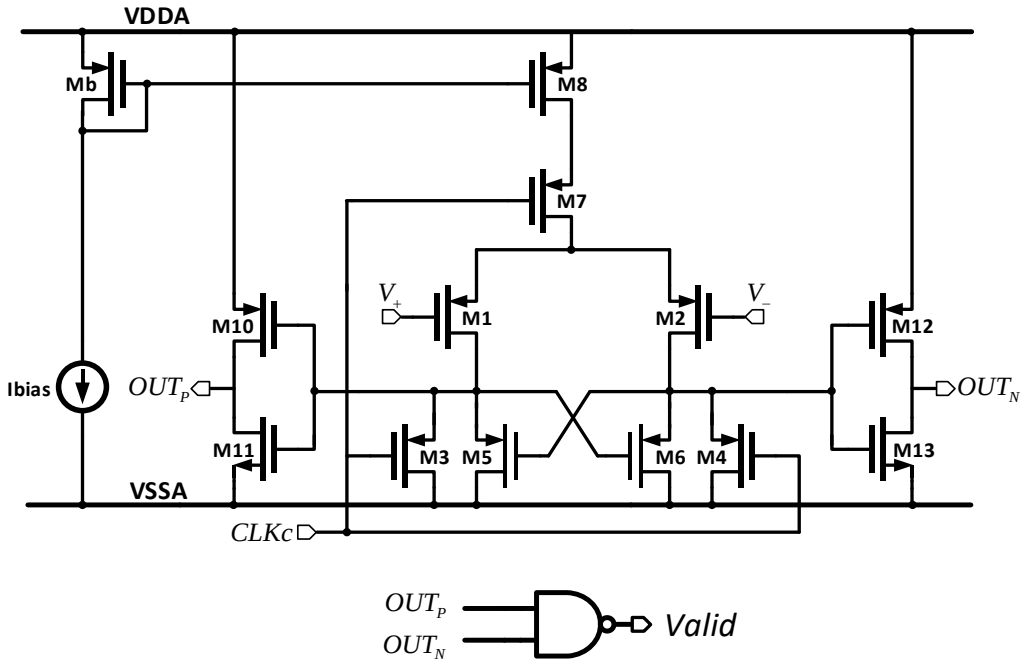

Figure 3.10 Schematic diagram of the dynamic comparator with a current source.

3.2.4 SAR Control Logic

To avoid using an additional clock generator, the proposed NS-SAR ADC uses an asynchronous control circuit to generate the necessary clock signal internally. Figure 3.11 shows the schematic and timing diagram of the asynchronous control logic [18]. The sampling phase for the NS-SAR ADC is about 43.75% of the clock period. The dynamic comparator generates the *Valid* signal. CLK_{sar} is the control signal of the sampling switches in the NS SAR quantizer. The sampling phase is about 87.5% of the clock period, as mentioned before. CLK_c is the control signal of the dynamic comparator. CLK_1 to CLK_4 sample the digital output codes of the comparator and control the signals for the capacitor arrays to perform the monotonic switching procedure.

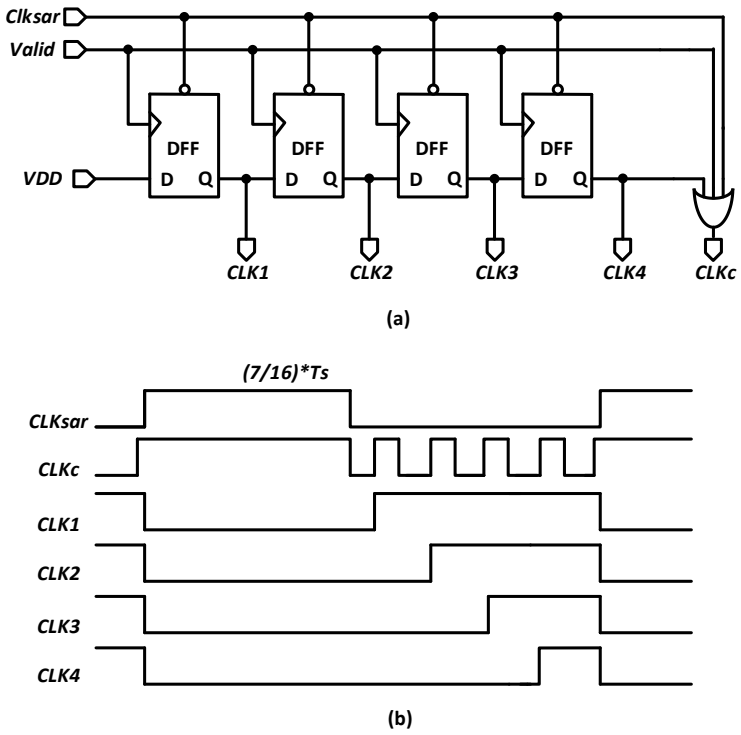

Figure 3.11 Asynchronous control logic: (a) Schematic. (b) Timing diagram.

Figure 3.12 shows the schematic and timing diagram of the NS-SAR DAC control logic. At the rising edge of CLK_i, a flip-flop samples the comparator output. If the output is high, the relevant capacitor is switched from V_{ref} to ground. If the output is low, the relevant capacitor is kept connected to V_{ref} . At the falling edge of CLK_i, all capacitors are reconnected to V_{ref}. An inverter is used as a switch buffer. The sizes of the switch buffer are scaled down based on the driven capacitances in the SAR capacitor array. Transmission gate switches are used as the sampling switch in the NS-SAR quantizer to ensure the sampling of a rail-to-rail signal from the loop filter output.

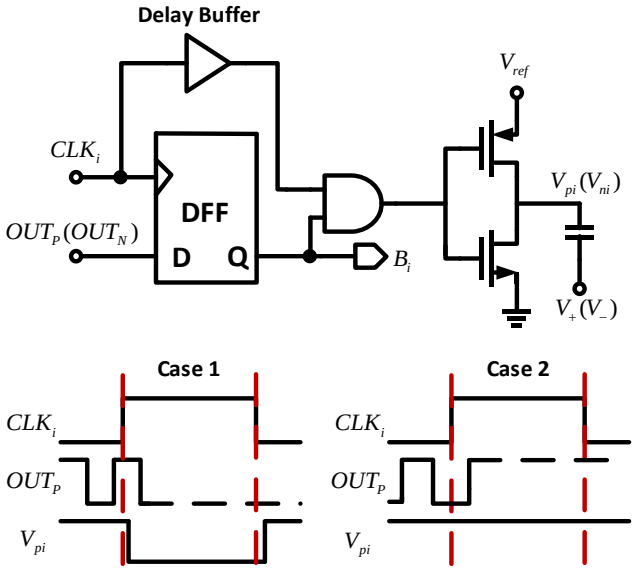

Figure 3.12 NS-SAR DAC control logic.

3.2.5 Data Weighted Averaging

Data weighted averaging is used in the feedback DAC to improve the linearity of the DAC at the modulator input. Figure 3.13 shows the overall circuit realization for DWA using a pointer and a logarithmic shifter. The 4-bit binary code from the NS-SAR quantizer is converted to a thermometer code and then goes into a 4-stage shifter. Meanwhile, the binary code goes into the pointer as well. The output of the pointer controls the level shift of the logarithmic shifter. Notice that the DWA only includes the shifter in the feedback path while the pointer calculation is outside the modulator loop. This minimizes the delay in the feedback loop from the DWA.

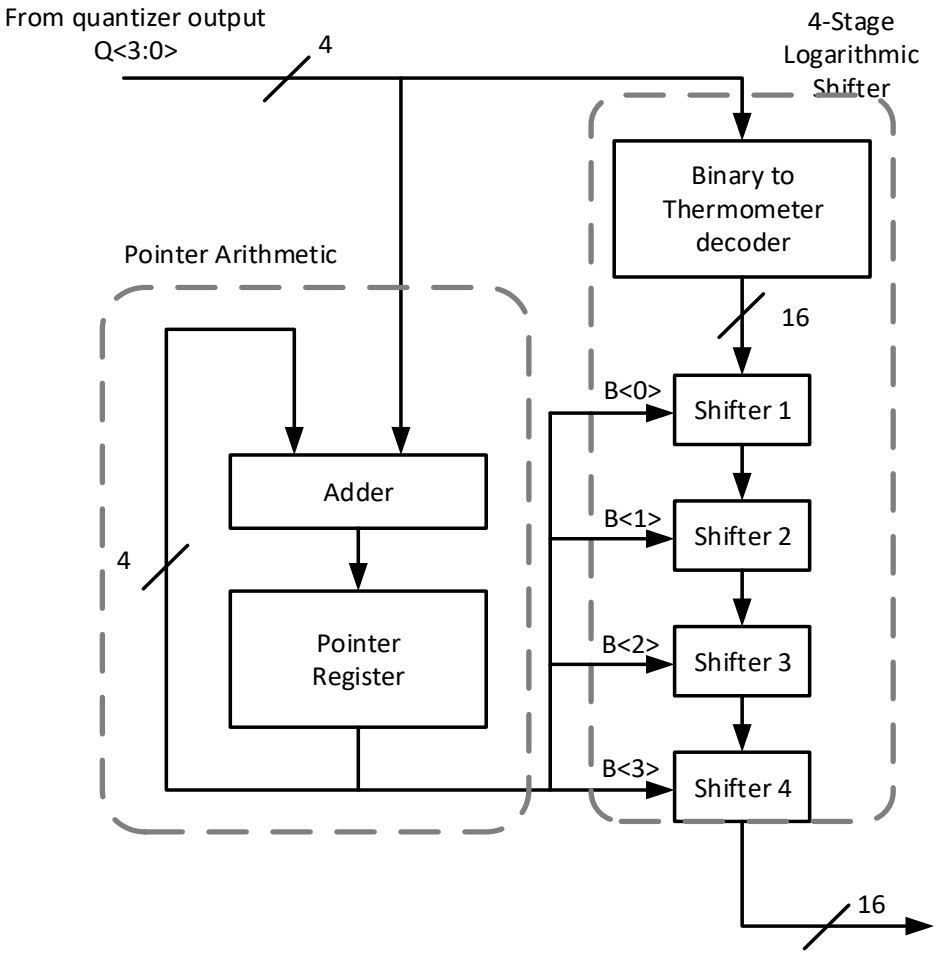

Figure 3.13 Overall circuit realization for DWA using a logarithmic shifter.

Figure 3.14 is the realization of a 4-bit logarithmic shifter. The solid arrow represents an input code of 1 and the dashed arrow represents an input code of 0. Based on the control signal from the pointer, the logarithmic shifter rotates the DAC unit element in every clock cycle. With relatively high oversampling ratio (OSR), the mismatch among DAC unit elements can be first-order shaped by DWA. Thus, the linearity of the DAC is improved.

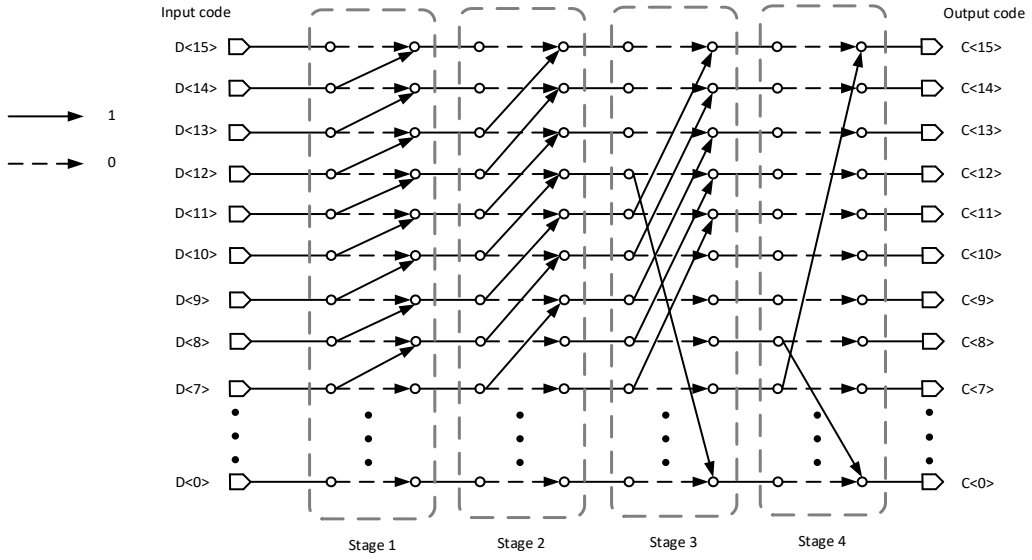

Figure 3.14 4-bit logarithmic shifter.

Chapter 4. Simulation Results

The proposed ADC is designed in a 65 nm CMOS process. The clock speed is 3.2 MHz and the ADC core consumes 50.7 µW. The supply voltage for the analog and digital blocks is 1.2 V and 1 V, respectively. Figure 4.1 shows the simulated 16384-points FFT output spectrum. The ADC achieves a peak SNDR of 84.5 dB and 50 kHz bandwidth with a 9.1 kHz, -4.4 dBFS input sinusoid signal. The simulated dynamic range of the prototype ADC is 86 dB, as shown in Figure 4.2. The overall power consumption of the ADC is presented in Figure 4.3. The opamp is the dominant power consuming block, dissipating about 72% of the overall power consumption. The comparator, SAR logic circuitry, and the ΣΔ DAC and DWA dissipate 1.4 µW, 1.6 µW, and 4.2 µW, respectively. The biasing circuit and the clock generator together dissipate around 4.5 µW.

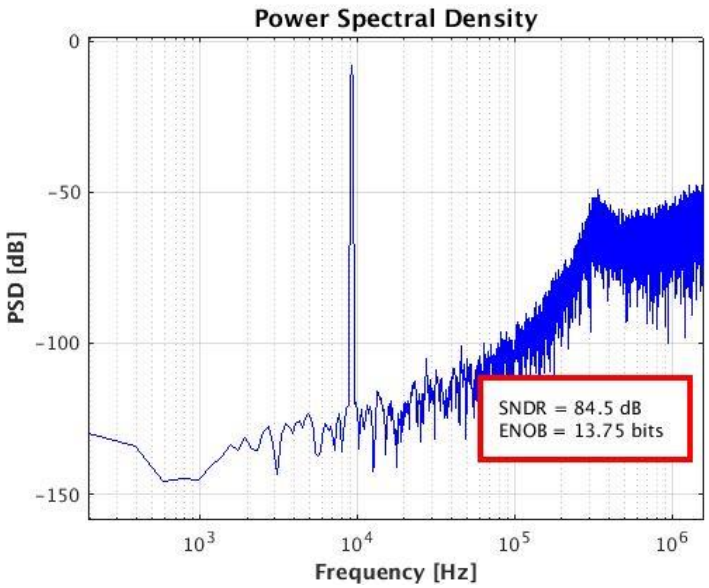

Figure 4.1 Simulated power spectrum density with an input signal at 9.1kHz.

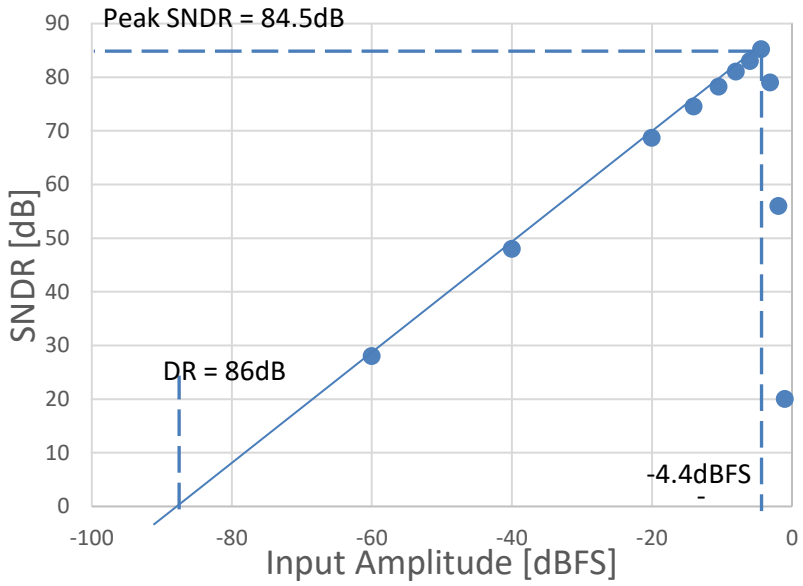

Figure 4.2 Simulated SNDR versus input signal amplitude.

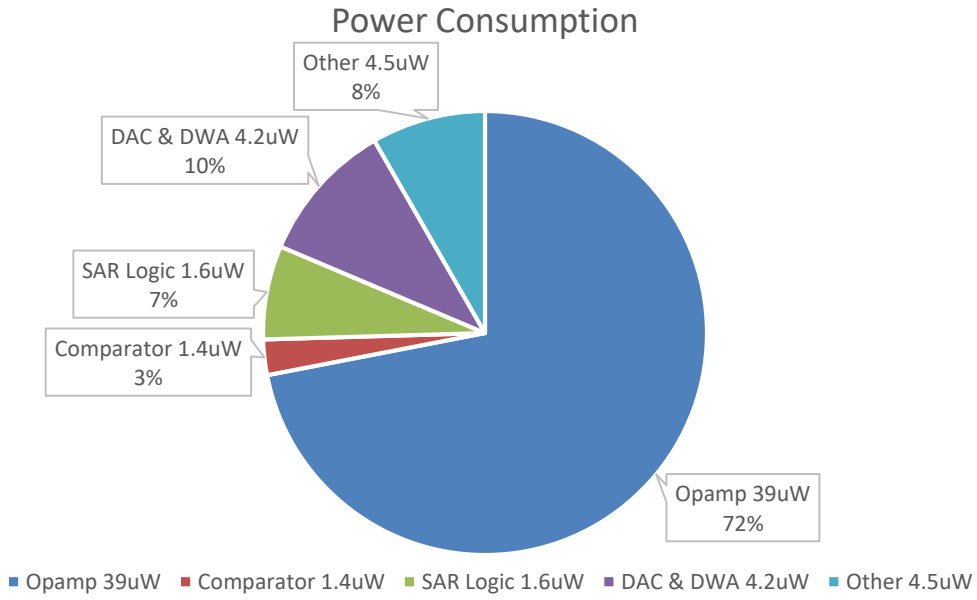

Figure 4.3 Overall power consumption.

The performance comparison with recent state of the art work is shown in Table I. The achieved figure-of-merit (FoM), defined by FoM = $Pw/(2Bw*2^{ENOB})$, is 36.9 fJ/conv-step. This proposed architecture achieves very competitive FoM, which further demonstrates the power efficiency of the NS-SAR inside a ΣΔ modulator.

TABLE. I

Performance Summary

	This work*	[16]	[20]	[21]	[22]	[23]	[26]	[28]
ARCHITECTURE	Single opamp DSM +NS-SAR	Single opamp DSM	SC DSM	Gm-C CT DSM	SAR	IADC	NS-SAR	SAR+DSM
Process	65nm	180nm	180nm	65nm	28nm	180nm	40NM	65nm
Supply	1.2V/1V	1.5V	1.8V	1.1V	1.55V/0.75V	1.5V	1.1	0.7V/0.85V
Sampling Frequency	3.2MHz	3.2MHz	6.144MHz	3.072MHz	100KHz	624KHz	8.4MHz	3.2MHz
Signal Bandwidth	50kHz	50kHz	24kHz	24kHz	2kHz	1kHz	262kHz	100kHz
SNDR	84.5dB	88.9dB	98.5dB	85dB	98dB	96.8dB	80dB	75dB
Power Consumption	50.7µW	140µW	280µW	37.1µW	37.1µW	35µW	143 µW	45.7µW
Dynamic Range	-	84dB	103.6dB	88dB	-	99.7dB	-	-
FoM_1(fJ/conv.-step)	36.9	61	84.8	173	143	305	33.9	50
FoM_2(dB)	174.4	-	177dB	168dB	175.3dB	171.4dB	173	168.3

*Based on simulation results.

Chapter 5. Conclusion

A single op-amp third-order ΣΔ modulator is proposed in this work. The prototype ADC is designed using 65nm 2P9M CMOS technology. The ΣΔ modulator utilizes a NS-SAR ADC as its quantizer to reduce the power consumption from the digital circuitry. The digital circuitry only consumes 8.3μW in this design, which proves the power efficiency of the NS-SAR quantizer. One extra order of noise shaping is also achieved through the NS-SAR quantizer. Overall, the prototype modulator attains 84.5dB SNDR over 50kHz signal bandwidth. Due to the extra-order of noise shaping from the NS-SAR quantizer, the total power consumption is only 50.7μW, which yields a FoM of 36.9fJ/conversion-step. This demonstrates the power efficiency of the proposed modulator for wireless sensor network and portable device applications.

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