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A new family of logic gates based on differential current-mode topologies has been developed for mixed-mode applications. By steering currents to the appropriate signal nodes, a constant current is maintained in the power supplies during the logic transitions of the gates hence eliminating the large overlap current that is inherent to conventional static gates. Simulations have shown that the current spike generated by these new gates is at least two orders of magnitude smaller than for the static gates. These gates also have higher noise immunity since the input stage is a differential pair. Experimental result indicated that the minimum propagation delay of the inverter gates is 770 ps using a standard digital 2 μm p-well CMOS technology.

CMOS DIFFERENTIAL LOGIC TECHNIQUES FOR MIXED-MODE APPLICATIONS.

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San-Hwa Chee

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Head of Department of Electrical and Computer Engineering

Redacted for privacy

Dean of Graduate School

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C	Capacitance in Farad
Kn	Transconductance of NMOS, A/V^2
Kp	Transconductance of PMOS, A/V^2
L	Length of MOSFET, micron
V	Voltage, volts
Vds_{xx}	Drain-to-source voltage of MOSFET XX, volt
$Vdsat_{xx}$	Saturation voltage of MOSFET XX, volt
Vgs_{xx}	Gate-to-source voltage of MOSFET XX, volt
V_L	Logic low voltage, volt
V_H	Logic high voltage, volt
Vsb	Source-to-bulk voltage of MOSFET, volt
Vsw	Voltage swing of logic gate, volt
Vtn	Threshold voltage of NMOS, volt
Vtp	Threshold voltage of PMOS, volt
W	Width of MOSFET, micron
$\left(\dfrac{W}{L}\right)_{xx}$	Aspect ratio of MOSFET XX
γ	Bulk threshold parameter, $volt^{1/2}$
λ	Channel length modulation, 1/volt
$\varnothing_F$	Surface potential, volt

CMOS DIFFERENTIAL LOGIC TECHNIQUES FOR MIXED-MODE APPLICATIONS.

1. INTRODUCTION

The demand for greater levels of system integration has created the need for analog and digital circuits on the same chip, i.e, mixed-mode systems. The advantages gained in mixed-mode VLSI systems are decreased production costs, higher performance, and ease of implementation [1]. However, current spikes that are generated by the conventional CMOS static digital gates during transition degrade the performance of the analog circuitry.

Wallmark and Shoji [2-3] have summarized the noise phenomena in digital VLSI circuits. and classified the generation of noise into two distinct mechanisms. The first is induced noise that is caused by noise voltage transmitted from one node to another. The other is the power bus noise due to the current spikes flowing through the resistance and inductance of the chip's power bus, bonding wire, and package interconnects. This noise affects all the circuits on the chip. Analog circuits with sampling, e.g., switched-capacitors, are especially susceptible to this noise which may be folded back into the baseband through aliasing reducing the dynamic range. Dynamic range is fundamentally limited by the amount of noise in the output signal over a certain bandwidth. It has also been shown that digital switching noise reduces the number of effective bits of an A/D converter [4]. Besides creating problems for analog circuitry, the current spikes can also cause glitches in digital circuitry [5]. Other effects of switching noise have also been studied [6].

Several techniques have been proposed to reduce digital noise [7-8]. Good layout techniques such as separate analog and digital power busses and pins help reduce induced noise. Reduction of the initial current transient that flows through the intrinsic package inductance has also been used to reduce power bus noise at the expense of gate speed. Rather than operating the digital portion of the system asynchronously, synchronous control can also be utilized to make the occurrence of power bus noise

more predictable, thereby providing easier control of the noise . However, the tradeoff is speed. To date, the most effective and widely used scheme has been the employment of guard rings to shield the digital switching noise from the analog circuitry. The disadvantage of this method is the additional die area consumed on the chip.

With the trend towards higher digital speeds, the above mentioned techniques may no longer be effective in minimizing the effects of switching noise. Therefore, new design techniques are needed for the digital circuits. In this thesis, three new circuit topologies based on differential current-mode techniques are introduced: (1) Source-Coupled Logic (SCL); (2) Enhancement Source-Coupled Logic (ESCL), and (3) Folded Source-Coupled Logic (FSCL). These topologies are derived from the bipolar Emitter-Coupled Logic gates and use a constant current source as a mechanism to switch the voltage level. Logic gates developed using these topologies do not generate large current spikes during logic transitions. It will be shown that these new fully-differential gates also have high noise immunity, complementary outputs, small propagation delays, and low energy losses in stray capacitances.

Chapter 2 will examine the operation of the SCL inverter and its design criteria. Based on the SCL, we will introduce the ESCL and the FSCL inverters. In Chapter 3, complex gates using the FSCL topology are presented. Chapter 4 deals with the input-output translators necessary for interfacing the differential current-mode gates to conventional static gates. Finally, experimental results are presented in Chapter 5.

2. SOURCE-COUPLED LOGIC GATES

Although static CMOS gates do not consume power under static conditions, large overlap current spikes are generated during logic-state transitions. In this work, we propose CMOS fully-differential current-mode topologies (similar to bipolar Emitter-Coupled-Logic configurations [9-10]) which employ current steering techniques to maintain an ideally constant current flow from the supplies. Ideally then, the large overlap current spikes characteristic of conventional static logic are eliminated. Another key feature of the source-coupled gates is their reduced logic swing of 500-800 mV compared to the 5 volt swing of conventional logic. There are three main advantages of the reduced logic swing :

- The displacement currents flowing in the power supply lines are reduced due to smaller voltage swing. Since displacement current is given by

$$I_{dis} = C(dV/dt) \tag{1}$$

  where C is the parasitic capacitances (e.g. gate capacitances) of the device and/or the output load capacitance, the reduced logic swing, dV, clearly causes a smaller displacement current.

- The propagation delay is proportionally reduced. From equation (1),

$$\Delta t = \frac{C\Delta V}{I} \tag{2}$$

  Hence, with a smaller logic swing, the delay time needed for the output voltage to change from one logic level to another is reduced.

- The energy loss in stray capacitance (e.g. gate capacitances and drain capacitances) is reduced. Since the energy stored on a capacitor is given by

$$E = \frac{1}{2}CV^2, \tag{3}$$

where C is the stray capacitances and V is the voltage across those capacitances, therefore the smaller voltage swing will cause less energy loss in stray capacitances. Similar to bipolar ECL, the source-coupled logic gates have synchronously-timed complementary outputs.

2.1 SOURCE-COUPLED INVERTER

The Source-Coupled logic inverter (SCL) derived from bipolar ECL is shown in Figure 1. It consists of a cascade of an NMOS differential input stage with PMOS diode-connected loads, and n-channel source-follower output stages. The differential pair, M1-M2, acts as a voltage-controlled current steering stage. Depending on the polarity of the logic voltage applied to the inputs of the differential pair, the tail current, Iss1, will flow through M1 or M2 into its PMOS diode-connected load. Besides steering the current Iss1, the inherent ability of the differential pair to reject any common-mode noise that appears at its inputs enhances the noise immunity of the inverter. The logic voltages that are developed across the PMOS loads are level shifted to the desired dc output level by the source-follower drivers M5 and M6. The source-followers also act as low-impedance output buffers that increase the driving capability of the overall inverter.

Figure 2 shows the complete SCL inverter gate including the dc bias circuits consisting of current mirrors MS1-MS4. Since constant currents are supplied to the inverter irrespective of any logic transitions, we can expect the power supply current to be nearly constant, and hence the noise spikes are significantly reduced. The presence of residual switching noise on the power lines is due to displacement currents induced in the supply capacitances at the nodes of the SCL gate.

In a static CMOS inverter, the total dynamic power consumed by the gate is given by [11]

$$P_{total} = C_L(VDD)^2 f \qquad (4)$$

where C_L is the load capacitance, VDD is the voltage supply, and f is the operating frequency. For the SCL inverter, the total static plus reactive power dissipation is
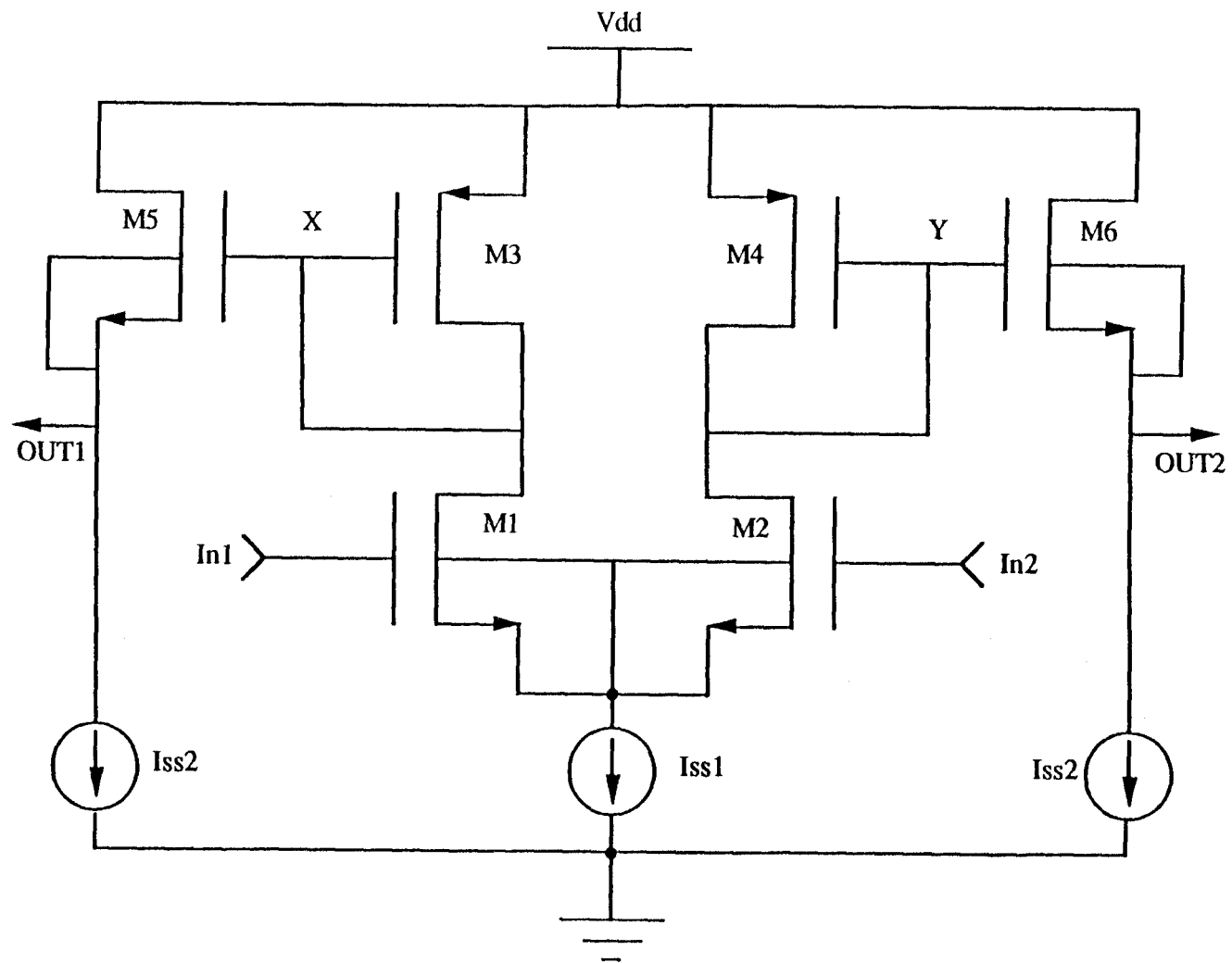
Vdd

M5   X   M3   M4   Y   M6

OUT1

In1   M1   M2   In2

Iss2   Iss1   Iss2

Figure 1 Source-Coupled Logic Inverter

OUT2

Figure 2 Source-Coupled Logic Inverter with bias circuitry shown

$$P_{total} = (Vsup)(Isup) + C_L(Vsw)^2 f \tag{5}$$

where Vsup and Isup are the dc power supply voltage and current, respectively. Since the SCL inverter voltage swing Vsw is small, the total power dissipation is approximately constant to very high frequencies. Comparing the two equations, it is evident that at very high operating frequencies, the total power consumption of the static inverter may actually be higher than for the SCL inverter, because Vsw is an order of magnitude smaller in the SCL gate.

2.1.1 SCL Design

The design procedure for the SCL inverter is as follows. Based on the bias currents and the logic swing of the circuit we are able to determine the size of the input differential pair M1-M2 which determines the input voltage swing. The operating voltage swing is then determined by sizing M3 and M4 appropriately. Next, we can calculate the size of the source-followers M5 and M6 to shift the output voltage to the desired level. The followings are a detailed analysis of the inverter.

Step 1: Determine the device sizes of the differential pair transistors, M1-M2. Define

$$V_{sw} = V_H - V_L$$

where V_H = output logic high voltage
$\quad\quad V_L$ = output logic low voltage.

To begin the design process, we first select the output voltage swing, V_{sw}. The V_{sw} is determined by the minimum required voltage swing to switch the current of the differential pair at the next stage. Using the standard Shichman-Hodges saturation drain-current equation, we determine the size of the differential pair devices, M1 and M2 as

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2Iss1}{K_n(V_{sw})^2} \tag{6}$$

Step 2: Determine the device geometries of the PMOS load devices M3-M4. For a branch that is off, the voltage developed across its PMOS load device is

$$\text{Xmax or Ymax} \approx \text{Vdd} - |\text{Vtp}|.$$

To ensure that the inverter has logic restoring capability, the voltage difference between internal nodes X and Y should be $|\text{Ymax} - \text{Xmax}| > \text{Vsw}$. In other words, the large-signal voltage gain of the circuit should be greater than one. Defining the operating voltage swing as $\text{Vop} = |\text{Vy} - \text{Vx}|$ and assuming M2 is off, we obtain

$$
\begin{aligned}
\text{Vop} &= \text{Vy} - \text{Vx} \\
&= (\text{Vdd} - \text{Vsg}_4) - (\text{Vdd} - \text{Vsg}_3) \\
&= (\text{Vsg}_3 - |\text{Vtp}_4|) \\
&= \sqrt{\frac{\text{Iss1}}{\left(\frac{\text{Kp}}{2}\right)\left(\frac{\text{W}}{\text{L}}\right)_{3,4}}} + |\text{Vtp}_3| - |\text{Vtp}_4|
\end{aligned}
$$

Assuming matched transistor pairs and no back-gate effects,

$$\text{Vop} = \sqrt{\frac{\text{Iss1}}{\left(\frac{\text{Kp}}{2}\right)\left(\frac{\text{W}}{\text{L}}\right)_{3,4}}} \tag{7}$$

Solving for $(\text{W/L})_{3,4}$, we have

$$\left(\frac{\text{W}}{\text{L}}\right)_{3,4} = \frac{\text{Iss1}}{\left(\frac{\text{Kp}}{2}\right)(\text{Vop})^2} = \frac{2\text{Iss1}}{\text{Kp}\,(\text{Vop})^2} \tag{8}$$

Step 3: Determine the logic high and low voltages. In addition to determining the size of the transistors, we must also choose the logic high and low voltages of the inverter. This procedure is similar to finding the input common-mode range of a differential-pair. The lower limit of the logic high voltage is given by

$$V_{HL} = Vgs_1 + Vdsat_{ms3} \quad \text{(with M1 on and M2 off)}$$

$$= \sqrt{\frac{Iss1}{\left(\frac{Kn}{2}\right)\left(\frac{W}{L}\right)_{1,2}}} + Vtn + Vdsat_{ms3} \tag{9}$$

where $Vdsat_{ms3}$ is the saturation voltage of the NMOS device MS3.

The upper limit of the logic high voltage assuming that M1 is on is given by

$$V_{HU} = Vdd - Vsg_3 + Vtn_1$$

$$= Vdd - \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} + |Vtp_3| + Vtn_1 \tag{10}$$

Hence from equations (9) and (10), V_H lies in the range

$$\sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} + Vtn + Vdsat_{ms3} < V_H \leq Vdd - \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} + |Vtp| + Vtn \tag{11}$$

With V_H determined, we then determine the logic low voltage using $V_L = V_H - Vop$.

Step 4: Determine the size of the source-followers devices, M5-M6. Once the logic high and low voltage of the inverter is determined, the amount of voltage required to be shifted by the source-followers can then be used to determine the device geometry of the source- follower and is given by

$$\left(\frac{W}{L}\right)_{5,6} = \frac{Iss2}{\left(\frac{Kn}{2}\right)(Vgs - Vtn)^2} \tag{12}$$

2.2 ENHANCEMENT-LOAD SOURCE-COUPLED INVERTER

The enhancement source-coupled logic inverter (ESCL) shown in Figures 3 and 4 uses the same current steering technique employed in the SCL inverter. The objective of ESCL is to merge the separate gain and level-shifting stages of SCL into a single stage resulting in potentially lower power dissipation and higher speed. The merging of the gain and level-shifting stage was accomplished using diode-connected NMOS load transistors as shown.

2.2.1 ESCL Design

The design procedure for the ESCL is the same as the SCL. We first select the bias current and the logic swing of the inverter. Next, the size of the input differential-pair, M1-M2, is calculated followed by the determination of the logic high and low voltage. With the output voltage determined, we can then calculate the geometry of the NMOS load device, M3-M4.

Step 1: Determine the device geometries of the input differential pair. Since the input stage is the same as for the SCL inverter, this is similar to the first step in SCL design.

Step 2: Determine the logic high and low voltages. The logic high voltage is determined by the branch that is off. Assuming M2 is off,

$$V_H = Vdd - Vtn_4 \tag{13}$$

To guarantee the circuit will maintain the logic swing, the voltage gain of the circuit should be greater than one. Hence

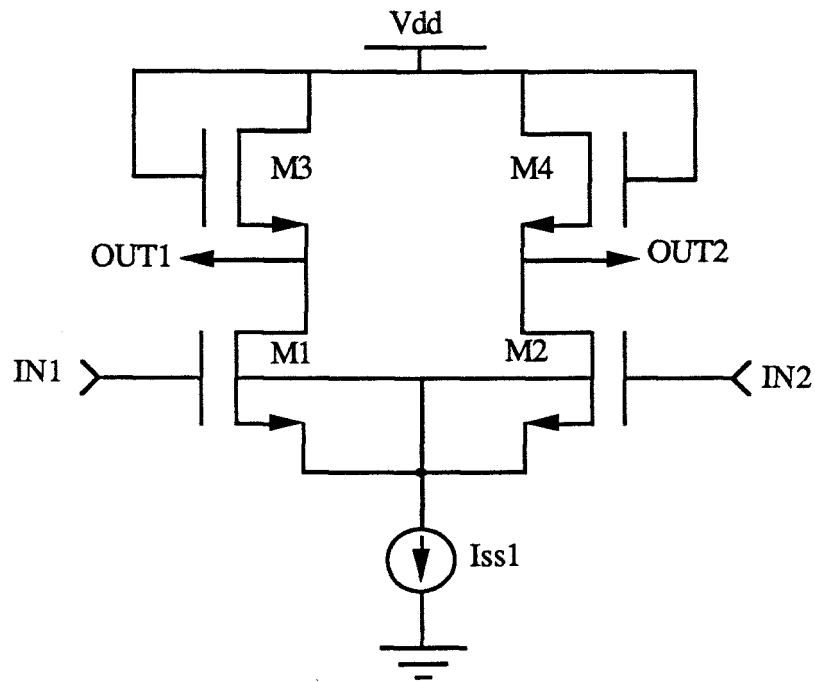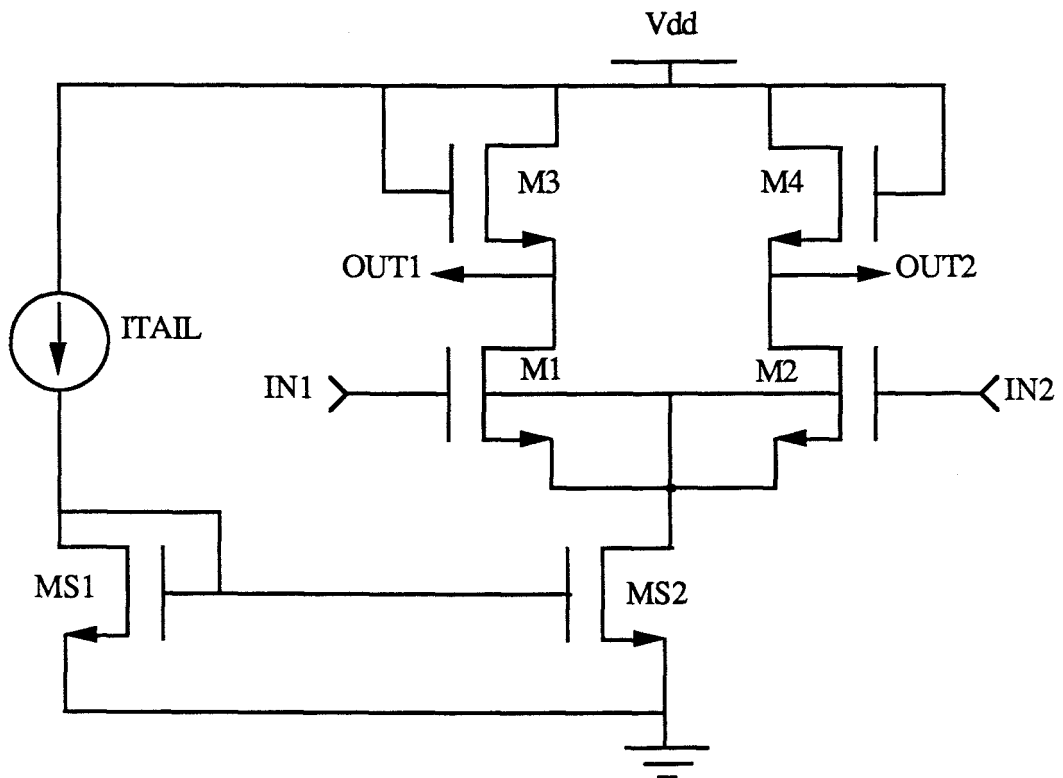$$Vout2 - Vout1 = Vop \geq Vsw \tag{14}$$

Figure 3   ESCL Inverter

Figure 4   ESCL Inverter with bias circuitry

Step 3: Determine the geometries of the NMOS load devices, M3-M4. The size of M3 and M4 can then be determined by

$$V_L = Vdd - Vgs_3$$

$$= Vdd - \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} - Vtn_3$$

If the substrates of M3 and M4 are connected to ground, the threshold voltages of M3 and M4 are given by

$$Vtn_{3,4} = Vto + \gamma \left(\sqrt{Vsb + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{15}$$

In this case, the substrates of M3 and M4 may be connected to the common bulk-source terminal for a p-well process. However, doing so will reduce the speed of the inverter due to the added p-well junction capacitance between the well and the substrate.

Substituting the above for the threshold voltage, we have

$$V_L = Vdd - \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} - Vto - \gamma \left(\sqrt{Vsb + 2\phi_F} - \sqrt{2\phi_F} \right)$$

With $Vsb = V_L$,

$$V_L = Vdd - \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} - Vto - \gamma \left(\sqrt{V_L + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{16}$$

Expressing in term of $\left(\frac{W}{L}\right)_3$,

$$\left(\frac{W}{L}\right)_3 = \frac{Iss1}{\left(\frac{Kn}{2}\right)} \left[\left(Vdd - V_L - Vto - \gamma \left(\sqrt{V_L + 2\phi_F} - \sqrt{2\phi_F} \right) \right) \right] \tag{17}$$

As seen, calculating device sizes in ESCL is simpler compared to the SCL inverter.

2.3 FOLDED SOURCE-COUPLED INVERTER

Based on the above discussion of the ESCL gate, it is desirable to merge the separate gain and level-shifting stages into a single stage. Furthermore, if the circuit is implemented in p-well technology it is desirable to have only constant current sources connected to Vdd. Since Vdd is directly connected to the substrate by using constant sources, minimal displacement current would flow from Vdd to the substrate reducing the noise propagated to the analog section. With these objectives in mind, the folded source-coupled logic (FSCL) has been developed. In the FSCL inverter topology (Figures 5 and 6), the gain and level-shifting functions have again been merged by employing a common-gate PMOS output structures, M3-M4. Like SCL, the input stage uses high transconductance NMOS transistors to maintain the highest possible speed. In addition to the single-stage topology, another major advantage of the FSCL technique is that only constant current sources, Iss2, are connected to the Vdd power bus. Therefore, displacement currents are prevented from generating noise spikes which may be coupled into the substrate via Vdd.

2.3.1 FSCL Design

The design methodology for FSCL is again very similar to SCL. We first select the bias currents and voltage swing of the inverter. Next the geometry of the input differential-pair is determined followed by the logic high and low voltages. With these voltages, we can then determined the size of the PMOS diode-connected load, M3-M4. Like SCL, the input stage uses high transconductance NMOS transistors to maintain the highest possible speed. In addition to the single-stage topology, another major advantage of the FSCL technique is that only constant current sources, Iss2, are connected to the Vdd power bus. Therefore, displacement currents are prevented from generating noise spikes which may be coupled into the substrate via Vdd.
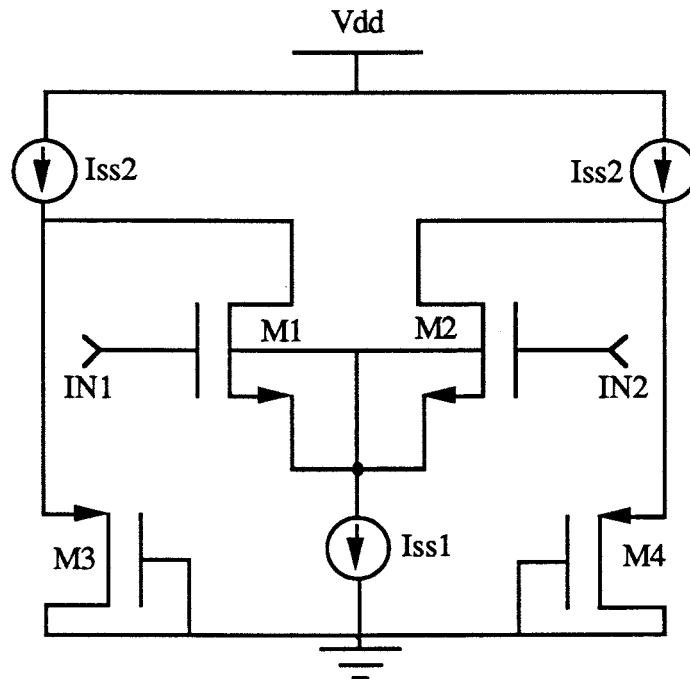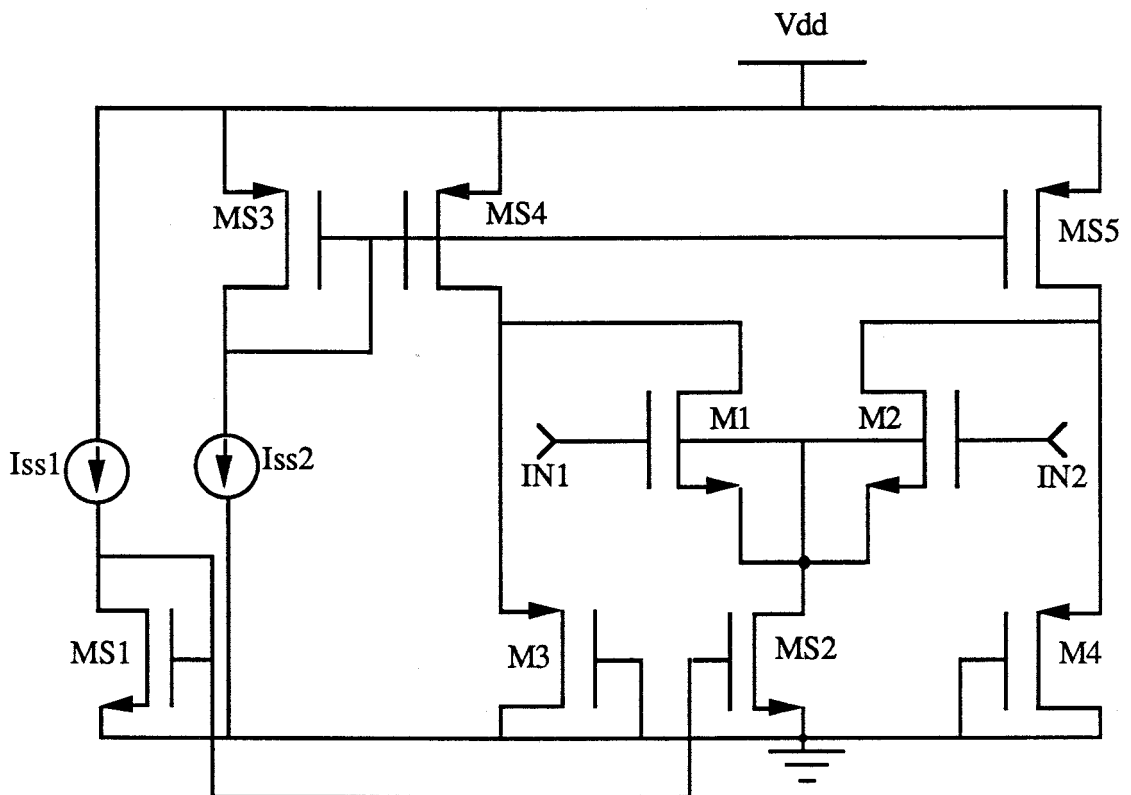
Figure 5   FSCL Inverter

Figure 6   FSCL Inverter with bias circuitry

Step 1: Determine the geometries of the input differential pair, M1-M2. This is the same as step 1 of SCL.

Step 2: Determine the logic high and low voltages. The input high logic voltage range is equivalent to the input common-mode range of the differential pair and is given by

$$Vtn + Vdsat_{ms2} + \sqrt{\frac{Iss1}{\left(\frac{Kp}{2}\right)\left(\frac{W}{L}\right)_3}} < V_H \leq Vdd - Vdsat_1 + Vtn. \tag{18}$$

With V_H selected, we select V_L such that $V_H - V_L > Vop$. In this case, V_H is generated by Iss2 flowing into a diode-connected PMOS load M3, and V_L is determined by the difference current (Iss2 - Iss1) flowing through the other PMOS load M4.

Step 3: Determine the sizes of the PMOS load devices, M3-M4. For logic high voltage V_H:

$$\left(\frac{W}{L}\right)_3 = \frac{Iss2}{\left(\frac{Kp}{2}\right)(V_H - |Vtp|)^2} \tag{19}$$

For logic low voltage V_L,

$$\left(\frac{W}{L}\right)_4 = \frac{Iss2 - Iss1}{\left(\frac{Kp}{2}\right)(V_L - |Vtp|)^2} \tag{20}$$

Since both devices' aspect ratio are the same, we equate equations (19) and (20)

$$\frac{Iss2}{\left(\frac{Kp}{2}\right)(V_H - |Vtp|)^2} = \frac{Iss2 - Iss1}{\left(\frac{Kp}{2}\right)(V_L - |Vtp|)^2}$$

$$Iss1 = Iss2\left[1-\left(\frac{V_L - |Vtp|}{V_H - |Vtp|}\right)\right]^2 \tag{21}$$

This gives us the relationship between Iss1 and Iss2.

2.4 SIMULATION RESULTS

SPICE simulations were performed to compare the types of inverters. The simulations are carried out to compare and measure the delay versus fanout, delay versus power dissipation, and the Vdd spike amplitudes generated by each inverter. All simulation results assume a 2 μm p-well digital CMOS technology from MOSIS.

2.4.1 Delay Versus Fanout

Unlike a TTL gate, the CMOS gates exhibit zero input gate current. Therefore, the fanout capability of CMOS gates under a static condition is infinite. However, due to the parasitic capacitances of the MOSFET, the propagation delay of the gate will be inversely proportional to its fanout. To ensure a good comparison is made for each type of inverter, the main bias current of all the inverters are chosen to be the same, i.e. Iss2(SCL) = Iss1(ESCL) = Iss2 (FSCL) = 0.1 ma. Besides same bias current, the voltage swing of the inverters are designed to be the same which is 800 mV. To obtain this characteristic curve, a cascade of five inverters is created and the delay is measured between the second and the fourth gate. For different fanout, the appropriate numbers of gates are connected at the outputs of each inverter. Figure 7 shows the simulated delay vs. fanout results for the different gates.
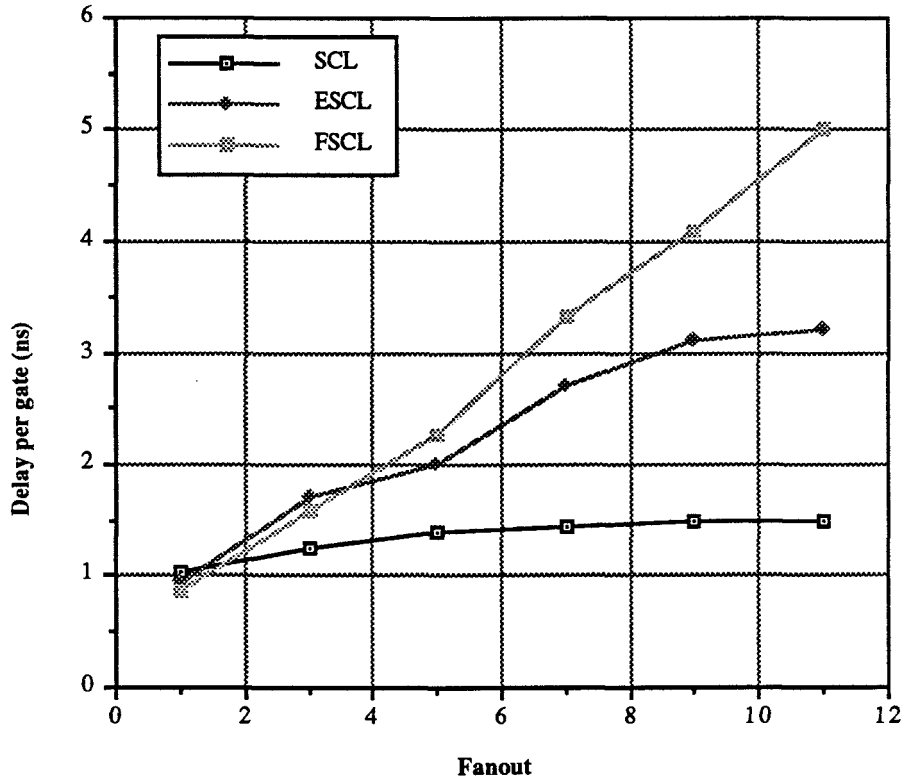
Figure 7   Fanout characteristic of our source-coupled inverters

As explained in the previous section, the output stages of SCL act as low-impedance output buffers so that the deviation in propagation delay with increased fanout is minimized. From the graph, the curves are approximately linear therefore we can extrapolate the curves for larger fanout.

2.4.2 Delay Versus Power

The sizes used for this characterization is obtained from the above section. The Power-Delay-Curve characteristic is obtained by varying the bias current of the circuit. The size of transistors are also sized so as to achieve the same voltage logic level and voltage swing. The simulated power-delay results for the three types of inverters are shown in Figure 8. Each curve exhibited some form of exponential characteristic and can be explained easily. As we increase the power, we increase the current.

Consequently, the time required to charge the capacitances is reduced. This effect creates the negative slope in the diagram which corresponds to a constant power-delay product. By increasing the current, we must also increase the size of the transistors in order to maintain a constant logic swing thereby making the parasitic capacitances larger. Therefore, a point is reached where the increase in capacitances dominates the reduction in delay due to the increase in charging currents.
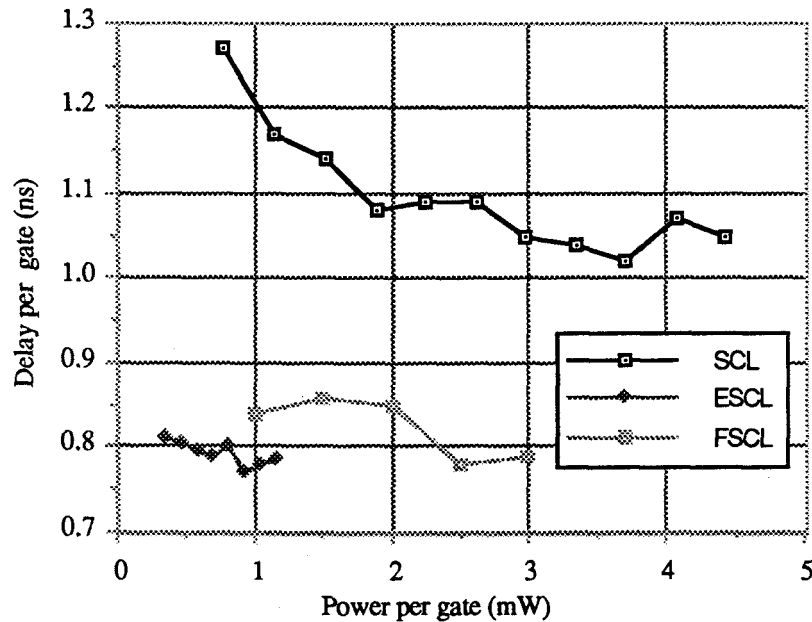
Figure 8   Power-Delay curves of our source-coupled inverter

2.4.3 Noise Spikes

As our main objective in developing these new gates was to reduce the switching noise spike generation, a detailed noise comparison to a static gate is necessary. As shown in Figure 9 there is at least two order of magnitude in digital noise reduction on the power lines by using the various source-coupled logic gates.
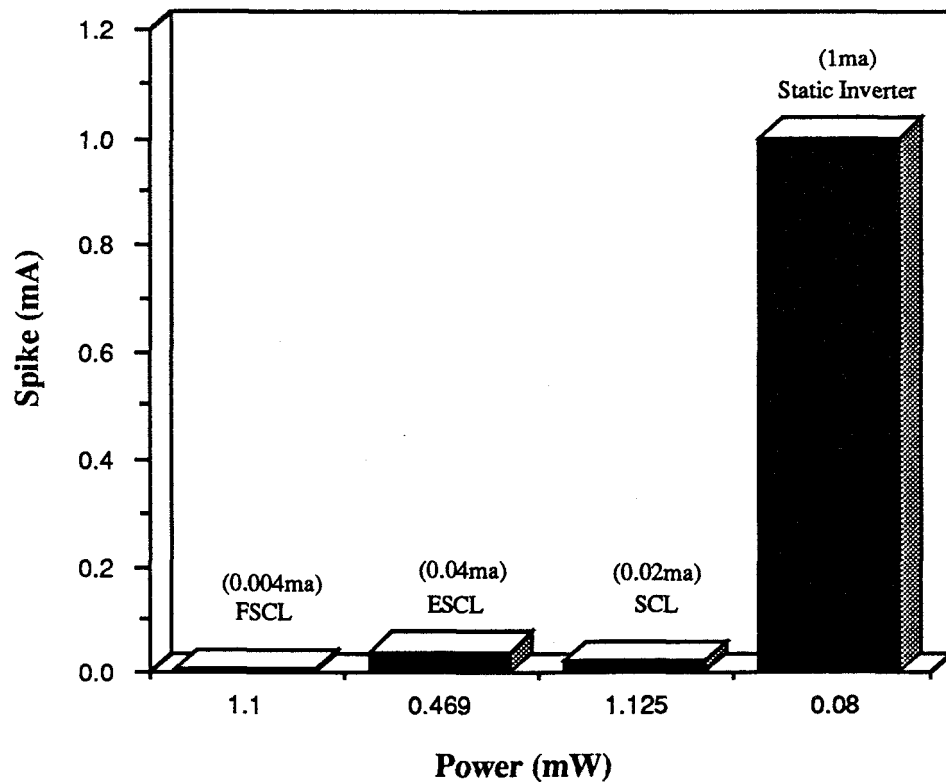
Figure 9   Noise spike comparison between our gates and static inverter

2.4.4 Speed Comparison

To ensure that the trade-off between speed and noise is tolerable, a comparison of speeds is necessary (Figure 10). Note that our gates are almost two times slower than the static inverter but we gain at least two orders of magnitude in reduction of switching noise. Furthermore, the SCL, ESCL, and FSCL gates provide complementary outputs. Complementary outputs would require the use of another cascaded static inverter in conventional logic, thus doubling its effective propagation delay to where it is comparable with the SCL gates.
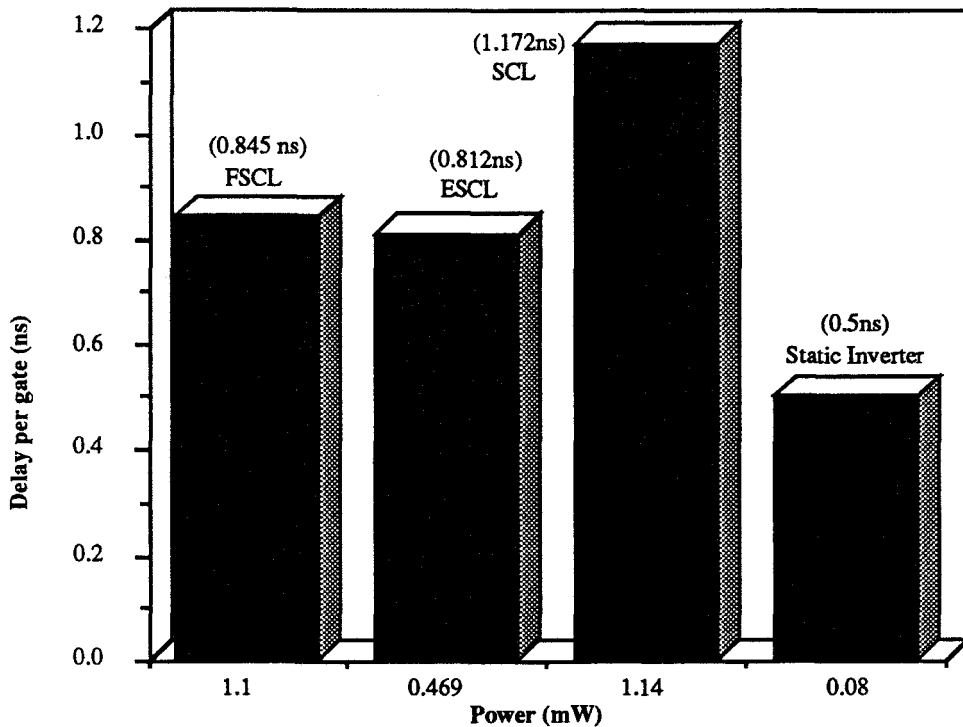
Figure 10   Speed comparison of different types of inverters

2.4.5 Power Consumption Versus Frequency Curves

Although SCL gates may at first appear to consume more power than static gates, at higher operating frequencies the total power loss of the static inverter is greater then the SCL. With SCL gates maintaining a constant flow of current irrespective of frequency, a cross-over point is reached where the dynamic power of the static gates exceeds the total power dissipation of the new gates. Figure 11 shows the simulation results. This curve is obtained by clocking the input of the cascade of inverters and varying the frequency of the clock and noting the average power consumed per gate at each frequency.

As can been seen, the power consumed by the static inverter increases linearly with frequency whereas the FSCL gate is approximately constant. This agrees well with the theory. The dotted line on the graph indicates what will happen to the total power dissipation of the FSCL gate at high operating frequency. The gradient of this line

which represents reactive power is smaller than the slope of the static inverter since the FSCL's logic swing is about ten times smaller.
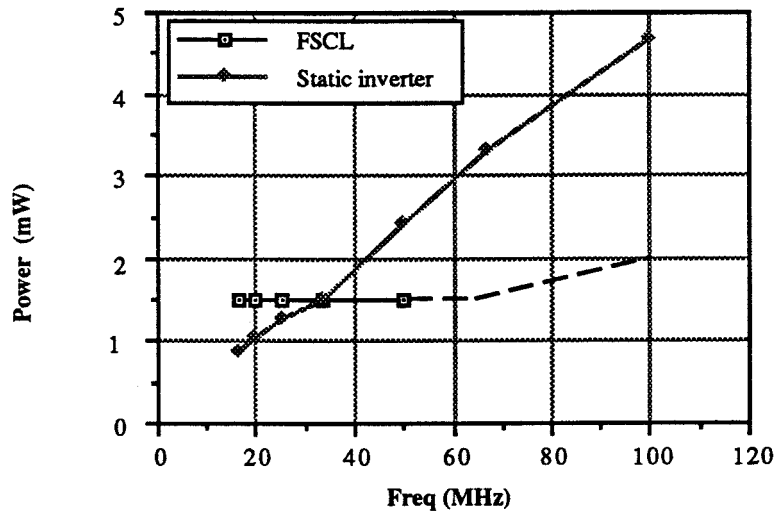

Figure 11   Power consumption versus frequency curves

* The table below shows the sizes used for the simulation of the Power versus Frequency curve.

FSCL

Vdd = 5 volts	
Bias Current, Iss1 = 0.1 mA	Bias Current, Iss2 = 0.2 mA
Size for M1-M2, $\dfrac{W}{L} = \dfrac{16\ \mu m}{2\ \mu m} = 8.5$	Size for M3-M4, $\dfrac{W}{L} = \dfrac{4\ \mu m}{2\ \mu m} = 2.0$
Size for MS4-MS5, $\dfrac{W}{L} = \dfrac{22\ \mu m}{2\ \mu m} = 11$	Size for MS2, $\dfrac{W}{L} = \dfrac{11\ \mu m}{2\ \mu m} = 5.5$

Static Inverter

PMOS size $= \dfrac{88\ \mu m}{2\mu m} = 44$ NMOS size $= \dfrac{48\mu m}{2\mu m} = 24$

In summary, we see that the SCL has the slowest speed compared to the ESCL and the FSCL but its fanout capability is the best among the other new topologies. On the other hand, the FSCL has the lowest Vdd current spike generation but has the worst fanout capability. The ESCL is the intermediate between the SCL and the FSCL in

terms of Vdd current spike generation and fanout capability. However, ESCL exhibits the lowest power consumption for a given speed.

3. COMPLEX GATE GENERATION

In this chapter, we develop a class of higher-level gates using the basic FSCL topology. The other two topologies can also be chosen for the development of complex gates in a similar manner, but FSCL was chosen here because of its lower spike generation.

3.1 BASIC IDEAS IN DEVELOPING COMPLEX GATES

The output structure for the higher-level gates remains the same as for the inverter. We split the total logic gate structure into two parts: the output section and the logic function mechanism (see Figure 12). The output stages consist of the current sources, Iss2, and the PMOS load devices, M1-M2. The output dc level is generated in the same manner as for the inverter. Therefore, size calculations for the inverter can be directly applied to the complex gates without modification.

To create the logic function mechanism, we can cascade a series of "gates". This technique, which is known as "series gating", does not increase the power consumption of the gate. It also requires fewer additional components that it is attractive as a standard synthesis technique for complex circuits. As an illustration of this technique, we compare the number of transistors needed to create a D-type flip-flop (Figures 13 and 14). It is obvious that only four additional transistors are needed to create the flip-flop from an FSCL inverter, whereas 10 additional transistors are needed from the static inverter.

3.2 SERIES GATING TECHNIQUE

The "series gating" uses a series cascade of "gates". There are only two configurations of "gates" needed to create any complex function: the differential pair and the cross-coupled differential pair (Figure 15).
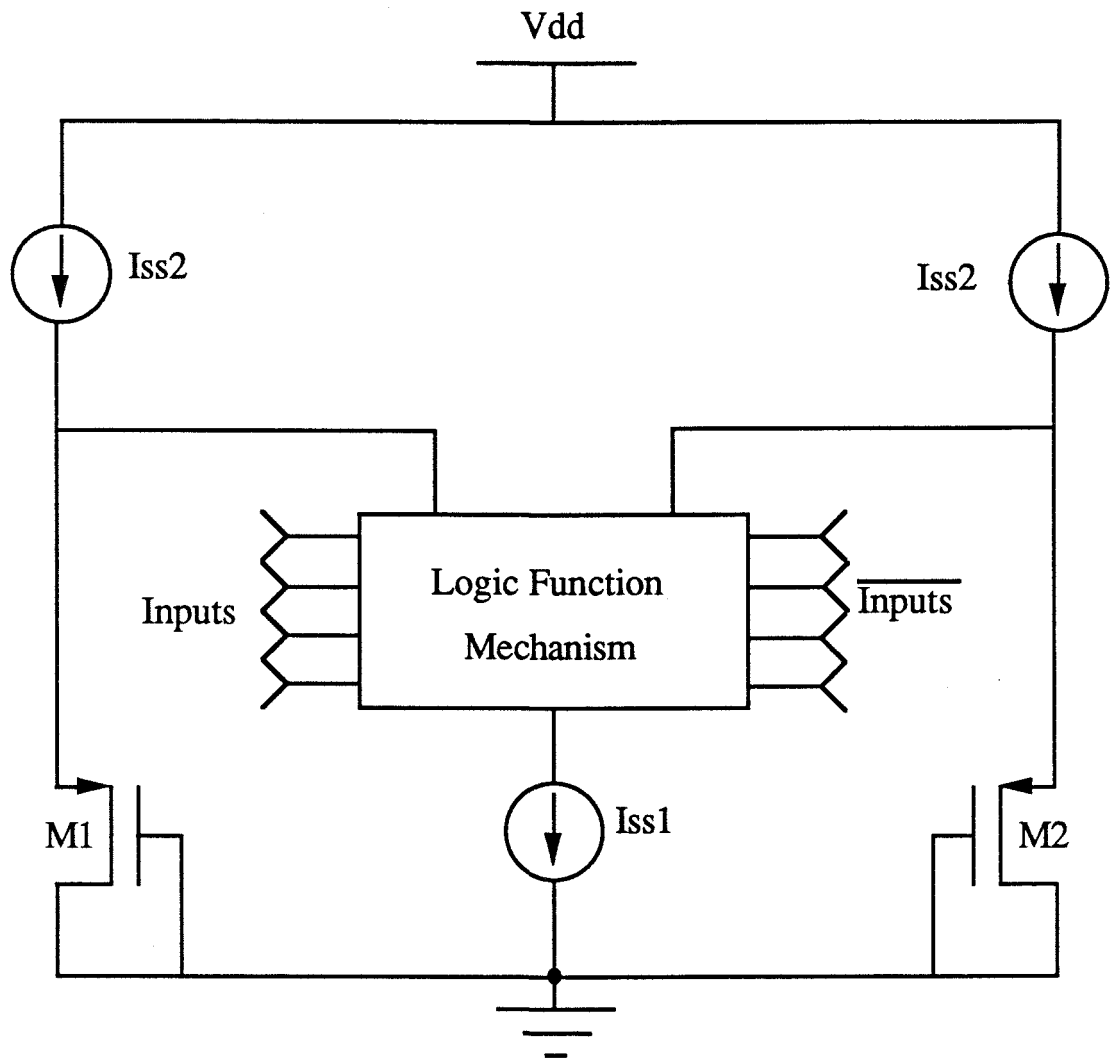
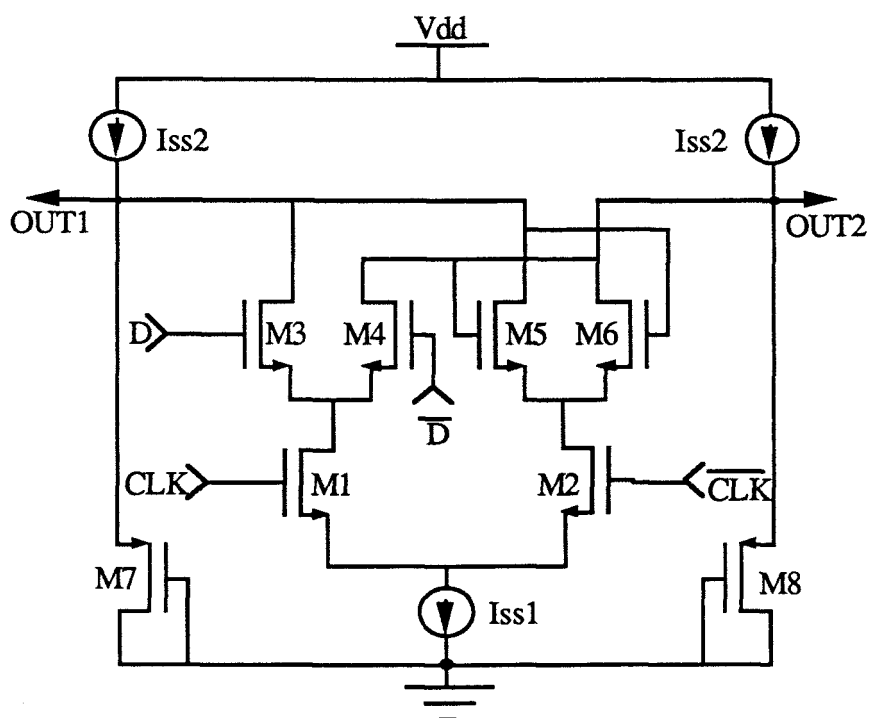**Figure 12   General structure of complex gates**
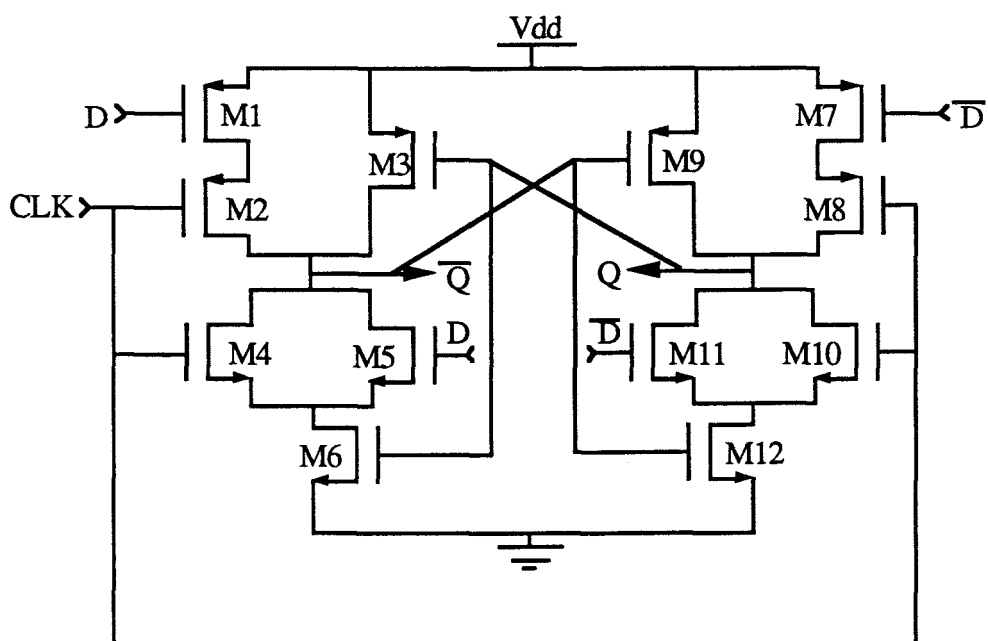
Figure 13   FSCL D-Type Flip-Flop
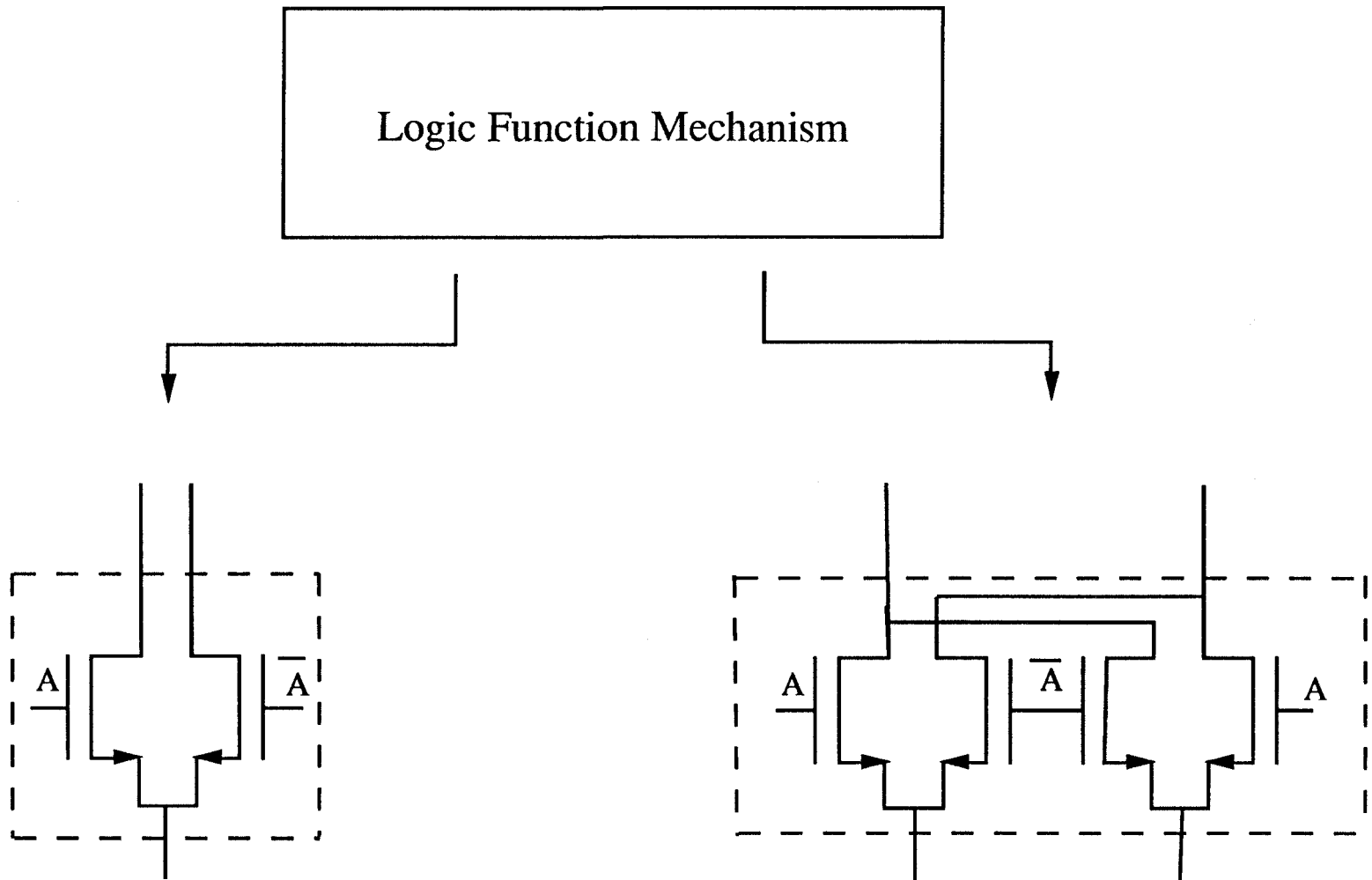

Figure 14   Static D-Type Flip-Flop

Figure 15   "Gate" circuitry for creating the logic function mechanism

To determine which "gate" circuitry to use, we first factor the complex function into complementary sub-expressions. We continue this recursively for both sub-expressions until factoring can no longer be achieved. The complement factorization is a consequence of our gates having complementary outputs. In general, the factored expressions will take either of two forms:

$$X = \left. \begin{array}{l} AB'+A'B \\ A'B'+AB \end{array} \right\} \text{Form I}$$

(Sum of two products)

Or

$$X = \left. \begin{array}{l} A'+B' \\ (A'+B')' \end{array} \right\} \text{Form II}$$

(Sum of two variables)

For those expressions in Form I, we create the function using a cascade of a differential pair and a cross-coupled differential pair. For the Form II type of expression, we use only the differential pair configuration. As an illustration of the above procedure, an example is shown below and a family of gates is developed.

Example: *For this example we implement the sum function of a 1-bit ripple adder.*

$$Sum = A'B'C + A'BC' + AB'C' + ABC$$

Step 1: Factor the expression into a combination of Form I and Form II formats:

$$Sum = C(A'B' + AB) + C'(A'B + AB')$$

The expressions in parenthesis are form I and can be implemented using a cascade of a differential pair and a cross-coupled differential pair as shown in Figure 16.
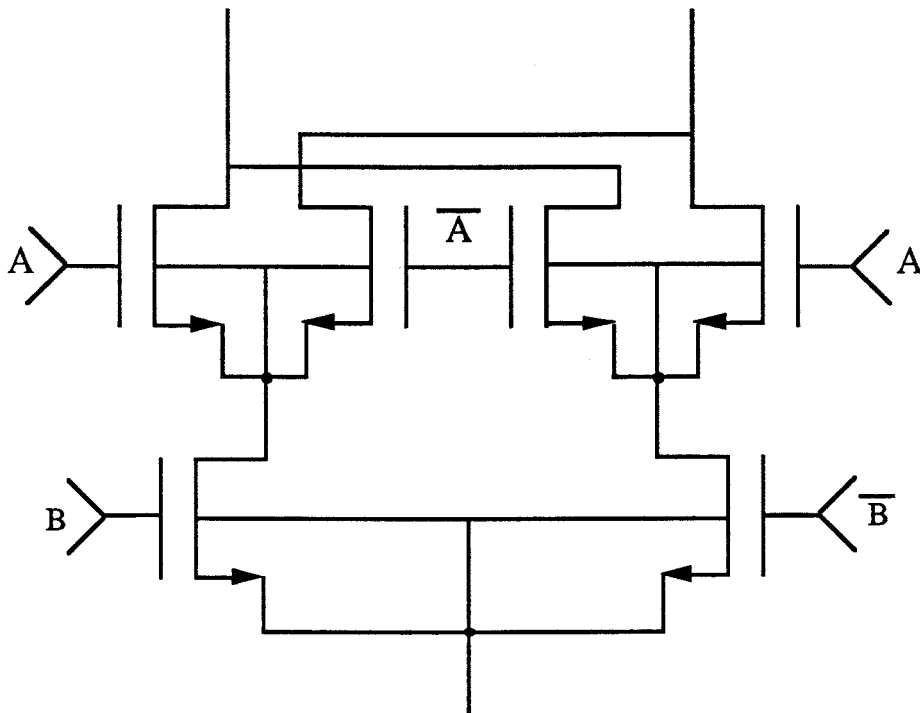
Figure 16   Connection for the expressions (A'B' + AB) and (A'B + AB')

Step 2: Next, we substitute a dummy variable into the parenthesis, noticing that one sub-expression is the complement of the other.

Sum = CX + C'X'   where X and X' are the dummy variables

Again, the simplified expression can be implemented using the same circuitry as above shown in Figure 17.
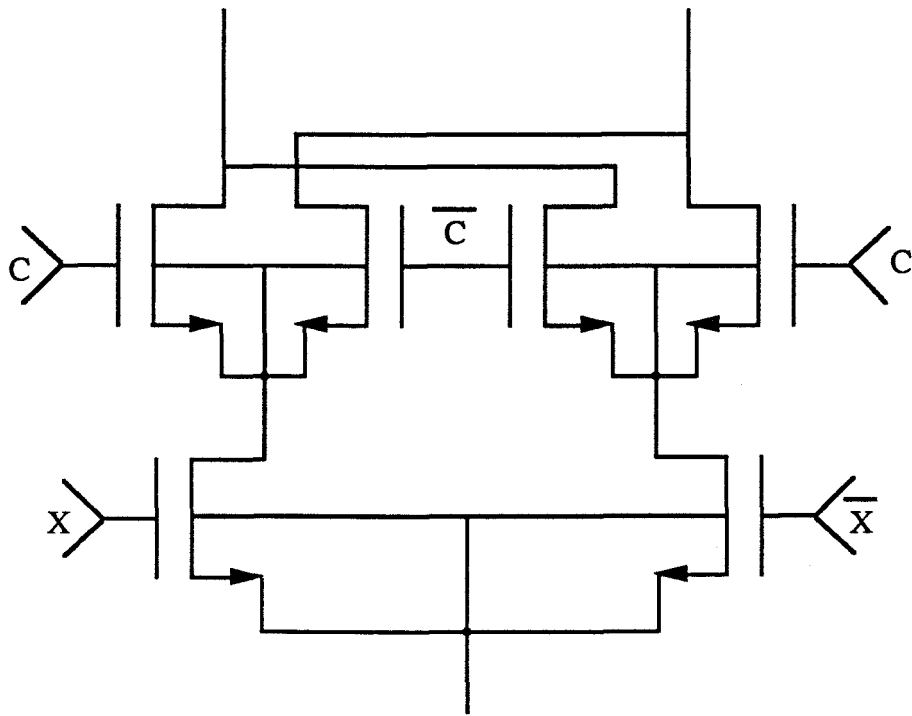
Figure 17   Connection for the function (CX + C'X')

Step 3: We now combine the circuits by replacing the X inputs to the differential pair by the former circuit, finally giving the complex circuit shown in Figure 18.

As illustrated by this example, by using the two types of "gate" circuits, we can create a complex function without difficulty. Another important point to mention is that the transistor sizes calculated for the inverter can also be used for the complex gates which speeds up the design process.

Some basic gate structures will be developed following the technique shown in the previous section. Sizes for all gates can be obtained from the inverter analysis given previously.

Figure 18   The schematic for the sum function of a 1 bit adder

3.3 BASIC GATES

Some basic gate structures will be developed following the technique shown in the previous section. Sizes for all gates can be obtained from the inverter analysis given previously.
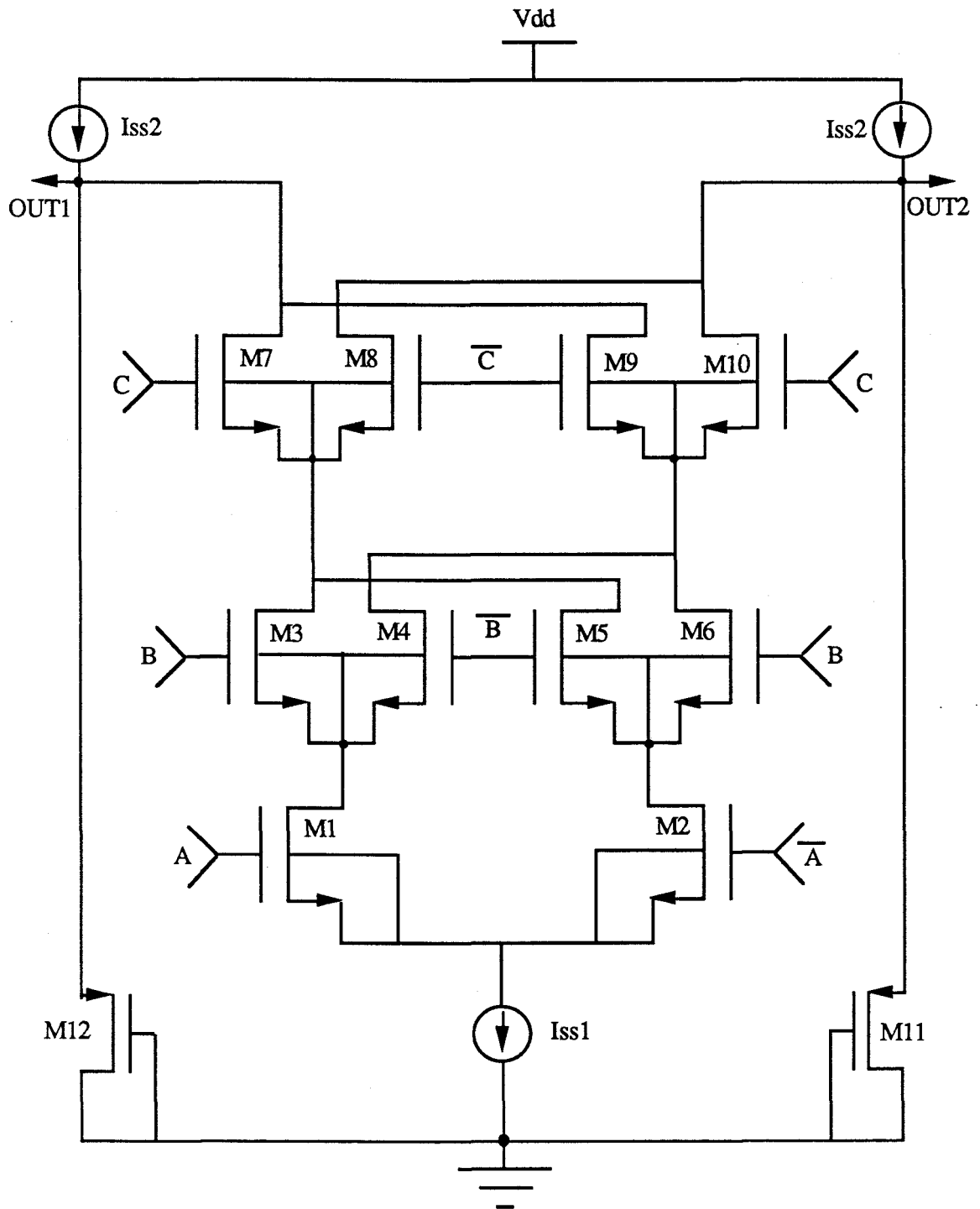
NAND/AND Gate

$$NAND = (AB)'$$
$$= A' + B'$$

The schematic for the AND/NAND gate is shown in Figure 19 and this is similar to form II given before.

NOR/OR Gate

$$OR = A + B$$

which is also form II. Note that we can generate the OR/NOR from the AND/NAND gate by first inverting the input signal. This will not increase the gate count as the previous gate feeding this gate has complementary outputs. Therefore, it is the connection from the previous stage to the AND/NAND gate that determines whether the gate is performing the AND/NAND function or OR/NOR function.

Exclusive NOR/OR Gate

$$Xor = AB' + A'B$$

This is in form I format therefore the exclusive NOR/OR gate is simply a cascade of a differential pair and a cross-coupled differential pair gate (Figure 20).

D-Type Flip-Flop

The expression for the D-type flip flop is given by

$$Qn = Clk*D + Clk'*Qn-1 .$$

This is form I format and the schematic of the D-type flip-flop is shown in Figure 21. Note that the inputs to one of the cross-coupled differential pairs is fed from the outputs to achieve the desired latching function.
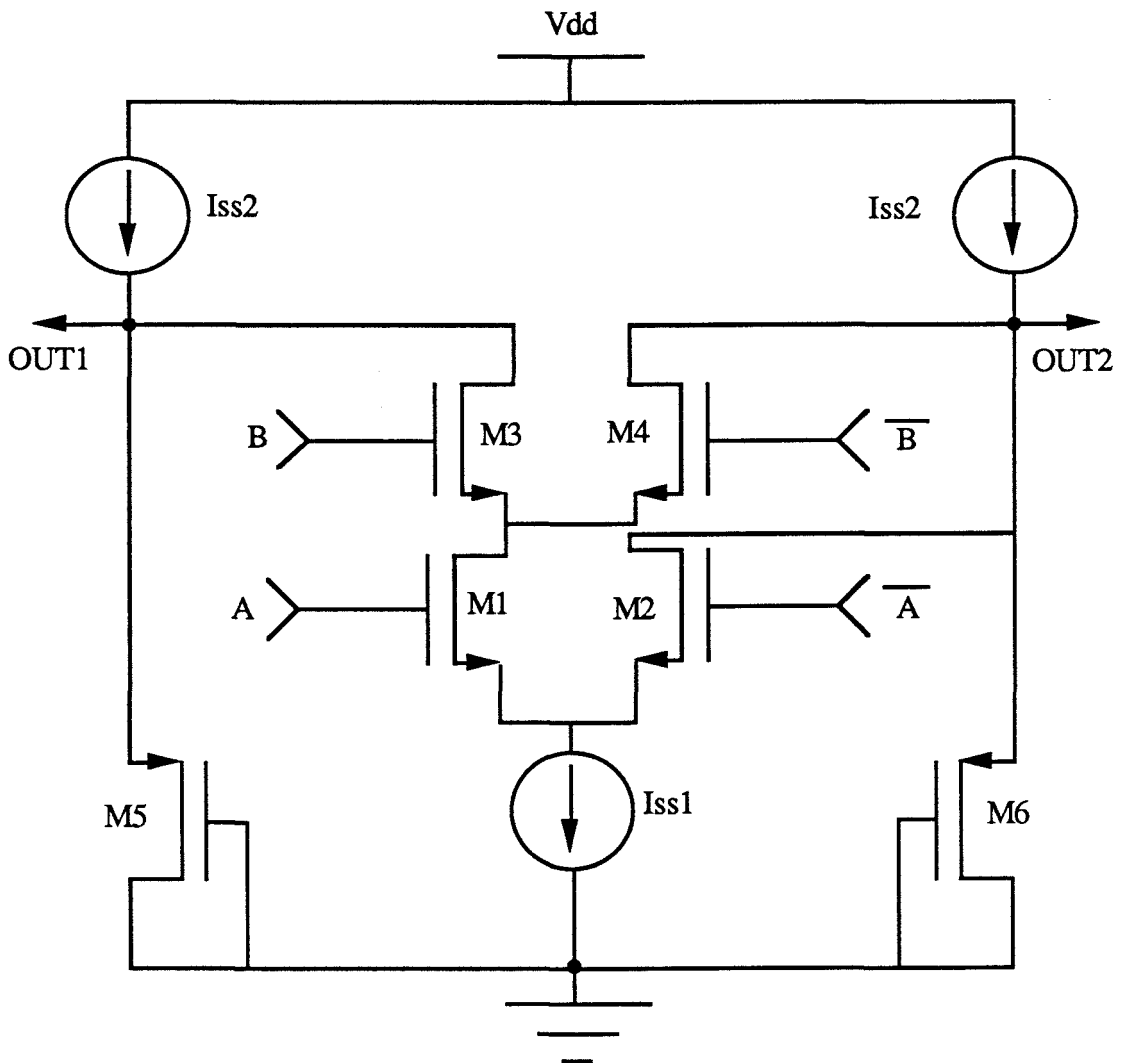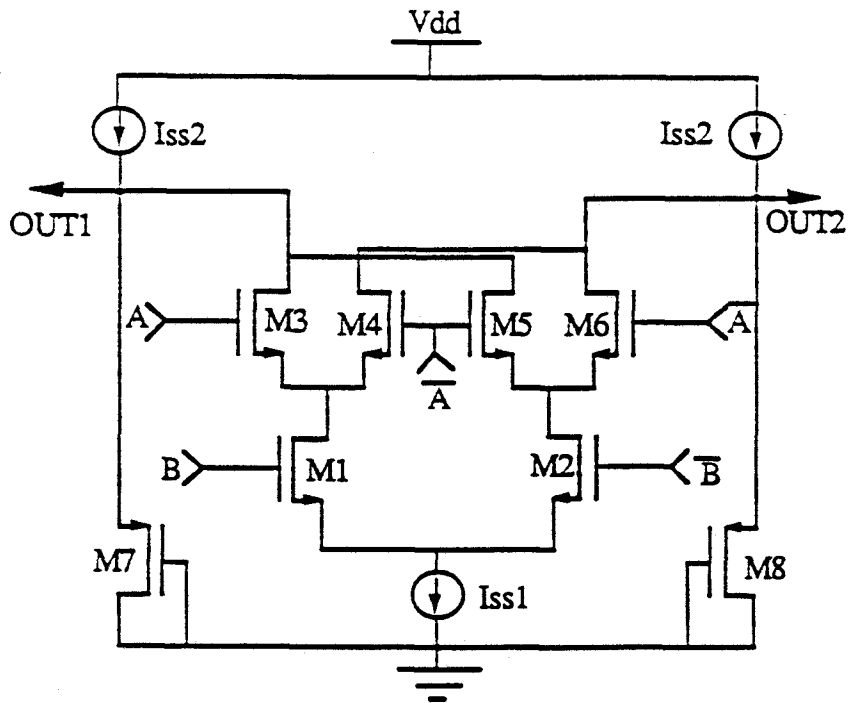

Figure 19   NAND/AND gate

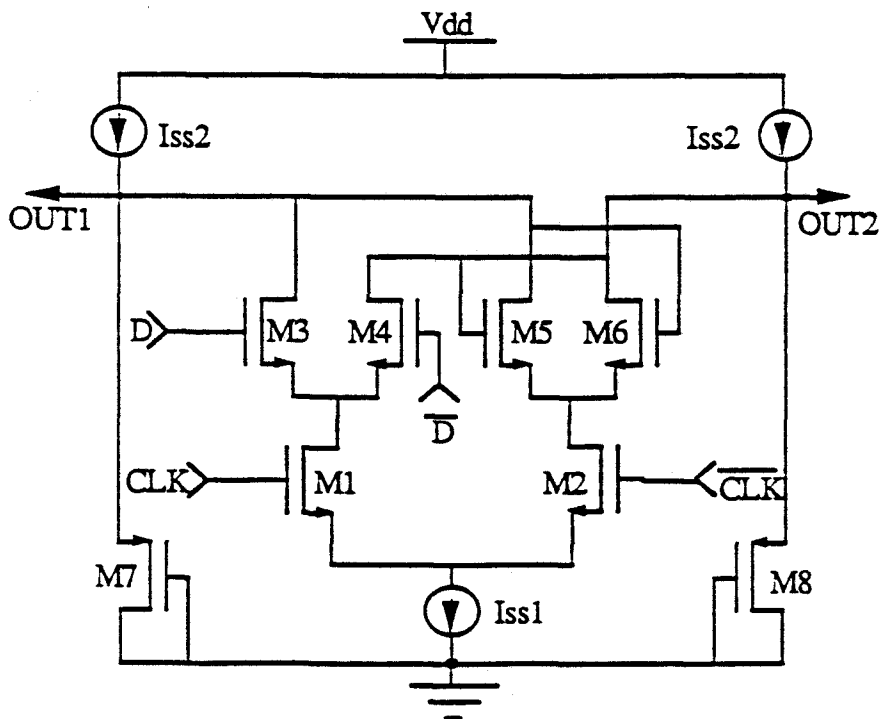Figure 20   Exclusive NOR/OR Gate

Figure 21 FSCL D-Type Flip-Flop

3.4 SIMULATION RESULTS FOR NAND/OR GATES

The powerful technique of series gating has been used to create several complex functions. The steps needed in using this technique have been illustrated through the use of an example. Some basic gates have also been shown. What is left now is to see the performance of these gates, as for example, the Nand/And gate. At the same time, we also show the performance of the Nor/Or gate.

3.4.1 Power-Delay Curve For Two Input NAND/AND Gate

Similar to the inverter, the curve is obtained by varying the bias currents while sizing the transistors to obtain the same logic swing and voltage level. The power consumed by the gate and its corresponding delay is then being noted. The shape of the power-delay curve is similar to the FSCL inverter's curve (Figure 22). This is not surprising as the NAND/AND gate structure was derived from the inverter. With lower power, the current available to charge the load capacitances is less and therefore the propagation delay is longer. For the same power, the speed of the NAND/AND gate is slower than the inverter because the logic function was realized by stacking two differential pairs resulting in reduced transconductances and larger capacitances. Hence, the steering of the current from one differential pair to the other is slower resulting in longer propagation delays for the NAND/AND gate.
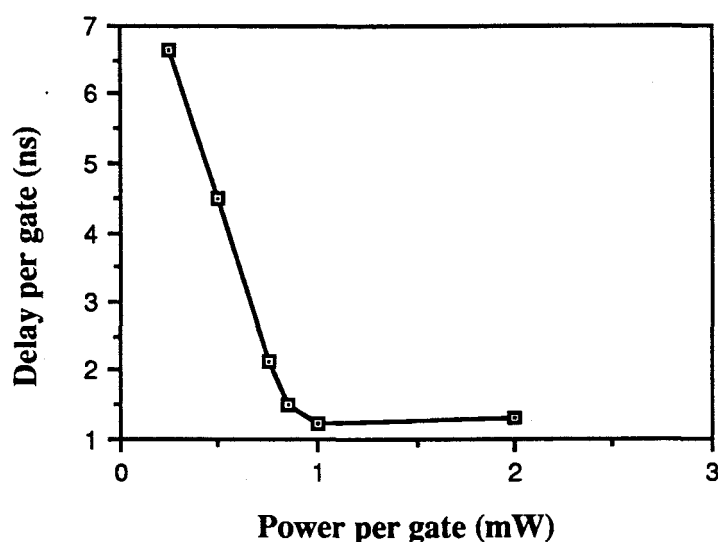
Figure 22   Power Delay Curve for a 2 Input Nand/And gate

3.5. INPUT/OUTPUT TRANSLATORS

Since the source-coupled gates are not TTL compatible, the need to interface to the present standard is evident. Input translators are designed for interfacing from the TTL logic level to the same source-coupled gate logic level whereas output translators do the reverse.

3.5.1 Input Translator

The TTL-FSCL input translator (Figure 23) is simply an FSCL inverter with one of its inputs tied to a dc bias voltage. This bias voltage is set to be in the middle of the TTL logic range. The other input is connected to the previous TTL level logic gate. With this arrangement, the voltage difference between the inputs due to the single-ended input is half that available with a fully-differential input. To compensate for this, the size of the input differential pair is scaled up by two times.

3.5.2 Output Translator

A differential-input to single-ended output scheme is used for the FSCL to TTL output translator, Figure 24. In this scheme, the voltage gain of one of the transistor of the differential pair is mirrored to the output via the diode-connected NMOS device M3.
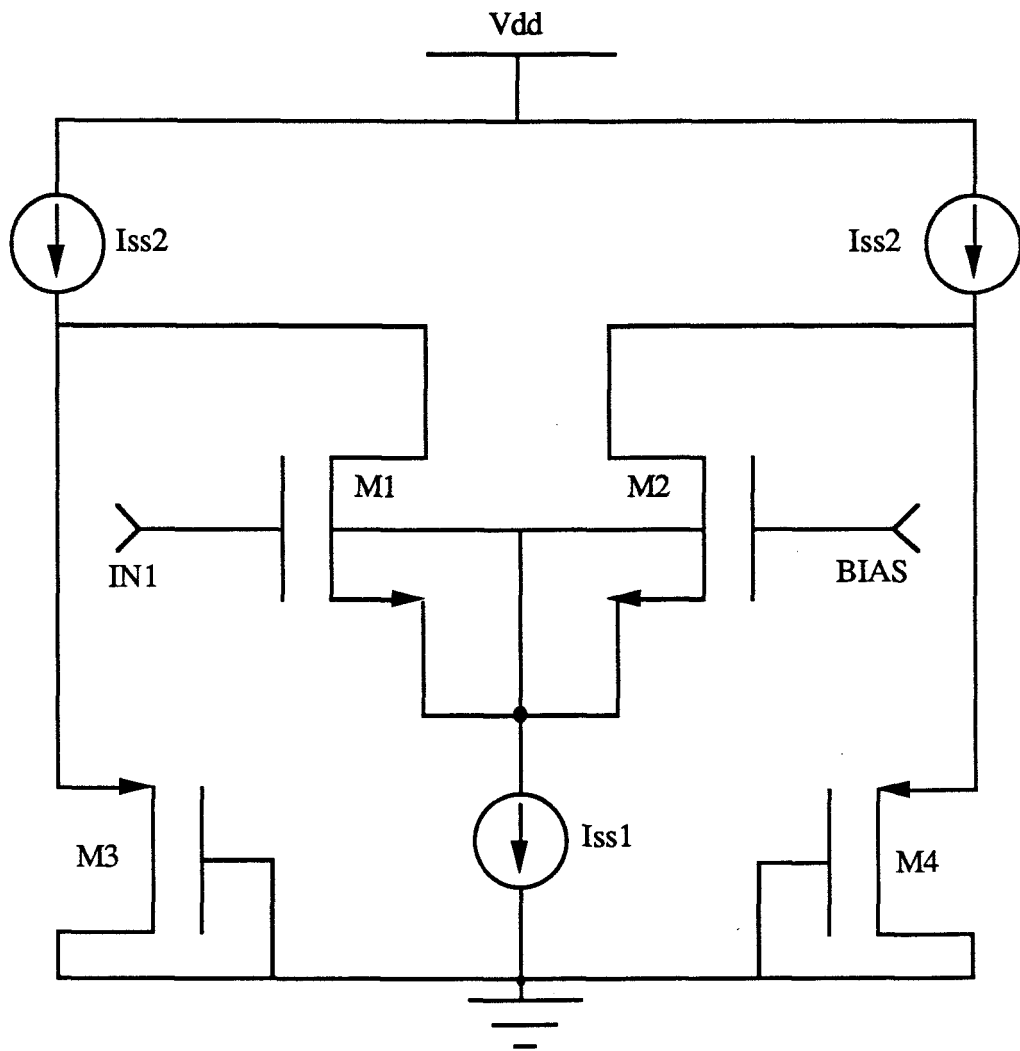
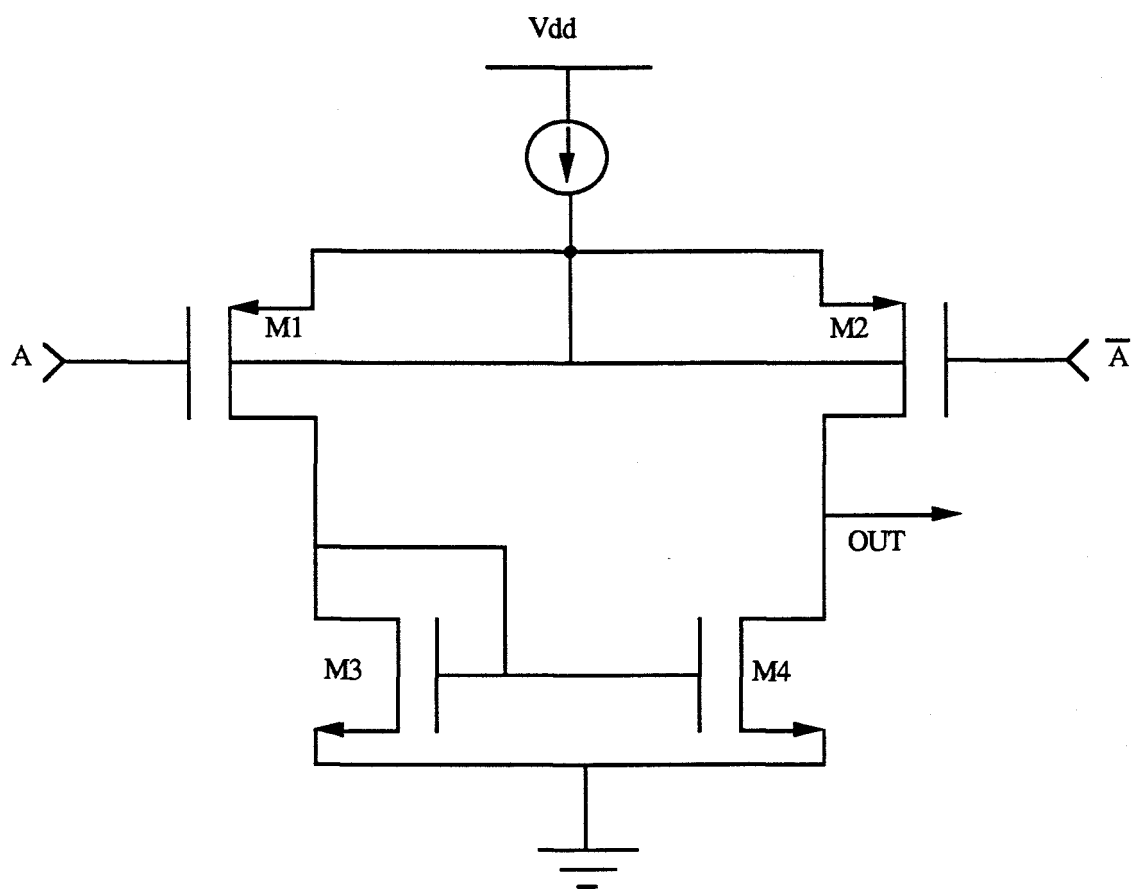Figure 23   TTL-FSCL input translator

Figure 24   Output translator

4. EXPERIMENTAL RESULTS

Several circuits using the new gates have been fabricated using a 2 um p-well CMOS process. Ring oscillators using ESCL and FSCL have been fabricated to measure the maximum speed and switching noise. To further characterize the FSCL inverter, a cascade of inverters with different fanouts have been fabricated. On a larger scale, a 4-bit ALU is being tested with preliminary results showing that it is capable of running faster than 50 MHz. Specific test results follow:

4.1 ESCL RING OSCILLATOR

Number of stages = 39	
Vdd = 5 volts	Bias Current, Iss1 = 0.2 mA
Size for M1-M2, $\dfrac{W}{L} = \dfrac{40\ \mu m}{2\ \mu m} = 20$	Size for M3-M4, $\dfrac{W}{L} = \dfrac{13\ \mu m}{2\ \mu m} = 6.5$
Frequency (measured) = 20 MHz	Frequency (simulated) = 24 MHz
Propagation delay (measured) = 641 ps	Propagation delay (simulated) = 534 ps
Power per gate (measured) = 1 mW	Power per gate (simulated) = 1 mW
Speed Power Product (measured) = 641 fJ	Speed-Power-Product (simulated) = 534 fJ

4.2 FSCL RING OSCILLATOR

Number of stages = 39	
Vdd = 5 volts	
Bias Current, Iss1 = 0.1 mA	Bias Current, Iss2 = 0.2 mA
Size for M1-M2, $\dfrac{W}{L} = \dfrac{17\ \mu m}{2\ \mu m} = 8.5$	Size for M3-M4, $\dfrac{W}{L} = \dfrac{5\ \mu m}{2\ \mu m} = 2.5$
Size for MS4-MS5, $\dfrac{W}{L} = \dfrac{18\ \mu m}{2\ \mu m} = 9$	Size for MS2, $\dfrac{W}{L} = \dfrac{11\ \mu m}{2\ \mu m} = 5.5$
Frequency (measured) = 18.2 MHz	Frequency (simulated) = 26 MHz
Propagation delay (measured) = 770 ps	Propagation delay (simulated) = 493 ps
Power per gate (measured) = 2 mW	Power per gate (simulated) = 2 mW
Speed Power Product (measured) = 1.41 pJ	Speed-Power-Product (simulated) = 0.9 pJ

Note that the simulation results are always faster than the experimental results. This can be attributed to the fact that no interconnect capacitances are included in the simulation.

4.3 CASCADE OF FSCL INVERTERS

To obtain the speed-power curve for the FSCL inverter, three different circuits were used, each consuming different amount of power. Also for each of these different circuits, fanout of three and five were fabricated to observe the fanout characteristic of the FSCL inverter. To enable us to measure the propagation delay of a single gate, a cascade of 23 inverters were used for each circuits with outputs taken from the second and the twenty-second stage as shown below. Note that one of the inverter's ground is separated from the rest to enable us to measure the switching noise of a single inverter.
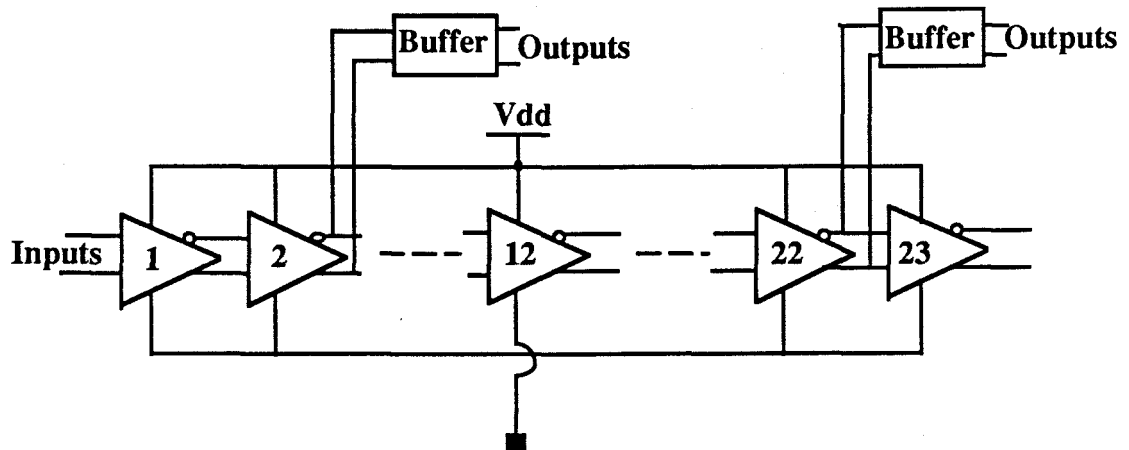

Figure 25 Test structure for the characterization of FSCL inverter

The sizes used for the circuits are indicated below:

Size #1

Vdd = 5 volts	
Bias Current, Iss1 = 0.1 mA	Bias Current, Iss2 = 0.2 mA
Size for M1-M2, $\frac{W}{L} = \frac{16\ \mu m}{2\ \mu m} = 8.5$	Size for M3-M4, $\frac{W}{L} = \frac{4\ \mu m}{2\ \mu m} = 2.0$
Size for MS4-MS5, $\frac{W}{L} = \frac{22\ \mu m}{2\ \mu m} = 11$	Size for MS2, $\frac{W}{L} = \frac{11\ \mu m}{2\ \mu m} = 5.5$

Size #2

Vdd = 5 volts	
Bias Current, Iss1 = 55µA	Bias Current, Iss2 = 0.1 mA
Size for M1-M2, $\dfrac{W}{L} = \dfrac{9\ \mu m}{2\ \mu m} = 4.5$	Size for M3-M4, $\dfrac{W}{L} = \dfrac{6\ \mu m}{4\ \mu m} = 1.5$
Size for MS4-MS5, $\dfrac{W}{L} = \dfrac{10\ \mu m}{2\ \mu m} = 5$	Size for MS2, $\dfrac{W}{L} = \dfrac{6\ \mu m}{2\ \mu m} = 3$

Size #3

Vdd = 5 volts	
Bias Current, Iss1 = 14 µA	Bias Current, Iss2 = 25µA
Size for M1-M2, $\dfrac{W}{L} = \dfrac{5\ \mu m}{4\ \mu m} = 1.25$	Size for M3-M4, $\dfrac{W}{L} = \dfrac{6\ \mu m}{14\ \mu m} = 0.43$
Size for MS4-MS5, $\dfrac{W}{L} = \dfrac{5\ \mu m}{4\ \mu m} = 1.25$	Size for MS2, $\dfrac{W}{L} = \dfrac{6\ \mu m}{8\ \mu m} = 0.75$

With the above sizes, the results from measurements and simulations are given below.

Size #	1	2	3
Delay/gate (ns) fanout 1	0.75 (0.90)*	1.25 (1.15)	3.70 (5.50)
Delay/gate (ns) fanout 3	1.25 (1.20)	2.20 (1.80)	N.A (7.00)
Delay/gate (ns) fanout 5	2.00 (1.60)	3.40 (2.05)	12.0 (10.5)
Static Power per gate (mW)	1.98 (2.00)	0.99 (1.00)	0.125 (0.125)

* Values in parenthesis indicate simulated result.

From the results above, we can obtain the power-delay curve and the fanout characteristic of our FSCL inverter.

4.3.1 Power-Delay Curve

The power-delay curve, shown on next page, allowed us to see indirectly the effect of bias current on the speed of the FSCL inverter. Besides that, the practical aspect of the curve is to help us to determine the size of the inverter needed for a required speed.
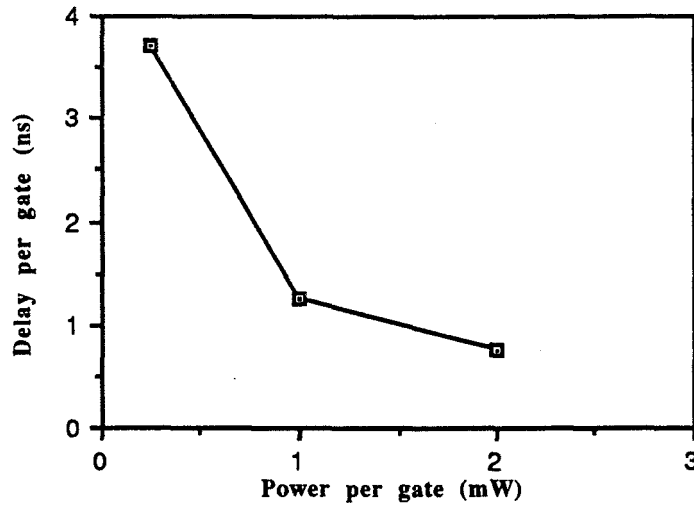
Figure 26   Power-Delay characteristic of FSCL inverter

4.3.2   Fanout Characteristic Of FSCL Inverter

To enable us to see the driving capability of our inverter, several fanouts were obtained for three bias current, figure 27.
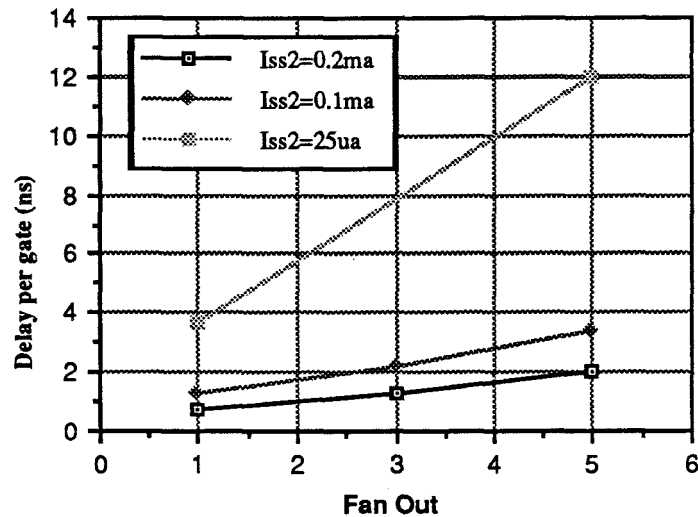

Figure 27   Fanout characteristic of FSCL inverter

Looking at the graph, the curves are rather linear hence allowing us to extrapolate our result for fanout greater than five.

5. CONCLUSION

Conventional static CMOS logic gates, which are widely used, create problems for the analog circuitry when used in mixed-mode applications. Noise and ground bounce generated during transitions of logic gates degrade the accuracy and dynamic range of the analog circuitry.

In this thesis, a new class of logic gates has been developed to overcome this problem. SCL, ESCL, and FSCL have been shown to generate two orders of magnitude less digital switching noise. Complex gates using FSCL have been developed using the series gating technique.

To test the functionality and application of this new family of gates, ring oscillators and a 4-bit ALU have been fabricated using 2 μm p-well process. The results obtained indicated the minimum propagation delay of our inverter is approximately 770 ps and the 4-bit ALU is capable of running at a speed of more than 50 MHz.

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