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John F. Wager

The drain current of InP MISFETs is often observed to decrease as a function of time after the application of a positive gate bias which involves an accumulation of electrons in the channel. Various models have been proposed for this drain current drift (DCD) phenomenon.

In this thesis, variable-temperature bias-stress measurements of InP MIS capacitors were employed in order to determine the dominant DCD mechanism from a analysis of the activation energy of the flat band voltage shift.

Two distinct activation energies at 40-50meV and 1.1-1.2eV were obtained from variable-temperature bias-stress measurements over a temperature range of 100-350K. The 40-50meV activation energy dominants the flat band shift at low temperatures and is consistant with thermally

activated tunneling of electrons from the InP conduction band into a discrete trap in the native oxide. The 1.1-1.2 eV activation energy is that predicted for phosphorous vacancy nearest-neighbour hopping (PVNNH) in which the channel electrons are captured by shallow acceptors which are created by the hopping of an In atom into a phosphorous vacancy. The estimated fraction of the flat band shift in these particular samples at room temperature due to PVNNH is approximately 20%.

The mechanism of PVNNH has also been investigated through a computer simulation of the flat band shift versus time. The simulation is based on an analysis of the kinetics of the PVNNH defect reaction sequence in which the electron concentration in the channel is related to the applied bais by a solution of the Poisson equation. The simulation demonstrates quantitatively that the temperature dependence of the flat band shift is associated with PVNNH for temperatures above room temperature. A slight deviation from the experimental data at high temperature is apparent in the simulation and several reasons for this small deviation are provided.

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Redacted for Privacy

Head of the Department of Electrical & Computer Engineering

Redacted for Privacy

Dean of Graduate School

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Typed by Min Tzuan Juang

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1. INTRODUCTION

Compound semiconductors such as GaAs and InP have attracted considerable attention for high speed applications because of their high electron mobility and saturation drift velocity. GaAs metal-semiconductor field effect transistor (MESFET) devices have demonstrated gate delays of 30ps [1,2]. An alternative high speed device is a metal-insulator-semiconductor field effect transistor (MISFET). In an enhancement-mode n-channel MISFET device, the Fermi level must be moved from a quiescent zero gate voltage position in which the device is off to a position near the conduction band edge in which the device is turned on. In the case of GaAs, due to the large interface state density, the Fermi level is virtually pinned at approximately 0.8V from the conduction band edge, which makes GaAs not suitable for the MISFET technology.

The interface state density reported for InP [3,4] is in the range of $10^{11} cm^{-2} eV^{-1}$. InP MISFETs have been successfully fabricated with chemical vapor deposited (CVD) SiO_2 gate dielectrics [5,6]. This has stimulated an interest in InP MISFETs for high frequency and/or high power applications.

However, attempts to further develop this technology

have been somewhat disappointing. Two major problems remain to be solved: (1) The instability of the drain current with time after the application of a gate bias and (2) variations in the channel mobility with processing. These problems are strongly affected by the chemical and physical structure of the semiconductor/insulator interface.

Electrical interface instabilities are manifest as hysteresis in capacitance-voltage (C-V) curves, hysteresis in low frequency current-voltage (I-V) measurements and drain current drift (DCD) in MISFETs. Gated Hall measurements [7] showed conclusively that the decrease in drain current is caused by a loss of electrons from the channel as was postulated by various researchers. Previous work concentrated on explaining the loss of electrons from the channel as associated with the trapping of these electrons in the oxide or deposited insulator, but were unable to satisfactorily account for both the time and temperature dependence of the drift. Van Vechten and Wager[8] have proposed that phosphorous vacancies near the interface may cause DCD. The proposed P vacancy nearest-neighbour hopping (PVNNH) model requires an activation energy of approximately 1.2eV, which is relatively large compared to a few tens of meV that have been reported [3,4]. Some recent work [9] supported this model by noting a reduction in DCD when a P overpressure was employed

during deposition of the gate dielectric.

In this thesis, the C-V technique was used to measure InP MIS capacitors to determine the relationship between the flat-band voltage shift as a function of time under bias. These bias stress measurements were obtained over a wide temperature range in order to investigate the possibility of the PVNNH induced drift.

Various models are discussed in Chapter 2 that have been proposed to explain DCD in InP MISFETs with special emphasis on the PVNNH mechanism.

The experimental techniques employed in this work are described in Chapter 3. Several important considerations in using the C-V measurement technique to determine the flat-band voltage shift are discussed.

In Chapter 4, the experimental results are presented. Sample curves are shown to illustrate the interpretation of the data and the method of extracting the activation energy of the shift from C-V curves in the temperature range of interest.

In Chapter 5, a computer simulation of the experimental data is described which is derived from the PVNNH model. Results of the simulation and the parameter estimation issues inherent in the simulation are also discussed in this chapter.

2. DRAIN CURRENT DRIFT IN InP MISFETS

2.1 Background

InP MISFETs often show drift in the measured drain voltage as a function of time after the application of an accumulating gate bias. Measurements made [4,10,11] indicate the following trends: (1) A linear relationship can be observed up to 10^4s if the output current is plotted vs the log time. (2) At a larger gate voltage, the decay is usually greater. (3) The amount of decay decreases as the temperature is lowered. (4) The current tends to saturate after 10^5s. (5) There is an incubation period of approximately 1sec before the onset of the drift.

Excellent reviews of the various models proposed to explain InP MISFET DCD have been provided by Wager et al. [12] and Zeisse et al. [13]. These models can be divided into two catagories: (1) Electron tunneling into the dielectric. (2) Vacancy motion in bulk InP.

The logarithmic time dependence of the drift immediately suggests the tunneling theory of Heiman and Warfield [14] who considered the application of Shockley-Read-Hall statistics to traps embedded in a dielectric adjacent to a semiconductor. Van Staa et al. [15] employed this model to interpret their constant-capacitance deep level transient spectroscopy (CCDLTS) measurements. The

traps are assumed to be distributed both spatially and energetically within the InP bandgap. This model implies a temperature independent electron capture, which is in conflict with the drift data reported.

Okamura and Kobayashi [3] proposed a model in which the DCD was due to thermally activated tunneling of electrons from the InP conduction band into a discrete trap in the native oxide which they estimated was 38meV above the Fermi level. A second discrete trap level in the insulator (Al_2O_3) within the InP bandgap was assumed to explain some residual drift that they observed in their devices even at low temperatures. This is perhaps the most popular DCD model.

Lile and Taylor [4] employed this model to analyze their InP devices and estimated an activation energy of 16meV, in good agreement with that obtained by Okamura and Kobayashi. The effect of trapped space charge on the band diagram has been neglected in this model. As the traps fill, the surface potential decreases because of the shielding associated with electrons captured by the traps. In the limit that the trapped charge equals the initial channel density per cm^2, all of the field lines which originate at the gate terminate on the trapped charge, the flatband condition is achieved, and the channel disappears. This model also predicts that the change in the drain current is smaller at higher gate voltage, but

it is found experimentally that more DCD is observed at larger gate bias [11].

Physical studies of the insulator-semiconductor interface of deposited SiO_2 on InP have been performed by Wager et al. [16,17] using x-ray photoemission spectroscopy (XPS) and electron loss spectroscopy (ELS). These studies have shown that the first 20-40Å of the native oxide on InP is composed primarily of $InPO_4$. The subsequent oxide layer is predominately In_2O_3 followed by SiO_2. Furthermore, it was estimated that the In_2O_3 conduction band edge was a few tenths of an eV higher than the InP conduction band edge. Based on this physical evidence, Goodnick et al. [7] proposed that electrons from the InP could tunnel through the $InPO_4$, to the In_2O_3 and remain trapped there. The temperature dependence arises from the activation of electrons which surmount the conduction band discontinuity between the InP and the In_2O_3. This model yields very good agreement with the experimental data, it accurately describes the temperature dependence of the drift and it correctly shows the incubation period of constant current. In fitting the experimental data, however, an interfacial oxide thickness of 44.2Å was required which is $\sim$2-5 times larger than what is typically found with a processed device. An additional problem with this model is the fact that re-emission of electrons from the In_2O_3 conduction band

should occur very rapidly even at low temperature when the device is biased out of accumulation. Thus, it is necessary that the electrons which are transported into the In_2O_3 by thermally assisted tunneling are then captured by a trap state within the In_2O_3 bandgap.

Meiners [18] has recently proposed an analytical model which shows that DCD may be caused by trapping of accumulated electrons by bulk traps in the semiconductor. The temperature dependence of this DCD is explained in terms of electron capture via multiphonon emission.

2.2 Flat-Band Voltage Shift in InP MIS Capacitors

Prasad [11] investigated the trapping of electrons in InP MIS capacitors in terms of the flat-band voltage shift ΔV_{fb} with time after a positive bias is applied. A linear relationship was observed between $\sqrt{\Delta V_{fb}}$ and log(t). This relationship was further verified by replotting the data obtained from Okamura and Kobayashi [3] and Lile and Taylor [4].

A formulation of the electron tunneling model derived by Prasad is as follows. Consider an InP MIS capacitor with an n-type substrate with a positive bias as shown in Fig.2.1. The surface is accumulated and electrons tunnel from the substrate into oxide traps. The applied bias bends the bands downwards, which brings the mono-energetic trap level close to the interface which causes enhanced

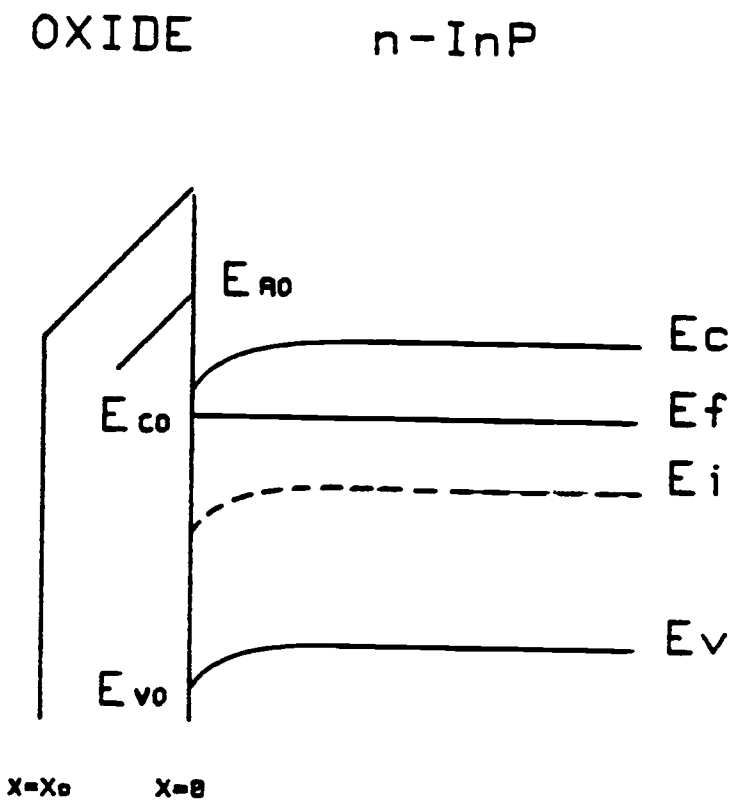


Fig. 2.1 An n-type InP MIS capacitor with oxide traps under positive bias [11].

tunneling at higher voltages. If N_{TA} is the number of available traps/cm^2 and N_{tr} is the number of traps that are filled, then

$$dN_{tr}/dt=S(x)v[n_s(N_{TA}-N_{tr})-n_1N_{tr}] \quad (2.1)$$

where S(x) is the capture cross-section of the oxide trap located at a distance x into the oxide, v is the thermal velocity of the electrons, n_s is the electron concentration at the surface of the semiconductor and n_1 is the equilibrium electron concentration if the Fermi-level were at the trap level.

A solution to equation (2.1) would give N_{tr} as a funccction of x and t. Since the centroid of the charge resides close to the interface, the shift in the C-V curve is given by

$$\Delta V_{fb}=qNe/Co \quad (2.2)$$

where

$$Ne=\int_o^{X_o} n_{tr}(x,t)dt \quad (2.3)$$

Co and Xo are the capacitance and thickness of the oxide, respectively.

In terms of trap parameters, equation (2.2) can be expressed as

$$\Delta V_{fb}=\frac{qN_{TA}}{Co}\int_o^{X_o} g(E)f(E)dx \quad (2.4)$$

where

$$g(E)=1-\exp[-t/\tau n\exp(ax)f(E)] \quad (2.5)$$

and

$$f(E)=[1+\exp(E_{AO}-Ef-qxEox)/kT] \qquad (2.6)$$

f(E) is the Fermi-function for electrons, g(E) can be thought of as a tunneling probability function, and τ_n and Eox represent the time-constant of the trap and oxide field respectively. The field at the semiconductor surface is reduced due to the trapped charge and this in turn, decreases n_s. The trap energy $E_{AO}-E_{CO}$ was found to range between 40 and 70 meV and the capture cross-section for the trap was found to be temperature dependent with an activation energy of 0.7eV and a high temperature cross-section of $10^{-15}cm^2$ in order to fit the experimental results.

2.3 P Vacancy Nearest-Neighbour Hopping

It has been argued [19] that in III-V (but not in II-VI) compound semiconductors the energy of antisite defect formation is so low that the dominant mode of vacancy diffusion is via nearest-neighbour hopping rather than hopping to second nearest-neighbour sites on the same sublattice. At least for the case of anion vacancies, strong experimental support for this diffusion mechanism [20,21] comes from the observation that Zn enhances by several orders of magnitude the rate of interdiffusion of both host anions and host cations in III-V superlattice structures.

Van Vechten and Wager [8] considered some of the

consequences of Vb nearest-neighbour hopping for III-V devices. Consider an InP MISFET, which has P vacancies in its gate region which were induced during device processing. Due to the diffusion of Vp's during high temperature processing, the material would initially contain Vp derived defects corresponding to each of the 11 stages of nearest-neighbour hopping as shown in Fig.2.2. The net charge states of these in intrinsic material alternates between +1 and -3. It is enough to consider one pair of states, e.g., Vp^{+} at step 1 (or 11) and $V_{IN}^{-}In_{P}^{-2}$ at step 2 (or 10). These are connected by the reaction

$$Vp^{+}+4e^{-} \Longleftrightarrow V_{IN}^{-}In_{P}^{-2}. \qquad (2.7)$$

These equilibrium concentrations are related by the Law of Mass Action as

$$[V_{IN}^{-}In_{P}^{-2}]/[Vp^{+}] \propto [e]^{4} \qquad (2.8)$$

Typically InP MISFETs are enhancement-mode devices, so they are depleted of electrons in the channel prior to the application of a gate bias. Thus the Fermi-level, Ef, and the electron concentration in the channel, [e], are relatively low and (2.7) is driven to the left so there are many more Vp^{+} than $V_{IN}^{-}In_{P}^{-2}$. When the InP MISFET is turned "on" it is biased to accumulation where $[e] \approx 10^{17} cm^{-3}$ and Ef approaches the conduction band edge. This forces the deionization of Vp^{+} to Vp^{o} and drives (2.7) to the right.

The coulombic cross-section for capture of one of the

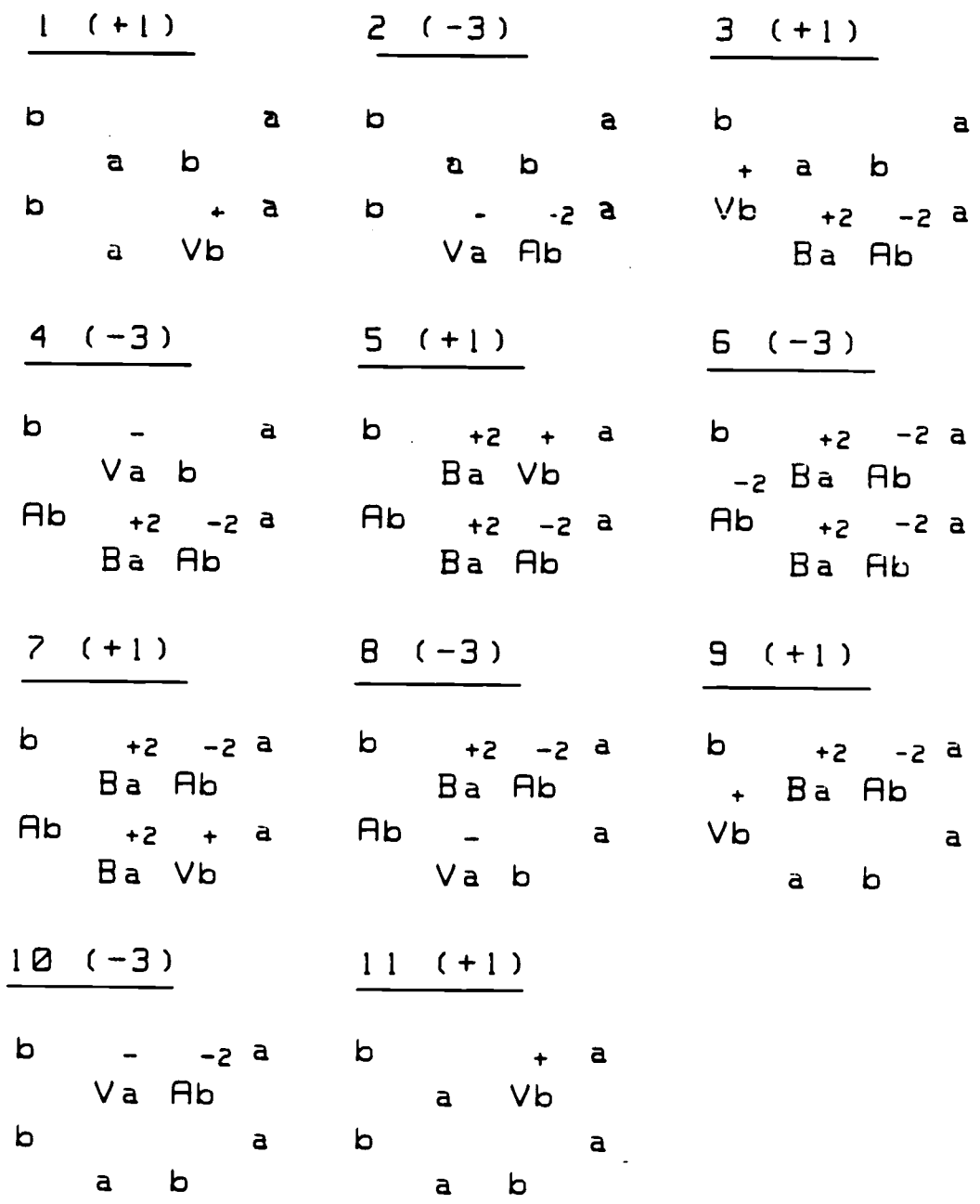


Fig. 2.2 Single anion (P) vacancy Vb nearest neighbour hopping.

electrons , e^- by Vp^+ is of order $10^{-12}cm^2$ and would thus require only about 1ps after [e] is driven to $10^{17}cm^{-3}$. Then the time for

$$Vp^o \rightarrow V_{In}{}^o In_p{}^o \qquad (2.9)$$

is given by

$$1/\tau = \nu_o \exp(\Delta Sm/k) \exp(-\Delta Hm/kT) \qquad (2.10)$$

where ν_o, ΔSm, and ΔHm are the attempt frequency, activation entropy , and activation enthalpy of this hop. The estimated values for ν_o, ΔHm and $\Delta Sm/k$ are $6.1x10^{12}s^{-1}$, 1.2eV and 17.5, respectively, which then yields τ=0.5s at room temperature. After the vacancy has hopped , the reaction $(V_{IN}In_P)^o+e^- \rightarrow (V_{IN}In_P)^-$ proceeds with a cross-section roughly equal to its geometrical cross-section, $\sigma_o=10^{-15}cm^2$, in a time of order 1ns. The capture of the second e^-, i.e., $(V_{IN}In_P)^-+e^- \rightarrow (V_{IN}In_P)^{-2}$, using the same expression as the problem of an α-particle tunneling through the coulombic barrier of a nucleus to become bounded in the attractive potential in its center, $\sigma(-1 \rightarrow -2)=2.8x10^{-18}cm$, which would imply a delay time of order 3μs. With the same assumptions, one would estimate $\sigma(-2 \rightarrow -3)=7.6x10^{21}cm^2$, a time of order 8ms is required.

After the InP MISFET is biased into strong accumulation, there is a delay of order 1sec [4] at room temperature before the source drain current begins to decay. This is in accord with the estimated incubation time required for reaction (2.9) at room temperature and

the assumption that the electron trapping responsible for the decay cannot occur until after the Vp has hopped to the In lattice. As mentioned by Goodnick et al. [16], conventional models of charge trapping cannot account for this time delay.

The estimated activation energy, ΔHm, for PVNNH is 1.2eV. An activation barrier this large implies a large reduction in the anion vacancy hopping with decreasing temperature. It is possible that the current decay observed at lower temperature is due entirely to interface traps while Vp hopping begins to contribute at room temperature.

This model predicts that minimizing [Vp] is an obvious solution to the DCD problem. Pande and Gutierrez [9] have deposited a phosphorous rich oxide onto p-type InP with an indirect oxygen plasma in the presence of a phosphorous vapor. Following deposition of this phosphorous-rich oxide, SiO_2 was deposited without removing the sample from the reactor. After annealing for 30 min at 300 C, the 1MHz C-V characteristics were free of hysteresis when swept between 4V. A less than 3% change in the channel current of an inversion-mode MISFET was observed after $2x10^4$s. This is the best InP drift result reported to date.

3. EXPERIMENTAL TECHNIQUE

3.1 InP MIS Capacitors

Undoped (n-type, $\approx 4 \times 10^{15}/cm^3$), (100) InP wafers were used in this study. The InP surface preparation consisted of degreasing boils in tetrachloroethylene, followed by rinses in methanol/acetone and methanol. The InP surface was then prepared in one of two ways:

(A) Room temperature KOH/methanol. The sample was treated for 1 min in a solution of KOH in methanol (2.5g of KOH in 200ml of methanol) which was maintained at room temperature.

(B) "Hot" KOH/methanol. the sample was treated for 1 min in the KOH/methanol solution heated at 70 C.

The samples were subsequently rinsed in methanol, isopropyl alcohol, and blown dry with nitrogen. A layer of approximately 850 Å of plasma-enhanced chemical vapor deposited (PECVD) SiO_2 was then deposited at 300 C.

The characteristics of these devices were reported by O. L. Krivanek et al. [22], using cross sectional high-resolution electron microscopy (HREM), x-ray photoemission spectroscopy (XPS) depth profiling, and C-V and G-V methods. The ellipsometric thickness of the native oxides reported for sample A and B are 15Å and 9Å, respectively. C-V measurements indicated that sample B has higher interface state density.

3.2 C-V measurements

Following Prasad's [11] approach, characterization of the trapping of electrons in InP MIS capacitors is accomplished by measuring the flat-band voltage shift of the C-V curves as a function of time at different temperatures under constant positive bias.

The C-V analysis was performed with an automated system based on Hewlett-Packard equipment consisting of a model 9845 desktop computer in conjunction with a 4275A digital LCR meter, a 4140B picoammeter/DC voltage source, and a 3455A digital voltmeter. The temperature-controlled probe system used in this research was from an MMR technologies Inc. low temperature microprobe system, model LTMP-3. Cooling of the sample is achieved by flowing high pressure (1800psig) pure nitrogen through a Joule-Thomson refrigerator, and resistance heating is used in combination with the refrigerator to achieve temperature balance. Desired temperature is programmed with a HP-85 desktop calculator via a microprocessor controller, model K-20, also from MMR, which dynamically controls the current that flows through the heating resistor. Electrical contact to the device is achieved via electrical feedthroughs to three micro probes housed in a vacuum chamber.

Indium is melted onto the backside of the capacitor in a way such that a small amount protrudes from the

underside so that back contact can be made. The measurement is initiated by shorting the sample and heating to 375 K for 10 min, in order to reproducibly initialize the trap occupancy. The temperature is then lowered to 350 C for 10 min to achieve thermal equilibrium. An initial C-V curve, which is considered to be stress-bias free, is then obtained by sweeping at a rate of 100mV/sec from +3V to -3V. Upon completion of the sweep, a +4V bias is applied to the gate of the capacitor for the desired amount of stress time, and another C-V curve is obtained. The bias stress time is defined as total amount of bias time applied to the sample prior to obtaining the C-V curve. The same procedure is repeated for progressively increasing stress-bias times. For example, if the desired stress-bias time is determined to be 500sec, 1000sec, 2000sec and 4000sec, the bias time between successive sweeps of the C-V curves is 500sec, 500sec, 1000sec and 2000sec, respectively. An example of the measured C-V curves is shown in Fig.3.1, which illustrates that the C-V curve shifts to the right under positive bias.

After all the desired C-V scans at a given temperature are obtained, the sample is shorted and the temperature is again raised to 375 K for one hour and the value of the capacitance at zero bias returns almost completely to its initial value. The temperature is then

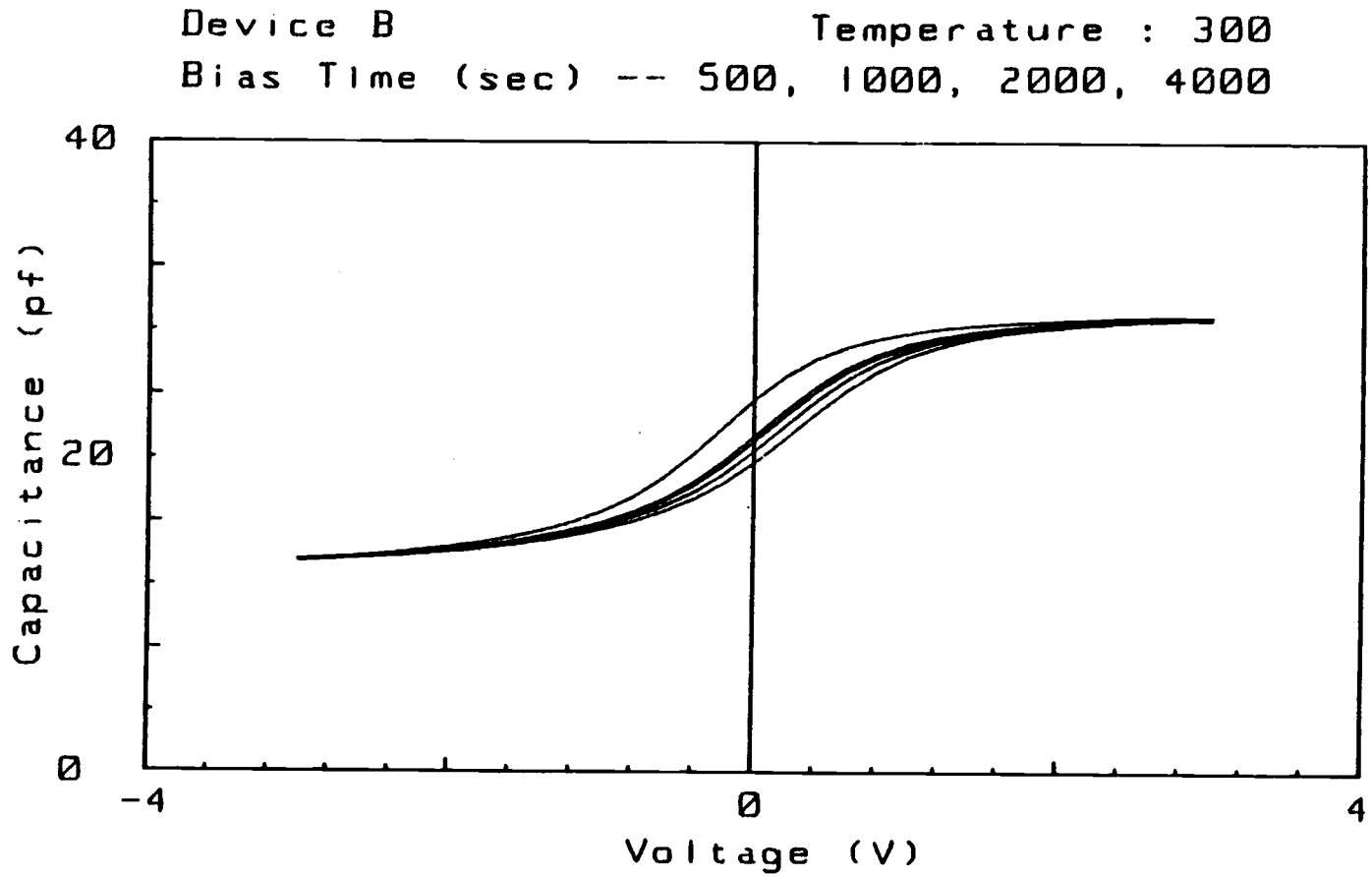


Fig. 3.1 Example of C-V curves measured under 4V positive bias-stress.

lowered to 325 K, and another positive-bias C-V measurement is repeated. This procedure is continued with 25 K intervals until a temperature of 100 K is reached.

4. EXPERIMENTAL RESULTS

4.1 Activation Energy Extraction

C-V bias-stress curves obtained under a 4V positive bias are shown in Figs. 4.1-4.4 for 4 of the 11 temperatures at which data were taken. The temperature dependence of the flat-band voltage shift is very obvious.

The amount of flat-band voltage shift (ΔV_{fb}) as a function of bias time is determined from the difference in the flat-band voltage (Vfb) after certain bias time compared to Vfb at a bias time of zero . As indicated in Fig.4.5, $\Delta V1$, $\Delta V2$, $\Delta V3$ and $\Delta V4$ correspond to Vfb shifts at bias-stress times of 500sec, 1000sec, 2000sec and 4000sec, respectively.

A linear relationship is obtained if $\sqrt{\Delta V_{fb}}$ is plotted vs log t as shown in Fig.4.6 and 4.7. Complete sets of data are listed in Table 4.1.

Activation energies associated with the mechanisms of electron trapping are determined from the slope of an Arrhenius plot; log(1/t) vs 1000/T, where T is the temperature in K, t is the bias time required to achieve a predetermined amount of shift in Vfb, e.g . 0.4V, at different temperatures. The Arrhenius curve was obtained at a flat band voltage shift 0.4V and the bias time at each temperature was interpolated or extrapolated from the experimentally observed linear relationship of $\sqrt{\Delta V_{fb}}$ vs

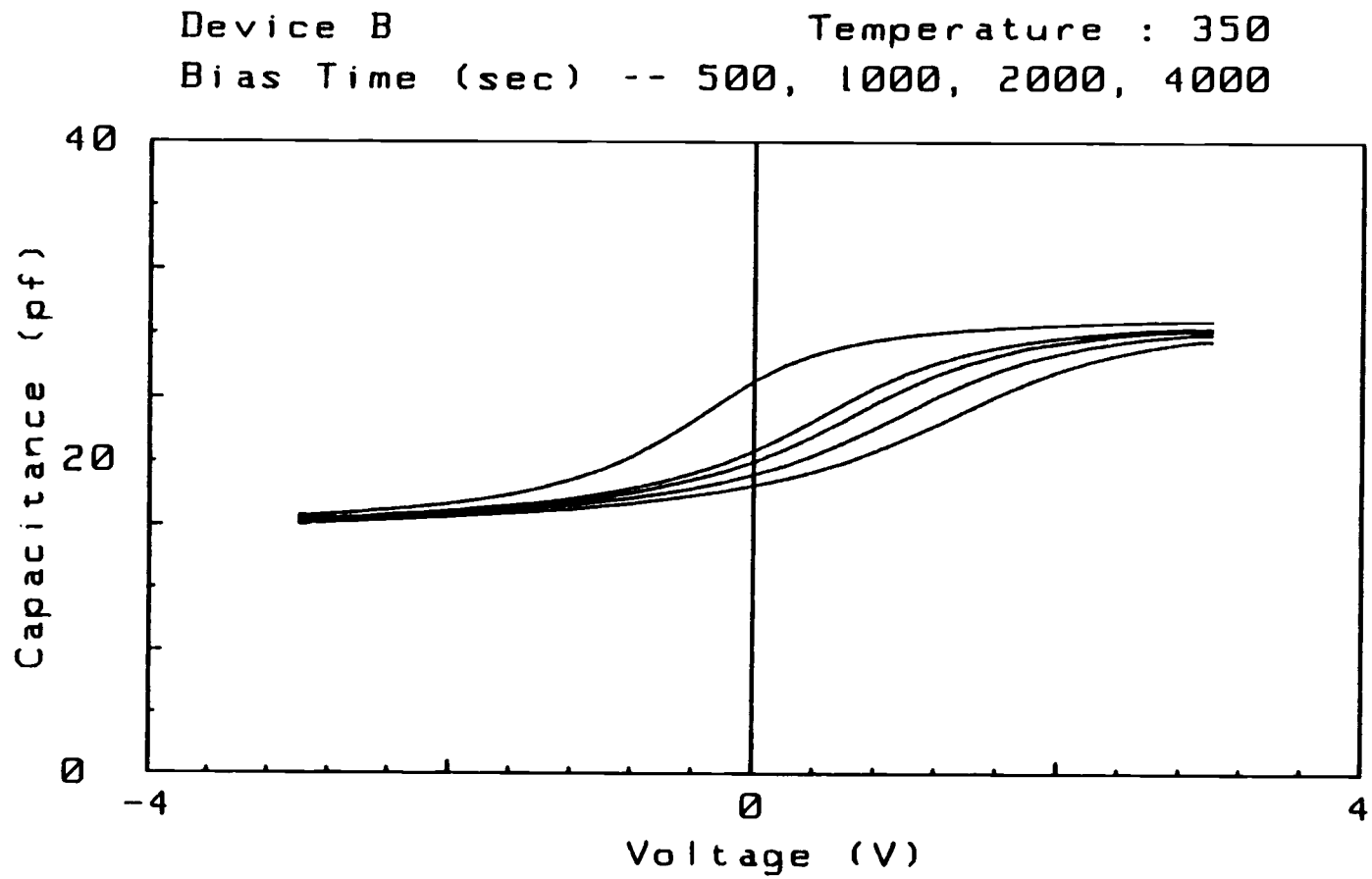


Fig. 4.1 Shift of C-V curves of device B under 4V positive bias-stress at 350 K.

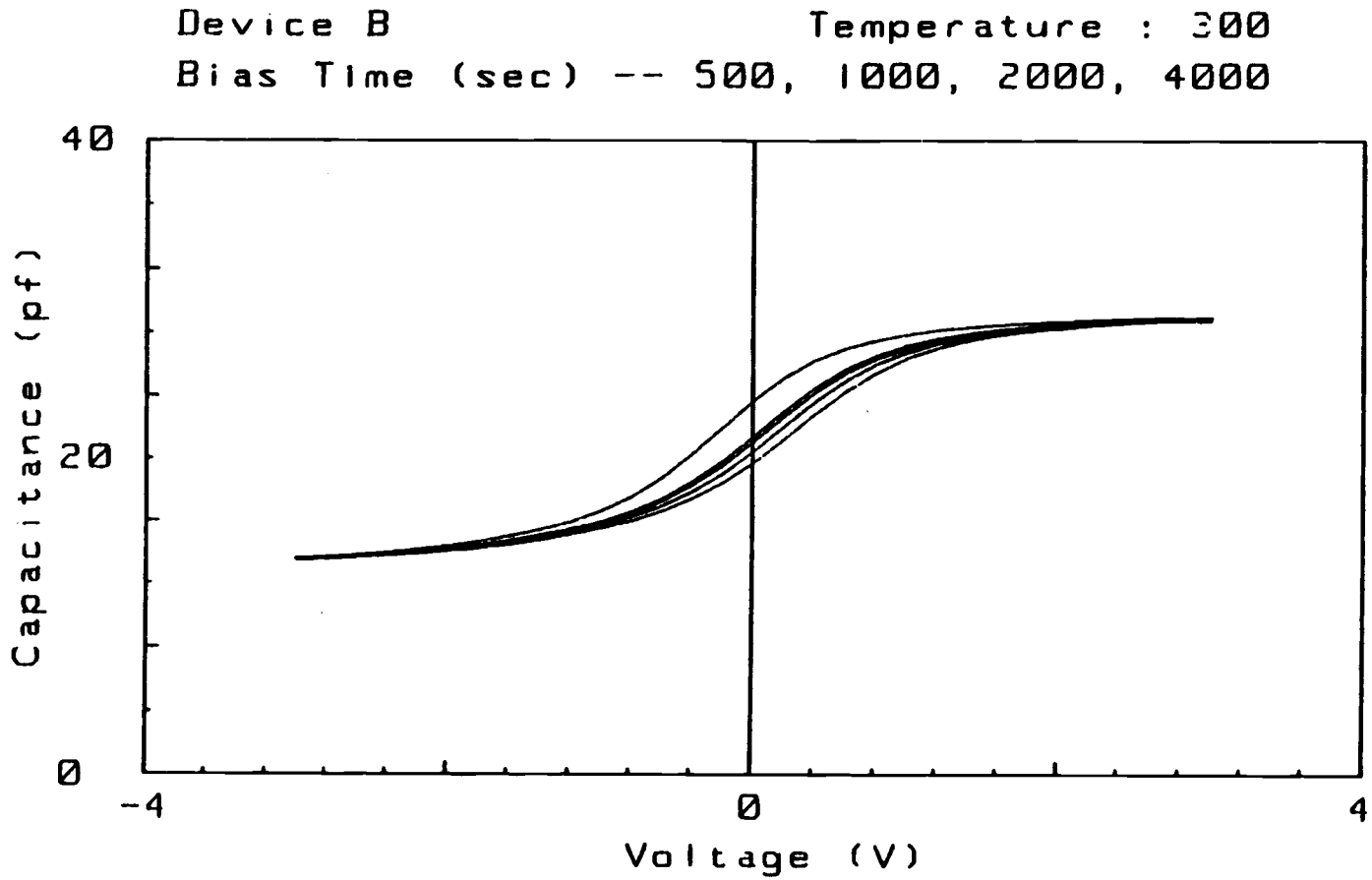


Fig. 4.2 Shift of C-V curves of device B under 4V positive bias-stress at 300 K.

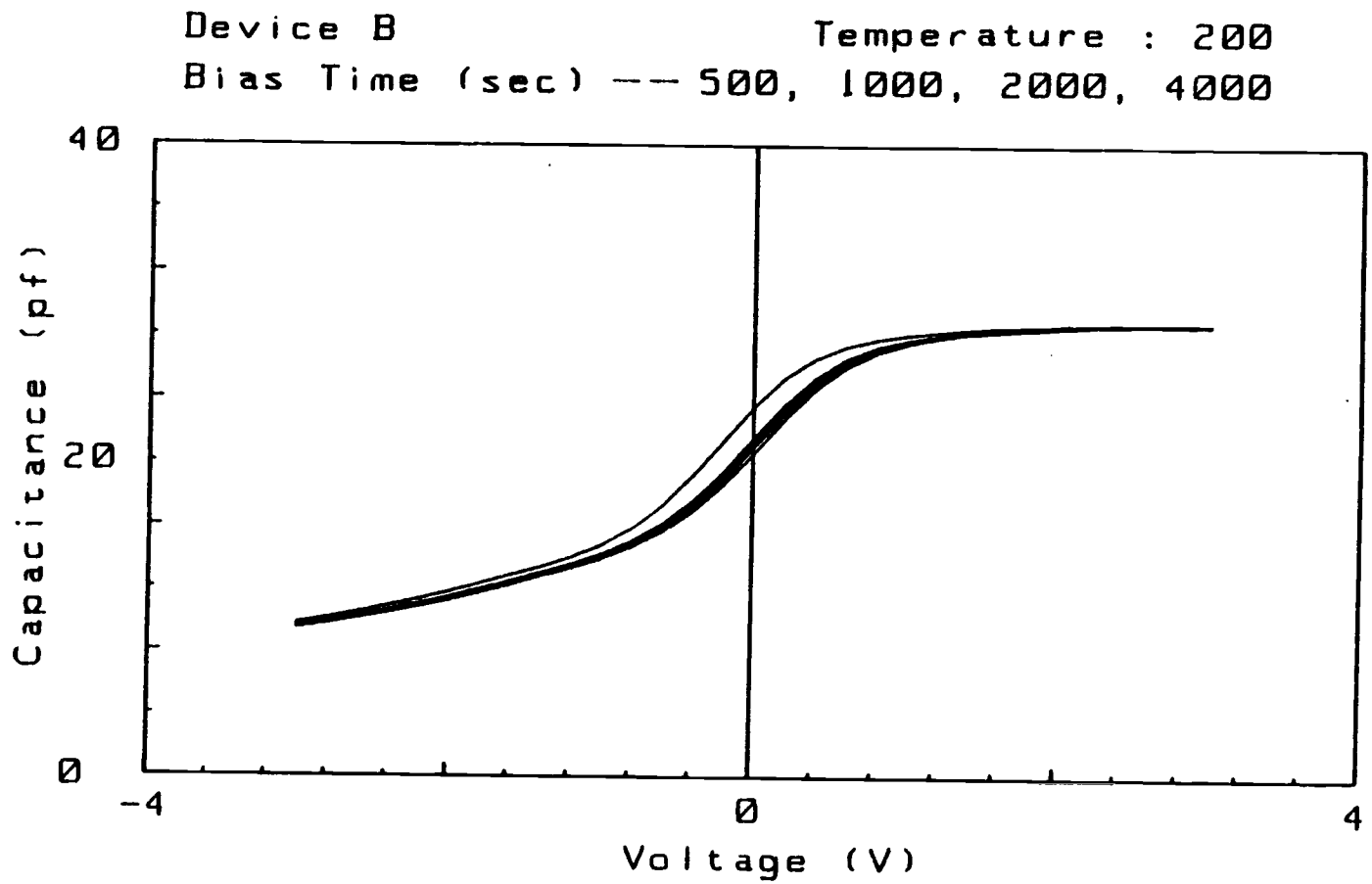


Fig. 4.3 Shift of C-V curves of device B under 4V positive bias-stress at 200 K.

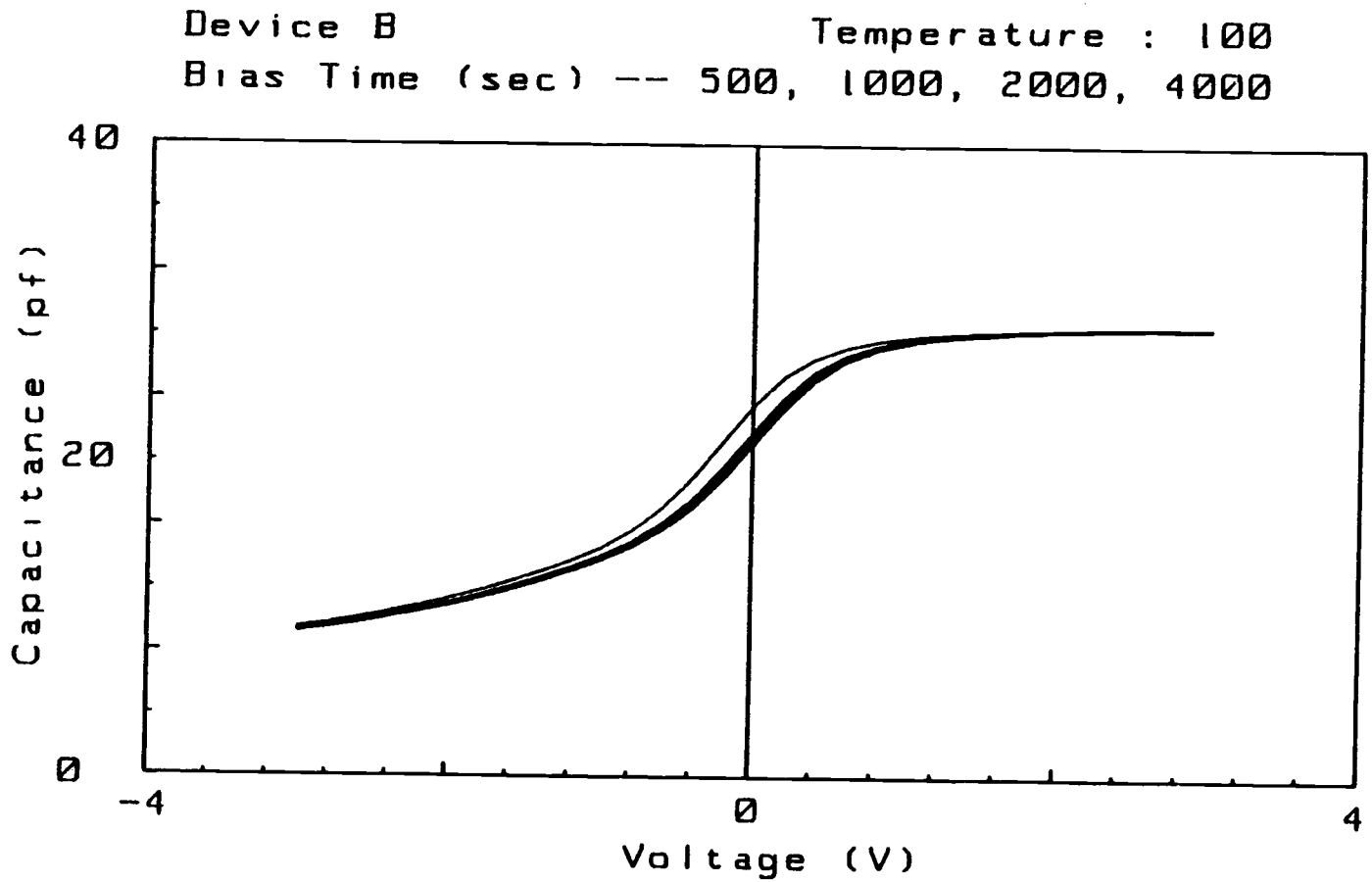


Fig. 4.4 Shift of C-V curves of device B under 4V positive bias-stress at 100K.

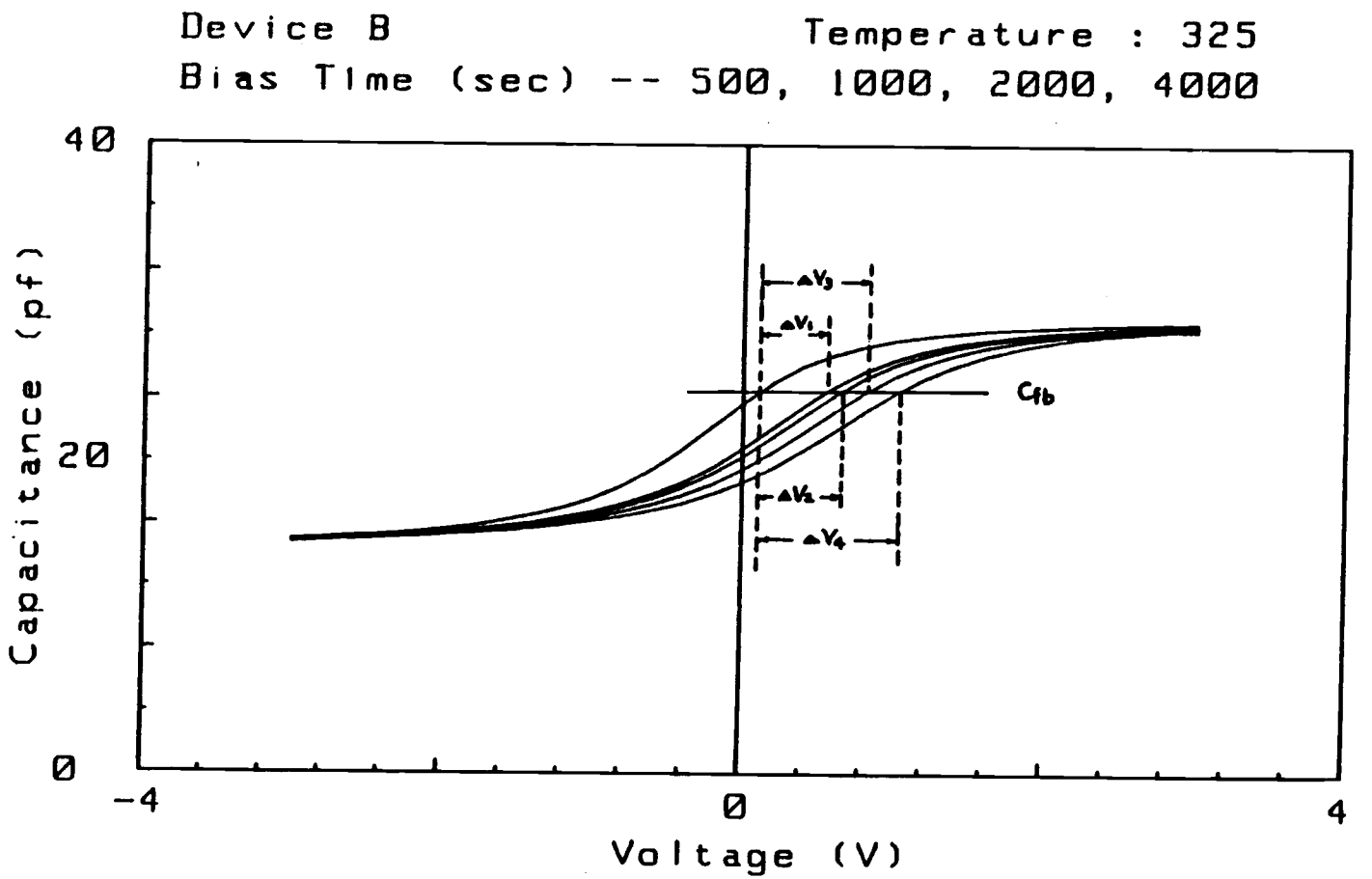


Fig. 4.5 Flat-band voltage shift extraction from the measured C-V curves.

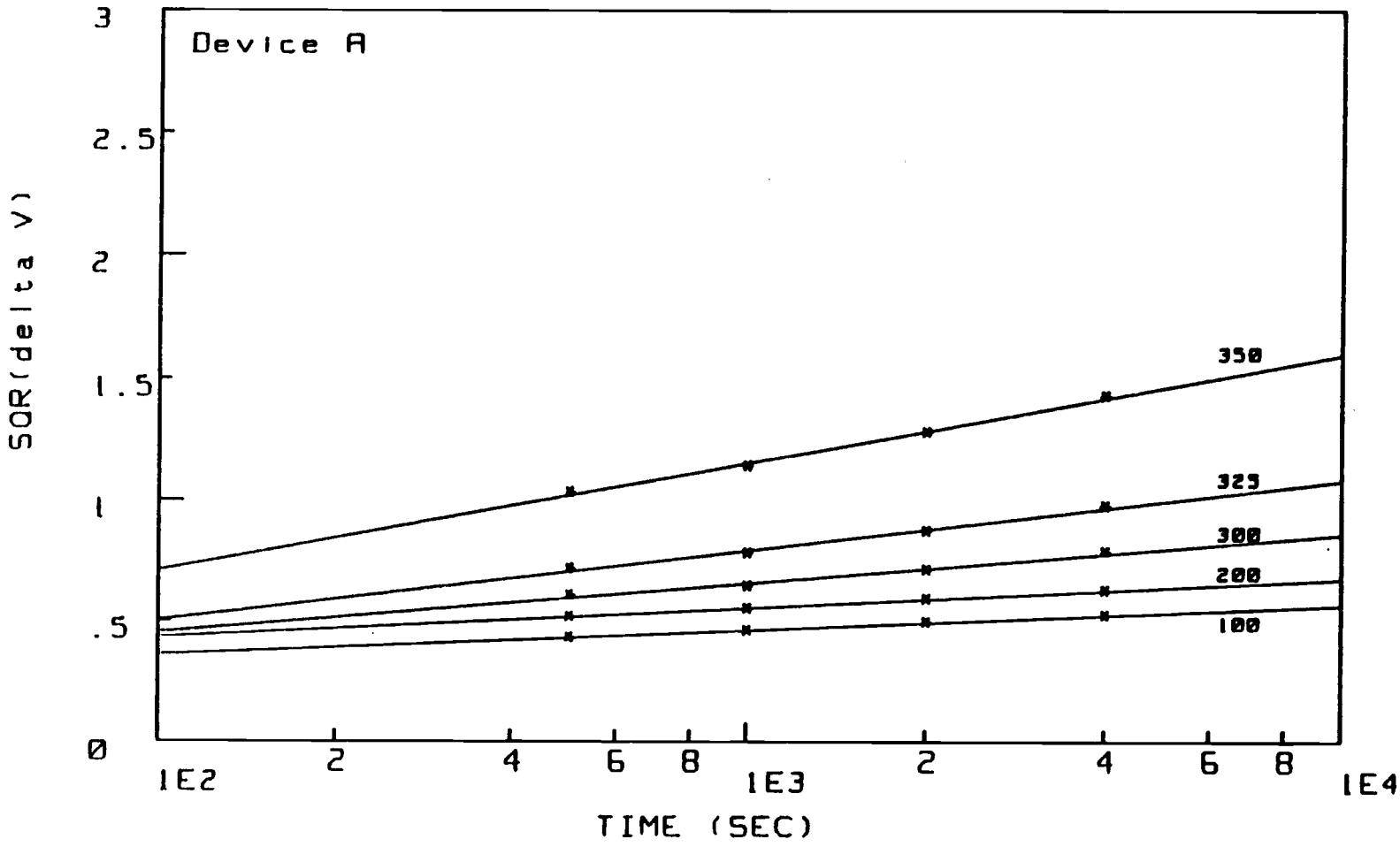


Fig. 4.6 Square root of ΔVfb vs log t of device A at five different temperatures.

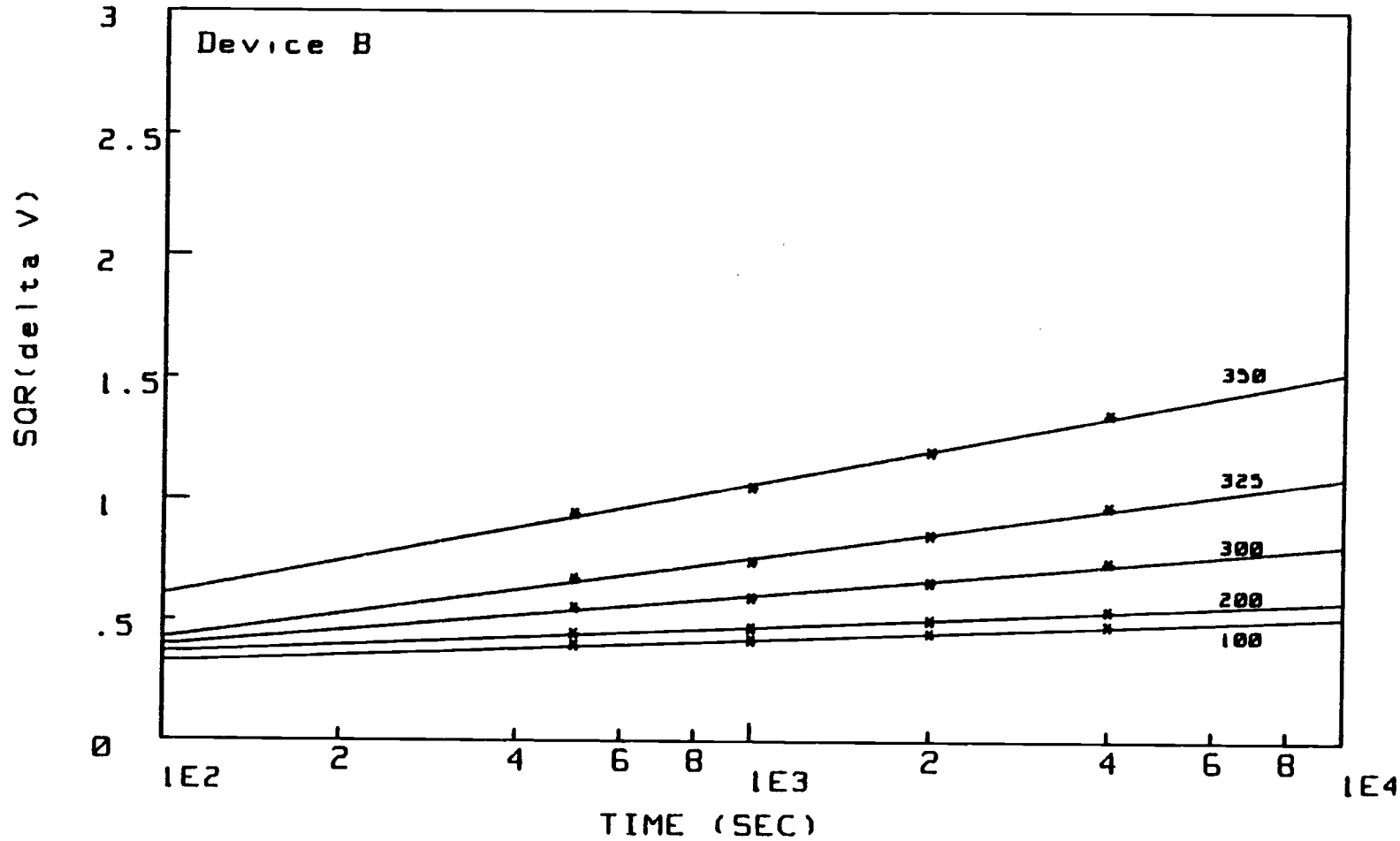


Fig. 4.7 Square root of ΔVfb vs log t of device B at five different temperatures.

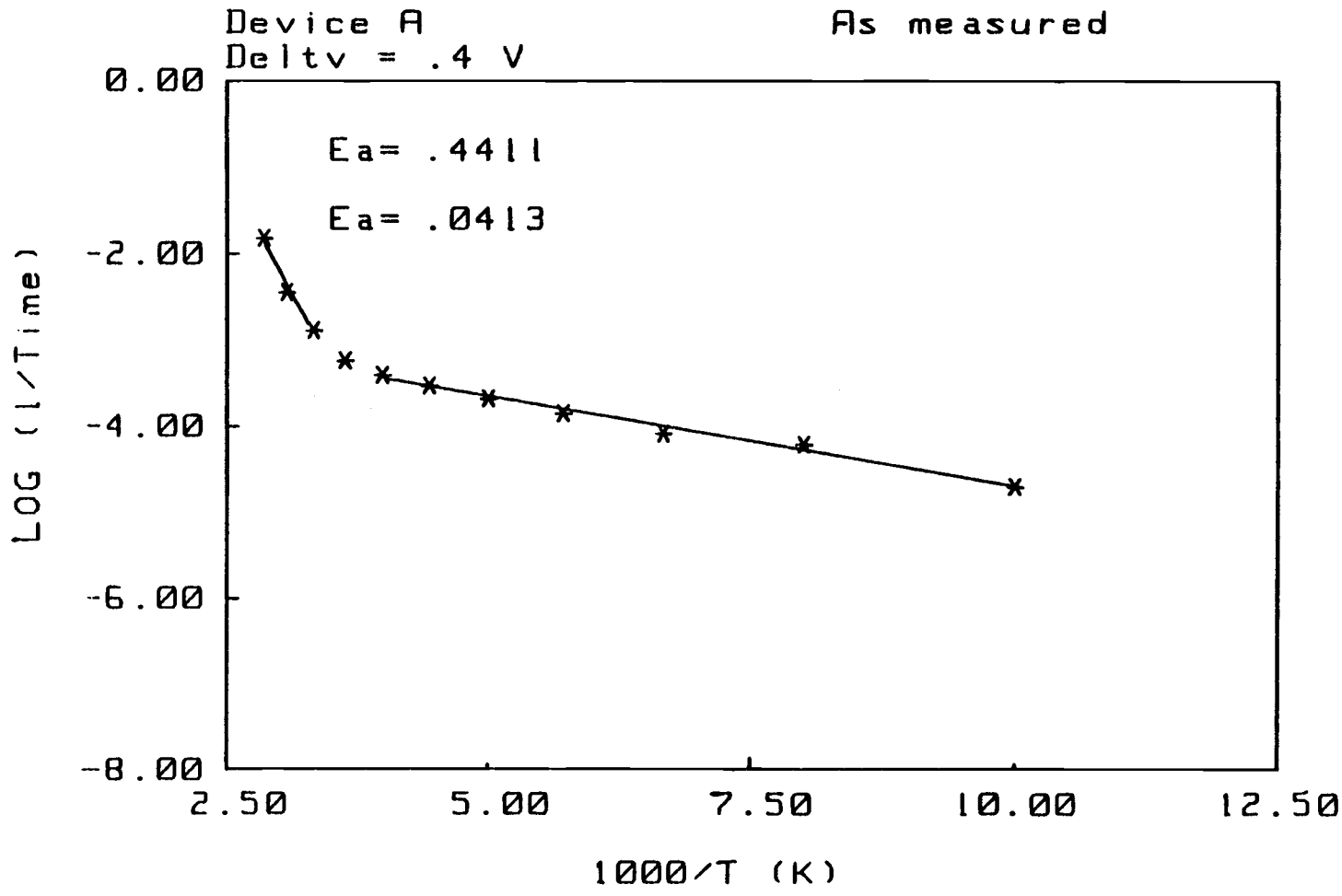
		Sample A		Sample B	
T K	tsec	ΔV	√ΔV	ΔV	√ΔV
350	500	1.0605	1.0289	.8792	.9377
	1000	1.2971	1.1389	1.0969	1.0473
	2000	1.6378	1.2798	1.4255	1.1939
	4000	2.0401	1.4283	1.8150	1.3472
325	500	.5101	.7142	.4481	.6694
	1000	.6036	.7769	.5487	.7407
	2000	.7555	.8692	.7216	.8495
	4000	.9481	.9737	.9353	.9671
300	500	.3637	.6031	.3019	.5495
	1000	.4107	.6409	.3482	.5900
	2000	.5024	.7088	.4278	.6541
	4000	.6143	.7838	.5426	.7366
275	500	.3105	.5573	.2486	.4986
	1000	.3439	.5864	.2832	.5322
	2000	.4082	.6389	.3365	.5800
	4000	.4761	.6900	.3977	.6307
250	500	.2924	.5407	.2281	.4776
	1000	.3305	.5749	.2636	.5134
	2000	.3810	.6172	.3112	.5579
	4000	.4340	.6588	.3618	.6015
225	500	.2838	.5327	.2026	.4501
	1000	.3178	.5638	.2395	.4894
	2000	.3601	.6001	.2743	.5237
	4000	.4146	.6439	.3218	.5673
200	500	.2655	.5153	.1955	.4422
	1000	.3003	.5480	.2175	.4664
	2000	.3439	.5865	.2495	.4995
	4000	.3879	.6228	.2893	.5739
175	500	.2523	.5023	.1850	.4301
	1000	.2867	.5355	.2117	.4601
	2000	.3247	.5698	.2422	.4922
	4000	.3644	.6037	.2804	.5296
150	500	.2305	.4801	.1788	.4228
	1000	.2621	.5120	.2053	.4530
	2000	.2983	.5461	.2336	.4833
	4000	.3351	.5788	.2704	.5200
125	500	.2222	.4714	.1601	.4001
	1000	.2526	.5026	.1847	.4298
	2000	.2863	.5351	.2114	.4598
	4000	.3216	.5671	.2350	.4848
100	500	.1835	.4284	.1539	.3923
	1000	.2089	.4571	.1720	.4147
	2000	.2408	.4908	.1978	.4447
	4000	.2696	.5193	.2267	.4761

Table 4.1 Measured amount of ΔVfb as a function of bias-stress time and temperature of both device A and B.

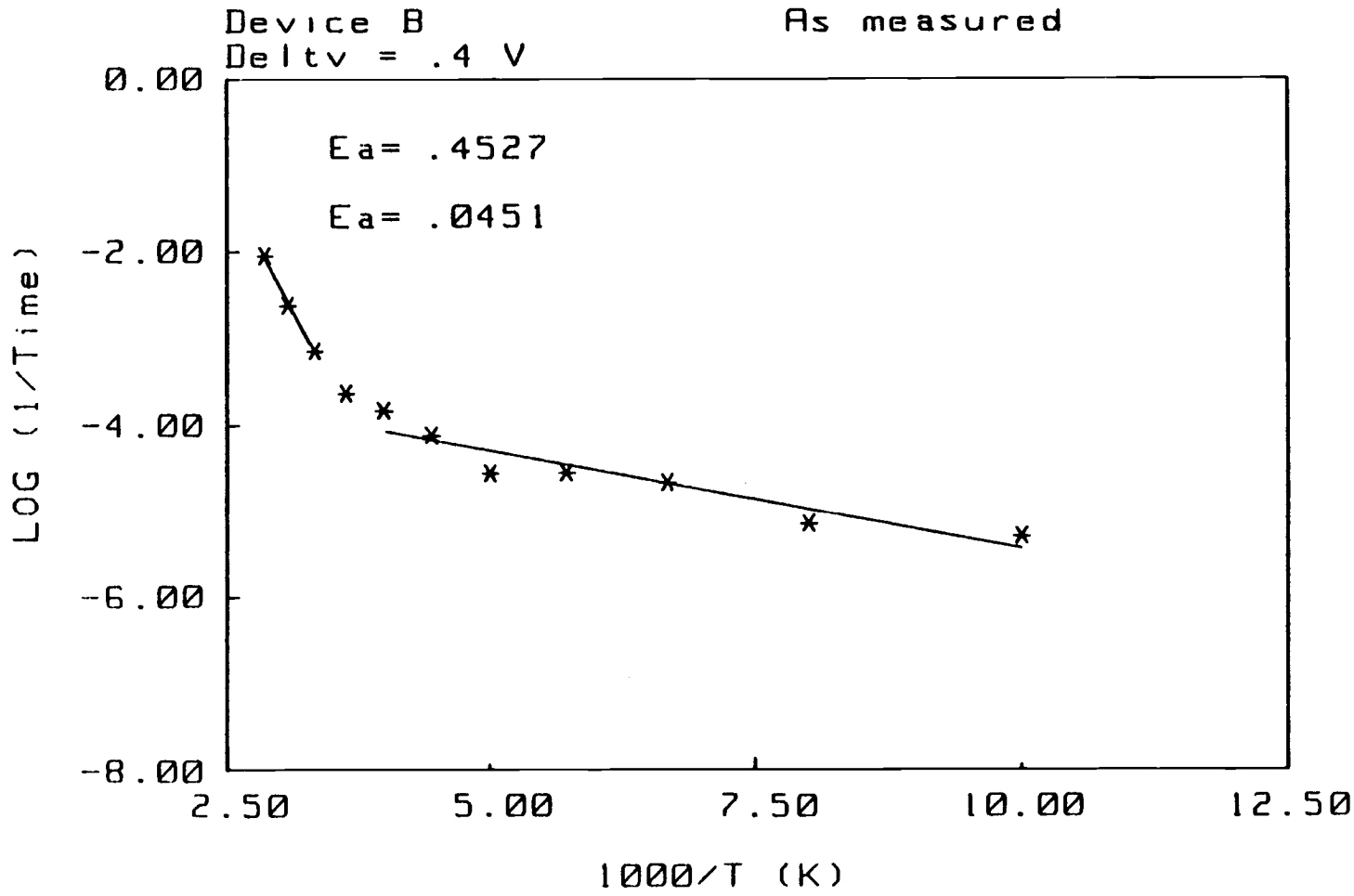
log t. Using a least square fit, the slopes and intercepts can be used to extrapolate or interpolate the amount of shift at any bias time or temperature.

Arrhenius plots are shown in Fig.4.8 and 4.9 for samples A and B, respectively. It is clear that there are two distinct electron trapping mechanisms which give rise to two different activation energies. The activation energies calculated from these figures are 0.44eV, 0.041eV for sample A and 0.45eV, 0.045eV for sample B. The point at 275K is chosen as the boundary point, which was not included in fitting either of the two portions of the curve. The low temperature activation energy of approximatedly 40-50meV is consistent with the model of thermionic tunneling of electrons into a discrete trap in the native oxide. The high-temperature, (300-350K), large activation energy (~0.45eV) must be explained by invoking another electron trapping mechanism. If it is assumed that only two mechanisms contribute to the shift in Vfb, this larger activation energy is actually an effective value which is a combination of two activation energies, $\Delta E1$ and $\Delta E2$, where $\Delta E2$ is 45meV or 41meV.

In another words, in the high-temperature(300-350K) range, two electron trapping mechanisms are operational and the measured slope of the Arrhenius curve yields an effective activation energy due to the combined effects of both mechanisms. In contrast, in the low-temperature(below



4.8 Arrhenius plot of device A at Vfb=.4V.



4.9 Arrhenius plot of device B at ΔVfb=.4V.

275K) range, only one electron trapping mechanism with an activation energy of 40-50meV is important. If it is assumed that these two mechanisms can be decoupled, an estimate of ΔE1 can be obtained. From the Arrhenius plot, it is apparent that the mechanism with the activation energy E1 starts to contribute to the flat band shift at above room temperature. Thus, the amount of flat band shift due to the thermionic-tunneling of electrons into the native oxide can be extrapolated into the high temperature regime and the amount of flat band shift due exclusively to the second mechanism may be estimated. This is accomplished by rearranging the data between temperatures of 100K to 250K into 4 groups according to the 4 bias times. Four bias-stress curves are then fitted, namely one curve for each bias time, 500sec, 1000sec, 2000sec, 4000sec. The amount of shift for these four bias times is then extrapolated into the high-temperature regime for the three temperatures, 300, 325 and 350K. The results of this extrapolation are shown in Fig.4.10 and 4.11. These figures indicate the estimated amount of flat band shift due exclusively to thermionic-tunneling as a function of stress time for the three temperatures of interest. The numerical values of this estimated flat band shift are listed in Tables 4.2 and 4.3.

The extrapolated amount of shift is then subtracted from the measured data, which yields difference curves as

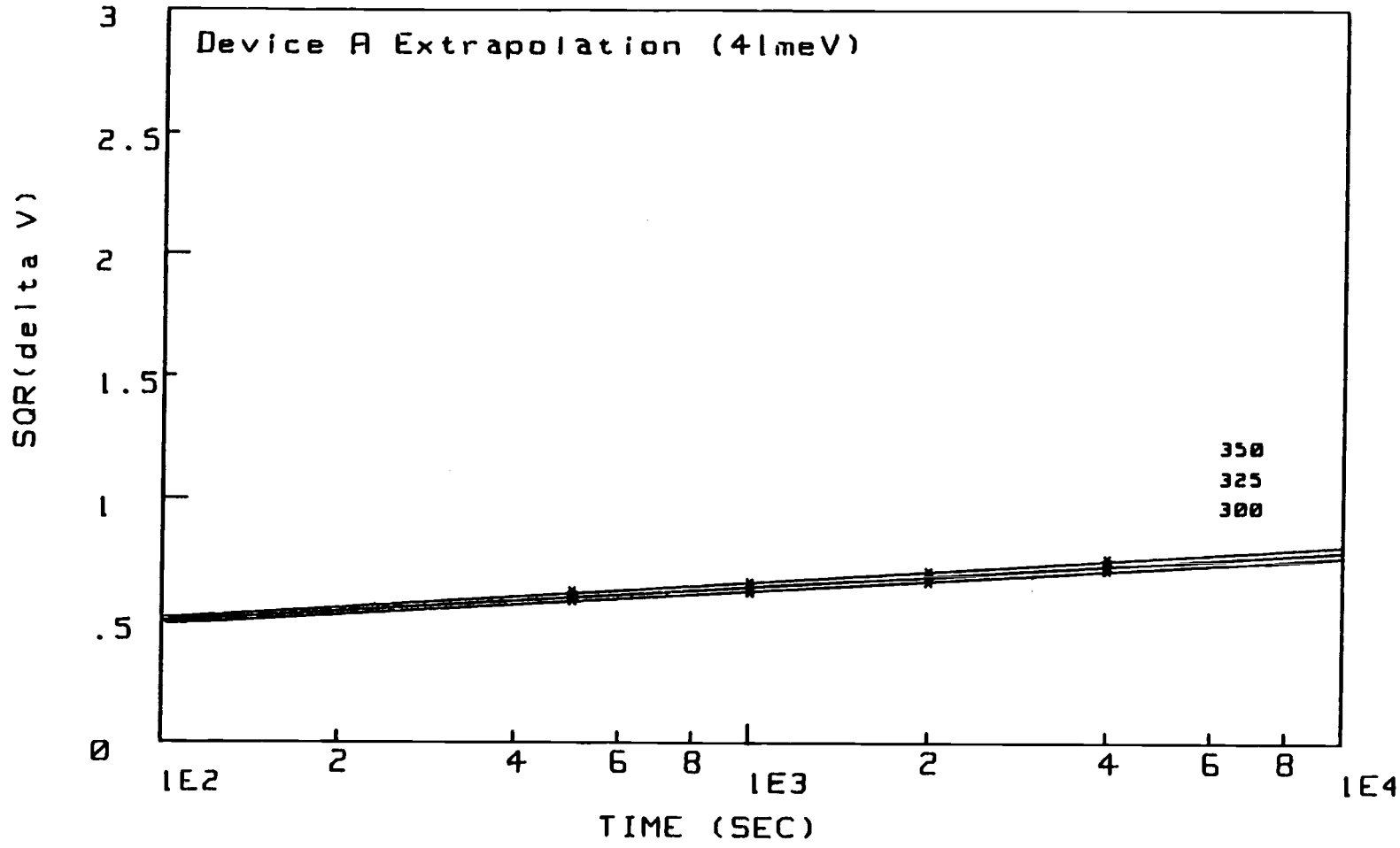


Fig. 4.10 Extrapolation of the ΔVfb from the measured tunneling effect of device A.

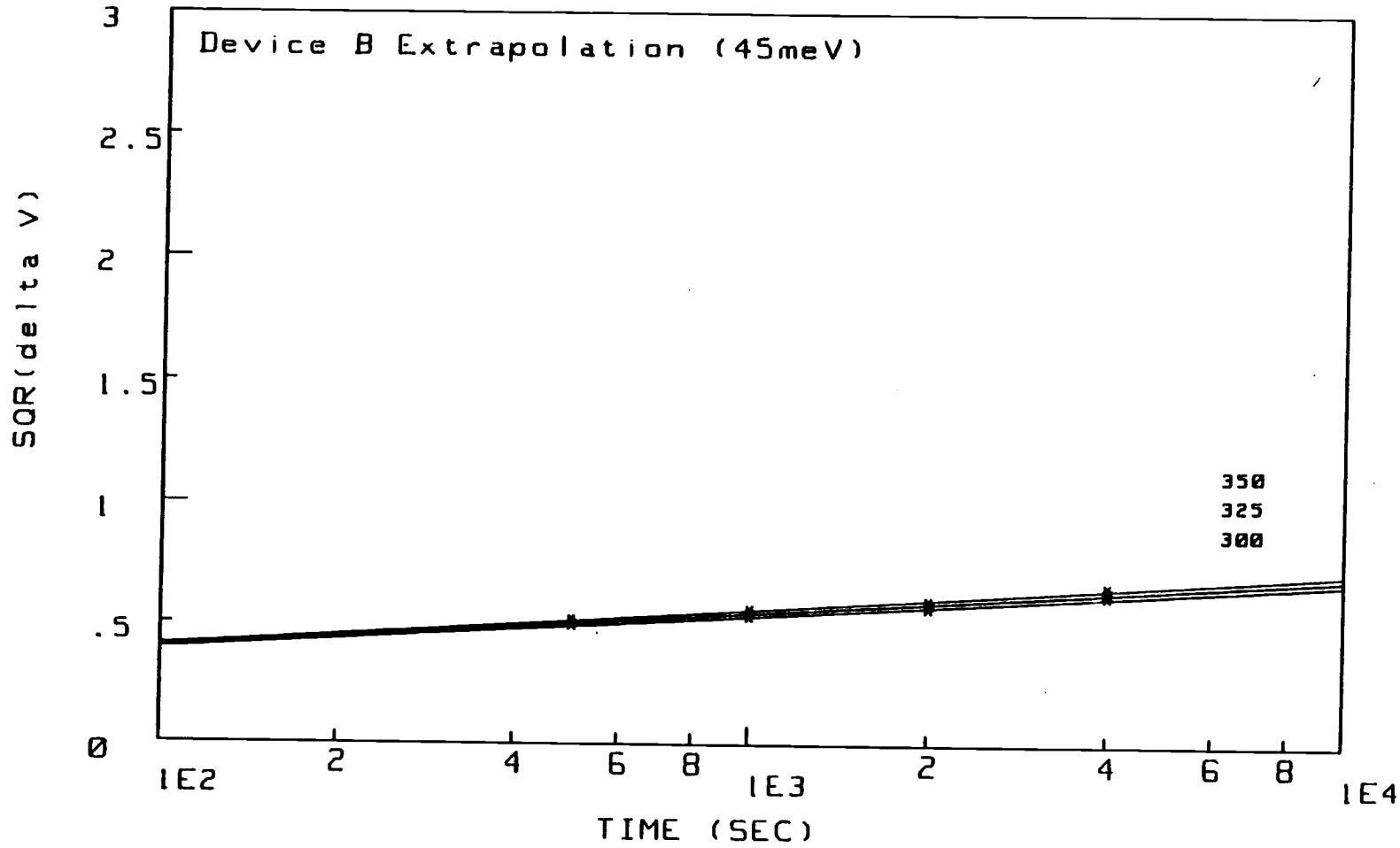


Fig. 4.11 Extrapolation of the ΔVfb from the measured tunneling effect of device B.

T K	tsec	ΔV	√ΔV	% Total
350	500	.3838	.6195	36.2
	1000	.4299	.6557	33.1
	2000	.4915	.7011	30.0
	4000	.5674	.7532	27.8
325	500	.3623	.6019	71.0
	1000	.4063	.6374	67.3
	2000	.4644	.6815	61.5
	4000	.5347	.7312	56.4
300	500	.3413	.5842	93.8
	1000	.3833	.6191	93.3
	2000	.4380	.6618	87.2
	4000	.5030	.7092	81.9

Table 4.2 Extrapolated amount of ΔVfb of device A at 350K, 325K and 300K.

T K	tsec	ΔV	√ΔV	% Total
350	500	.2637	.5135	30.0
	1000	.3106	.5573	28.3
	2000	.3551	.5959	24.9
	4000	.4266	.6532	23.5
325	500	.2514	.5014	56.1
	1000	.2952	.5433	53.8
	2000	.3376	.5810	46.8
	4000	.4036	.6353	43.2
300	500	.2394	.4893	79.3
	1000	.2802	.5293	80.5
	2000	.3205	.5661	74.9
	4000	.3812	.6115	70.3

Table 4.3 Extrapolated amount of ΔVfb of device B at 350K, 325K and 300K.

shown in Figs.4.12 and 4.13 and Tables 4.4 and 4.5. These difference curves correspond to the flat band shift when electron trapping is due exclusively to the ΔE1 mechanism. ΔE1 is then determined by plotting an Arrhenius curve from the difference curves. As shown in Figs.4.14 and 4.15, the activation energies deduced in this manner are 1.2eV and 1.1eV for sample A and B, respectively, which are in close agreement with that predicted by the PVNNH model. The activation energies obtained from these experiments are summarized in Table 4.6.

4.2 Long Bias Time Measurements

In order to investigate the saturation behavior of the shift in Vfb, long bias time (up to 64,000sec) measurements were made on sample B at 300K and 350K, as shown in Figs.4.16 and 4.17. The corresponding flat band shifts are listed in Table 4.7. At 300K the $\sqrt{\Delta V_{fb}}$ vs log t curve is linear up to stress time of 64,000sec. At 350K, however, there is a deviation from linearity and the curve exhibits saturation near 32,000sec, and a slight decrease at 64,000sec. This decrease is probably an artifact of the measurement. After biasing for 64,000sec, the 4V positive bias is removed in order to perform the C-V sweep to determine the flat band shift. If the bias is removed, even for a short time, while the flat band shift is in

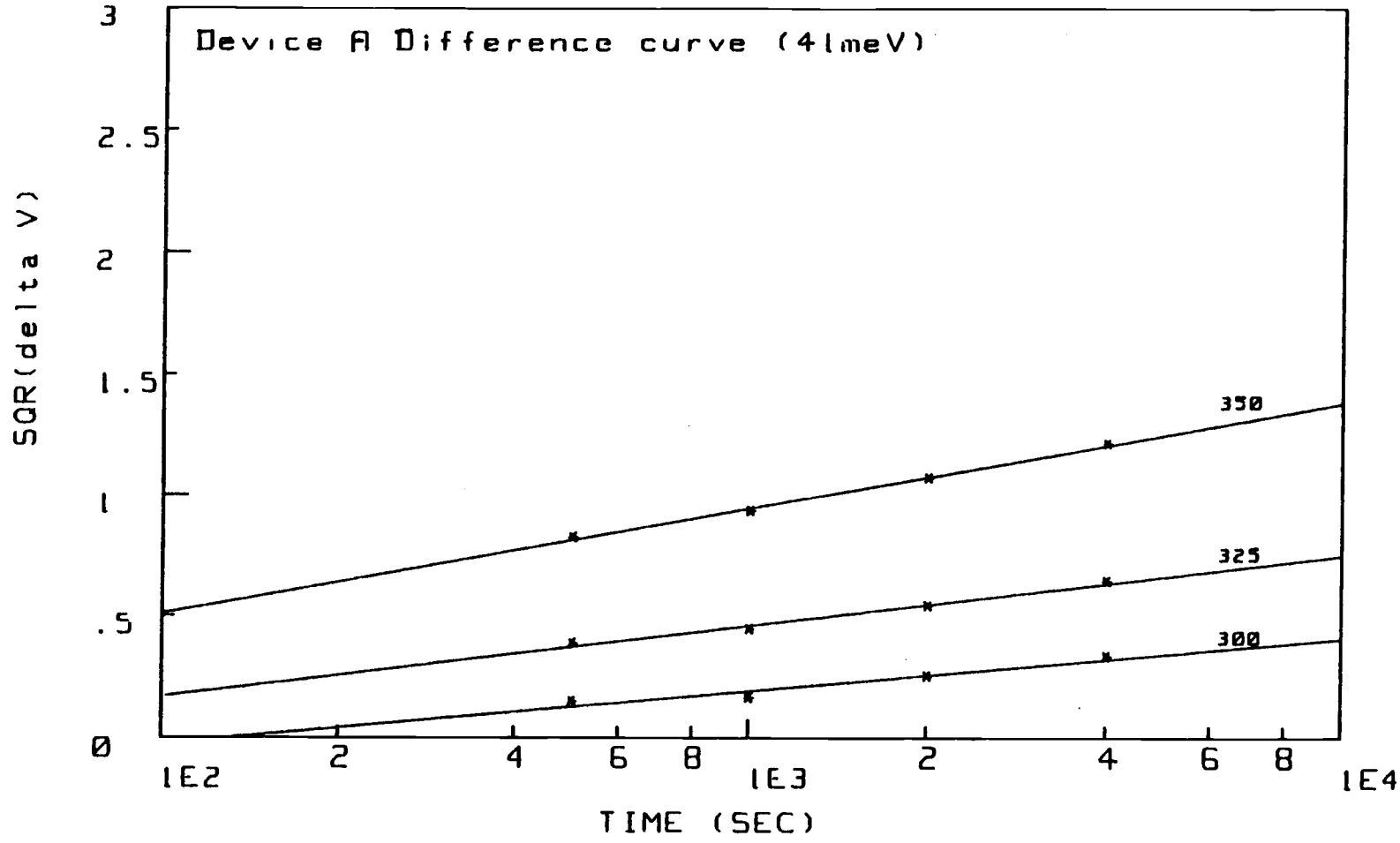


Fig. 4.12 Difference curves of device A, shift in Vfb due only to PVNNH.

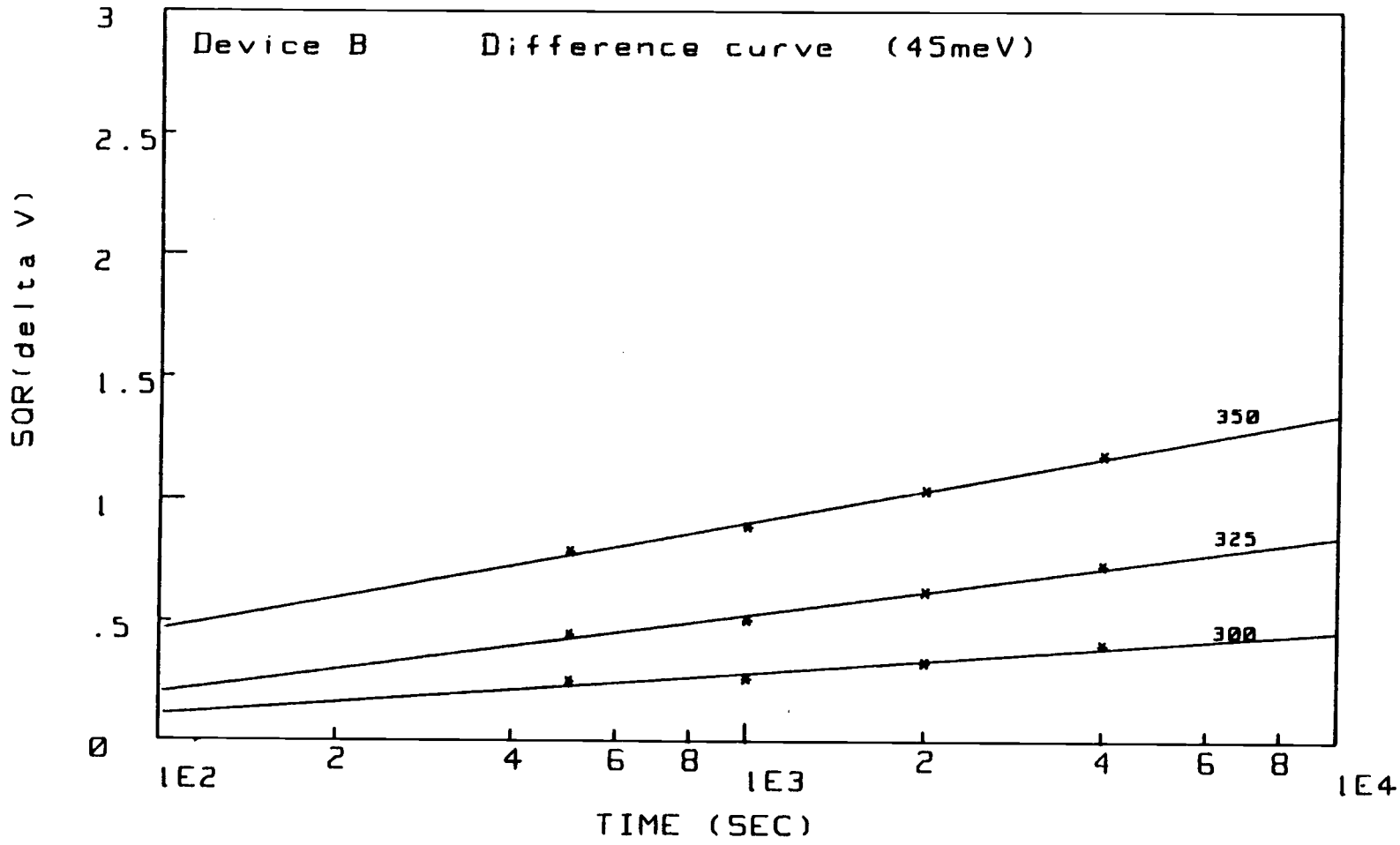


Fig. 4.13 Difference curves of device B, shift in Vfb due only to PVNNH.

T K	tsec	ΔV	√ΔV	% Total
350	500	.6767	.8226	63.8
	1000	.8672	.9312	66.9
	2000	1.1463	1.0707	70.0
	4000	1.4727	1.2135	72.2
325	500	.1478	.3844	29.0
	1000	.1973	.4442	32.7
	2000	.2911	.5395	38.5
	4000	.4134	.6430	43.6
300	500	.0224	.1497	6.2
	1000	.0274	.1655	6.7
	2000	.0644	.2538	12.8
	4000	.1113	.3336	18.1

Table 4.4 Calculated amount of ΔVfb of device A due only to PVNNH at 350K, 325K and 300K.

T K	tsec	ΔV	√ΔV	% Total
350	500	.6155	.7845	70.0
	1000	.7863	.8867	71.7
	2000	1.0704	1.0346	75.1
	4000	1.3884	1.1783	76.5
325	500	.1967	.4435	43.9
	1000	.2535	.5035	46.2
	2000	.3840	.6197	53.2
	4000	.5317	.7292	56.8
300	500	.0625	.2500	20.7
	1000	.0680	.2608	19.5
	2000	.1073	.3276	25.1
	4000	.1614	.4017	29.7

Table 4.5 Calculated amount of ΔVfb of device B due only to PVNNH at 350K, 325K and 300K.

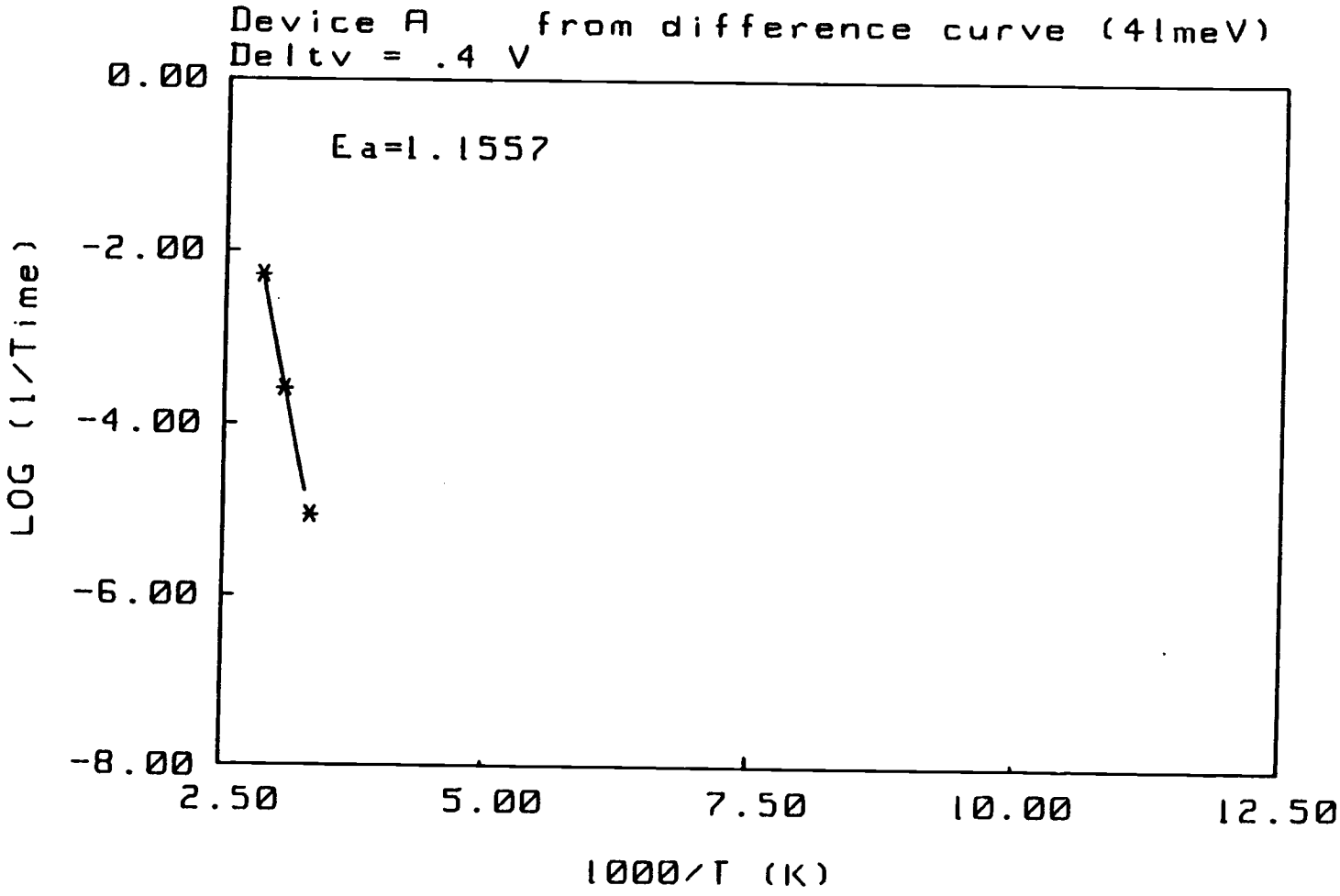


Fig. 4.14 Activation energy of PVNNH calculated from the measured data of device A.

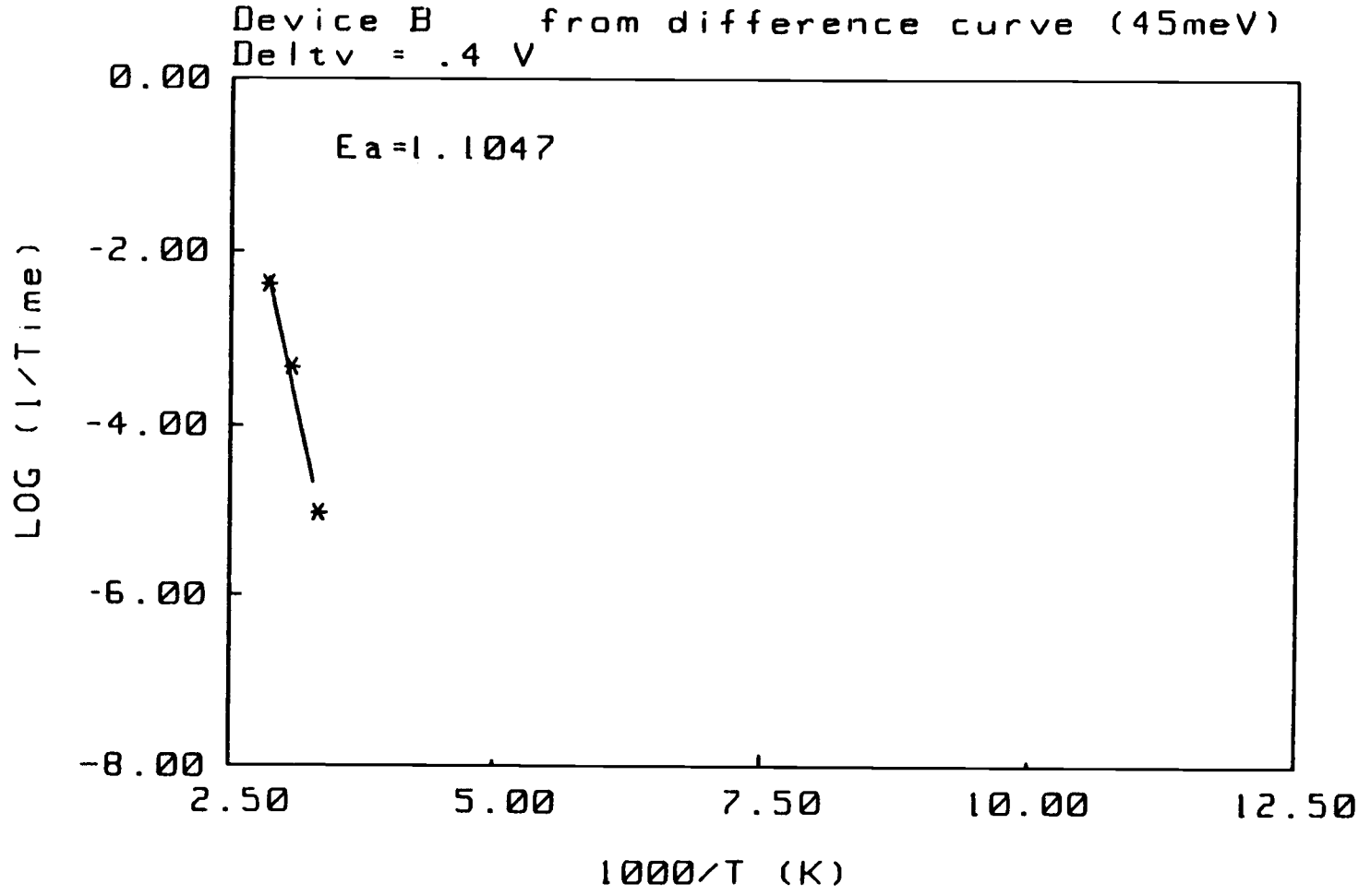


Fig. 4.15 Activation energy of PVNNH calculated from the measured data of device B.

Sample	100K-250K	300K-350K
A	41meV	1.16eV
B	45meV	1.10eV

Table 4.6 Summary of the activation energies of both sample A and B at two temperature ranges.

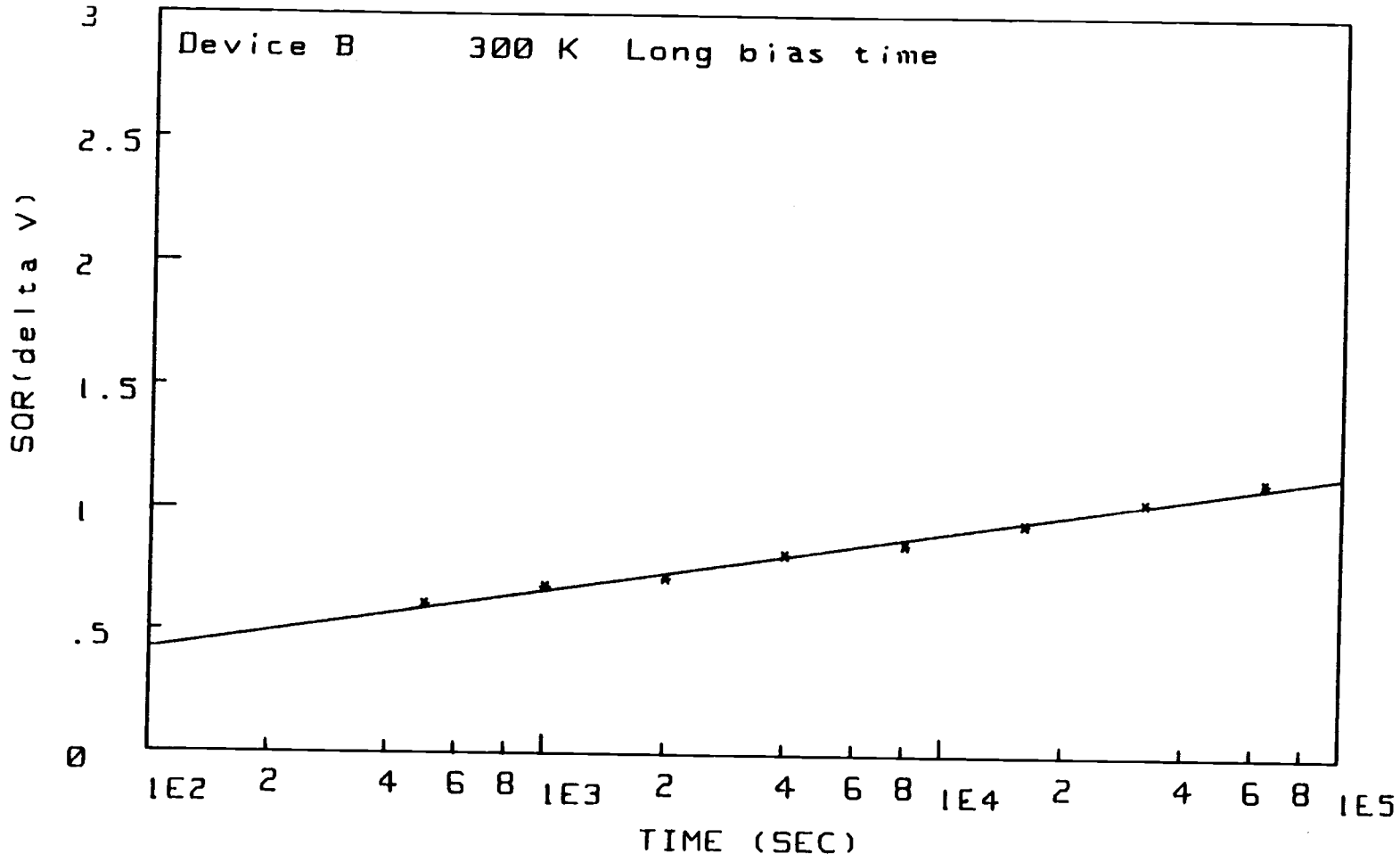


Fig. 4.16 Long bias-stress time measurement of device B at 300 K.

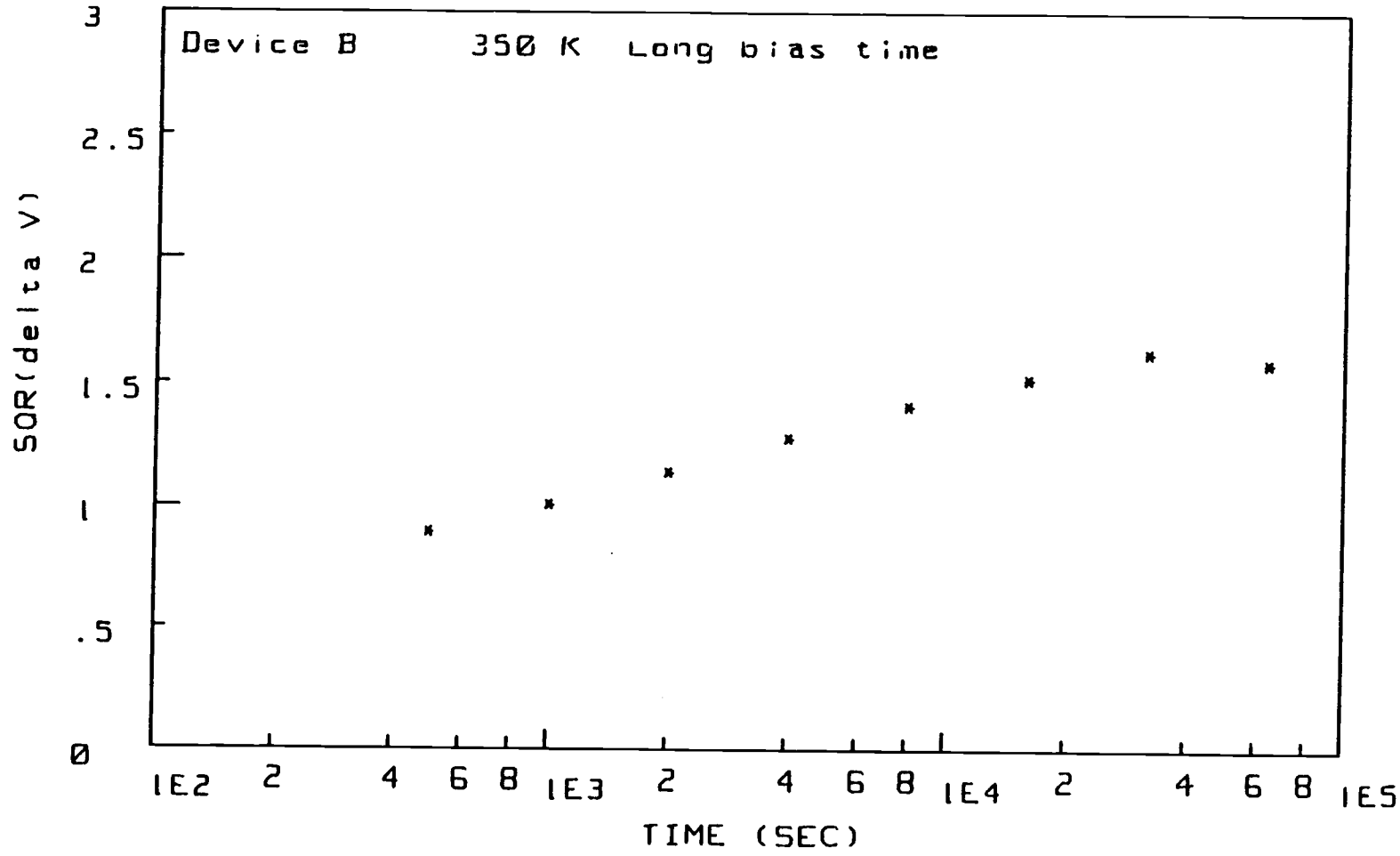


Fig. 4.17 Long bias-stress time measurement of device B at 350 K.

T K	tsec	ΔV	$\sqrt{\Delta V}$
350	500	.7880	.8877
	1000	1.0039	1.0019
	2000	1.2907	1.1361
	4000	1.6256	1.2750
	8000	1.9772	1.4061
	16000	2.2974	1.5157
	32000	2.6317	1.6222
	64000	2.5027	1.5820
300	500	.3665	.6054
	1000	.4609	.6789
	2000	.5132	.7164
	4000	.6665	.8164
	8000	.7372	.8586
	16000	.8917	.9443
	32000	1.0771	1.0379
	64000	1.2657	1.1251

Table 4.7 Results of long bias-stress time measurement of device B at 350K and 300K.

saturation, the amount of shift measured would be substantially reduced due to a reverse reaction that is operational during the C-V scan. Thus, at 350K, this sample exhibits saturation in this flat band shift at a stress time of approximately 32,000sec.

The saturation behavior is believed to result from one of two possibilities; (1) Enough electrons are trapped from the channel that the flat band condition is reached. (2) The native oxide traps are completely saturated with electrons and the phosphorous vacancy concentration is negligable because of nearest neighbour hopping. Which of these two saturation mechanisms is operational depends on the relative quantity of native oxide traps and initial phosphorous vacancy concentration which are determined by the device structure and processing conditions.

4.3 Native Oxide Trap Density and P Vacancy Concentration

A rough estimate of the trap density in the native oxide and the phosphorous vacancy concentration in the InP near the interface can be made from the experimental data.

Taking the largest experimentally observed flat band shifts (bias stress times of 32,000sec for sample B and 4000sec for sample A and B at 350K), the native oxide trap density can be approximated by assuming trapping occurs only in the native oxide layer, and the trapped electrons are distributed uniformly,

$$Nox = \frac{\Delta V_{nox} Cox}{t_{nox} q} \qquad (4.1)$$

where ΔV_{nox} is the shift in the flat band voltage due to electrons trapped in the native oxide only, which is extrapolated from the low temperature data, and t_{nox} is the thickness of the native oxide.

The phosphorous vacancy concentration at the InP surface can be estimated by assuming a simple exponential distribution of the trapped electrons in the InP accumulation layer, with maximum at the surface and zero at a distance L_D from the interface. The P vacancy concentration is then estimated as,

$$[Vp]_s = \frac{2.72 \Delta V_{PVNNH} Cox}{3 L_D q} \qquad (4.2)$$

where ΔV_{PVNNH} is the shift due only to PVNNH which is obtained by subtracting the flat band voltage shift in the native oxide from the total flat band voltage shift. The factor of 2.72 comes from exponential of 1. These and other estimated values are listed in Table 4.8.

The estimated values for the native oxide trap concentrations are 9.6E17cm^{-3} for sample A and 2.2E18cm^{-3} for sample B. This estimate should be considered to be a firm upper limit in the case of sample B which exhibits saturation in the flat band voltage shift , while it is not the case for sample A since saturation was not obtained. These values compare fairly well with 3.7E18cm^{-3}

Sample bias	Item	Measured total	Tunneling only	PVNNH only
A 350K 4,000s	ΔV	2.0401	0.5674	1.4727
	Ne	5.2E11	1.4E11	3.8E11
	ox.trap.d	--	9.6E17	--
	[Vp]s	--	--	4.8E16
B 350K 4,000s	ΔV	1.8150	0.4266	1.3884
	Ne	4.6E11	1.1E11	3.5E11
	ox.trap.d	--	1.2E18	--
	[Vp]s	--	--	4.5E16
B 350K 32,000s	ΔV	2.6317	0.7859	1.8458
	Ne	6.0E11	2.0E11	5.0E11
	ox.trap.d	--	2.2E18	--
	[Vp]s	--	--	6.0E16

Table 4.8 Estimated amount of native oxide trap density and [Vp] near the interface.

estimated by Lile and Taylor [4] from field-effect mobility measurements, but is larger than the value $1.5E17cm^{-3}$ estimated by Okamure and Kobayashi [3].

In any event, a certain amount of variation in the estimated oxide trap density is to be expected between various researchers because of variations in device processing and differences in the techniques used to estimate the trap density.

The estimated value for the phosphorous vacancy concentration in InP is $6E16cm^{-3}$, which is a value reasonable that would be expected in these samples since a phosphorous over pressure was not employed in preparing the sample and the oxide is deposited under direct plasma conditions using plasma-enhanced chemical vapor deposition (PECVD) technique.

4.4 Sources of Experimental Error

There are several sources of error inherent in the measurement method employed. During every sweep of the C-V curve, the 4V positive bias is removed temporarily. The voltage sweep begins at +3V. If the flat band shift has not saturated, the sweep in the positive voltage region introduces additional flat band shift, while the sweep from 0 to -3V decreases this shift. Depending on the previous bias history, the effects of sweeping from +3V to 0V may be different than that of the sweep from 0 to -3V.

Also, the Vfb obtained from the first sweep, which was considered to be the zero bias time, would not be the actual Vfb.

The sweep rate is chosen to be 100mV/sec, and 60 sec is required to obtain a C-V curve. If the bias time were small compared to 60sec, the flat band shift associated with the voltage sweep would introduce appreciable errors in the analysis of the flat band shift. This effect was observed in the initial experiments when the bias times were chosen to be 40sec, 80sec, 120sec, 240sec, 480sec and 960sec. For these short bias times, using the same approach as described in section 4.1, the resulting activation energies obtained were 0.48eV and 3.9meV, as shown in Fig.4.18. Note that a considerable amount of error is introduced into the measurement if the bias times are not substantially larger than the voltage sweep time.

There are two ways to reduce this error. One way is to use long bias times. With bias times of 500sec, 1000sec, 2000sec and 4000sec, the amount of error should be substantially reduced because the sweep time is approximately 12% of the shortest bias-stress time.

Another way of minimizing the error is by modifying the method of obtaining Vfb. Instead of making a complete C-V sweep, Vfb can be found using a "search" method.

The computer controlled search method is initialized at a given temperature by first biasing the sample

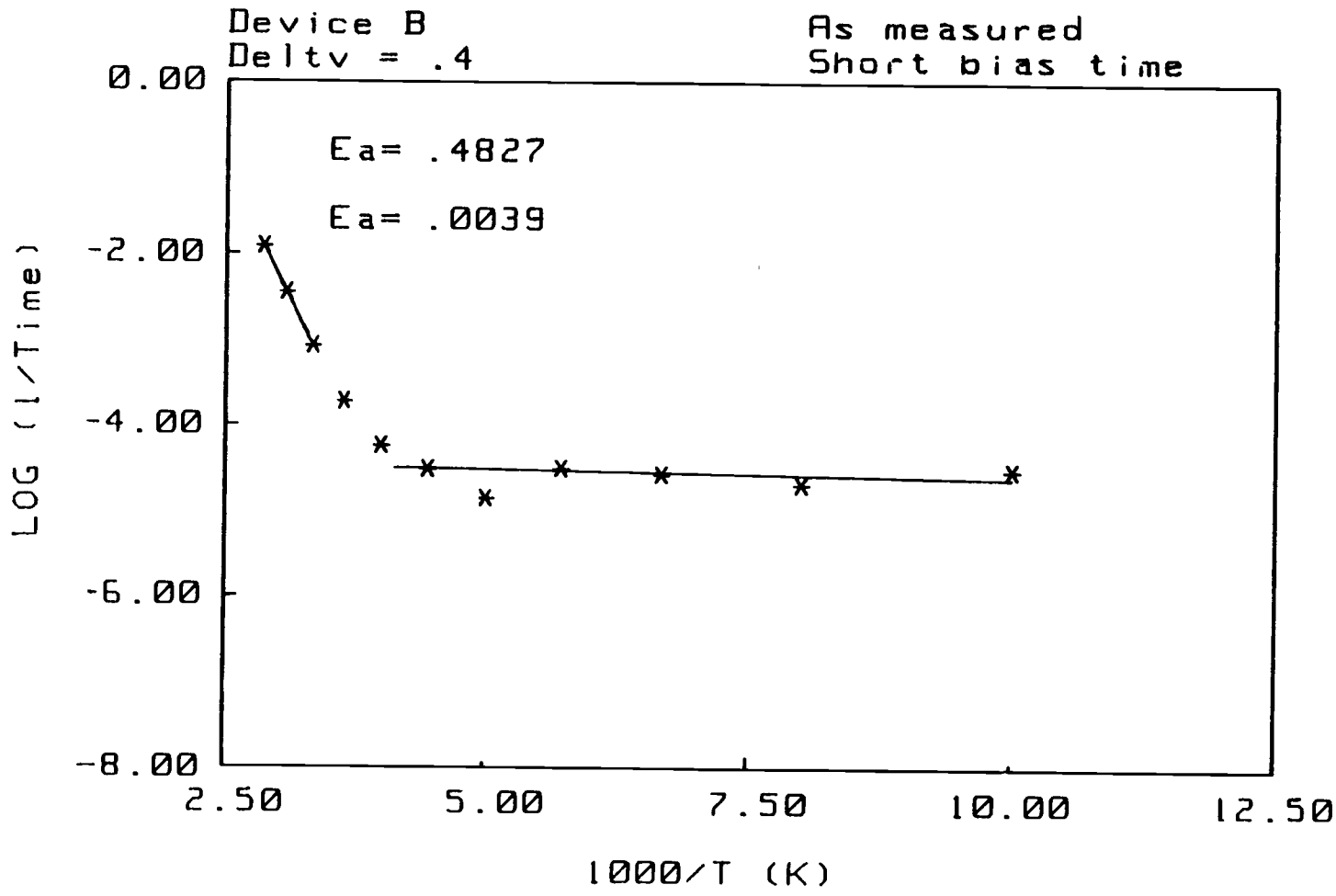


Fig. 4.18 Arrhenius plot of device B when the bias-stress times were chosen to be 40sec, 80sec, 120sec, 240sec, 480sec and 960sec.

momentarily (~1sec) into accumulation to measure the oxide capacitance, and hence assess the flat band capacitance, Cfb. Vfb is then found by beginning at zero volts and incrementing the voltage until the measured capacitance is approximately Cfb. Vfb is then interpolated from the nearest two adjacent points. The amount of search time depends on the required accuracy; in this experiment a maximun search time of 10sec yielded satisfactory results. A +4V bias is then applied for the desired amount of stress time. The +4V bias is then removed, and Vfb is again found by a computer controlled search. This procedure of bias-stressing the sample and searching for Vfb is repeated for larger bias times. The error due to the shift during the voltage sweep is thus decreased considerably, and, of prime importance, the effects of the negative bias portion of the sweep are completely avoided.

The search method was used as a comparison to the method employed in the experiment which employs a minimun bias-stress time of 500sec. The results are shown in Fig.4.19 and Table 4.9, where the dashed line is the shift measured by the "Vfb search" method. Note that in this case the measurements were done on different capacitor dots located on different positions on the sample. Thus, some scatter in the data is expected. Fig 4.19 indicates that the amount of experimental error associated with long bias time method is quite acceptable.

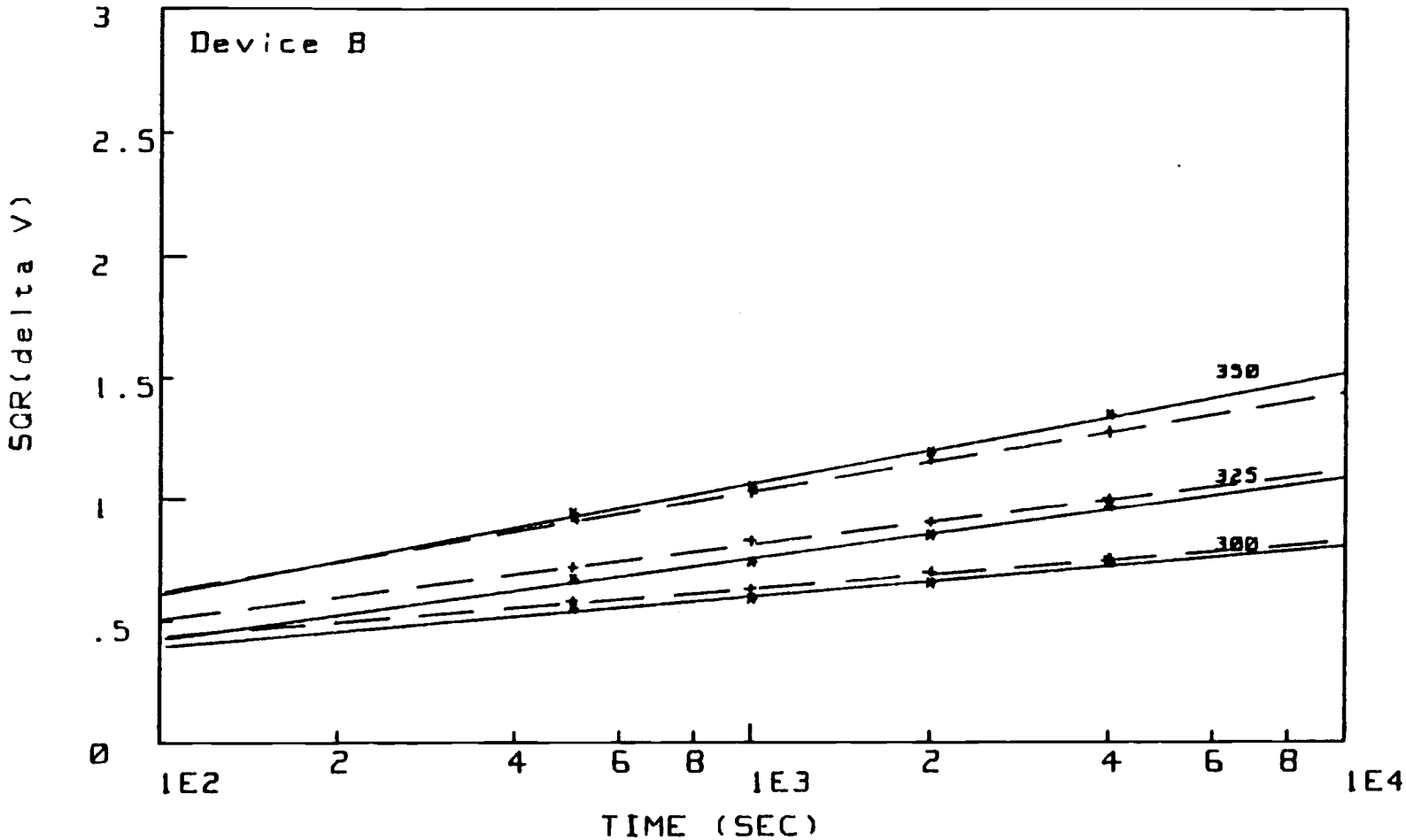


Fig. 4.19 Deviation of the measured C-V curves using "sweep" and "search" techniques.Where the dashed line is from the search method.

T K	tsec	ΔV Sweep	ΔV Search	% devi.
350	500	.8792	.8246	6.6
	1000	1.0969	1.0445	5.0
	2000	1.4255	1.3371	3.5
	4000	1.8155	1.6288	11.0
325	500	.4481	.5139	-12.0
	1000	.5487	.6759	-18.0
	2000	.7216	.8060	-10.4
	4000	.9353	.9999	-6.5
300	500	.3019	.3357	-10.0
	1000	.3482	.3882	-10.3
	2000	.4278	.4789	-10.7
	4000	.5426	.5683	-4.5

Table 4.9 Deviation of the results measured using "Sweep" and "Search" techniques of device B at 350K, 325K and 300K.

5. COMPUTER SIMULATION

In this chapter, the results of a computer simulation of the flat band voltage shift versus time for the PVNNH mechanism are described. The simulation is based on an analysis of the kinetics of the PVNNH defect reaction sequence. Electron trapping is accounted for in a semi-empirical fashion, electron shielding is accounted for by a solution of the Poisson equation, and the kinetic rate equation is solved iteratively. The simulation agrees quite well with the temperature-dependence of the flat band voltage shift but deviates slightly from the experimental data at high temperature. Several reasons for this deviation are suggested.

5.1 PVNNH Rate Mechanism

After an n-type InP MIS capacitor is biased into accumulation, the electron concentration in the accumulation layer is increased to approximately $10^{17}cm^{-3}$, which favors the formation of a negatively charged antisite defect complex, $(V_{In}In_P)^{-3}$. According to Van Vechten and Wager [8], as described in Chapter 2, the reaction sequence and time constants at room temperature for the individual steps of the forward reaction are as follows:

$$Vp^{+}+e^{-}<==>Vp^{o} \qquad \tau_1=1ps \qquad (5.1)$$

$$Vp^{\circ} \Longleftrightarrow (V_{In}In_p)^{\circ} \qquad \tau_2=0.5s \qquad (5.2)$$

$$(V_{In}In_p)^{\circ}+e^{-} \Longleftrightarrow (V_{In}In_p)^{-} \qquad \tau_3=1ns \qquad (5.3)$$

$$(V_{In}In_p)^{-}+e^{-} \Longleftrightarrow (V_{In}In_p)^{-2} \qquad \tau_4=3us \qquad (5.4)$$

$$(V_{In}In_p)^{-2}+e^{-} \Longleftrightarrow (V_{In}In_p)^{-3} \qquad \tau_5=8ms \qquad (5.5)$$

The rate limiting step is 5.2, in which the indium atom hops into the phosphorous vacant site.

The kinetic equation for step 5.2 is:

$$\frac{d[(V_{In}In_p)^{\circ}]}{dt}=k_{2+}[Vp^{\circ}]-k_{2-}[(V_{In}In_p)^{\circ}] \qquad (5.6)$$

where k_{2+} and k_{2-} are the rate constants for the forward and reverse reaction of step 5.2, where k_{2+} is just the inverse of τ_2. Since the time constants of the other four steps are much smaller than the time constant of step 5.2, we can treat step 5.1 as if it is in equilibrium;

$$K1=\frac{[Vp^{\circ}]}{[Vp^{+}][e^{-}]} \qquad (5.7)$$

where K1 is the equilibrium constant for step 5.1. Once $(V_{In}In_p)^{\circ}$ is formed, it captures electrons very quickly and becomes $(V_{In}In_p)^{-3}$. In this case, equation 5.6 can be rewritten by replacing $[Vp^{\circ}]$ obtained in terms of $[Vp^{+}]$, $[e^{-}]$ and K1 from 5.7. Similarly, $[(V_{In}In_p)^{\circ}]$ can be replace by:

$$[(V_{In}In_p)^{\circ}]=\frac{[(V_{In}In_p)^{-3}]}{K3K4K5[e^{-}]^3} \qquad (5.8)$$

and k_{2-} can be calculated from $K2=k_{2-}/k_{2+}$ where K2,K3,K4,K5 are the equilibrium constants of step 5.2,

5.3, 5.4, and 5.5, respectively. K2 can be estimated from the activation energy that is obtained from the experiment , K3,K4,K5 can be calculated from the energy that is released associated with the capture of electrons in these traps,

$$-kT\ln K1=-[Ef-E_I(Vp)] \quad (5.9)$$

$$-kT\ln K2=1.1 \quad (5.10)$$

$$-kT\ln K3=-[Ef-E_{I2}(In_p)] \quad (5.11)$$

$$-kT\ln K4=-[Ef-E_{I1}(In_p)] \quad (5.12)$$

$$-kT\ln K5=-[Ef-E_I(V_{In})] \quad (5.13)$$

the calculated K2 at 300K and 350K is 3.6E-19 and 1.5E-16 , the corresponding k_{2-} is 5.6E18 and 1.3E16 for 300K and 350K, respectively. The ionization levels of vacancies and antisite defects in InP have been estimated [8] by H. Temkin et al. [23] and J. P. Buisson et al. [24] to be 0.21eV, 0.17eV, 0.04eV and 0.99eV for V_{In}, $E_{I1}(In_p)$, $E_{I2}(In_p)$ and $E_I(Vp)$ respectively. Using these values, with a doping concentration of 4E15cm^{-3}, the equilibrium constants estimated at 300K are K3=1.9E20, K4=1.3E18, K5=1.0E17 and K3=4.8E16, K4=6.5E14, K5=1.7E14 at 350K, respectively. According to these values, the reverse reaction is very small and the rate equation can be approximate by:

$$\frac{d[(V_{In}In_p)-3]}{dt}=K1k_{2+}[Vp^+][e^-] \quad (5.14)$$

However, if equation 5.14 is used in the simulation,

with the procedure that is described later, the temperature dependence of the flat band shift can not fit to the experimental data. The amount of flat band shift obtained from the simulation at 350K would be smaller by a factor of 3 compared to that obtained from the experiment.

Another possible reaction sequence is proposed to describe the kinetics of the reaction, as shown in Fig. 5.1. The solid line indicates the relative activation barrier that is associated with these individual reaction steps before the application of the gate bias. After the gate bias is applied, the quasi-Fermi level position is shifted toward the conduction band, and the energy that released is associated with an electron captured by the trap is increased by an amount that is approximately the amount of shift in the Fermi-level. Since the rate of electron capture by these traps is very fast, the barrier that an electron has to overcome is small. If the applied gate bias is slightly larger than the barrier for the forward reaction of step 5.3, a new activation barrier curve representing this condition would be as the dashed line shown in Fig.5.1. Note that the relative positions of the neutral species Vp^{o} and $(V_{In}In_{p})^{o}$ are not influenced by the change in the Fermi-level, the change in the Fermi-level smears out the forward barriers for steps 5.1 and 5.3, which results in only three steps left in the reaction sequence:

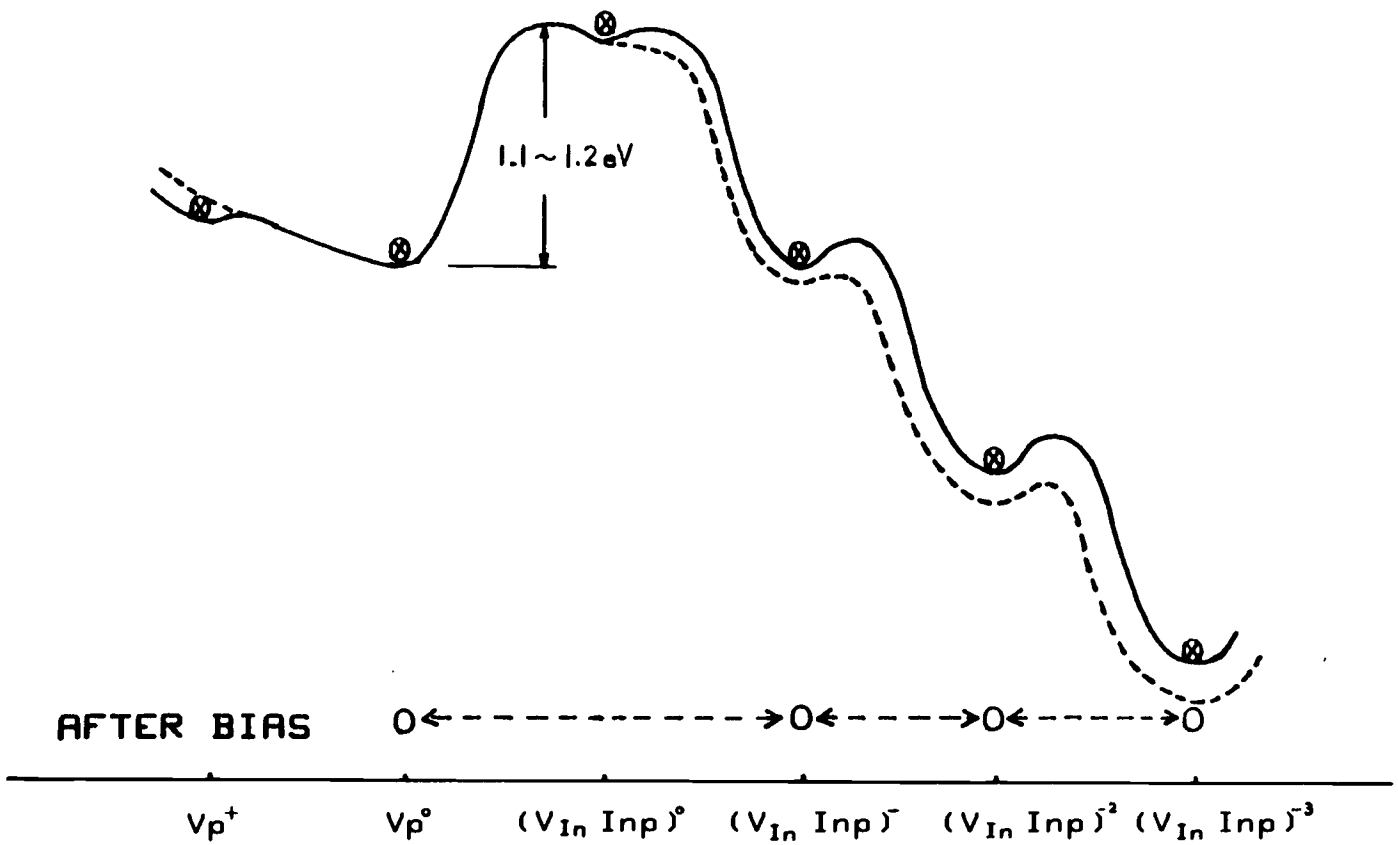


Fig. 5.1 Proposed relative reaction barriers for the PVNNH mechanism. Solid line and dashed line correspond to before and after applying the gate bias, respectively. Only 3 stable configurations are left when the bias is applied.

$$Vp^{o}+e^{-}\langle==\rangle(V_{In}In_{p})^{-} \quad (5.15)$$

$$(V_{In}In_{p})^{-}+e^{-}\langle==\rangle(V_{In}In_{p})^{-2} \quad (5.16)$$

$$(V_{In}In_{p})^{-2}+e^{-}\langle==\rangle(V_{In}In_{p})^{-3} \quad (5.17)$$

The rate limiting step is now 5.15, and the time constant for this forward reaction can be approximated by the time constant of step 5.2. Steps 5.16 and 5.17 are very fast compared to step 5.15. Using similar argument as for the five step sequence, the reverse reaction rate is very small and can be neglected. The kinetic equation is then:

$$\frac{d[(V_{In}In_{p})^{-3}]}{dt}=k_{+}[Vp^{o}][e^{-}] \quad (5.18)$$

The number of trapped electrons associated with the formation of $(V_{In}In_{p})^{-3}$ that is measured is only 3. The equation for the trapped electron concentration is then:

$$\frac{dNtr}{dt}=3k_{+}[Vp^{o}][e^{-}]. \quad (5.19)$$

The electron concentration $[e^{-}]$ depends on the surface potential ψs. As trapping occurs, shielding due to the trapped electrons reduces the effective bias, and the surface potential decreases. $[e^{-}]$ is also a function of distance from the oxide-InP interface, it can be expressed in terms of the electric potential $\psi(x)$ in the InP. To find $\psi(x)$, the Poisson equation must be solved. If degenerate statistics are not used, for the purpose of simplicity, it can be shown [25] that,

$$Es=\frac{2}{L_D}\left[(e^{\beta\psi s}-\beta\psi s-1)+\frac{Pno}{Nno}(e^{-\beta\psi s}+\beta\psi s-1)\right]^{1/2} \qquad (5.20)$$

and Es can also be shown [26] to be

$$Es=\frac{\epsilon_{ox}}{\epsilon_s}\left[\frac{Vg-\psi s-\psi ms}{Xo}-\frac{qNe}{\epsilon_o\epsilon_{ox}}\left(1+\frac{\bar{X}}{L_D}\right)-\frac{qNe'}{\epsilon_o\epsilon_{ox}}\right] \qquad (5.21)$$

where ψms is the work function difference between Al and InP, $\beta=kT/q$, L_D is the Debye length, Vg is the gate voltage applied, Xo is the oxide thickness, Ne is the number of trapped electrons per centimeter square, Ne' is the number of trapped electrons in the native oxide per square centimeter, $\bar{X}$ is the centroid of the trapped electrons from the interface,

$$\bar{X}=\frac{\int_o^{LD} XNtr(x,t)\,dx}{Ntr(x,t)\,dx} \qquad (5.22)$$

$$Ne=\int_o^{LD} Ntr(x,t)\,dx \qquad (5.23)$$

where Ntr(x,t) is the concentration of the trapped electrons as a function of distance from the interface and as a function of time. The thickness of the accumulation layer was approximated as the Debye length. The electric potential can be approximated as

$$\psi(x)=xEs/L_D \qquad (5.24)$$

and electron concentration in the accumulation layer is then

$$[e^-]=N(x)=Nnexp(\beta\psi(x)) \qquad (5.25)$$

Equations 5.19 through 5.25 describe the trapping process, and the flat band voltage shift ΔVfb is

$$\Delta Vfb = \frac{qNe}{Co}\left(1+\frac{\bar{X}}{L_D}\right)+\frac{qNe'}{Co} \qquad (5.26)$$

where Co is the oxide capacitance.

However, simulation of the flat band voltage shift is not straight forward. The contribution from electrons trapped in the native oxide, Ne', is estimated in an empirical fashion by extrapolating the low temperature experimental curves in order to deduce the amount of flat band shift at high temperature (i.e. 300, 325, 350K) which is due to native oxide trapping. As shown in Fig.4.11, this procedure amounts to assuming that the flat band shift is simply a superposition of the shift from the two mechanisms.

The simulation begins at zero time with the assumption that no electrons are initially trapped. This simplified assumption may be relaxed later. Es is solved to determine the electron concentration in the accumulation layer. The accumulation layer is divided into 50 sections in order to numerically accomplish the integrations indicated in equations 5.22 and 5.23. It is assumed that Ntr, Es, $[Vp^{o}]$ and $[e^{-}]$ are constant during the calculation time increment Δt. Ntr is then

$$Ntr(t+\Delta t)-Ntr(t)=3k_{+}[Vp^{o}](x,t)[e^{-}](x,t)\Delta t/\tau \qquad (5.27)$$

The phosphorous vacancy concentration is a function of distance into the accumulation layer because the consumption rate of the vacancy depends upon the electron

concentration, which is also position-dependent. Ntr(x,t) is then integrated for the whole accumulation layer thickness to obtain the trapped electron density due to PVNNH, and then added to the amount calculated from the extrapolated value of electrons that are trapped in the oxide at the time of the calculation to obtain the total amount of trapped electrons. $\overline{X}$ and ΔVfb are then calculated. For the next time increment, $\overline{X}$, Ne and Ne' are substituted into equation 5.12 and a new surface electric field is calculated . The procedure is repeated until the desired simulation time period is achieved. A flow chart for the simulation is illustrated in Fig. 5.2.

The length of the calculation time increment, Δt, has to be chosen to be small enough such that Es, $[Vp^{o}]$ and $[e^{-}]$ remain approximately constant, as assumed in the formulation. Time increments of 0.001sec, 0.1sec and 1sec were used for the three simulation temperatures, and yielded virtually the same result; deviations were only 0.5%.

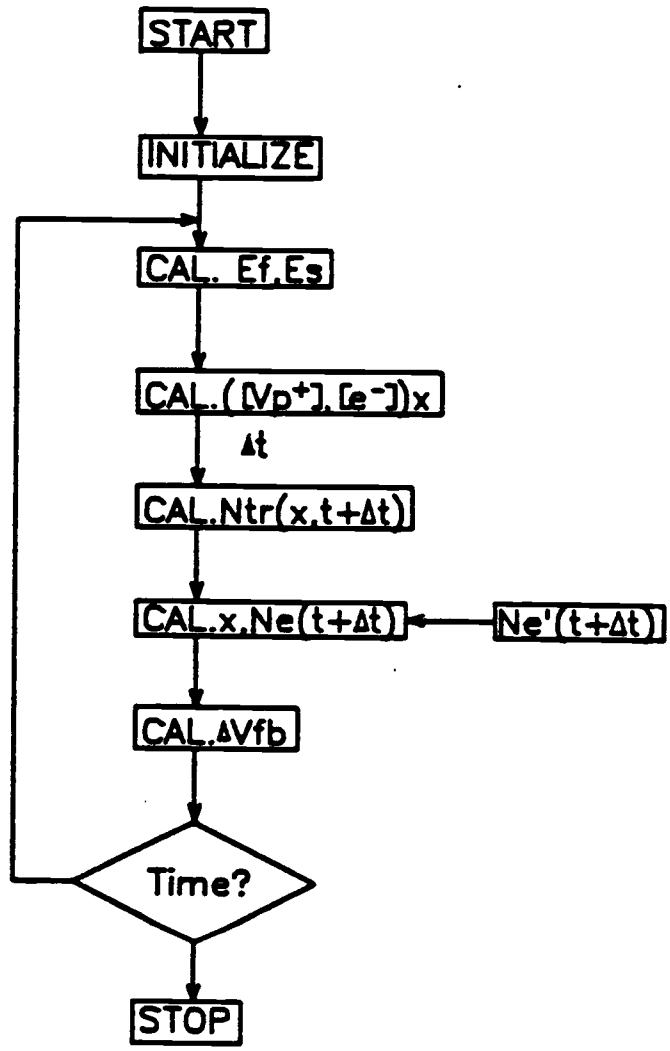


Fig. 5.2 Simulation flow chart.

5.2 Simulation Results

The simulated shift in the flat band voltage is shown in Figs. 5.3, 5.4, 5.5 and Table 5.1. Parameters chosen in these simulations are: $[Vp^{o}]$=2E17, $\Delta Sm/K$=15 and Ea=1.1eV, respectively.

The results of the simulation show good agreement with the experimentally determined temperature dependence of the flat band shift. The linear relationship between $\sqrt{\Delta Vfb}$ and log t is also found in the simulation, but starts to deviate after 200sec of bias time at 350K. The reasons for the deviation at high temperature observed in the simulation may be associated with the simple assumptions that were made to simplify the calculation assuming that the accumulation thickness is that of the Debye length and the use of nondegenerate statistics. One possible reason for this deviation is that other steps of the PVNNH mechanism, such as step 2 to 3 in Fig.2.2, can also occur, changing the charge state of the defect-complex from -3 to +1. Electrons would again be released and this would reduce the number of trapped electrons. A second reason for this deviation between the computer simulation and the experimental data at high temperature is that the two DCD mechanisms may be coupled together in a nonlinear fashion which was not accounted for in the simulation. Superposition was implicitly assumed in the simulation which implies a linear relation between the two DCD

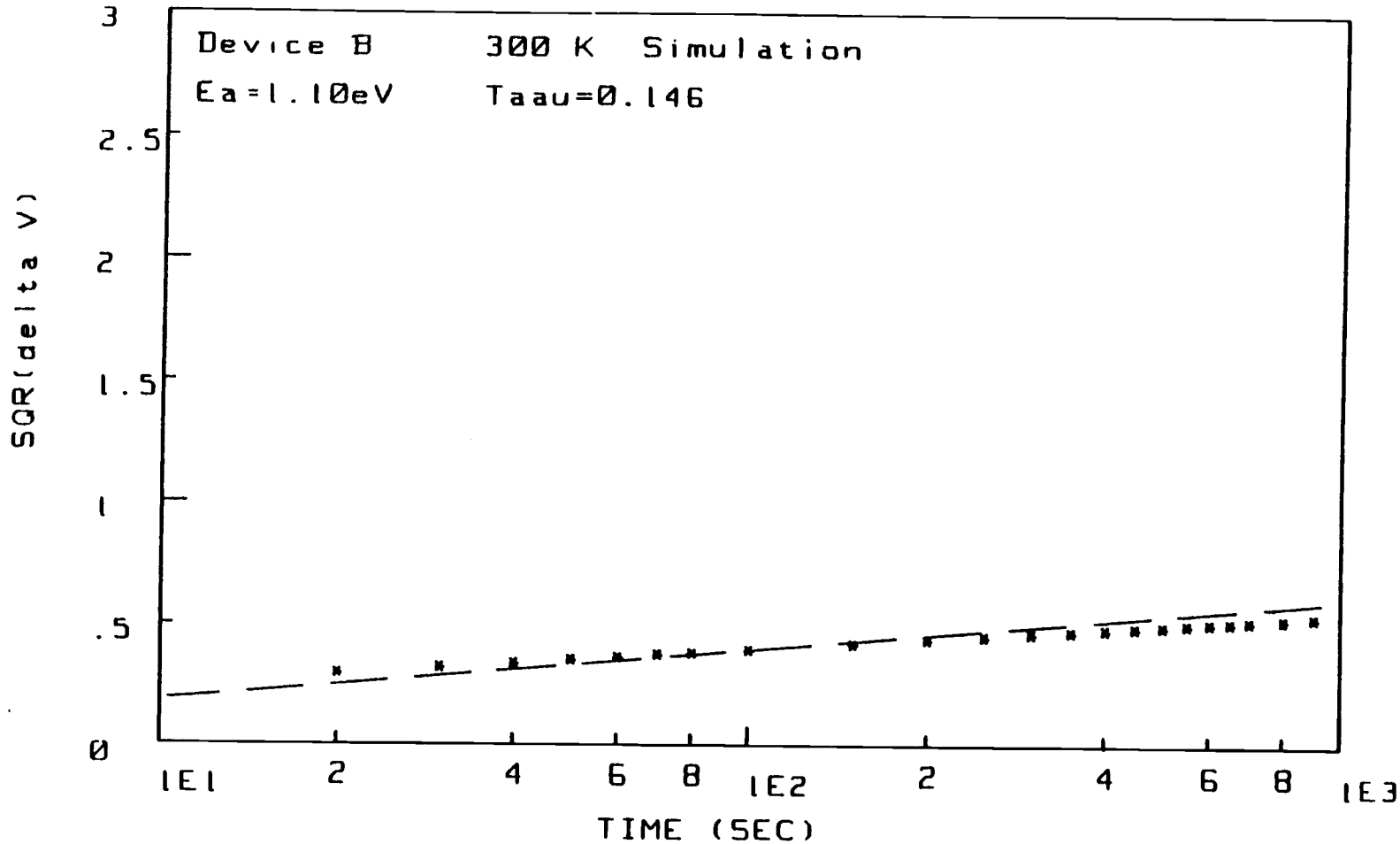


Fig. 5.3 Simulated shift of Vfb for device B at 300K, dashed line is the result from measurement. [Vp]=2E17.

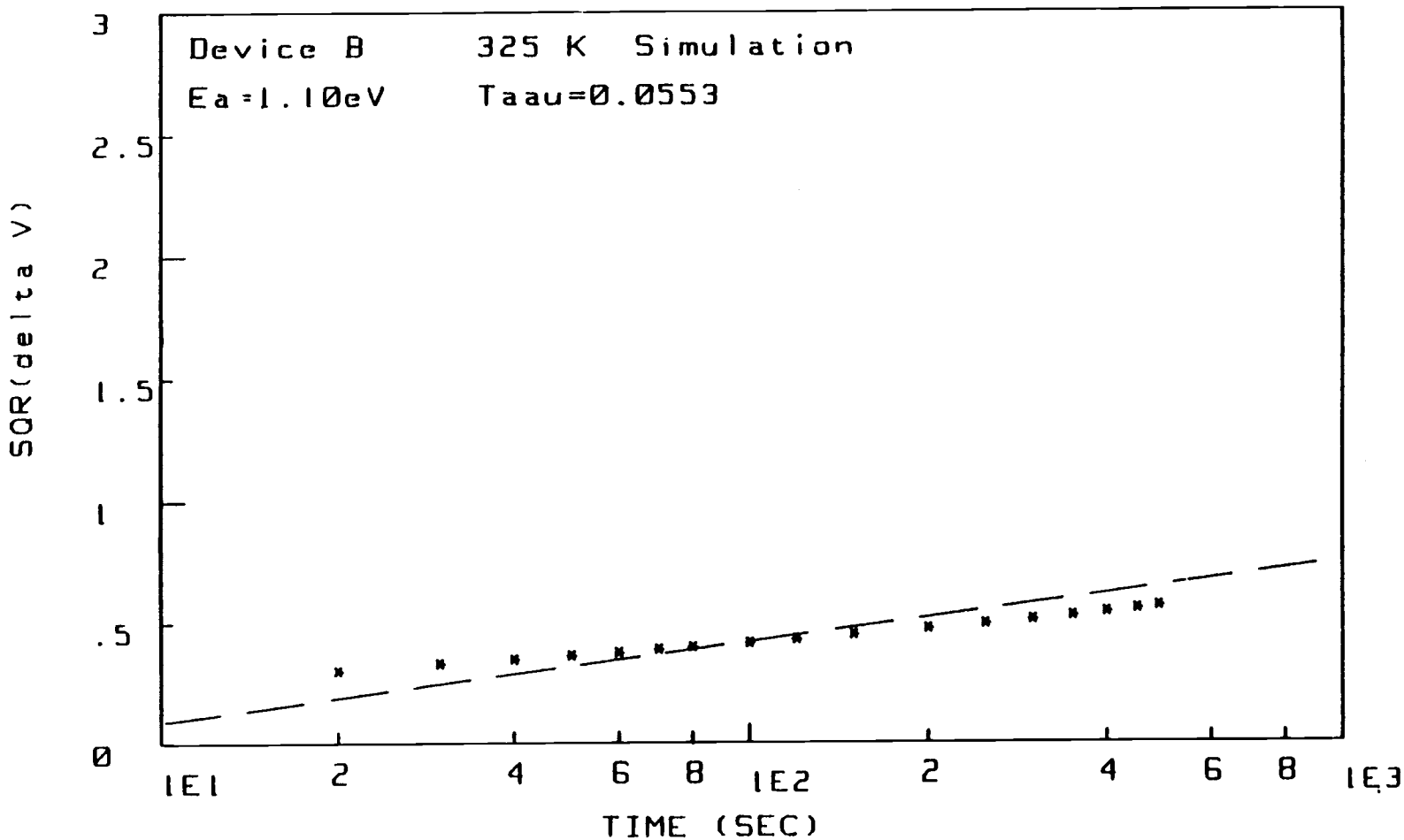


Fig. 5.4 **Simulated shift of Vfb for device B at 325K, dashed line is the result from measurement. [Vp]=2E17.**

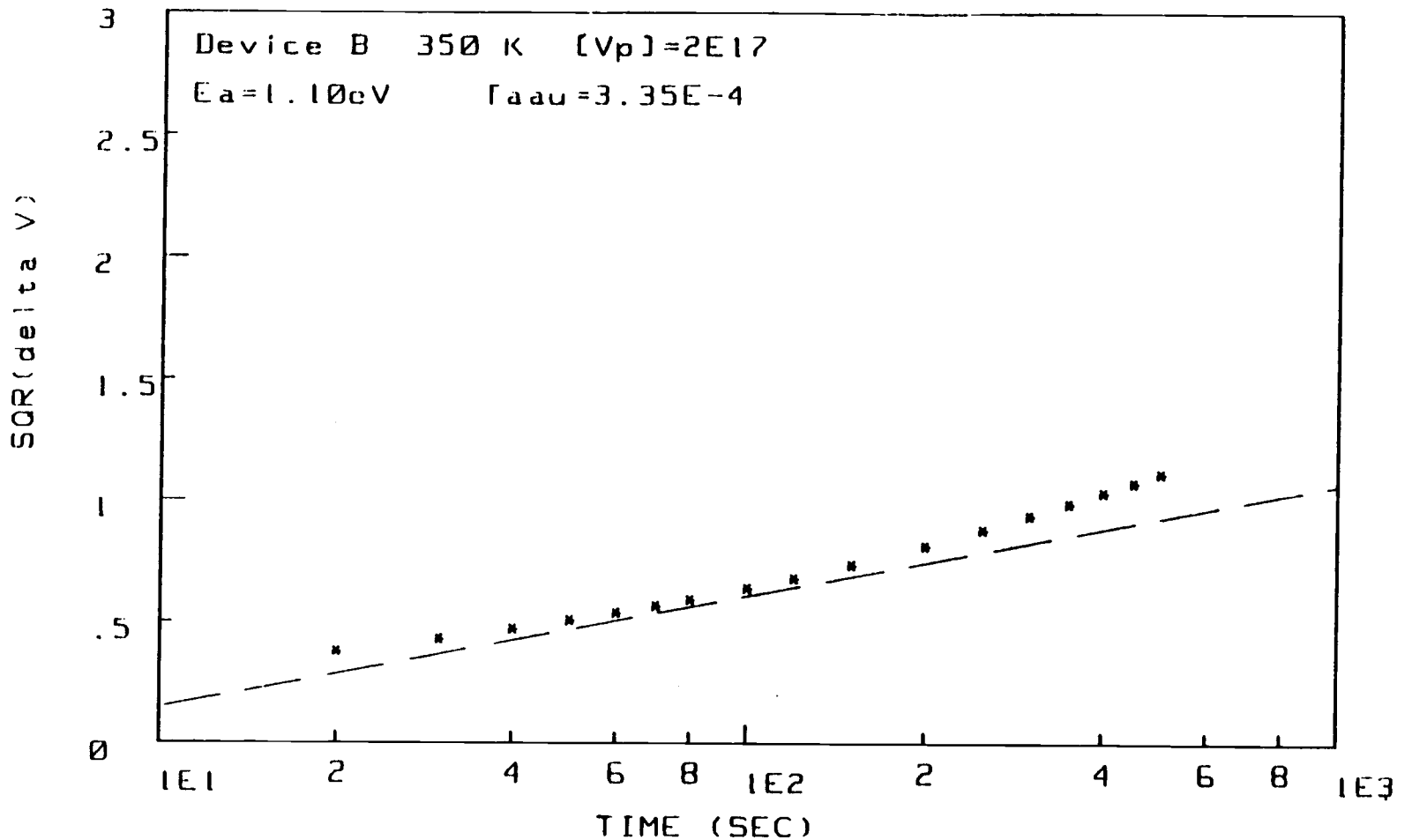


Fig. 5.5 Simulated shift of Vfb for device B at 350K, dashed line is the result from measurement. [Vp]=2E17.

T K	tsec	$\sqrt{\Delta Vfb}$ fitted from measur.	$\sqrt{\Delta Vfb}$ simulated	% devi.
350	60	0.5046	0.5351	+6.0
	120	0.6421	0.6767	+5.5
	240	0.7796	0.8603	+10.4
	480	0.9172	1.0863	+18.4
325	60	0.3499	0.3774	+7.0
	120	0.4500	0.4306	-4.3
	240	0.5502	0.4908	-10.8
	480	0.6504	0.5639	-13.3
300	60	0.3474	0.3591	+3.4
	120	0.4099	0.4016	-2.0
	240	0.4725	0.4444	-5.9
	480	0.5351	0.4877	-8.9

Table 5.1 Summary of simulated results and deviations.

mechanisms. A third possible reason for this deviation is that coulombic effects between the charged defects and between the defects and the electric field (e.g. the Poole-Frankel effect) have not been taken into consideration in the present formulation of the simulation.

The value ΔSm/k in equation 2.10 was chosen to be 15 in the simulation, which according to Van Vechten and Wager [8], is derived from:

$$\Delta Sm/k=\ln(8Do/\gamma a^2\nu o) \qquad (5.28)$$

where Do is the preexponential factor of the diffusion constant for In self-diffusion in InP, a=5.869Å is the lattice parameter, γ is a geometrical constant equal to 1.0, and νo is the attempt frequency. Using Do=1E5 cm/s reported by Goldstein [27], this gives ΔSm/k=17.5. But determination of Do from experiment is very difficult and there is always uncertainty in using this value. For this reason ΔSm/k is also considered an adjustable parameter in the simulation. Obviously, the vacancy concentration and ΔSm/k that can be chosen are not unique. Observation shows that if the vacancy concentration and time constants are all reduced by a factor of two, the simulation yields a almost completely identical result.

In the previous simulations, it is assumed that no electrons are initially trapped. If the initial density of trapped electrons was assumed to be 2E11cm^{-2}, this would

yield a much better fit, as shown in Fig.5.6.

Several other simulations were performed neglecting the effect of electrons trapped in the native oxide. Curves simulated in this way did not exhibit the experimentally observed linear behavior of the flat band shift. This indicates that coupling between the two instability mechanisms is important in establishing the flat band shift. Fig.5.7 shows the temperature dependence of the PVNNH mechanism, note that deviations from linearity occur at high temperatures in the simulation while the experimental curves exhibit linearity even at 350K. Effects of different vacancy concentrations and time constants are illustrated in Figs.5.8 and 5.9, smaller vacancy concentrations and time constants yield curves with more linear behavior. With a larger gate bias, the flat band shift is larger, as shown in Fig.5.10. A variation of the InP doping concentration does not have a strong effect on the amount of shift, as illustrated in Fig.5.11.

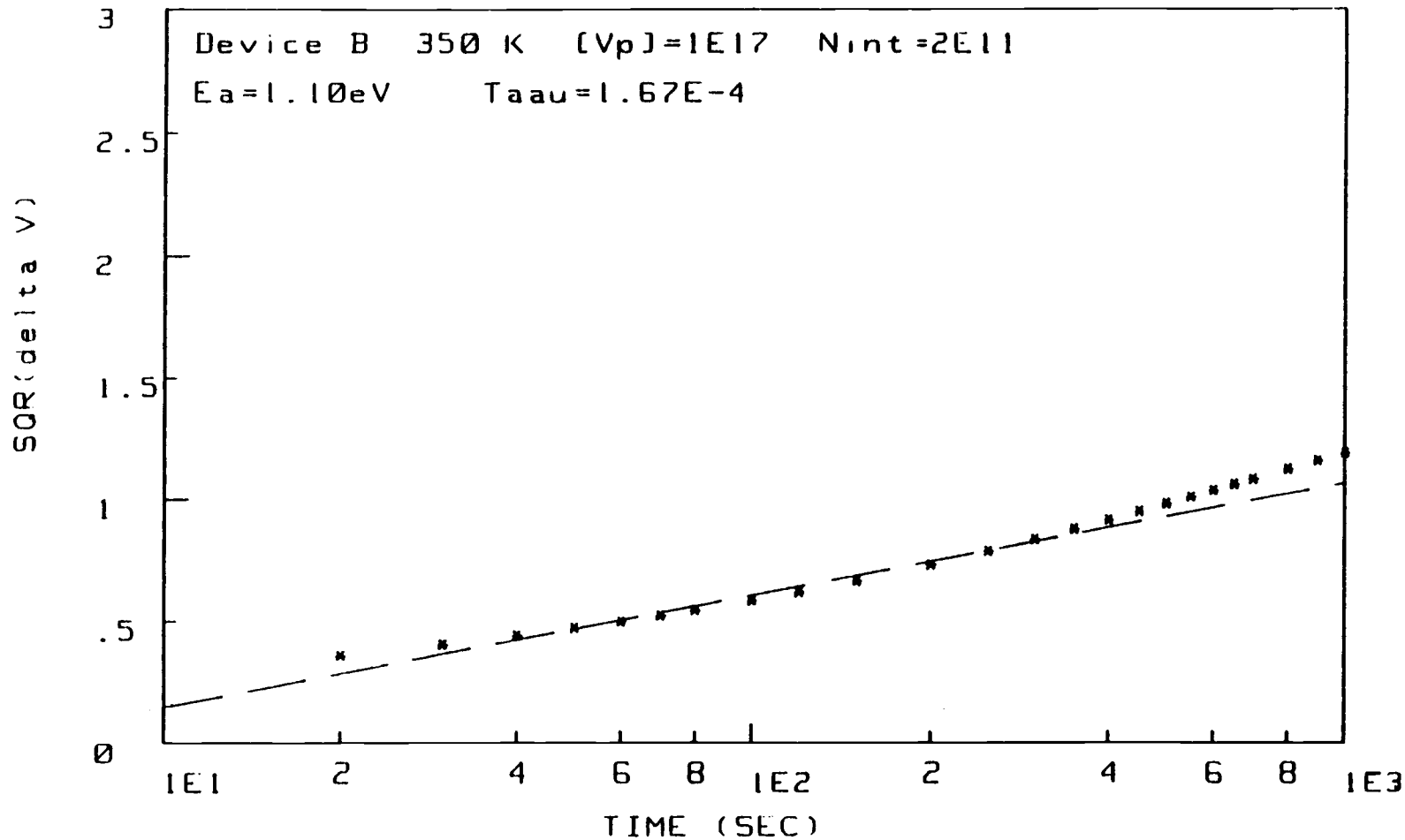


Fig. 5.6 Simulated shift with 2E11cm^{-2} initially trapped electrons.

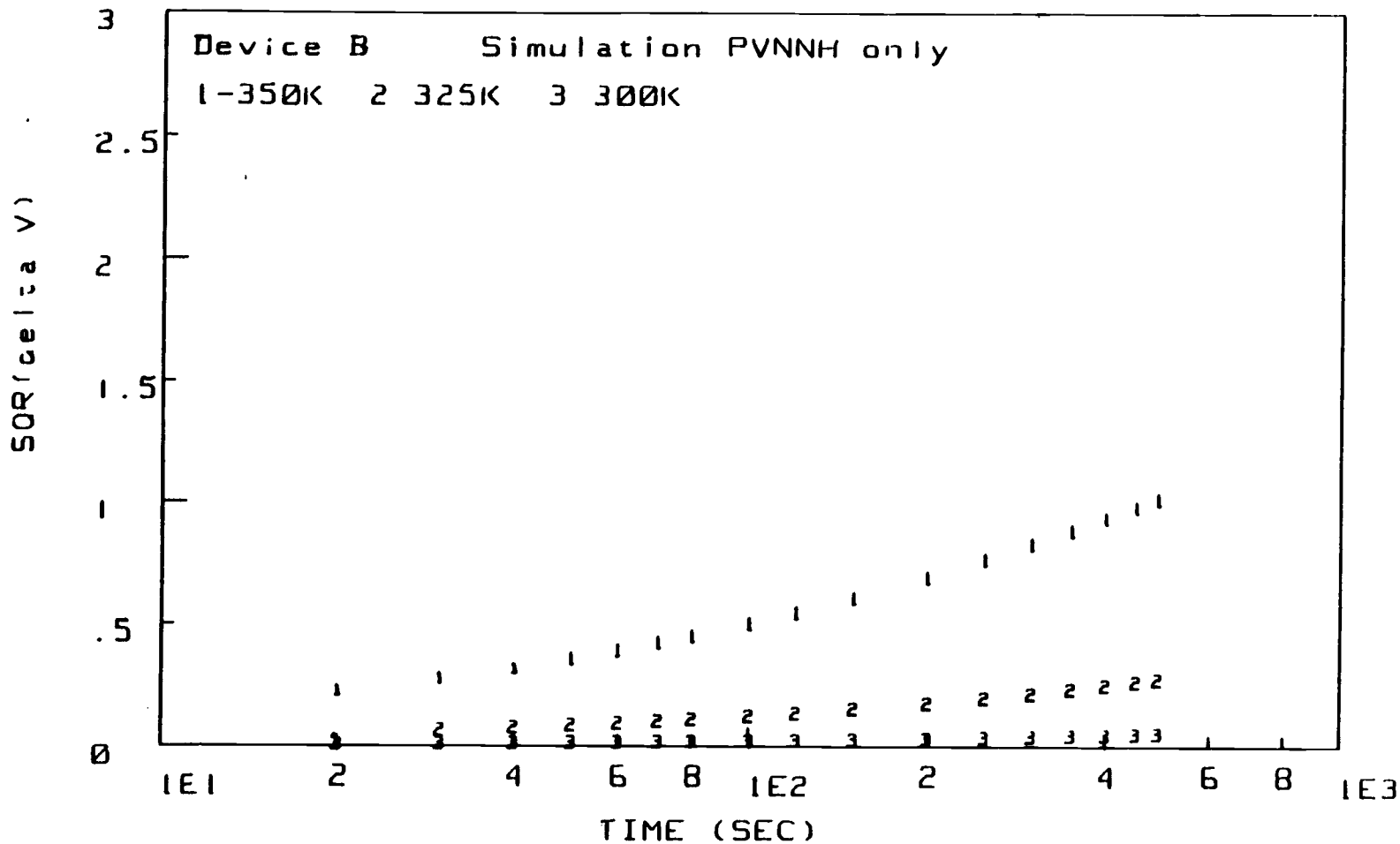


Fig. 5.7 Simulated amount of shift due only to PVNNH as a function of temperature.

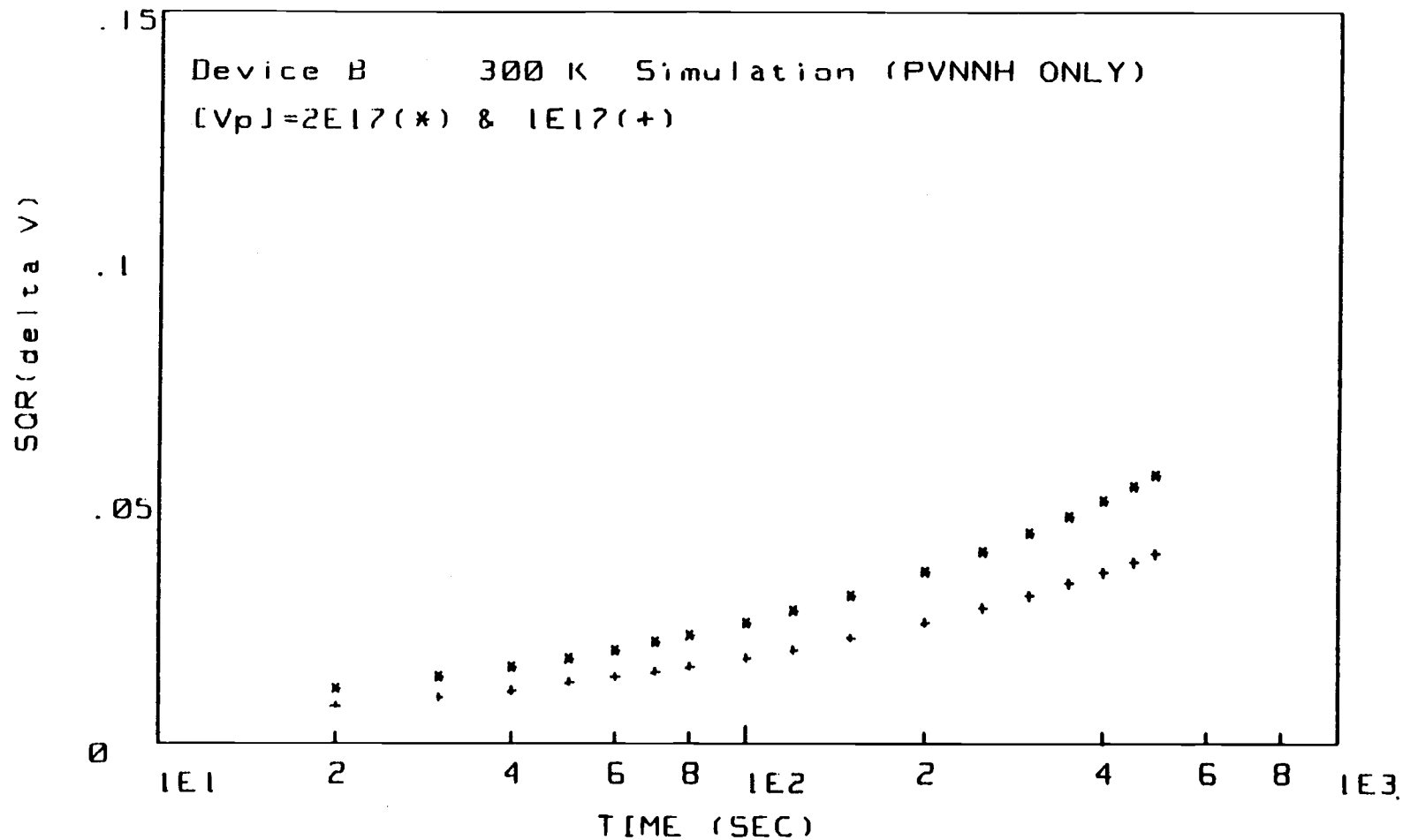


Fig. 5.8 Simulated amount of shift due only to PVNNH with different [Vp].

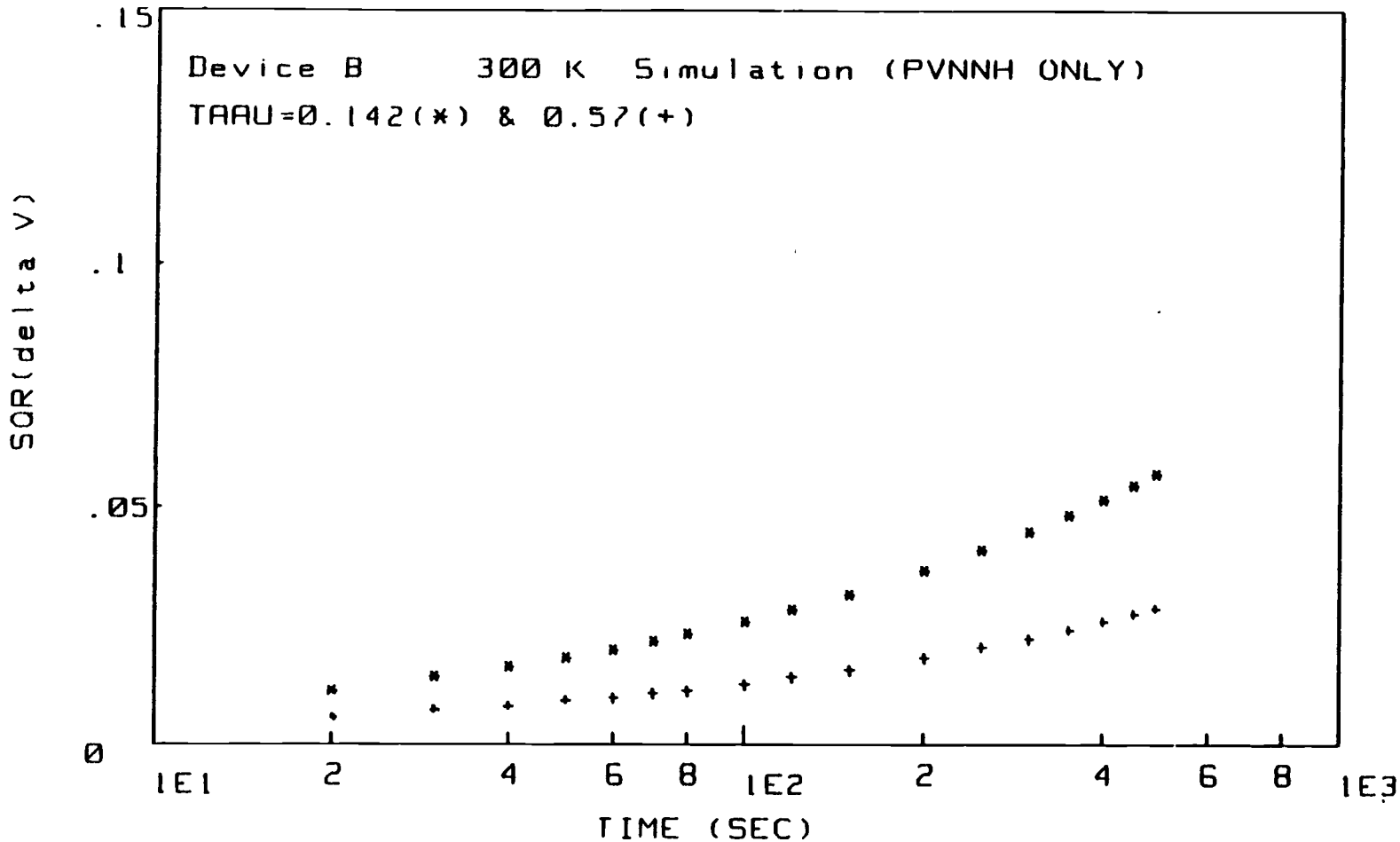


Fig. 5.9 Simulated amount of shift due only to PVNNH with different time constant.

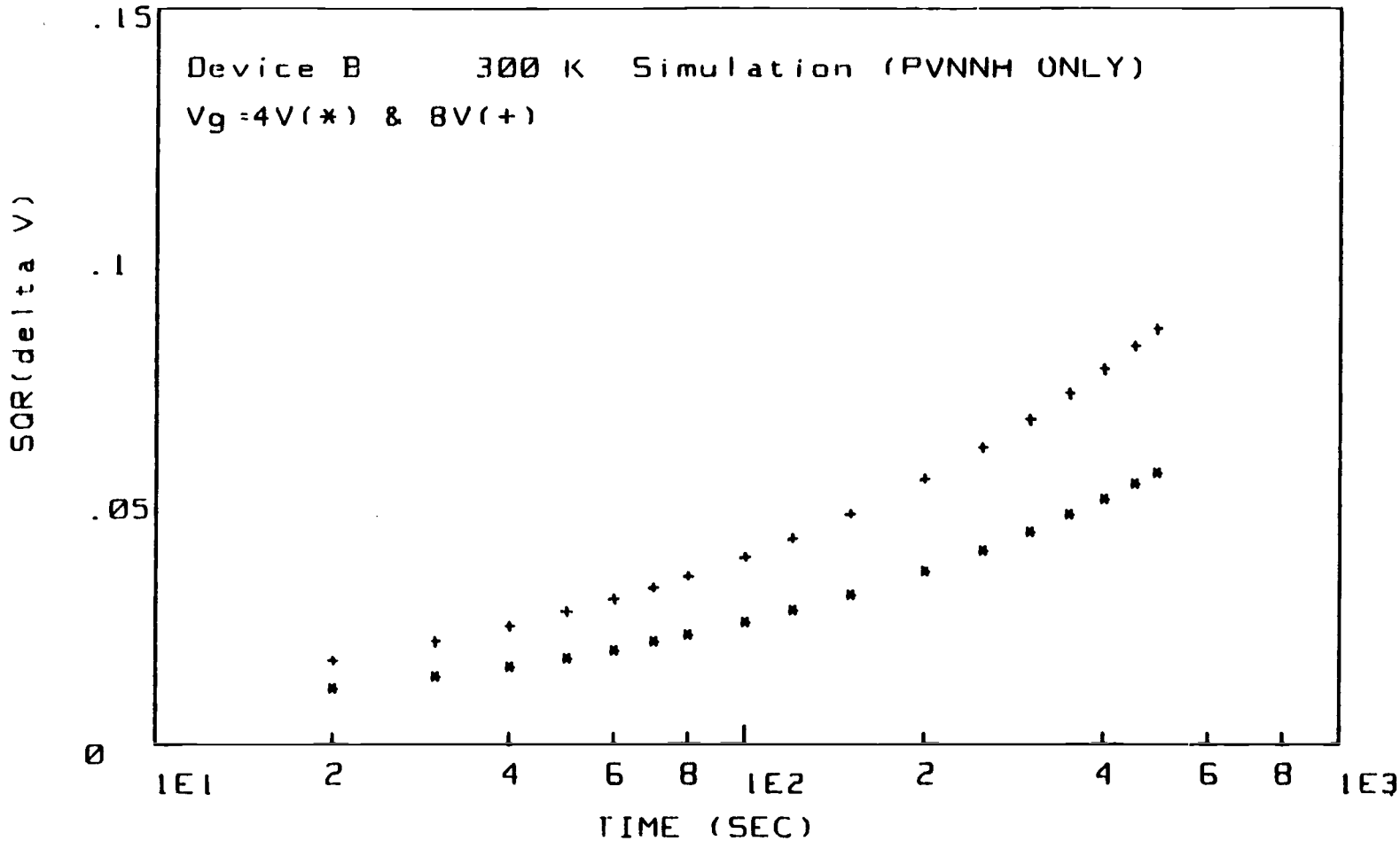


Fig. 5.10 Simulated amount of shift due only to PVNNH under different gate bias.

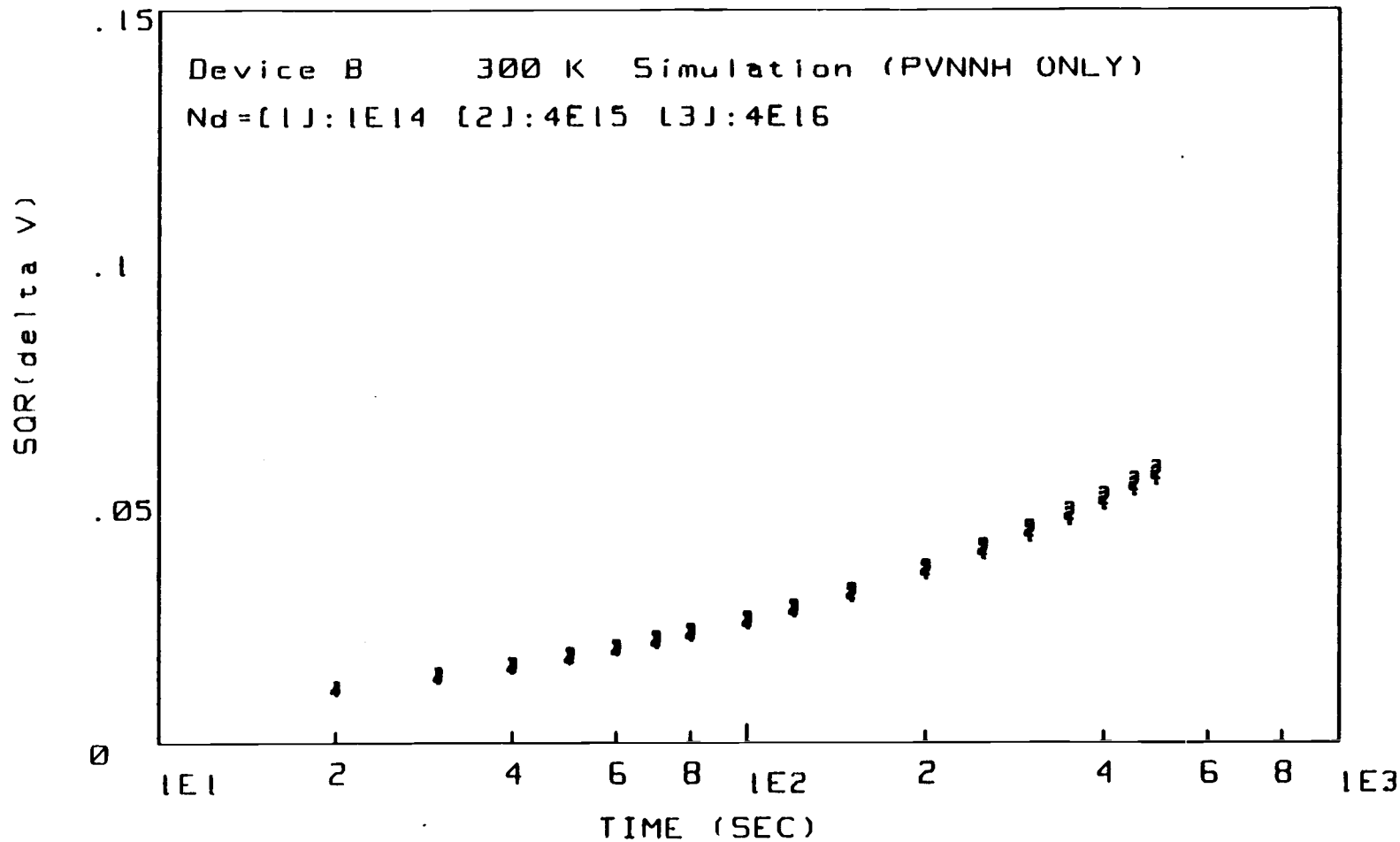


Fig. 5.11 Simulated amount of shift due only to PVNNH with different doping concentration in InP.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER WORK

The degradation in the drain current characteristics of InP MISFETs has been identified to be composed of contributions by at least two distinct mechanisms; anti-site defect complex formation which results from phosphorous vacancy nearest neighbour hopping, and electrons trapped in the native oxide. The corresponding activation energies are 1.1-1.2eV and 40-50meV, respectively. The estimated fraction of the flat band voltage shift in these particular samples at room temperature due to PVNNH is approximately 20%, which shows that the effect of PVNNH is very important in InP MISFETs, and would strongly influence the electrical characteristics of InP devices.

A computer simulation based on an analysis of the three step kinetics of the PVNNH defect reaction sequence agrees quite well with the experimental results. But certain deviations are observed at high temperature. This deviation may be due to nonlinear coupling between the two DCD mechanisms, coulombic effects of the charged defects which changes the reaction gate, or that more complicated defect complexes form by nearest neighbour hopping.

There are several important issues to consider for further development:

1. It has been reported [9,13] that specially

prepared InP MISFETs fabricated using a phosphorous over pressure have improved DCD characteristics. Variable-temperature bias-stress measurements of samples prepared in this manner should be performed in order to assess the extent of this improvement and to discern which DCD mechanism is associated with this improvement.

2. The 1.1-1.2eV activation barrier indicated in Fig.5.1 is inconsistent with the thermodynamic equilibrium values of the initial and final state of 1.78eV as calculated using the thermodynamic estimates [28] of Van Vechten. Refinements of this simple theory can be made [29] to account for defect-defect interactions so that the difference in the thermodynamic values of the initial and final state are consistent with the measured activation energy of 1.1-1.2eV. This would require that the equilibrium difference energy be less than 1.1-1.2eV.
3. The computer simulation could be refined to account for deviations in the simulated curve compared to the experimental curve at high temperature.

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