AN ABSTRACT OF THE THESIS OF

Tao Wang for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on May 29, 2012.

Title: Low-Power High-Resolution Delta-Sigma ADC Design Techniques.

Abstract approved:

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Gabor C. Temes

This dissertation presents a low-power high-resolution delta-sigma ADC. Two new architectural design techniques are proposed to reduce the power dissipation of the ADC. Compared to the conventional active adder, the direct charge transfer (DCT) adder greatly saves power by keeping the feedback factor of the active adder unity. However, the inherent delay originated from the DCT adder will cause instability to the modulator and complex additional branches are usually needed to stabilize the loop. A simple and power-efficient technique is proposed to absorb the delay from the DCT adder and the instability issue is therefore solved. Another proposed low-power design technique is to feed differentiated inverted quantization noise to the input of the last integrator. The modulator noise-shaping order with this proposed technique is effectively increased from two to three without adding additional active elements.

The delta-sigma ADC with the proposed architectural design techniques has been implemented in transistor-level and fabricated in 0.18 μm CMOS technology. Measurement results showed a SNDR of 99.3 dB, a DR of 101.3 dB and a SFDR of 112 dB over 20 kHz signal bandwidth, resulting in a very low figure-of-merit (FoM) in its application category. Finally, two new circuit ideas, low-power parasitic-insensitive switched-capacitor integrator for delta-sigma ADCs and switched-resistor tuning technique for highly linear Gm-C filter design are presented.

Low-Power High-Resolution Delta-Sigma ADC Design Techniques

by
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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Tao Wang, Author

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DEDICATION

I dedicate this dissertation to both my parents. My father, Benyi Wang did not only raise me up but also taxed himself dearly to support my education and intellectual development. He met his demise during my PhD study and had sacrificed himself so much to keep me undistracted. My mother, Jiqing Song has been a source of motivation that propels me to my goals. Her undeniable, unconditional and unselfish love has nourished my life with lots of good qualities.

In Memory of My Father

Chapter 1 Introduction

The cost of digital signal processing (DSP), compared to analog signal processing (ASP), generally decreases with lower power supplies and smaller feature sizes from advanced technologies. The reusability of codes used to automatically synthesize DSP circuits is usually very high between different technologies. DSP compared to ASP can also implement more complicated and robust functions and there is no need to tune analog components such as R, L and C. The real world, however, is full of analog signals such as sound, video, light and temperature. To make DSP possible, analog signals have to be first converted to digital signals. Analog-to-digital converter (ADC) plays an important role in signal processing by performing analog-to-digital conversion. Depending on the applications, ADCs could have different signal bandwidths (BWs) and resolutions.

1.1 Motivation

Medium to high resolution sensor applications are becoming more and more widespread [1-1][1-2][1-3]. Examples include electrocardiogram (ECG), electroencephalography (EEG), strain gauge, gas detector, differential pressure transducer, weighing sensor, etc. A complete analog-front-end (AFE) is often needed in these applications to convert small analog signals to be measured to digital signals which carry the input information and will be processed by DSP circuits.

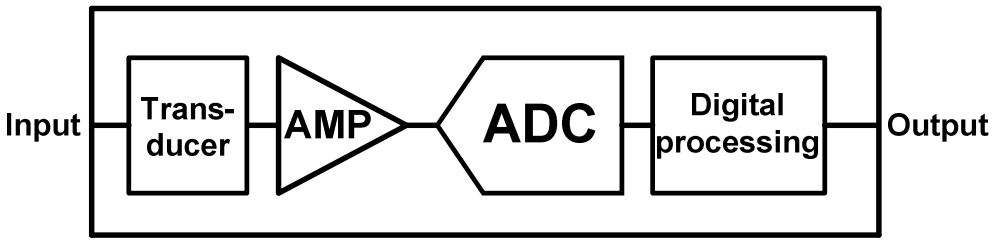

Figure 1-1. Analog-front-end composition.

Fig. 1-1 shows the composition of a typical AFE. The transducer is used to convert physical signals to be measured to voltage, current or charge. Usually the converted signal is very weak in amplitude and needs to be amplified by the amplifier which could be a programmable gain amplifier (PGA) or a low noise amplifier (LNA), before being converted to digital signal by the ADC following the amplifier. A small-scale digital circuit may also be included for interfacing with DSP circuits.

The sensors containing AFE are usually portable and powered by battery. Therefore, low-power operation is very crucial in these sensor applications. The ADC is the core of the AFE and consumes considerable amount of the AFE total power. The conversion accuracy required in some sensor applications could be as high as 16 bits. Compared to audio applications, absolute accuracy (offset, offset temperature drift, gain error, gain error temperature drift) is also important. Developing low-power high-resolution ADC structures for sensor applications becomes the design target of the thesis work.

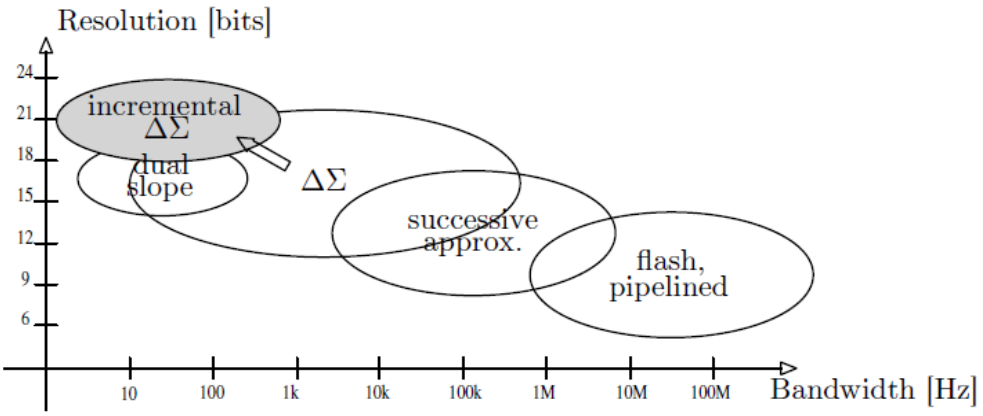

Figure 1-2. Applications of A/D converter structures for typical resolution and bandwidth requirement

Although the signal bandwidth could be designed up to one half of the clock frequency for Nyquist-rate ADCs (pipelined ADCs, flash ADCs, interpolating ADCs, etc), the achievable effective number of bits (ENOB) rarely exceeds 15 bits, even with sophisticated analog and digital calibration schemes. Shown in Fig. 1-2 [1-4], compared to Nyquist-rate ADC, delta-sigma ADC and incremental ADC is well-known for their

capability of achieving very high conversion resolution (≥16 bits) with less accurate analog building blocks [1-4]-[1-14]. This comes with the price of reduced signal bandwidth or increased clock frequency.

1.2 Thesis Organization

The remainder of the thesis is organized as follows. Chapter 2 discusses some existing design techniques for low-power high-resolution ADCs and introduces the proposed delta-sigma ADC architecture featuring two new low-power design techniques. Chapter 3 shows the circuit implementation of the proposed DSADC. Main building blocks such as first integrator, second integrator, DCT adder, 15-leve internal quantizer, DWA logic, are described in details. Chapter 4 deals with evaluation board setup and chip measurement results. Two new design techniques are introduced in chapters 5-6. Chapter 5 describes a low-power parasitic-insensitive switched-capacitor integrator for delta-sigma ADCs. A switched-resistor tuning technique for highly linear Gm-C filter is presented in chapter 6. Chapter 7 concludes this PhD dissertation.

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Chapter 2 Design Techniques for Low-Power High-Resolution ADCs

2.1 Delta-Sigma Modulation Techniques

2.1.1 Oversampling Technique

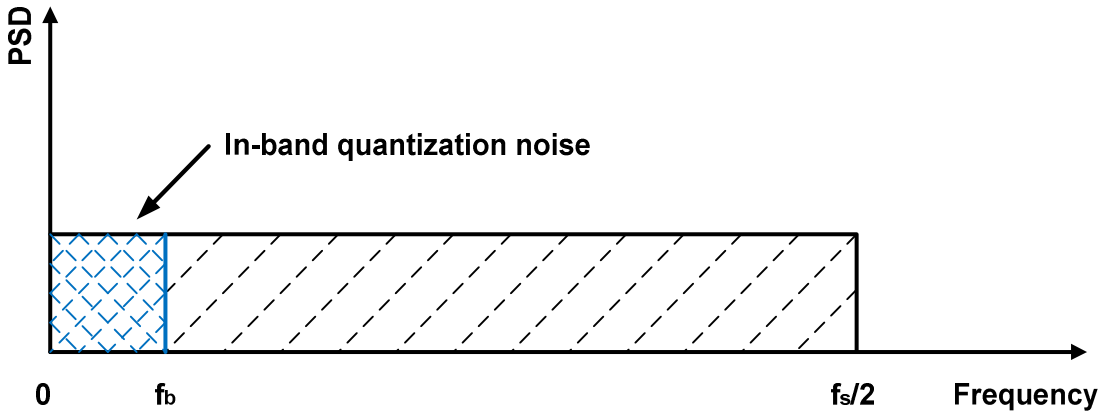

Fig. 2-1. PSD reduction of quantization noise by using oversampling technique.

The oversampling ADC usually samples the input signal at frequencies much higher than Nyquist frequency and trades conversion speed for conversion accuracy. Fig. 2-1 shows how the quantization noise power spectral density (PSD) of the ADC gets reduced by oversampling technique. The rectangular area representing the total quantization noise power is unchanged regardless of different sampling frequencies. However, the PSD of the quantization noise gets reduced with increased sampling frequency. The integrated quantization noise power from DC to fixed frequency of interest f_b also gets reduced. The ratio of sampling clock frequency over Nyquist frequency is called the oversampling ratio (OSR). Every doubling of sampling frequency halves the quantization noise spectral density and improves SNR by 3dB [2-1].

2.1.2 Noise-Shaping Technique

Another way of suppressing quantization noise is to use noise shaping technique [2-2]. Fig. 2-2 shows the general single feedback delta-sigma modulator topology which shapes

quantization noise to out-of-band frequencies. The modulator output $V_{out}(z)$ is a weighted combination of signal input $V_{in}(z)$ and quantization error Q(z),

$$V_{out}(z)=V_{in}(z)\times H(z)/(1+H(z))+Q(z)/(1+H(z))=V_{in}(z)\times STF(z)+Q(z)\times NTF(z) \quad (2\text{-}1)$$

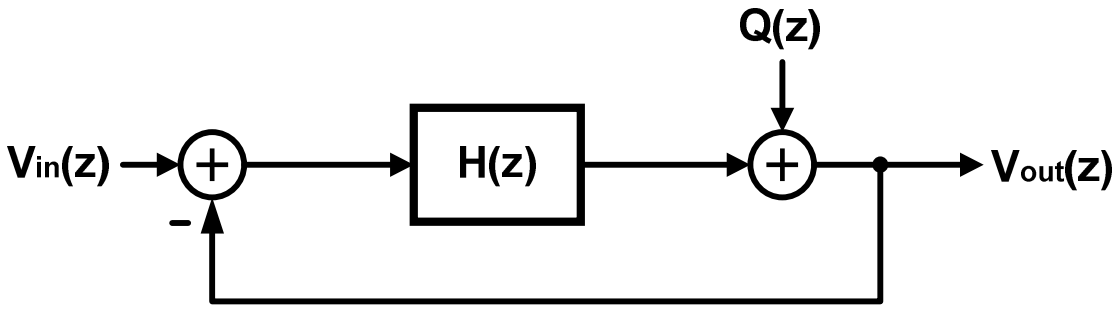

Fig. 2-2. General single feedback delta-sigma modulator topology.

STF(z) stands for the signal transfer function in z-domain and NTF(z) is short for noise transfer function in z-domain. |STF(z)| is usually near unity in the signal bandwidth and can be compensated in the digital post processing. For a low-pass delta-sigma modulator, |NTF(z)| shows a high-pass function and filters out most of the low-frequency energy of the quantization noise. Fig. 2-3 shows the high-pass function from the NTF of the low-pass delta-sigma modulator.

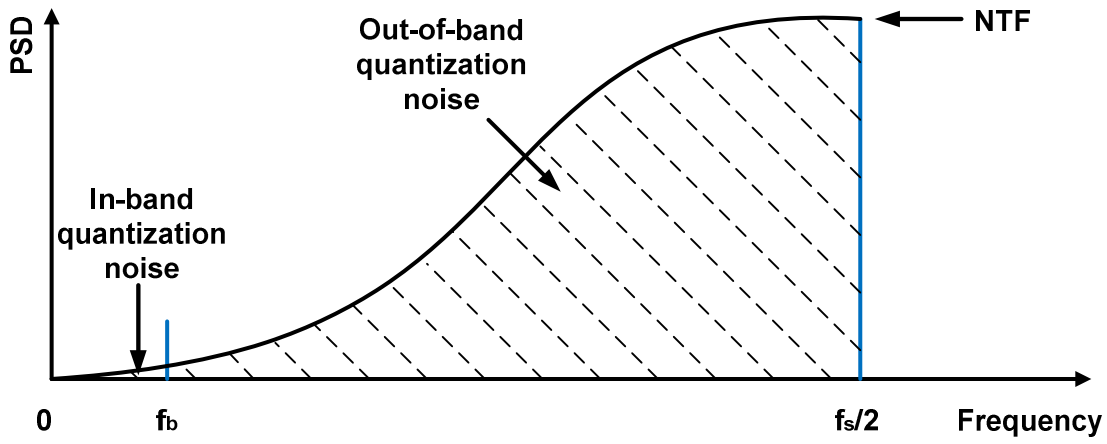

Fig. 2-3. High-pass function from the NTF of the low-pass delta-sigma modulator.

Combining the advantages of oversampling technique and noise-shaping technique, oversampling delta-sigma ADC makes good trade-offs between speed and accuracy and the achievable accuracy could be over 16 bits.

2.2 Design Considerations for High-Resolution ADCs

2.2.1 Incremental ADC vs. Delta-Sigma ADC

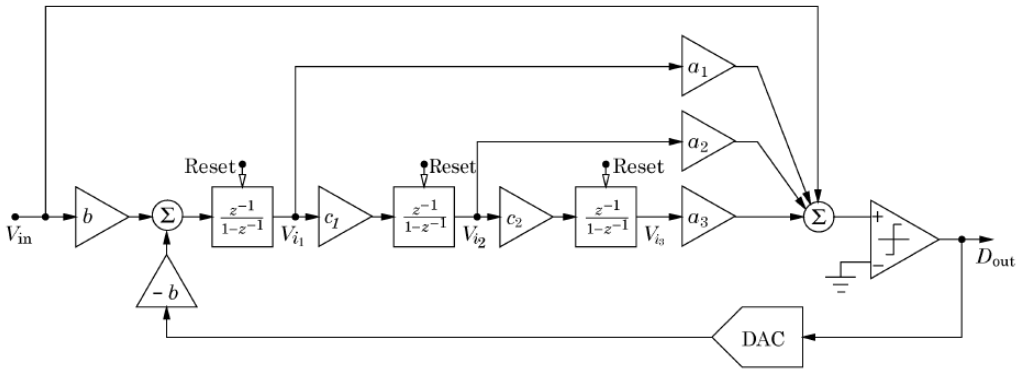

Fig. 2-4. Block diagram of a high-order feed-forward incremental ADC.

Fig. 2-4 shows the block diagram of a high-order feed-forward incremental ADC [2-3]. The working principle of the incremental ADC is similar to that of the oversampling delta-sigma ADC. However, they differ in a few ways: The decimation filter of the incremental ADC can be as simple as a cascade of a few integrators, while for delta-sigma ADC there is no straightforward design for decimation filter; it is easy for incremental ADC to be time-interleaved, while for delta-sigma ADC complicated post processing circuitry may be needed; compared to delta-sigma ADC which operates continuously, incremental ADC needs additional switches and digital logic circuitry to periodically reset its internal memories for normal operation; for the same modulator parameters such as loop order, OSR and internal quantizer resolution, incremental ADC suffers SNR loss because the order of digital decimation filter is usually one order less than that of its counterpart [2-4].

2.2.2 Discrete-Time vs. Continuous-Time

Opamps are usually employed in discrete-time (DT) switched-capacitor (SC) delta-sigma ADC to build up integrators. The opamp loop unit-gain-bandwidth (UGB), controlled by the feedback factor and the opamp open-loop UGB, usually needs to be a few times the sampling clock frequency to settle opamp output to the desired accuracy. For continuous-time (CT) delta-sigma ADC, however, waveforms change continuously and the restriction on opamp loop UGB is usually relaxed. Therefore, CT delta-sigma ADC usually can be clocked 3 to 5 times faster than its counterpart for the same sampling clock frequency [2-5].

The anti-aliasing filter which consumes a considerable amount of power is usually needed before the input to the DT delta-sigma ADC to suppress signals around multiples of the sampling clock frequency. For CT delta-sigma ADC, the requirement for the anti-aliasing filter can be greatly relaxed or even eliminated, since CT delta-sigma ADC has inherent anti-aliasing characteristic.

However, there are a few reasons why DT delta-sigma ADC is preferred in high-resolution applications over its CT counterpart. The sampling in DT delta-sigma ADC happens at the signal input and only the input is affected by the clock jitter. The sampling in CT delta-sigma ADC, in contrast, happens at the input of the internal quantizer, which means the jitter affects the sum of the input plus quantization noise. Most of the charge in DT delta-sigma ADC is transferred at the start of the clock phase and the error of the total amount of charge transferred in one clock phase due to clock jitter is usually very small. For CT delta-sigma ADC, charge is usually transferred at a constant rate over the clock phase so the charge error due to jitter is relatively large compared to DT case [X]. Therefore, CT delta-sigma ADC is usually more sensitive to clock jitter than its DT counterpart. For high-resolution ADC applications, the requirement on clock jitter performance for CT delta-sigma ADC is very stringent [2-6].

The RC time constant of the CT delta-sigma ADC usually needs to be tuned to make sure the modulator loop is stable and the signal-to-quantization noise ratio (SQNR) is not

severely degraded. For DT SC delta-sigma ADC, the loop coefficients are dependent on the capacitor matching which could be very accurate. Therefore, DT delta-sigma ADCs are usually robust and insensitive to capacitor value variations.

The voltage coefficient (VC) of the metal capacitor may be a lot better than that of the resistor. The sampling linearity at the input of the first integrator puts an upper limit to the overall achievable linearity of the modulator. For high-resolution applications, metal capacitor with very good VC will not limit the possible maximum input to the modulator and the nonlinearity contributed by the metal capacitor can be negligible.

2.2.3 Loop Configuration Optimization

Single-loop modulator is usually preferred over multi-stage noise-shaping (MASH) ADC in low-bandwidth high-resolution applications because quantization noise is easily suppressed by the NTF with high OSRs. MASH ADC is especially useful where OSR of the modulator is limited by the achievable sampling clock frequency and the power dissipation budget [2-7]-[2-11]. MASH ADC, however, usually suffers from the mismatch of analog NTF and digital NTF and calibration is needed to achieve high resolution.

High-order modulator can be easily built up by replacing the internal quantizer with a first-order delta-sigma modulator. More aggressive noise-shaping can be obtained from a high-order modulator, compared to a first-order modulator. To get the same quantization noise suppression for high resolution application, a high-order modulator may only need a reasonably low OSR, while for a first-order delta-sigma modulator a huge OSR is not surprising. High-order modulators also suffer less from idle tones, compared to a first-order modulator.

Multi-bit internal quantizer offers a better white noise quantization noise approximation and gets more aggressive noise shaping than its single-bit counterpart, although feedback DAC linearity has to be corrected by dynamic element matching (DEM) techniques [2-12]-[2-26].

2.3 Proposed Low-Power Delta-Sigma ADC

The analog power supply of the application is 5V. The resolution required is at least 16-bit effective number of bits (ENOB) over a signal bandwidth of 20kHz. The technology available is 0.18um CMOS technology. The proposed delta-sigma ADC architecture is shown in Fig. 2-5 below. A third-order 15-level internal quantizer discrete-time delta-sigma modulator loop is employed to get enough quantization noise suppression. The simulated SQNR of the proposed delta-sigma ADC is over 120dB. The OSR of the delta-sigma modulator is 64. Low-distortion feed-forward structure [2-27] is especially power-efficient in high-resolution delta-sigma ADC since the output of each integrator contains only quantization noise. Fig. 2-6 shows the circuit diagram of the proposed ADC. To reduce the power dissipation of the ADC, two new techniques are proposed.

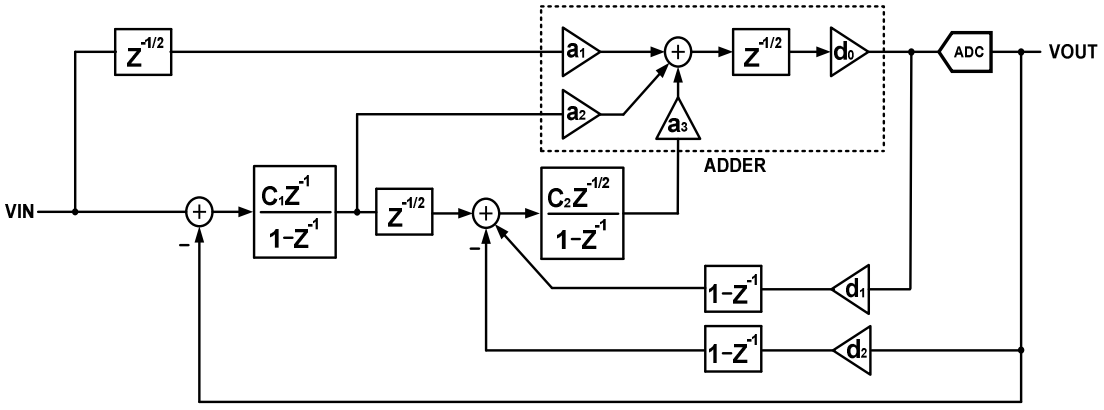

Fig. 2-5. Architecture of the proposed low-power delta-sigma ADC.

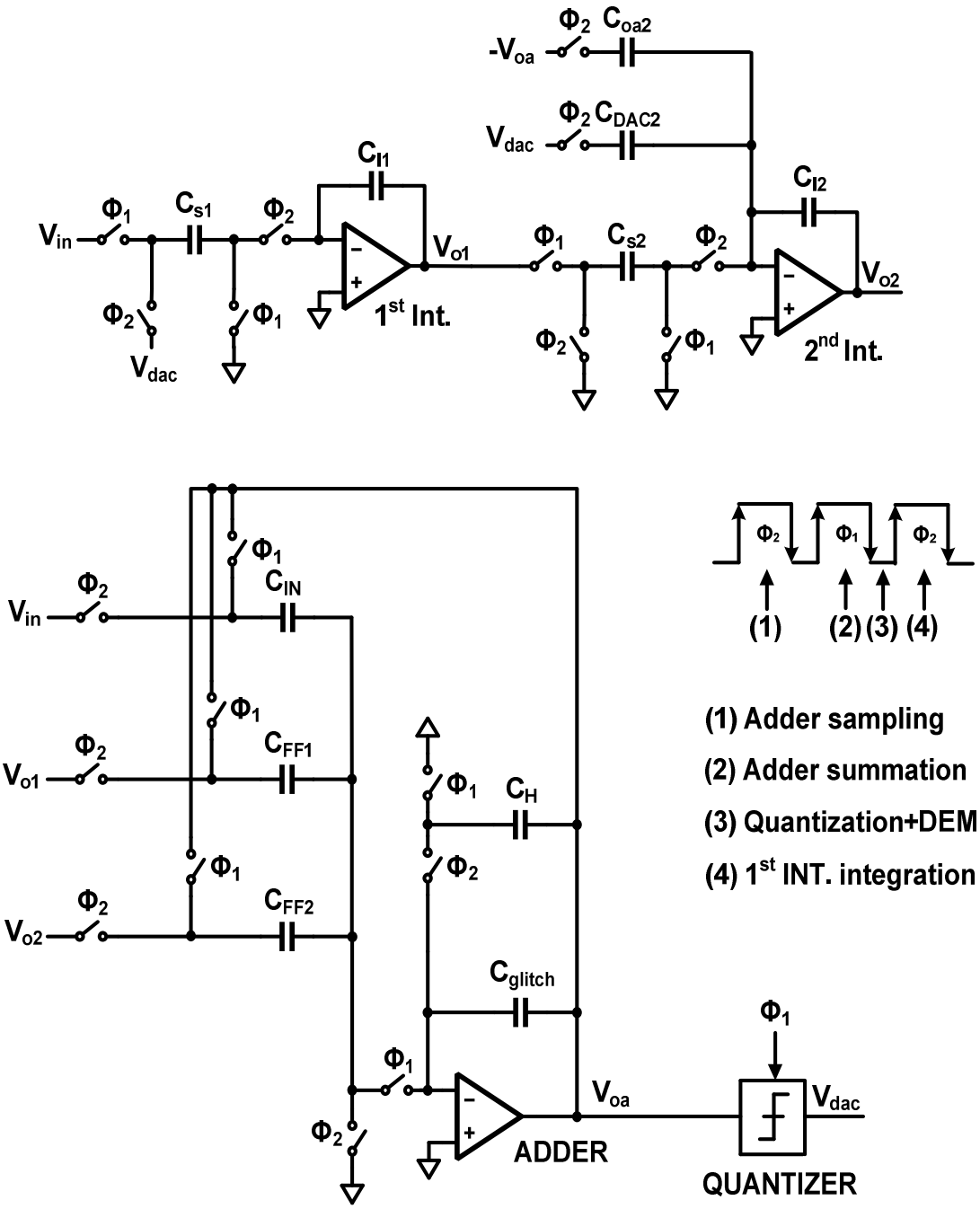

Fig. 2-6. Circuit diagram of the proposed delta-sigma ADC.

2.3.1 DCT Adder with Modified Timing

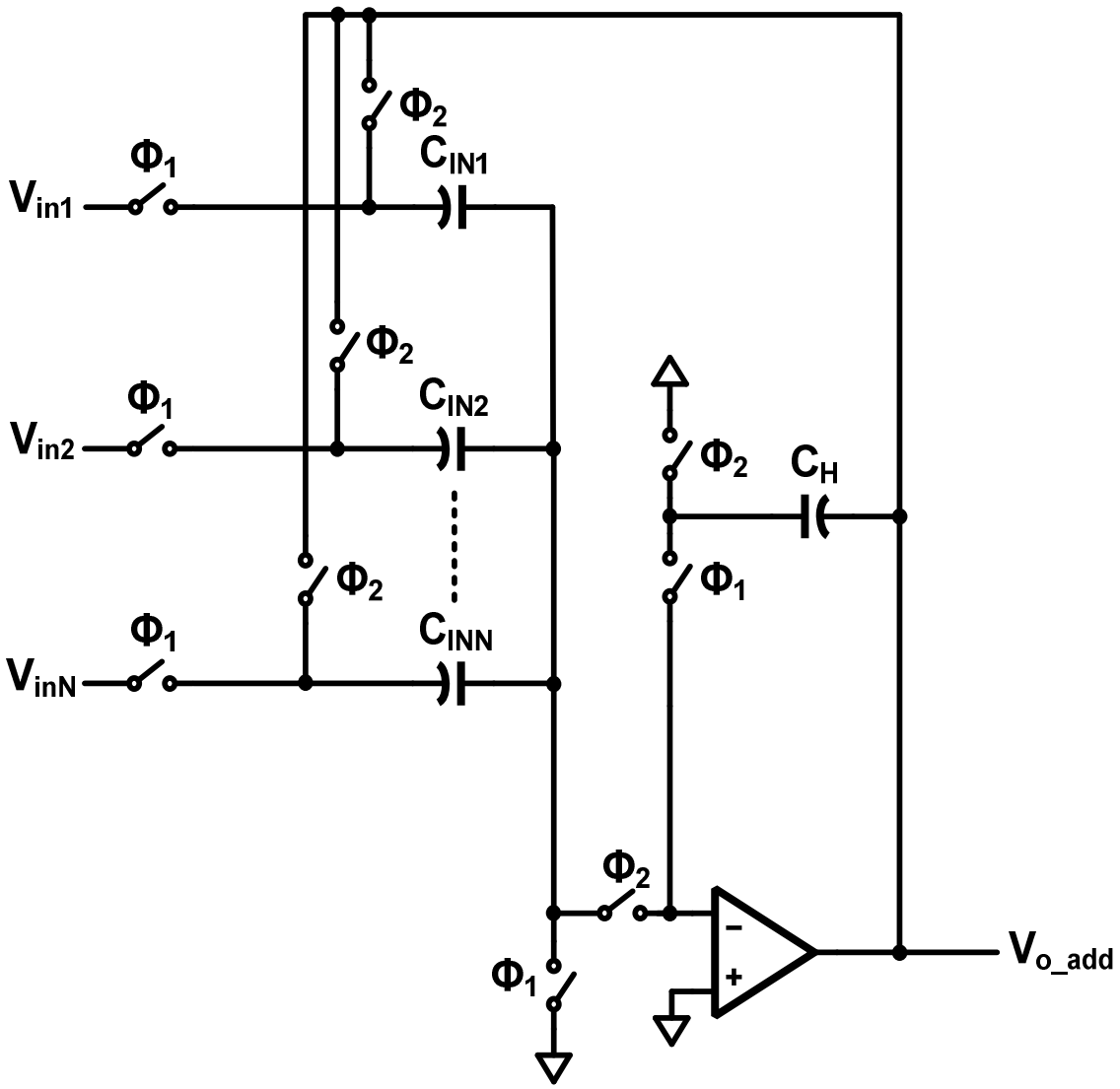

Fig. 2-7. DCT adder.

Fig. 2-7 shows the circuit diagram of the DCT adder [2-28]. During phase Φ_1, all sampling capacitors sample their corresponding input signals onto the bottom plates. During phase Φ_2, all the bottom plates are connected to the output of the adder. The

charge stored on these sampling capacitors is shared and the adder output is a weighted sum of the sampled input voltages. Capacitor C_H samples the current adder output and forms the hold capacitor across the opamp input and output during phase Φ_1. The feedback factor during phase Φ_2 is ideally unity. In real transistor-level implementation, however, metal wire routing, opamp input parasitic capacitors, switches parasitic capacitors and sampling capacitors parasitic capacitors slightly degrade the loop UGB by reducing the feedback factor. The adder samples its input voltages during phase Φ_1 and outputs the sum at the end of phase Φ_2, which introduces an inherent half sampling clock cycle delay.

The active adder needed for the feed-forward structure usually consumes a considerable amount of the total power due to its small feed-back factor, especially for the feed-forward structure. Compared to the conventional active adder, DCT adder greatly saves power by keeping the feedback factor of the active adder unity and the opamp used does not participate in the charge redistribution. However, the inherent delay originated from the DCT adder will cause instability to the modulator and usually complex additional branches are employed to stabilize the modulator loop.

A simple and power-efficient scheme is proposed to absorb the delay from the DCT adder. Shown in Fig. 2-6, the DCT adder performs the addition in phase Φ_2, instead of phase Φ_1, which is the case for the conventional active adder for the delta-sigma ADC. Thus, half sampling clock cycle delay is implemented for the signal feed-forward path [2-29] and the associated modulator instability issue is eliminated without requiring extra compensation branches [2-30]. The capacitors from the quantizer are connected to the adder output during phase Φ_1 as the partial load.

2.3.2 Noise-Shaping Enhancement Technique (NSET)

To further reduce the power dissipation of the modulator, a NSET is also proposed. The underlying principle of NSET is similar to noise-coupling technique shown in Fig. 2-8 [2-31][2-32].

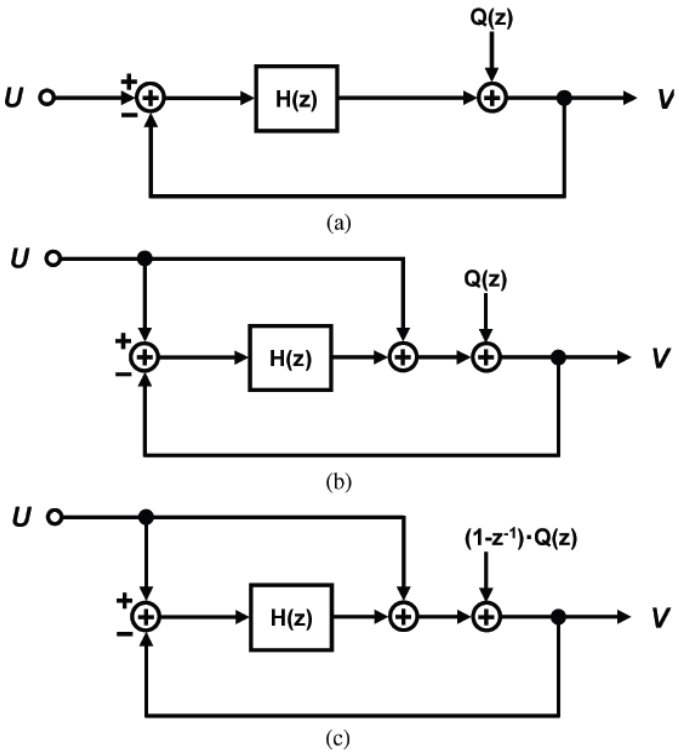

Fig. 2-8. Principle of noise-coupling technique: (a) Conventional delta-sigma modulator. (b) Low-distortion delta-sigma modulator. (c) Low-distortion delta-sigma modulator with first-order noise-coupling.

Fig. 2-8(a) shows the conventional delta-sigma modulator. Fig. 2-8(b) shows the low-distortion delta-sigma modulator by adding a signal feed-forward path to the adder. Fig. 2-8(c) introduces the noise-coupling technique based on Fig. 2-8(b). Noise-coupling technique replaces the quantization noise item Q(z) in the transfer function with high-pass filtered quantization noise which in this case is $(1-Z^{-1})Q(z)$. The transfer function expresses the modulator output as a combination of the signal input and quantization noise. Therefore, the effective noise-shaping order is increased without adding extra integrators. Noise-coupling technique uses less active elements to implement the same NTF and therefore saves power. Higher-order noise-coupling could also be implemented by adding more branches.

However, if noise-coupling is applied to the adder, the DCT adder has to be modified and the feedback factor will be greatly reduced. As shown in Fig. 2-5, the differentiated inverted quantization noise is fed to the input of the second integrator and then integrated. The output of the second integrator therefore contains delayed inverted quantization noise. The noise-shaping order of the proposed structure is effectively increased from two to three by properly choosing the modulator coefficients d_0, d_1, d_2, c_2 and a_3. The differentiated quantization noise is implemented by charging floating capacitors shown in Fig. 2-6, where CDAC2 is a set of 14 small unit capacitors.

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Chapter 3 Circuit Implementation

3.1 Integrator Design

3.1.1 First Integrator

Fig. 3-1 shows the circuit diagram of the first integrator. The timing of the first integrator is shown in Fig. 3-2. Switches S_1 and S_2 are closed during phase Φ_1. Switches S_3 and S_4 are closed during phase Φ_{1a}. Switches S_5 and S_6 are closed during phase Φ_2. Switches S_7 and S_8 are closed during phase Φ_{2a}. Phases Φ_1 and Φ_2 are non-overlapping clock phases. Phases Φ_{1a} and Φ_{2a} are advanced versions of phases Φ_1 and Φ_2, respectively. Switches S_3 and S_4 are turned off slightly before switches S_1 and S_2 are turned off. Similarly, switches S_7 and S_8 are turned off slightly before switches S_5 and S_6 are turned off. Since the sources and drains of switches S_3, S_4, S_7, and S_8 are biased at fixed potentials, the charge injections from these switches are to the first-order approximation constant and introduce little non-linearity. Signal-dependent charge injections from switches S_1, S_2, S_5, and S_6 are prevented because the top plates of sampling capacitors are floating at the closing instants of these switches. This advanced cut-off technique [X] minimizes the signal-dependent charge injection and improves the sampling linearity.

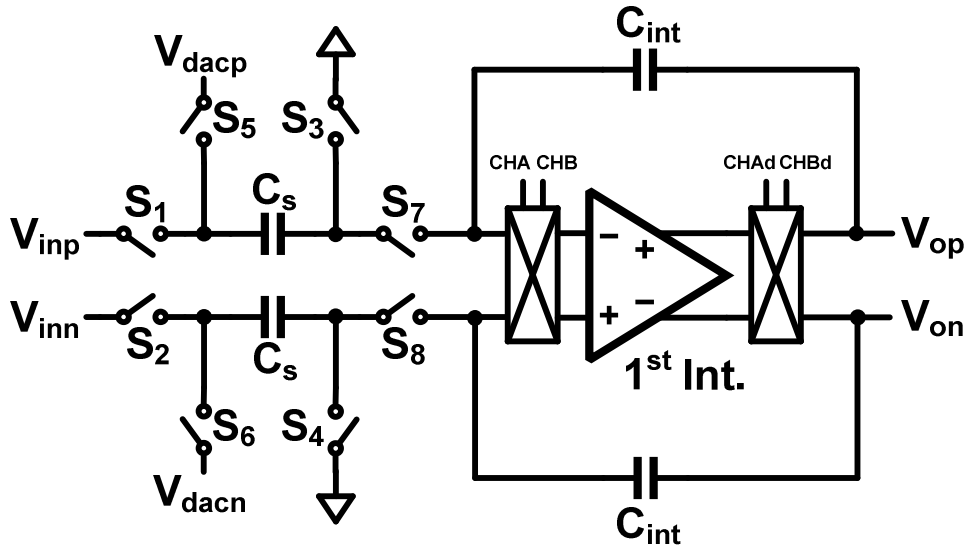

Fig. 3-1. The circuit diagram of the first integrator.

The overdrive voltage of a regular CMOS switch varies with different input signal amplitudes, which results in varying on-resistance of the sampling switch and therefore signal-dependent non-linear sampling error. Bootstrapping technique [3-2] is used to enhance the sampling linearity of the first integrator. Shown in Fig. 3-3, the capacitor C_b is charged to V_{dd} during phase Φ_2. M_0 is cut off in this phase by connecting its gate to ground. During phase Φ_1, the capacitor C_b is reconnected between the gate and source of M_0. The overdrive voltage of M_0 during Φ_1 in this case is always V_{dd}-V_{th}, no matter what the input voltage is. The on-resistance of switch M_0 in linear region is linearly proportional to the overdrive voltage which in this case is V_{dd}-V_{th}. Therefore, the on-resistance of switch M_0 neglecting second-order effects is kept constant and the sampling linearity is greatly improved. Since overdrive voltage is increased by bootstrapping technique, smaller sampling switch sizes can be used.

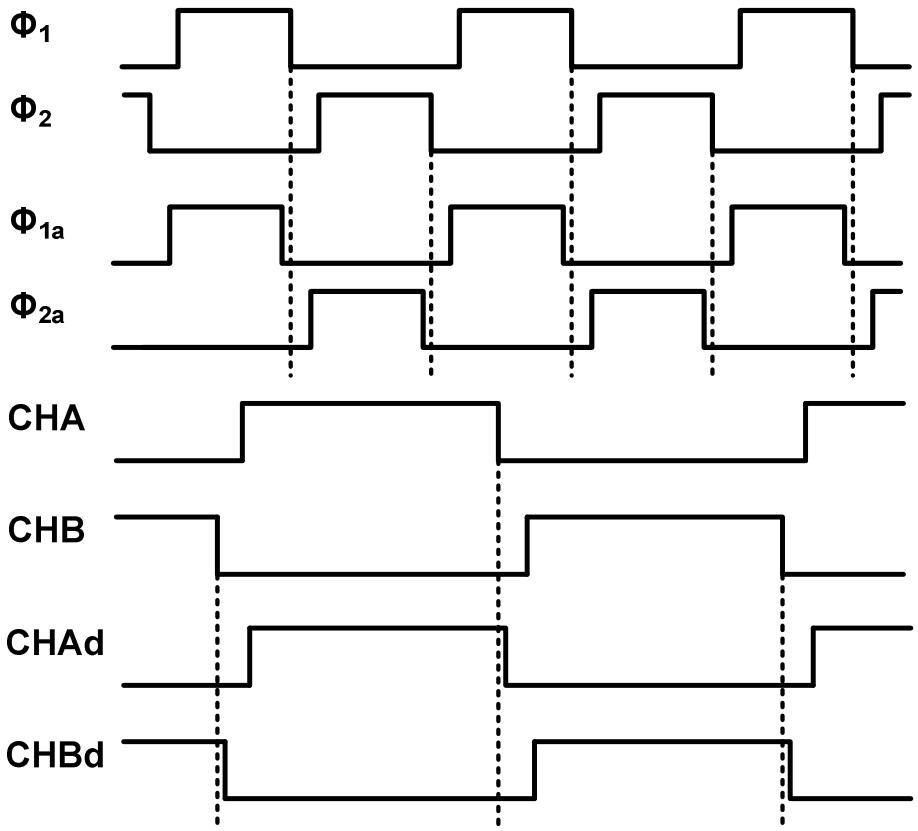

Fig. 3-2. The timing of the first integrator.

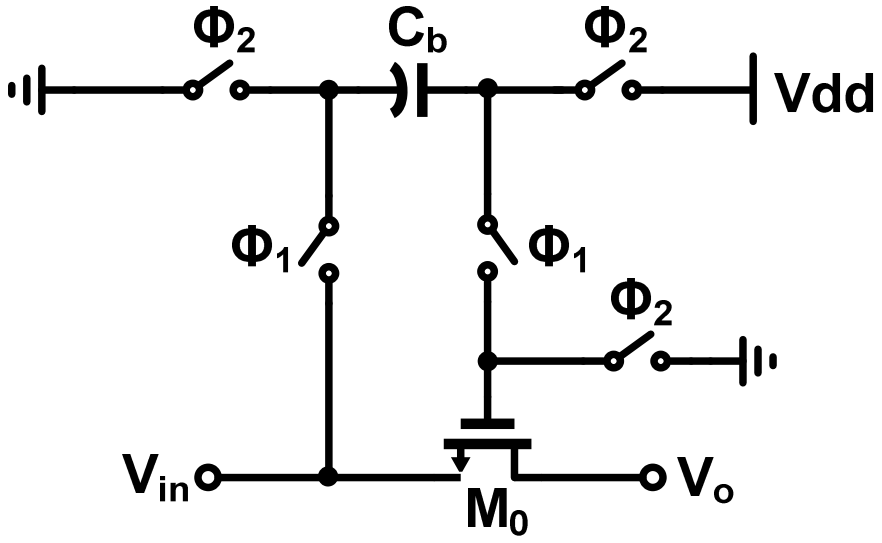

Fig. 3-3. Principle of bootstrapping technique.

Chopper stabilization technique [3-3] is used to reduce the DC offset and flicker noise of the opamp. Chopping is performed in the middle of the sampling phase to reduce the disturbance caused by the chopping activity [3-4]. The chopper has been simulated and proved to be efficient to reduce the dc offset and flicker noise. Chopper function could be turned off by the controlling bit in the design in order to observe the difference with the chopper turned on and off.

It is cheaper to suppress the quantization noise than the sampling noise in modulators with high OSRs. For power-efficient designs, the sampling capacitor size is usually chosen in such a way that the ADC noise floor is dominated by kT/C noise. The sampling capacitor and feedback DAC share the same set of unit capacitors in this design to increase the feedback factor of the first integrator. The total sampling capacitor size is 1.05pF. There are 14 unit capacitors with each one being 75fF.

The matching accuracy of unit capacitors is another concern when determining the total sampling capacitor size and therefore the unit capacitor size. A bigger unit capacitor size results in better matching accuracy. Dynamic element matching (DEM) techniques mentioned in chapter 2 can be used to enhance the feedback DAC linearity. The minimum unit capacitor size can be theoretically calculated based on the capacitor matching information and the modulator parameters such as OSR, internal quantizer resolution and DEM algorithm effectiveness. However, the most practical way of verifying whether the chosen unit capacitor size is big enough to make the influence of the unit capacitors mismatch of the feedback DAC on the modulator performance negligible is to run behavioral level Monte Carlo simulations. The unit capacitor in this project is a comb metal capacitor. Beside its good matching property, the comb metal capacitor also shows very small voltage coefficient (VC), and the nonlinearity originated from non-zero VC under high voltage input is negligible. The Monte Carlo simulations show the unit capacitor size of 75fF is adequate for the matching purpose.

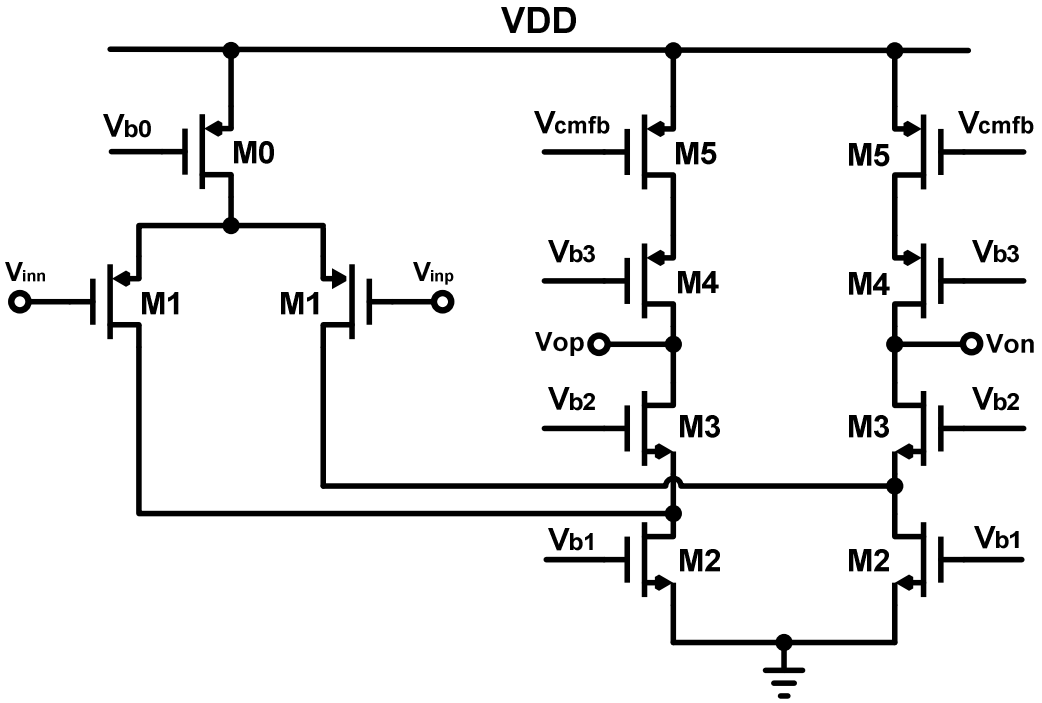

Fig. 3-4. PMOS-input folded cascode single-stage operational amplifier.

Fig. 3-4 shows the circuit diagram of the PMOS-input folded cascode single-stage operational amplifier [3-5]. With the proposed delta-sigma ADC architecture, the signal component in the loop is negligible and the modulator processes mostly quantization noise. The output swing of the first integrator is small, and therefore cascode structure could be used.

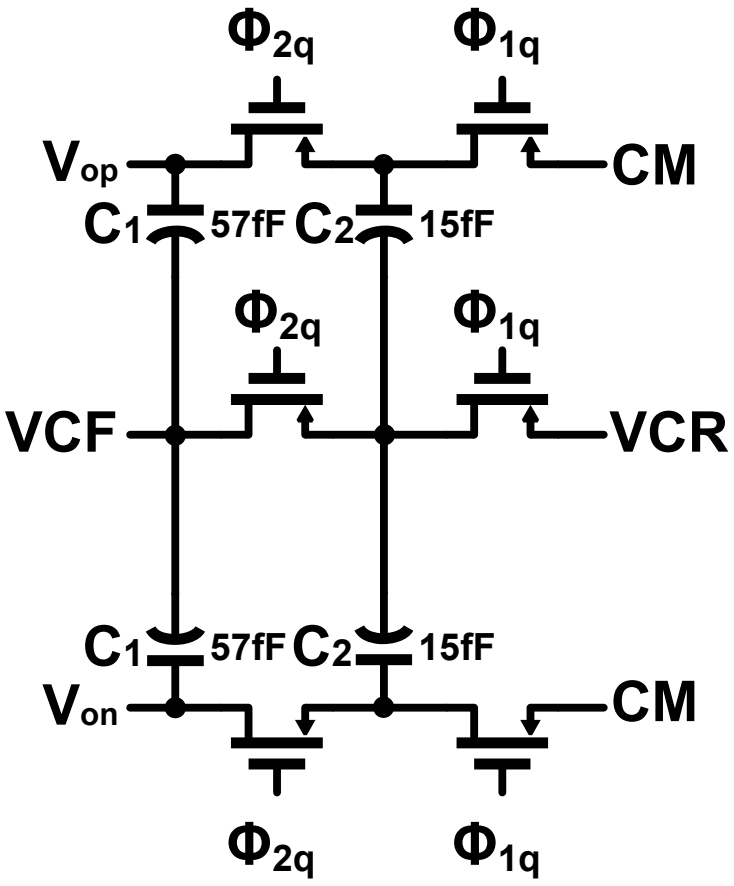

Fig. 3-5. Switched-capacitor CMFB circuit for the opamp of the first integrator.

To reduce the on-resistances of the switches S_7 and S_8 in Fig. 3-1, NMOS transistors are used for these switches and a low opamp input common mode of 0.5V is used. The

signal bandwidth is 20 kHz and the OSR is 64. The sampling clock frequency is 2.56 MHz and the loop UGB is designed to be 12.7 MHz in the typical corner. The gain factor of the first integrator is 1. Considering the parasitic capacitors at the opamp input, the feedback factor β_1 is assumed to be 0.45. The sum of the loading capacitors during the integration phase considering parasitic capacitors is C_{L1}=0.97pF. The required trans-conductance is $g_{m1}=2\pi C_{L1}UGB/\beta_1$=170μS. Shown in Fig. 3-4, the static current I_{d1} of each PMOS transistor M_1 of the input differential pair is 12μA. Therefore, the ratio g_{m1}/I_{d1} in this design is roughly 14. The static current flowing through the PMOS transistor M_5 is mostly determined by the slew rate requirement of the opamp, and is optimized to be 9μA. The total static current consumption of the opamp of the first integrator including biasing circuit is 45μA.

The DC gain of the opamp is around 87dB, which sufficiently suppresses the non-linearity induced by the finite DC gain of the opamp. The output resistance of a high DC gain single-stage opamp is usually very high and the common-mode feedback (CMFB) circuit with two equivalent resistors attached to the opamp outputs to sense the opamp output common-mode voltage will decrease the DC gain, unless impractically huge resistors (tens of megohm) are used. Instead, switched-capacitor CMFB [3-6] circuit is used to stabilize the output common-mode voltage of the first integrator, and the DC gain is not affected by this CMFB circuit.

Shown in Fig. 3-5, V_{op} and V_{on} are the differential outputs of the first integrator. “CM” is the reference output common-mode voltage which is set to be 2.5V (one half of the analog power supply). “VCR” is the reference voltage input, generated by the biasing network, for the CMFB circuit. “VCF” is the output from the CMFB circuit to control the gate of M5 and therefore the output common-mode voltage of the opamp. C_2 is roughly a quarter of C_1.

The power supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR) are designed to be over 100dB to minimize the influences from the power supply noise and common-mode voltage variation on the modulator performance.

3.1.2 Second Integrator

Fig. 3-6 shows the circuit diagram of the second integrator with differentiated quantization noise injection. Single-ended representation is shown for simplicity. However, the real circuit implementation is fully differential.

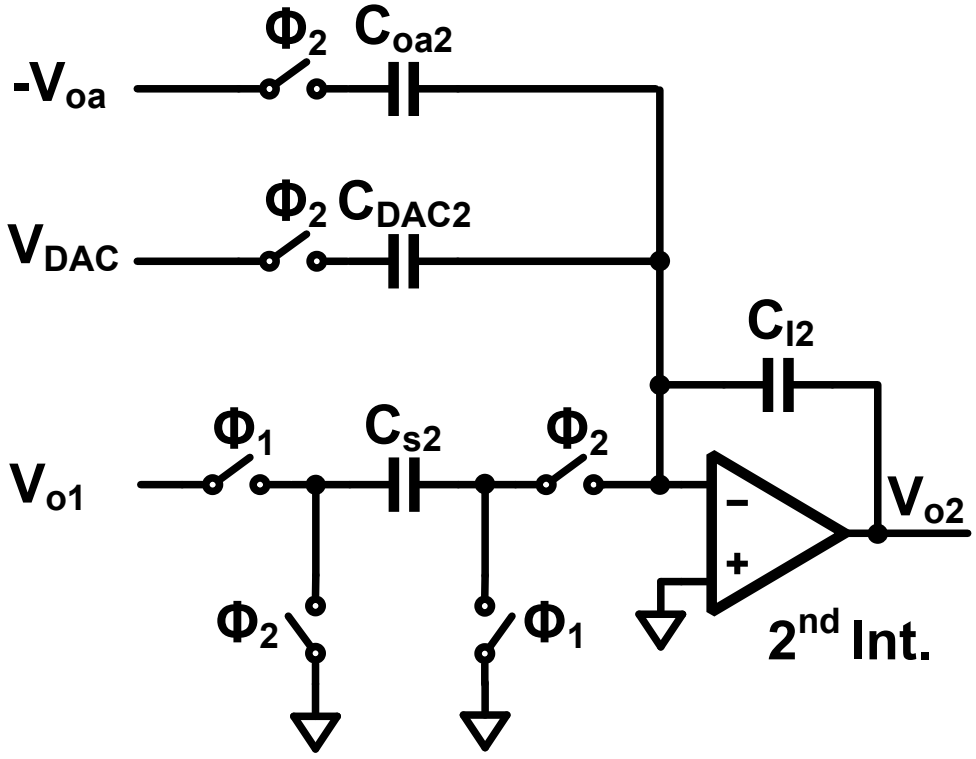

Fig. 3-6. The second integrator with differentiated quantization noise injection.

The unit capacitor size for the second integrator is 11.5fF. The sampling capacitor C_{s2} consists of 14 unit capacitors. The integration capacitor C_{I2} consists of 7 unit capacitors. The differentiated quantization noise injection function is implemented by two branches C_{oa2} and C_{DAC2}. C_{oa2} is made up of 49 unit capacitors and is connected to the DCT adder output during phase Φ_2. C_{DAC2} is made up of 14 unit capacitors whose bottom plates are controlled by the shuffled internal quantizer output.

Fig. 3-7 illustrates the opamp used for the second integrator. Since the requirements on the on-resistances of the sampling switches of the second integrator are greatly relaxed compared to those of the first integrator, a NMOS-input cascode single-stage opamp is used and the opamp input common-mode voltage is set to 1.5V. The output common-mode voltage is set to 2.5V, and a switched-capacitor CMFB circuit is used. The opamp for the second integrator consumes 20μA static current.

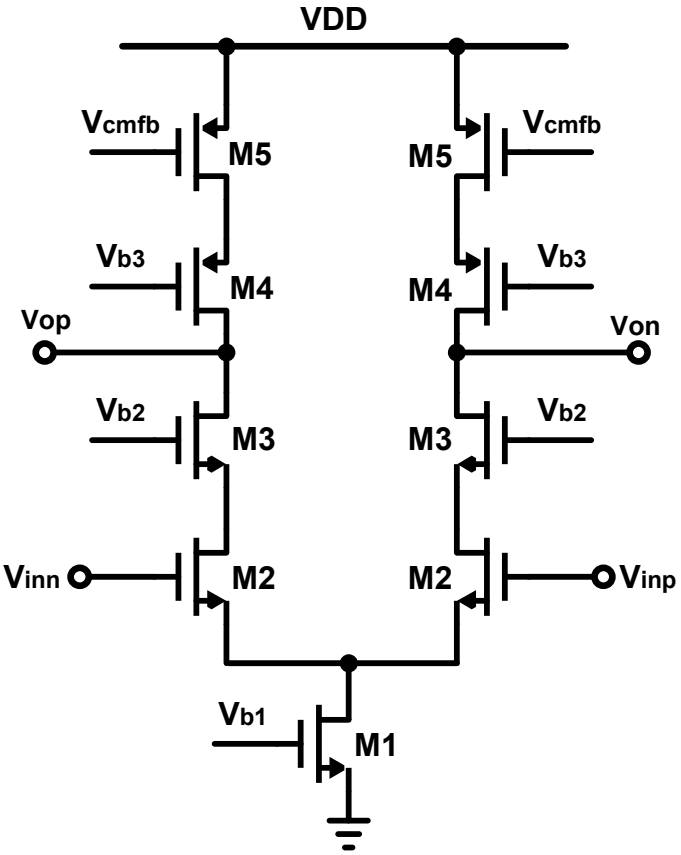

Fig. 3-7. NMOS-input cascode single-stage opamp for the second integrator.

3.1.3 DCT Adder Design

Fig. 3-8 shows the capacitive loading of the DCT adder during phase Φ_2. During phase Φ_2, the adder holds its output by connecting the capacitor C_H in unity gain configuration.

The adder also charges the capacitor C_{oa2} at the input of the second integrator. The total capacitive loading considering 20% top and 20% bottom parasitic capacitors is 406fF.

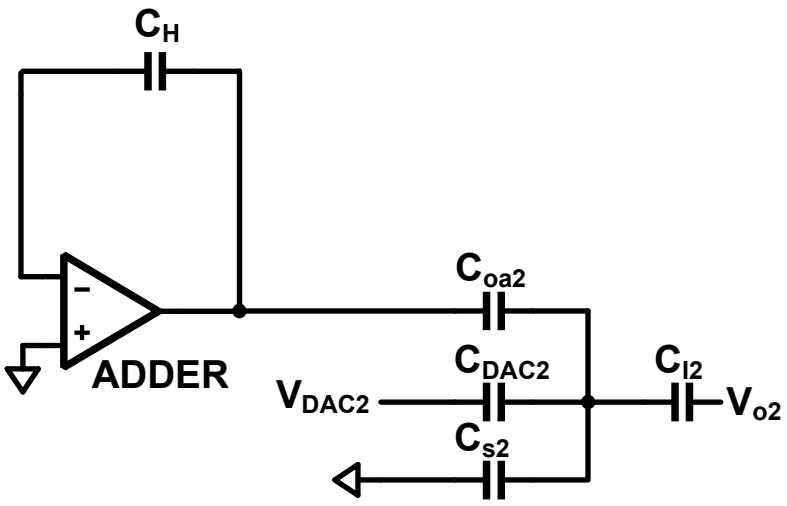

Fig. 3-8. The capacitive loading of the DCT adder during phase Φ_2.

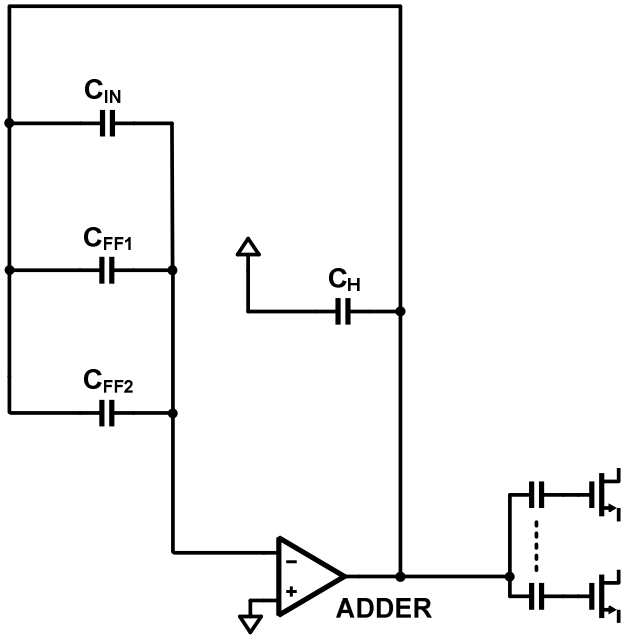

Fig. 3-9. The capacitive loading of the DCT adder during phase Φ_1.

Fig. 3-9 shows the capacitive loading of the DCT adder during phase Φ_1. The sampling capacitors of the adder, the hold capacitor C_H and the loading capacitors from the internal quantizer form the loading of the adder. The total capacitive loading considering 20% top and 20% bottom parasitic capacitors is 820 fF. The DCT adder consumes 10 μA static current.

3.2 Internal Quantizer Design

Shown in Fig. 3-10, the 15-level internal quantizer is composed of a resistor ladder, clock buffers, and 14 comparator cells. To accommodate the inherent attenuation of the DCT adder, the quantizer reference is scaled down by a factor of 3.5. The comparator cell is made up of the preamplifier with the offset cancellation scheme, the regenerative latch, and the SR latch.

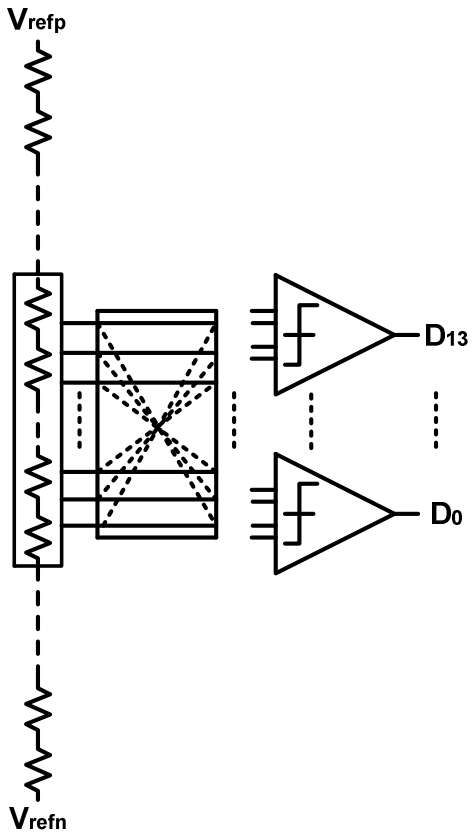

Fig. 3-10. Circuit diagram of the quantizer.

The preamplifier with the offset cancellation scheme [3-7][3-8] is shown in Fig. 3-11. When F2q is low, the preamplifier is in the unity gain configuration, and the offset of the input pair of the preamplifier is stored on the offset cancellation capacitor C_c. The preamplifier DC gain is designed to be around 20 dB. Therefore, the offset of the circuits following the preamplifier is reduced by 10 when referred to the comparator input. The UGB of the preamplifier is around 10 MHz. The biasing current of the preamplifier is 350 nA.

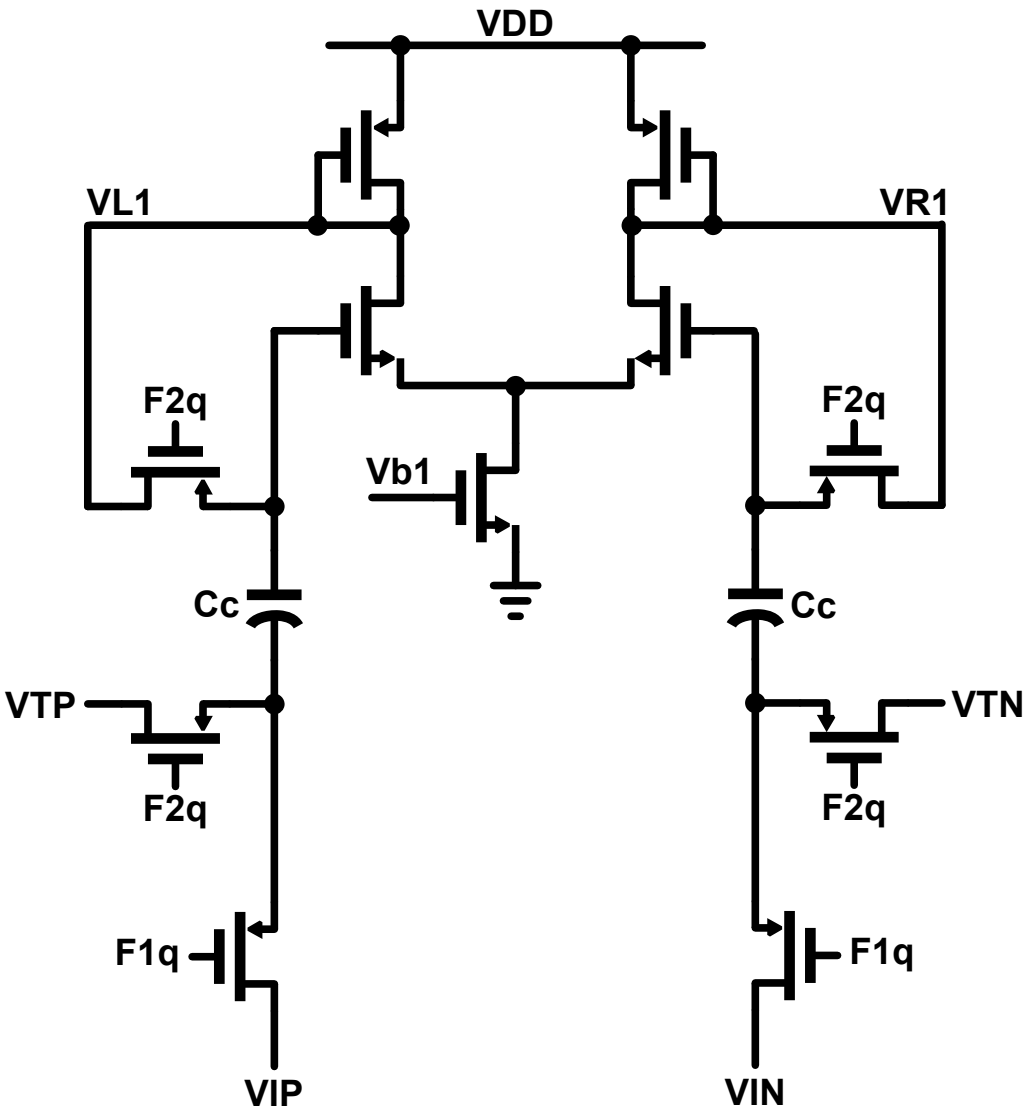

Fig. 3-11. The preamplifier with the offset cancellation scheme.

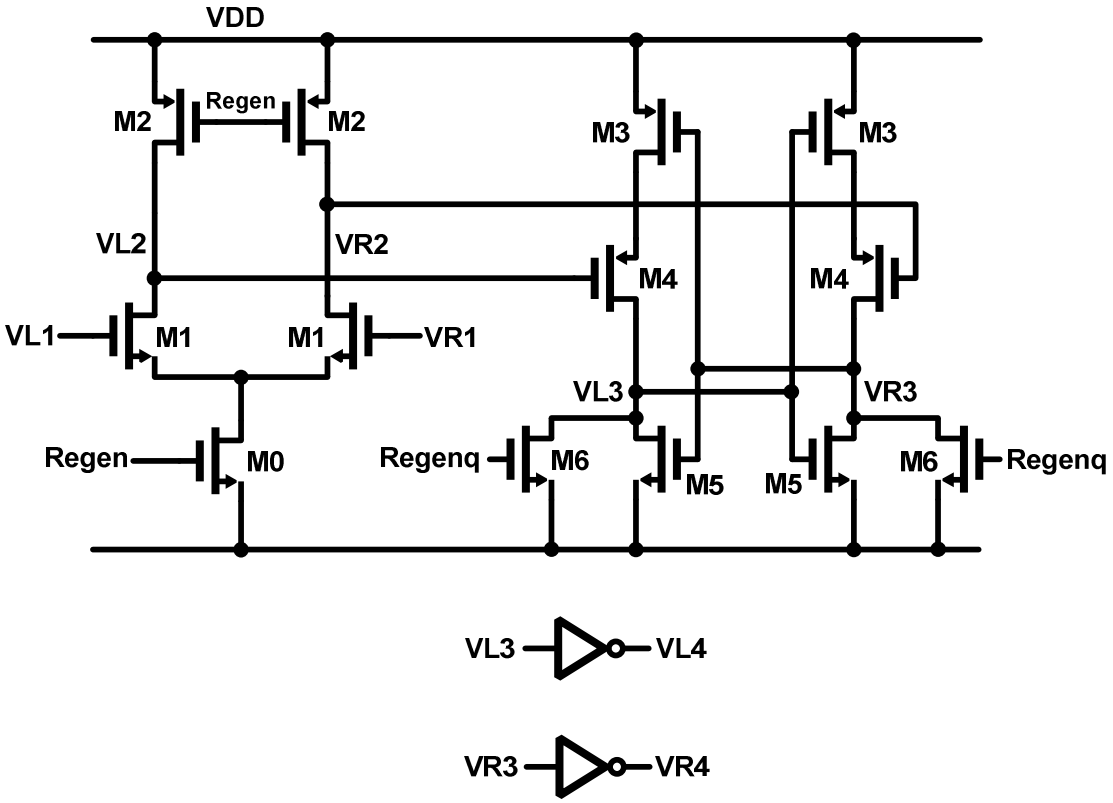

Fig. 3-12. The regenerative latch.

The regenerative latch [3-9] is shown in Fig. 3-12. When Regen is low, nodes VL2 and VR2 are pulled to VDD, and nodes VL3 and VR3 are pulled to ground by Regenq. At the end of the phase Φ_1, Regen goes up and nodes VL2 and VR2 begin to be discharged by M_0. Due to the voltage difference between nodes VL1 and VR1, the discharge rates at nodes VL2 and VR2 are different. Regenq goes down, and nodes VL3 and VR3 are no longer pulled to ground. If the discharge rate of the node VL2 is faster than that of VR2, node VL3 will be pulled up to VDD and node VR3 will be pulled down to ground eventually by the positive feedback. A pair of inverters is inserted between the regenerative latch and the SR latch to isolate the kickback noise from the SR latch. Fig. 3-13 shows the circuit diagram of the SR latch.

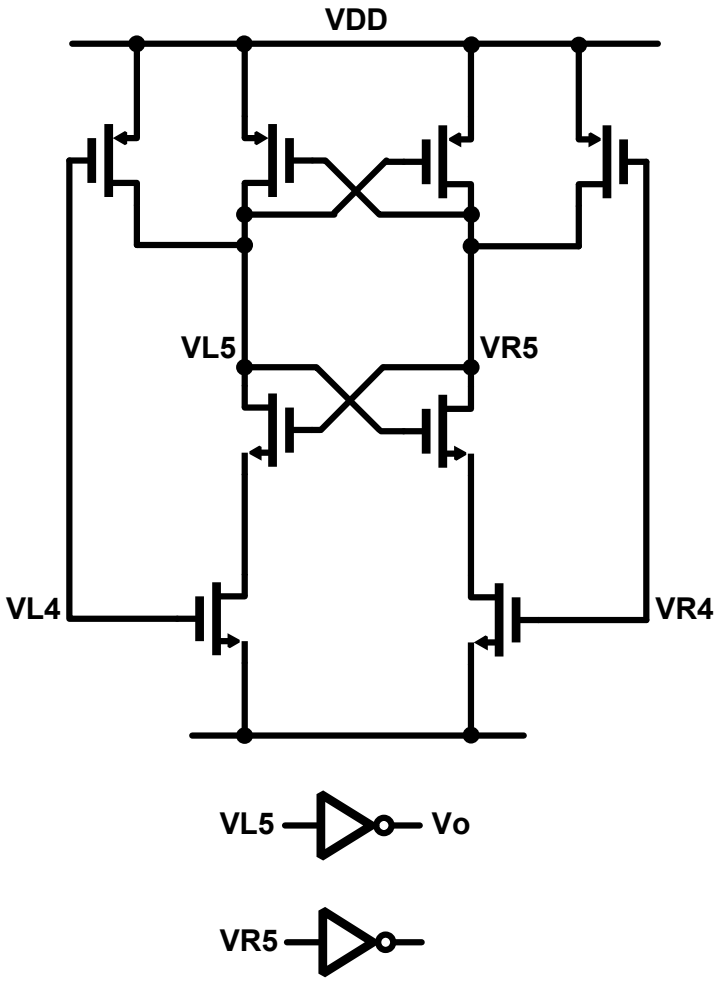

Fig. 3-13. SR latch.

The differential quantization step of the resistor ladder is around 120 mV. The 3σ offset of the comparator is around 20 mV. MATLAB simulations with either +20 mV or -20 mV randomly added offset to each comparator input show unnoticeable performance loss.

3.3 DWA Logic

Shown in Fig. 3-14, the high-to-low voltage translators (HLVTs) convert the 5 V internal quantizer output and control signals to 1.8 V digital signals, as the inputs to the

DWA core logic. The 1.8V outputs of DWA core logic are reconverted back to 5V feedback DAC control signals by low-to-high voltage translators (LHVTs). Fig. 3-15 shows the circuit diagram of the LHVT.

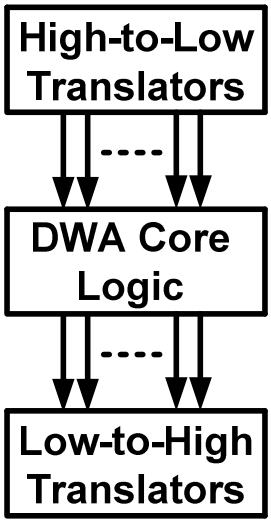

Fig. 3-14. DWA logic overview.

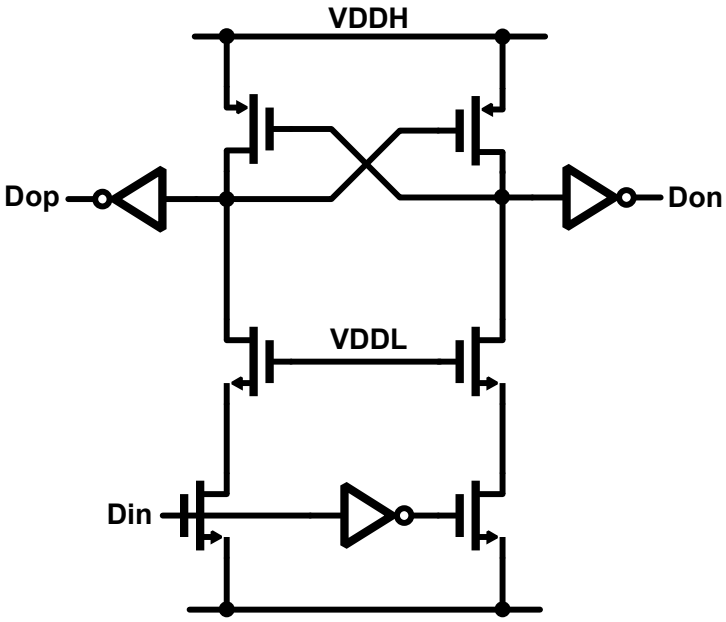

Fig. 3-15. Circuit diagram of the LHVT.

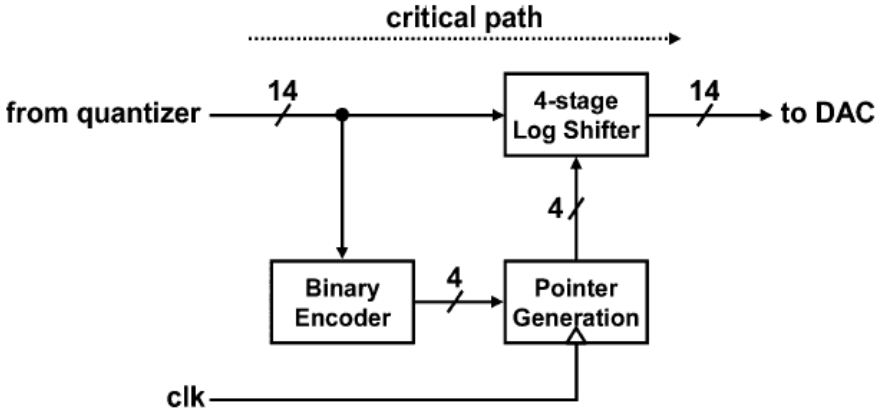

Fig. 3-16. Architecture of the DWA core logic.

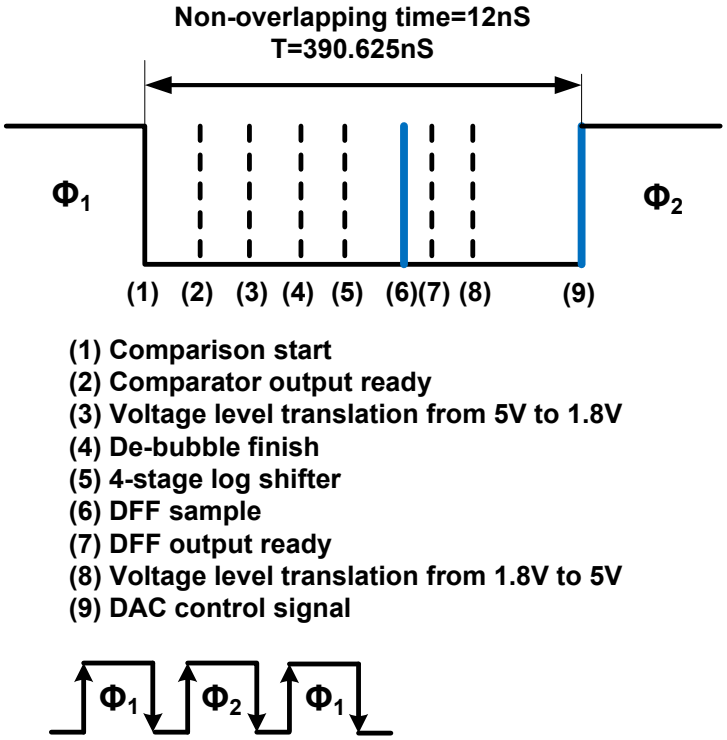

Fig. 3-17. DWA logic timing.

Fig. 3-16 shows the architecture of the DWA core logic [3-10]. The thermal code from the internal quantizer output is converted to binary code by the binary encoder. The output of the binary encoder enters the pointer generation block which is a ripple carry

adder. The output of the pointer generation block controls the 4-stage log shifter which is used to shuffle the internal quantizer output. The shuffled quantizer output effectively shapes the feedback DAC mismatch error, and greatly improves its linearity. Fig. 3-17 shows the DWA timing. On the falling edge of phase Φ_1, the internal quantizer starts the quantization. When the quantizer finishes the quantization, its output is converted from 5V logic level to 1.8V logic level by HLVTs, which are followed by the de-bubble logic and the 4-stage log shifter. In the same clock period, the output of the 4-stage log shifter must be ready before the sampling instant of the D flip-flops (DFFs). The output of the DFFs is converted back from 1.8 V logic level to 5 V logic level by LHVTs whose outputs must be ready before the next rising edge of phase Φ_2 to avoid glitches.

3.4 Layout and Simulation Results

Fig. 3-18 shows the layout of the design. The die area including pads is 2.6 mm*2.6 mm. The core area is 0.9 mm*0.5 mm. There are 48 pads with 12 on each side. Fig. 3-19 shows the simulated power spectral density (PSD) of the modulator output.

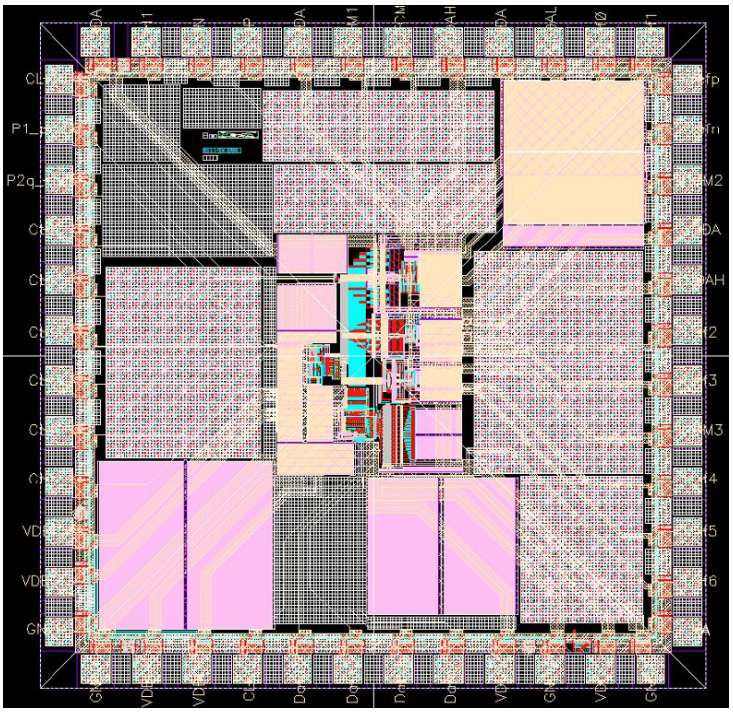

Fig. 3-18. Layout of the proposed ADC.

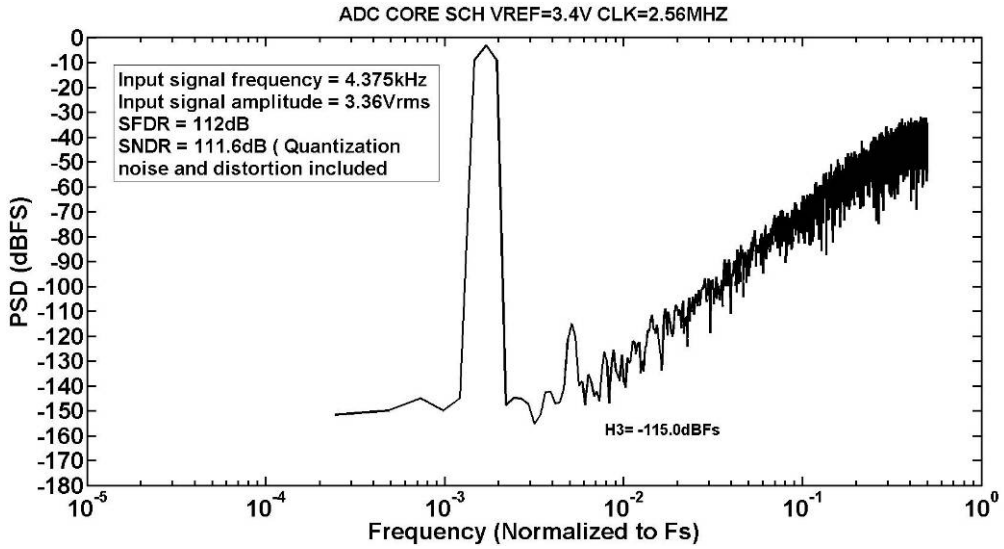

Fig. 3-19. Simulated PSD of the modulator output.

Reference

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Chapter 4 Measurement Results

4.1 Test Setup

Fig. 4-1 shows the test environment and wires hookup. Fig. 4-2 shows the printed circuit board (PCB) platform for the measurement setup. The input signal comes from an Audio Precision signal generator. The thermometer codes at the output of the internal quantizer are converted to 4-bit binary codes and then buffered to output pins $D_3D_2D_1D_0$ for measurement. The output signals $D_3D_2D_1D_0$ are captured by a logic analyzer. A serial clock SCLK is also available, and used as a reference clock to synchronize data capture. Fig. 4-3 shows the photo of the entire die. Fig. 4-4 shows the core area of the die.

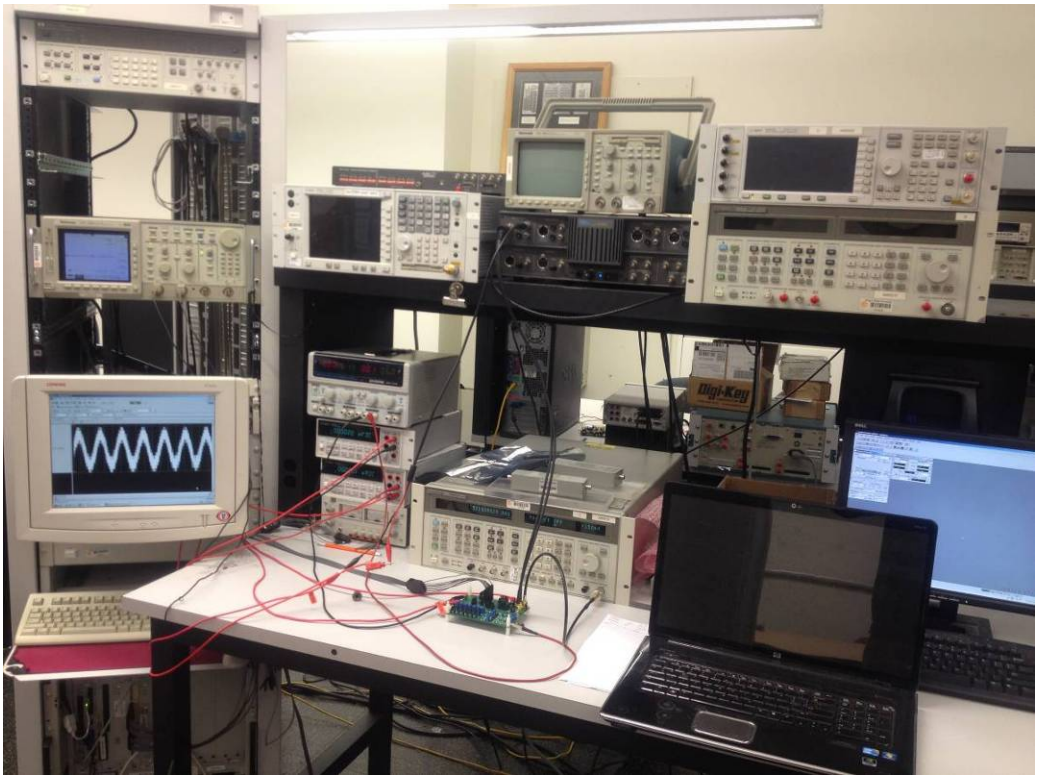

Fig. 4-1. Test environment.

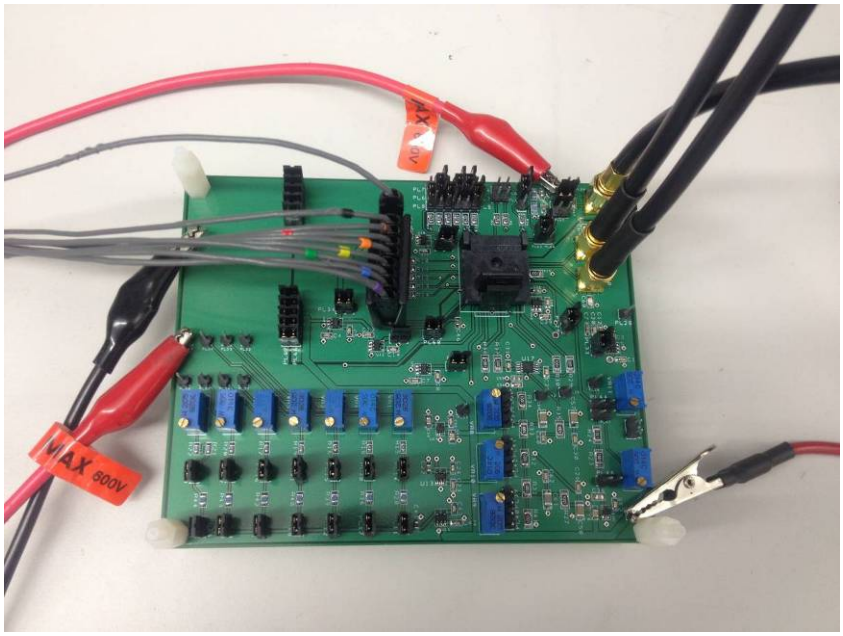

Fig. 4-2. PCB test platform.

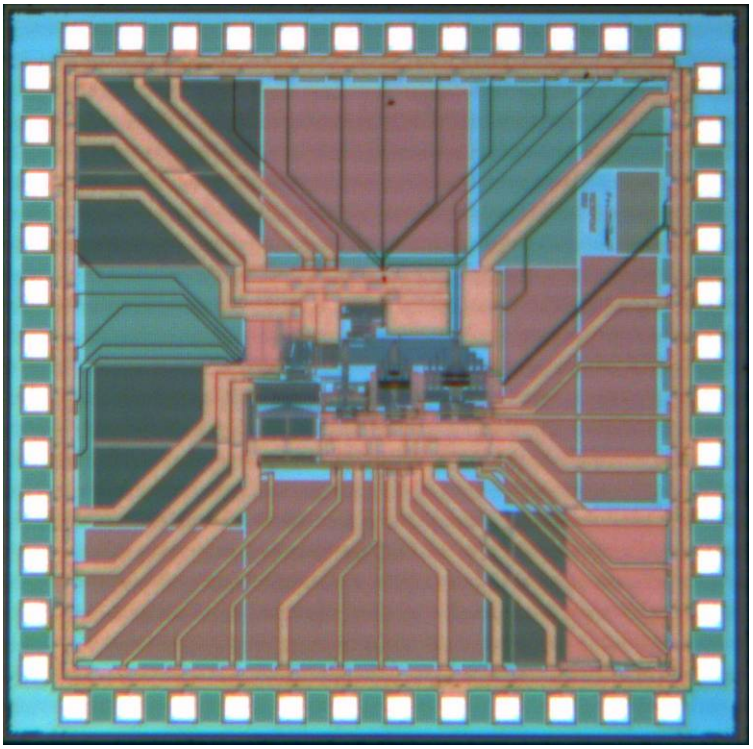

Fig. 4-3. Entire die photo.

Fig. 4-4. Core area die photo.

4.2 Measurement Results

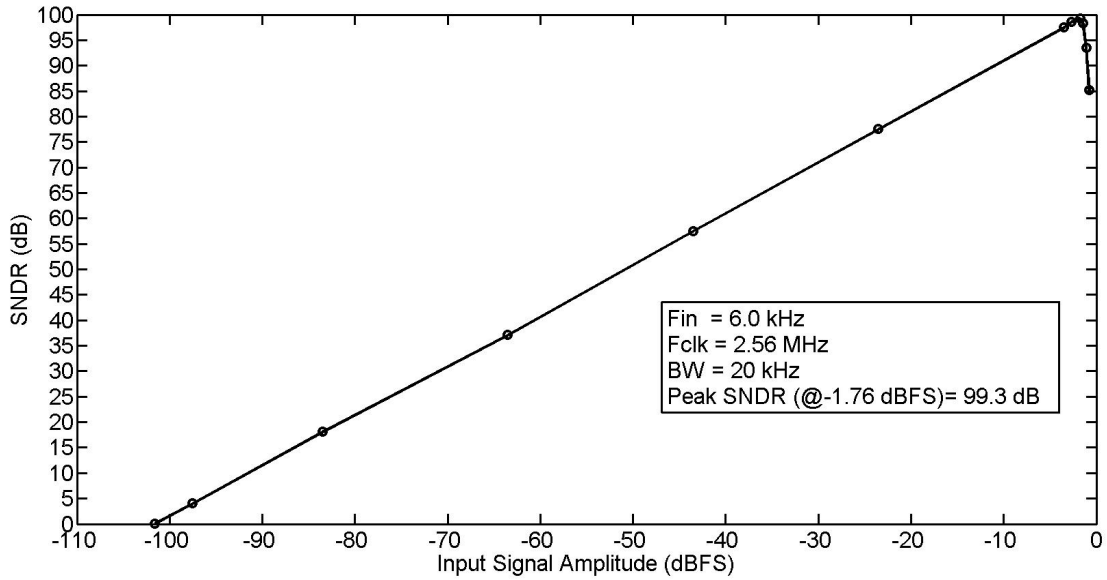

Fig. 4-5. SNDR versus input amplitude.

Fig. 4-5 shows the SNDR versus input signal amplitude. Fig. 4-6 shows the PSD of the modulator output in a log scale without chopping. Fig. 4-7 shows the PSD of the

modulator output in a log scale with chopping. Fig. 4-8 shows the PSD of the modulator output within the signal bandwidth in a linear scale without chopping. Fig. 4-9 shows the PSD of the modulator output within the signal bandwidth in a linear scale with chopping. The DC offset is reduced by 17dB with chopper turned on.

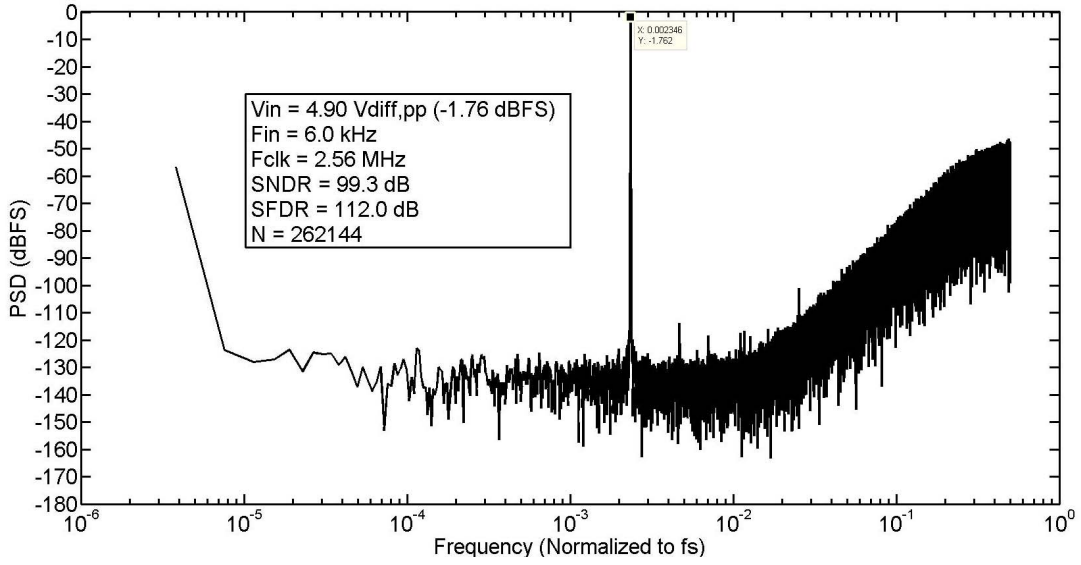

Fig. 4-6. PSD of the modulator output (Chopper off).

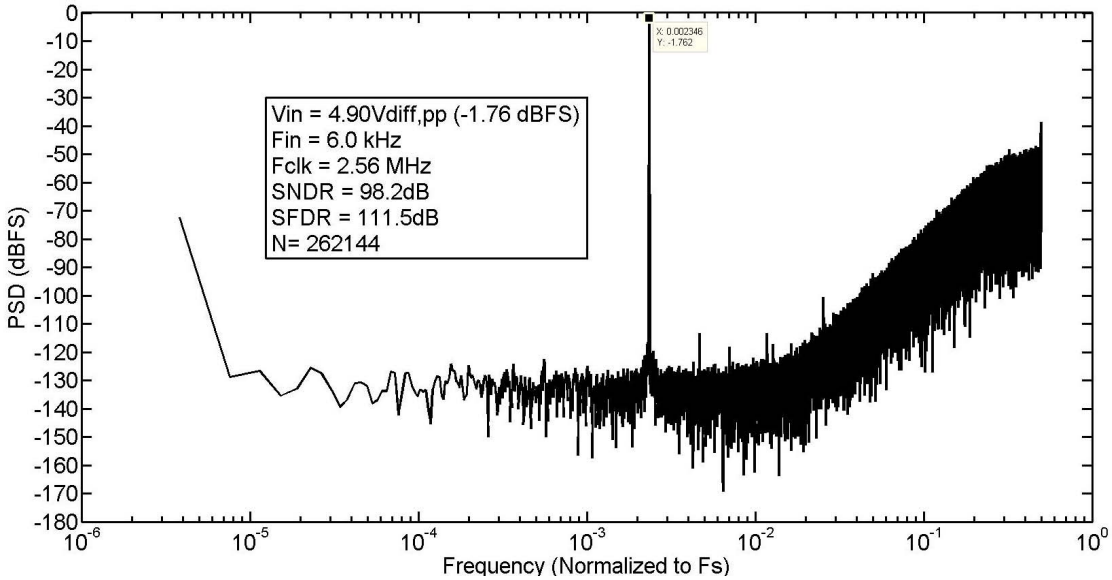

Fig. 4-7. PSD of the modulator output (Chopper on).

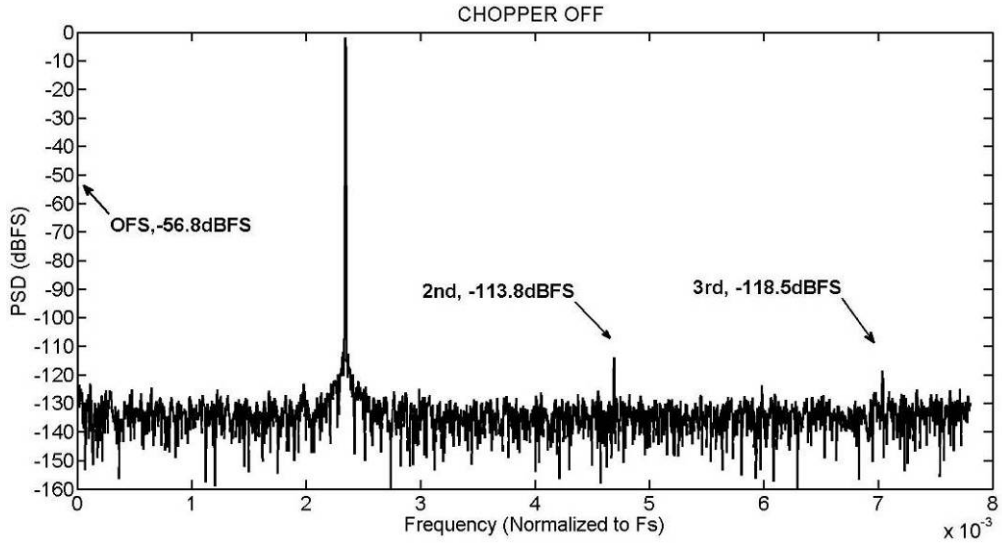

Fig. 4-8 PSD of the modulator output within the signal bandwidth (Chopper off).

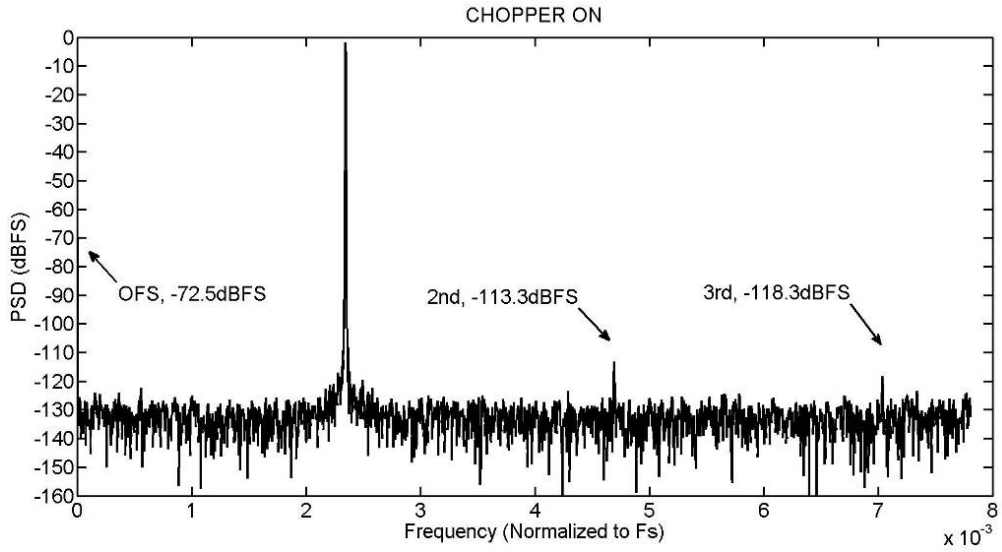

Fig. 4-9 PSD of the modulator output within the signal bandwidth (Chopper on).

Table 4-1 summarizes the performance of the device. Table 4-2 compares the FoM of this work to the state-of-the-art converters which obtained over 15-bit ENOB. Notice that in very high-resolution applications, the quantization noise compared to the sampling noise in a sound design should be negligible. In order to increase ENOB by 1 bit, the

sampling capacitor size has to be increased 4X, resulting in 4X power dissipation. Compared to the general Walden figure-of-merit (FoM_1) below, FoM_2 [4-9] below adds a factor 2 in the exponent before the factor (SNDR-1.76)/6.02. This work is among the best in DSMs (ENOB>15-b), and achieves the lowest FoM_1 and FoM_2 in DSMs (ENOB>15-b) above 100-nm technology node.

$$FoM_1 = \frac{Power}{2 \times BW \times 2^{(SNDR-1.76)/6.02}} \tag{4-1}$$

$$FoM_2 = \frac{Power}{2 \times BW \times 2^{2\times(SNDR-1.76)/6.02}} \tag{4-2}$$

Table 4-1. Summary of measured ADC performance

Specifications	Value
Technology	0.18 um CMOS
Power supplies	5.0(A)/5&1.8(D)
Analog power dissipation	570 µW
Digital power dissipation	530 µW
Total power dissipation	1.1 mW
Maximum input amplitude	-1.76 dBFS (1.73 V_{rms})
Signal bandwidth	20 kHz
Clock frequency	2.56 MHz
OSR	64
Peak SNDR/SNR	99.3/99.5 dB (@ -1.76 dBFS)
SFDR	112 dB
Dynamic range (DR)	101.3 dB
Die area	6.8 mm^2 (2.6 mm * 2.6 mm)

Core die area	0.38 mm^2 (0.44 mm*0.86 mm)

Table 4-2. Comparisons to the state-of-the-art converters (ENOB>15).

	Source	BW (kHz)	OSR	SNDR (dB)	Power (mW)	Power Supply (V)	Type	CMOS (um)	FoM_1 (pJ/conv.)	FoM_2 (10^{-3}fJ/conv.)
[4-1]	ISSCC03	20	128	105.0	55.0	5	DT 5th	0.35um	9.5	65.1
[4-2]	ISSCC05	20	128	97.0	18	3.3	DT&CT 2nd	0.35um	7.8	134.4
[4-3]	ISSCC05	20	154	95.0	37	3.3	DT&CT 2nd	0.18um	20.1	437.7
[4-4]	CICC08	20	128	97.5AW	9.9	3.3	DT 2nd	0.13um	4.0	65.9
[4-5]	CICC11	24	64	95.0	0.371	1.0	DT 3rd	0.065um	0.168	3.7
[4-6]	JSSC03	24	N/A	104.5	230	5/3.3	DT 6th	0.35um	34.9	254.4
[4-7]	JSSC08	20	154	115.0ET	290	5/2.5	DT 5th	0.35um	15.8	34.3
[4-8]	JSSC09	25	100	95.0	0.87	0.7	DT 2nd	0.18um	0.379	8.2
This work		**20**	**64**	**99.3**	**1.1**	**5/1.8**	**DT 3rd**	**0.18um**	**0.363**	**4.8**

ET=Estimated, AW=A-weighted

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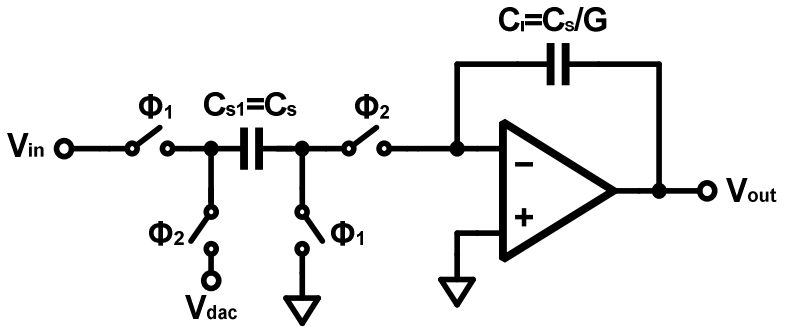
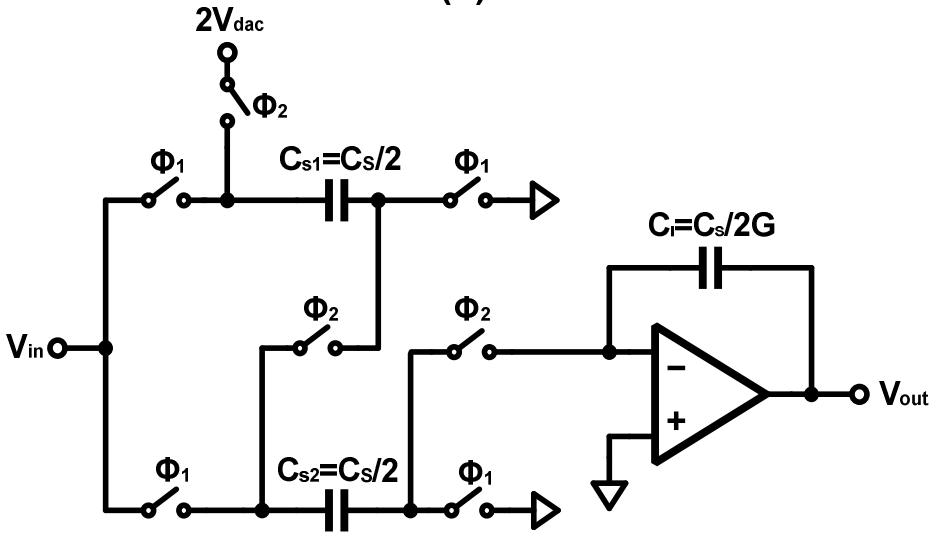
Chapter 5 Low-Power Parasitic-Insensitive Switched-Capacitor Integrator for Delta-Sigma ADCs

5.1 Background

A new low-power parasitic-insensitive switched-capacitor (SC) integrator is proposed for ΔΣ ADCs. Compared to the conventional SC integrator, the new one achieves much lower power dissipation for the same sampling noise specification. A cancellation technique is used to reduce the nonlinearity of the integrator. An effective ΔΣ ADC topology is described which can incorporate the new integrator. Simulation shows that high linearity can be achieved by the new integrator, while consuming very low power.



(a)



(b)

Fig. 5-1. (a) Conventional SC integrator. (b) Nilchi-Johns integrator.

SC ΔΣ ADCs are widely used in high-resolution applications, since they are insensitive to parasitics and allow relaxed accuracy requirements. However, SC circuits introduce sampling noise due to the thermal noise generated by the on-resistance of the sampling switches. Sampling noise is usually the dominant noise source, and is costlier to suppress than quantization noise in high-resolution ADC applications.

Nilchi and Johns proposed a new SC integrator which has lower sampling noise for the same power dissipation (or lower power dissipation for the same sampling noise) than the conventional SC integrator [5-1]. Fig. 5-1 compares the Nilchi-Johns integrator with a conventional one. Compared to the conventional SC integrator, the new integrator has smaller load capacitor and higher feedback factor. Therefore, for the same clock frequency and sampling noise, the required OTA transconductance is smaller by a factor of 4. Unfortunately, due to the doubled voltages in the input branch, the maximum allowable input voltage is halved in the new circuit. Hence, it is best suited for applications at the front end of a system, where the signal is very small.

To solve this problem, a modified structure which has the same beneficial features as the Nilchi-Johns integrator, but without the restrictions on the maximum input signal [5-2] was proposed earlier. However, similarly to the Nilchi-Johns integrator, the new integrator in [5-2] is still sensitive to parasitic capacitances and its linearity is hence limited. In this chapter, a new cancellation technique is described which significantly improves the linearity of the integrator.

5.2 Performance Analysis

Fig. 5-2 shows the integrator of [5-2], where G is the gain factor of the integrator. The power of the in-band sampling noise voltage during Φ_1 is $kT/(OSR \cdot C_s)$ [5-3]. Here, k is the Boltzmann constant, OSR is the oversampling ratio of the modulator, and T is the absolute temperature in degrees Kelvin. During Φ_2, the two sampling capacitors are connected in series, and the effective capacitance is hence $C_s/4$. The voltage difference across this equivalent capacitance is $2(V_{in}-V_{dac})$. Therefore, this sampling scheme

amplifies the difference between V_{in} and V_{dac} by a factor 2. The power of the thermal noise charge delivered into the integration capacitor during Φ_2 is $4kT/C_s$. This value is four times that of the conventional SC integrator shown in Fig. 1(a). However, the sampling capacitors in series provide a signal gain of 2, and therefore the input-referred voltage noise power remains kT/C_s.

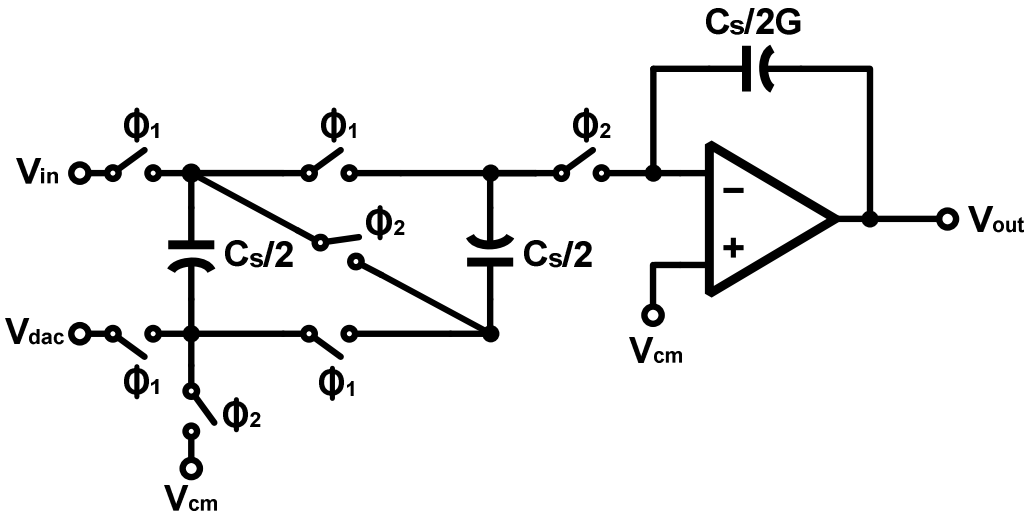


Fig. 5-2. Low-power parasitic-sensitive SC integrator.

The power dissipation of the integrator in Fig. 5-2 is the same as that in Fig. 5-1(b). Compared to the conventional SC integrator, both save 75% of the power dissipation [5-1].

For a detailed theoretical comparison, Figs. 5-3 and 5-4 show the conventional SC integrator and the low-power SC integrator in the integration phase. Here, k is the gain of the integrator. N_s is the number of capacitors in parallel during the sampling phase Φ_1 (in this case, N_s=2). The feedback factors β_C and β_L for the two circuits are

$$\beta_C = \frac{C_s/k}{C_s/k + C_s} = \frac{1}{1+k} \tag{5-1}$$

$$\beta_L = \frac{C_s/(kN_s)}{C_s/(kN_s) + C_s/N_s^2} = \frac{N_s}{N_s + k} \tag{5-2}$$

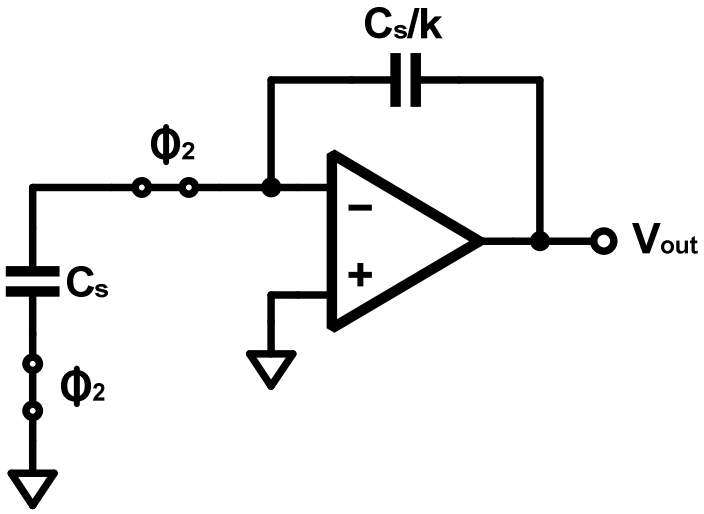


Fig. 5-3. Conventional SC integrator in the integration phase.

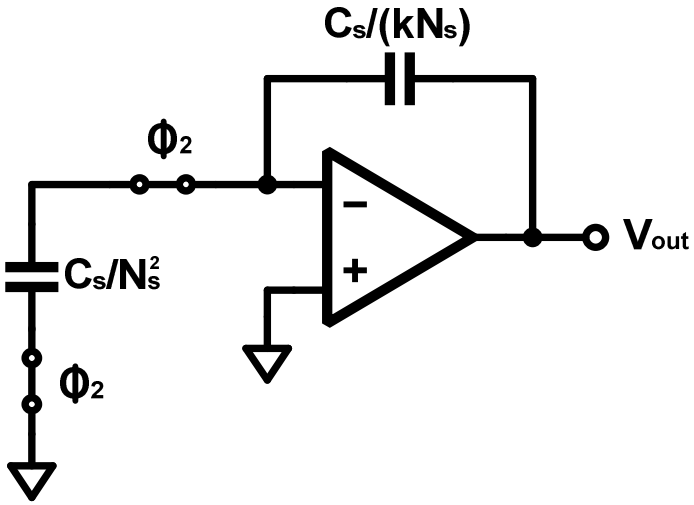


Fig. 5-4. Low-power SC integrator in the integration phase.

Neglecting the parasitics and the load from the next stage, the load capacitances of the integrators in the integration phase are given by

$$C_{L,C} = \frac{C_s^2 / k}{C_s / k + C_s} = \frac{C_s}{1+k} \tag{5-3}$$

$$C_{L,L} = \frac{C_s^2/(kN_s^3)}{C_s/(kN_s) + C_s/N_s^2} = \frac{C_s/N_s}{N_s + k} \tag{5-4}$$

The power of the amplifiers is proportional to the required gm [5-1]. Hence, it is given by

$$P_C = k_0 g_{m,C} = \frac{k_0 \omega_{-3dB} C_{L,C}}{\beta_C} = k_0 \omega_{-3dB} C_s \tag{5-5}$$

$$P_L = k_0 g_{m,L} = \frac{k_0 \omega_{-3dB} C_{L,L}}{\beta_L} = \frac{k_0 \omega_{-3dB} C_s}{N_s^2} \tag{5-6}$$

Here, k_0 is the proportionality constant between the power required and the transconductance of the amplifier, while ω_{-3dB} is the closed-loop 3-dB bandwidth. Therefore, for the same kT/C noise specification, the proposed low-power SC integrator saves a significant amount of power. The saving is the same as for the Nilchi-Johns integrator. Table I compares the performances of the conventional SC integrator and the low-power SC integrator.

Table 5-1. Comparison of the conventional SC integrator and the low-power SC integrator

	Conventional SC integrator	Low-power SC integrator
Gain	k	k
Sampling capacitance	C_s	C_s
Integration capacitance	C_s/k	$C_s/(kN_s)$
kT/C noise	$2kT/(OSR \cdot C_s)$	$2kT/(OSR \cdot C_s)$
Feedback factor	$(1+k)^{-1}$	$N_s(N_s+k)^{-1}$
Capacitance load	$C_s(1+k)^{-1}$	$(C_s/N_s)(N_s+k)^{-1}$
Power dissipation	$k_0\omega_{-3dB}C_s$	$k_0\omega_{-3dB}C_sN_s^{-2}$

However, both integrators in [5-1] and [5-2] are affected by the nonlinear parasitic capacitances loading both sides of the switch connecting the two capacitors during Φ_2. The achievable linearity is therefore limited.

5.3 Parasitic-Insensitive Low-Power Integrator

Fig. 5-5 shows the proposed differential parasitic-insensitive SC integrator. The noise and power dissipation are the same as those of Fig. 5-2, neglecting the small cancellation capacitors C_c. For a well-matched layout, the parasitic capacitors at nodes V_{x1} and V_{x2} are approximately the same. The sum of extra charges stored at nodes V_{x1} and V_{x2} during Φ_1 due to these parasitic capacitors is unchanged, and is not signal-dependent. The parasitic capacitance at node V_{x0} has no effect on the linearity.

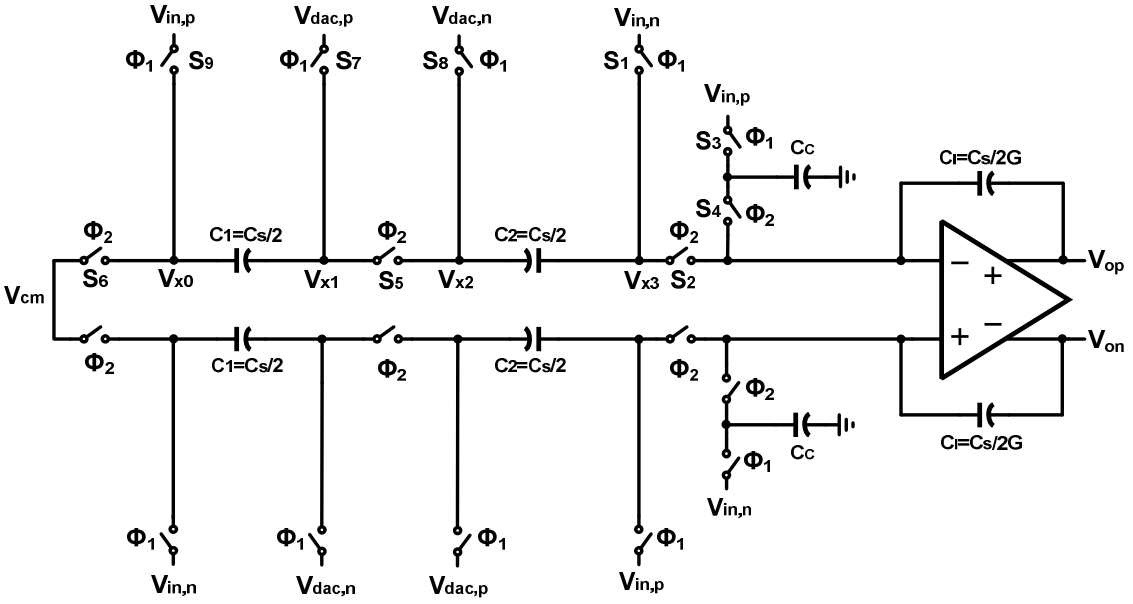


Fig. 5-5. Proposed low-power parasitic-insensitive SC integrator.

The parasitic capacitance at node V_{x3} is, however, problematic. It is comprised of a linear part and a nonlinear part. The linear part arises mainly from the parasitic capacitance of the top-plate of capacitor C_2. This will cause a small amount of signal leakage into the loop, but it does not harm the linearity of the integrator.

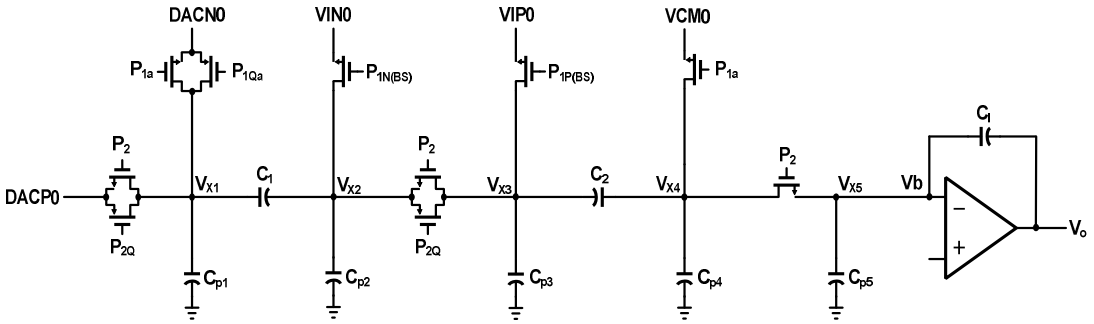


Fig. 5-6. Proposed low-power parasitic-sensitive SC integrator.

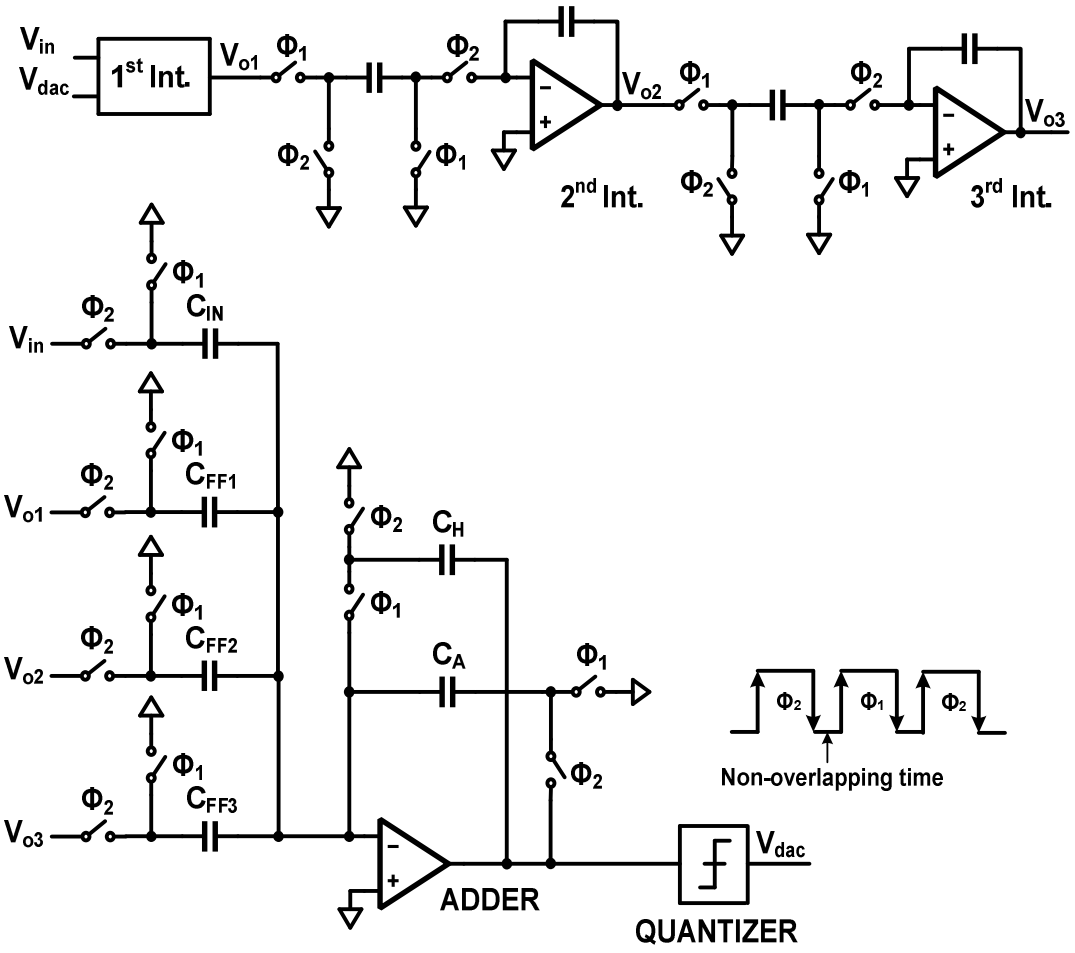


Fig. 5-7. Modified low-distortion ΔΣ ADC.

The nonlinear part is due to the nonlinear capacitances of the switches connected to node V_{x3}. An extra cancellation capacitor C_c and its associated switches can be added to reduce the nonlinearity of the integrator. The value of C_c should be chosen to equal the top-plate parasitic of capacitor C_2, which can be found during layout parasitic extraction. The sizes of switches should be the same (S_1=S_3, S_2=S_4) to cancel the nonlinear capacitances of the switches. Another source of integrator nonlinearity comes from the charge injection from switches S_1 and S_3. Minimizing the switch sizes and using doubled clock signal improves the achievable integrator linearity.

The positions of V_{inp} (V_{inn}) and V_{dacp} (V_{dacn}) can also be swapped. Fig 5-6 shows one of the possible variations.

Fig. 5-7 shows the modified low-distortion (MLD) ΔΣ ADC incorporating the parasitic-insensitive low-power SC integrator as its input stage. On the falling edge of Φ_2, the output of the adder is available. The quantizer performs the quantization during the non-overlapping time, and the DAC control signals are ready before the beginning of next phase Φ_1. Although the input signal entering the modulator loop is not fully cancelled, there is no noticeable increase in the output swings of integrators in Fig. 5-5. Compared to the modulator topology in [5-4], where one full clock period delay was used in the signal feed-forward path, this MLD structure has a half period delay in the signal feed-forward path, and therefore the output swing of each integrator is smaller.

5.4 Simulation Results

The MLD ΔΣ ADC shown in Fig. 5-7, with the proposed parasitic-insensitive low-power SC integrator shown in Fig. 5-5, was simulated assuming a 0.18 μm CMOS technology. All switches in Fig. 5-5 were modeled by real transistors. Switches S_2 and S_4-S_8 were transmission gates. Switches S_1 and S_3 were NMOS switches with doubled clock signals, to reduce the signal-dependent charge injection. Switch S_9 was an NMOS switch. A boot-strapped switch [5-5] could be used here to reduce the size. The sampling clock frequency was 2.56 MHz, the OSR was 32. There were 15 internal quantization levels and the input sampling capacitor C_s of the modulator was 1 pF. Additional 50 fF,

100 fF, 100 fF and 50 fF parasitic capacitors were added at nodes V_{x0}, V_{x1}, V_{x2} and V_{x3}, respectively. A -3 dBFS (FS=1.44 V) 2.03125 kHz sine-wave input was used for the simulation. The computed power spectral density (PSD) of the modulator output is shown in Fig. 5-8. Sampling noise was not included in order better to observe the nonlinearity of the integrator. It can be seen that very high linearity (SFDR=106.2 dB) can be achieved with the new scheme. Simulations also showed that C_c in Fig. 5-5 needs not to be matched exactly with the parasitic capacitor at node V_{x3}, since even large mismatch will cause only small nonlinear errors.

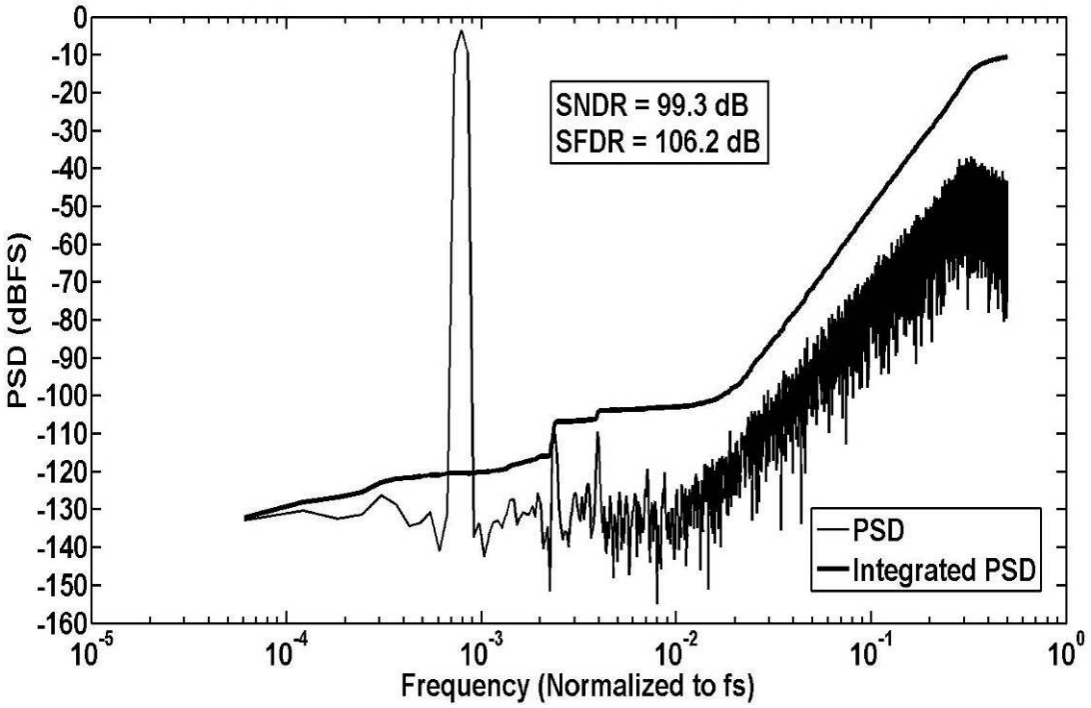


Fig. 5-8. PSD of the modulator output.

5.5 Conclusion

A low-power parasitic-insensitive SC integrator was proposed for ΔΣ ADCs. Simulation with the novel structure verified the achievable high linearity using the new integrator. In an advanced technology where shorter channel lengths may be used, charge

injection and nonlinear parasitic capacitances could be further reduced. Therefore, the linearity of this new integrator can be further improved in an advanced technology.

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Chapter 6 Switched-Resistor Tuning Technique for High Linear Gm-C Filter Design

6.1 Introduction

A new tuning technique is proposed to enable highly linear active Gm-C filter design. The transconductance cells of the Gm-C filter are tuned using switched resistors (SRs) which change the equivalent reference resistance of each cell. In the master tuning circuit, a feedback loop containing a continuous-time comparator is used to force the equivalent resistance of an SR branch to be equal to that of a SC branch. Thus, using the output of the loop with an automatically adjusted duty cycle, all time constants of the Gm-C filter can be tuned simultaneously. A second-order low-pass Butterworth filter model was developed and simulated. The result verified the effectiveness and excellent linearity of the proposed tuning method.

The switched-resistor (SR) technique was introduced to allow the realization of low-voltage highly linear R-C filters [6-1][6-2]. This chapter describes how the SR technique can be used to tune the time constants of Gm-C filters and achieve high linearity at the same time. Gm-C filter tuning methods using triode transconductors [6-3][6-4] or transistors working in triode region as the degeneration resistors [6-5] usually limit the overall achievable linearity of the filters. In both schemes mentioned above, the linearity of the filter relies on the linearity of the transconductance of the transistors in triode region which behave like controlled nonlinear resistors. The proposed SR tuning scheme employs source degeneration resistors and changes their equivalent resistance by changing the average current through the resistors. The SR tuning method doesn't rely on the control of a nonlinear element, and therefore makes the design of highly linear filters possible.

6.2 Transconductance Cell with SR Source Degeneration

Fig. 6-1 shows the schematic of the proposed Gm cell with SR source degeneration. M_1 is the switch in series with resistor R_1. It controls the equivalent resistance of the R_1 branch. The "on" time of M_1 is changed by the tuning signal $V_{tune}(t)$.

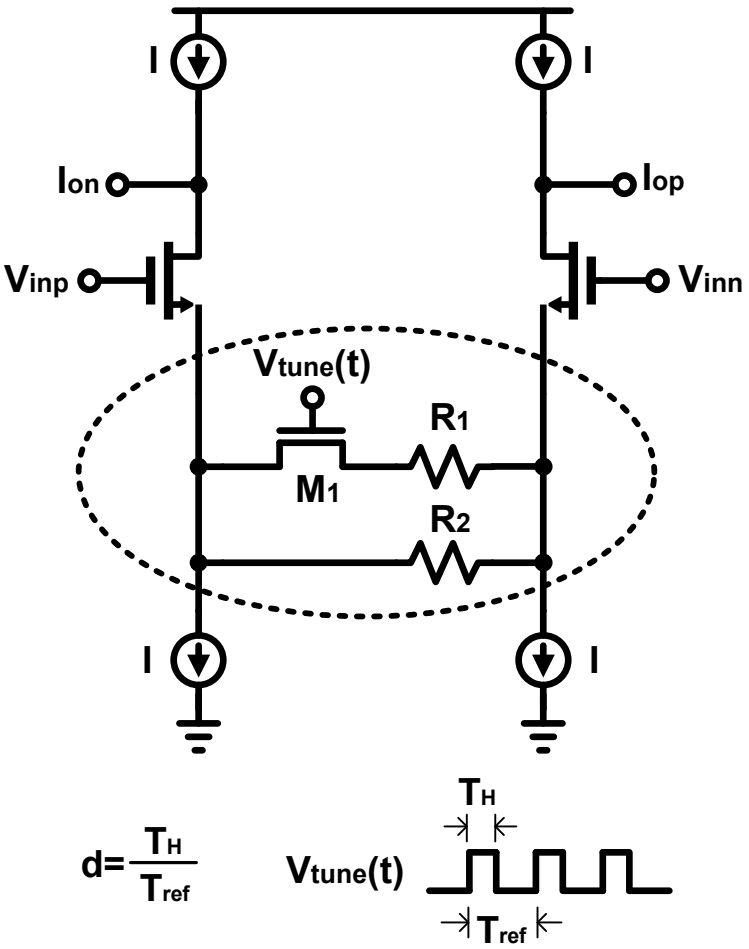

Fig. 6-1. Gm cell with SR source degeneration.

The time-averaged transconductance is given by

$$G_m = \frac{g_m}{1+g_m R_{eq}} = \frac{g_m}{1+g_m(R_2 \,\|\, (R_1 d^{-1}))} \tag{6-1}$$

where g_m is the transconductance of the input devices, d is the duty cycle of the tuning signal $V_{tune}(t)$ and R_{eq} is the average resistance of the SR branch. If $g_m R_{eq} >> 1$, then $Gm \sim 1/R_{eq}$. The tuning range of G_m is

$$G_{TR} = [R_2^{-1} + d_1 R_1^{-1}, R_2^{-1} + d_2 R_1^{-1}] \tag{6-2}$$

where $[d_1, d_2]$ is the duty cycle range of $V_{tune}(t)$. The assumption that the product of the transconductance of input differential pairs and the equivalent resistance of two resistor branches is much bigger than unity was used when deriving (6-2). In the design example used in this chapter, the parameter values $g_m > 20$ mS, $R_1 = 6$ kΩ, $R_2 = 44$ kΩ, $d_1 = 0.2$ and $d_2 = 0.8$ were assumed, satisfying $g_m R_{eq} >> 1$.

The values of R_1 and R_2 should be chosen based on two main conditions. First, the value of R_1 should be much bigger than the nonlinear "on" resistance of switch M_1 to ensure that the linearity of Gm is not affected by the non-linearity of switch M_1. Second, the transconductance tuning range should be large enough to counteract the expected capacitance variation.

When the tuning circuit reaches the steady state, it will generate a tuning signal with a fixed duty cycle for the filter. The periodic variation of the tuning signal $V_{tune}(t)$ will modulate the input signals of Gm cells, and this will generate unwanted tones at frequencies $mf_{tune} \pm nf_{in}$ (m, n=1,2,3…), where f_{tune} and f_{in} are the frequencies of the tuning signal and the input signal, respectively. These tones may be suppressed by limiting the bandwidths of the Gm cells, and by choosing the clock frequency of the tuning circuit sufficiently high. The unwanted tones will be far away from the band of interest if the tuning signal frequency is high enough, and they will be attenuated by the low-pass filter transfer function.

6.3 Design Example

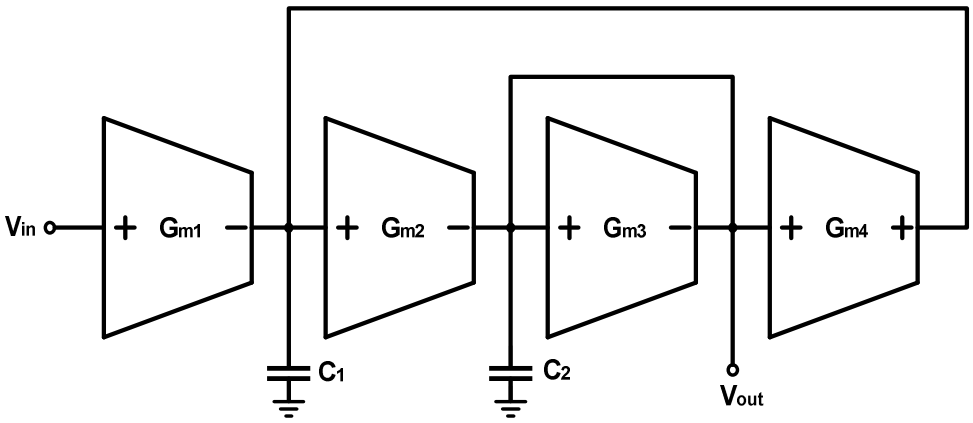

Fig. 6-2. Second-order low-pass Butterworth Gm-C filter.

Fig. 6-2 shows the second-order low-pass Gm-C filter used in the example. A single-ended model is shown for simplicity, although the actual implementation is normally fully differential. $G_{m1}=G_{m2}=G_{m3}=G_{m4}=0.1$mS, $C_2=mC_u=22.5$pF and $C_1=nC_u=45$pF (m, n=1,2,3…, k=m/n=0.5) were used for better matching in layout. Here, C_u is the unit capacitance value used in the layout. The transfer function is

$$\begin{aligned} H(s) &= \frac{V_{out}}{V_{in}} \\ &= \frac{G_{m1}G_{m4}^{-1}}{1+sG_{m3}G_{m2}^{-1}G_{m4}^{-1}C_1+s^2G_{m2}^{-1}G_{m4}^{-1}C_1C_2} \\ &= \frac{1}{1+sG_{m1}^{-1}C_1+s^2k(G_{m1}^{-1}C_1)^2} \end{aligned} \tag{6-3}$$

Therefore, the filter frequency response can be stabilized by keeping the $G_{m1}^{-1}C_1$ products in (6-3) constant. Fig. 6-3 shows the tuning circuit, where P_1 and P_2 are non-overlapping clock phases with a clock period T_{ref}. The output of the (unclocked) comparator $V_{tune}(t)$ is fed back to the gate of switch M_s , and thus the average resistances of the SC and SR branches are forced to be equal. When the tuning circuit reaches the steady state, the equations

$$T_{ref} C_{1t}^{-1} = R_{2t} \,||\, (R_{1t} d^{-1}) = R_{t,eq} \tag{6-4}$$

and

$$C_{1t}^{-1} R_{t,eq} = T_{ref} \tag{6-5}$$

hold, where d is the duty cycle of $V_{tune}(t)$. As the numbers in Fig. 6-3 illustrate, R_{1t}, R_{2t} and C_{1t} can be chosen to be smaller than the values used in the filter, so that the frequency of tuning signal $V_{tune}(t)$ may be high enough, and hence the unwanted tones may be far away from the band of interest. The tuning signal $V_{tune}(t)$ is then used to tune the reference branches in all Gm cells. If the integrator capacitors are well matched to each other and to C_{1t}, all filter time constants will be accurately tuned to track T_{ref}.

Fig. 6-4 shows how the opamp output $V_o(t)$ of the tuning circuit affects the duty cycle of the tuning signal $V_{tune}(t)$. In the slow condition, the current through the two resistors is smaller than that of the typical condition. It takes a longer time in this condition for the opamp output $V_o(t)$ to go down than under the typical condition and the duty cycle is therefore increased. The same analysis applies to the fast condition.

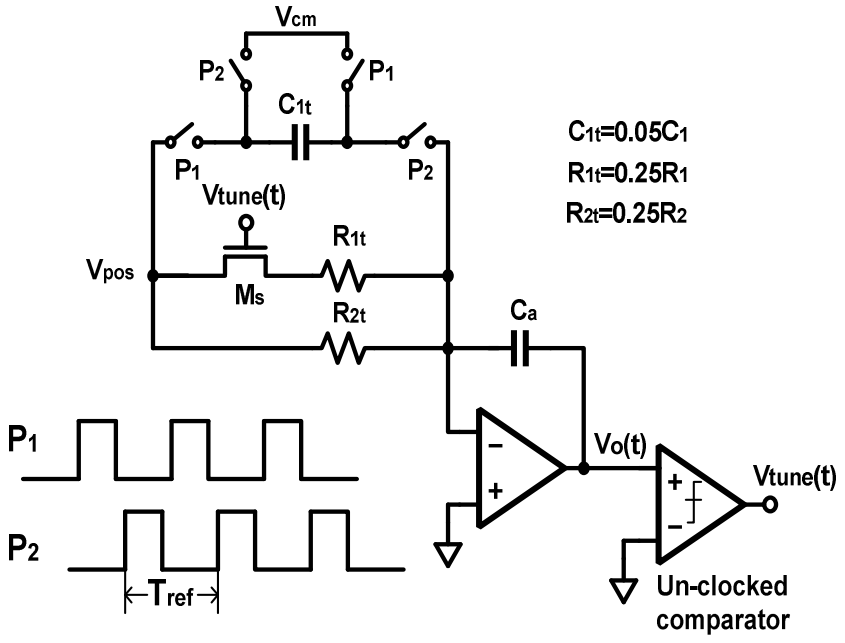

Fig. 6-3. SR tuning circuit.

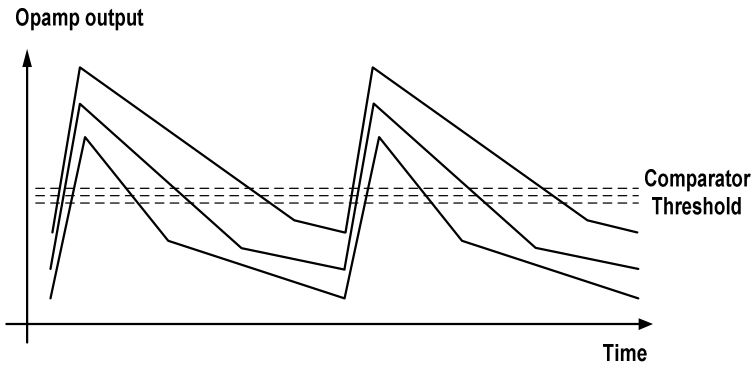

Fig. 6-4. Opamp output of the tuning circuit. Top curve: slow condition (both R and C have a +25% error), middle curve: typical condition (no errors in R and C), bottom curve: fast condition (both R and C have a -25% error).

Note that the tuning circuit is effectively a first-order delta-sigma modulator. The branch containing M_s and the two resistors acts as the feedback DAC, while C_{1t} and its associated switches form the input branch. The tuning performance may be enhanced by adding more integrators into the loop, and thus raising the order of the modulator to 2, or even to 3.

6.4 Simulation Results

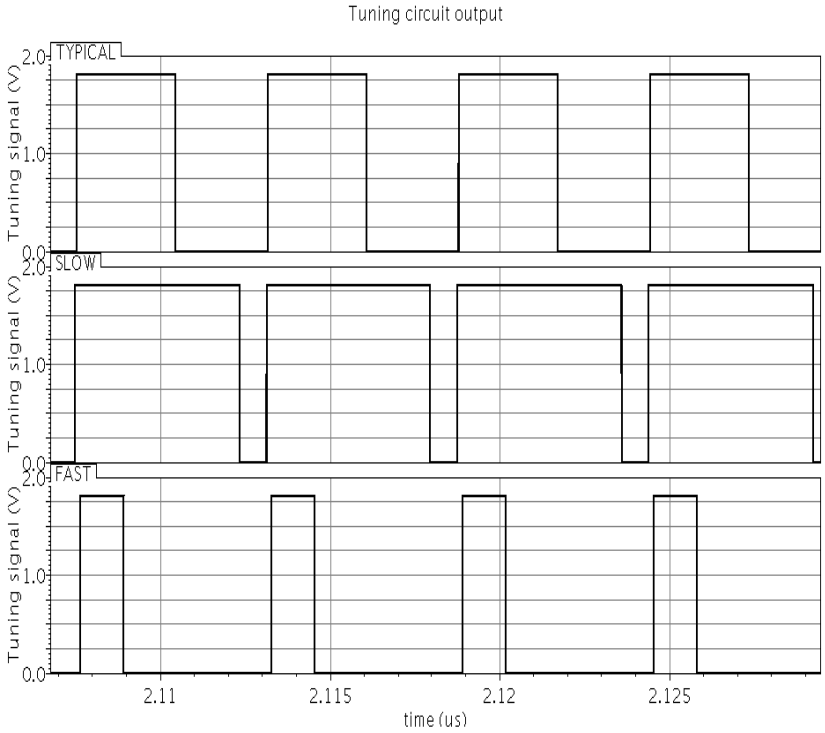

Fig. 6-5. Tuning signal with variable duty cycle.

Fig. 6-5 shows the tuning signal $V_{tune}(t)$ generated by the tuning circuit. The duty cycles are shown for different fabrication conditions: typical (no errors in R and C), slow (both R and C have a +25% error) and fast (both R and C have a -25% error). They vary significantly to compensate for the R and C variations. Figs. 6-6 and 6-7 illustrate the filter frequency response and its cutoff frequency variations under the three different fabrication conditions.

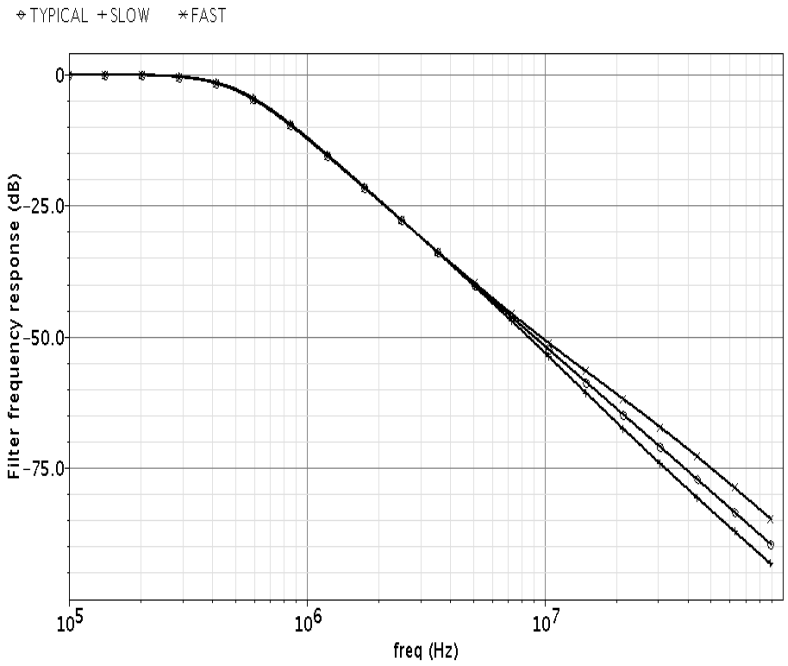

Fig. 6-6. Tuned filter frequency responses under different conditions. Top curve: fast condition, middle curve: typical condition, bottom curve: slow condition.

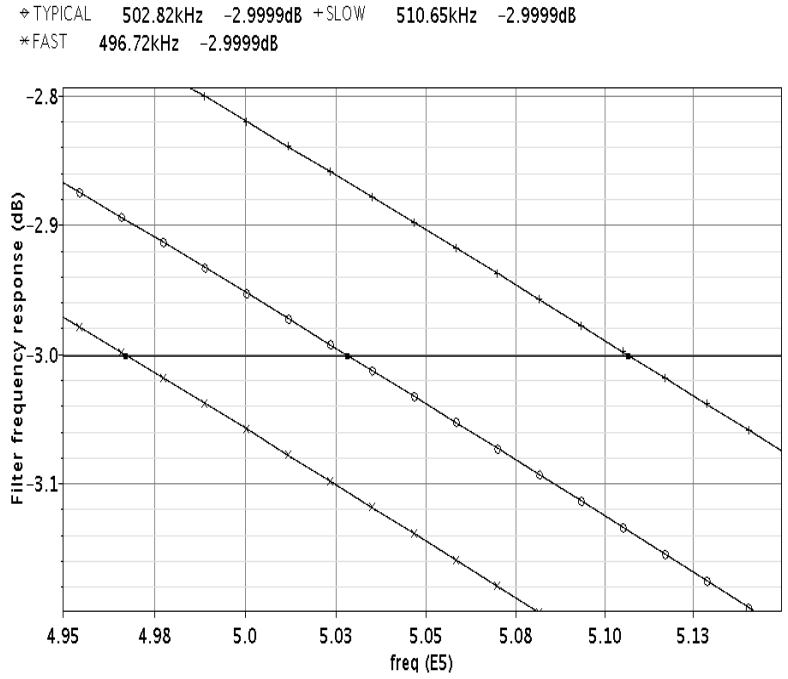

Fig. 6-7. Filter cutoff frequency variation.

The cutoff frequency in the typical case is 500 kHz, and its peak-to-peak variation in the tuned filter is only about 3%, in contrast to the 110% peak-to-peak variation that results without compensation.

Fig. 6-8 shows the spectrum of the filter output with a 2 Vpp, 70 kHz sine-wave input signal. As can be seen from the graph, the spurs introduced by the clock modulation effects are very small, and they occur far from the signal band. This is due to the high tuning clock frequency. Also, there is no noticeable signal distortion due to the tuning process.

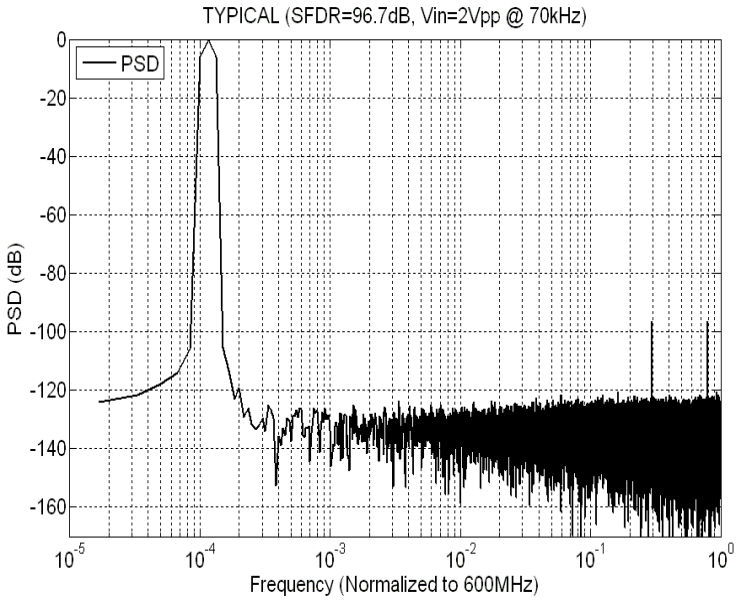

Fig. 6-8. Filter output spectrum.

6.5 Conclusion

A new Gm-C filter tuning method was proposed. It is based on switched-resistor tuning. The tuning process is accurate, and it does not limit the achievable linearity of the filter. Simulation of a typical filter verified the effectiveness of the proposed tuning technique.

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Chapter 7 Conclusions

Chapter 1 describes the application background of the thesis work. The motivation of the thesis work is to come up with architectural innovations so that the total power consumption of the ADC could be greatly reduced.

Chapter 2 first describes two underlying basic principles of delta-sigma modulation: oversampling technique and noise shaping technique. Comparisons are then made between discrete-time DSADC and continuous-time DSADC, between incremental ADC and DSADC, between single-loop and MASH, between single-bit internal quantizer and multi-bit internal quantizer, and between first-order delta-sigma modulator and high-order delta-sigma modulator. Finally, the proposed DSADC featuring two new architectural low-power design techniques is introduced.

Chapter 3 shows the circuit implementation of the proposed DSADC. Main building blocks such as first integrator, second integrator, DCT adder, 15-level internal quantizer, DWA logic, are described in details.

Chapter 4 talks about evaluation platform setup and chip measurement results. Comparisons to the state-of-the-art designs are also made.

Two new design techniques are introduced in chapters 5-6. Chapter 5 describes a low-power parasitic-insensitive switched-capacitor integrator for delta-sigma ADCs. Simulation with the novel structure verified the achievable high linearity using the new integrator, while consuming as low as one quarter of the power of the conventional integrator under the same specifications. Chapter 6 discusses a switched-resistor tuning technique for highly linear Gm-C filter. The tuning process is accurate, and it does not limit the achievable linearity of the filter.