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High-accuracy and high-speed CMOS track-and-hold (T/H) or sample-and-hold (S/H) circuits are an important part of the analog-to-digital interface. The switched-capacitor (SC) circuits usually contain one or more op-amps whose dc offset, finite gain, finite bandwidth have a big impact on the accuracy of the track-and-hold circuit. Basic correlated double sampling (CDS) scheme can reduce such effects, but the compensation that it provides may not be good enough for high-accuracy application. Also, the high-quality analog poly-poly capacitors used in most SC circuits are not available in a basic digital CMOS process. The MOSFET-only predictive track-and-hold circuit, discussed in this thesis, replaces the poly-poly capacitors with easily-available low-cost area-saving MOSFET capacitors biased in accumulation region. It also uses the predictive correlated double sampling (CDS) scheme, in which the op-amp predicts its output for the next clock period during the present clock period, so that the adjacent two output samples are nearly the same. The predictive operation results in more correlation between the unwanted signal and the signal that is subtracted during the double sampling, and hence can achieve offset and gain compensation over wider frequency range. Hence, this circuit is suitable for high-accuracy applications, while using only a basic digital process.

MOSFET-Only Predictive Track and Hold Circuit

by

Xiangping Qiu

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Chapter 1. Introduction

High-accuracy and high-speed CMOS track-and-hold or sample-and-hold circuits form an important part of the analog-to-digital interface. The op-amp's dc offset, finite gain, finite bandwidth all have big impact on the accuracy of the track-and-hold circuit (T/H). The CDS (correlated double sampling) scheme, effective in reducing these effects at lower frequency, may not be good enough at higher frequencies up to half of the sampling rate. Also the high-quality analog poly-poly capacitors used in most switched-capacitor circuits are not available in a basic digital process. This work is aimed at solving such problems.

In Chapter 2, we discuss the nonlinearity of the capacitor implemented by MOSFET. With a more exact analysis of the capacitor in the accumulation region, we have its nonlinear relationship and find out how its nonlinearity depends on process variation.

In Chapter 3, we first explain the basic CDS (correlated double sampling) idea. Two basic examples are the resetting compensation T/H circuit and the inverting tracking mode T/H. Then we introduce the predictive CDS method, which is used in the chip implemented. To have a good understanding of the circuit, gradual improvements leading to the final implementation are explained, which include improved switching, more balanced load in different phases and new settling phase inserted to alleviate the error caused by the change of opamp gain in tracking and holding phases. We also explain some additional considerations for using MOSFET-only capacitors and driving off-chip capacitance. Detailed schematics specifying transistor size are shown and the post-layout simulation results are also given.

In Chapter 4, we examine the circuit nonideality's impact on the performance and show that the circuit design is good enough to satisfy the performance without imposing stringent requirement on the components . Those practical considerations include non-zero and non-linear on-resistance of the switches, nonideal aspects of op-amp (finite gain, finite bandwidth, non-zero output resistance, finite slew rate), thermal noise caused by the switches and the noise caused by the op-amp with emphasis on the sampling and holding's effect.

Finally in Chapter 5, a summary is given and topics for future work are recommended. We can apply predictive CDS schemes in SC filters like the post-filter in the delta-sigma DAC. Also, we can use series or parallel branches in the main circuit to further reduce the harmonic distortion caused by the nonlinearity of MOSFET capacitors.

Chapter 2. MOSFET capacitor's nonlinearity

2.1 Introduction and gate structure

Most analog processing blocks use highly-linear, low-voltage coefficient, uniform poly-poly capacitors which are obtained at extra fabrication cost. Therefore it is desirable to find an alternative way. MOSFET capacitors, by contrast, are available in any digital process, have large capacitance per unit area due to the thin oxide , and good matching properties (relative mismatches of MOS gate capacitance are as low as 0.02% have been reported [1]). However, their voltage coefficients are bigger.

Fig. 2-1 shows four gate structures that can be employed as capacitors in a p-well CMOS process. The first two need to be operated in the accumulation region while the other two need to be operated in the inversion region.

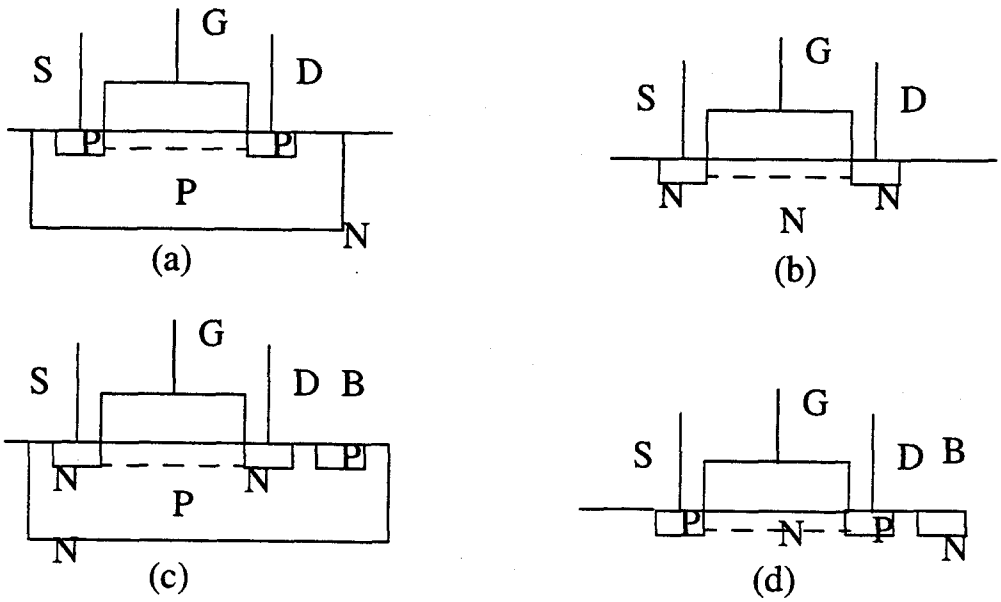

Figure 2.1: Gate structure in a p-well CMOS technology

The model for the MOS capacitor with V_{ds}=0, valid for low and medium-frequency operation is shown in the Fig.2.2. In accumulation configuration, the S, D, B are physically shorted. In strong inversion region, to remove the effects of reverse biased substrate junction capacitance, V_d=V_s=V_b is set. Thus in usual linear approximation, we have.

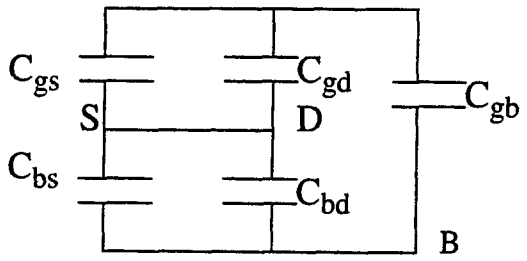

Figure 2.2: Intrinsic capacitances of the MOSFET when V_{ds}=0

In strong inversion : $C_g = C_{gs} + C_{gd} + C_{gb} \approx \frac{C_{ox}}{2} + \frac{C_{ox}}{2} + 0 = C_{ox}$

In accumulation: $C_g = C_{gs} + C_{gd} + C_{gb} \approx C_{ox}$

We also notice that the overlap capacitances are in parallel with C_{gs} and C_{gd}. Also, the possible well-to-substrate capacitance needs to be considered. To make the MOSFET capacitance linear, we need to either bias it in the accumulation region or in strong inversion. For capacitors grounded or almost grounded (like connected to the virtual ground of the op-amp), we can do it in quite a direct way.

2.2 Accurate model of the MOSFET gate capacitance

In the usual analysis of the MOSFET capacitance, we neglect the thickness of the surface channel. In such case, the C_g in inversion is a constant when V_d=V_s=V_b. To

determine the relationship of C_g to V_g, we have to make more appropriate assumptions [1]. Let's take a NMOSFET as an example. The conclusion is valid also for PMOS, except for some polarity changes. We have the following equations, valid for nondegenerate silicon:

$$V_{GB} = V_{FB} + \psi_s - Q'_c / C'_{ox} \tag{2.1}$$

$$Q'_c = -\mathrm{sgn}(\psi_s) F \sqrt{N_A \phi_t} \left\{ \exp\left(\frac{-\psi_s}{\phi_t}\right) + \frac{\psi_s}{\varphi_t} + \exp\left[\frac{\psi_s - (2\phi_F + V_{SB})}{\phi_t}\right] - 1 \right\}^{0.5} \tag{2.2}$$

where ψ_S represents the surface potential, ϕ_F is the Fermi potential, ϕ_t is the thermal voltage, V_{FB} is the flat-band voltage, V_{GB} is the gate-to-bulk voltage, Q_c' is the total semiconductor charge per unit area, and C_{ox}' is the oxide capacitance per unit area. From the above, the small-signal gate capacitance per unit area is given by:

$$C'_g = \frac{d}{dV_{GB}} Q'_G = \frac{-dQ'_c}{dV_{GB}} \tag{2.3}$$

where $C'_g = C'_{gs} + C'_{gd} + C'_{gb}$

as $V_{BS} = V_{DS} = 0$, the non-linear junction capacitance is 0. The C'_g can be considered as the serial combination of the oxide capacitance and the semiconductor space charge capacitance:

$$\frac{1}{C'_g} = \frac{1}{C'_{ox}} + \frac{1}{C'_c} \text{ where } C'_c = \frac{-dQ'_c}{d\psi_s} \tag{2.4}$$

A. Accumulation region: If we just retain the dominant exponential term in (2.2), then we have the following approximation:

$$Q'_c \approx F \sqrt{N_A \phi_t} \exp\left(\frac{-\psi_s}{2\phi_t}\right) \tag{2.5}$$

Therefore we have,

$C'_c = -\frac{dQ'_c}{d\psi_s} \approx \frac{Q'_c}{2\phi_t}$, then substituting (2.1), we get

$$C'_c \approx \frac{Q'_c}{2\phi_t} = \frac{(V_{GB} - V_{FB} - \psi_s)C'_{ox}}{2\phi_t} \approx C'_{ox}\frac{V_{GB} - V_{FB}}{2\phi_t} \qquad (2.6)$$

where ψ_s has been neglected in the numerator of (2.6), because in this region ψ_s is small. (a very small ψ_s is enough for exponential increase of Q'_c --meaning much larger voltage on oxide than silicon). Hence, the semiconductor space-charge capacitance depends almost linearly on the gate voltage. The total gate capacitance is then given by

$$C'_g \approx C_{ox}\left[1 - \frac{2\phi_t}{|V_{GB} - V_{FB}| + 2\phi_t}\right] \qquad (2.7)$$

which applies both in NMOS and PMOS. For the analysis for circuits with weakly nonlinear components it is useful to obtain the power series expansion of the nonlinear term around a bias voltage V_R. From (2.4) it follows that

$$C'_g = \frac{C'_{ox}}{1 + C'_{ox}/C'_c} = C'_{ox}\left(1 - \frac{C'_{ox}}{C'_c} + \left(\frac{C'_{ox}}{C'_c}\right)^2 - \ldots\right) \qquad (2.8)$$

From (2.6) and (2.8), writing $V_{GB} = V_R + V$ where V_R is the dc bias voltage and $V << V_R$

$$C'_g \approx C'_{ox}\left(1 - \frac{2\phi_t V}{(V_R - V_{FB})^2} + \frac{2\phi_t V^2}{|V_R - V_{FB}|^3} + \ldots\right) \qquad (2.9)$$

B. Strong inversion: The total semiconductor charge Q'_c is the sum of the inversion-layer charge and the depletion-region charge. Assuming that the depletion charge is constant and the inversion charge varies exponentially with the surface potential, it follows that

$$-Q'_C \approx F\sqrt{2N_A\phi_F} + F\sqrt{N_A\phi_t}\exp\left(\frac{\psi_s - 2\phi_F}{2\phi_t}\right)$$

which results in: $$-Q'_c \approx F\sqrt{2N_A\phi_F} + 2\phi_t C'_c$$

Substituting the above Eq. in (2.1), we get

$$C'_c \approx C'_{ox}\frac{|V_{GB} - V_T|}{2\phi_t} \tag{2.10}$$

where ψ_s was assumed to be equal to $2\phi_F$ and V_T is the classical strong inversion threshold voltage. The total gate capacitance is given by

$$C'_g \approx C'_{ox}\left[1 - \frac{2\phi_t}{|V_{GB} - V_T| + 2\phi_t}\right] \tag{2.11}$$

Therefore, in strong inversion, a power series analogous to (2.9) for the gate capacitance is valid if V_{FB} is substituted by V_T. The error in this case is usually larger than for accumulation. The approximation is still good enough to model weak nonlinearities of C_g' in strong inversion. We end this Section with a comment on the weak non-linearities of MOSFET capacitance either in accumulation or strong inversion with their strong non-linearities in flat-band condition. The voltage coefficient in the latter case is given by

$$V_{cc} = \frac{1}{C_g}\left|\frac{dC_g}{dV_{GB}}\right| = \frac{C'^{\,2}_{ox}}{3q\varepsilon_{sc}N_A} \tag{2.12}$$

while in the accumulation it is $$V_{cc} \approx \frac{2\phi_t}{(V_R - V_{FB})^2} \tag{2.13}$$

in the strong inversion it is $$V_{cc} \approx \frac{2\phi_t}{(V_R - V_T)^2}. \tag{2.14}$$

In flat-band condition the voltage coefficient (2.12) has a strong dependence on the technological parameters C_{ox}' and N_a. On the other hand, both in strong inversion and accumulation, the voltage coefficients are asymptotically independent of technological parameters. For a 5-V technology, typical V_T values range from 0.6 to 1.0 V. If a bias voltage equal to 2.5 V is applied to a gate capacitor in such technology, the voltage capacitance coefficient lies between 14 and 22 kppm/V.

Chapter 3. Predictive track and hold circuit

The nonlinearities of MOSFET capacitor were evaluated in last chapter. In this chapter, we shall analyze the principles of a track and hold circuit [3][4] implemented using MOSFET capacitors.

3.1 Correlated double sampling (CDS)

The basic idea of CDS is to sample the unwanted quantity in one phase, sample the signal plus the unwanted quantity in another phase and then substract it from the one in the first phase , after which a cleaner signal output can be obtained. A resetting T/H circuit using the basic scheme is shown in Fig. 3.1 [2]. Similar basic schemes for amplifiers, and comparators can be found in [5]. In ϕ_1, capacitor C is charged to the input signal and the combined-input-referred offset and noise. In ϕ_2, the left plate of the capacitor is connected

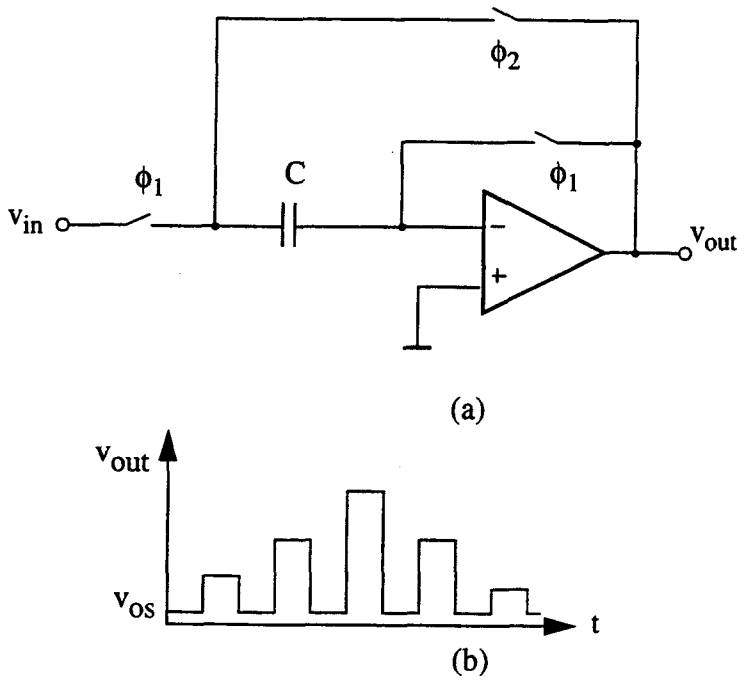

Figure 3.1: Resetting compensation T/H circuit

to the output of the opamp. If the opamp is an ideal one, then the output in ϕ_2 will be exactly the signal at the end of the last ϕ_1. In the non-ideal opamp case, the output error will be the difference between the negative input values of the opamp during the two phases, that is $V_{outerr}(nT) = v_{os}(nT) - v_{os}(nT - T/2)$. The transfer function from V_{os} to V_{outerr} is (1-$z^{-1/2}$) which highpassed the input error. But in this circuit, the opamp is reset to V_{os} in ϕ_1, therefore, the opamp needs a high slew rate. A modified gain and offset compensated track and hold circuit was proposed by Wang and Temes [4] in 1987. It is shown in Fig.3.2.

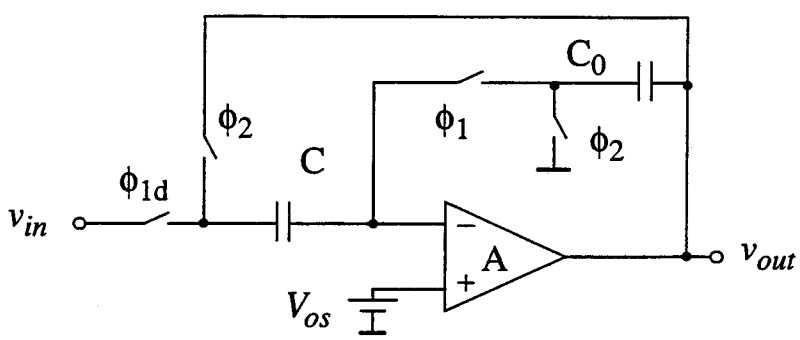

Figure 3.2: Non-predictive CDS track/hold circuit

In phase 1, the input capacitor C and feedback capacitor C_0 make the circuit operate in inverting tracking mode while C is charged to v_{in} and the offset. In phase 2, the left plate of C is flipped to the output of the opamp to implement the holding function. In this circuit, in spite of the inverted tracking in ϕ_1, which causes the output to swing away from the next holding value, it is less than the swing in the previous resetting compensation circuit when the input changes slowly, thus providing a reduced sensitivity to the finite dc gain of the opamp when the input frequency is much lower than the clock frequency. Analysis shows that when the input signal is approaching half of the sampling rate, the error will actually be greater than for the one without compensation because the output will swing from one peak to another peak with inverted tracking. The delayed cutoff ϕ_{1d} is used to reduce signal-dependent distortion.

3.2 Predictive CDS track/hold circuit

3.2.1 Basic predictive track/hold circuit

To change the inverted tracking in the previous circuit, the predictive version is shown in the Fig 3.3 [3]. In phase 1, the circuit is in a noninverting tracking mode because of the help of the added capacitor C_2, whose value is twice as big as C_1 which is connected to the non-inverting input in this phase and charged to $v_{c1} = v_{in} - V_{os} + v_{in}/A_1$ Assuming

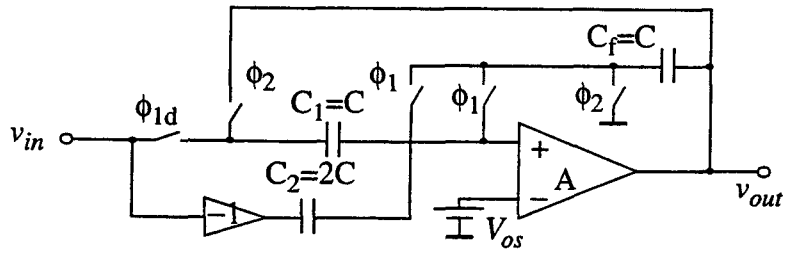

Figure 3.3: Basic predictive track and hold circuit

ideal tracking, when phase 2 turns high, the output will be $v_{out} = V_{os} - v_{out}/A_2 + v_{c1} = v_{in} + v_{in}/A_1 - v_{out}/A_2$. If A_1 and A_2 are exactly the same, then v_{out} is exactly the same as v_{in}. If not, then the order of the difference will be around the square of the gain, thus greatly enhancing the accuracy. Also in this circuit, the linearity of tracking is less important than in the previous ones, thus the matching requirement between C_1 and C_2 is reduced. The above circuit can easily be implemented in a differential form, thereby reducing the common-mode noise and even-order distortion. One of the disadvantages of this circuit is that in the holding phase, the right plate of C_2 is floating while the left plate is connected to the continous input signal. This makes the voltage across C_2 unchanged in the hold phase and it'll take more time for the output to settle in the next tracking phase.

3.2.2 *Improved switching predictive track/hold circuit*

A solution to this problem is shown in Fig. 3.4(a-c). The value of the four capacitors are same. During the tracking phase shown in Fig. 3.4(b) we have the C_3 and C_f path implement the tracking function. The charge on the sampling and holding capacitor C_1 is balanced by the charge on C_4 (note that C_4 is connected to $-v_{in}$ while C_1 is connected to

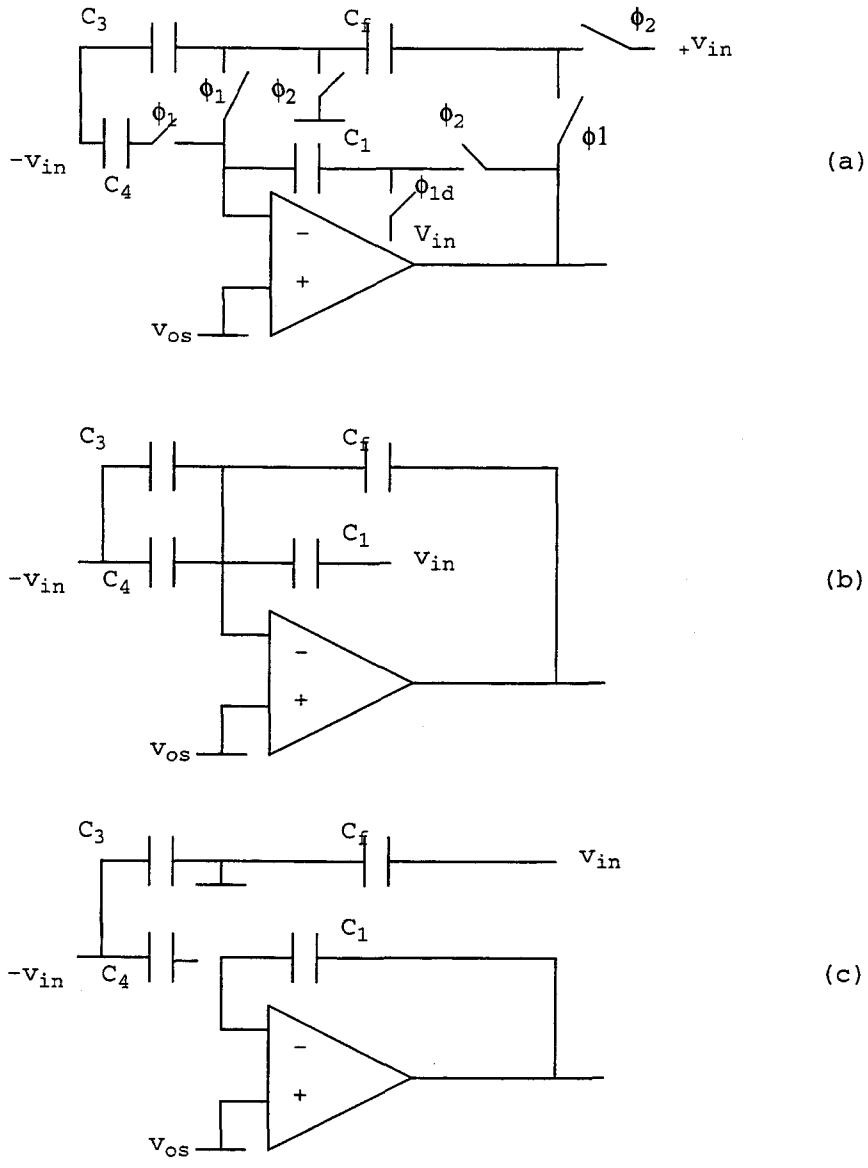

Figure 3.4: Improved switching track and hold circuit
(a) full circuit (b) tracking (c) holding

v_{in}). In the holding phase (Fig. 3.4c), the right plate of C_1 is connected to the opamp output while C_3 are precharged to $-v_{in}$ and C_f to v_{in} thereby speeding next tracking transience. We can use two track/hold circuits either in cascade or in parallel to realize the sample and hold function. In the latter way the speed of sampling and holding is twice as fast as that of the track and hold circuit (Fig 3.5). When the upper T/H circuit is tracking, the output of the

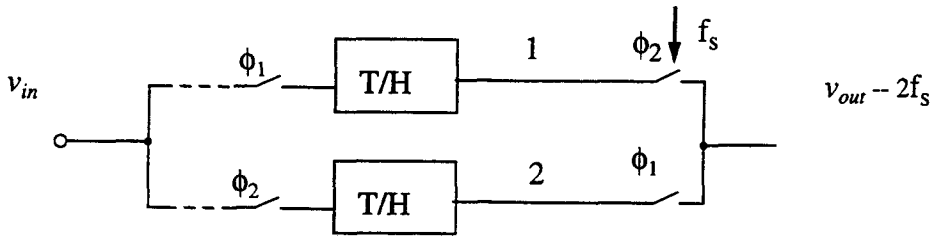

Figure 3.5: Pingpong structure to realize S/H

whole circuit is the output of the lower T/H circuit which is in the holding phase. In the next phase, the situation is just the reverse. Because both T/H circuits are insensitive to the matching of the capacitors , the final mismatch error can be neglected.

Let's analyze the effective load in the two phases of the circuit. A general diagram for such a circuit is shown in Fig. 3.6.

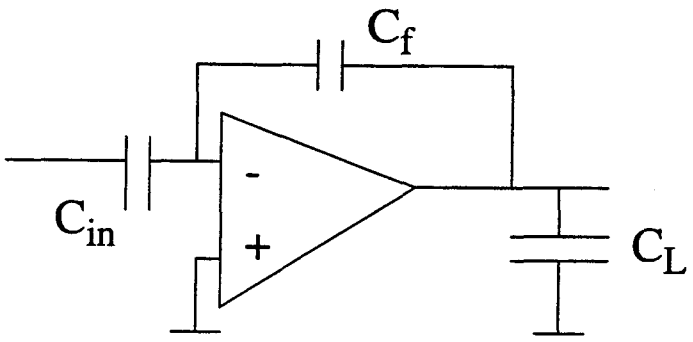

Figure 3.6: General circuit representation of feedback switched circuit.

The effective load is:

$$C_{eff} = C_{in} + C_L + \frac{C_{in}C_L}{C_f}$$

For the track and hold circuit discussed just before, the effective load for the two phases can be calculated:

tracking: $C_{in} = C_1 + C_3 + C_3 + C_{inpara} \approx 3C \quad C_{eff} = 3C + C_L + (3CC_L)/C_f$

holding: $C_{in} = C_{inpara} \quad C_{eff} = C_{inpara} + C_L + (C_{inpara}C_L)/C_1$

Here, C_{inpara} denotes the parasitic capacitance at the input of the opamp. Therefore we can see that the effective loads in the tracking and holding phases are not balanced. What's more, it is observed that the sampling and holding capacitor C_1 is charged between the input signal and the virtual ground of the opamp, which makes the transition from tracking to holding more sensitive to the opamp.

3.2.3 *Balanced-load predictive track/hold circuit*

A better way of dealing this problem is to make the holding capacitor charge between the input signal and a fixed ground instead of the virtual ground of the opamp. It is shown in the following Fig. 3.7.

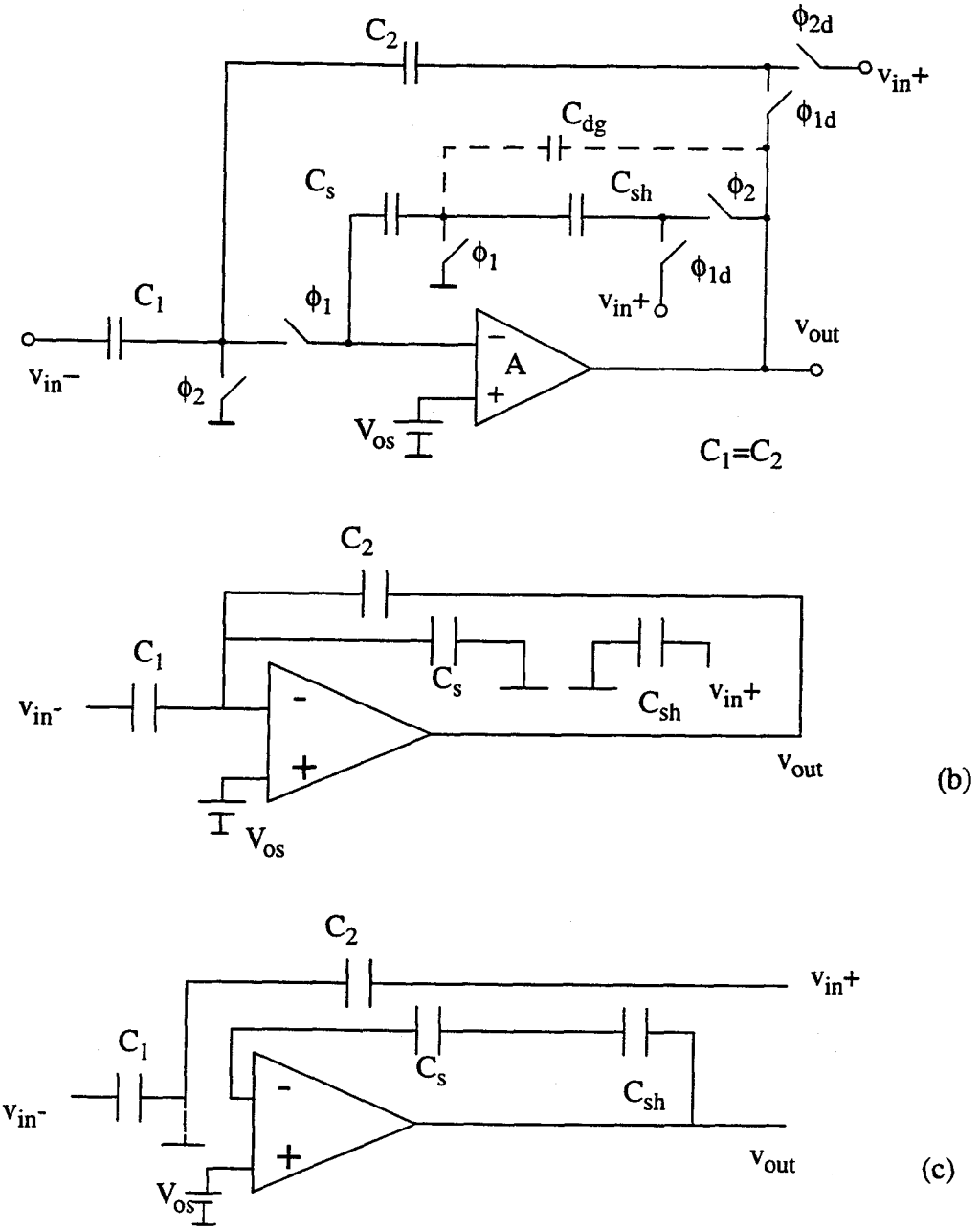

Figure 3.7: Improved version of the T/H circuit utilizing the error- storage capacitor to make the opamp load more balanced (a) full circuit (b) tracking (c) holding

It can be seen that in the tracking phase, the number of capacitors connected to the virtual ground is reduced from three in previous circuits to two in this circuit.

3.2.4 Track-settle-hold predictive track/hold circuit

In the above predictive CDS circuits, it can be observed that the difference between the opamp gains in the tracking and holding phases will affect the accuracy of the compensation. In the last version of the circuit, the opamp is connected to a continous signal in the tracking phase while connected to an almost fixed signal in the holding phase. As we know, the gain near dc (almost fixed signal) can be ten times or more larger than the gain in the tracking phase when the opamp is connected to the changing input whose frequency is one or two orders above the first pole of the opamp. Therefore, an inserted settling phase in which the changing input is disconnected from the opamp will reduce the error caused by this gain difference. The clock phases are shown in Fig. 3.8. The full single-ended final version is shown in Fig. 3.9(a-d).

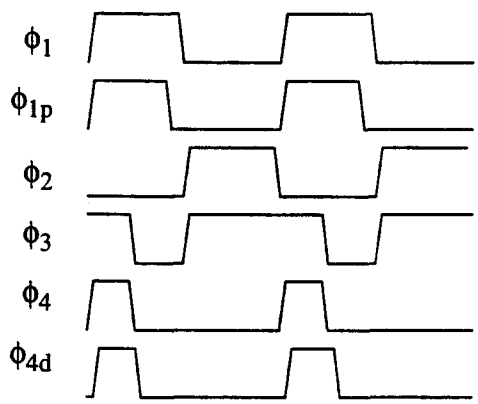

Figure 3.8: Clock phases of the T/H circuit

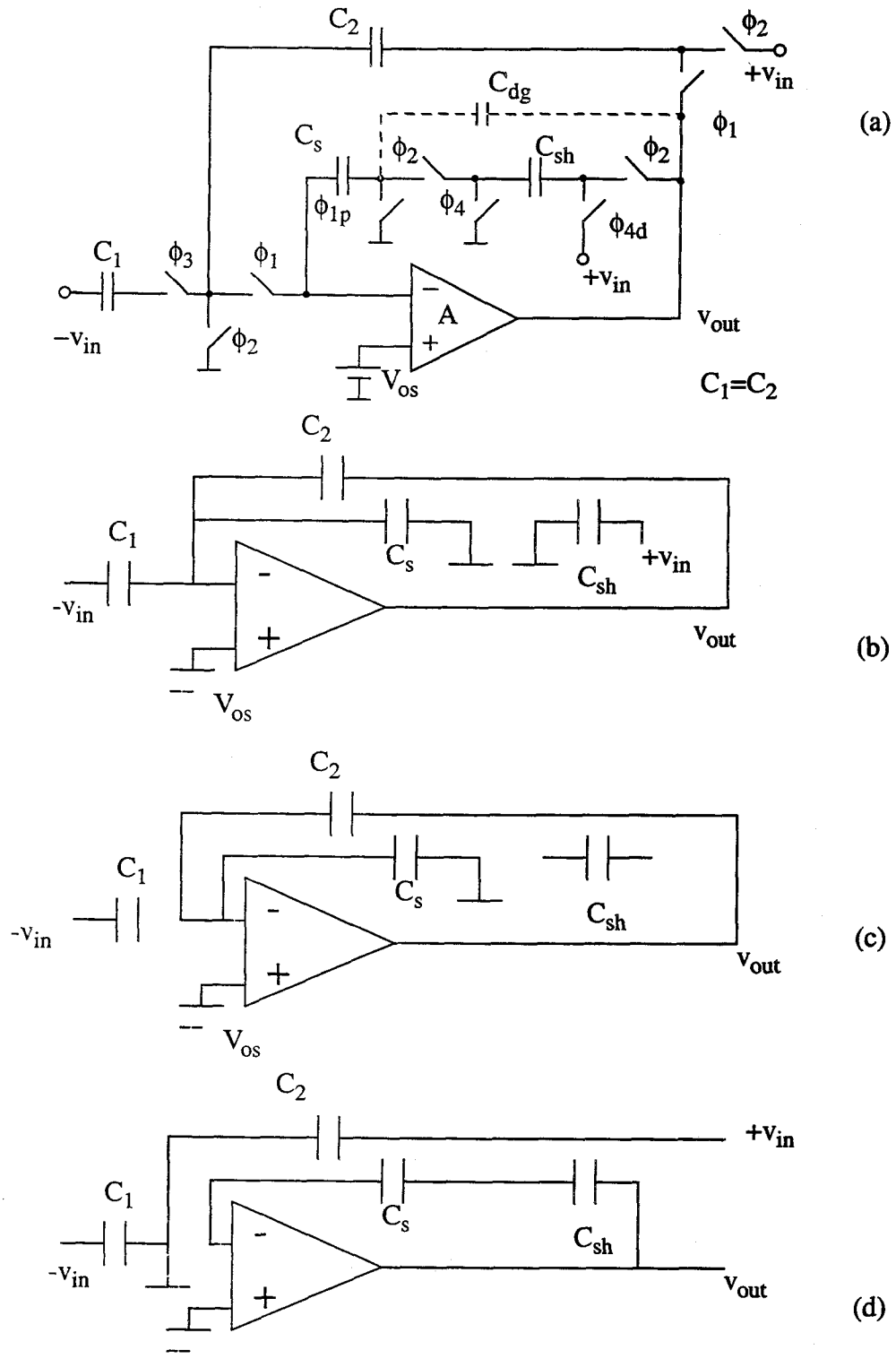

Figure 3.9: Single-ended final version of the track-settle-hold predictive T/H circuit (a)full circuit (b) tracking (c)settling (d) holding

3.3 Implementation and post-layout simulation results

Because this test chip needs to drive directly the off-chip pin whose capacitance is assumed to be around 15 pF, the requirement on speed must be reduced compared to what it would be if it were driving, e.g., an on-chip ADC. With balanced consideration on power and frequency, the switch size is smaller than it would be otherwise if it would be integrated with other systems on the chip, e.g., several switches sizes were changed from 20 μm to 12 μm in this circuit. Also the switches connecting the wide-swing signal are bigger than the ones connected to lower-swing signal in order to reduce the effects of greater nonlinearity of MOSFET switch on-resistance under bigger swing. The actual implementation is the fully differential one shown in Fig. 3.10 and Fig. 3.11. New analog ground pins agd_b agd_e are added in the main circuit to bias the MOSFET capacitors in charge transfer path. The bottom plate of C_s is connected to the input of the opamp. In order to bias it in the accumulation region as other capacitors, the opamp is designed to be able to work at low input common-mode (CM) voltage (it works at 0 V common mode in our simulation). There are two T/H blocks sharing a clock generator. The transistor sizes of the track and hold stage are also shown in Fig. 3.11. The clock generator is shown in Fig. 3.12. The op-amp used in this circuit is shown in Fig. 3.13. It has a dc gain of 60 dB, a unit-gain-frequency at 33 MHz and a phase margin of 80 degree as shown in Fig. 3.14. As will be shown in the nonideal effects analysis in next chapter, these parameters are adequate. The "w/l" or "w\l" symbol on the transistor means its width w and length l. For parallel transistors, the number m of unit devices is shown as in $\frac{w/l}{m}$ or $\frac{w\backslash l}{m}$.

Additional consideration is the common-mode-feedback (CMFB) circuit, which is on the right side of the stage shown before in Fig. 3.11. The MOSFET capacitors C_{cm_c} are always charged between the opamp output nodes and the CMFB node. Since the output can swing down to 0.5 V from its CM (2.5 V) and the CMFB node changes very little around

1.1 V, if we directly biased a MOSFET capacitor between them, then it wouldn't be always in accumulation region. Therefore each C_{cm_c} is split into a pair of series MOSFET capacitors. Similarly each C_{cm_h} is also split into a pair of series MOSFETs to improve the linearity. A new pin $v_{biasmos}$, is added for setting the voltage of the common node of the series capacitors. The difference between C_{cm_c} and C_{cm_h} is this: without splitting, C_{cm_c} can be out of accumulation region. But without splitting, C_{cm_h} will be in less linear accumulation region. Another reason for splitting C_{cm_h} is to help set the bias of the split C_{cm_c} in ϕ_1. Although the deeper the MOSFET capacitor is biased in the accumulation region, the better its linearity, we don't set $v_{biasmos}$ too high as when ϕ_1 turns high, the swing of the common node of the two series MOSFET capacitors may be so high that the switches which are connected to $v_{biasmos}$ and supposed to be "off" may be "on".

The simulated differential input and differential output signals are shown in Fig. 3.15. The frequency of the input signal is 100 kHz, the clock rate of the T/H is 1 MHz, the final output sample-and-hold rate is 2 MHz. The post-layout simulation gives 80 dB STHD. As the input signal frequency goes up, the STHD will decrease gradually. Fig. 3.16 shows the two T/H outputs and the final S/H output. It can clearly be seen that the two T/H are working in turns generating the holding wave. Fig. 3-17 shows the impact of the CM on the T/H output of this circuit. For example, from about 19.76 μs to 20 μs, which is the holding phase of one T/H, both positive output and negative output of that T/H have a CM shift. But they are cancelled in the differential output. The layout of the circuit is shown in Fig. 3-18. THA1 denotes the first track and hold stage. THA2 denotes the second one. OP_BIAS means the op-amp bias circuit. The CMFB1 and CMFB2 denote the CMFB circuit for the op-amps in THA1 and THA2 respectively. This chip has been submitted to the Orbit1.2 μm process for fabrication. It will be tested when received at OSU.

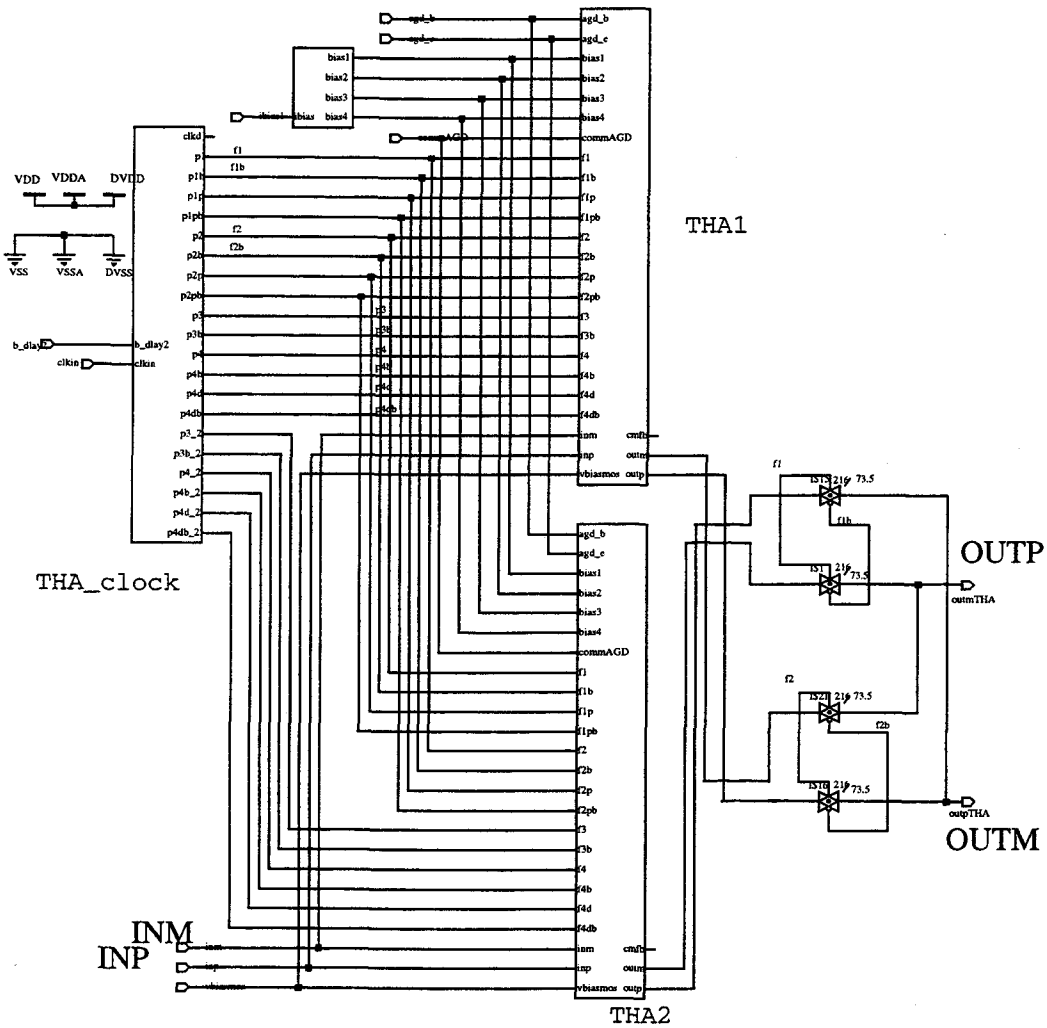

Figure 3.10 The block diagram of the T/H circuit

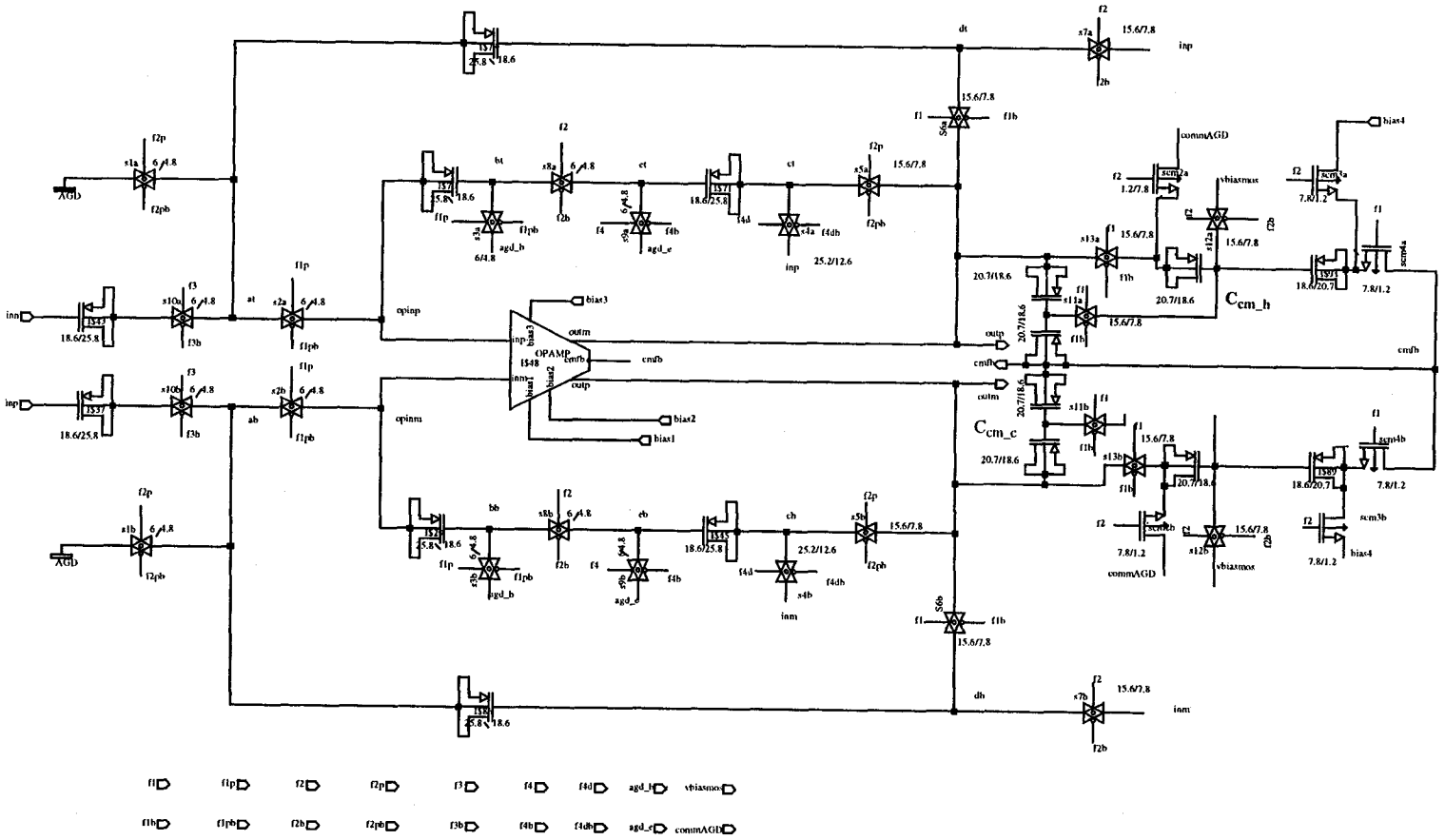

Figure 3.11 Predictive MOSFET-only track and hold circuit

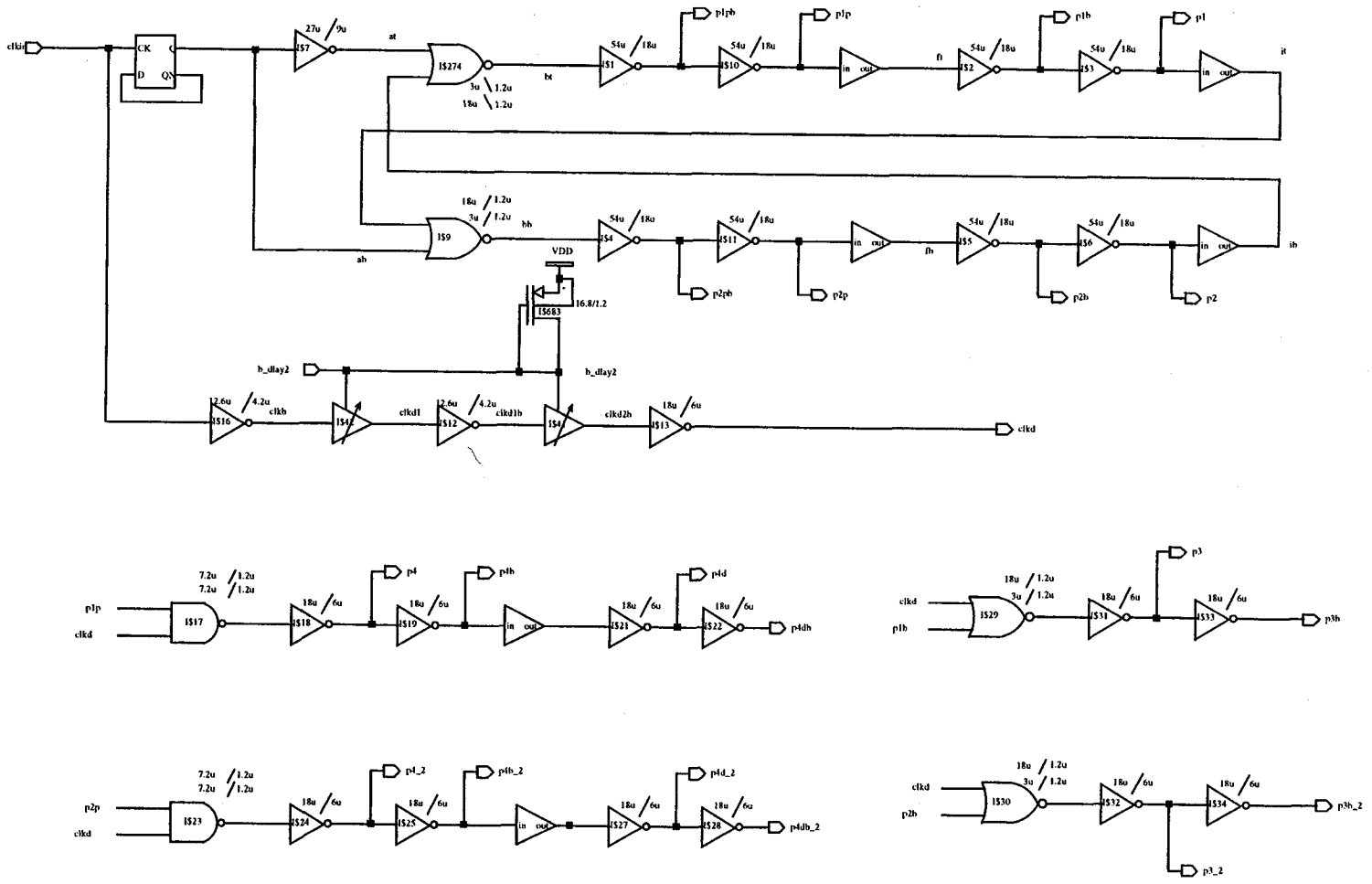

Figure 3.12 The clock generator of the T/H stage

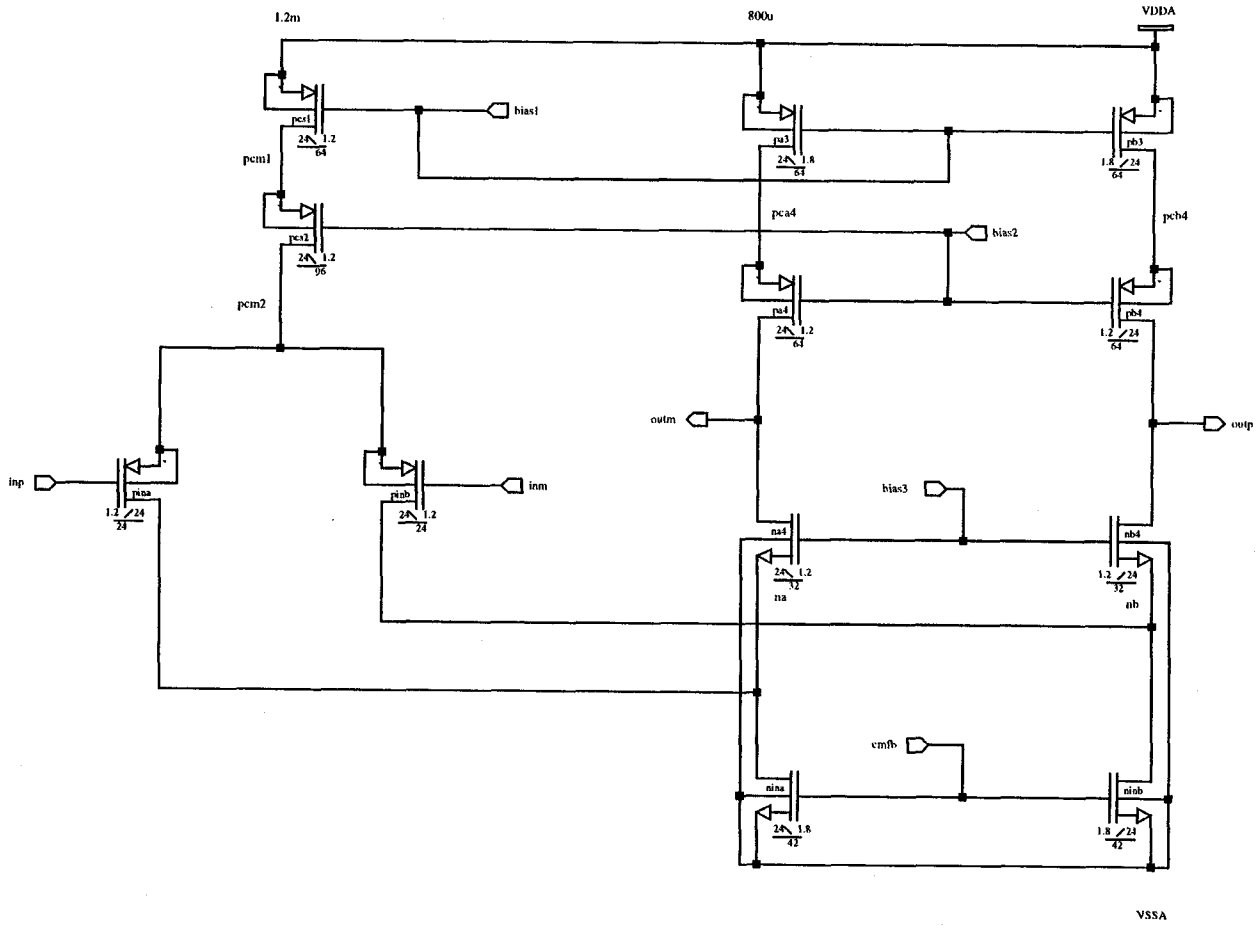

Figure 3.13 The folded-cascode op-amp used in the T/H stage

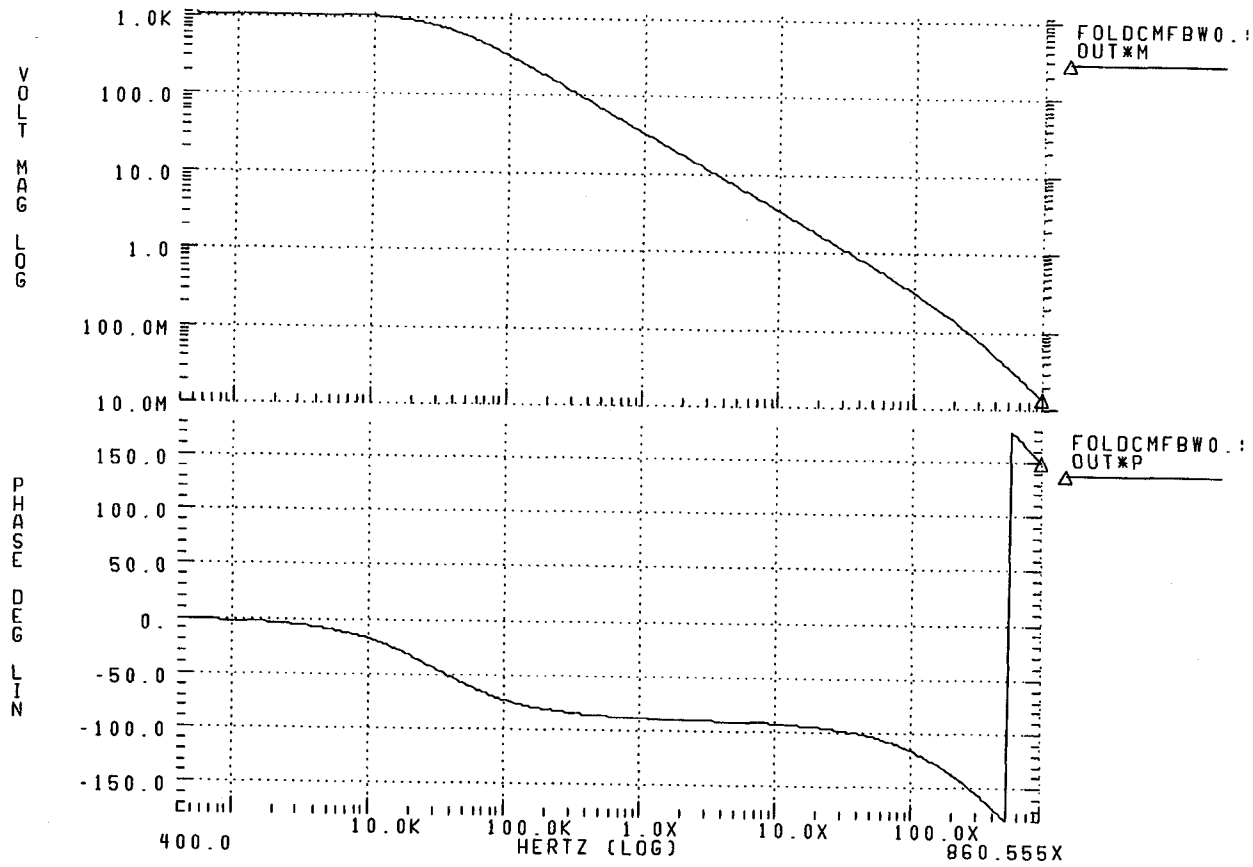

Figure 3.14: AC performance of the opamp used in the T/H circuit

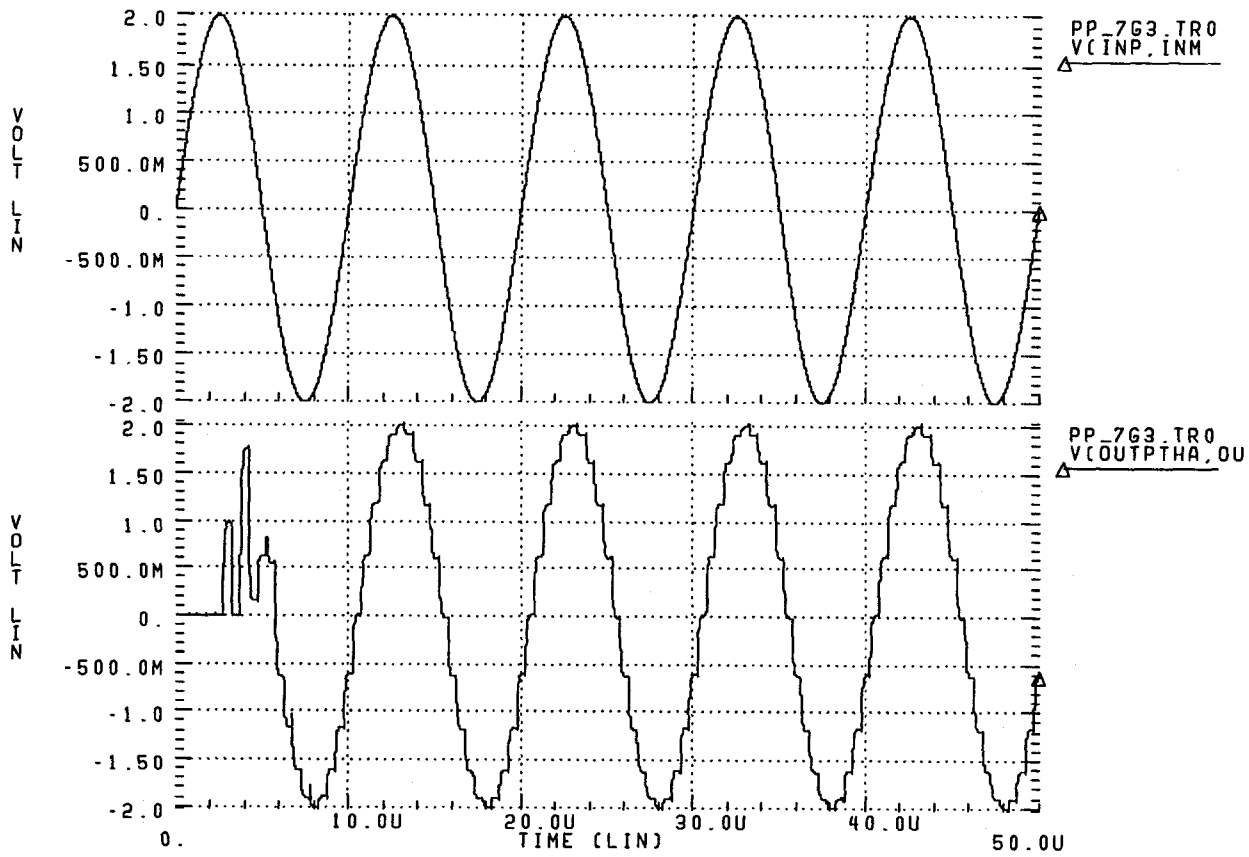

Figure 3.15: Differential input and output signals

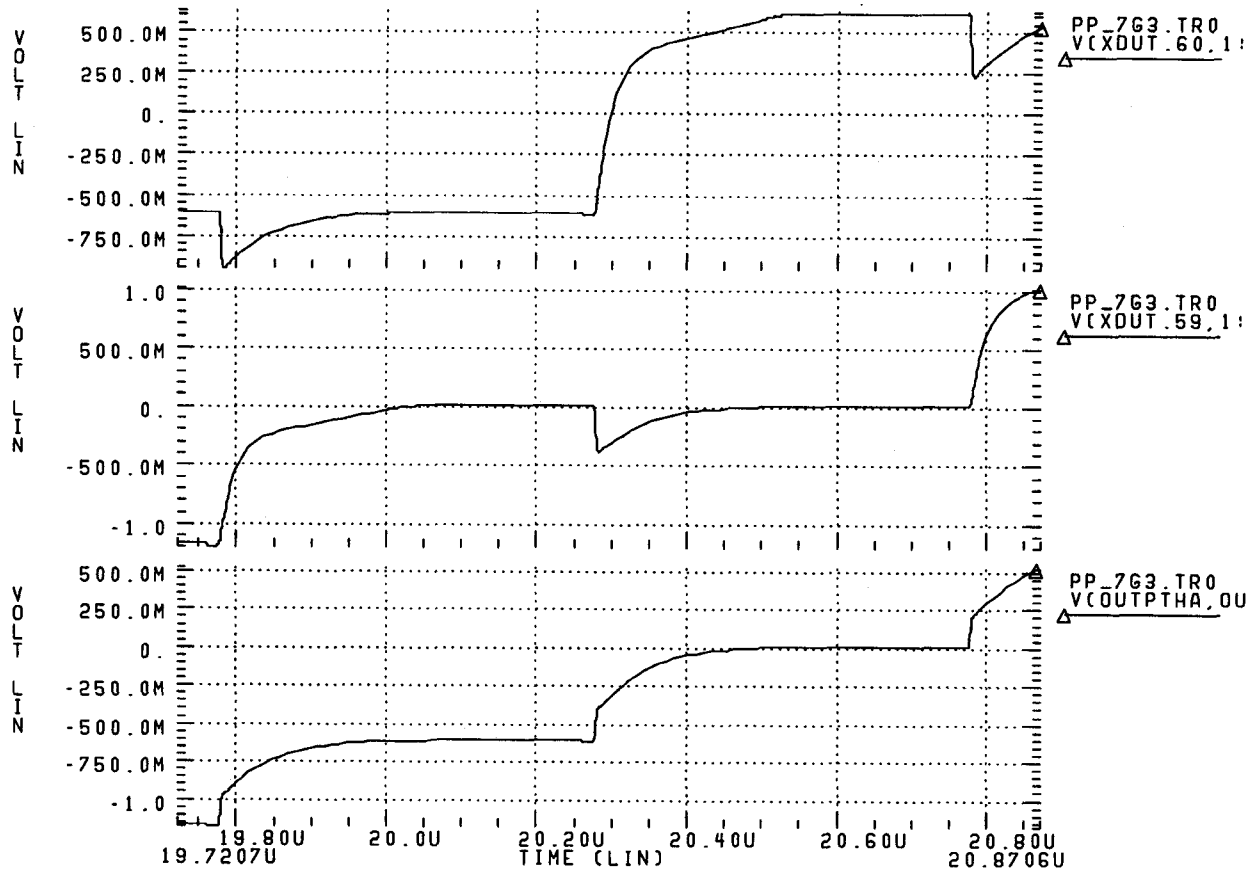

Figure 3.16: The T/H outputs and the S/H output

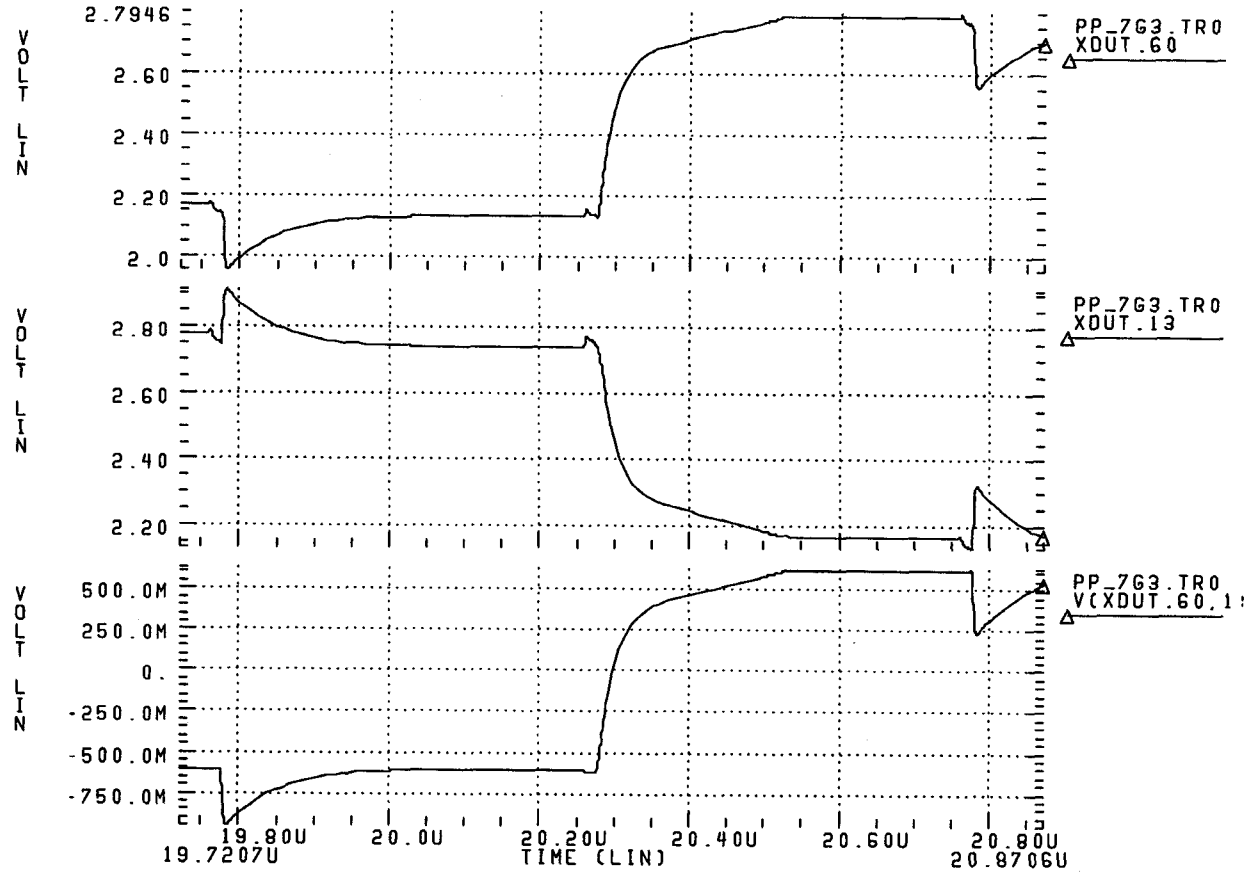

Figure 3.17: Positive, negative and differential output of the T/H circuit

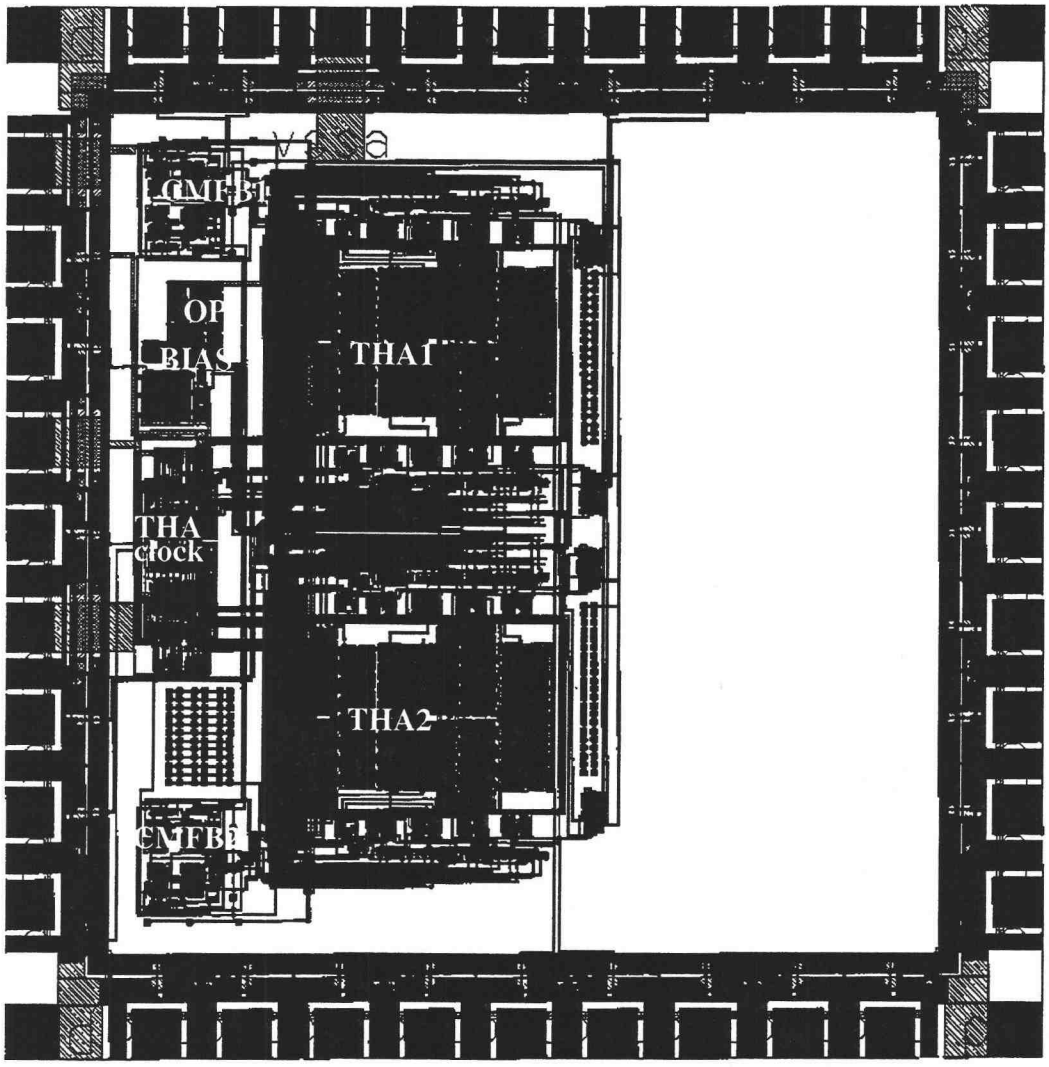

Figure 3.18: The layout of the circuit

Chapter 4. Nonideal Component Effects

4.1 Non-zero "on"-resistance

The instant value of the clock signal on the gate of the MOSFET is usually the power supply voltage, like Vdd or Vss. Therefore for the switch shown in Fig. 4.1.1, $|v_{GS} - v_T| > |v_{DS}|$ is usually satisfied and the MOSFET is in the non-saturated region and therefore behaves as a linear resistor value of $R_{on} = \frac{1}{2k(v_{GS} - V_T)}$.

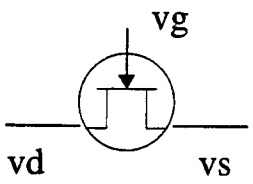

Figure 4.1.1: MOSFETswitch

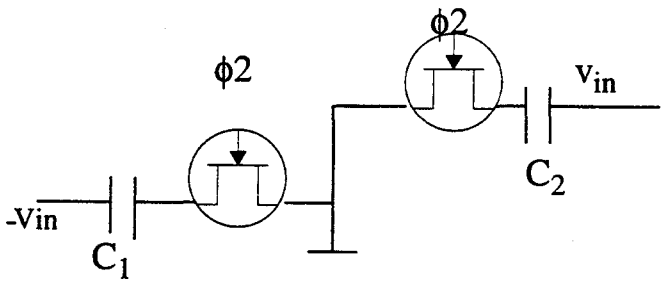

Figure 4.1.2: Holding phase

In the holding phase in Fig. 4.1.2 taken from Fig. 3.7(c), C_1 and C_2 are continously charged to $-v_{in}$ or v_{in}. In order for the capacitor to reach the final value of v_{in} accurately enough before the next tracking phase starts, we need to find the requirement on the value of R_{on}. Note that in the holding phase, the jump of the input is only a step of the sine wave (not from 0 to a new value), thus for oversampled signals, the change of V_{gs} is small, thus we can use an average R_{on} to represent the charging process. At the

end of the holding phase, usually the change of voltage across C_1 or C_2 shall be within 0.1% the desired value, that gives $T/2 > 7T_{on} = 7R_{on}C$, so $R_{on} < T/(14C)$. After substituting the parameter values of post-layout simulation, we find they satisfy the relation. Notice that R_{on} is both process and temperature-dependent, therefore we need to design for the worst case variation.

4.2 Nonideal opamp effects

The MOS operational amplifier is the most important and complicated part of the switched-capacitor circuits. Because of the finite gain, high-frequency rolloff, output resistance, leakage current, nonlinear distortion, noise and slew-rate, the opamp can't perform as a ideal voltage controlled voltage source. In the following, these nonideal effects will be discussed [7-9].

4.2.1 The effect of finite opamp gain

For a voltage-controlled voltage source, the inverting input of the opamp is a true virtual ground. But for an actually opamp, it's not. In Fig. 4.2.1 , just when the circuit is

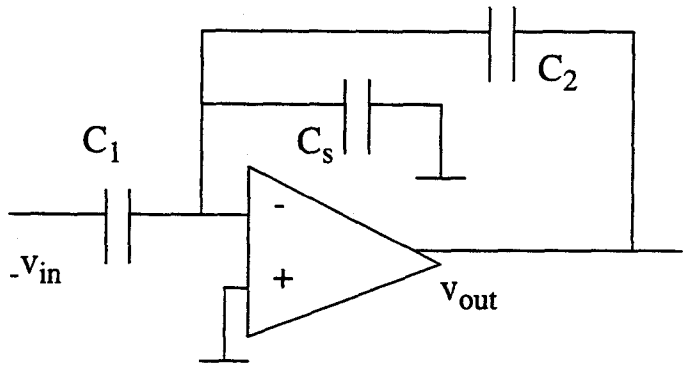

Figure 4.2.1: Tracking of the circuit.

going from holding back to tracking, the node voltage between the C_1 and C_2 is changed from 0 to virtual ground whose potential is $-\frac{v_{out}(n)}{A_0}$. At the end of tracking which is T/4 later, according to charge conservation,

$$(C_1+C_s+C_2)(v_{out}(nT+T/4)/A_0-0)=$$

$$-C_2((v_{out}(nT+T/4)-v_{out}(nT))+C_1(v_{in}(nT+T/4)-v_{in}(nT))=0 \quad (4.2.1)$$

Let C_{2b} denote $C_2+(C_1+C_2+C_s)/A_0$, then the transfer function is

$$V_{out}(z)/V_{in}(z)=(C_1-C_1z^{-1})/(C_{2b}-C_2z^{-1}) \quad (4.2.2)$$

while the ideal one is $(C_1-C_1z^{-1})/(C_{2b}-C_2z^{-1})$.

So the difference factor is $(1+\alpha-z^{-1})/(1-z^{-1})$ where $\alpha=C_{2b}/C_2-1$. The error in magnitude and phase are both about the order of α. As the opamp gain is usually greater than 1000, α is quite small and this effect is negligible.

4.2.2 The effect of finite opamp bandwidth

For a real opamp, the gain decreases after the first pole. The opamp's ability to maintain the input as a virtual ground is greatly reduced. Let us assume the simple one-pole model for discussion. The analyzed circuit is the single-ended version, which doesn't affect its applicability because we don't discuss the charge injection, common-mode jump etc. in this analysis. And we're also assuming two-phase operation for simplicity.

Refer to Fig. 4-2-1, as the input signal frequency is usually much higher than the frequency of the first pole, the transfer function can be approximated as

$$A_V(s) \approx -\frac{\omega_t}{j\omega} \quad (4.2.3)$$

In the time domain

$$\frac{d}{dt}v_o(t) = -\omega_t v_1(t) \quad (4.2.4)$$

Applying the charge conservation principle in the tracking phase, we have:

$$C_2(v_o(t)-v_1(t))+C_1(-v_{in}(t)-v_1(t))+C_s(-v_1(t))=$$

$$C_2(v_o(nT-T))+C_1(-v_{in}(nT-T))+C_s(-v_1(nT-T)) \quad \text{i.e.}$$

$$C_2(v_o(t)\text{-}v_o((n\text{-}1)T)+C_1(\text{-}v_{in}(t)\text{-}(\text{-}v_{in}((n\text{-}1)T))=$$

$$(C_1+C_2+C_s)(v_1(t)\text{-}v_1((n\text{-}1)T)) \qquad (4.2.5)$$

Here we omit the very small difference of the right plate voltage of C_s from 0 in holding phase. Note here the input is the negative side of the input, differentiate it, substitute (4.2.4) and let

$$v_{in}(t)=A\ sin\ \omega_{in}t \qquad (4.2.6)$$

we have:

$$(C_1+C_2+C_s)dv_1(t)/dt+\omega_tC_2v_1(t)$$

$$=-C_1dv_{in}(t)/dt=-AC_1\omega_{in}cos\omega_{in}t \qquad (4.2.7)$$

$$\text{i.e.}\quad \frac{dv_1}{dt}+\frac{\omega_tC_2}{C_1+C_2+C_s}v_1=-\frac{AC_1\omega_{in}\cos\omega_{in}t}{C_1+C_2+C_s} \qquad (4.2.8)$$

The solution is:

$$v_1(nT-T+t)=(v_1(nT-T)+K\cos\varphi)\exp(-k_0t)-K\cos(\omega_{in}t+\varphi) \qquad (4.2.9)$$

where $K=-(AC_1\omega_{in})/(\sqrt{\omega_{in}^2(C_1+C_2+C_s)^2+\omega_t^2C_2^2})$

$tg\varphi=-\omega_{in}(C_1+C_2+C_s)/(\omega_tC_2),\ -\pi/2<\varphi<0$

$k_0=\omega_tC_2/(C_1+C_2+C_s)$

$k_1=k_0*\ T/2$

So, we get

$$v_1(nT\text{-}T/2)=(v_1(nT\text{-}T)+B)exp(\text{-}k_1)\text{-}Kcos(\omega_{in}T/2+\varphi) \qquad (4.2.10)$$

And $v_o(nT\text{-}T/2)\text{-}v_o(nT\text{-}T)=(1+C_1/C_2+C_s/C_2)(v_1(nT\text{-}T/2)$

$$\text{-}v_1(nT\text{-}T))+(v_{in}(nT\text{-}T/2))\text{-}v_{in}(nT\text{-}T))C_1/C_2 \qquad (4.2.11)$$

In the holding phase, we have:

$$v_o(t)-v_1(t)=v_o(nT-T/2)-v_1(nT-T/2) \tag{4.2.12}$$

differentiating it, we have:

$$dv_o(t)/dt=dv_1(t)/dt, \tag{4.2.13}$$

substitute (4.2.4) into (4.2.9),

$$dv_1(t)/dt=-\omega_t v_1(t) \tag{4.2.14}$$

solving the result in the value of v_1 at $t=nT$ as:

$$v_1(nT)=v_1(nT-T/2)exp(-k_2) \tag{4.2.15}$$

where $k_2=\omega_t T/2$

also substituting this result into (4.2.12) gives:

$$v_o(nT)=v_o(nT-T/2)-v_1(nT-T/2)(1-exp(-k_2)) \tag{4.2.16}$$

Therefore, k_1 and k_2 determine how fast the exponential damping is. As $k_2>k_1$, we only need to have $k_2=\omega_t T/2 \ll 1$. $\omega_t > 5\omega_c$ is a good criterion which satisfies this and won't cause too much noise aliasing into baseband which will be shown in Section 4.3.

4.2.3 The finite opamp slew rate

In a real opamp, it takes time for the opamp to slew to the next holding value. If the slew rate is so slow that the output voltage cannot reach its final value within the time slot, nonlinear distortion will occur. Assuming the input signal is $v(t)=A \sin \omega_{in} t$, the maximum slope possible for the sample-and-hold output is $\left|\frac{dv}{dt}\right|_{max} = \omega_{in} A$ which occurs when the output crosses zero. The maximum step is then,

$$\Delta v_{max} \approx \left|\frac{dv}{dt}\right|_{max} \frac{T}{2} = \frac{\omega_{in} A}{2f}$$

If we assign, say x=15% of the T/2 to slewing. then we have

$$S_r \geq \frac{\Delta v_{max}}{t_{slew}} = \frac{\omega_{in} A}{2fx(T/2)} = \frac{\omega_{in} A}{x}$$

Substituting the parameters we have about the opamp, this condition is found to be satisfied.

4.2.4 The effect of finite output resistance

The op-amp, which ideally is a voltage-controlled voltage source, has in fact a non-zero output resistance R_0. This may be of the order of only a few kΩ, if a buffer output stage is used, but it can be much larger (of the order of several MΩ) if there is no buffer stage in the opamp as in a folded-cascode opamp. The effect of R_0 is illustrated in Fig. 4.2.2 during the tracking phase, when the opamp is discharging C_1 and recharging C_2 , C_s and C_L

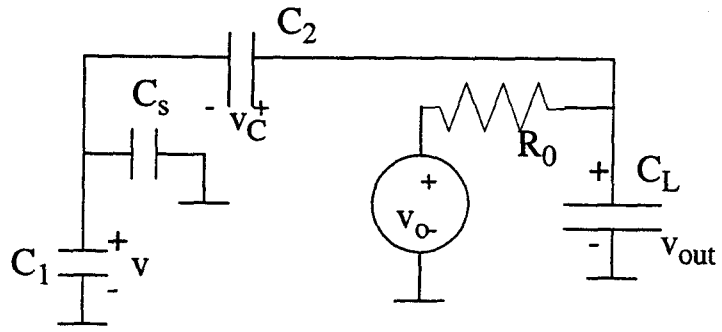

Figure 4.2.2: The effects of R_{out} on the circuit.

Here, the transfer function of the opamp is assumed to be: $v_o(\omega)/v(\omega)=\omega_0/(j\omega)$

i.e. $dv_o/dt=-\omega_0 v$ (4.2.17)

It was also assumed that the on-resistance of the switches is low, so that the initial redistribution of charges between C_1, C_2 and C_L when the ϕ_2 goes high is negligible. We then analyze the subsequent transience caused by the non-zero op-amp output resistance. According to KVL,

$$v_{out}=v_o-iR_0 \tag{4.2.18}$$

and the KCL and branch relations give:

$$i = C_L\frac{dv_{out}}{dt} + C_1\frac{dv}{dt} \tag{4.2.19}$$

Also, if the initial value of $v(t)$ and $v_c(t)$ are v^0 and v_c^0, respectively, then by charge conservation at node A (note that $v_i=-v_{in}$ in this case) ,

$$C_s(v-v^0)+C_1((v-v_{in})-(v^0-v_{in}^0))=C_2v_c-C_2v_c^0=C_2v_{out}-C_2v-C_2v_c^0 \tag{4.2.20}$$

i.e

$$v=C_2(v_{out}-v^0)/(C_1+C_2+C_s)+(C_1v_{in}-C_1v_{in}^0+C_sv^0)/(C_1+C_2+C_s) \tag{4.2.21}$$

Assuming $v_{in}=Asin\omega_{in}t$, and differentiating it, we have:

$$dv/dt=C_2/(C_1+C_2+C_s)dv_{out}/dt+A\omega_{in}\cos\omega_{in}t*C_1/(C_1+C_2+C_S) \tag{4.2.22}$$

Substitute (4.2.22) into (4.2.18) and (4.2.19), we have:

$$v_{out} = v_0 - R_0T_0\frac{dv_{out}}{dt} - \frac{R_0C_1^2A\omega_{in}\cos\omega_{in}t}{C_1+C_2+C_s} \tag{4.2.23}$$

where $T_0=R_0(C_L+C_1C_2/(C_1+C_2+C_s))$. Let $V^0=v_c^0-v^0C_1/C_2$, differentiate it, and with (4.2.17), we have:

$$dv_{out}/dt=\omega_0C_2(v_{out}-v^0)/(C_1+C_2+C_s)+C_1(v_{in}-v_{in}^0+C_sV^0)/$$

$$(C_1+C_2+C_s)-R_0(C_L+C_1C_2/(C_1+C_2+C_s))d^2v_{out}/dt^2+kv_{in}(t) \tag{4.2.24}$$

where $k=R_0C_1^2A\omega_{in}^2/(C_1+C_2+C_S)$

This second-order differential equation has a damped sine-wave function as its solution. The time constant T_1 of the exponential damping is, for usual values, determined almost completely by the time associated with R_0 whose value is the reverse of the real part of frequency eigenvalue of the equation,

$$\lambda_f = \frac{1 + j\sqrt{\left(4T_0\frac{\omega_0 C_2}{C_1 + C_2 + C_s} - 1\right)}}{2T_0} \qquad (4.2.25)$$

The real part is $1/(2T_0)$, so we have $T_s=2T_0$. Therefore, for 0.1% accuracy we should have the time for tracking $T/4>7*T_s=7*2R_0(C_L+C_1C_2/(C_1+C_2+C_s))$. After examining, we find the opamp designed can satisfy this condition.

4.3 Noise

In this Section, noise in this system will be discussed. Here, the single-ended version will be analyzed whose results can be easily applied to the differential version.

4.3.1 Thermal Noise

There are two important mechanisms for noise generation in an MOS transistor. One is the thermal noise, with an approximately constant power spectral density (PSD) .

In a real resistor R, the electrons are in random thermal motion. As a result, a fluctuating voltage appears across the resistor even in the absence of a current from an external circuit. Thus, the Thevenin model of the noisy resistor is shown in Fig. 4.3.1a. Clearly, the higher the absolute temperature T of the resistor, the larger v_{nT} will be. Actually, it can be shown that the mean square of v_{nT} is given by

$$\overline{v_{nT}^2} = 4kTR\Delta f = 4\theta R\Delta f \qquad (4.3.1)$$

Here, k is the Boltzmann's constant, and Δf is the bandwidth in which the noise is measured, in Hz (The value of 4θ at room temperature is 1.66×10^{-20}VC). θ is used to avoid confusion between the same symbol denoting temperature and clock period. The

average value (dc component) of the thermal noise is zero. Since its spectral density S(f) is independent of the frequency, at least for low frequencies, it is a "white noise". Clearly Fig. 4.3.1a can be redrawn in the form of a Norton equivalent, that is as a (noiseless) resistor in parallel with a noise current source i_{nT} (Fig. 4.3.1b), The value of the latter is given by: $\overline{i_{nT}^2} = 4kTG\Delta f$

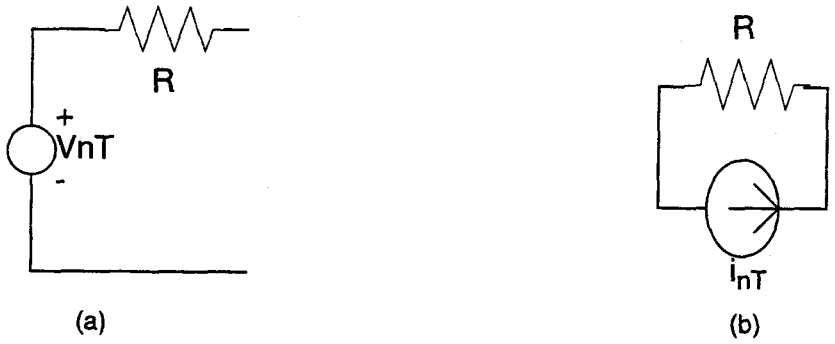

Figure 4.3.1: Thermal noise in a resistor (a) Thevenin equivalent (b) Norton equivalent

Since the channel of a MOSFET in condition contains free carriers, it's subject to thermal noise. Therefore, Eqs.(4-3-1) and (4-3-2) will hold with R given by the incremental channel resistance. The noise can then be modelled by a current source, as shown in Fig. 4.3.2a. If the device is in saturation, its channel tapers off, as we know, and the approximation $R=3/(2g_m)$ can be used in (4-3-2) In most circuits, it is convenient to pretend that i_{nT} is caused by a voltage source connected to the gate of an otherwise noiseless MOSFET, this "gate referred" noise voltage is shown in Fig. 4.3.2(b) and given by

$$\overline{v_{nT}^2} \approx \overline{(i_{nT}/g_m)^2} = \frac{8kT}{3g_m}\Delta f$$

As an example, for a transistor with W= 200um, L=10um, C_{ox} =4.34x10-8F/cm^2 which is

operated in saturation at a drain current iD=200 μA, the gate-referred noise voltage at room tempeature is about 9 nV/$\sqrt{Hz}$.

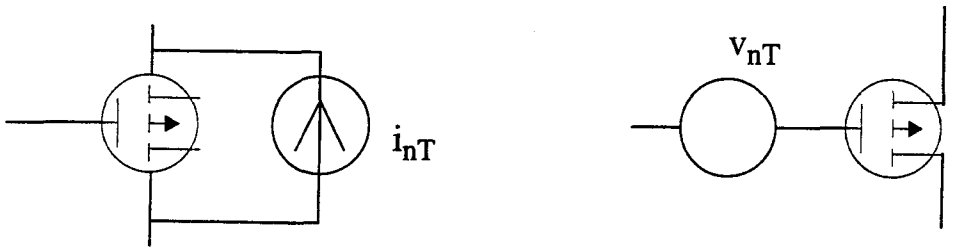

Figure 4.3.2: Equivalent models for the thermal noise in a MOSFET (a)noisy current (b) equivalent nosiy gate voltage

4.3.2 1/f Noise

The other dominant noise is the flicker noise (1/f) noise . In a MOS transistor, extra electron energy states exist at the boundary between the Si and SiO_2. These can trap and release electrons from the channel, and hence introduce noise. Since the process is relatively slow, most of the noise energy will be at low frequencies. The PSD is given by the approximating formula:

$$\overline{v_{nf}^2} = \frac{K}{WLC_{ox}}\frac{\Delta f}{f} \qquad (4.3.2)$$

Here, C_{ox}WL equals the gate-to-channel capacitance in the triode region, and K is a process and temperature-dependent parameter. A typical value is $3x10^{-24}$ V^2F. For the transistor described in the last section, at a low frequency 1 kHz, this formula gives a noise voltage of 83 nV/$\sqrt{Hz}$, which is much bigger than the corresponding thermal noise. But in the holding phase of our track and hold system, when the bulk of noise -- the S/H noise is generated , there is no current flowing through it and the MOSFET capacitor does not contribute any 1/f noise. Thus in the calculation below, we'll omit 1/f noise. The noise in the settling phase is also neglected because in this phase only the small direct noise exists.

4.3.3 Noise calculation

First we discuss the opamp noise.

Consider a noise voltage source with a mean-square value

$$\overline{dv^2} = S(f)df \tag{4.3.3}$$

where S(f) is the spectral noise density. So in a small bandwidth Δf, the root-mean-square value of the noise is given by

$$v = \sqrt{S(f)\Delta f}$$

Thus the noise voltage in bandwidth Δf can be modelled approximately by a voltage source with an rms value v. Network noise calculations for a given circuit then can be obtained by using general circuit theory. The only difference is that when multiple noise sources are applied, as is usually the case in practical circuits, we can represent each noise source by a separate noise generator and calculate the output contribution of each one. The total output noise power in bandwidth Δf is calculated as a mean-square value by adding the individual mean square contribution from each output noise. This requires that all the original noise sources be independent, which is satisfied in this circuit.

Consider this track and hold system and assume it is fed from a low source impedance so that the equivalent input noise voltage determines the noise performance. The opamp input-referred noise spectral density was computed using HSPICE as $S_i(f)=30*10^{-18}\ V^2/Hz$.

The thermal noise spectral density caused by the opamp is the product of the opamp-input referred noise spectral density and the magnitude square of the voltage gain. The total output noise voltage accumulated from zero to half of the sampling frequency is obtained by integrating the spectral density.

Due to the internal sampling and holding performed by the switches and capacitors, the internally generated thermal noise in the switched capacitor circuit will be

replicated in the frequency domain, and for usual parameter values, the thermal noise will get seriously undersampled and hence aliased. As a result, the main part of the PSD is limited to f_c while its magnitude will be multiplied by $2f_{noise}/f_c$, where f_{noise} is determined by the inverse of the time constant associated with the on-resistance of switches or the unit-gain-frequency of the opamp. In this case, the limiting factor is the f_t of the opamp.

If the noise of each MOSFET in the opamp is represented by its equivalent input noise voltage generator, then the equivalent input noise voltage of the opamp can be obtained. It is necessary to get the transfer function *A(f)* from the noninverting input of the opamp to the output of the system. In the holding phase, it can be seen that when positive input of the opamp changes, the output will have the same change, *A(f)*=1

thus $\int_0^{f_2/2} A^2(f)df = f_c/2$, since $\overline{v_{op}^2} = ((2f_0)/f_c)S_d \int_0^{f_c/2} A^2(f)df = f_0 S_d$, so the

result is:

$33*10^6*30*10^{-18}=1*10^{-9}\ V^2$

Second, we consider the switch noise. From the noise model of (4.3.1), the thermal noise for switches in the circuit of Fig. 4.3.3 can be modelled as follows. When the switch is on, the power spectral density is

$$S(f) = \frac{\overline{v^2}}{\Delta f} = S_T(f)\left|\frac{1/(j\omega C)}{R_{on}+1/(j\omega C)}\right|^2$$

The general shape of the S(f) is shown in Fig. 4.3.4 . Now we consider the noise at the holding phase. Due to the effects of sampling and holding, we have:

$$S^{S/H}(f) = \left(\frac{\tau}{T}\right)^2\left(\frac{\sin\pi\tau f}{\pi\tau f}\right)^2\sum_{-\infty}^{\infty}S(f-kf_c)$$

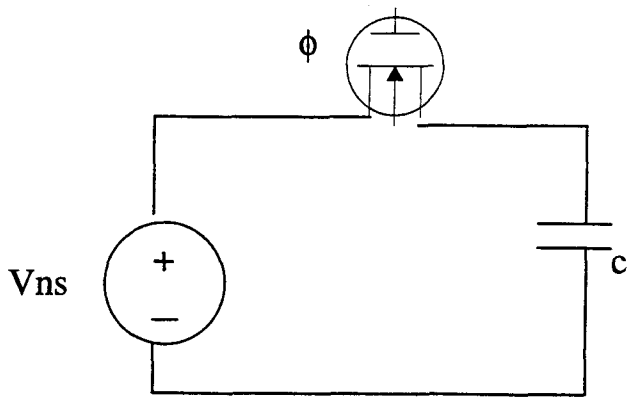

Figure 4.3.3: Switched-capacitor noise

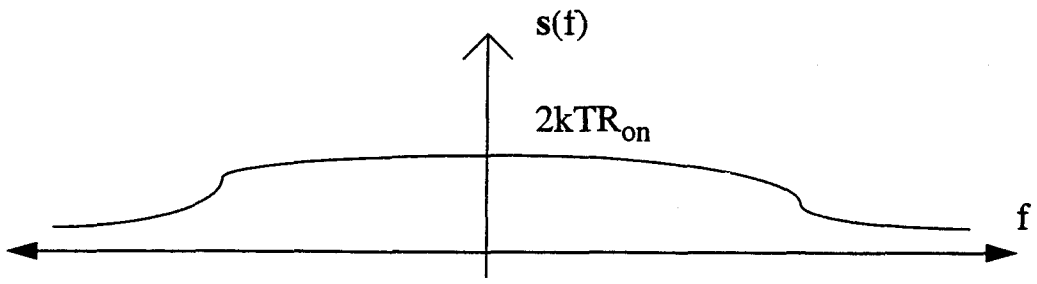

Figure 4.3.4: General shape of direct noise

The original direct noise spectrum can be approximated by the rectangle shown in dashed line in the Fig.4.3.5.

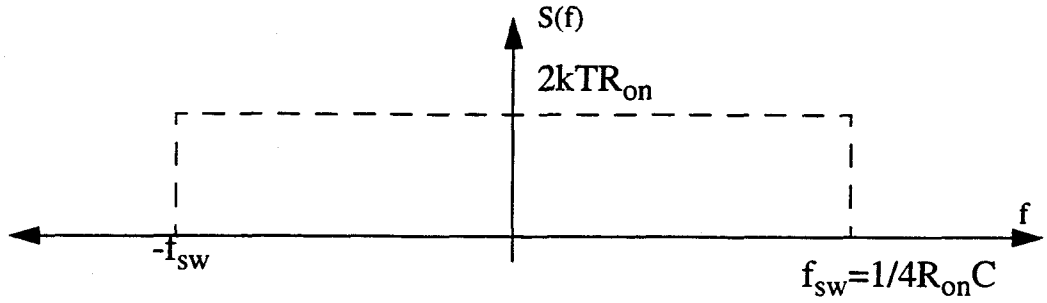

Figure 4.3.5: Approximation of direct noise for calculation of S/H noise, the area below the rectangle is same as the original low-pass function extending to infinity

The bandwidth associated with the idealized box response is thus $f_{sw}=1/4T_{on}$. According to the previous equation on S/H noise, this aliasing will cause the direct noise

spectrum to be shifted by integer multiples of 1/T and the resulting replicas added and then multiplied by the sinc function.

In our circuits, the W/L of the switching MOSFET is required to be big enough for a complete charge transfer. For a 0.1% settling accuracy, the period of time when the switch is on-- mT shall be 7 times as big as T_{on}, the charging time constant of the switch and the capacitor. So $mT > 7T_{on}$,and $f_{sw} = \frac{1}{4T_{on}} \geq \frac{7}{4mT} = 3.5 f_c$.

The power in the baseband is multiplied by $2f_{sw}/f_c$,

$$2f_{sw}/f_c * S(f)=(1/2R_{on}C/f_c)*2\theta R_{on}=\theta/(Cf_c)$$

Thus the total noise power in the baseband due to all the replicas is θ/C Therefore it doesn't help to reduce R_{on} below the value required by the settling-time condition since while this reduces the direct thermal noise PSD $S_d(\omega)$, it increases the aliasing, and the two effects cancel. By contrast, increasing C reduces both the direct and the aliased thermal noise PSDs.

At the beginning of the pre-holding phase (including tracking and settling during which both C_s and C_h is not switched) , both C_s and C_h have an amount of kT/C noise caused by the switches which connect them to analog ground. In the holding phase, C_s is switched and connected to the left plate of C_h and the right plate of C_h is switched to the output. KT/C noise in two phases adds up, the result is

$$v_{sw}^2 = \frac{2\theta}{C_s} + \frac{2\theta}{C_h}$$

With calculation, we get

$v_{sw}^2=2.5*10^{-8}\ V^2$

Because the switch kT/C noise is independent of the opamp noise, we can add their power,

$$v_{total}^2=v_{sw}^2+v_{op}^2=2.6*10^{-8}\ V^2$$

So the estimated total output noise is v_{total}=161 μV, the dynamic range (DR) is around 84.8 dB for single-ended version. For differential one in our case, there's a 3 dB improvement. So the final DR is 87.8 dB. It is better than STHD. Therefore harmonic distortion dominates.

Chapter 5. Summary and Future work.

In this thesis, we discussed:

1. The idea of CDS (correlated double sampling) and its improvement--predictive CDS techniques to reduce the harmonic distortion in T/H circuits. Some considerations on switching, speed and settling were also discussed.

2. The nonlinearity of MOSFET capacitor implemented in accumulation and in the strong inversion region.

3. Consideration on implementing the chip with MOSFET capacitors and direct off-chip load. Post-layout simulation results were also given.

4. The nonideal component effects on the performance of the circuit.

The original contribution of this work is that the predictive CDS techniques and properly biased MOSFET capacitors (replacing high-quality analog poly-poly capacitors which are not available in a basic digital process) are combined to realize a high-accuracy T/H stage.

Based on the discussion, the following future work is recommended:

1. Applying predictive CDS techiques in SC filters, such as the post-filter used in the delta-sigma DACs.

2. Using series or parallel compensated capacitor branches everywhere to reduce further the effects of MOSFET capacitor's nonlinearity .

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