AN ABSTRACT OF THE THESIS OF

Kiseok Yoo for the degree of Master of Science in Electrical and Computer Engineering presented on December 3, 2003.

Title: OP-AMP Free SC Biquad LPF and Delta-Sigma ADC

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Un-Ku Moon

The objective of this work is to explore the feasibility of replacing conventional op-amps with inverters in switched-capacitor (SC) circuits. In order to verify the idea, a low-pass filter (LPF) and a second-order delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) are designed in the 0.5-μm CMOS technology. The low-pass filter structure is based on biquad sections, and the $\Delta\Sigma$ ADC system is based on a low-distortion modulator topology. The feasibility of the proposed idea is demonstrated with system and circuit level.

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OP-AMP Free SC Biquad LPF and Delta-Sigma ADC

by
Kiseok Yoo

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Kiseok Yoo, Author

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TABLE OF CONTENTS

Page

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

OP-AMP FREE SC BIQUAD LPF AND DELTA-SIGMA ADC

1. INTRODUCTION

Switched-capacitor (SC) circuits are very important building blocks in analog mixed signal systems due to their accurate frequency response as well as good linearity and dynamic range. Switched-capacitor circuits can provide highly accurate discrete-time frequency response since filter coefficients are obtained by capacitor ratios. The capacitor ratios can be set accurately and are less susceptible to process variation. Switched-capacitor circuits are also used as gain stages, voltage-controlled oscillators, and data converters [9] among various applications.

An operational amplifier (op-amp) is the most important analog block in switched-capacitor circuits. SC circuits are based on charge-transfer and op-amp provides virtual ground to enable accurate charge-transfer. It can be proved that the accuracy of the charge transfer and hence the performance of SC circuits is limited by the non-idealities in the op-amp like finite op-amp gain, offset etc. To overcome these limitations introduced by the op-amp, some attempts are being made to replace op-amp with relatively simple circuits. One of these approaches is using a unity-gain buffer [6]. There are many advantages of using unity-gain buffers rather than op-amps in switched-capacitor circuits. First, unity-gain buffers can be realized using much simpler circuits than op-amps, therefore circuit design become much easier. Second, since unity-gain buffer circuits are much simpler, they require smaller silicon die area, resulting in a better yield. Third, unity-gain buffers consume less power and hence are suitable for portable application requiring long battery life. An alternative approach is using a simple inverter instead of an op-amp. Inverter offers similar advantage as a unity-gain buffer.

The objective of this work is to explore the feasibility of using inverters in SC circuits. In order to verify the feasibility of using simple inverters in SC circuits, a switched-capacitor biquad LPF and a second-order delta-sigma analog-to-digital converter (ADC) are designed in the 0.5-μm CMOS.

The thesis organization is as follows. In Chapter 2, the switched-capacitor biquad-filter is briefly described and a couple of low pass filter design are presented. Inverter and switch design is presented in Chapter 3. Chapter 4 describes the fundamentals of the delta-sigma modulator. The special features, which are oversampling and noise-shaping, of delta-sigma modulator are revisited. A wide-band low-distortion delta-sigma ADC is introduced and modified to the inverter based delta-sigma ADC in Chapter 5. Also Chapter 5 is devoted to the circuit implementation of the op-amp free second-order delta-sigma modulator. The simulation results are given in Chapter 6. The layout of inverter and ADC is shown in Chapter 7. Finally, Chapter 8 presents conclusion for this thesis.

2. SWITCHED-CAPACITOR BIQUAD FILTER

High performance filters are commonly realized either in continuous-time domain or discrete-time domain depending on the application. Continuous-time filters are realized using passive elements like resistors, capacitors and inductors, and their active counterparts can be derived by using active elements like transconductance stages or op-amps . There are some problems to directly implement continuous-time filters in monolithic form. First, continuous-time filters need large resistors and capacitors. Second, it requires accurate RC time constant. Discrete-time filters are built using switched-capacitor networks in which the required transfer function is realized by appropriately transferring charge among various capacitors. Switched-capacitor filters can present the solution to these problems. Although SC circuits are known since mid 1960s, the monolithic switched-capacitor filters have come into prominence in the late 1970s [3][4]. A switched-capacitor biquad filter is presented in the next section

2.1. Biquad Filter Design

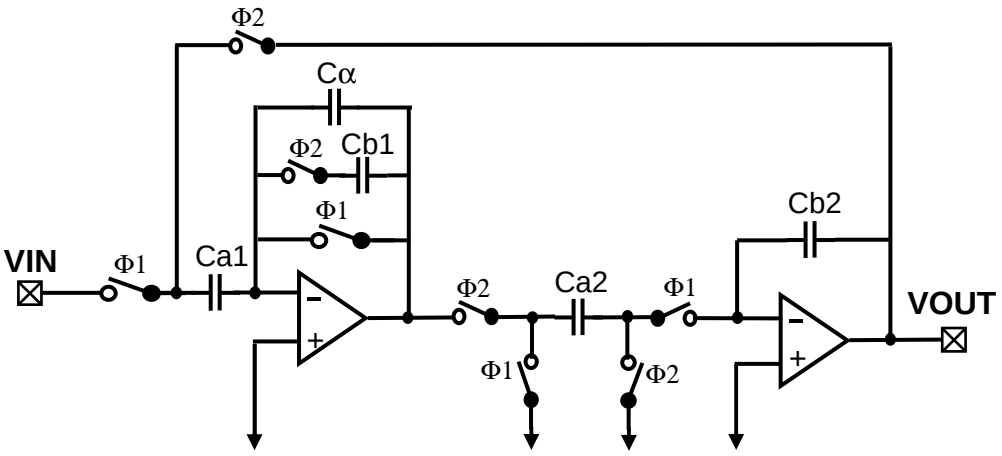


Figure 2.1. The α-damping biquad filter

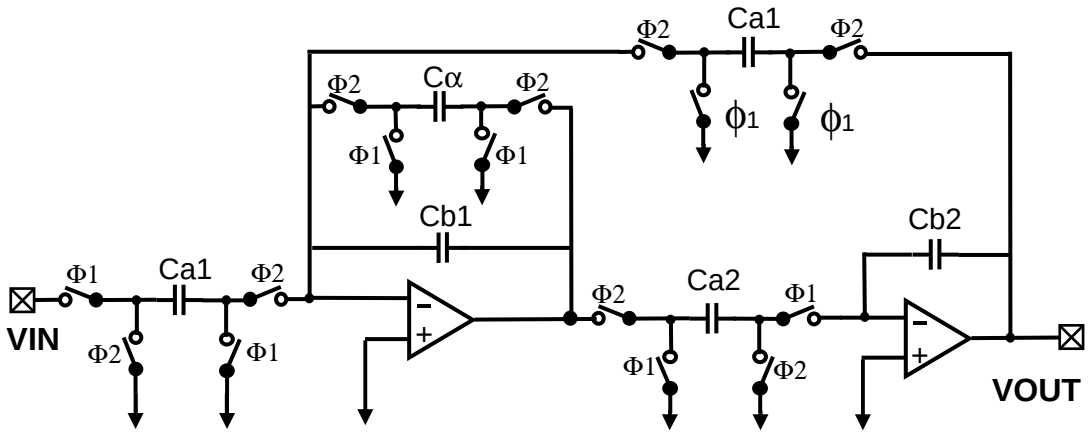
To achieve the higher order switched capacitor filters, lower-order sections are cascaded. Typically, higher-order transfer function $H(z)$ is divided into the product

of second order blocks. If $H(z)$ is an odd order function, one first-order factor is added to this product.

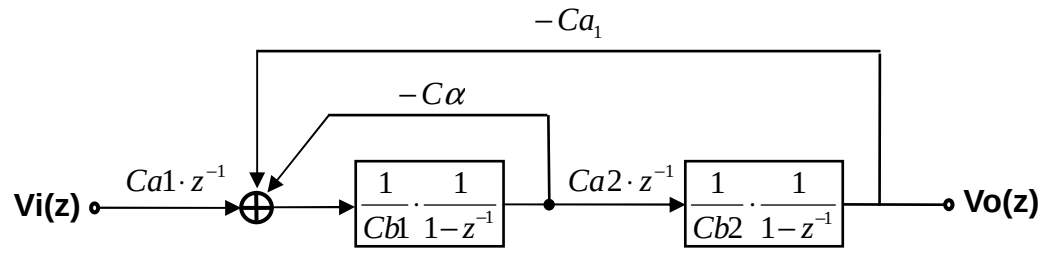
The biquadratic transfer function H(z) is given by

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 a + b_0} \tag{2.1}$$

These second-order sections are often called biquads. In this chapter, two types of biquad LPF topologies are presented. The first type is called α-damping biquad filter is shown in Figure 2.1 and equivalent schematic is presented in Figure 2.2(a). The associated signal-flow diagram is shown in Figure 2.2(b).



(a)



(b)

Figure 2.2. Equivalent schematic of Figure 2.1, and a signal-flow graph

The transfer function of α-damping biquad filter can be calculated by applying Mason's rule on the signal-flow diagram and is given by

$$H(z)=\frac{C_{a1}\cdot C_{a2}\cdot z}{C_{b2}(C_{\alpha}+C_{b1})z^2+(C_{a1}\cdot C_{a2}-C_{b1}\cdot C_{b2}-C_{b2}(C_{\alpha}+C_{b1}))z+C_{b1}\cdot C_{b2}} \qquad (2.2)$$

If we choose $Ca1=Ca2$, $Cb1=Cb2$, then $Ca1=Ca2=\sqrt{b_2+b_1+b_0}$, $Cb1=Cb2=b_o$, and $C\alpha=\frac{b_2-b_0}{\sqrt{b_0}}$.

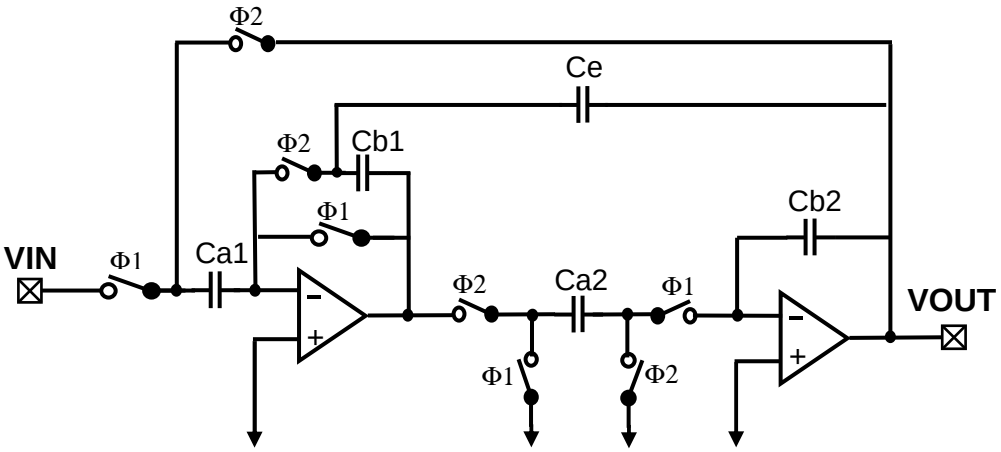
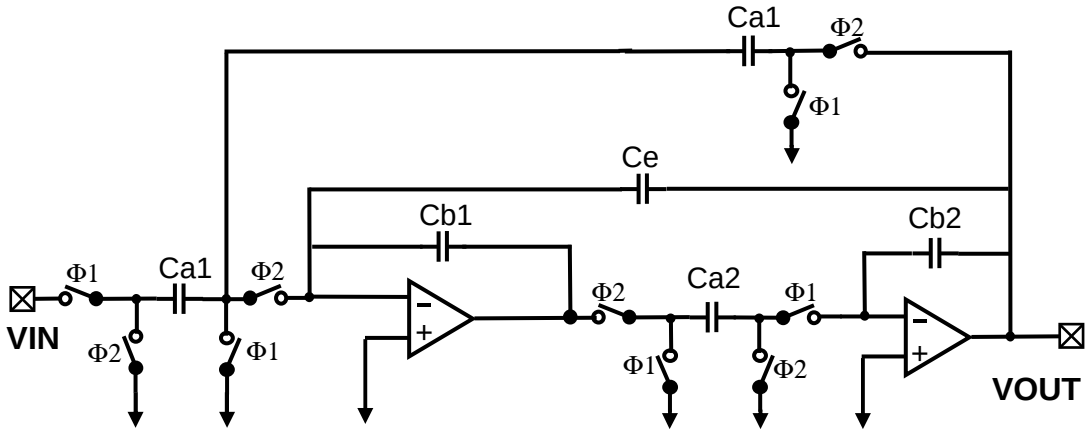


Figure 2.3. The e-damping biquad filter

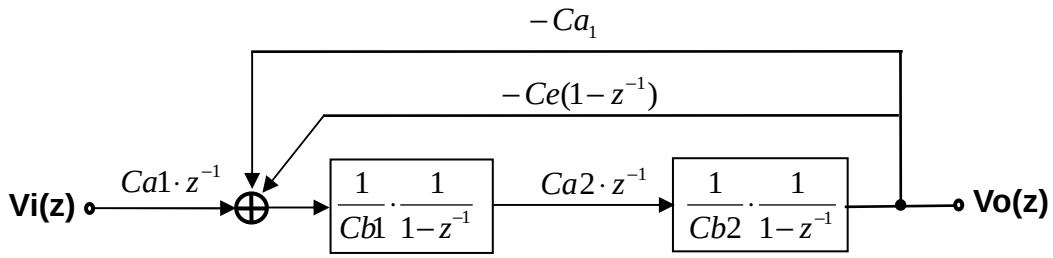
The second type shown in Figure 2.3 and equivalent schematic is presented in Figure 2.4 (a) is called e-damping biquad filter and its signal-flow is presented in Figure 2.4 (b). The transfer function of e-damping biquad filter can be similarly derived as

$$H(z)=\frac{C_{a1}\cdot C_{a2}\cdot z}{C_{b1}\cdot C_{b2}\cdot z^2+(C_{a1}\cdot C_{a2}+C_{a2}\cdot C_e-2C_{b1}\cdot C_{b2})z+C_{b1}\cdot C_{b2}-C_{a2}\cdot C_e} \qquad (2.3)$$

To get capacitor values, same procedure is applied for e-damping biquad filter. If $Ca1=Ca2$, $Cb1=Cb2$, then $Ca1=Ca2=\sqrt{b_2+b_1+b_0}$, $Cb1=Cb2=\sqrt{b_2}$, and $Ce=\frac{b_2-b_0}{\sqrt{b_2+b_1+b_0}}$.



(a)



(b)

Figure 2.4. Equivalent schematic of Figure 2.3, and a signal-flow graph

2.2. Simulation Result

The fourth-order low-pass Bessel filter is used to demonstrate the idea of using inverters instead of op-amps to realize the SC sections in the filter. Two biquad sections are cascaded to realize the fourth order filter. The target 3dB bandwidth of this filter is 20 kHz with an OSR of 128. The capacitor values were calculated by equating the coefficients of theoretical transfer function in Eq. 2.2 with the required transfer function obtained using MATLAB. The switch-cap simulator was used to confirm the correct behavior of α-damping and e-damping topologies. The circuits were implemented with ideal components in switch-cap simulator. MATLAB and switch-cap simulation results are compared and the result is shown in Figure 2.5.

Since the both results are identical, two topologies are confirmed to have required fourth-order Bessel filter characteristics.

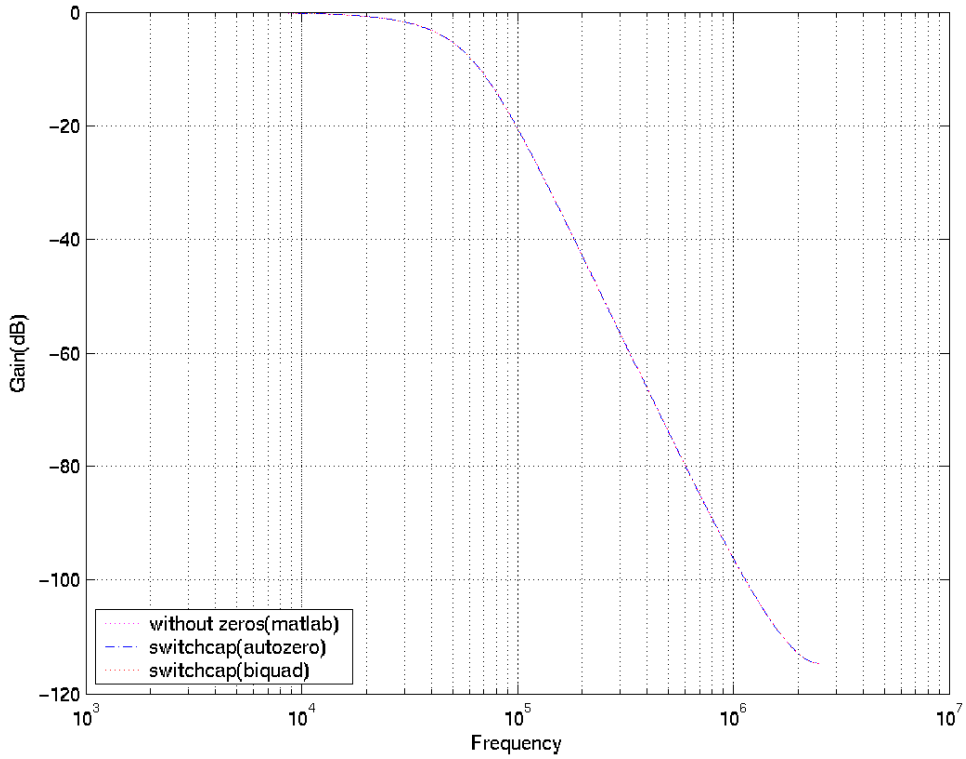


Figure 2.5. MATLAB and switch-cap simulation results

Figure 2.6 illustrates the transient analysis of the α-damping and the e-damping filters with different op-amp bandwidth and gain conditions with a 2.5 V DC input. The number 1 plot is the output of the e-damping filter when op-amp is modeled as 1GHz unity-gain bandwidth (UGB) and 100 dB DC gain. This output is almost same as input level. Transient simulations for various DC gain and bandwidth conditions summarized in Table 2.1 indicate that the output is relatively insensitive to the opamp gain and bandwidth. The output level of α-damping is deviated by 0.058 V from 2.5 V. However, e-damping filter shows better result than α-damping filter with same DC gain. In conclusion, e-damping filter shows better performance than α-damping with

same DC gain and bandwidth op-amps. Since 40 dB DC gain can be relatively easily implemented the e-damping filter is chosen as biquad LPF.

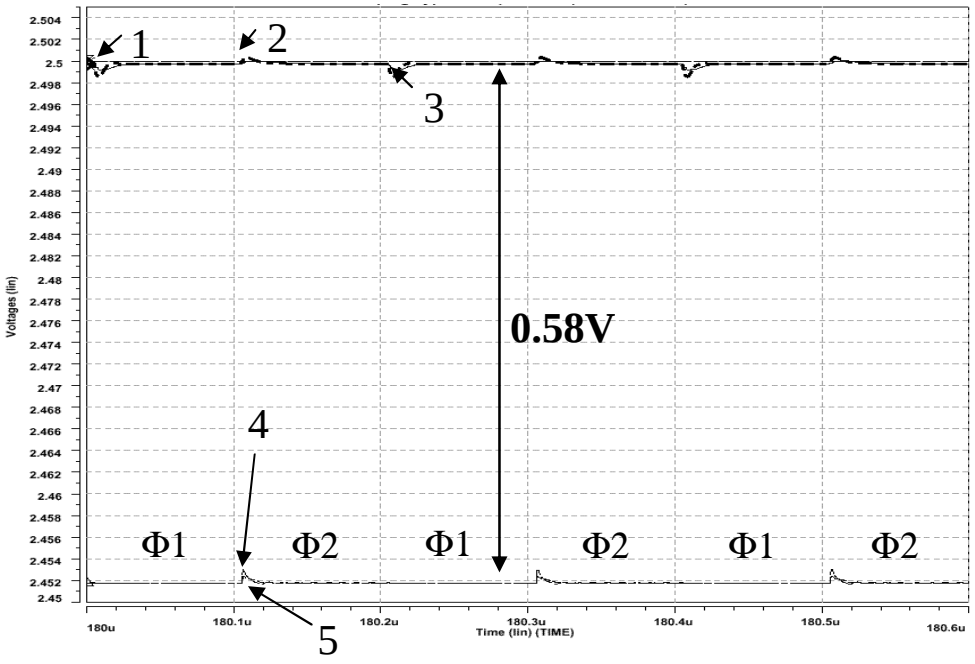


Figure 2.6. Transient Analysis of α-damping and e-damping filters

OPAMP SPEC (using ideal VCCS)			
		UGB(Hz)	GAIN(dB)
1	E-damp	1G	100
2		100M	40
3		40M	40
4	α-damp	100M	40
5		40M	40

Table 2.1. Transient simulation conditions

Figure 2.7 is the transient plot of e-damping filter with some various DC gain and bandwidth conditions as indicated in the figure. While the response of the e-damping filter is less affected by the UGB change, lower op-amp DC gain degrades the filter response considerably. As a result, the op-amp biquad LPF has at least 40 dB DC gain.

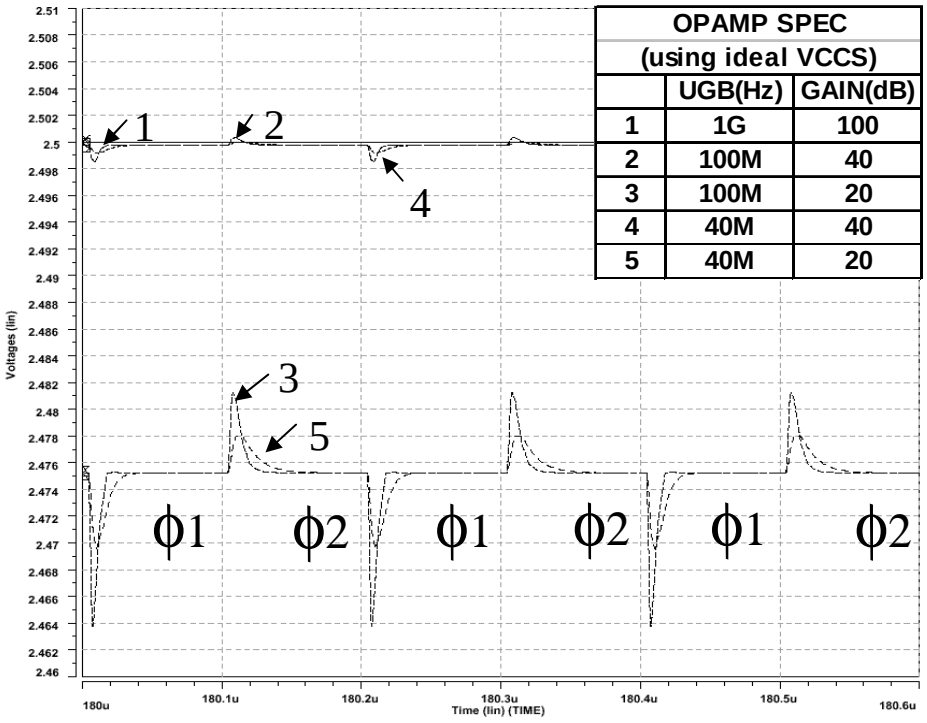


Figure 2.7. Transient Analysis of e-damping filters

2.3. Biquad LPF Based on Inverter

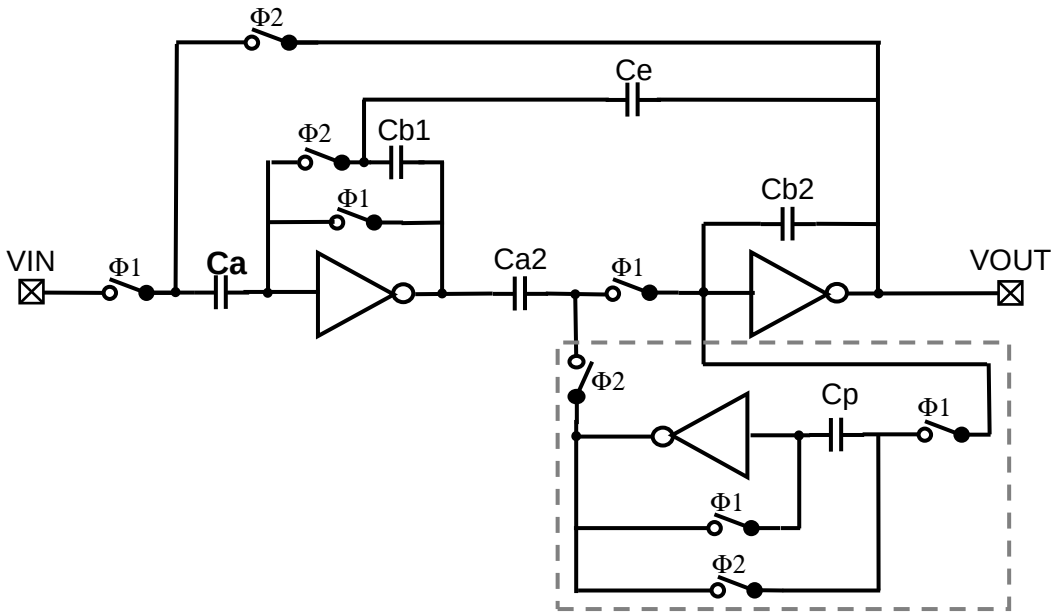


Figure 2.8. The e-damping biquad LPF based on inverters

As shown in Figure 2.8, the e-damping biquad filter in Figure 2.3 is modified to inverters based filter design. The circuits in a dotted rectangle are offset-compensated track and hold circuits [5]. The inverter is reset during each tracking phase. This track and hold circuit provides the reference voltage to sample the charge on Ca2.

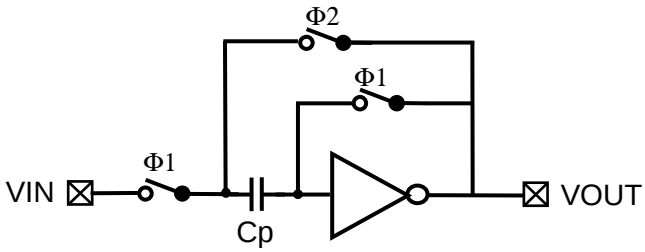


Figure 2.9. Offset-compensated T/H circuit

3. OPAMP FREE SC CIRCUIT DESIGN

This research is mainly focused on finding alternate solutions to substitute the conventional op-amps in SC circuits. In this chapter, the design of an inverter that can potentially replace the op-amp is presented. Switches in SC circuits also play a major role in the overall performance. The design of various switches in the filter are also presented.

Inverter is based on cascoded [10] structure due to its large output impedance and hence higher DC gain. In general, this high gain is obtained with minimal speed penalty. The other advantage is that this can reduce the short channel effects, since cascode structure limits Δ(overdrive voltage) across input drive transistor.

3.1. Inverter Design

Figure 3.1 shows the inverter schematic which will be used in biquad LPF and delta-sigma ADC. M5, M7, M9, M15-M17, and M20 are low threshold voltage (0.4 V) PMOS transistors.

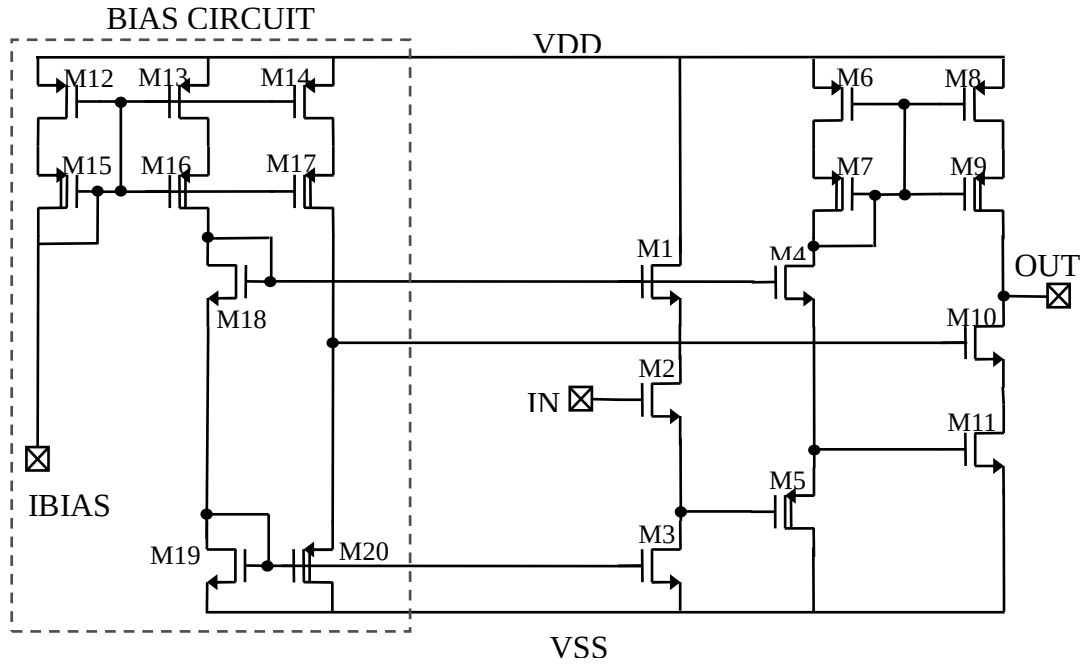


Figure 3.1. Inverter design based on cascode structure

Transistors M8-M11 form the cascoded output stage [8] and M6-M7 self-bias M8 and M9. The low V_T transistors guarantee that M6 and M8 always operate in saturation region. This structure uses simple biasing and can operate to low supply levels. The role of M4 is to increase the gate voltage of M6-M9. M2 operates as source follower to raise input dc level. M1 cascodes input source follower M2 for improved power supply rejection, thus V_{GS} of M1 is less dependent on supply. The bias circuit consists of M12-M20. W/L ratios of all the transistors are shown on Table 3.1.

M1	5/0.8	M8	40/0.8	M15	10/0.8
M2	5/0.8	M9	40/0.8	M16	10/0.8
M3	5/0.8	M10	20/0.8	M17	10/0.8
M4	20/0.8	M11	20/0.8	M18	5/0.8
M5	40/0.8	M12	10/0.8	M19	5/0.8
M6	40/0.8	M13	10/0.8	M20	10/0.8
M7	40/0.8	M14	10/0.8		

Table 3.1. Transistors W/L (μm/μm) ratio of the inverter

3.2. Simulation Results

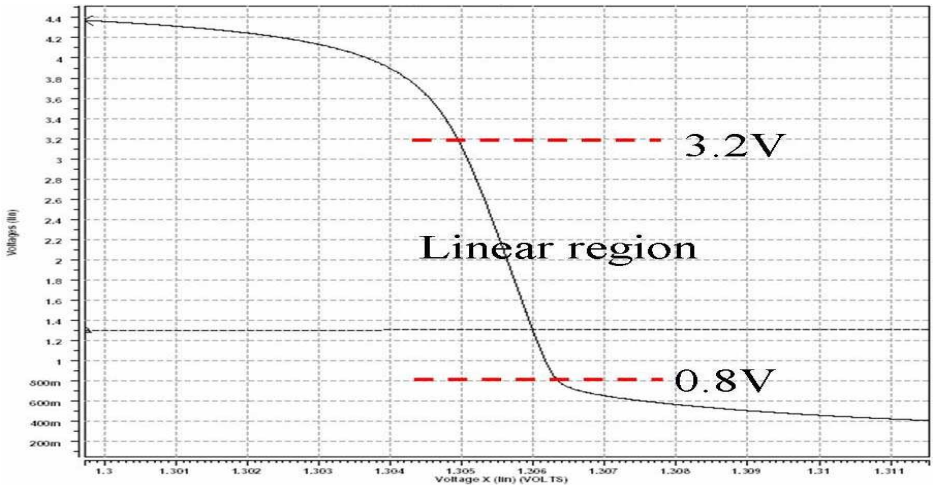


Figure 3.2. DC characteristic of the inverter

The DC transfer characteristic of the inverter is shown in Figure 3.2. The linear range of the inverter is from 0.8V to 3.2V and reset level is about 1.3V.

Figure 3.3 shows the AC characteristics of proposed inverter and the important results are summarized in Table 3.2.

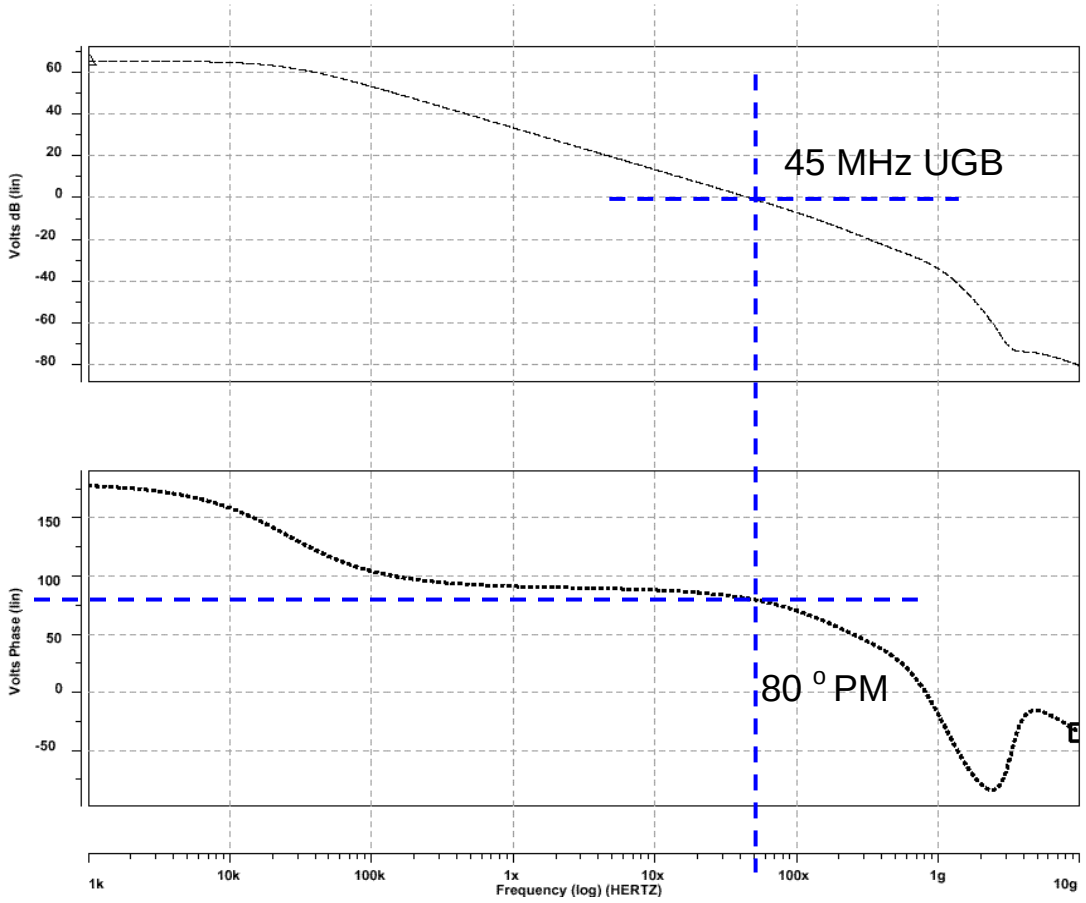


Figure 3.3. AC characteristic of the inverter

DC Gain	65.2 dB
Unity Gain Bandwidth	45 MHz
Phase Margin	80^{o}
Total Current	337.3 µA
Power Consumption	1.7 mW

Table 3.2. Characteristics of the inverter

45 MHz Unity-Gain Bandwidth and 80^o is sufficient for the intended voice application. Figure 3.3 indicates that there are zeros at high frequencies, but transient simulations indicate that these zeros do not degrade the response of the inverter.

3.3. Switch Design

In switched-capacitor circuits, the switch is an important component. Fast switching operation can be achieved by increasing W/L ratio of transistor or reducing sampling capacitor. However, there are several design trade-offs in doing one or the other.

3.3.1. Channel Charge Injection

A simple sampling circuit is shown in Figure 3.3. The channel charge is given by

$$Q_{CH} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \tag{3.1}$$

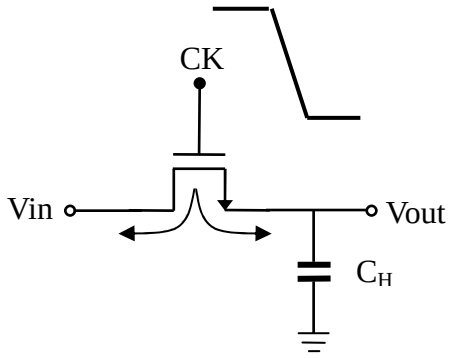


Figure 3.4. Channel charge injection [16]

When the transistor turns off, this charge moves to the source and drain, which is called channel charge injection. The charge moving to the input is absorbed by the input source but the output is affected by the remaining channel charge deposited on to the capacitor. The output voltage deviation due to channel charge is

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \tag{3.2}$$

Assuming the total channel charge moves on to the sampling capacitor, the output voltage is given by

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H} \tag{3.3}$$

and ignoring the phase shift between the input and output, the output is given by

$$V_{out} = V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}(V_{DD} - V_{TH})}{C_H} \tag{3.4}$$

3.3.2. Charge Injection Cancellation

There are various methods to remove the channel charge injection. One of those is using a dummy switch [1][2], as shown in Figure 3.5.

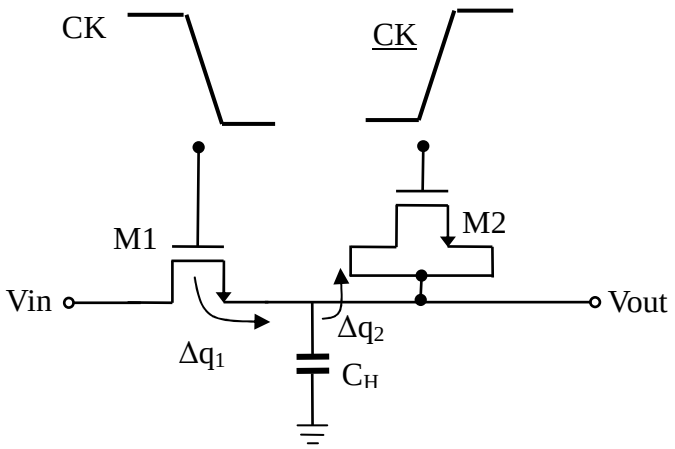


Figure 3.5. Addition of dummy device to reduce charge injection and clock feedthrough [16]

If Δq_1 is equal to half of channel charge of M1, when M1 turns off, this charge is deposited onto the sampling capacitor. However, Δq_2 is absorbed by M2 to create channel half phase later. To remove Δq_1, Δq_1 must be same as Δq_2. M2 is tied

between the drain and source, thus the size of M2 is chosen to be $W_2=0.5W_1$, $L_2=L_1$. Therefore $\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{Th2})$.

Figure 3.6 shows the switch which will be used in op-amp free LPF and delta-sigma modulator. This consists of 4 NMOS transistors, the W/L ratios are all equal to 2/0.5 (μm/μm) and a CMOS inverter is used for providing opposite phase clock to dummy switches.

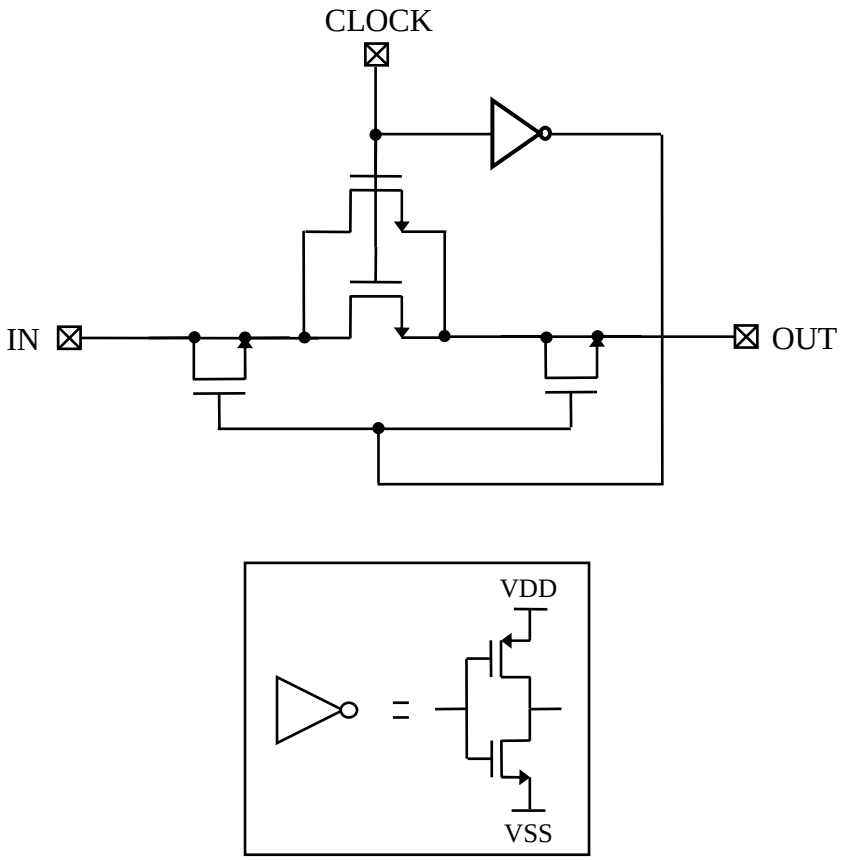


Figure 3.6. Proposed charge injection canceling switch

4. DELTA SIGMA MODULATOR

Oversampling data converters have been widely used for high-resolution medium-to-low-speed applications such as high-quality digital audio. The delta-sigma modulator was proposed in 1962 [11]. Due to two reasons, oversampling delta-sigma modulators have been adopted frequently. First, oversampling converters avoid many of the difficulties of implementing analog circuitry at the expense of more complicated digital circuitry. Second, they require simpler anti-aliasing filters for A/D converters and smoothing filters for D/A converters. Oversampling converters usually use noise shaping which is referred to as delta-sigma ($\Delta\Sigma$) modulator. By applying oversampling and noise shaping, delta-sigma modulator can achieve very high resolution for relatively low-frequency signals. Oversampling delta-sigma data converters have been mainly used for digital audio applications. Recently, as the speed of submicron devices has been increasing, delta-sigma modulators are researched for wider band systems such as wireless RF communications [13]. In this chapter, quantization noise, oversampling and noise shaping will be reviewed.

4.1. Quantization Noise

Quantizers play an important role in delta-sigma ADCs. This chapter describes fundamental theory of quantization to examine the noise in delta-sigma ADCs.

4.1.1. Nyquist-rate Converters

The quantization error is the difference between the input and the output values of a quantizer. Uniform quantization, which is characterized by quantization steps of identical level spacing (Δ) on quantization step, is commonly used. If the input is normalized to ± 1, this quantization step is $\Delta = 1/2^{n-1}$, where n is the number of bits. Figure 4.1 illustrates the input-output characteristics of a 6-level quantizer, with a continuous-amplitude input x and a quantized output y which is represented by the following equation.

$$y = Gx + e\,, \tag{4.1}$$

where G is the slope of the straight line and e is the quantization error. If the input signal *x* is very active, the quantization error *e* can be an uniformly distributed random number in the range ± Δ/2. Under this assumption, its mean square value or quantization noise power is given by

$$e_{rms}^2 = \frac{1}{\Delta} \cdot \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{4.2}$$

The spectral density of *e*, $S_e(f)$, is white and its power is between $-f_s/2$ and $+f_s/2$, where f_s is the sampling frequency. In Nyquist rate converters, f_s is usually two times the signal band f_0.

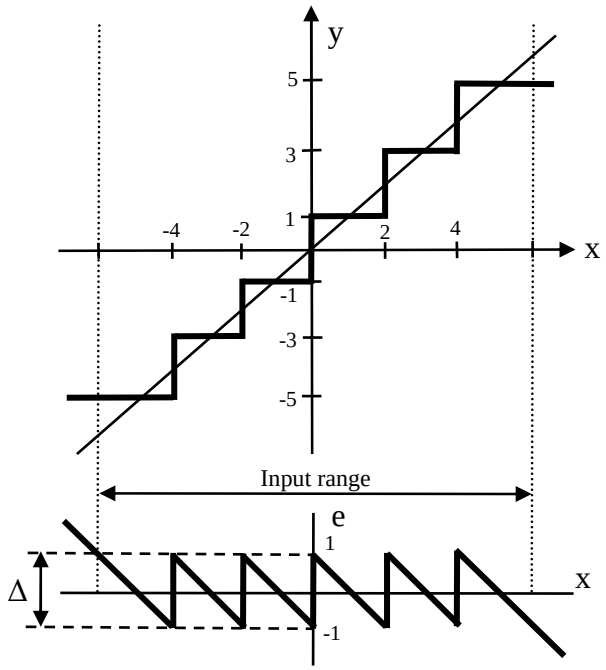


Figure 4.1. Uniform 6-level quantization characteristic

4.1.2. Oversampled Converters

Oversampled converters use a much higher sampling frequency than the Nyquist frequency. The oversampling ratio OSR is,

$$OSR \equiv \frac{f_s}{2 f_0} \tag{4.3}$$

As shown in Eq. (4.2), the quantization noise power is not related to the sampling frequency. Therefore, the quantization noise power in oversampled converters is the same as in Nyquist-rate converters. However, the percentage of this in the interest bandwidth is much smaller than the noise power of Nyquist converters, as shown in Figure 4.2. The in-band quantization noise is inside of shaded area, and is given by

$$P_e = \int_{-f_s/2}^{f_s/2} \frac{\Delta^2}{12} \cdot \frac{1}{f_s} df = \frac{\Delta^2}{12}\left(\frac{1}{OSR}\right) \tag{4.4}$$

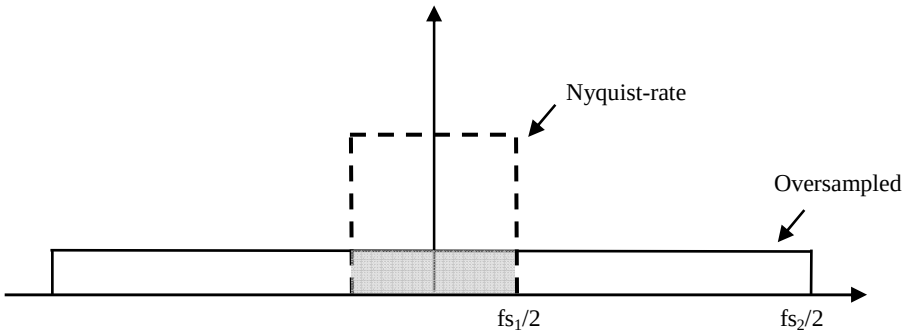


Figure 4.2. Quantization Noise Spectrum in Nyquist-Rate and Oversampled Converters [14]

Thus, doubling of the sampling frequency decreases the in-band quantization noise power by 3 dB (or, equivalently, 0.5 bits) [12].

4.2. Oversampling with Noise Shaping

Figure 4.3 shows the linear model of a general noise-shaped delta-sigma modulator. Analyzing this linearized circuit in the z-domain, the output is

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \tag{4.5}$$

where $S_{TF}(z)$ is a signal transfer function and $N_{TF}(z)$ is a noise transfer function. These transfer functions are given by

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \tag{4.6}$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1-z^{-1} \tag{4.7}$$

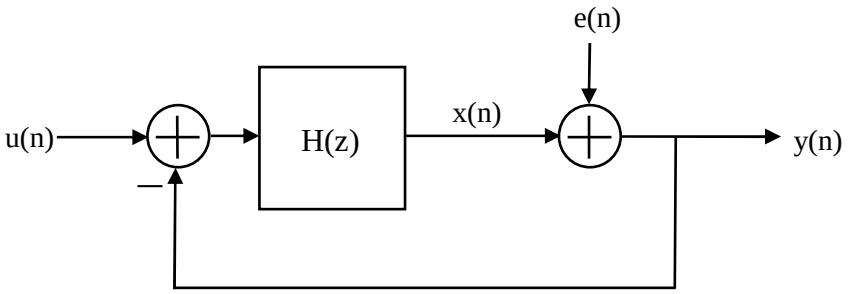


Figure 4.3. Linear model of the modulator showing injected quantization noise.

respectively, if the loop filter transfer function is $H(z) = z^{-1}/(1-z^{-1})$. Therefore, the digital output is a delayed replica of the analog input signal, and the quantization noise is shaped by the filtering function of N_{TF}.

$$\left|N_{TF}(e^{j\omega T})\right| = 2\sin(\omega T/2) \tag{4.8}$$

where $T = 1/f_s$ is the sampling period. For low frequencies ($\omega T \langle\langle 1$), $\left|N_{TF}\right| \approx \omega T$. Since the loop filter H(z) is a low-pass filter function, the dc and low frequency components of the feedback loop are very similar to the input signal u(n). N_{TF} is a high-pass filter function, so it blocks the quantization noise around the signal band at low frequency. However, high frequency noise is not suppressed by the feedback. This out of band noise is removed by additional post filtering.

The second-order noise shaping is briefly reviewed, since second order delta-sigma ADC is adopted in this work.

4.3. Second-Order Noise Shaping

The in-band quantization noise can be suppressed aggressively by using a higher-order loop filter. Two cascaded integrators are needed to implement a second-

order loop filter. The block diagram of a second-order delta-sigma modulator is shown in Figure 4.4.

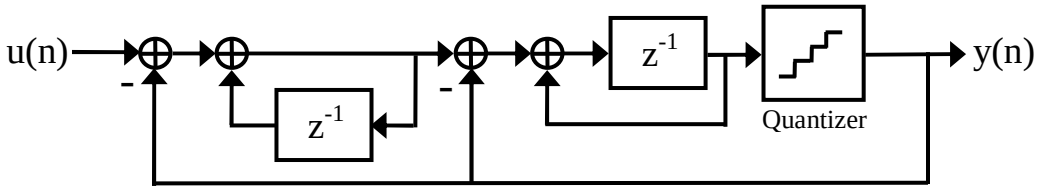


Figure 4.4. Second-order ΔΣ modulator [12]

The signal transfer function and the noise transfer function of this modulator are given by

$$\begin{aligned} S_{TF}(f) &= z^{-1} \\ N_{TF} &= (1-z^{-1})^2 \end{aligned} \tag{4.9}$$

Therefore, the noise-shaping function of a second-order modulator is the square of that given in Eq. (4.8), and the magnitude of the noise transfer function is

$$\left|N_{TF}(e^{j\omega T})\right| = 4\sin^2(\omega T/2) \tag{4.10}$$

The quantization noise power over the frequency band from 0 to f_0 is given by

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\left|N_{TF}(f)\right|^2 df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[4\sin^2\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{4.11}$$

If $f_0 << fs$ (OSR >>1), then sin((πf)/fs) is approximately (πf)/fs, and Eq. (4.11) is equal to

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{2f_0}{f_s}\right)^5 = \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{4.12}$$

If we choose the sinusoidal wave input signal then its maximum peak value without clipping is $2^N(\Delta/2)$. Under this assumption, the signal power of maximum amplitude sinusoidal wave is $P_s \cong \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$. Thus the maximum SNDR for the second-order delta-sigma modulator is

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{5}{\pi^4}(OSR)^5\right) \tag{4.13}$$

or, equivalently,

$$SNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{4.14}$$

Figure 4.5 is the plot of noise-shaping transfer functions. The in-band noise power nearby f_o is decreased as the noise-shaping order increases.

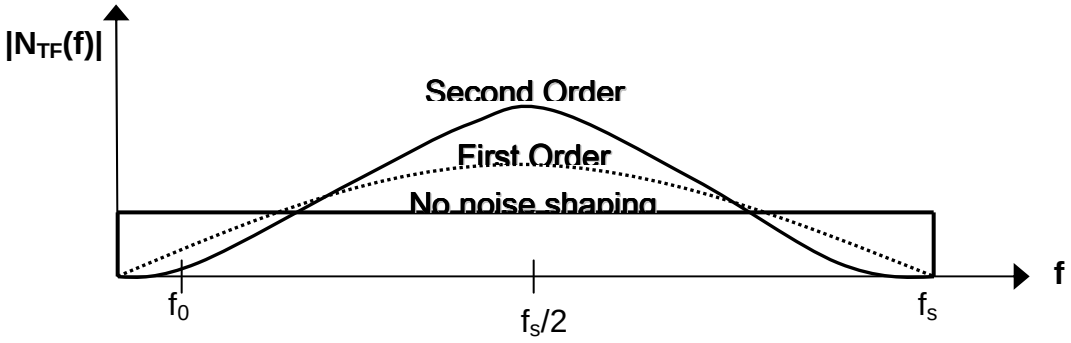


Figure 4.5. Some different noise-shaping transfer functions [12]

5. OP-AMP FREE ΔΣ ADC DESIGN

A second-order delta-sigma ADC based on the wideband low-distortion delta-sigma ADC topology [15] is adopted to implement the inverter-based switched-capacitor circuit.

In this section, the wideband low-distortion delta-sigma ADC topology will be briefly described and modified to suit the inverter-based circuit.

5.1. The Wideband Low-Distortion Delta-Sigma ADC Topology [15]

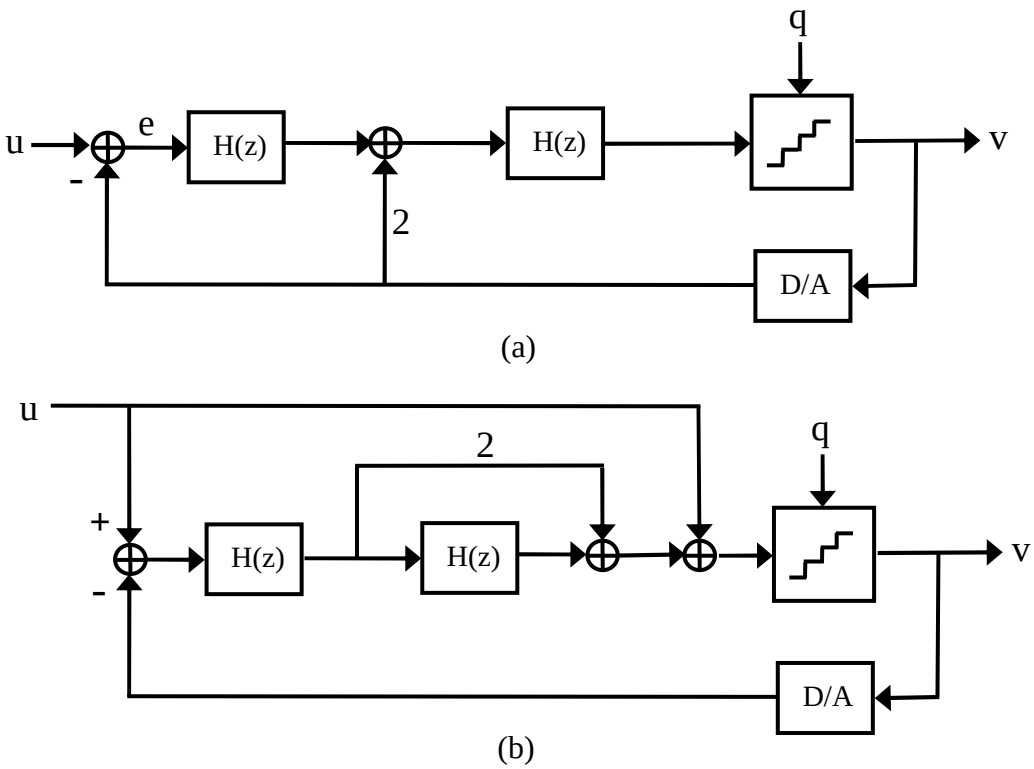


Figure 5.1. (a) Traditional Topology, (b) Reduced distortion topology

The system level schematic of a wideband low-distortion delta-sigma ADC is shown in Figure 5.1(a). In the traditional second order delta-sigma modulator shown in Fig 4.4, the signal transfer function is $S_{TF}(f) = z^{-2}$. The error signal e is the difference between the input and output signals and the ΔΣ loop tries to reduced this

difference in the desired frequency band. The delay term of $S_{TF}(f)$ is subtracted from the input u, thus e contains the portion of the input signal processed through the nonlinearity integrators. The harmonics could be appeared by this nonlinearity op-amp gain and slew-rate effects.

This is achieved by making $S_{TF}(f)=1$ without changing noise transfer function. If $S_{TF}(f)=1$, then e does not contain input portion, therefore no input portion goes through the nonlinearity integrators. Another advantage is that just one DAC is used in this topology, thus reducing chip size and complexity.

5.2. Inverter Based Second Order Delta-Sigma ADC Topology

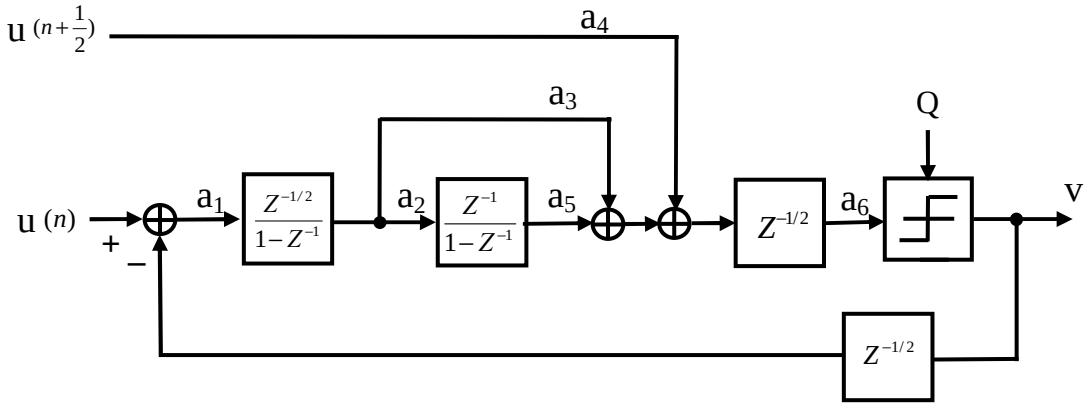


Figure 5.2. Inverter based second order delta-sigma ADC topology

The wideband low-distortion delta-sigma ADC topology is modified to the topology of Figure 5.2. If the input signal is slowly changed, the half cycle difference between u(n) and u(n+1/2) can be very small. Thus u(n) and u(n+1/2) can be assumed equal. Under this assumption, the output signal is

$$v = \frac{a_4 a_6 (z^{-\frac{1}{2}} - 2z^{-\frac{3}{2}} + z^{-\frac{5}{2}}) + a_1 a_3 a_6 (z^{-1} - z^{-2}) + a_1 a_2 a_5 a_6 z^{-2}}{1 - 2z^{-1} + z^{-2} + a_1 a_3 a_6 z^{-\frac{3}{2}} + (a_1 a_2 a_5 a_6 - a_1 a_3 a_6) z^{-\frac{5}{2}}} u + \frac{(1 - z^{-1})^2}{1 - 2z^{-1} + z^{-2} + a_1 a_3 a_6 z^{-\frac{3}{2}} + (a_1 a_2 a_5 a_6 - a_1 a_3 a_6) z^{-\frac{5}{2}}} Q \quad (5.1)$$

The coefficients were obtained using MATLAB (simulink simulator), so as to avoid saturation at the output of each integrator. The gain coefficients are, a_1=1/5, a_2=1/3, a_3=1, a_4=1/10, a_5=3/2, a_6=10. Then Eq. 5.1 is

$$v = \frac{z^{-\frac{1}{2}} + z^{-1} - 2z^{-\frac{3}{2}} - z^{-2} + z^{-\frac{5}{2}}}{1 - 2z^{-1} + 2^{-\frac{3}{2}} + z^{-2} - z^{-\frac{5}{2}}} u + \frac{(1 - z^{-1})^2}{1 - 2z^{-1} + 2^{-\frac{3}{2}} + z^{-2} - z^{-\frac{5}{2}}} Q \quad (5.2)$$

This topology was simulated using MATLAB (simulink) to compare performance with the wideband low-distortion delta-sigma ADC topology. Simulation conditions are given by

Input frequency	1.77 kHz
Input amplitude	0.8
Sampling frequency	5.12 MHz
OSR	128
quantizer	1bit (2 levels)

Table 5.1. Summary of simulation conditions

Figure 5.3 is the FFT output spectrum of the wideband low-distortion delta-sigma ADC. Lower plot of Figure 5.3 is enlarged plot of upper plot to show the low frequency region in detail. As shown in Figure 5.3, the SNDR is 84.6 dB. Figure 5.4 is the FFT result of the inverter-based second-order delta-sigma ADC and SNDR is 85.2 dB. Thus, the performance of modified topology is comparable to previous topology.

However, these SNDRs are a little bit lower than the theoretical value. This results from using 1-bit (2-level) quantizer. Table 5.2 is the SNDR summary of the second-order delta-sigma modulator with different quantizers. The traditional Bose-Wooley structure [7] was simulated.

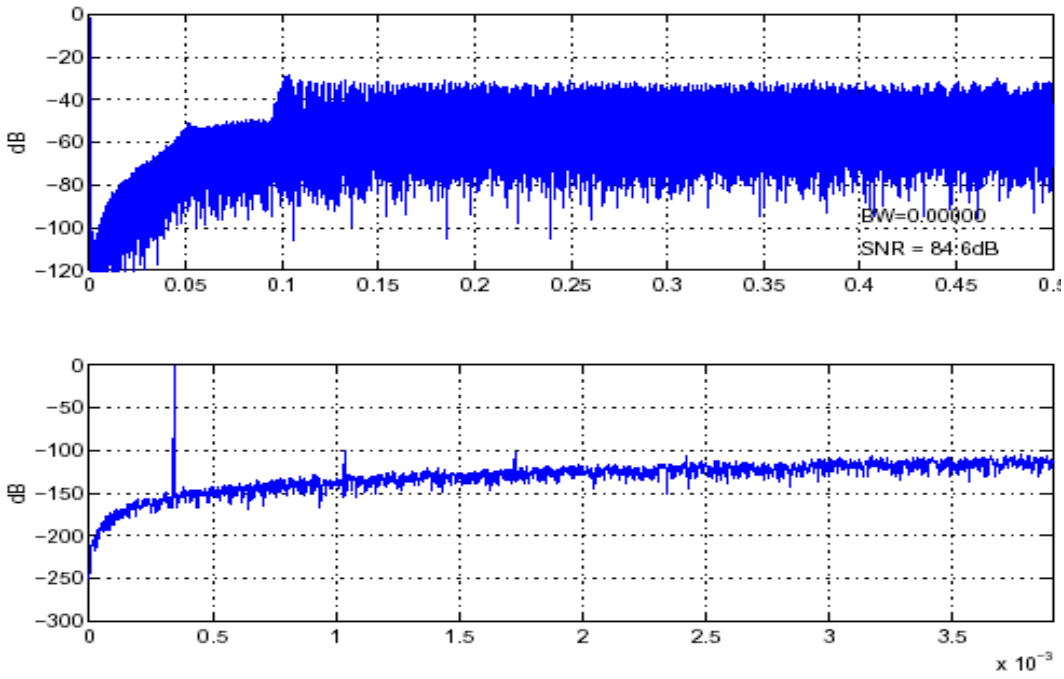


Figure 5.3. Output spectrum of the wideband low-distortion delta-sigma ADC

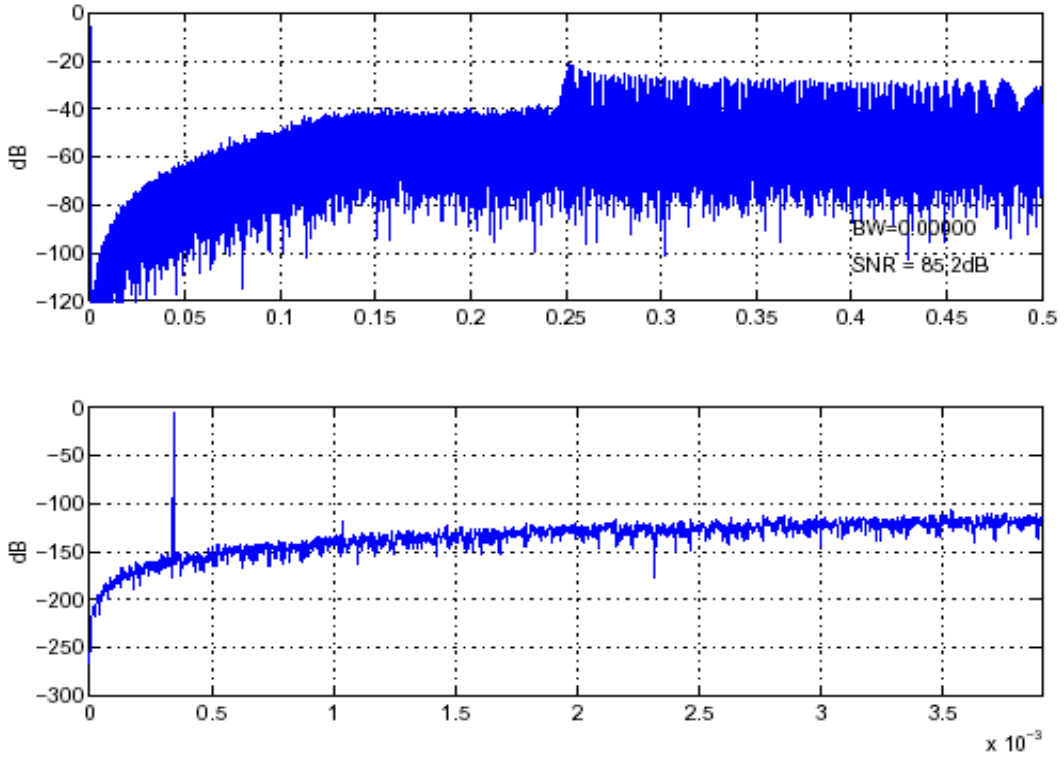


Figure 5.4. Output spectrum of inverter based second order delta-sigma ADC

Level	N	$SNR_{theoretical}$ (dB)	SNR (dB)	Difference (dB)
2	1	98.31	86.3	12.01
3	1.6	101.83	93.8	8.03
4	2	104.33	99.5	4.83
5	2.3	106.26	103.2	3.06
8	3	110.35	109.3	1.05
9	3.2	111.37	110.3	1.07
16	4	116.37	115.9	0.47
17	4.1	116.89	116.3	0.59

Table 5.2. SNDR of traditional second order delta sigma ADC with different quantizer levels (OSR=128)

The higher level quantizer uses, the smaller difference is obtained between theoretical SNDR and simulation SNDR. If the quantizer is over 2 bits (4-level), the difference is below 5 dB. Thus the SNDR result of Figure 5.3 and Figure 5.4 is systematic problem due to 1-bit quantizer and can be improved by increasing the number of quantization levels. However, this work is not focused on improving SNDR in view of systematic method. Consequently, the performance of the wideband low-distortion delta-sigma ADC topology and the modified ADC topology is similar, suggesting that this modified topology can be adopted to implement the inverter based delta-sigma ADC.

5.3. Overall Circuit Level Schematic

5.3.1. 1-bit DAC Schematic

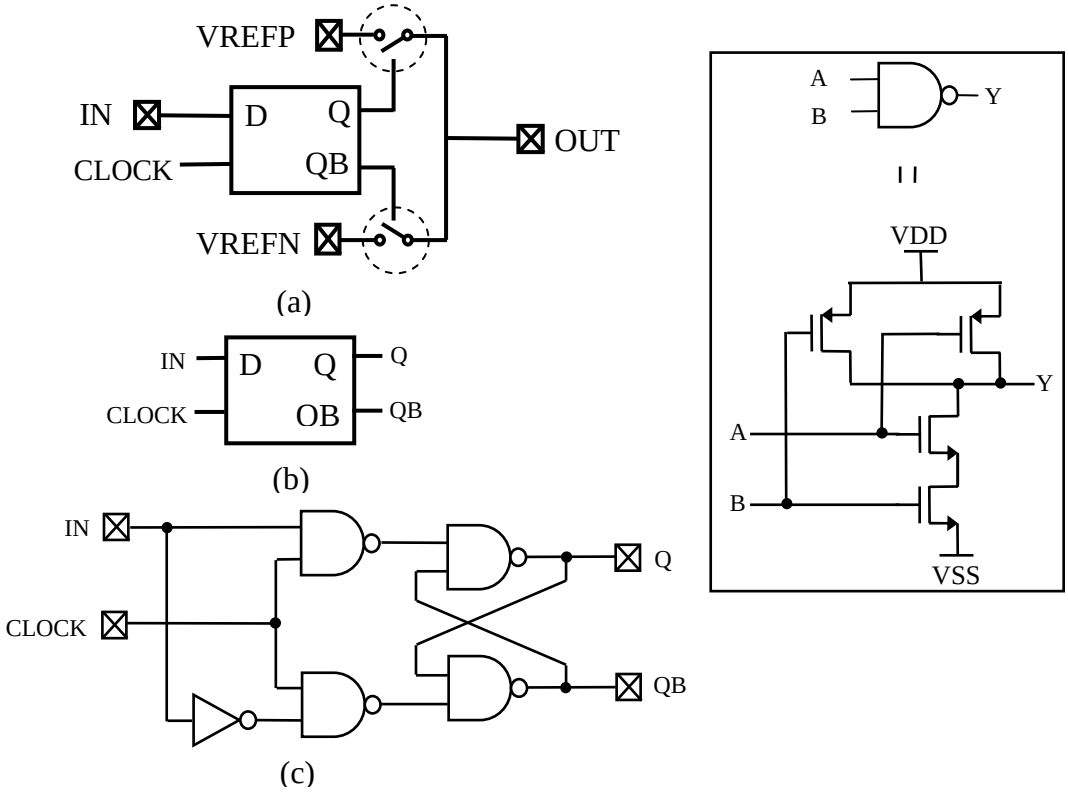


Figure 5.5. 1-bit DAC

Figure 5.5(a) illustrates the schematic of the 1-bit DAC used in the delta-sigma ADC. As shown in Figure 5.5(b)(c), the clocked D-flip flop was adopted in the 1-bit DAC design. There is no delay through the DAC. However, in ADC topology, this 1-bit DAC delays the incoming data for a half-clock cycle, since the DAC operates to determine the output during phase 1 and this output is transferred to the next summing node during phase 2.

5.3.2. Overall Circuit Level Schematic

The overall circuit level schematic of the op-amp free delta-sigma ADC is shown in Figure 5.4. The capacitor value were chosen through the result from the previous Chapter 5.2. The capacitor values are

CA1	0.25 pF
CA2	1.25 pF
CB1	0.25 pF
CB2	0.75 pF
CC1	0.25 pF
CC2	2.5 pF
CC3	3.75 pF
Cp	0.25 pF

Table 5.3. Capacitance value of ADC

The large inverters are cascoded inverters and the small inverters are simple CMOS inverters. The 1-bit quantizer consists of these CMOS inverters. The circled switches are the CMOS switches since switches on the signal path should be realized with transmission gates to avoid malfunction due to the varying nature of the signal. The other switches are the charge canceling switches which are proposed in Chapter 3.2. ‘agnd1’ is 2.5 V since input signal’s reference voltage is 1.3 V and ‘agnd2’ is 1.3 V since reset level of second integrator’s inverter is around 1.3 V. The circuits inside the rectangle operate with the same role described in Chapter 2.2.

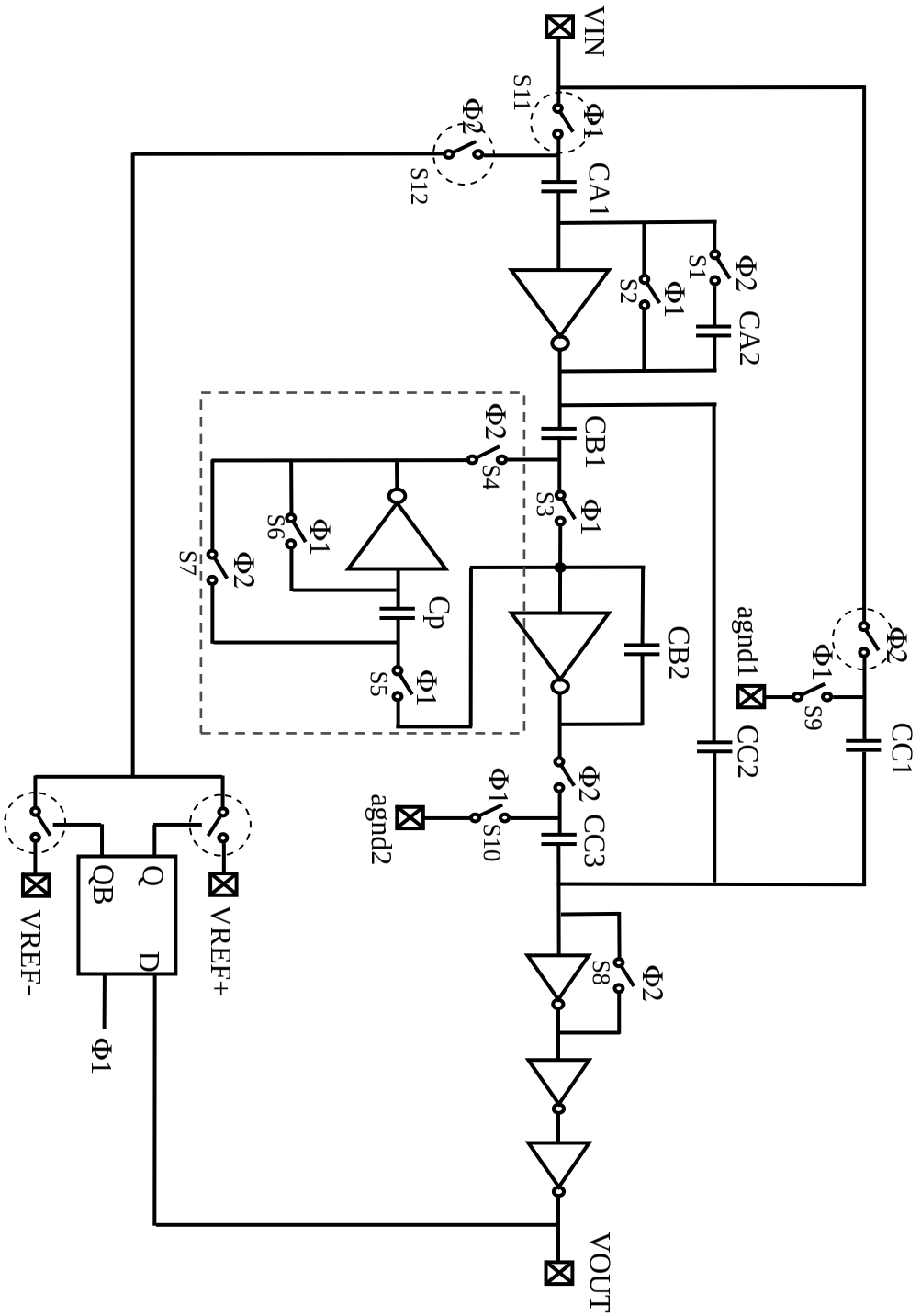


Figure 5.6. Circuit level design of inverter based second order delta-sigma ADC

6. SIMULATION RESULTS

Circuit level simulations were done in HSPICE to verify the op-amp free delta-sigma ADC. The following figures show simulation results. Figure 6.1 shows the FFT plot of the second-order delta-sigma ADC using ideal components. The inverters were modeled with voltage-controlled current sources. The gain of the modeled inverters is 40 dB and the unity-gain bandwidth is 40 MHz. Voltage-controlled resistors were used to model the ideal switches. The input is a 3.05 kHz sine wave with a 4 Vp-p amplitude. A 2.5 V reference voltage and 5 V supply voltage were used. The sampling frequency f_s is 5 MHz and the simulation data segment contained 8192 (2^{13}) samples; this segment was taken after discarding 250 samples to remove transient effects. The oversampling ratio (OSR) is 128.

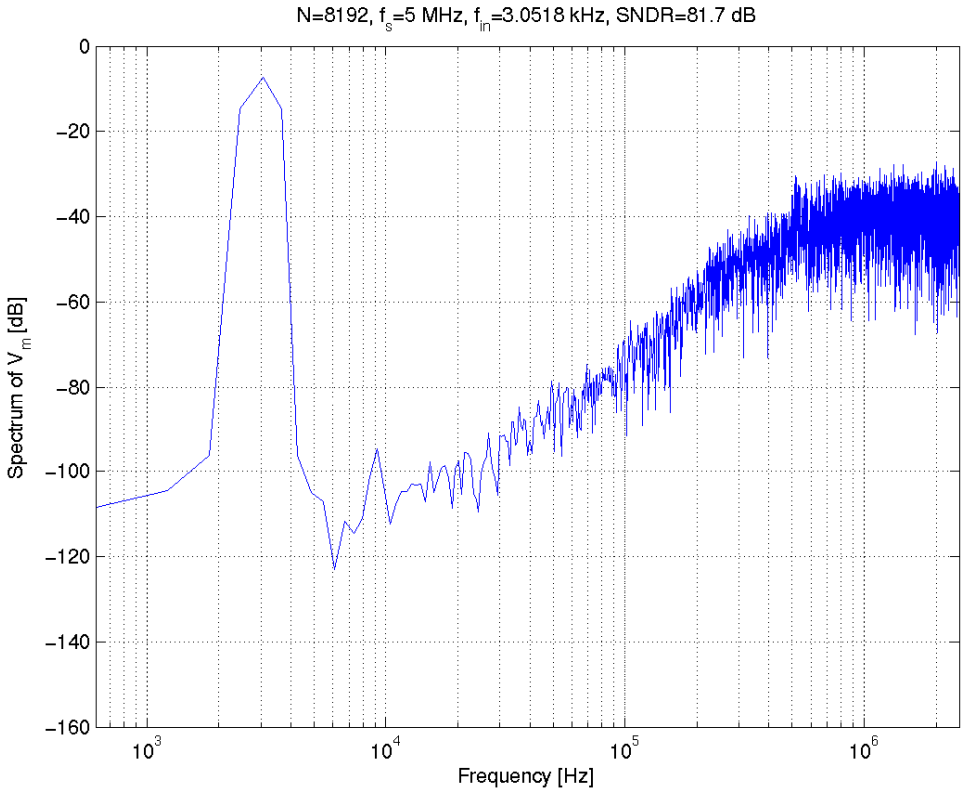


Figure 6.1. FFT plot using ideal components

As shown in Figure 6.1, the SNDR is 81.7 dB. This result is about 5 dB lower than predicted from the system level simulation done in MATLAB. However, the result could be better if the number of samples used in simulation was increased.

Figure 6.2 shows the FFT result. In this simulation, most components are modeled with real transistor-level circuits except for the switches which are ideal. The SNDR is about 81.3 dB. This result is similar to Figure 5.7 and shows the feasibility of inverter based delta-sigma ADC.

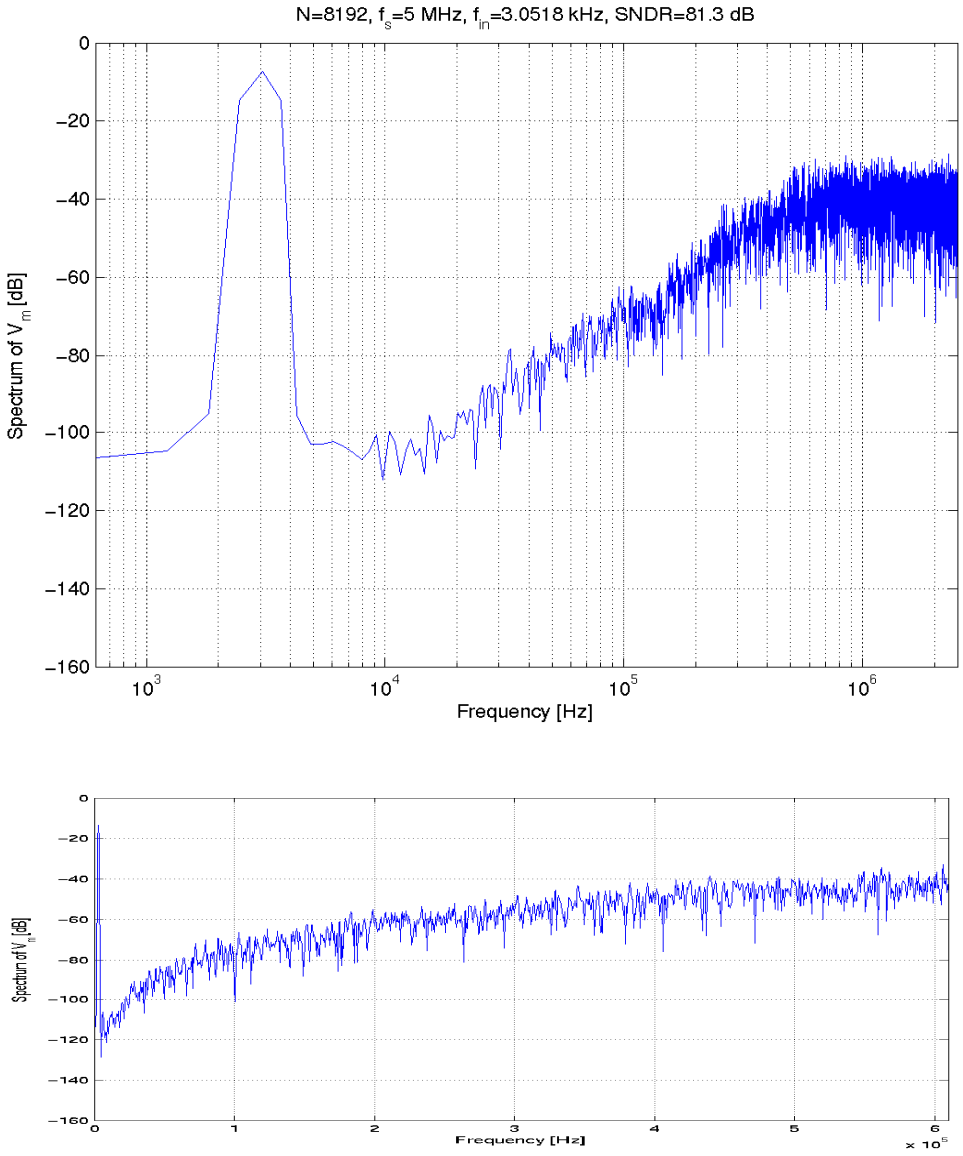


Figure 6.2. FFT result

Figure 6.3 is the FFT result for the case where the ADC uses full transistor-level circuits, including the switches. In this plot, the results from the circuit level simulation show that the SNDR is 40.8 dB. The degradation is due to harmonics. These are caused by the transistor-level switches. For that reason, the switches were checked one by one. Only one switch was replaced at a time by its transistor-level implementation, while keeping others as ideal components. As seen in Table 6.1, most switches degrade SNDR and first integrator's switches were parts that caused major degradation. Thus, a different kind of switches (NMOS, CMOS, etc) and different switch sizes were simulated. However, there was no big difference. Therefore, these distortions are not related to the amount of the channel charge.

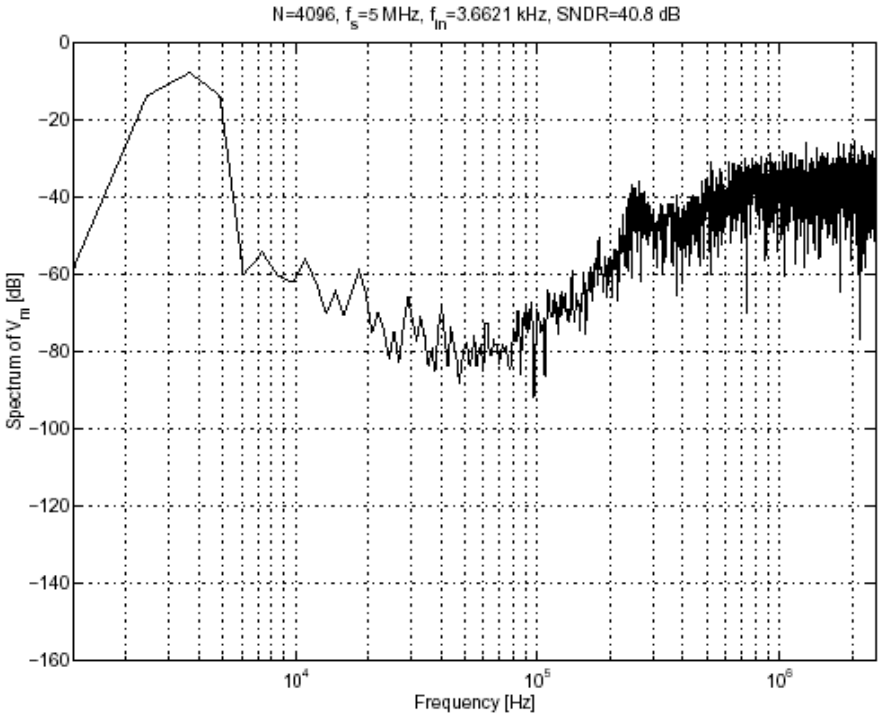


Figure 6.3. FFT result of the transistor level simulation

S1	46.6dB	S6	74.2dB
S2	47.1dB	S7	68.7dB
S3	64.0dB	S8	75.8dB
S4	67.6dB	S9	69.1dB
S5	79.9dB		

Table 6.1. Summary of SNDR

Besides this, early falling clock was tried to prevent the input dependent charge injection. In Figure 5.6, the channel charge of S11 and S12 is dependent on the input and the DAC respectively. If the clock falling edge of switches S1 and S2 is dropped earlier than those of S11 and S12, the charge in CA1 dose not change, since capacitor CA1 is floated. Therefore, the channel charges of S11 and S12 do not result in harmonics but just offset. However, this method did not solve the distortion problem. Another tried method was to reduce the input amplitude. In previous simulations, a 4 Vp-p sine input was used. However, in another simulation, this input amplitude reduced under 2Vp-p to check the saturation in ADC.

Although several methods were tried to solve the problem, there was still a distortion problem. Thus, the different types of switches and delta sigma ADC structures should be considered to solve the distortion problem.

7. LAYOUT

In this chapter, layouts of inverter based biquad LPF and inverter based the second-order delta-sigma ADC are presented. The 0.5-μm CMOS technology was used to implement layouts.

7.1. Inverter Layout

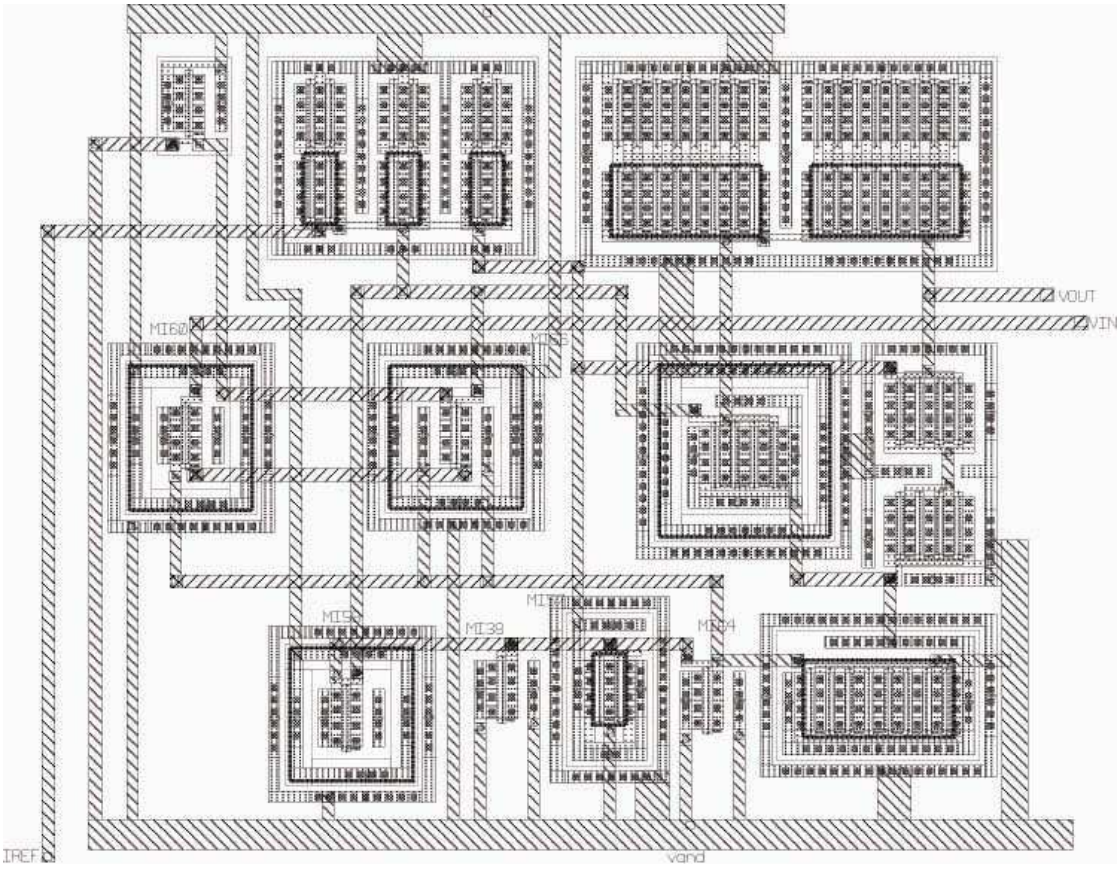


Figure 7.1. Inverter layout

A few of NMOS, PMOS, and low threshold voltage PMOS were implemented. IREF metal line providing the current is connected to the pad and this pad will be connected to the off chip resistor. The current can be varied with the resistor value .

7.2. LPF and ADC Layouts

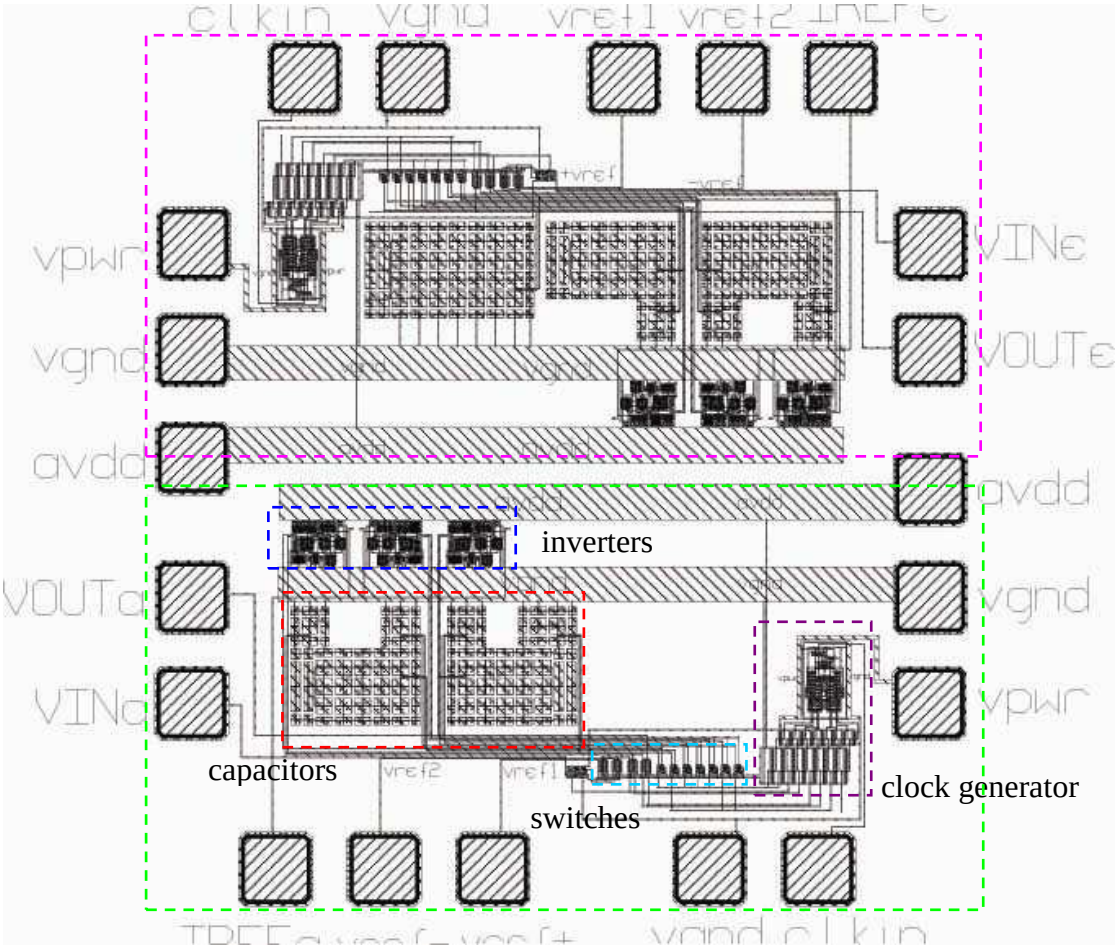


Figure 7.2. Inverter based biquad LPF layout

α-damping and e-damping filters were implemented in one chip for the purpose of the test. As seen in Figure 7.2, the upper plot is e-damping filter and the lower plot is α-damping filter. Figure 7.3 is the layout of the inverter based the second-order delta-sigma ADC.

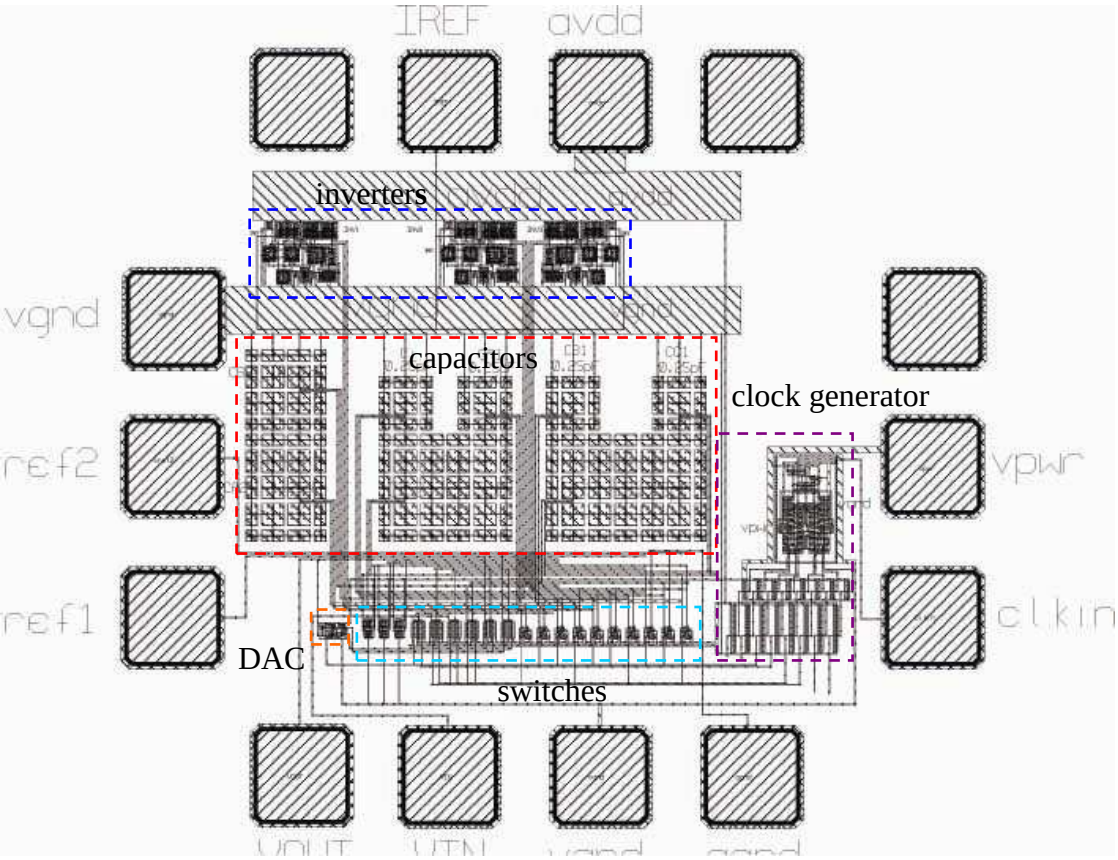


Figure 7.3. Inverter based second-order delta-sigma modulator layout

8. CONCLUSION

This thesis explored the possibility of replacing an op-amp with a simple inverter. A biquad filter and a second-order delta-sigma modulator using simple inverters are presented to verify the feasibility of the inverter based switched-capacitor circuits. Both the circuits are designed in the 0.5-μm CMOS technology.

The system level simulations showed that the SNDR of 85.2 dB can be achieved using these inverters in a delta-sigma modulator ADC. When ideal circuit components were used, the circuit level simulation result showed a SNDR of 81.7 dB. This result was about 5 dB lower than predicted from the system level simulation done in MATLAB. The result could be better if the number of samples used in simulation was increased. Also, when the real transistor level circuits, except for the switches were used, the performance result was SNDR of 81.3 dB. This result shows the feasibility of using inverter instead of op-amp in SC circuits. However, when all the circuits including switches are used, harmonics come out. These seems to be from transistor level switches. This distortion problem is not related with the switch size, indicating that this problem does not result from the amount of the switch channel charge. Different types of switches and switch sizes were simulated to solve this problem. In addition to these simulations, the early falling clock and reduced input amplitude were used in simulation. Nevertheless, the distortion problem was not solved. Thus, the different types of switches and delta sigma ADC structures should be considered to solve the distortion problem.

This thesis work showed that if the real transistor level circuits except switches are used, the performance is comparable to the system level result. Thus if switches problem is solved, op-amp could be replaced the inverter in switched-capacitor circuits. Finally, the layouts of the biquad filter and ADC were done.

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