AN ABSTRACT OF THE THESIS OF

Kai Tuan Yan (Kelvin) for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on January 8, 1996. Title: Noise Measurements, Models and Analysis in GaAs MESFETs Circuit Design.

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This research work focuses on the mechanism for the generation of thermal and 1/f noise in GaAs MESFETs. The goal of this research is to attain a more accurate noise model for GaAs MESFETs to update as well as upgrade existing noise models in the open literature. Circuit designs in III-V or compound semiconductor technology are only as good as the device models and knowledge of the noise characteristics.

A thermal noise model that includes hot electron effects has been derived for GaAs MESFETs. Specifically, the model describes accurately the excess channel noise coefficient, or "gamma", which is several times higher than the theoretical limit of 2/3 for a JFET. Some simple approximations are made for hot electron effects which can be incorporated into the derivation and accounted for by a simple numerical integration technique. The measurement of this "gamma" is done by a dedicated circuit consisting of the devices under test and a low noise transimpedance amplifier . The experimental results of measured and calculated noise coefficients of depletion mode GaAs MESFETs in the 0.6μm and 1μm gate length GaAs MESFETs technologies are shown to be in good agreement.

The 1/f noise phenomena associated with devices involving semi-insulating materials, for instance GaAs MESFET's on semi-insulating GaAs, has long been a perplexing problem. No reasonable explanation has ever been given, although there are many different theories. A completely new theory which attributes the 1/f noise to the semi-insulating substrate itself is developed. The 1/f noise is a bulk phenomenon with localized high frequency variations and long range low frequency fluctuations in the substrate with the lowest frequency being constrained only by the thickness of the material. The model is based on employing a distributed equivalent circuit in evaluating the semi-insulating substrate. The results demonstrate a close agreement between modeled and measured data.

Noise Measurements, Models and Analysis in GaAs MESFETs Circuit Design

by

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Noise Measurements, Models and Analysis in GaAs MESFETs Circuit Design

1. INTRODUCTION

1.1 Brief History of GaAs MESFETs Noise Research

The purpose of this section is to summarize some of the key developments in the past which have had an important impact on the current state of noise theory for the GaAs MESFETs. The history of noise research is well documented in a contribution by Van der Ziel [1]. The historical development of the noise theory began with the development of Einstein's Theory of the Brownian motion of suspended particles. Schottky applied Einstein's theory and mathematically postulated the existence of thermal noise. Schottky was the first one to apply Fourier analysis to the random shot noise which was generated in a saturated thermionic diode. Van der Ziel further expounded on Schottky equation for shot noise and derived a diffusion model for noise. The early research on JFET's assumed the noise to be shot noise [1]. However, it was later discovered that the noise was thermal in nature. Van der Ziel [2] derived the spectrum of the drain current noise at saturation to be:

$$\overline{i_n^2} = 4kTg_m\Gamma\Delta f \qquad (1.1)$$

Where it was postulated by Van der Ziel that the value of Γ is between 1/2 and 1. It was further postulated by Jordan [3] that the Γ value for a MOSFET is 2/3. As the channel lengths are shortened to the order of less than 1μm, the value of Γ will be larger due to the existence of hot electron noise [4].

There are five types of noise sources in GaAs MESFETs: (1) flicker noise, (2) diffusion noise, (3) generation recombination noise, (4) shot noise and (5) thermal noise.

1.2 Different Types of Noise Sources in GaAs MESFETs

1.2.1. Flicker Noise or 1/f Noise

There are many different explanations of flicker noise or 1/f noise. Duh et. al [5] attributed the 1/f noise to number fluctuation of carriers in the channel that is usually associated with oxide trapping states. They observed that this noise is most prevalent in the frequency range 20Hz to 600Hz. In MOSFET's, the flicker noise is temperature independent and is due to the large interface between the semiconductor and the oxide [8].

Explanations of the origin of 1/f noise in GaAs devices are varied and this explains the difficult nature in obtaining a credible theory for 1/f noise in GaAs devices. In fact, according to Hughes et al. [6] the 1/f noise corner frequency of recent commercial MESFETs does not vary much from the 50 MHz noise corner frequency found by Hooper et al. at a research laboratory in 1969. The explanations of the sources of the origin of 1/f noise range from quantum noise, generation recombination noise, intervalley scattering, lattice scattering, mobility fluctuations, bulk traps, metal-interface states, backside interface, substrate problems, number fluctuations, temperature fluctuations, and surface states etc.

An early attempt to describe the 1/f noise of GaAs MESFETs is a paper by Shu et al. [7] which tried to discriminate between number fluctuation and mobility fluctuation in

1/f noise. In another attempt at a 1/f noise theory, Van der Ziel in his papers [8] [9] gave an empirical theory of 1/f noise in terms of Hooge's parameters which is an attempt to come up with a better model to fit experimental data. It should be noted that Hooge's parameter is not at all constant for a particular type of solid state device. For example the value Van der Ziel obtained in 1985 [8] varies greatly from that of Tacano [9] in 1991. There are many different theories in the open literature on 1/f noise, however there is no unified theory which can effectively describe the 1/f noise characteristics of GaAs devices.

1.2.2 Diffusion Noise

Diffusing impurity ions or dislocations along dislocation lines can result in diffusion noise. Rucker-Hellum's [10] experimental data shows a non-monotonic current dependence for low frequency noise characterized by $1/f^{\alpha}$ where α is close to 1 below 1 KHz and 1.1 to 1.3 for frequency above 1KHz at low currents. However, for high currents α is close to 2.

Diffusion noise usually occurs in the frequency range of 600Hz to 2MHz. A explanation of diffusion noise is given in reference [11]. In this case the noise is due to the diffusion of a trap.

The theory of one-dimensional diffusion noise has been modified and applied to explain the low frequency noise in GaAs current limiters [12]. The diffusion constant depends exponentially on temperature and the activation energy varies with electric field because of the Poole-Frankel effect. The calculated activation energy is very close to the value reported in connection with leakage current in GaAs MESFETs. The diffusion

constant differs by many orders of magnitude from the diffusion constant of electrons or the one-dimensional diffusion of ions along dislocation lines. The problem with the latter theories is that they imply mass transfer from one location to another.

1.2.3 Generation and Recombination Noise

Generation and recombination noise occurs at approximately 10 KHz when the FET is biased at high currents. This is not a measurement artifact but such bumps are characteristic of a single energy level transition such as trapping-detrapping or an intervalley scattering type of process [10]. It has been claimed by Hughes et al. [6] that generation and recombination is the domination contributor to 1/f noise and can be reduced by determining an optimum doping level of the channel.

On the other hand, Forbes et al. [13] have clearly demonstrated that 1/f noise is not due to the generation and recombination process. By increasing the temperature of the devices the bumps associated with generation and recombination noise all move to higher frequencies, leaving behind a residual 1/f noise component. Forbes proposed and demonstrated that a buried channel device structure can be used to suppress generation recombination noise. Unfortunately, the p-type barrier layer at the surface did little to reduce 1/f noise. [13, 14]

1.2.4. Thermal Noise and Hot Electron Noise

For a GaAs MESFETs biased in the pinch off region, there is an additional noise source which needs to be taken into account as described in a paper by Baechtold [12].

This noise source is said to be due to the intervalley scattering noise which is commonly known as the hot electron noise, and Baechtold shows that it can be reduced by reducing the thickness of the channel. The introduction of hot electron noise is due to the reduction in the gate length which results in high field strengths in the channel and a reduction in the carrier mobility. Baechtold points out that the noise model by Van der Ziel [2], [15] is only valid for long channels FETs where the carrier mobility and noise temperature remain fixed. However, when the gate length of the channel is reduced, hot electron noise is observed and a more accurate noise model takes into consideration the noise temperature which is a function of the electric field.

Van der Ziel has attempted to describe some of the other characteristics of thermal noise [16]. Γ for long channel devices has the value about 2/3, but for short channel devices, in which the gate covers only a small part of the channel as in most GaAs FETs, Γ will be larger even if no hot electron effects are present due to a geometry effect. When hot electrons do exist, Γ becomes considerably larger and increases with decreasing temperature.

If the current is high but the drain voltage is kept relatively low to avoid overheating, at lower frequency, Γ varies as 1/f as expected for flicker noise whereas at higher frequency attains a limiting value that is larger than that expected for thermal noise. The current understanding is as follows; the effect at high temperature is due to the a geometry effect possibly aided by a temperature-independent hot electron effect, whereas the low-temperature data reflects a temperature-dependent hot electron effect.

1.3 Summary

Various values which have been experimentally determined for Γ ranging from 1.589 to 2.164 by Ogawa [17] and a more recent paper by Scheinberg et al. [18] gave a value of 1.7 for Γ, but listed no reference or reason. There is no clear understanding of noise in GaAs MESFETs technology. Even in the case of channel noise there is no reliable data for the appropriate value for Γ. Worst of all there is still no reasonable explanation for the large 1/f noise corner frequency of up to 100 MHz.

1.4 Overview of the Chapters

Chapter 2 details the different type of GaAs MESFETs models that are present in the PSpice simulator. It also gives an overview of the ion implantation GaAs MESFETs process. Chapter 3 examines the two different noise measurement techniques. The first technique uses discrete MESFETs which are coupled with a low noise bipolar amplifier. The second technique uses a dedicated circuit with test devices integrated with a transimpedance amplifier circuit. Chapter 4 describes the theory for the channel noise coefficient of a GaAs MESFETs. It gives the relationship between hot electron effects and the channel noise. Chapter 5 is an extension of the theory of the channel noise coefficient to include sub-micron MESFETs. Chapter 6 outlines the theory and model for the 1/f noise of GaAs MESFETs. All these results are summarized in chapter 7 and an attempt is made to place these findings into perspective. Numerous recommendations are made for future work.

2. GaAs MESFETs MODELS

2.1 Introduction

Device models seek to reflect the critical characteristics of the device with the complexity of the model limited by consideration of the need to use computer time as efficiently as possible. Device models can be physical, empirical or semi-empirical. The device models that we are primarily interested in are the GaAs models. The GaAs models as given in PSpice [19] are listed as follows Curtice model, Statz model and finally TriQuint model; these are called Level 1 ,2 and 3 respectively. It should be noted that all of these models are semi-empirical in that they are based on physical formulae that are coupled with arbitrary fitting parameters for adjustment to approximate a particular fabrication process. A summary of the different GaAs MESFETs models in the open literature has been given by Yan [20].

2.2 GaAs MESFETs Models

2.2.1 Curtice Model

The Curtice equivalent circuit is as shown in Fig. 2.1. The drain current I_{ds} is approximated by,

$$I_{ds} = \beta(1+\lambda V_{ds})(V_{gs} - V_T)^2 \tanh(\alpha V_{ds}) \qquad (2.1)$$

where V_{ds} is the drain to source voltage, V_{gs} is the gate to source voltage, V_T is the threshold voltage, and β, λ and α are fitting parameters. Curtice [21] uses the same

equation to estimate the drain current for both the linear and saturation region. Therefore the model does not reflect very accurately the variation of I_{ds} with changing V_{gs} especially if the V_T is large [21].

2.2.2 Statz Model

The Statz model [22] uses the same equivalent circuit, Fig. 2.1, as the Curtice model. The difference is in the modeling of the drain current. Statz's model gives a good prediction of the drain current, I_{ds}, in both the linear and saturation region.

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1 + B(V_{gs} - V_T)}(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \qquad (2.2)$$

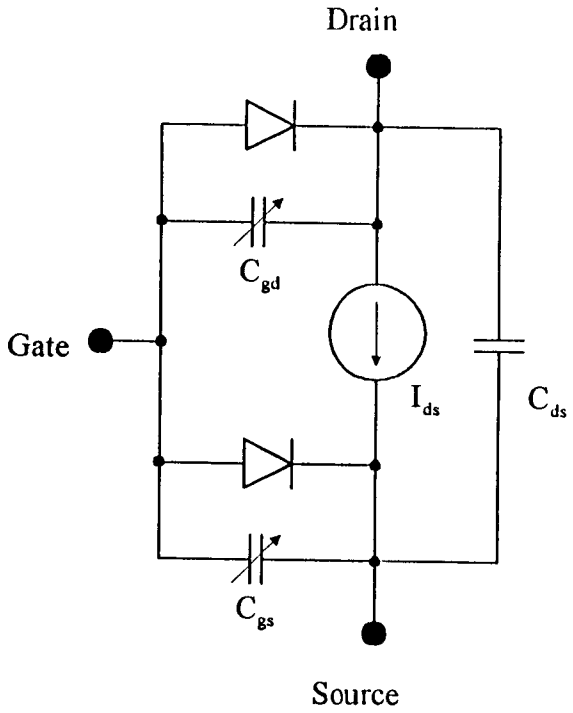
where B, β, λ and α are fitting parameters. B has a value between $.5V^{-1}$ and $2.6V^{-1}$, and is a measure of the doping profile extending into the semi-insulating substrate and therefore is dependent on the fabrication process.

2.2.3 TriQuint Own Model, TOM

The TriQuint Own Model or TOM model [23] is a modification of the Statz's model as shown in Fig. 2.2. At low values of the drain current, I_{ds}, with the device biased near cutoff, the Statz model give erroneous predictions of the small signal parameters such as gain and drain resistance over the dynamic range of the device.

The first modification is to have a better drain conductance fit at low drain current. This is done by modifying the V_T in the Statz's drain current equation as follow,

$$V_T' = V_T - \gamma V_{ds} \qquad (2.3)$$



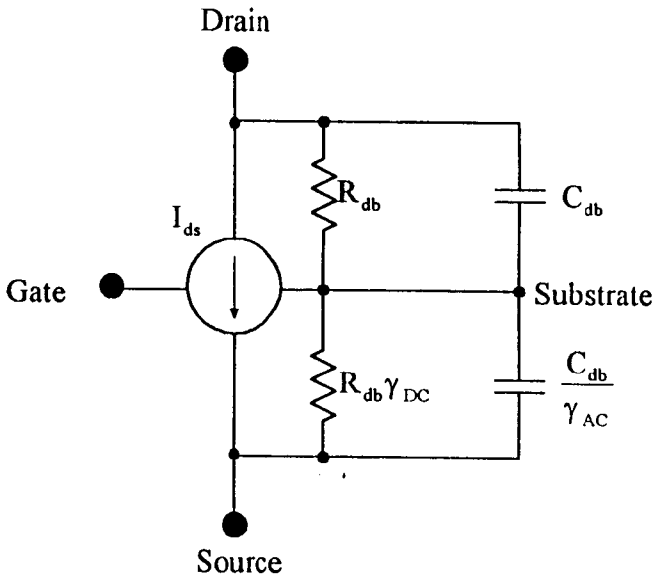
Level 1 Curtice Model

$$I_{ds} = \beta(1+\lambda V_{ds})(V_{gs} - V_T)^2 \tanh(\alpha V_{ds})$$

Level 2 Statz Model

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1+B(V_{gs} - V_T)}(1+\lambda V_{ds})\tanh(\alpha V_{ds})$$

Figure 2.1 Pspice Level 1 & 2 GaAs MESFETs



$$I_{ds} = \frac{I_{dso}}{1 + \delta V_{ds} I_{dso}}$$

$$I_{dso} = \beta\left(V_{gs} - V_T'\right)^Q \tanh(\alpha V_{ds})$$

$$V_T' = V_T - \gamma V_{ds}$$

Figure 2.2 Pspice Level 3 GaAs MESFETs Model

A nonlinear equivalent circuit model for the GaAs FET has been developed based on the small-signal device model and separate current measurements including drain-gate avalanche current data from a paper by Curtice [24]. Materka [25] developed a simple and fairly accurate large signal dynamic circuit type model for the GaAs MESFETs for use in circuit design. This modification of the Statz model, as given in the previous section, has been suggested by both the Materka [25] and Curtice [24],

$$I_{ds} = \frac{I_{dso}}{1+\delta V_{ds} I_{dso}} \tag{2.4}$$

Another modification is given in above equation for I_{ds} which reflects the way in which the drain current is reduced at higher values of current and voltage.

$$I_{dso} = \beta(V_{gs} - V_T)^Q K \tanh(\alpha V_{ds}) \tag{2.5}$$

The value of Q in the above equation is approximately equal to 2. This equation is the Statz model for the drain current with B and λ set to zero. Therefore, the TOM parameters γ and δ replace B and λ in the Statz model.

2.3 PSpice Noise Parameters

The noise parameters in PSpice [19] are calculated in a 1Hz bandwidth with the following spectral power densities as shown below.

For the parasitic sheet resistances, R_s, R_d and R_g the resistive thermal noise is,

$$\overline{I_{R_s}^2} = \frac{4kTArea}{R_s} \tag{2.6}$$

$$\overline{I_{R_d}^2} = \frac{4kTArea}{R_d} \tag{2.7}$$

$$\overline{I_{R_g}^{\,2}} = \frac{4kTArea}{R_g} \tag{2.8}$$

The intrinsic noise of GaAs MESFET is calculated by the formula,

$$\overline{I_{ds}^{\,2}} = 4kTg_m\Gamma + [KF * \frac{\{(I_{ds})_{DC}{}^{AF}\}}{Freq}] \tag{2.9}$$

The $4kTg_m\Gamma$ in equation (2.9) is the thermal noise while $[KF * \frac{\{(I_{ds})_{DC}{}^{AF}\}}{Freq}]$ is the 1/f noise component. It will be shown later that the current Pspice noise model is deficient and will be replaced by a more accurate physical model.

2.4 GaAs MESFETs Process

The fabrication process used in the manufacture of GaAs MESFETs is similar to the ion implantation process of silicon integrated circuits. The main difference lies in that GaAs MESFETs process is done at a lower temperature because the GaAs wafers start to dissociate at temperature above 550°C.

Fig. 2.3 is the cross sectional view of TriQuint Semiconductor's QED/A or L=1μm process. The gold-based interconnect technology uses airbridge technology as shown in Fig. 2.3. The use of gold provides low resistance interconnect and allows higher current density.

In addition, TriQuint Semiconductor has also implemented a sub-micron technology process called QED/2. This technology uses a selective buried P-layer implant to shield the effect of substrate defects and thus reduce the frequency dependence of the output conductance. The electrons trapped in deep levels will remain captured for times

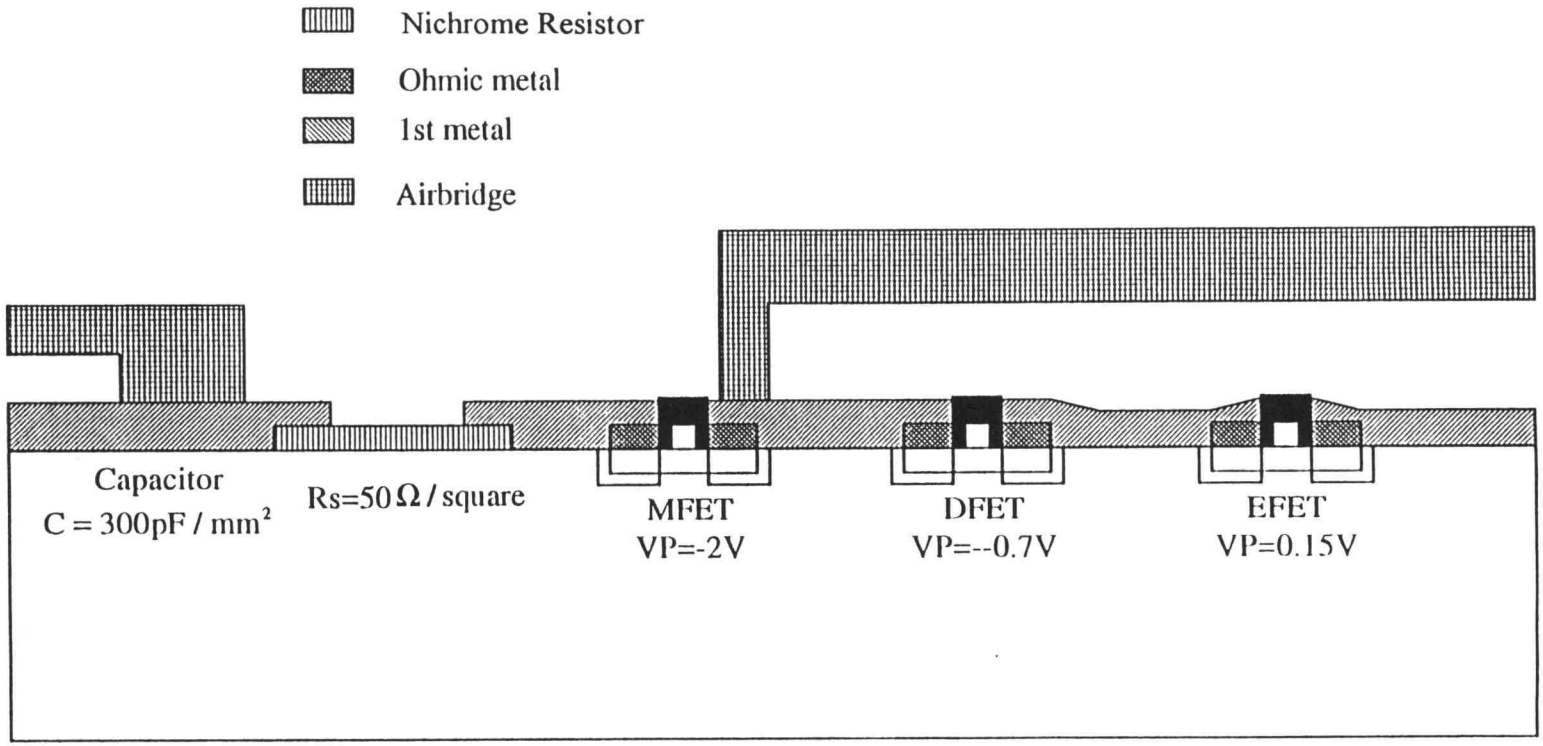


Figure 2.3 QED/A GaAs MESFETs Process

on the order of microseconds to seconds. These long time constants correspond to frequencies in the approximate hertz to megahertz range which are observed in the low frequency dispersion. Also, the airbridge technology used in the QED/A process is abandoned for 4 layers of metal interconnect separated by approximately 1μm of dielectric.

Both QED/A and QED/2 process offer high precision nichrome thin-film resistors. The QED/2 process with the reduction in gate length has boosted the unity gain frequency, F_t, from 12GHz in the QED/A process to approximately 20GHz in QED/2 process. This research work is mainly concerned with the depletion mode MESFETs or DFET used in these two technologies.

2.5 Summary

Fig. 2.4 is a common general representation of a fiber optics data link. Low noise design is crucial in order to produce a high performance data link. Better noise models will ultimately lead to better circuit design with low noise performance. For instance, the capability to design a transimpedance amplifier, which forms a part of the front end detection in the receiving end of a fiber optics network, will improve the bit error rate. An understanding of these device and bias considerations are necessary to optimize utilization of MESFETs in low noise amplifiers for fiber optic communication systems and other applications.

Another impact of better noise models in the fiber optic data link is in the clock and data recovery sub-system. Phase noise is a crucial consideration in the loop filter

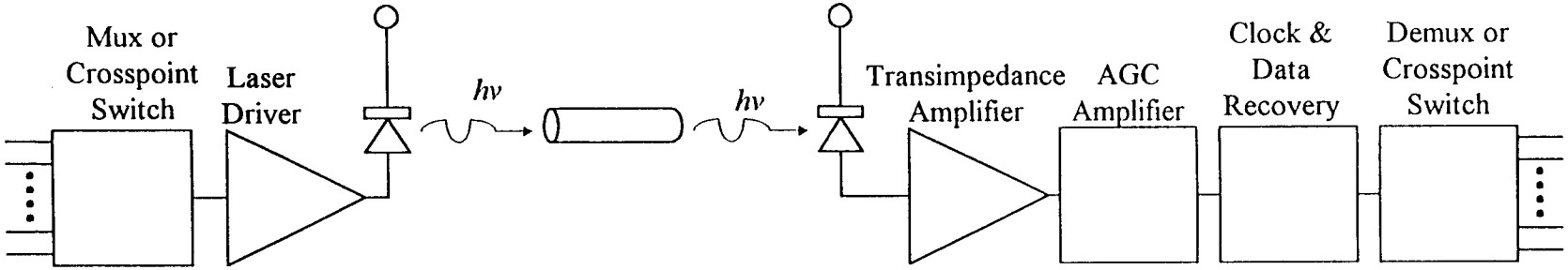


Figure 2.4 Fiber Optics Data

design of a phase lock loop system. The design of faster loop filter is more complex and a better prediction of the phase noise will enable the designer more flexibility to take advantage of the usable frequency range before the circuit is dominated by the lower frequency 1/f phase noise. Therefore, an accurate 1/f noise model will allow the designer to have an optimum loop filter design for maximum jitter suppression.

3. NOISE MEASUREMENTS TECHNIQUES OF GaAs MESFETs

3.1 Introduction

We have established two noise measurement methods for GaAs MESFETs. The first method uses discrete MESFETs integrated with a low noise amplifier. The second method demonstrates the method of integrating the MESFETs under test with a transimpedance amplifier specifically designed for noise measurement. Integrating the depletion mode MESFETs or DFET with a transimpedance amplifier has the advantage of reducing the parasitic capacitance and inductance as compared to using discrete individual components [1-2].

3.2 Noise Measurement of Discrete Depletion Mode GaAs MESFETs, DFET

The initial phase of this work involved using classical techniques to measure noise with discrete MESFETs and small bipolar amplifiers [30]. GaAs MESFETs were hybrid mounted with low noise, high frequency bipolar video amplifiers. As shown in Fig. 3.1 and Fig. 3.2, attention is taken to ensure proper shielding of the circuitry which is mounted on a copper board. Care is also taken to avoid ground loops. The noise is measured using a spectrum analyzer with a DC block at the output prior to being connected to the spectrum analyzer, which is denoted by the 50Ω load on the extreme right in both Fig. 3.1 and Fig. 3.2. The gain of the low noise amplifier or LNA can be selected. In the low frequency setup, Fig. 3.1, a low gain of 100v/v is selected for a larger amplifier

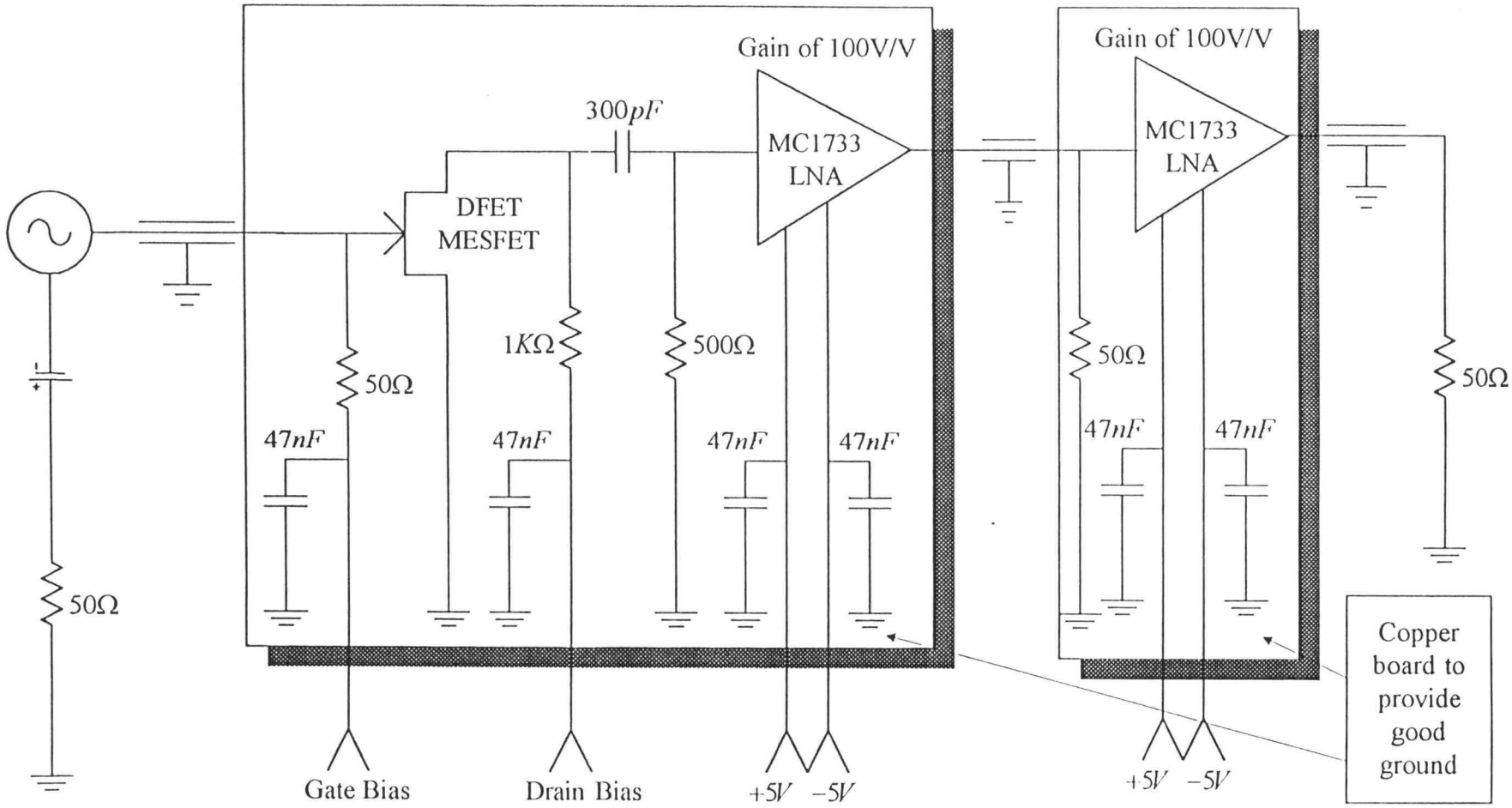


Figure 3.1 Noise measurement test setup for discrete DFET MESFETs at low frequency 20KHz to 5MHz

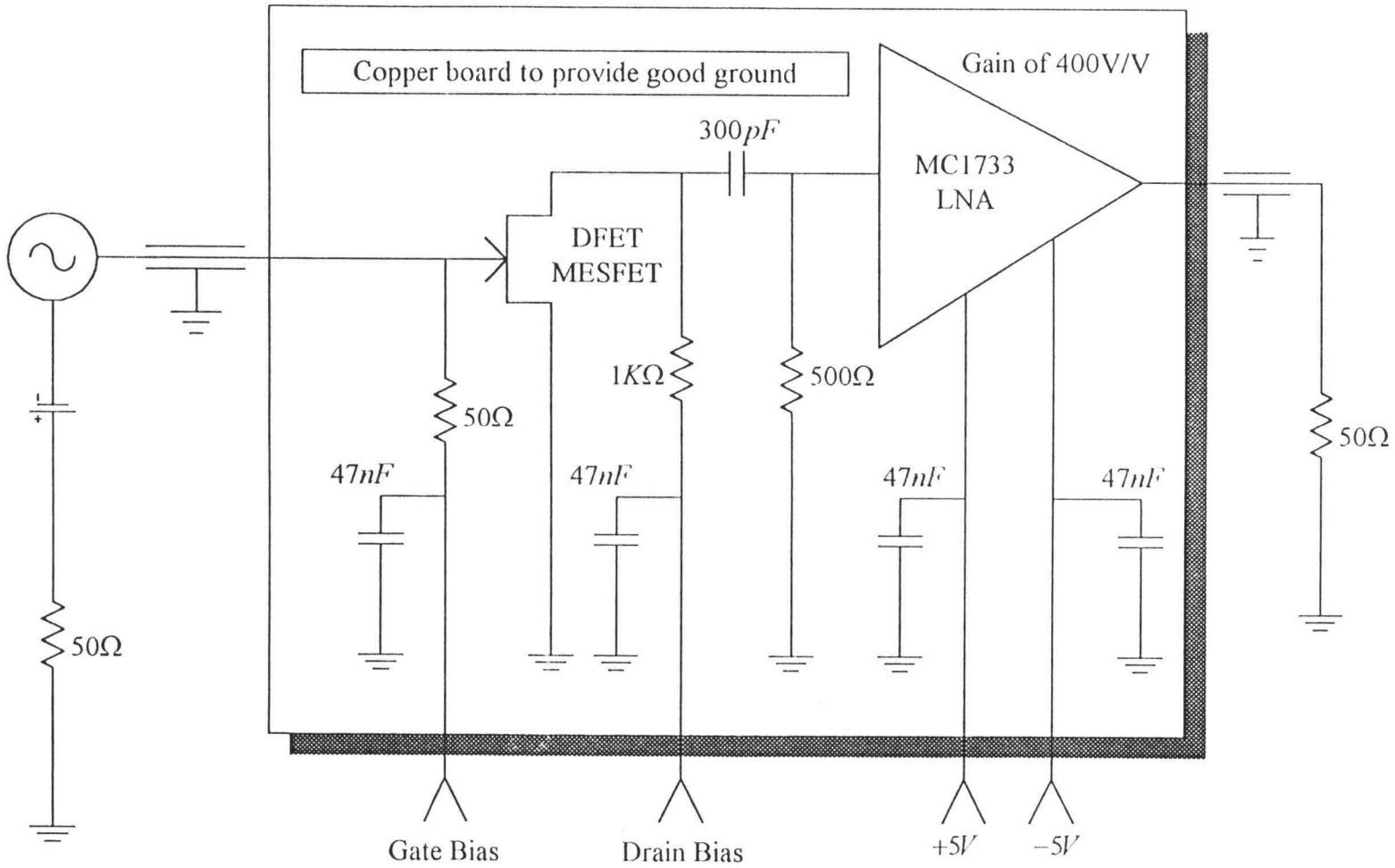


Figure 3.2 Noise measurement test setup for discrete DFET MESFETs at high frequency 5MHz to 105MHz

bandwidth. In this setup the overall gain of the system is increased by cascading an amplifier of similar gain in series. In the high frequency setup, a gain of 400v/v is selected for the amplifier that provides enough bandwidth and sufficient gain for measurement up to 105MHz.

The spectrum analyzer will measure the system noise when the device under test, DUT, is in the off mode. When the device is biased in the saturation region, the noise measurement is taken again. The increase in the noise level is due to the additional channel noise of the DUT for that particular biasing point. The square root of the difference of the squares of the measured RMS noise voltages with the FET in the "on" and "off" conditions gives the total noise of the depletion mode FET at the output of the system. With the DUT connected, the gain of the system is measured from the gate of the DUT. Therefore, the RMS noise referred from the output to the gate of the DUT can be computed. The noise voltage at the drain of the DUT is then calculated since the gain of the DUT is known. The RMS current is calculated by dividing the input noise voltage at the amplifier by the input resistance.

Both systems have been calibrated using a noise diode for accuracy. A correction needs to be applied in using the Tektronix spectrum analyzer since the noise bandwidth is not the same as signal bandwidth. For a signal bandwidth of 30KHz, the measured noise is about 3dbm smaller than the actual value in accordance with the application note for the spectrum analyzer used in this experiment. The RMS noise current is quite flat around 20MHz as shown in Fig. 3.3. It is also noted there are generation and recombination noise components as indicated by the hump at frequencies around 100KHz.

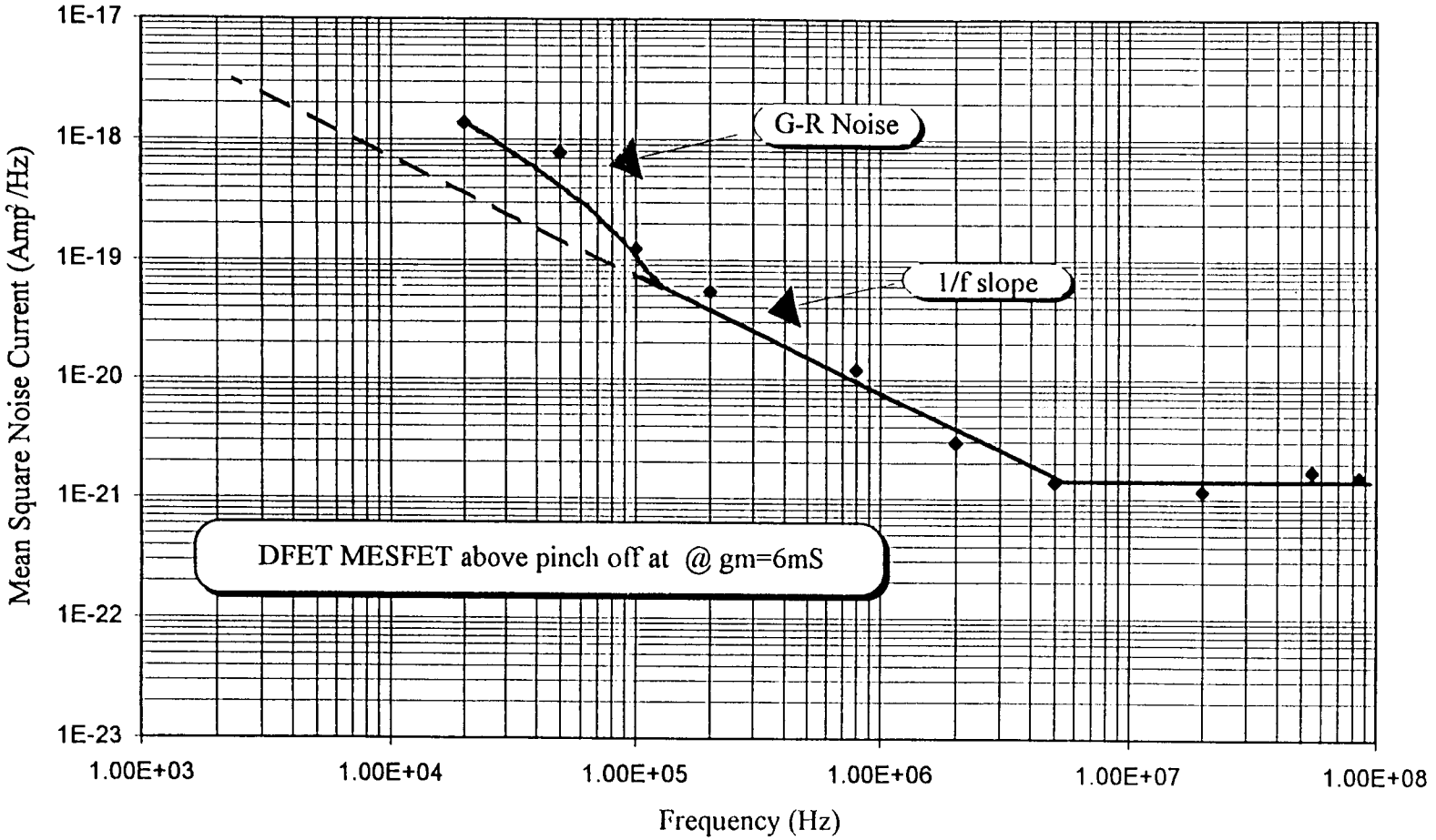


Figure 3.3 Noise spectrum of discrete GaAs depletion mode MESFETs

3.3 Noise Measurement using Transimpedance Amplifier with Integrated DFET

The circuit schematic of the transimpedance circuit design with integrated devices under test consisting of short gate length DFET MESFETs of W/L of 120μm/1μm and long gate length DFET MESFETs of W/L of 400μm/8μm. The circuit is designed so that the selected DUT can be bonded and tested separately. The drains of both DUTs are AC coupled to a broad band transimpedance amplifier so that a direct measurement of the channel noise of the DUT can be made [31].

The circuit has been simulated with bonding and wiring parasitics using PSPICE with the level 3 model or TriQuint Own Model, TOM. The transimpedance amplifier (TIA) is a low noise, high gain single stage cascode amplifier. The simplified schematic of the TIA is as shown in Fig. 3.4. This high performance transimpedance amplifier uses a similar amplification methodology for the input stage as an earlier low noise transimpedance amplifier with automatic gain control capability [32].

The semi-insulating substrate of the GaAs MESFETs technology greatly reduces parasitic capacitances and thus is an excellent choice for low noise high speed applications. To further enhance the low noise capability of GaAs MESFETs technology, clever circuit tricks can be employed. For instance, we chose resistive loads, R1 and R2 for the input cascode stage to minimize the contribution of the channel noise of the active load MESFETs. However, there is a tradeoff between gain and noise when choosing between the passive resistive load and an active MESFETs load. A passive load provides low noise and low gain while an active load provides higher noise and higher gain. The supplementary current flowing through R1 has the effect of increasing the

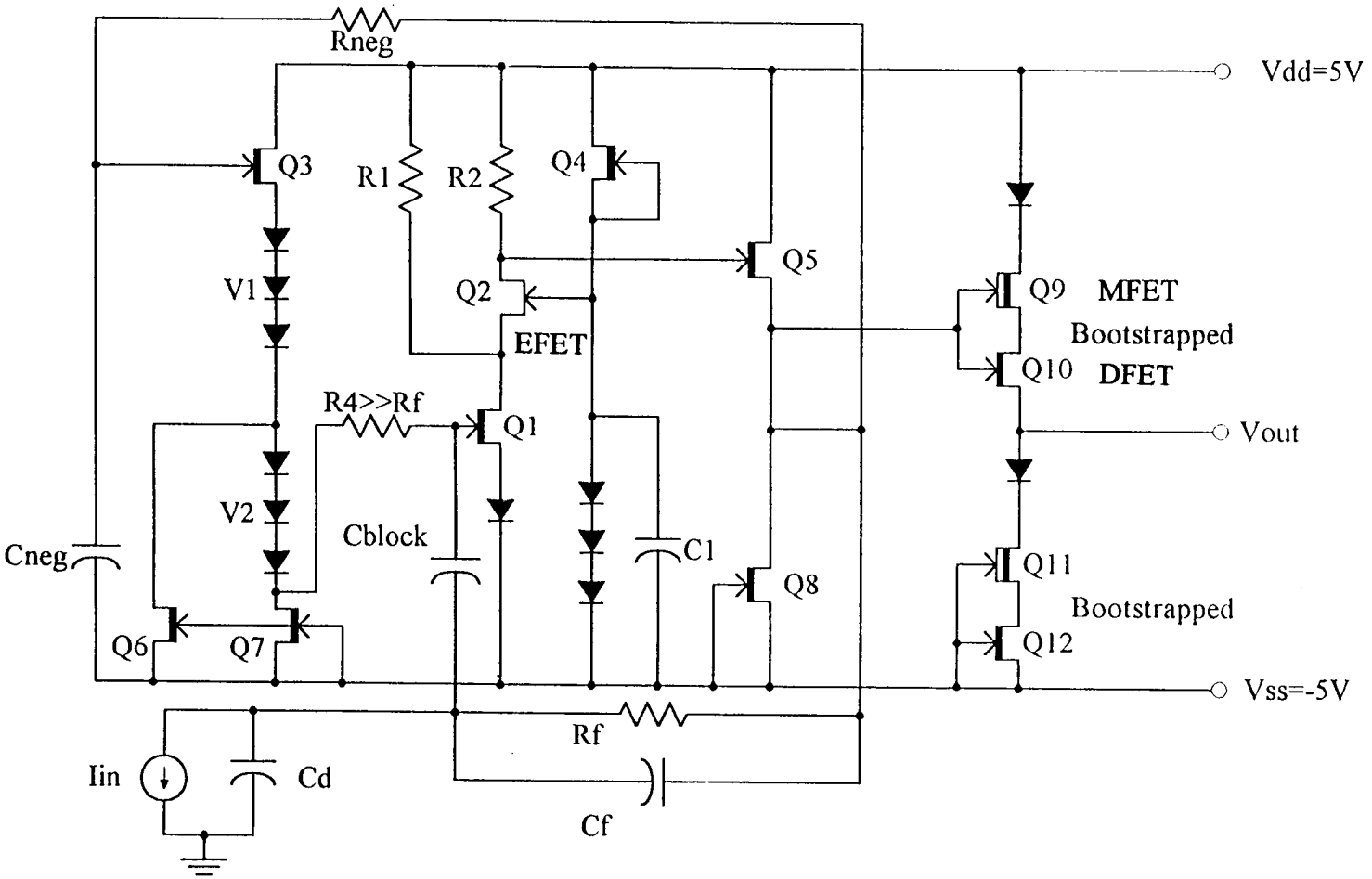


Figure 3.4 Simplified Schematic Diagram of L = 1μm transimpedance amplifier, TIA

transconductance of Q2 and thereby increases the gain of the cascode stage further. DC negative feedback is employed to establish the operating point [32].

The output stage is bootstrapped [33-34] to give a source follower gain at the output stage of close to unity. The output resistance is chosen to be $50\,\Omega$ for matching purposes as measurements are made over several hundreds of MHz. A blocking capacitance, Cblock is used to AC couple the input to Q1.

Cf is employed to reduce peaking. In addition, the circuit designed has no problem handling parasitic bonding inductances of 3nH and transmission line delays of 200ps in simulations in our region of operation of 100KHz to 500MHz. As indicated in Fig. 3.5, the resistor, R4, is implemented using long gate MESFETs with a width of $2\,\mu m$. Multiple FETs are employed to avoid saturation. The resistance of R4 is chosen to be $500K\,\Omega$ to provide the much needed boost in the input resistance at the gate of Q1 which is reduced by the negative feedback operation. The high resistance value of R4 as shown in Fig. 3.4 is achieved with a great reduction in die area as compared to using a NiCr thin film resistor.

It should be noted the overall TIA bandwidth is given by

$$TIA_{Bandwidth} = \frac{A_v}{2\pi R_f C} \qquad (3.1)$$

where A_v is the open loop gain of the amplifier, R_f is the feedback resistance and C is the total input capacitance.

In Fig. 3.6, a small current perturbation is introduced at the input of the TIA with the output driving a matched $50\,\Omega$ load. A smooth transimpedance curve is obtained showing a simulated effective bandwidth of 500MHz which was confirmed by

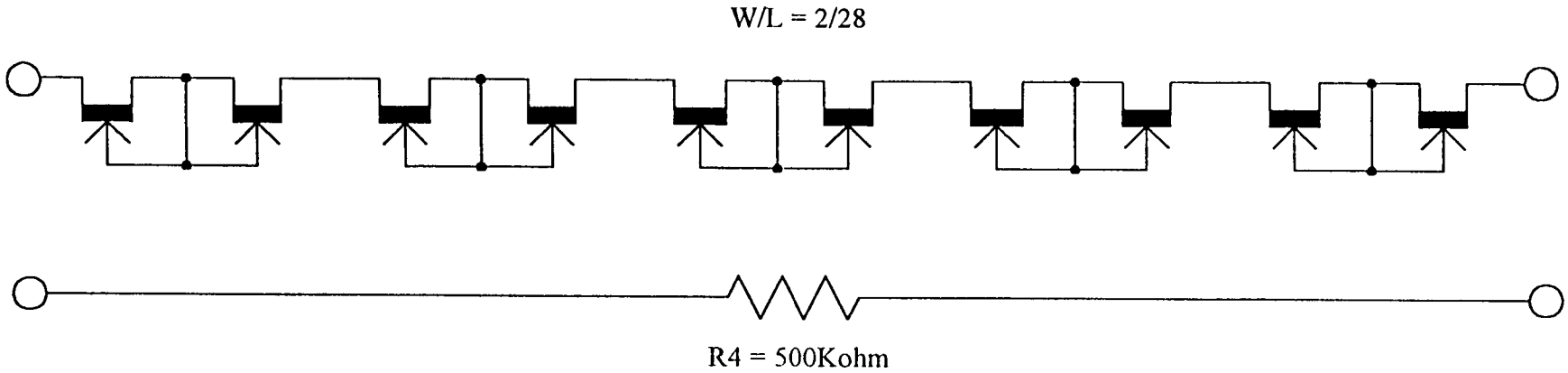


Figure 3.5 Depletion MESFETs Pinched Resistor

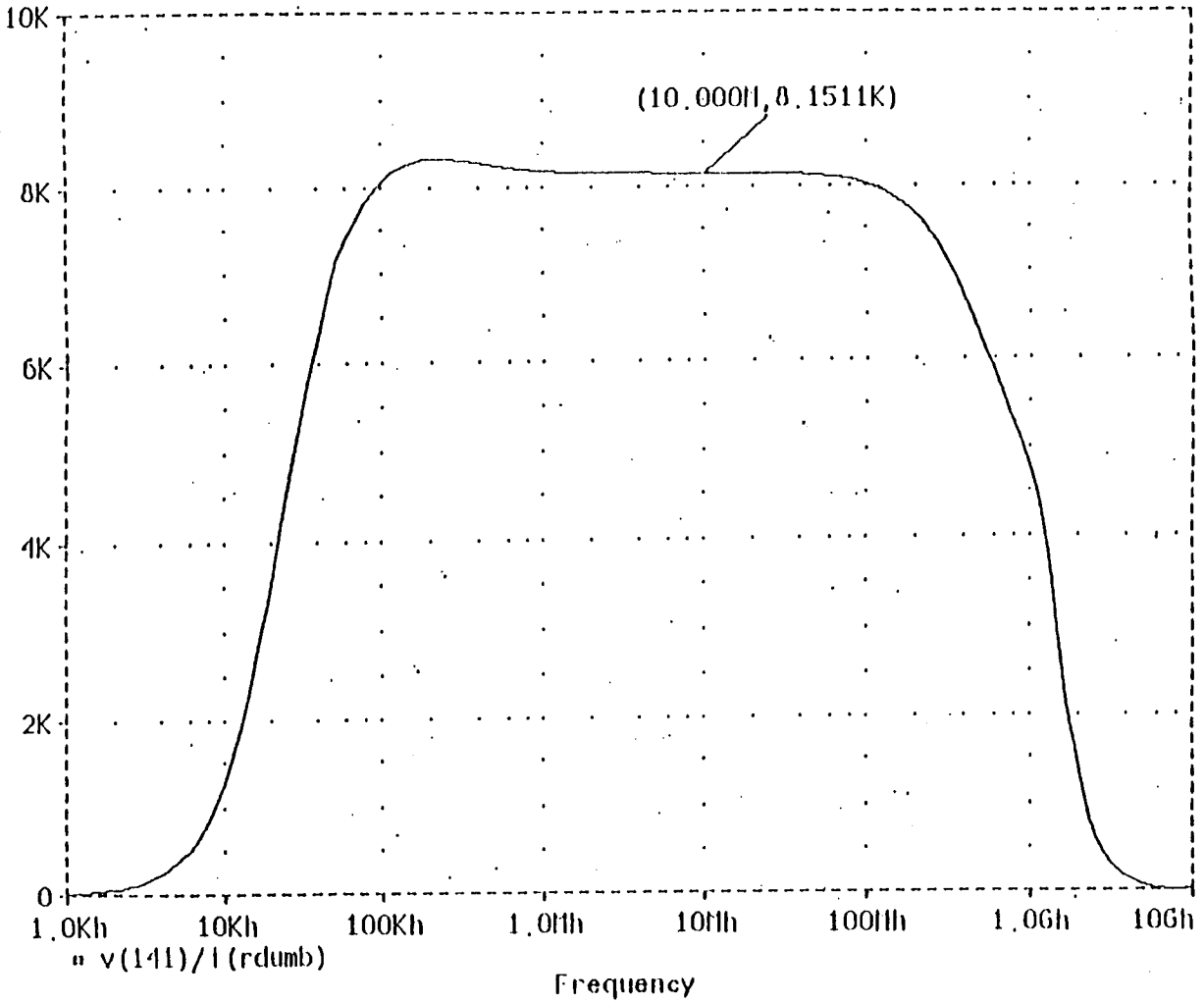


Figure 3.6 Effective bandwidth range of 100KHz to 500MHz of tranimpedance amplifier

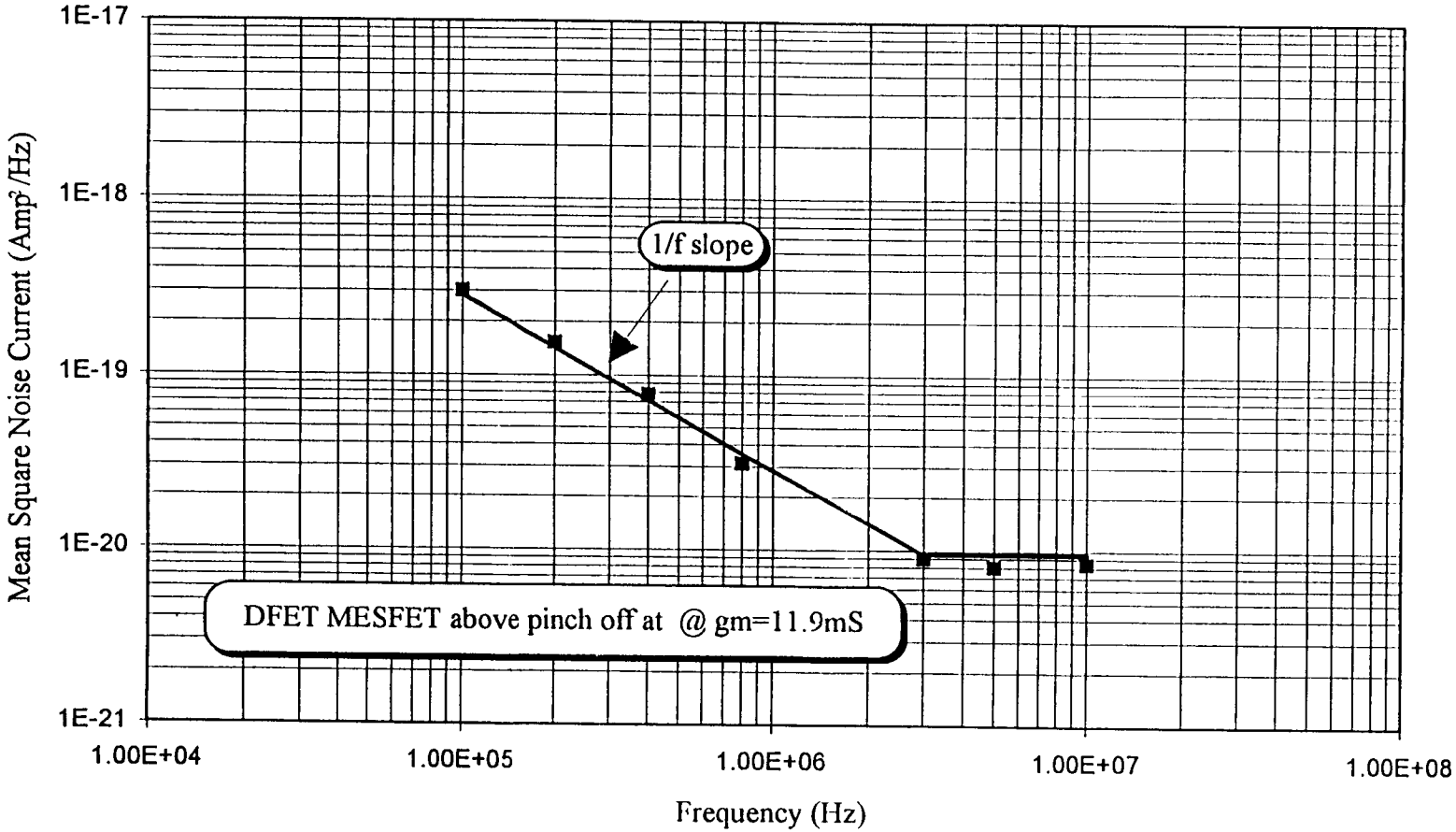


Figure 3.7 Noise spectrum of integrated GaAs depletion mode MESFETs

experimental measurements described in a later section. The DFETs under test have gate lengths of 1 μm and 8 μm. Both FETs which are bonded out separately in different die, share a common gate and drain. The experimentally obtained values of channel noise factor or Γ for both long gate and short gate length devices are reconciled with the modeled Γ values.

As mentioned in the earlier section, the normalized noise measurement computed by the square root of the difference of the squares of the measured RMS noise voltages with the FET in the "on" and "off" conditions give the total noise of the depletion mode FET at the output of the system. Therefore the RMS noise current as shown in Fig. 3.7 consist of both the 1/f and thermal noise of the MESFETs.

3.4 Summary

There is no unified theory nor reliable data on the exact dependence of noise on hot electron effects in MESFETs and bias conditions. Likewise, there is still no clear understanding of the basic cause of 1/f noise in III-V devices in general. The discussions in later chapters will serve to quantify the nature of the problem and set a lower bound for the usable frequency range of MESFETs. Analog designs in III-V or compound semiconductor technology are only as good as the device models and knowledge of the noise characteristics. The 1/f noise in particular is common to all III-V devices, and not just MESFETs. The results obtained have indicated that the 1/f corner frequency is in the range of 1MHz to 30MHz. These techniques for noise measurement will be the basis of noise measurements in later chapters.

4. CURRENT MODELS AND WORK ON CHANNEL NOISE IN FET's

4.1 Motivation

Van der Ziel [2] originally derived the equations for the mean square noise current of a JFET and obtained $\overline{i_n^2} = 4kT\Delta f g_{max} Q(x,y)$ where Q(0,0)=1 if the transistor is operating in the linear range, and Q(0,1)=1/2 for a forward biased gate and if the transistor is saturated with high transconductance g_{max}. For most bias conditions he suggested Q=2/3 as an appropriate value. Subsequently, Jordan et al. [3] applied the same type of analysis to a MOSFET and in the limiting case obtained

$$\overline{i_n^2} = 4kT\Delta f g_{max}(2/3) \qquad (4.1)$$

The value 2/3 has become widely accepted and is used in both PSPICE models for MESFETs and MOSFETs [39].

These theories hold below the saturation point and do not include the hot electron effects dominant in most micron and sub-micron devices. The original theory for JFET's was modified by introducing an effective temperature of the channel to account for hot electron effects [4]. This approach was adopted for MESFETs used at microwave frequencies and in modeling noise figures [5] [10] [11]. The approach at microwave frequencies is to make g_{max} large, $g_{max} >> g_s$ where $1/g_s$ is the source impedance in the gate circuit of the FET by using large width devices, typically W=300μm. The noise figure is minimized in this manner. For MOSFET Abidi [3] has more recently measured the channel noise of short channel MOSFET devices with hot electron effects where

$$\overline{i_n^2} = 4kT\Delta f g_{max}\Gamma \qquad (4.2)$$

and found Γ to vary from Γ=2/3 to Γ=8. No theory or explanation was however given. The situation in the industry is at best confused, most engineers have idea of what noise model to use and little reliable data to on which to base any noise model. This is best illustrated by PSPICE

$$\Gamma = 2/3 \qquad (4.3)$$

for any and all FET's regardless of bias condition and hot electron effects. Changing the value 2/3 requires recompiling the whole program and is not easily accomplished.

Even for just MESFETs alone clearly there is a need to provide measurements and data and modern devices as both function of bias conditions and with hot electron effects.

Measurements of channel noise at these frequencies is not easy and requires special care and careful calibrations. Our demonstrated ability to fabricate devices for test and transimpedance amplifiers on the same chip for frequencies above 100MHz constitutes a unique ability and advantage. Experience with past measurement has however demonstrated that we need to be able to measure the overall gain of the devices under test and the amplifier at all frequencies of interest. Simulations of an amplifier performance at other frequencies than those measured is not reliable in spite of using the best model available. This will require first using a 50Ω termination on chip at the gate to measure the gain. For noise measurements this will then be by-passed by wire bonding the 35pF capacitor. Using only the capacitor makes gain measurement above 10MHz difficult.

Also the measurements must be self consistent, once Γ in

$$\overline{i_n^2} = 4kT\Delta f g_{max}\Gamma \qquad (4.4)$$

is determined, then this value when put back into PSPICE should simulate the noise of the amplifier alone if the device under test is biased off.

In the subsequent section, a derivation is given for the channel noise coefficient of FET's operating in the saturation region [28]. Some simple approximations are made for hot electron effects which can be incorporated into the derivation and accounted for by a simple numerical integration technique. Experimental results of measured and calculated noise coefficients are compared for depletion mode MESFETs of different gate lengths. This model gives a much more realistic representation of the channel noise coefficients for short gate devices rather than the simple 2/3 value currently used in circuit simulations.

4.2 Channel Noise Coefficient Theory

4.2.1 Derivation of the Channel Noise Coefficient of a Saturated FET

The equations derived by Van der Ziel [2] and Jordan [3] apply only for an FET below saturation; the solution after saturation is taken as the limiting case. The technique of Jordan and Jordan [3] is to consider a FET in the linear or triode region with an AC short circuit between the drain and source. Each element of the channel is considered separately. The mean square noise current is calculated and its contribution to the drain noise current is thus determined.

Here, we provide an alternative solution [28] where we consider only a saturated FET as shown in Fig. 4.1. The equations here will be derived for a MOSFET but applied

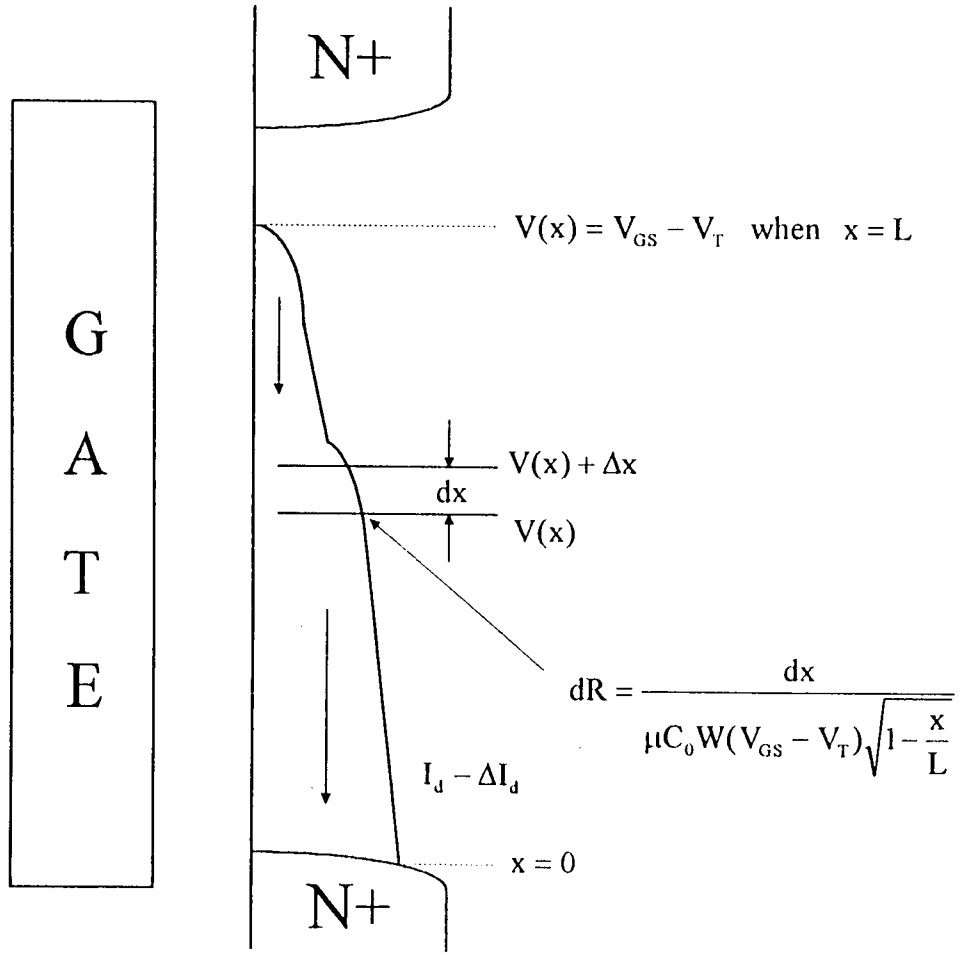


Figure 4.1 MOSFET in saturation showing a potential variation, ΔV, at location x along the channel

to a JFET; similar equations hold for a JFET but the algebra is more complicated. For a MOSFET in saturation, the potential at the drain end of the channel is

$$V(x) = (V_{GS} - V_T) \tag{4.5}$$

The potential variation along the channel is,

$$V(x) = (V_{GS} - V_T)(1 - \sqrt{1 - \frac{x}{L}}) \tag{4.6}$$

The conductance along the channel is therefore,

$$g(x) = \mu C_o W(V_{GS} - V_T - V(x)) \tag{4.7}$$

which can be written as,

$$g(x) = \mu C_o W(V_{GS} - V_T)(\sqrt{1 - \frac{x}{L}}) \tag{4.8}$$

For a small element in the channel length dx the resistance is then

$$dR = \frac{dx}{\mu C_o W(V_{GS} - V_T)\sqrt{1 - \frac{x}{L}}} \tag{4.9}$$

Nyquist's theorem states that the open circuit emf of a resistance R at temperature T, in a small frequency interval Δf, is $\sqrt{4kTR\Delta f}$. Using Nyquist's theorem, the potential variation at location, x, and for element dx is

$$\overline{V_n^2(x)} = 4kT\Delta f \frac{dx}{\mu C_o W(V_{GS} - V_T)\sqrt{1 - \frac{x}{L}}}$$

$$= 4kT\Delta f \frac{\frac{dx}{L}}{\mu C_o \frac{W}{L}(V_{GS} - V_T)\sqrt{1 - \frac{x}{L}}} \tag{4.10}$$

A potential ΔV, variation at point x, in the channel will change the drain current.

$$\int_0^L dx(I_d - \Delta I_d) = W \int_0^{V_x} \mu C_o (V_{GS} - V_T - V(x))dV$$

$$+ W \int_{V_x + \Delta V}^{V_{GS} - V_T} \mu C_o (V_{GS} - V_T - V(x))dV \qquad (4.11)$$

where without potential variation,

$$\int_0^L dx I_d = \int_0^{V_{GS} - V_T} \mu C_o (V_{GS} - V_T - V(x))dV \qquad (4.12)$$

and $$I_d = \mu C_o \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2} \qquad (4.13)$$

where $$g_{max} = \mu C_o \left(\frac{W}{L}\right)(V_{GS} - V_T) \qquad (4.14)$$

By expanding equation (4.11) and keeping only the first order terms in ΔV then,

$$\Delta I_d = \mu C_o \left(\frac{W}{L}\right)(V_{GS} - V_T - V(x))\Delta V \qquad (4.15)$$

and we can define a transconductance for variations at point x, which will be

$$g_m(x) = \frac{\Delta I_d}{\Delta V} = \mu C_o \left(\frac{W}{L}\right)\sqrt{1 - \frac{x}{L}} \qquad (4.16)$$

The mean square variation in the drain current due to variations at x will be,

$$\overline{i_n^2(x)} = \overline{V_n^2(x)}\, g_m^2(x) \qquad (4.17)$$

$$\overline{i_n^2(x)} = 4kT\Delta f \frac{\frac{dx}{L}}{\mu C_o \frac{W}{L}(V_{GS} - V_T)\sqrt{1 - \frac{x}{L}}} \left(\mu C_o \frac{W}{L}\sqrt{1 - \frac{x}{L}}\right)^2 \qquad (4.18)$$

$$\overline{i_n^2(x)} = 4kT\Delta f g_{max}(\sqrt{1-\frac{x}{L}})(\frac{dx}{L}) \tag{4.19}$$

and summing up all contributions, the total mean square fluctuation in the drain current will be,

$$\overline{i_n^2(x)} = 4kT\Delta f g_{max}\int_0^1 \frac{dx}{L}\sqrt{1-\frac{x}{L}} \tag{4.20}$$

which results in,

$$\overline{i_n^2} = 4kT\Delta f(2/3)g_{max} \tag{4.21}$$

This is the same result obtained by Jordan and Jordan [3] by considering a FET below saturation and then taking the limiting case. Our derivation here explicitly relates to a FET in saturation and we can clearly identify the two separate components contributing to the mean square drain current fluctuations. Specifically,

$$\overline{V_n^2(x)} = \frac{4kT\Delta f\frac{dx}{L}}{\mu C_o\frac{W}{L}(V_{GS}-V_T-V(x))} = \frac{4kT\Delta f\frac{dx}{L}}{\mu C_o\frac{W}{L}(V_{GS}-V_T)\sqrt{\left(1-\frac{x}{L}\right)}} \tag{4.22}$$

and

$$g_m(x) = \mu C_o(\frac{W}{L})(V_{GS}-V_T-V(x)) = \mu C_o(\frac{W}{L})(V_{GS}-V_T)\sqrt{1-\frac{x}{L}} \tag{4.23}$$

as such this particular formulation can then be used in modeling hot electron effects since $\overline{V_n^2(x)}$ and $g_m(x)$ can be considered separately.

4.2.2 Hot Electron Effects

Some of the early work on hot electron effects on FET noise performance are those of Klaassen [4] and Baechtold [12]. For GaAs MESFETs, we make some simple assumptions for the effective temperature,

$$T_e = T\left(1+\frac{\frac{dV}{dx}}{E_c}\right)^n \tag{4.24}$$

and dependence of mobility on electric field,

$$\mu = \mu_o\left(1+\frac{\frac{dV}{dx}}{E_c}\right)^{-1} \tag{4.25}$$

and the device equation,

$$I_D = I(x) = \mu C_o W((V_{GS}-V_T)-V(x))\frac{dV}{dx} \tag{4.26}$$

$$I_D + \frac{I_D dV}{E_c dx} = \mu_o C_o W((V_{GS}-V_T)-V(x))\frac{dV}{dx} \tag{4.27}$$

$$I_D dx = \mu C_o W((V_{GS}-V_T)-V(x))dV - I_D dV \tag{4.28}$$

If we integrate up to a position, x, where $V = V(x)$ then,

$$I_D x = \mu C_o W((V_{GS}-V_T)-\frac{V^2(x)}{2})dV - \frac{I_D V(x)}{E_c} \tag{4.29}$$

which can be solved for V(x),

$$V(x) = (V_{GS}-V_T)\left[(1-b)-\sqrt{(1-b)^2-\frac{cx}{L}}\right] \tag{4.30}$$

$$(V_{GS} - V_T) - V(x) = (V_{GS} - V_T)\left[b - \sqrt{(1-b)^2 - \frac{cx}{L}} \right] \tag{4.31}$$

where

$$c = \frac{E_c L}{E_c L + (V_{GS} - V_T)} \tag{4.32}$$

$$b = \frac{(V_{GS} - V_T)}{2(E_c L + (V_{GS} - V_T))} = \frac{(1-c)}{2} \tag{4.33}$$

By integrating over the whole length of the channel,

$$I_D L = \mu_o C_o W((V_{GS} - V_T)^2 - \frac{(V_{GS} - V_T)^2}{2}) - \frac{I_D (V_{GS} - V_T)^2}{E_c} \tag{4.34}$$

which can be solved for I_D ,

$$I_D = \mu_o C_o \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2} \left(\frac{E_c L}{E_c L + (V_{GS} - V_T)}\right) \tag{4.35}$$

$$I_D = \left(\mu_o C_o \left(\frac{W}{L}\right) \frac{(V_{GS} - V_T)^2}{2}\right) c \tag{4.36}$$

In other words, hot electron effects have served to reduce the current by a factor "c".

Now

$$\overline{i_n^2} = 4kT\Delta f \mu_o C_o \left(\frac{W}{L}\right)(V_{GS} - V_T) \int_0^1 \frac{dx}{L} \left(1 + \frac{\frac{dV}{dx}}{E_c}\right)^{n-1} \left(b + \sqrt{(1-b)^2 - \frac{cx}{L}}\right) \tag{4.37}$$

If, E_c , the critical field approaches infinity then c=1 and b=0 and the original equations in (4.20) and (4.21) apply and a simple result follows from,

$$\overline{i_n^{\,2}} = 4kT\Delta f\mu_o C_o\left(\frac{W}{L}\right)(V_{GS}-V_T)\int_0^1\left[\left(1+\frac{\frac{dV}{dy}}{E_c}\right)^{n-1}\left(b+\sqrt{(1-b)^2-cy}\right)\right]dy \qquad (4.38)$$

which results in $\Gamma=2/3$.

Making a change of variable in the equation with hot electron effects,

$$y=\frac{x}{L} \quad \text{and} \quad \frac{dV}{dx}=\left(\frac{1}{L}\right)\left(\frac{dV}{dy}\right) \qquad (4.39)$$

$$\overline{i_n^{\,2}} = 4kT\Delta f\mu_o C_o\left(\frac{W}{L}\right)(V_{GS}-V_T)\int_0^1\left[\left(1+\frac{\frac{dV}{dy}}{E_c}\right)^{n-1}\left(b+\sqrt{(1-b)^2-cy}\right)\right]dy \qquad (4.40)$$

$$V(y)=(V_{GS}-V_T)\left(b+\sqrt{(1-b)^2-cy}\right) \qquad (4.41)$$

The following definitions are used which are consistent with the common usage in the literature,

$$g_{max}\Gamma=\gamma g_{do} \qquad (4.42)$$

$$\Gamma=\gamma\frac{g_{do}}{g_{max}} \qquad (4.43)$$

$$g_{do}=\mu_0 C_o\left(\frac{W}{L}\right)(V_{GS}-V_T) \qquad (4.44)$$

$$g_{max}=\frac{\partial I_{DS}}{\partial V_{GS}} \qquad (4.45)$$

then $$g_{max}=\mu_o C_o\left(\frac{W}{L}\right)(V_{GS}-V_T)c[c+b] \qquad (4.46)$$

and $$g_{max}=g_{do}c[c+b] \qquad (4.47)$$

The result with hot electron effects is then,

$$\overline{i_n^{\,2}} = 4kT\Delta f g_{max}\Gamma \tag{4.48}$$

where $$\Gamma = \frac{\int_0^1 \left[\left(b+\sqrt{(1-b)^2-cy}\right)\left(1+\frac{b}{\sqrt{(1-b)^2-cy}}\right)^{n-1}\right]dy}{c(c+b)} \tag{4.49}$$

These equations are then used as an empirical fit to describe a JFET or MESFETs. For a JFET the derivation is similar but the algebra is much more complicated.

4.3 Noise Measurement

Integrating the depletion mode MESFETs or DFET together with the transimpedance amplifier has the advantage of reducing the parasitic capacitance and inductance as compared to using discrete individual components as discussed in previous work on noise measurements [35-36]. This high performance transimpedance amplifier's bandwidth is determined by driving the 2KΩ resistor over a broad band of frequencies with the DFET floating. The experimental gain is found to satisfy the design specifications of 100KHz to 500MHz. The TIA output noise as measured from the spectrum analyzer is flat above 50MHz. Thus, the transimpedance amplifier has a flat gain characteristics for frequencies from 100KHz to 500 MHz as shown in Fig. 3.7 of the previous chapter. The die photo of the TIA with integrated DFET is shown in Fig. 4.2.

The noise measurement setup is shown in Fig. 4.3. All the DC power supply leads are properly bypassed to ground to minimize any noise pickup by measurement

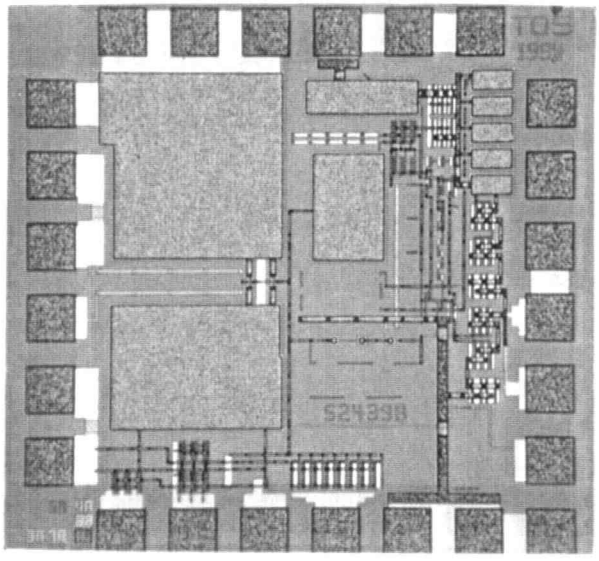


Figure 4.2 Die photo of L = 1μm transimpedance amplifier with integrated depletion mode MESFETs or DFET

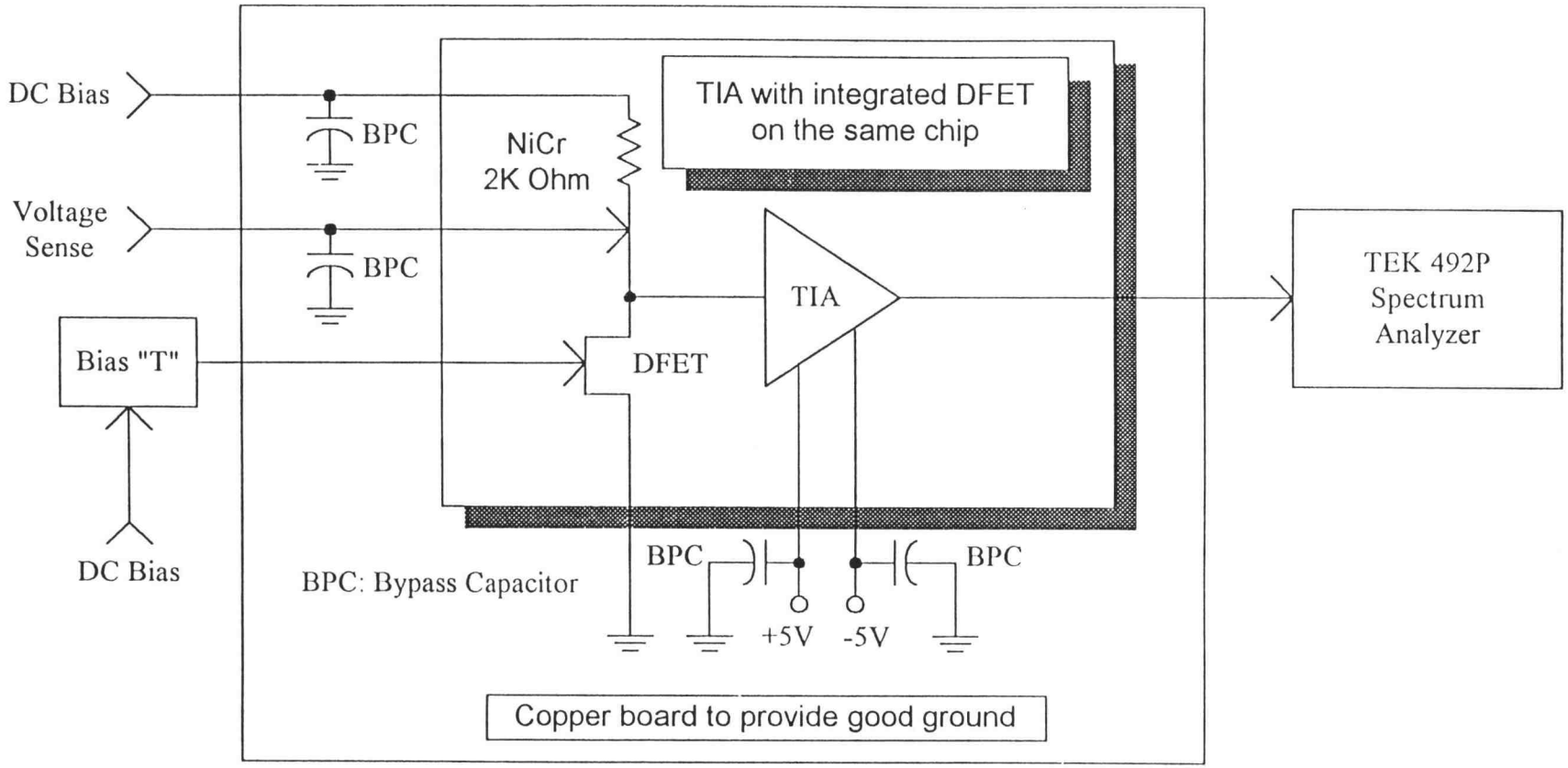


Figure 4.3 Noise Measurement Test Setup

instruments. In addition, the chip is mounted on a copper board with all unused leads, bypass capacitors and the circuit design ground sharing the same copper board ground. This technique greatly suppresses any spurious noise pick up from the environment and is conducive to high frequency measurements of up to 1GHz. In order to have a more accurate representation of Γ, we have included all parasitics and loading resistance effects of the FET. After considering all parasitics, the gate resistance (R_g), source (R_s), and the load resistance (R_L) at the drain of the DFET and after some simple algebraic manipulation, a more complicated formula for the noise spectral density of the FET is obtained and given in equation (4.50).

From this equation a measured value of Γ can be computed.

$$\frac{\overline{i_d^2}}{\Delta f} \approx \frac{4kTg_m\Gamma}{\left(1+g_mR_s\right)^2}\left[1+\frac{g_m\left(R_s+R_g\right)}{\Gamma}+\frac{\left(1+g_mR_s\right)^2}{\Gamma g_mR_L}\right] \tag{4.50}$$

Fig. 4.4 shows the measurement setup using the HP8503 S-parameter test system to measure the overall gain of the system for different bias conditions. The overall gain of the system from the gate of the DFET to the output is designed to be in the range of 10dB to 40dB, depending on the bias condition of the DFET. As an example, the overall gain from the gate of the DFET is determined to be 34.9dB or 55.6V/V with the DFET biased at $V_{GS} = 0V$ and $V_{DS} = 2.5V$. Thus, V_n, the root mean square noise voltage referred back to the gate of the DFET can be obtained by dividing the normalized measured noise by the gain with the system noise of the DFET in the "off" mode taken into consideration.

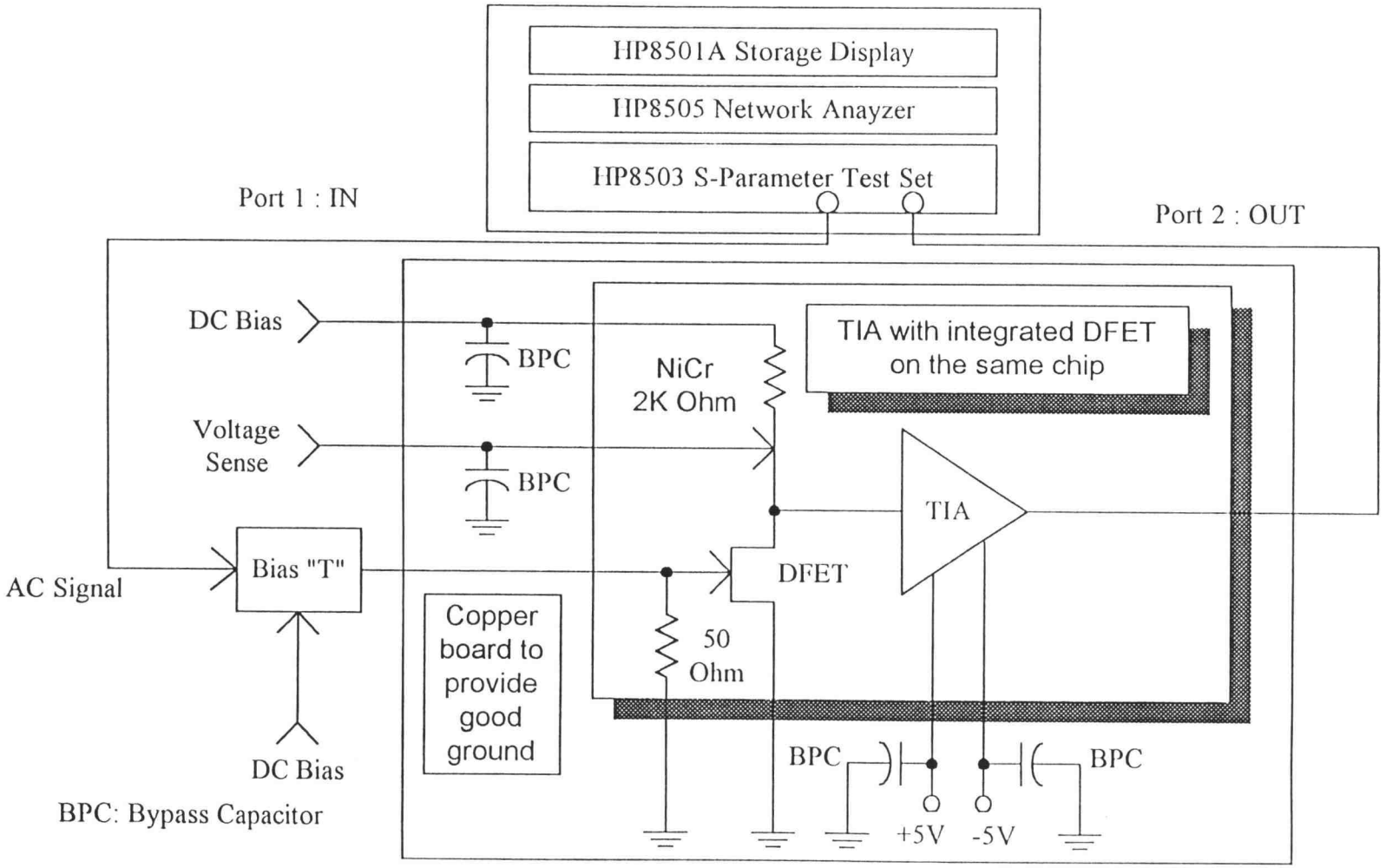


Figure 4.4 Test setup to measure the overall gain of the system with different DFET's bias conditions

The noise is measured using a spectrum analyzer with a DC block at the output prior to being connected to the spectrum analyzer. The spectrum analyzer will measure the system noise when the DFET is in the off mode with $V_{GS} = -2V$ and $V_{DS} = 0V$. The square root of the difference of the squares of the measured RMS noise voltages with the FET in the "on" and "off" conditions gives the total channel noise of the depletion mode FET. Fig. 4.5 and Fig. 4.6 show the output noise spectrum of the DFET biased at the above "on" and "off" conditions respectively. The root mean square noise voltage referred back to the gate can be measured by dividing by the overall gain of the system. The channel noise current, $\sqrt{\frac{\overline{i_d^2}}{\Delta f}}$, can then be calculated by multiplying the noise voltage at the gate, V_n, by the external G_m of the DFET. The computation of the external G_m takes into consideration the parasitic source resistance as follows,

$$G_m \cong \frac{g_m}{1+g_m R_S} \tag{4.51}$$

With the application of equation (4.50), the appropriate value of Γ can be obtained for various bias conditions. Using this method we can experimentally determine the different values of Γ for different bias conditions along the I-V characteristics curves. Fig. 4.7 and Fig. 4.8 shows the measured Γ values for a short gate length FET of 1 μm and a long gate length FET of 8 μm, respectively. These characteristic I-V curves with the channel noise coefficient superimposed is similar to the work done by Abidi for MOSFET's [38]. Care however must be exercised in interpreting the results of Abidi

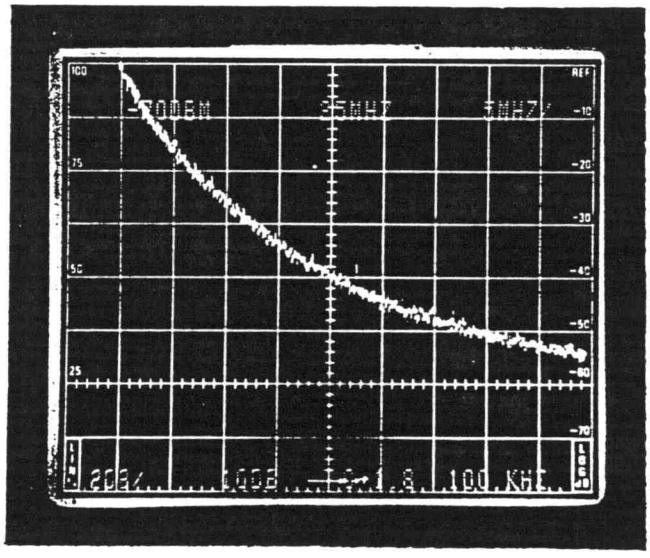


Figure 4.5 Noise Spectrum of DFET "on" condition; Vgs=0V and Vds=2.5V

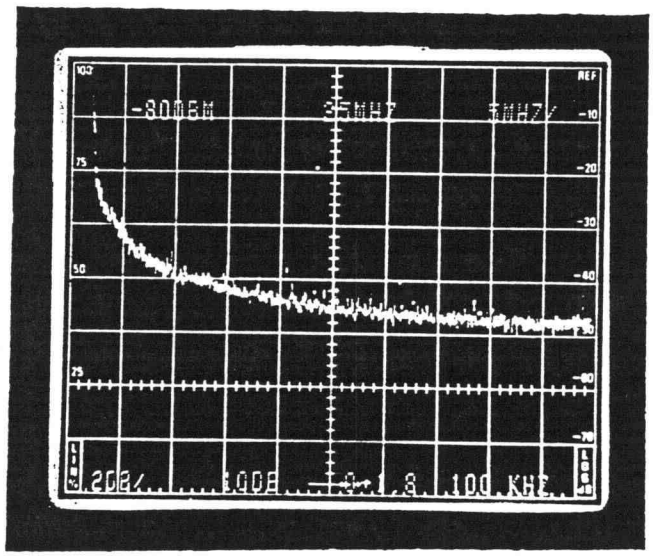


Figure 4.6 Noise Spectrum of DFET "off" condition; Vgs=-2V and Vds=0V

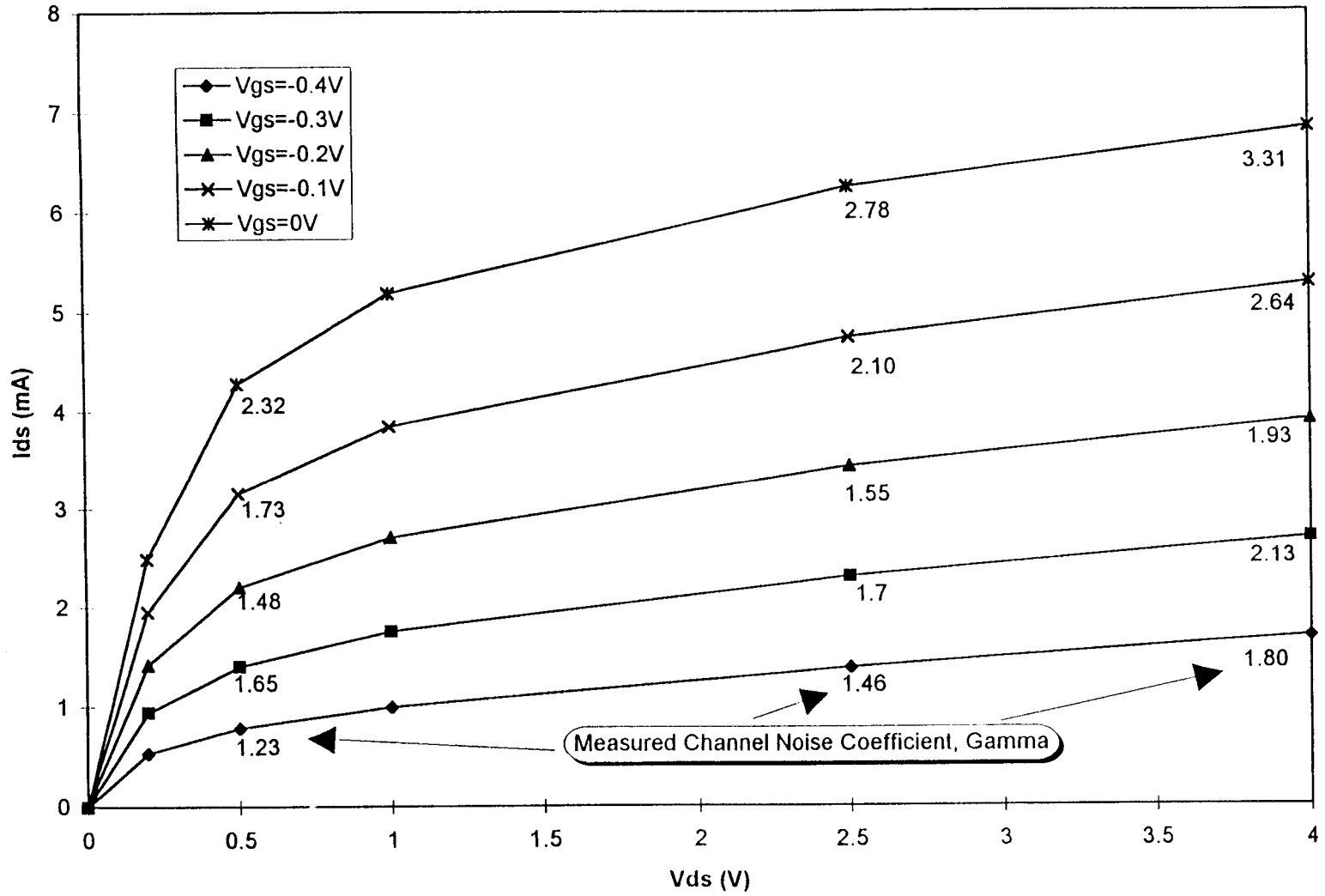


Figure 4.7 Measured Channel Noise Coefficient, Γ, for different bias condition along the IV curve of a short gate length DFET with dimensions W = 40μm, L = 1μm and number gates, NG=3

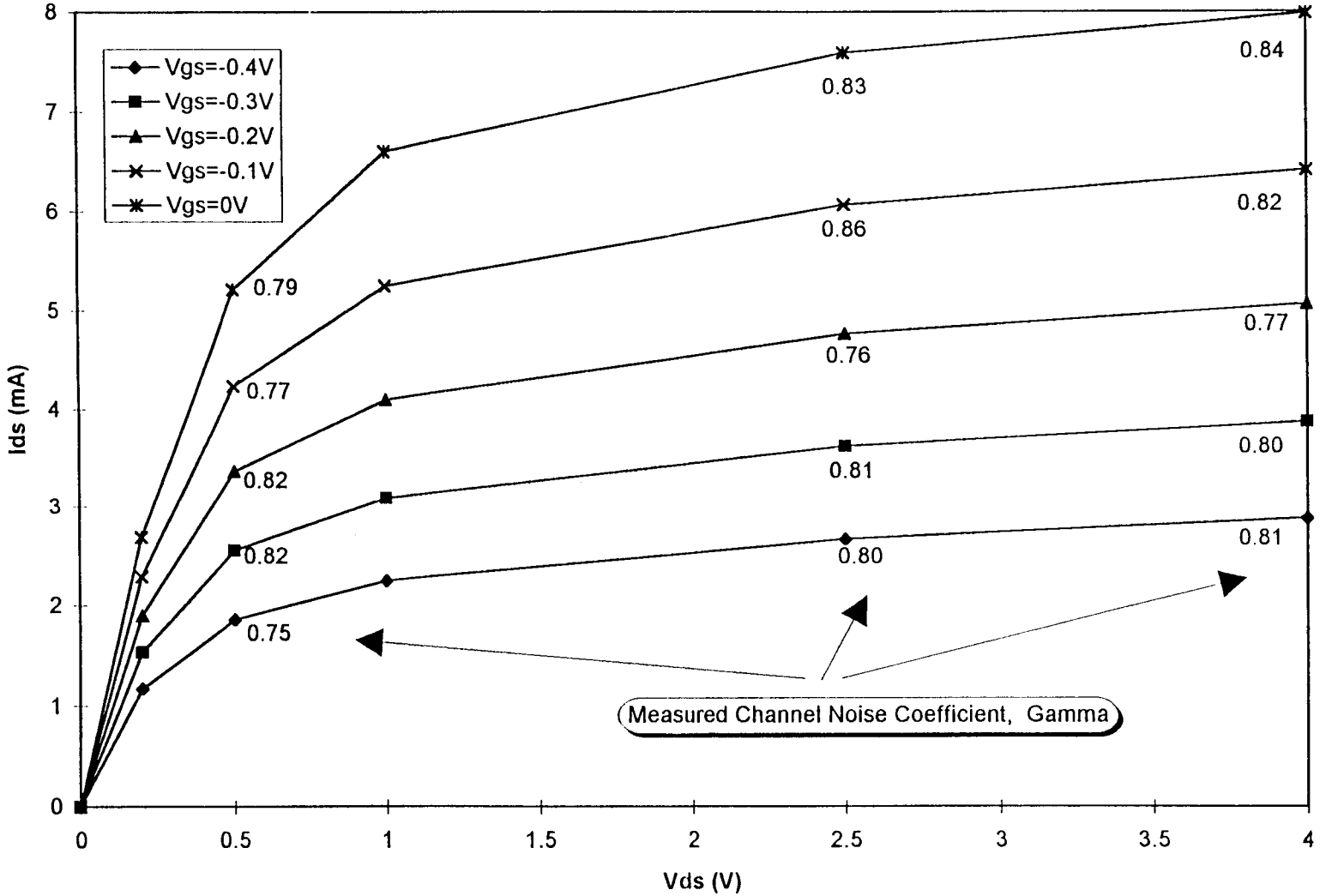


Figure 4.8 Measured Channel Noise Coefficient, Γ, for different bias condition along the IV curve of a long gate length DFET with dimensions W = 50μm, L = 8μm and number gates, NG=8

[38], because the channel noise coefficient has been given in terms of the drain conductance rather than transconductance as is normally the case in circuit simulations. It will be shown later that we can use the ratio of the drain current for a long gate FET and short gate FET to predict Γ values for different bias condition.

4.4 Application of the Model to Experimental Data on L=1μm Technology

4.4.1 Steps in Determination of Γ

In order to fit the experimentally determined Γ noise data, the following steps are used;

(i) Fit the I-V curves to the square law FET characteristics given by the previous equations.

(ii) V_T is found by plotting $\sqrt{I_{DS}}$ versus V_{GS}, as shown in Fig. 4.9. For the short gate (Lg= 1μm) device, then $V_t = -0.8V$.

(iii) The reduction in drain saturation current due to hot electron effects is described by a factor "c"; consider both the long gate length device and short gate length with $V_{GS} = 0V$; and $V_{DS} = 1.0V$ which corresponds approximately to the saturation condition; from the values of the current we can find the factor "c" which reduces the current in the short gate length device. For the long gate length device, Lg=8μm , the saturation current is $130mA/mm$ for $\frac{W}{L} = 1$ while it is $44mA/mm$ for $\frac{W}{L} = 1$ for the short gate length device yielding c=0.4 approximately.

This value of "c" is then used to determine the critical electric field, E_C;

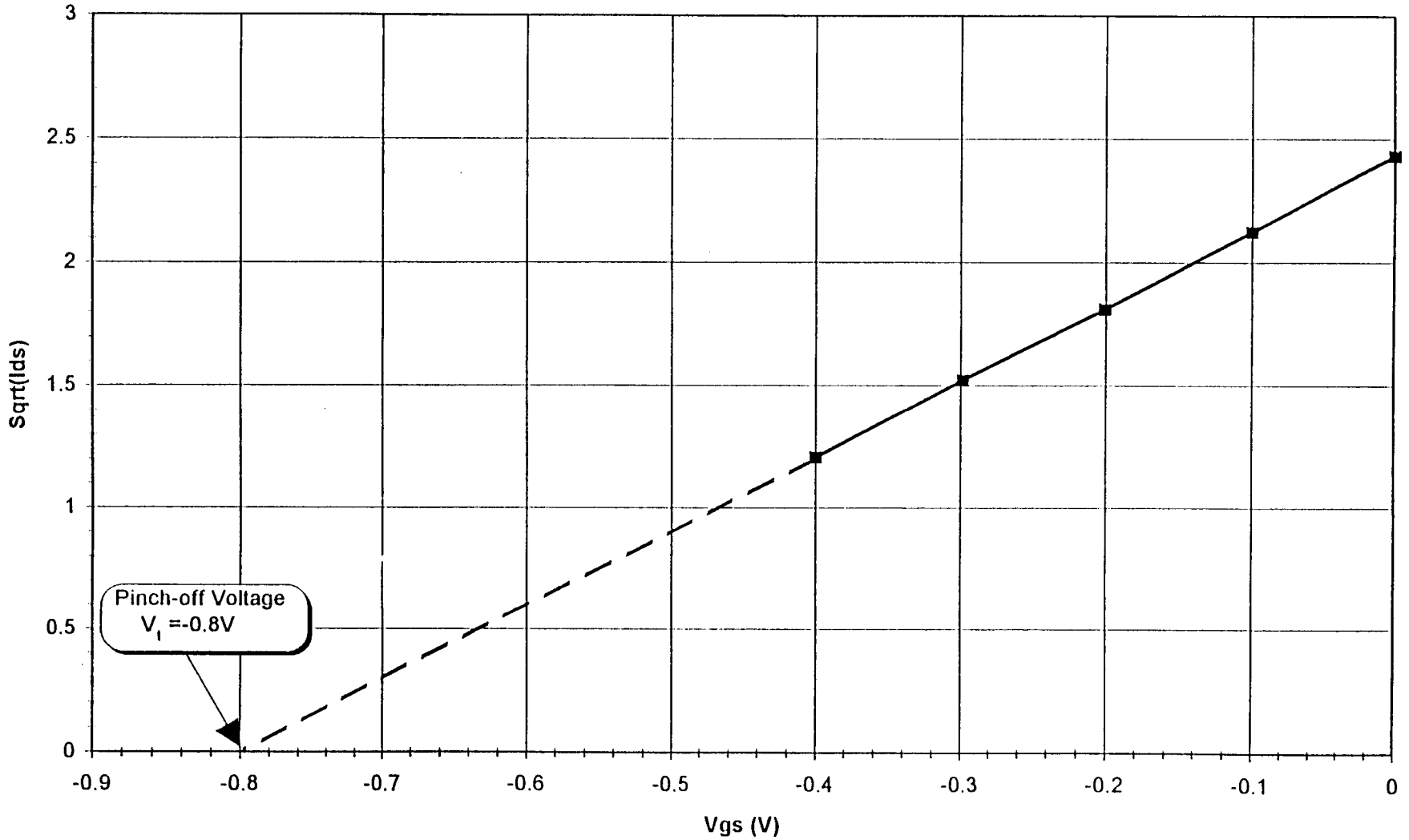


Figure 4.9 Pinch-off voltage determination for L = 1μm

$$c = \frac{E_c L}{E_c L + (V_{GS} - V_T)} \tag{4.52}$$

$$E_c = 4X10^3 V/cm,\ L = 1\mu m \tag{4.53}$$

For other gate voltages at saturation we can then use the above formula to determine a new value of "c". This then gives all the values of Γ at saturation and these can be plotted on the characteristic curves.

For drain voltage above the saturation point, $V_{DS} > (V_{DS})_{Saturated}$, the channel length is shortened due to the excess drain voltage. The drain current increases since

$$I_{DS} = (const)(\frac{1}{L_{mod}})c_{mod} \tag{4.54}$$

and $(\frac{1}{L_{mod}})c_{mod}$ increases as L_{mod} becomes smaller. The reduction in L_{mod} with the same potential drop along the channel will cause increases in hot electron effects due to a higher electric field. The value of c_{mod} is now a function of L_{mod}, which becomes smaller when L_{mod} is reduced and the net result is a larger value of Γ. From the increase in I_{DS}, c_{mod} can be determined, and we can also calculate the value of Γ.

4.4.2 Examples of Computation of Γ for Various Bias Condition for Short Gate Length FET L=1μm

From equation (4.48), $\Gamma = \dfrac{\int_0^1 \left[\left(b + \sqrt{(1-b)^2 - cy}\right)\left(1 + \dfrac{b}{\sqrt{(1-b)^2 - cy}}\right)^{n-1}\right] dy}{c(c+b)}$ and selecting n=1, the above equation reduces to,

$$\Gamma = \frac{\int_0^1 \left(b + \sqrt{(1-b)^2 - cy}\right) dy}{c(c+b)} \tag{4.52}$$

and it should be noted that b is related to c by the following equation,

$$b = \frac{1-c}{2} \tag{4.53}$$

As a check of the above formula, we take the ideal situation in which there are no hot electron effects. In this case, c=1, and the correponding value of Γ is 0.667. A numerical integration is performed and the values of Γ tabulated for different values of "c".

At bias condition (I) for which $V_{GS} = 0V$ and $V_{DS} = 1.0V$.

For the short gate length MESFETs from Fig. 4.7,

$$I_{DS}\left(\frac{W}{L} = \frac{120}{1} = 120\right) = 5.1mA \tag{4.54}$$

For the long gate length MESFETs from Fig. 4.8,

$$I_{DS}\left(\frac{W}{L} = \frac{400}{8} = 50\right) = 6.6mA \tag{4.55}$$

$$c = \left(\frac{5.1}{6.6}\right)\left(\frac{50}{120}\right) = 0.32 \tag{4.56}$$

Applying equation (4.57) and (4.58), Γ =3.

From equation (4.54), $c = \frac{E_c L}{E_c L + (V_{GS} - V_T)}$. We can compute the value of the critical electric field, E_c, for a short gate length MESFETs for which L=1μm by the following,

$$0.32 = \frac{E_c L}{E_c L + 0.8} \tag{4.57}$$

$$0.68 E_c L = 0.256 \tag{4.58}$$

$$E_c = 4X10^3 V/cm \tag{4.59}$$

With this value of $E_c = 4X10^3 V/cm$, we can next calculate another bias condition near V_{dsat} or the saturation point. The bias condition (II) chosen is $V_{GS} = -0.4V$ and $V_{DS} = 0.25V$.

$$c = \frac{E_c L}{E_c L + (V_{GS} - V_T)} \tag{4.60}$$

$$c = \frac{0.4}{0.4 + 0.4} = 0.5 \tag{4.61}$$

Applying equation (4.56) and (4.57), Γ= 1.5.

Next we consider $V_{GS} = -0.4V$ and $V_{DS} = 2.5V$ for bias condition (III), where channel length modulation has an impact on the drain current. From bias condition (II) in which $V_{GS} = -0.4V$ and $V_{DS} = 0.25V$, the drain current for the 1μm short gate length MESFETs is $I_{DS} = 0.53mA$. From equation (4.55), $I_{DS} = (const)(\frac{c}{L})$, we can calculate the $(const) = 1.06X10^{-3}$. At $V_{GS} = -0.4V$ and $V_{DS} = 2.5V$, the drain current is 1.38mA. We can then move to compute $E_c L_{mod}$ which incorporate the channel length modulation effect at high drain voltage condition. Applying equation (4.55),

$$I_{DS} = \frac{(const)E_C}{E_C L_{mod} + (V_{GS} - V_T)} \tag{4.62}$$

$$E_c L_{mod} = 0.33 \tag{4.63}$$

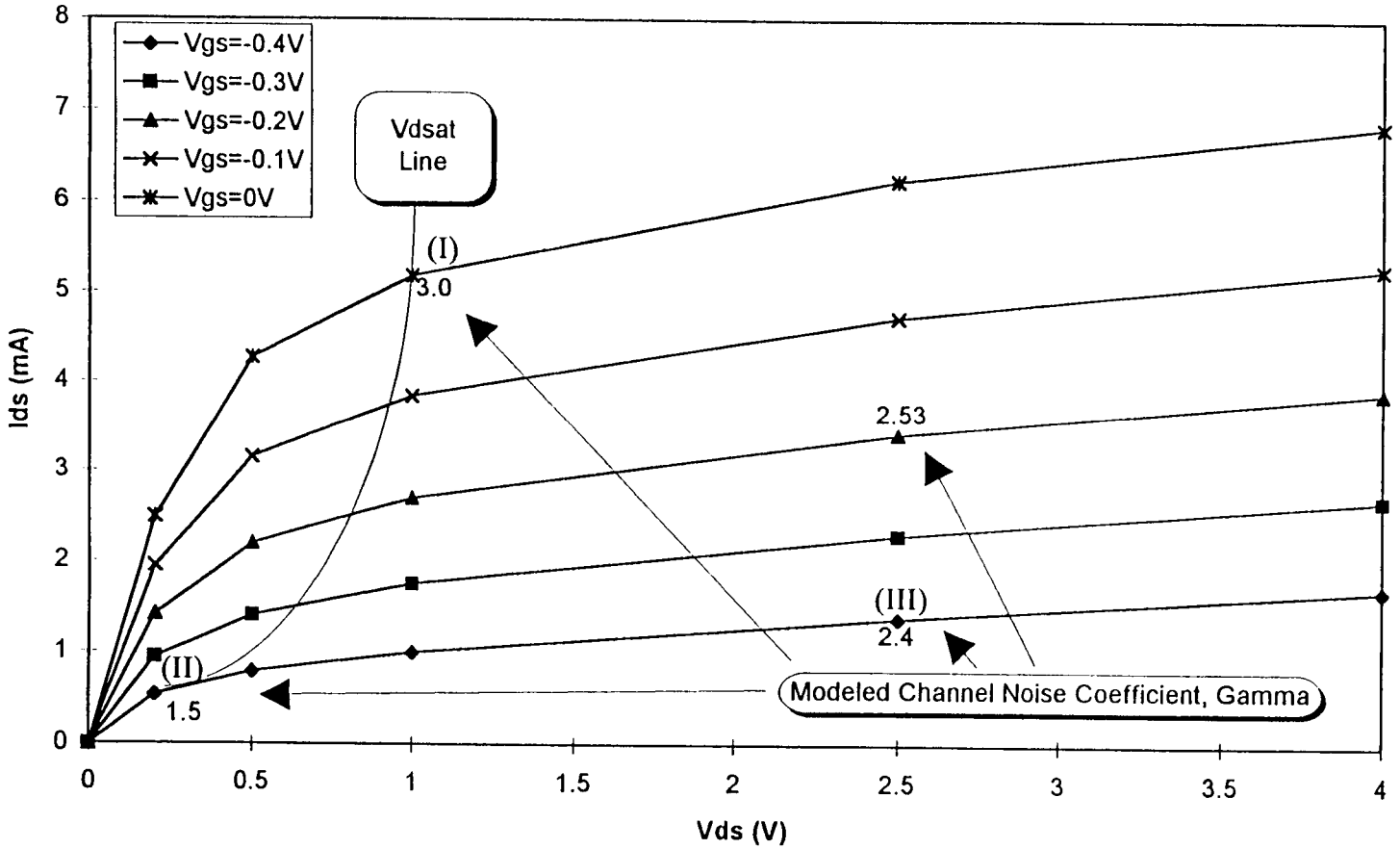


Figure 4.10 Modeled Channel Noise Coefficient, Γ, for different bias conditions (I), (II), (III) along the IV curve of a short gate length DFET with dimensions W = 40μm, L = 1μm and number gates, NG=3

Applying equation (4.53), the modified value of C_{mod} which take into consideration the channel length modulation effect is,

$$C_{mod} = \frac{0.33}{0.33+0.4} = 0.45 \tag{4.64}$$

which gives a corresponding value of Γ=2.4. Fig. 4.10 shows the modeled channel noise coefficient for the above three bias condition.

4.5 Summary

This thermal noise models based on this new theory can be implemented into a SPICE simulator or derivatives of Berkeley's SPICE. For instance, PSPICE models currently use the ideal value of noise coefficient, Γ, of 2/3 which needs to be corrected if noise performance is to be modeled accurately [39]. Work on the thermal noise modeling of MOSFET's has progressed continuously [41-42]. More recent work on thermal noise modeling includes that of Wang et al. [43] which specifically addresses the issue of thermal noise modeling in analog integrated circuits. To the best of our knowledge, our work represents the first time MESFETs devices have been integrated together with a high performance transimpedance amplifier with the sole purpose of updating and addressing the issue of channel noise coefficients of a commercially available GaAs MESFETs process.

The simple model presented here gives a good representation of the noise coefficients at saturation in short gate length MESFETs devices. These values are considerably different than the simple 2/3 value currently used in circuit simulations. It is

clear that this type of model can probably also be used to describe MOSFET's [38], if some modifications and changes in the definitions are made.

CHANNEL NOISE COEFFICIENT OF SUB-MICRON MESFETs

5.1 Introduction

In this chapter, the thermal noise model derived in chapter 4 is applied to 0.6μm MESFETs technology [35]. The transimpedance amplifier is a low noise, high gain single stage cascode amplifier. The transimpedance amplifier used is similar to the previous design in L=1μm except that the capacitor Cneg is removed to prevent low frequency peaking in this technology as shown in Fig. 5.1. Other changes are minor with proper modication of device widths to accomodate proper DC biasing. This high performance transimpedance amplifier uses a similar amplification methodology for the input stage as an earlier low noise transimpedance amplifier with automatic gain control capability [32]. A die photo of the TIA with the integrated DFETs is shown in Fig. 5.2. The DFET's under test have gate lengths of $0.6\,\mu m$ and $8\,\mu m$. Both FETs, which are bonded out separately in different die, share a common gate and drain. Fig. 5.3 shows the frequency response of the TIA which has an upper corner frequency of 1.2GHz.

5.2 Application of the Model to Experimental Data on L=0.6μm Technology

The noise measurement technique used here is the same as in chapter 4. From Fig. 5.4 at 80MHz, which is well beyond the 1/f corner frequency of the DFET, the overall gain from the gate of the DFET to the output is measured. The DFET biased at $V_{GS} = -0.1V$ and $V_{DS} = 2.5V$ and is in the "on" mode and the gain is determined to be 29.8dB or 31V/V. The noise is measured using a spectrum analyzer with a DC block at

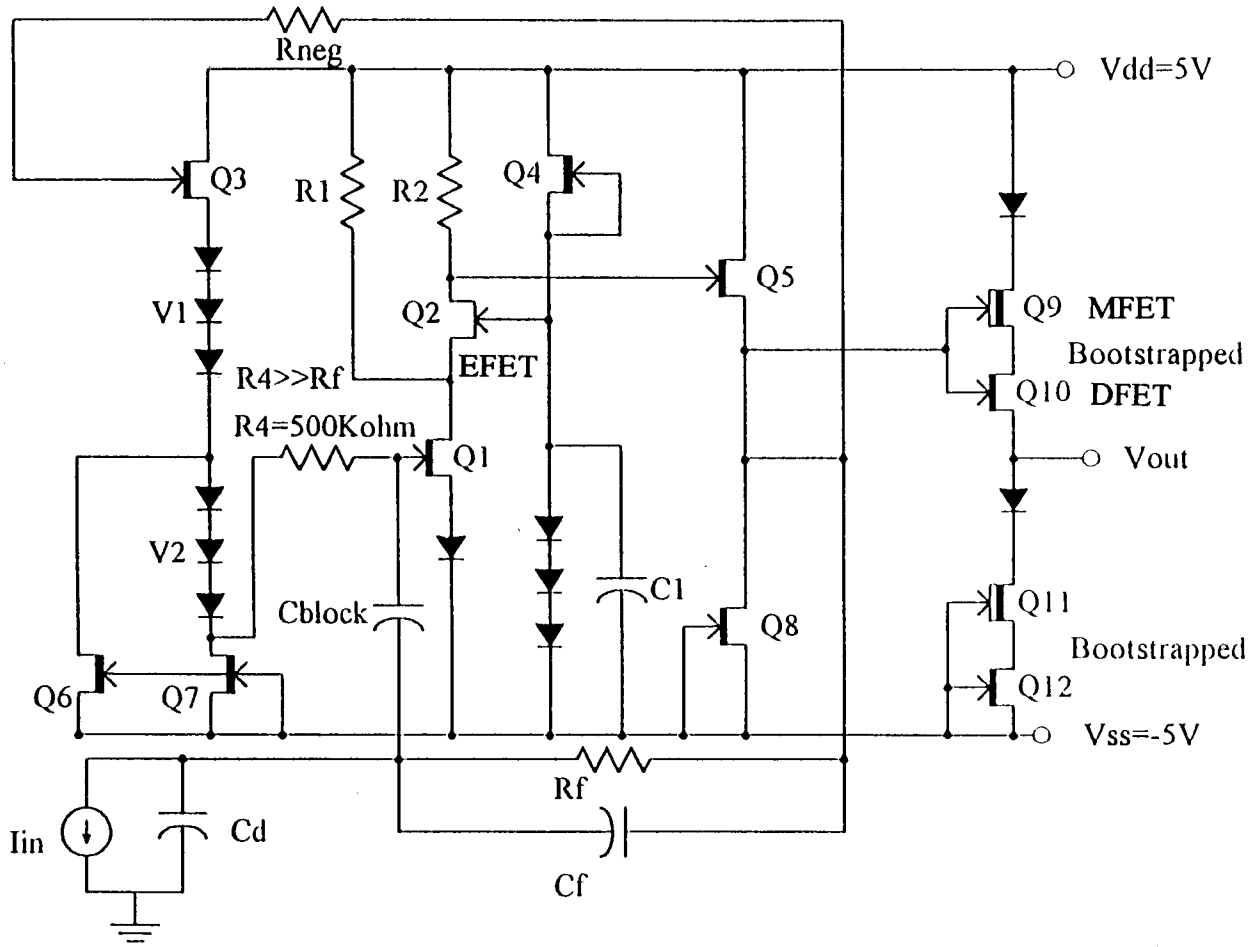


Figure 5.1 Simplified Schematic Diagram of L = 0.6μm transimpedance amplifier, TIA

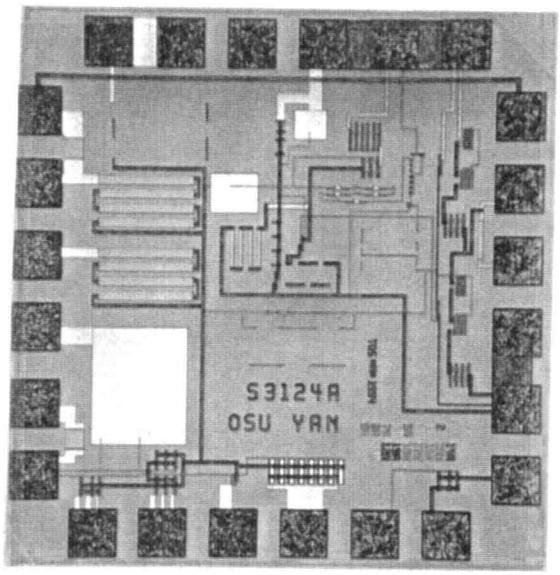


Figure 5.2 Die photo of L = 0.6μm transimpedance amplifier with integrated depletion mode MESFETs or DFET

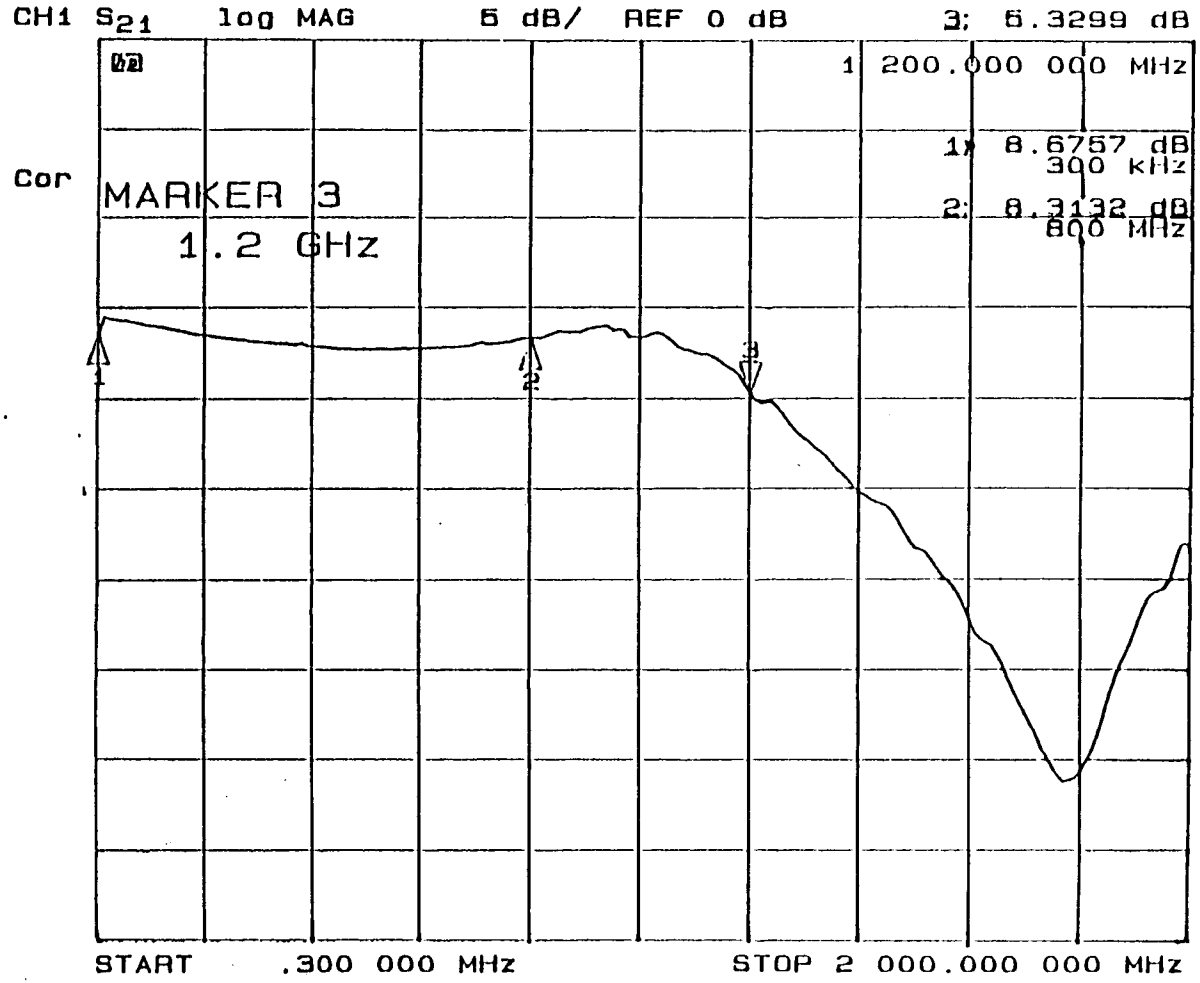


Figure 5.3 Forward transmission coefficient, S_{21} of tranimpedance amplifer

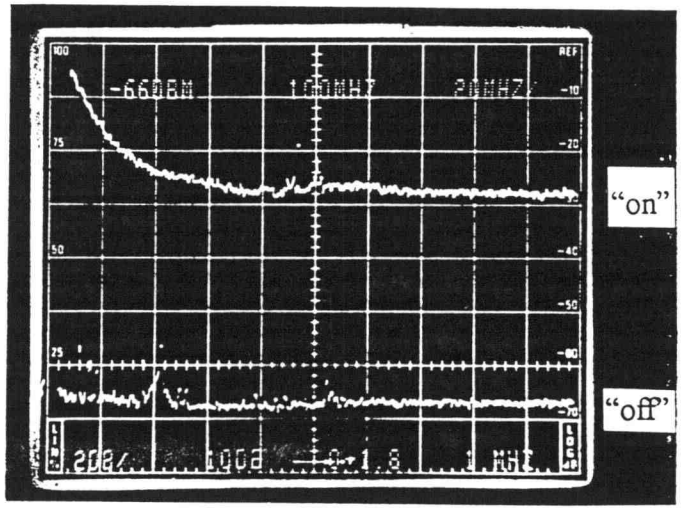


Figure 5.4 Noise Spectrum of DFET "on" and "off" conditions

the output prior to being connected to the spectrum analyzer. The spectrum analyzer will measure the system noise when the DFET is in the off mode with $V_{GS} = -2V$ and $V_{DS} = 0V$. The increase in the noise level in the "on" mode is due to the additional channel noise of the DFET for that particular biasing point. The square root of the difference of the squares of the measured RMS noise voltages with the FET in the "on" and "off" conditions gives the total channel noise of the depletion mode FET. The root mean square noise voltage referred back to the gate can be measured by dividing by the overall gain of the system. With the application of equation (4.51), the appropriate value of Γ can be obtained for various bias conditions as shown in Fig. 5.5.

Also, a V_T=-0.92V is found by plotting $\sqrt{I_{DS}}$ versus V_{GS}.

For the short gate length MESFETs L=0.6μm,

$$I_{DS}\left(\frac{W}{L} = \frac{120}{0.6} = 200\right) = 8.1mA \tag{5.1}$$

For the long gate length MESFETs L=8μm,

$$I_{DS}\left(\frac{W}{L} = \frac{400}{8} = 50\right) = 3.88mA \tag{5.2}$$

$$c = \left(\frac{8.1}{3.88}\right)\left(\frac{50}{200}\right) = 0.52 \tag{5.3}$$

Applying equation (4.57) and (4.58), Γ =1.98.

From equation (4.54), $c = \dfrac{E_c L}{E_c L + (V_{GS} - V_T)}$, the value of the critical electric field, E_c, for a short gate length MESFETs for which L=0.6μm can be computed by the following,

$$E_c = 1.66X10^3\,V/cm \tag{5.4}$$

With this value of $E_c = 4X10^3\,V/cm$, we can next calculate another bias condition near V_{dsat} or the saturation point. The bias condition (II) chosen is $V_{GS} = -0.4V$ and $V_{DS} = 0.25V$.

$$c = \frac{E_c L}{E_c L + (V_{GS} - V_T)} = 0.657 \tag{5.5}$$

Applying equation (4.57) and (4.58), Γ= 1.36.

Next we consider $V_{GS} = -0.4V$ and $V_{DS} = 2.5V$ for bias condition (III), where channel length modulation has an impact on the drain current. From bias condition (I) in which $V_{GS} = -0.4V$ and $V_{DS} = 0.25V$, the drain current for the 1μm short gate length MESFETs is $I_{DS} = 1.52mA$. From equation (4.56), $I_{DS} = (const)(\frac{c}{L})$, we can calculate the $(const) = 1.39X10^{-3}$. At $V_{GS} = -0.4V$ and $V_{DS} = 2.5V$, the drain current is 6.1mA. We can then move to compute $E_c L_{mod}$ which incorporate the channel length modulation effect at high drain voltage condition. Applying equation (4.56),

$$E_c L_{mod} = 0.45 \tag{5.6}$$

Applying equation (4.54), the modified value of C_{mod} which take into consideration the channel length modulation effect is,

$$C_{mod} = \frac{0.45}{0.45 + 0.52} = 0.46 \tag{5.7}$$

which gives a corresponding value of Γ=2.38. Fig. 5.6 show the modeled channel noise coefficient for the above three bias conditions.

5.3 RF Measurement

Fig. 5.7 is the RF measurement test setup. The S-parameters are obtained by measurement of a L=0.6μm and W=300μm DFET with a high frequency probe station. "FetFitter" an optimization program developed at Cascade Microtech is used to extract the lumped parameter values of equivalent circuit in Fig. 5.8. With these extracted values, the unity gain frequency, F_t, can thus be obtained as a function of different bias conditions.

5.4 Figure of Merit for Transimpedance Amplifier

A figure of merit commonly used for transimpedance amplifier designs is $\frac{\Gamma}{F_t}$, which is proportional to the mean square value of the channel noise shown in Fig. 5.9. The optimum biased condition is the point where $\frac{\Gamma}{F_t}$ is minimized.

5.5 Summary

The channel noise coefficient theory developed in Chapter 4 has also been sucessfully implemented in state-of-the-art sub-micron MESFETs technology. The measured channel noise coefficients are larger for all bias condition for this smaller gate length technology. This is consistent with the theory which attributes the increase in hot electron effects due to the channel length reduction which then leads to an increase in the

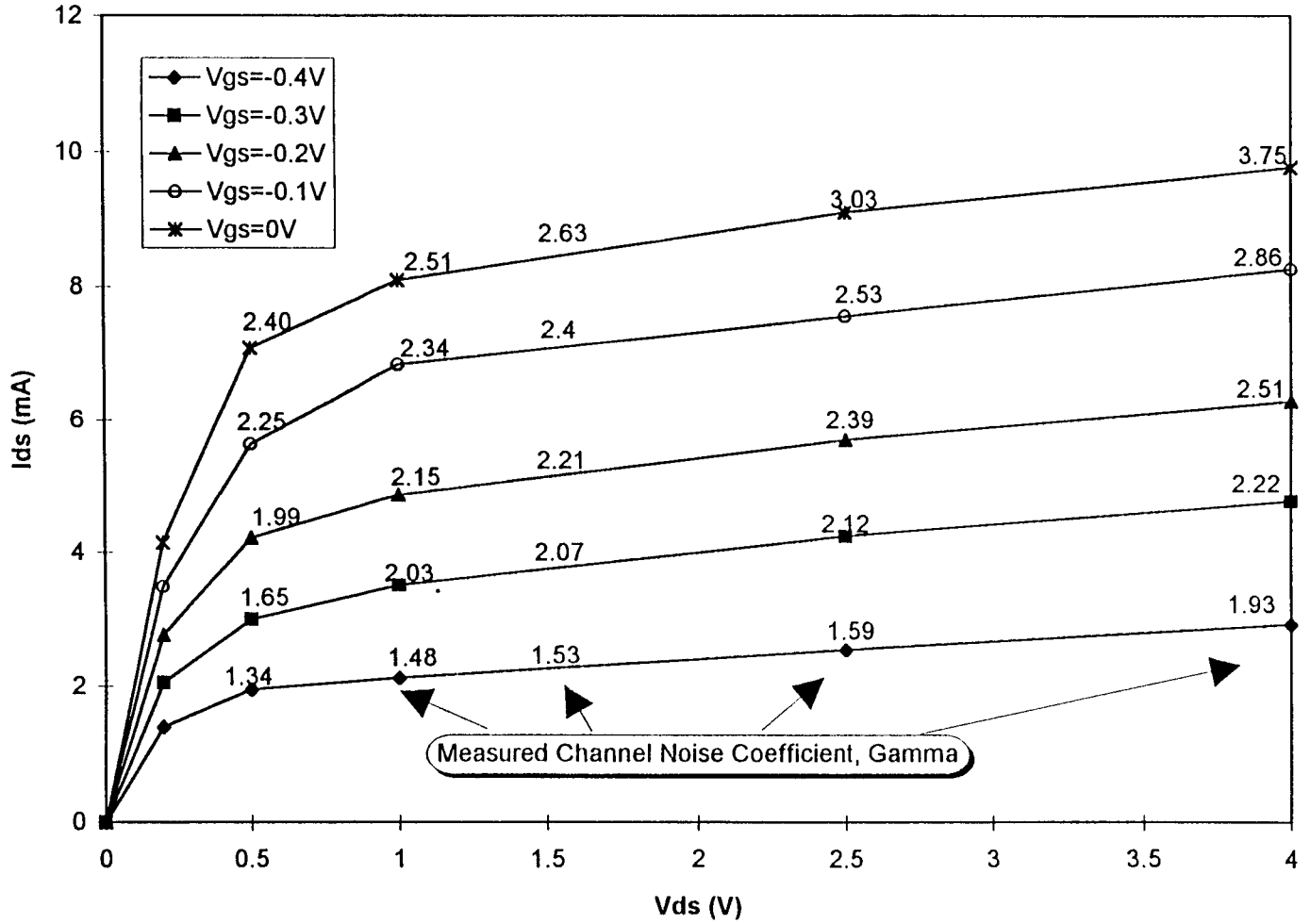


Figure 5.5 Measured Channel Noise Coefficient, Γ, for different bias condition along the IV curve of a short gate length DFET with dimensions W = 40μm, L = 0.6μm and number gates, NG=3

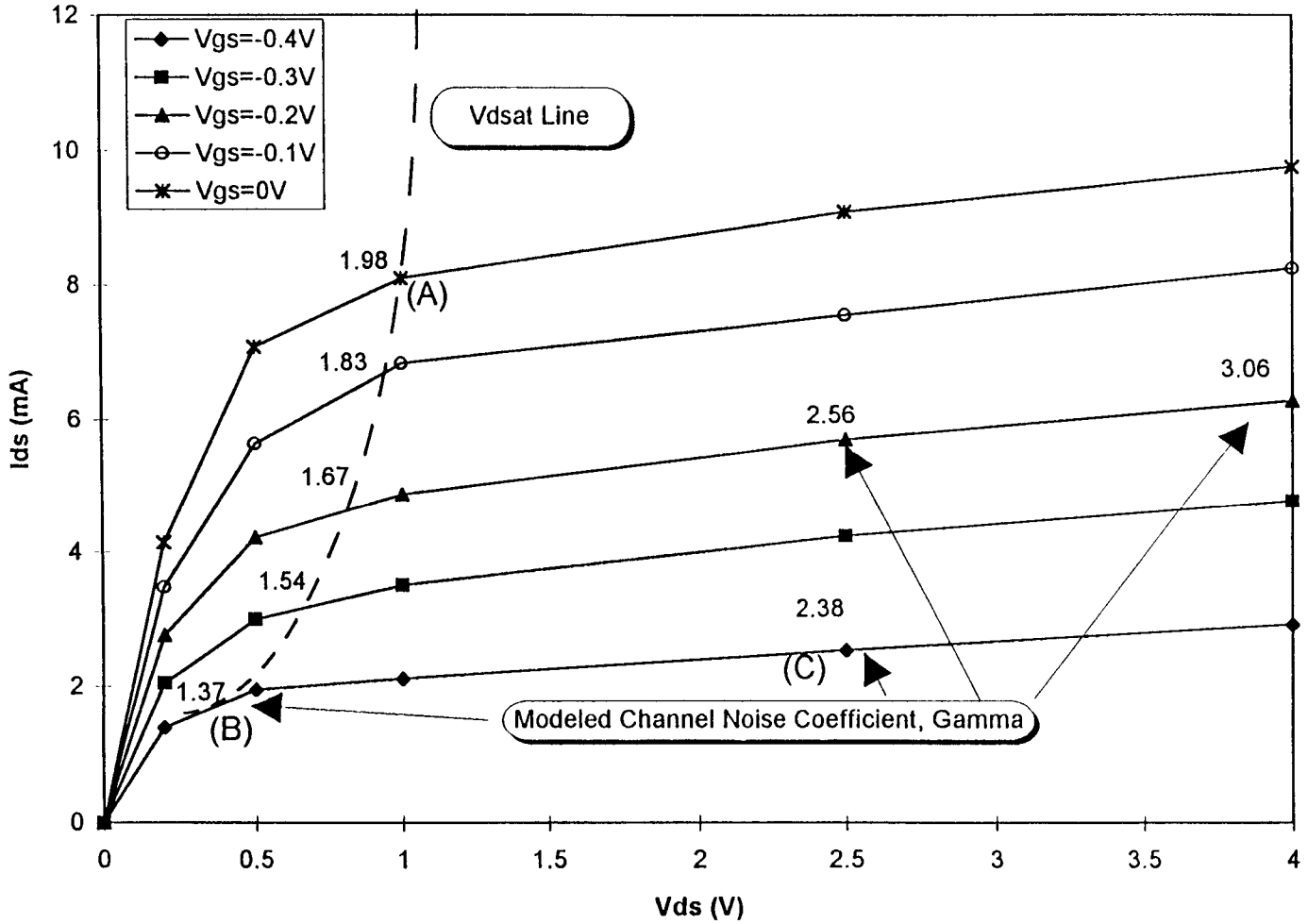


Figure 5.6 Modeled Channel Noise Coefficient, Γ, for different bias conditions (A), (B), (C) along the IV curve of a short gate length DFET with dimensions W = 40μm, L = 0.6μm and number gates, NG=3

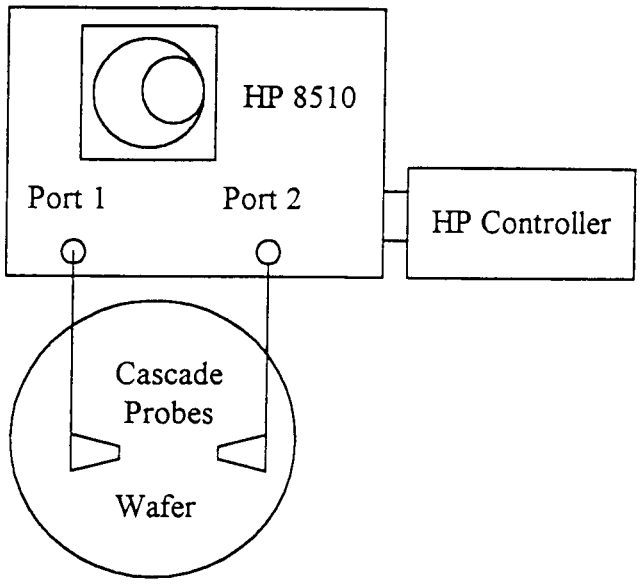


Figure 5.7 RF measurement test setup

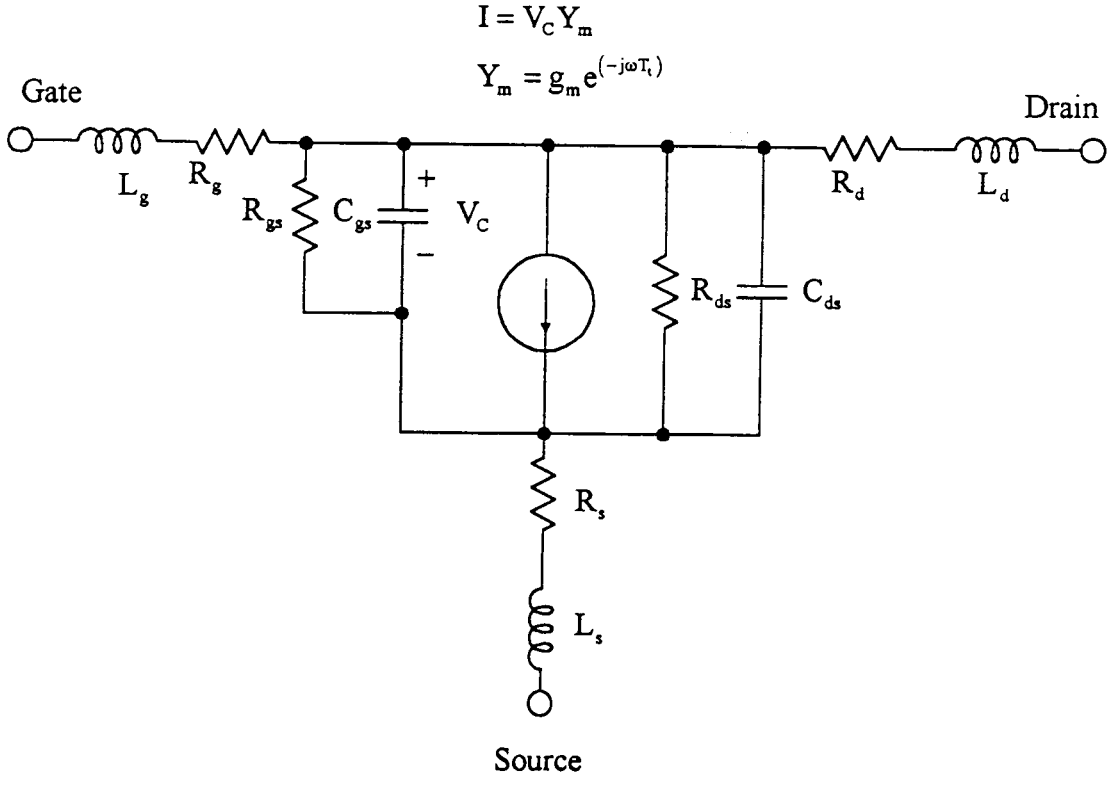


Figure 5.8 Linear equivalent circuit model

predicted channel noise coefficient. In addition, an optimum bias condition occurs at Vgs=0V and with Vds close to the Vdsat condition.

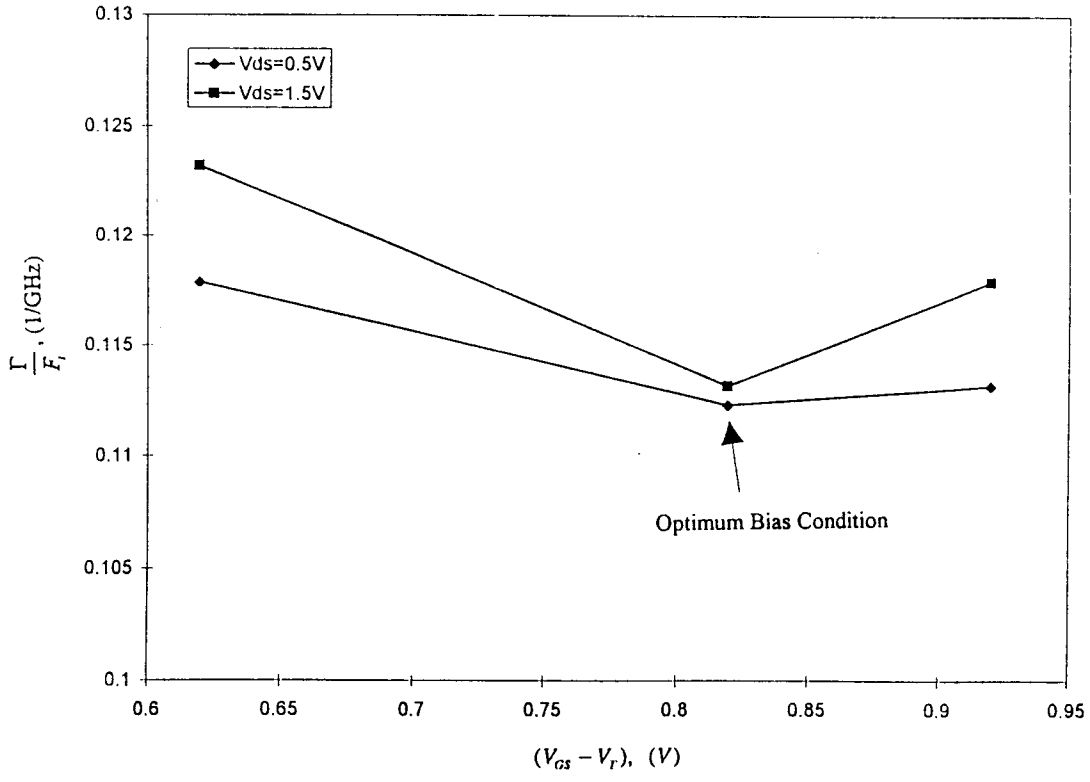


Figure 5.9 Transimpedance amplifier's figure of merit

6. MODEL FOR THE 1/f NOISE MESFETs

6.1 Motivation

A formula for the 1/f noise corner frequency for GaAs MESFETs is developed. The formula is based on a new theory where the 1/f noise is a bulk phenomena with localized high frequency variations and long range low frequency fluctuations in the substrate with the lowest frequency being constrained only by the thickness of the material. The model is based on employing a distributed equivalent circuit technique in evaluating the semi-insulating substrate. The results demonstrate a close match between modeled and measured data [29].

6.2 Introduction

The 1/f noise phenomena associated with devices involving semi-insulating materials, for instance GaAs MESFETs on semi-insulating GaAs, has long been a perplexing problem. No reasonable explanation has ever been given, although there are many different theories.

In earlier reports on the 1/f noise of GaAs MESFETs, Van der Ziel in his papers [44-45] gave an empirical theory of 1/f noise in terms of Hooge's parameters, which is an attempt to come up with a better empirical model to fit experimental data. It should be noted that the Hooge's parameter is not at all constant for a particular type of solid state device. For example, the value Van der Ziel obtained in 1985 [44] varies greatly from that of Tacano [46] in 1991. Another attempt by this group to describe the 1/f noise of GaAs

MESFETs is a paper by Shu et al. [47] which tried to discriminate between number fluctuations and mobility fluctuations resulting in 1/f noise. Hughes et al. [48] attributed this 1/f noise to generation-recombination. The explanations of the sources and the origin of 1/f noise range from quantum noise, generation recombination noise, intervalley scattering, lattice scattering or mobility fluctuations, bulk traps, metal-interface states, backside interface, substrate problems, number fluctuations and temperature fluctuations to surface states. Therefore, the present literature on 1/f noise is elusive. Although a number of mechanisms have been proposed, there is no unified theory that can effectively describe the 1/f noise characteristics of GaAs devices. We propose here a completely new theory which attributes the 1/f noise to the semi-insulating substrate itself.

6.3 Theory

The solution to this problem, 1/f noise in semi-insulating materials has been suggested by the equivalent circuit techniques of C. T. Sah. [1] [2] These equivalent circuit concepts have been able to reproduce a number of very elegant solutions to difficult problems in conduction in semiconductors and frequency response. The generalized equivalent circuit for a semiconductor is shown in Fig. 6.1. The problem of dielectric relaxation of a bulk sample is represented in Fig. 6.2. Here R represents the resistance of the sample, C_k the dielectric capacitance, and the time constant is just the dielectric relaxation time:

$$R = \frac{d}{q\mu n A} \tag{6.1}$$

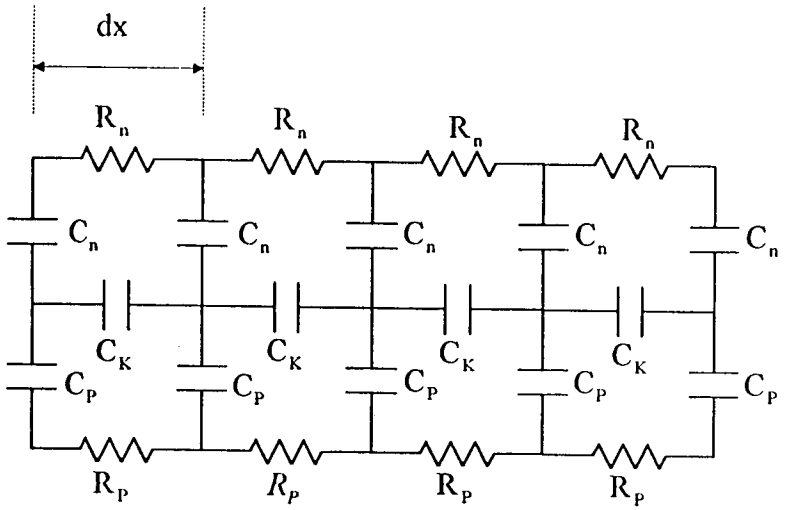


Figure 6.1 Generalized equivalent circuit model without generation-recombination

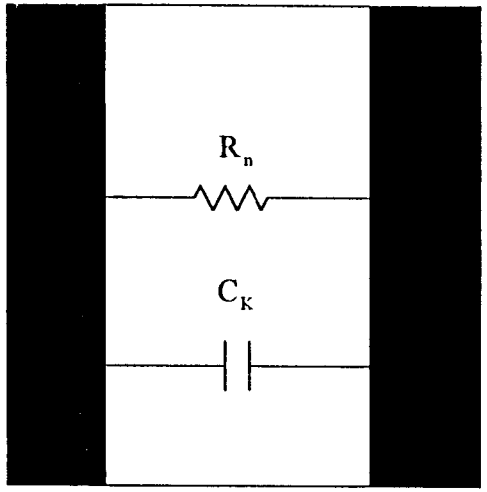


Figure 6.2 Dielectric relexation of a bulk sample

$$C_k = \frac{k_s \varepsilon_o A}{d} \tag{6.2}$$

where all symbols have their usual meanings and the dielectric relaxation time,

$$T_d = RC_k = \frac{k_s \varepsilon_o}{q\mu n} \tag{6.3}$$

At very high frequencies then the sample appears as a dielectric capacitance, usually this radian frequency is extremely high, of the order of $\omega = 10^{12}$ rad./sec. At low frequencies, the sample is resistive. Likewise the equivalent circuit technique shown in Fig. 6.3 yields the Debye capacitance at the edge of a space charge region in a p-n junction or MOS device. The impedance looking into the bulk semiconductor at the edge of the depletion region can be found by transmission line techniques [51-52];

$$Z_o = \left(\frac{Z}{Y}\right)^{\frac{1}{2}} \tag{6.4}$$

$$Z_o = \left(\frac{1}{j\omega C_k j\omega C_n}\right)^{\frac{1}{2}} = \left(\frac{1}{j\omega (C_k C_n)^{\frac{1}{2}}}\right) \tag{6.5}$$

where the dielectric capacitance $C_k = \frac{k_s \varepsilon_o A}{dx}$, and the capacitive effect of the majority carriers $C_n = \left(\frac{q^2}{kT}\right) ndxA$ in each volume element of extent dx. In this case, the propagation constant, γ, is all real and,

$$\gamma dx = (ZY)^{\frac{1}{2}} = \sqrt{\frac{q^2 n}{kTk_s \varepsilon_o}}\ dx \tag{6.6}$$

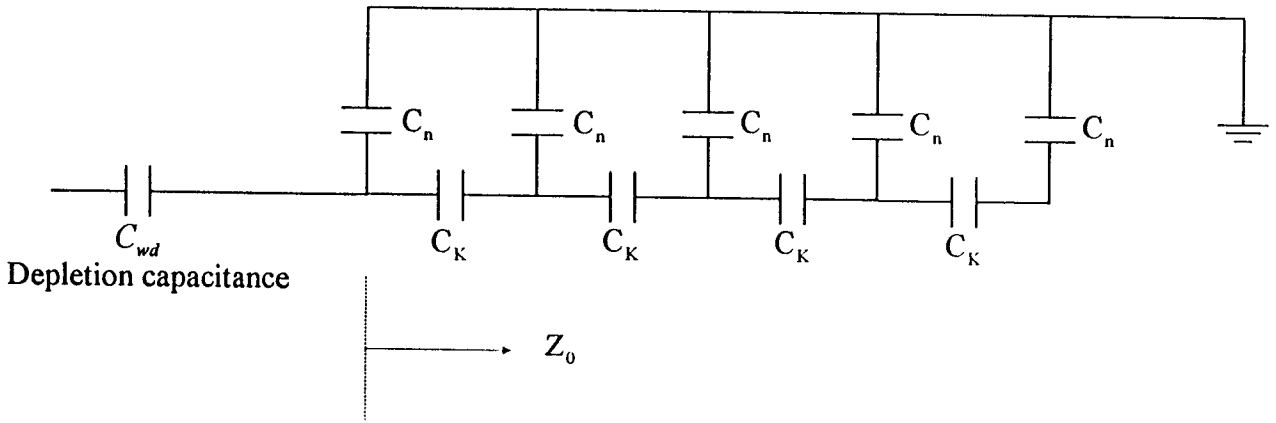


Figure 6.3 Transmission line problem at the edge of depletion region

and γ is just the reciprocal Debye length. For samples longer than this short Debye length the impedance looking into the transmission line is just $Z = \frac{1}{j\omega C_d}$ where C_d is the Debye capacitance.

$$C_d = \sqrt{\frac{q^2 k_s \varepsilon_o n}{kT}} \tag{6.7}$$

These equivalent circuit concepts have been able to reproduce a number of very elegant solutions to difficult problems in conduction in semiconductors and frequency response [51-52]. These techniques have been applied more recently to semi-insulating materials [53][63]. GaAs MESFETs fabricated on semi-insulating substrates are the most obvious application of this analysis. The case of most practical interest is that with the FET biased in the saturation region, resulting in current injection into the substrate, a disturbance in the substrate and consequently noise. Even without current injection, the substrate will have thermal noise at very low frequencies given by the Nyquist formula and the resistance of the substrate [53][63]. This case will not be treated here.

The basic background material for the case where there is current injected into the semi-insulating substrate will be repeated here where it is appropriate to represent the semi-insulating substrate using these equivalent circuit techniques. Fig. 6.4 shows that for each volume element dx, there are C_n and R_n which represent the capacitive effect and resistive effect respectively associated with the redistribution of carriers.

$$R_n = \frac{dx}{q\mu n A} \tag{6.8}$$

$$C_n = \frac{q^2 n A dx}{kT} \tag{6.9}$$

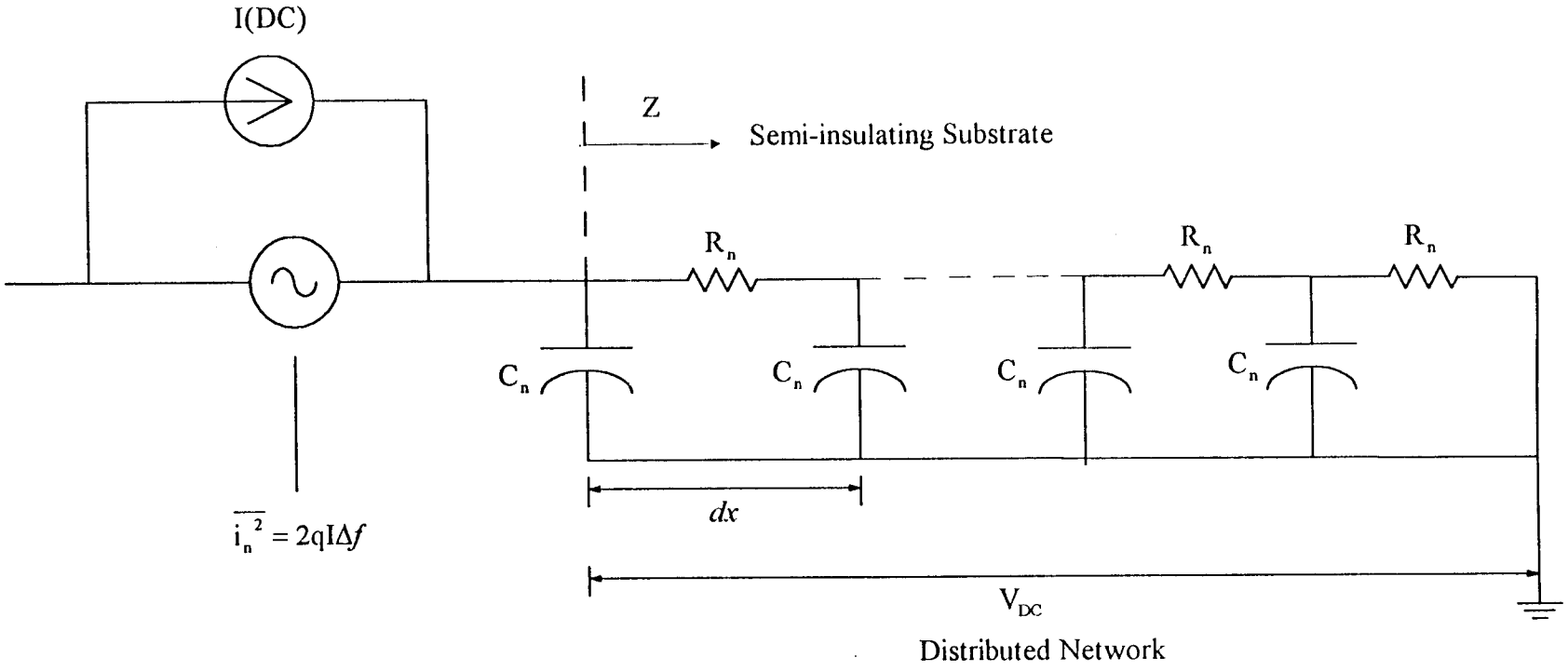


Figure 6.4 Transmission line model for current injection into semi-insulating substrate. Z is the sending end impedance of the distributed network. Substrate material is assumed to be n-type

Under these circumstances, the equivalent transmission line problem for the impedance seen looking into the semi-insulating material is shown in Fig. 6.4. In this case both the characteristic impedance and propagation constant are both complex, being neither real or imaginary,

$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R_n}{j\omega C_n}} \tag{6.10}$$

$$Z_o = \frac{1}{\sqrt{j\omega}} \sqrt{\frac{(\frac{kT}{q})}{\mu}} \frac{1}{qnA} \tag{6.11}$$

$$\gamma dx = \sqrt{ZY} = \sqrt{j\omega C_n R_n}\ dx \tag{6.12}$$

$$\gamma = \sqrt{j\omega} \sqrt{\frac{1}{\frac{kT}{q}\mu}} \tag{6.13}$$

For a short line, the sample is small in extent or if the frequency is low, then the sending end impedance is

$$Z = Z_o \tanh(\gamma l) = Z_o(\gamma l) \tag{6.14}$$

which simplifies to,

$$Z = Z_{DC} = R = \frac{l}{q\mu nA} \tag{6.15}$$

or just the DC resistance of the sample.

For long lines of larger extent or high frequency, the sending end impedance of this lossy line is

$$Z = Z_o = \frac{Z_{DC}}{\gamma l} \tag{6.16}$$

If, as shown in Fig. 6.4, we now inject a DC substrate current I, into this semi-insulating material, there will be a shot noise source with mean square noise current;

$$\overline{i_n^2} = 2qI\Delta f \tag{6.17}$$

This mean square noise current will result in a mean square noise voltage at the point of injection;

$$\overline{v_n^2} = \overline{i_n^2}|Z|^2 \tag{6.18}$$

$$\overline{i_n^2} = \frac{2qI\Delta f Z_{DC}^2}{|\gamma l|^2} \tag{6.19}$$

Because $$IZ_{DC} = V_{DC} \tag{6.20}$$

and $$(\frac{V_{DC}}{l})(\frac{\mu}{l}) = \frac{v_d}{l} = \frac{1}{t_t} = \omega_c \tag{6.21}$$

this simplifies to $$\overline{v_n^2} = 2(\frac{kT}{q})q\Delta f Z_{DC}(\frac{\omega_c}{\omega}) \tag{6.22}$$

at the surface of the sample for frequencies higher than the reciprocal transit time. Here, ω_c is the reciprocal of the transit time of the carriers across the substrate.

At frequencies lower than the reciprocal transit time the solution reverts back to the short line case where the sample is just resistive.

$$\overline{v_n^2} = 2\ q\ I\ \Delta f\ R \tag{6.23}$$

$$\omega_{cth} = (\frac{kT}{q})(\frac{\mu}{l^2}) \tag{6.24}$$

The low corner frequency, ω_{cth}, is the reciprocal of the transit time in response to the thermal voltage $(\frac{kT}{q})$, and is obtained from equations (6.22) and (6.23).

1/f noise is a bulk phenomena due to fluctuations of charge and potential inside the high impedance semi-insulating material [36]. The lowest frequencies are associated with long range fluctuations and require samples of large volume and extent. Injecting current into high impedance semi-insulating materials with a large DC voltage drop across them will result in large mean square 1/f noise voltages, given by

$$\overline{v_n^2} = 2(\frac{kT}{q})\Delta f \frac{Z_{oc}}{(t_t \omega)} \tag{6.25}$$

Fig. 6.5 shows the mean square noise voltages of this distributed network with current injection. The case without current injection or just thermal noise in the substrate [53] when the FET has no drain to source voltage is not given here.

These results are directly applicable to GaAs MESFETs on semi-insulating substrates. Impact ionization and multiplication of carriers in the drain region of MESFETs at higher drain voltages will result in non-trivial substrate currents being injected into the semi-insulating substrate. Large mean square 1/f noise voltages will result which will backgate the FET channel and be amplified by the backgate transconductance of the device. This problem is similar to the substrate current and backgate transconductance in silicon MOSFET's, except they usually have low impedance substrates at room temperature.

This theory predicts the 1/f or 1/ω frequency dependence. The DC current is the substrate current of a GaAs MESFETs being injected into the semi-insulating substrate. This produces a backgate noise voltage which is amplified by the backgate

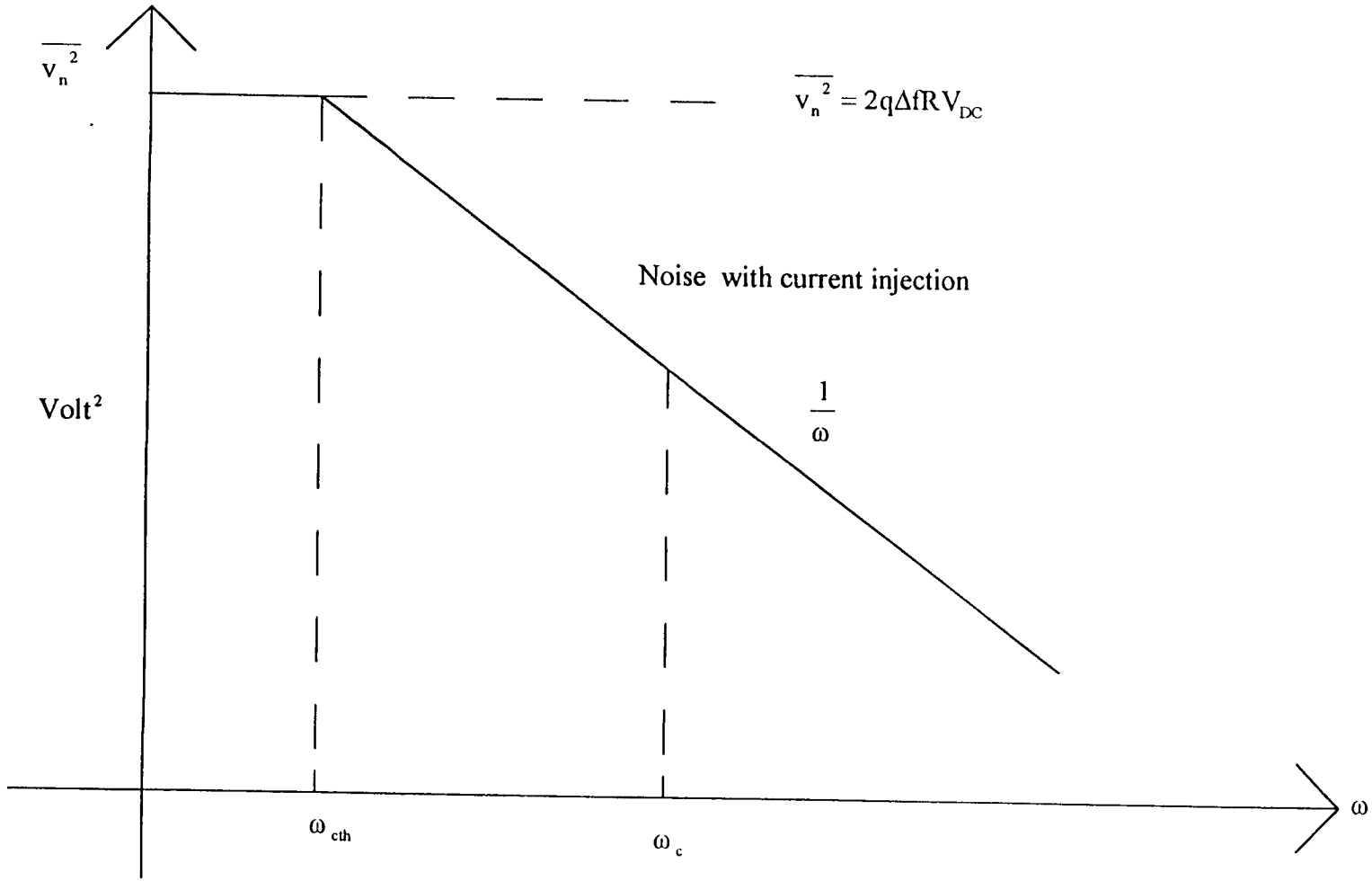


Figure 6.5 Mean square noise voltage

transconductance, g_{mbg}. The mean square noise current at the drain is the mean square voltage amplified by $g_{mbg}^{\ 2}$.

$$\overline{i_{n\ 1/f}^{\ 2}} = g_{mbg}^{\ 2}\ \ 2(\frac{kT}{q})q\Delta f\frac{R\omega_c}{\omega} \tag{6.26}$$

The equation of the mean square thermal noise of a GaAs MESFETs is commonly represented as,

$$\overline{i_{n\ thermal}^{\ 2}} = 4kTg_m\Gamma\Delta f \tag{6.27}$$

where g_m is the FET transconductance and Γ is normally assumed to be 2/3. [2]

Equating the 1/f and thermal mean square currents locates the 1/f corner frequency,

$$\omega_{1/f} = \frac{g_{mbg}}{2\ \Gamma\ g_m}(g_{mbg}\ \ R)\ \ \omega_c \tag{6.28}$$

Equation (6.28) then predicts relatively the high 1/f noise corner frequencies in GaAs MESFETs technology [54]. The results and theory presented here are different from the various explanations given previously for the 1/f noise of MESFETs. [47] [48] [55-59]

6.4 Experimental

In an attempt to verify the 1/f corner frequency formula, we have measured the DC value of g_{mbg} has been measured by applying DC bias to the substrate. A value of g_{mbg} of 0.01mS has been obtained for a depletion mode MESFETs biased above pinch off with a g_m value of 11.9mS. The reciprocal of the transit time of the carriers, ω_C, is computed to be 1.6×10^5 radians/sec with the assumption that the DC voltage developed across the semi-insulating substrate sample is 1V. Fig. 6.6 is the die photo of the discrete

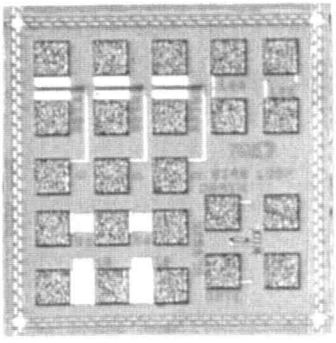


Figure 6.6 Die Photo of discrete MESFETs

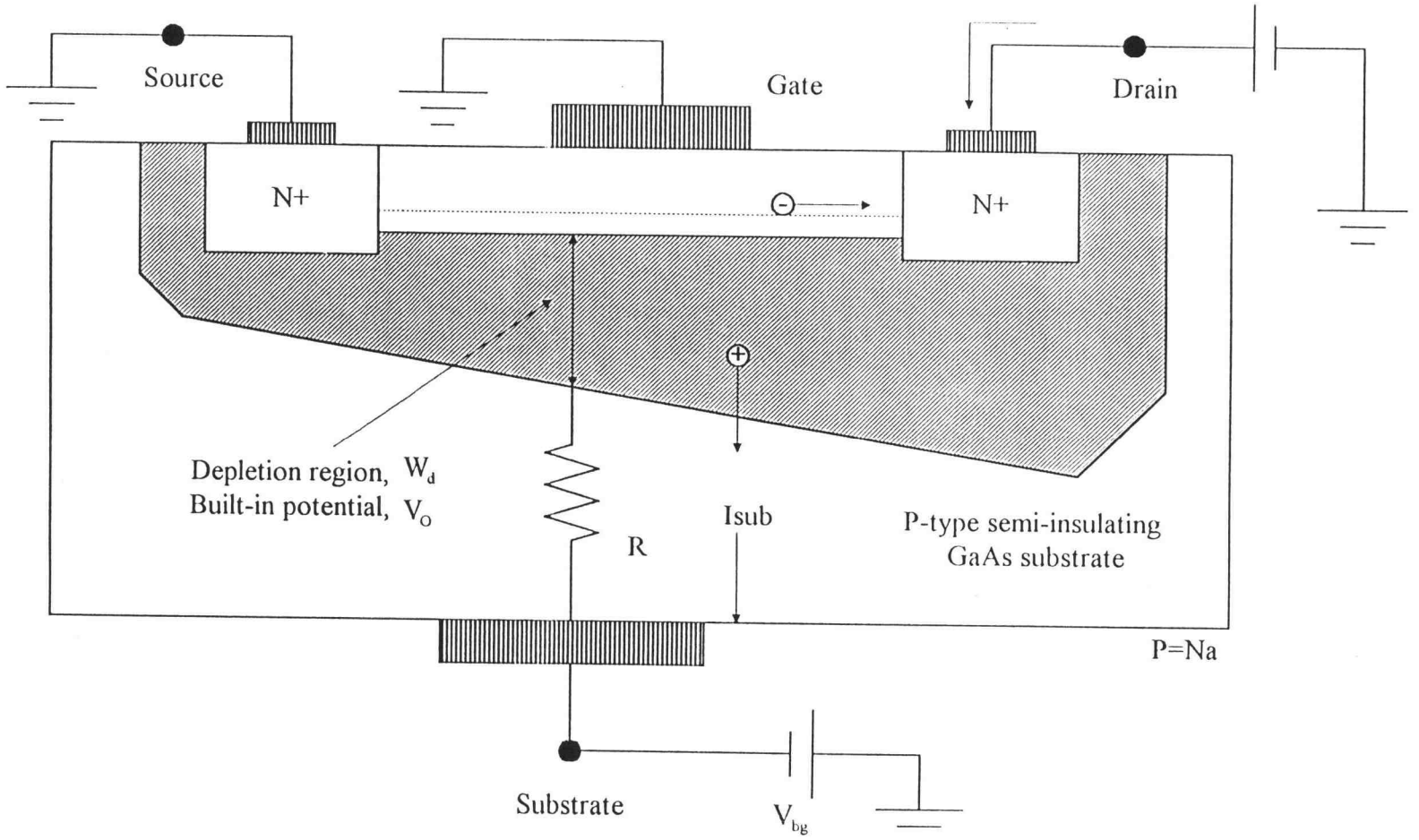
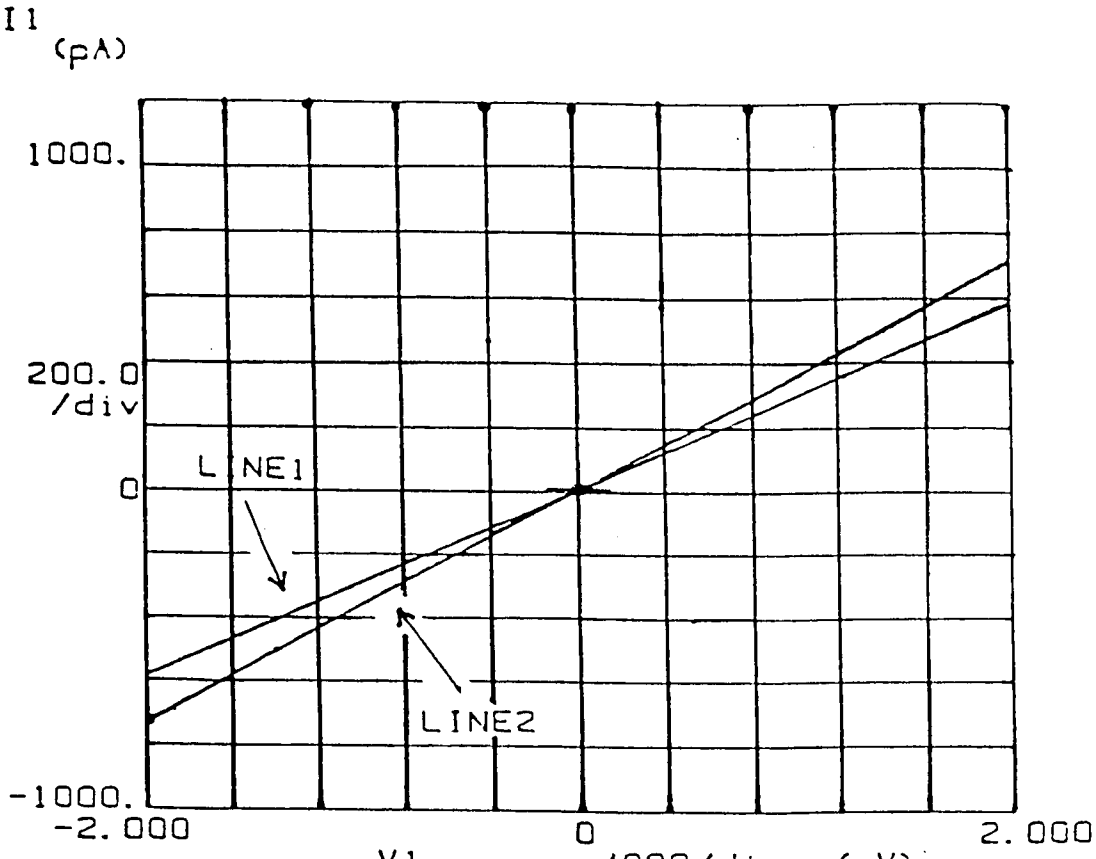


Figure 6.7 Cross-section of a MESFETs device structure. The voltage, V, developes across the substrate thickness, d, due to leakeage and substrate current



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	294E-12	3.40E+09	-23.1E-03	6.80E-12
LINE2	355E-12	2.81E+09	-23.2E-03	8.25E-12

Figure 6.8 Measurement of GaAs MESFETs post process substrate resistance, LINE1 and LINE2 indicate arbitrary sites on the same wafer with the corresponding resistance indicated by 1/GRAD

MESFETs. Fig. 6.7 is the cross sectional view of the MESFETs with R is the low frequency DC resistance of the substrate. Fig. 6.8 shows a small sample of the values of the measured resistance of the substrate obtained by biasing the drain, source, and channel with respect to the backside substrate contact. It has been found experimentally that the resistance can vary from $1X10^{9}$ to $1X10^{10}$ ohms, which includes the parallel resistances of source to backside and drain to backside. For demonstration purposes, an R value of $2.4X10^{10}$ ohm is chosen. With these numbers, we have computed the corner frequency to be 4MHz.

The noise spectrum of a depletion mode MESFETs biased with a g_m value of 11.9mS has been measured. The noise measurement was performed by coupling the depletion mode, DFET MESFETs with a low noise bipolar amplifier which has a bandwidth of up to 100MHz as described in a paper by Reimbold. [59] The output is then coupled to a spectrum analyzer. With the DFET biased above pinch off at a transconductance value of 11.9mS, the 1/f noise corner frequency is indicated in Fig. 6.9 to be between 3MHz and 6MHz. This compares favorably the 1/f noise corner frequency predicted by the bulk phenomena theory.

Other noise sources may of course also contribute low frequency noise. Fig. 6.10 shows another sample which displays some generation-recombination noise [61-62] as a bump at around 100KHz. This is superimposed on the background of 1/f noise. It had been claimed by Hughes et al. [48] that generation and recombination is a contributor to 1/f noise and can be reduced by determining an optimum doping level of the channel. On the other hand, Forbes et al. [18-19] have clearly demonstrated that 1/f noise is not due to

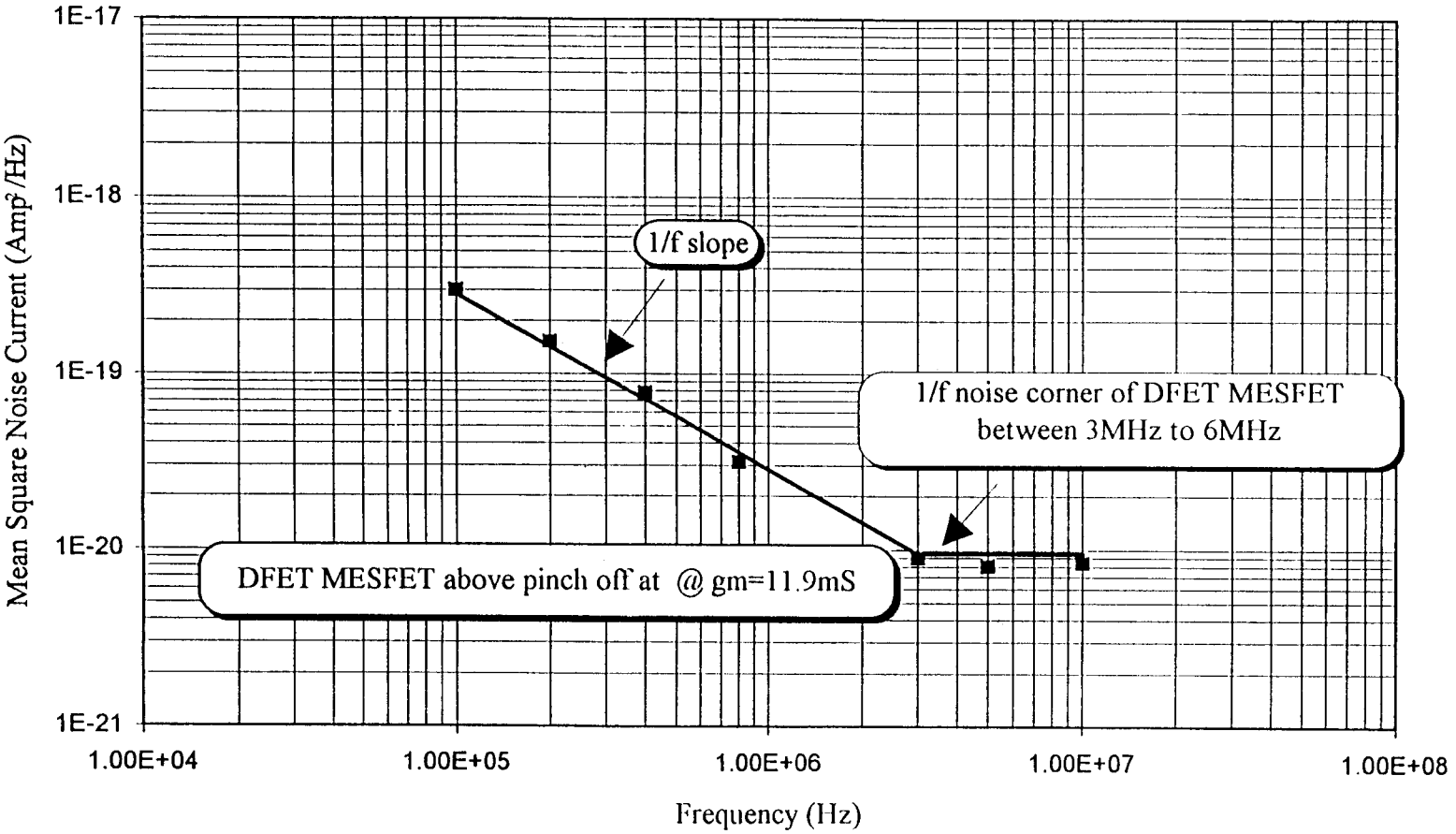


Figure 6.9 Depletion mode GaAs MESFETs noise spectrum with FET biased above pinch-off with g_m =11.9mS

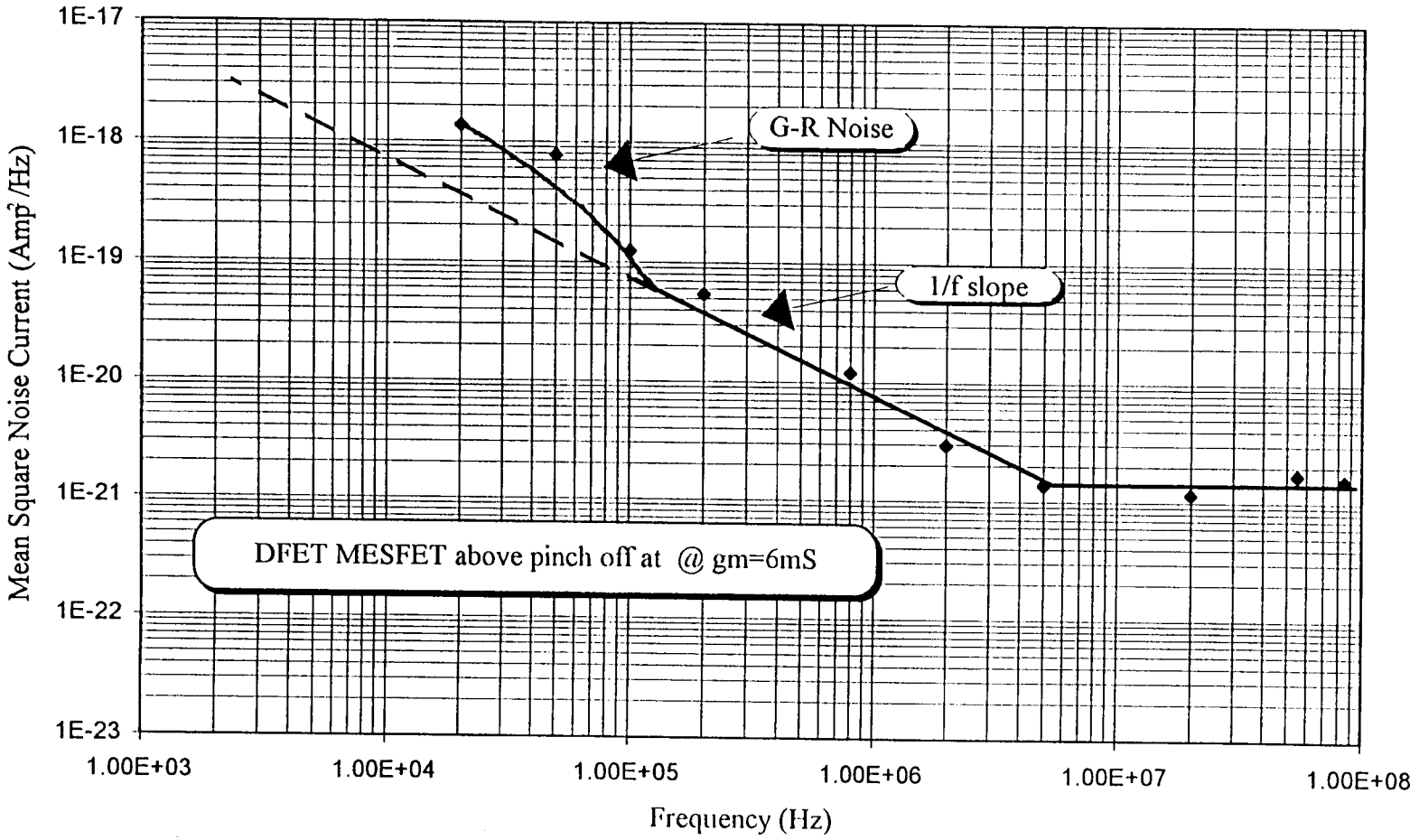


Figure 6.10 Depletion mode GaAs MESFETs noise spectrum with FET biased above pinch-off with g_m =6.0mS

the generation and recombination process. By increasing the temperature of the devices, the bumps associated with generation and recombination noise all move to higher frequencies leaving behind a residual 1/f noise component. Forbes proposed and demonstrated a buried channel device structure that can be used to suppress generation-recombination noise. [62]

6.5 Comparison of 1/f Noise Performance of L=1μm and L=0.6μm Technology

Using the same techniques described in Chapter 4, the mean square noise current for the frequency range of 100KHz to 100MHz can be measured. Fig. 6.11 gives the "off" condition for Vgs=-2V and Vds=0V which will be the reference noise level. With the test DFET W/L=120μm/1μm biased above pinch off and at g_m value of 20mS, the output noise spectrum is measured as shown Fig. 6.12. This noise spectrum needs to be corrected by the normalized mean square noise current indicated in Fig. 6.13. The same measurement is made for 0.6μm technology with the test DFET with W/L=120μm/0.6μm biased at a g_m value of 20mS and the output noise spectrum measured as shown in Fig. 6.14. Similarly, this noise spectrum needs to be corrected by the normalized mean square noise current as shown in Fig. 6.15.

Fig. 6.16 is the combination of Fig. 6.13 and Fig. 6.15 to highlight the fact that the 1/f noise using the short gate length MESFETs technology has improved. This is probably due to the reduction of R, substrate resistance, due to the implantation of the buried P-layer underneath the DFET.

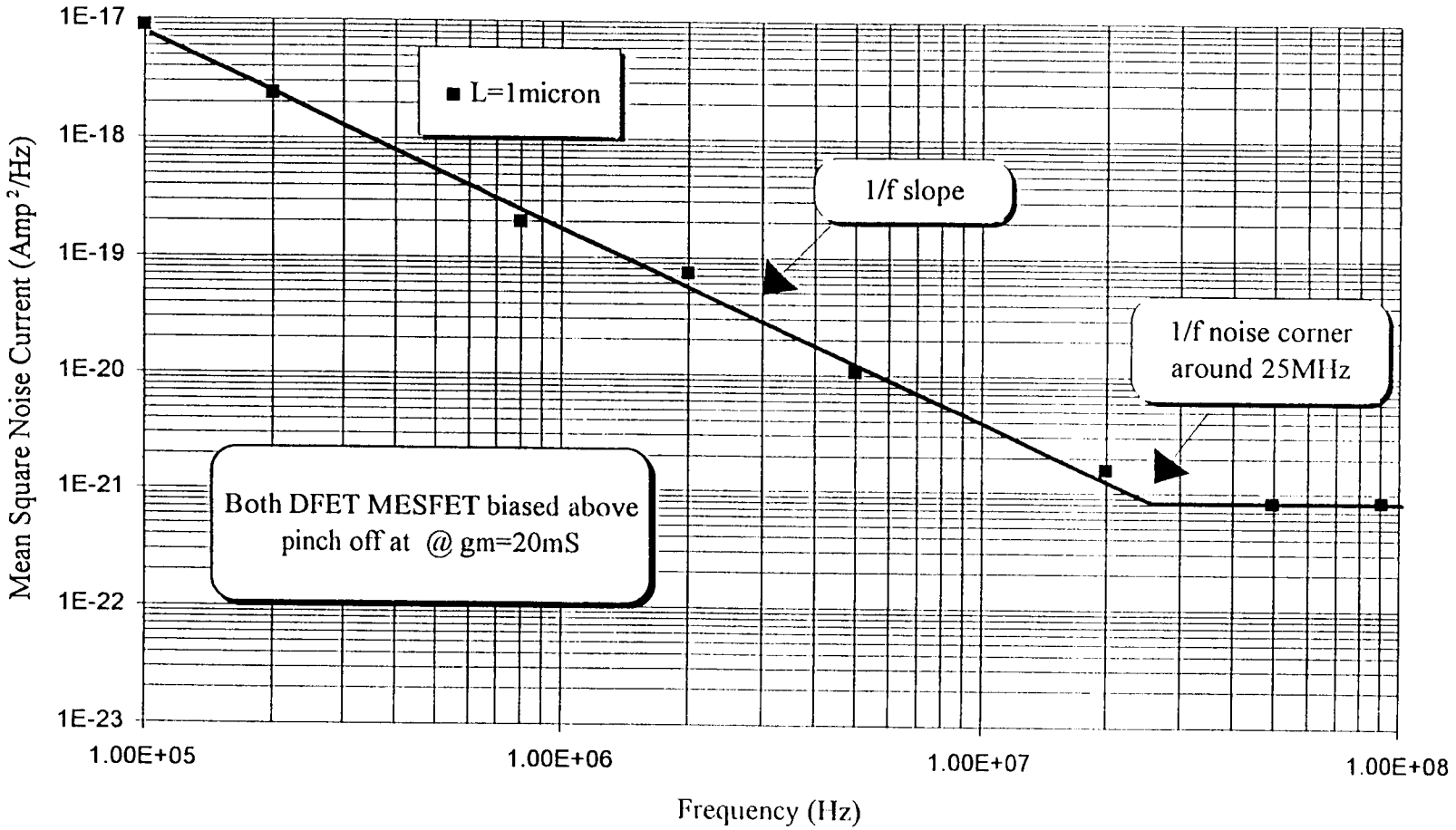


Figure 6.13 Mean square output noise spectrum at "on" condition for DFET MESFETs biased V_{gs} = 0V and V_{ds} = 1.5V where g_m =20mS in L = 1μm technology

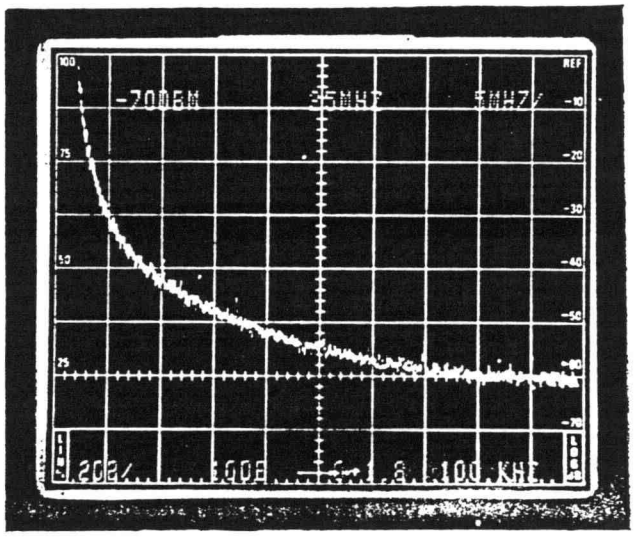


Figure 6.14 Output noise spectrum at "on" condition for DFET MESFETs biased $V_{gs} = -0.1V$ and $V_{ds} = 1.5V$ where $g_m = 20mS$ in $L = 0.6\mu m$ technology

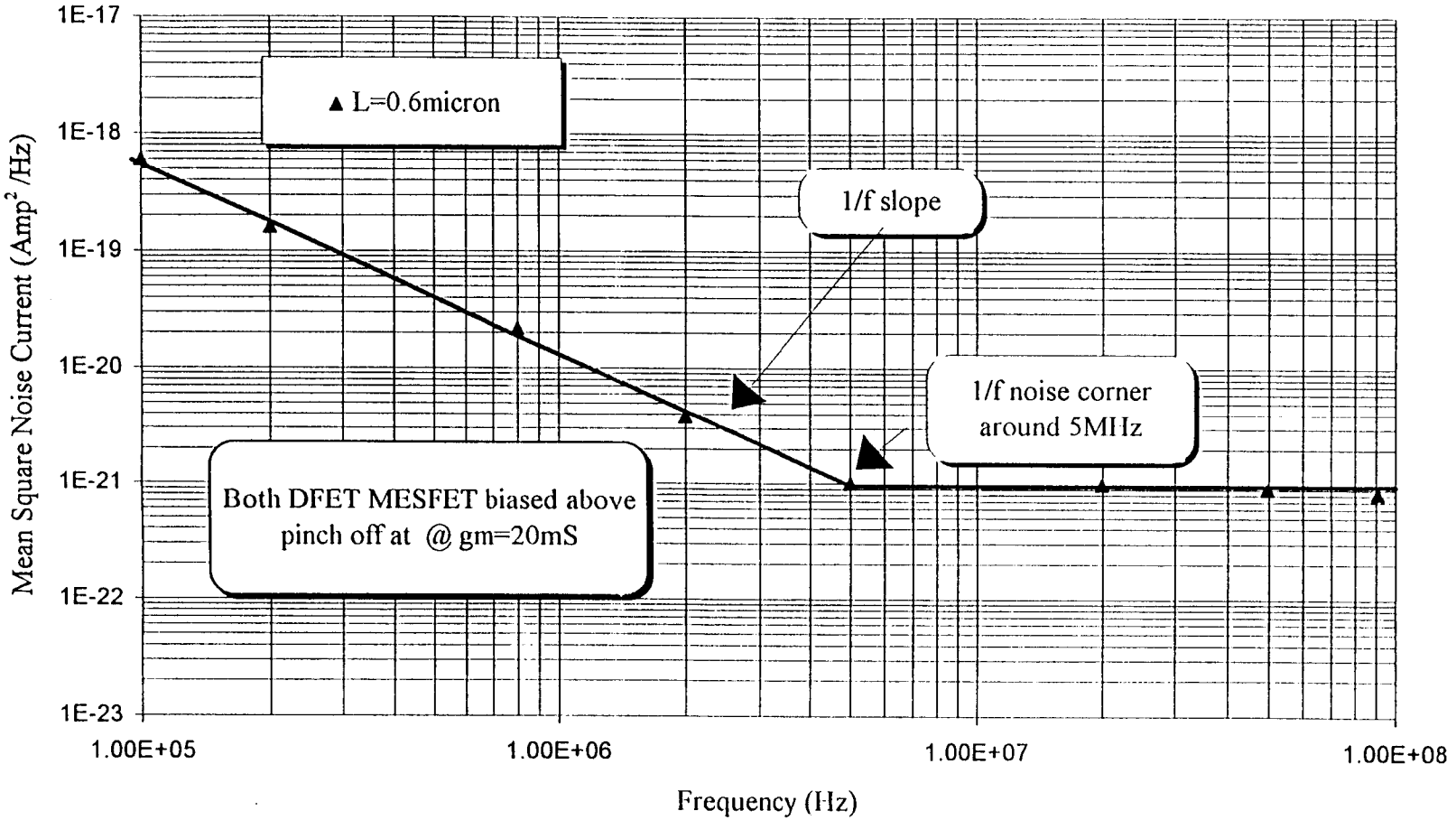


Figure 6.15 Mean square output noise spectrum at "on" condition for DFET MESFETs biased V_{gs} = −0.1V and V_{ds} = 1.5V where g_m =20mS in L = 0.6μm technology

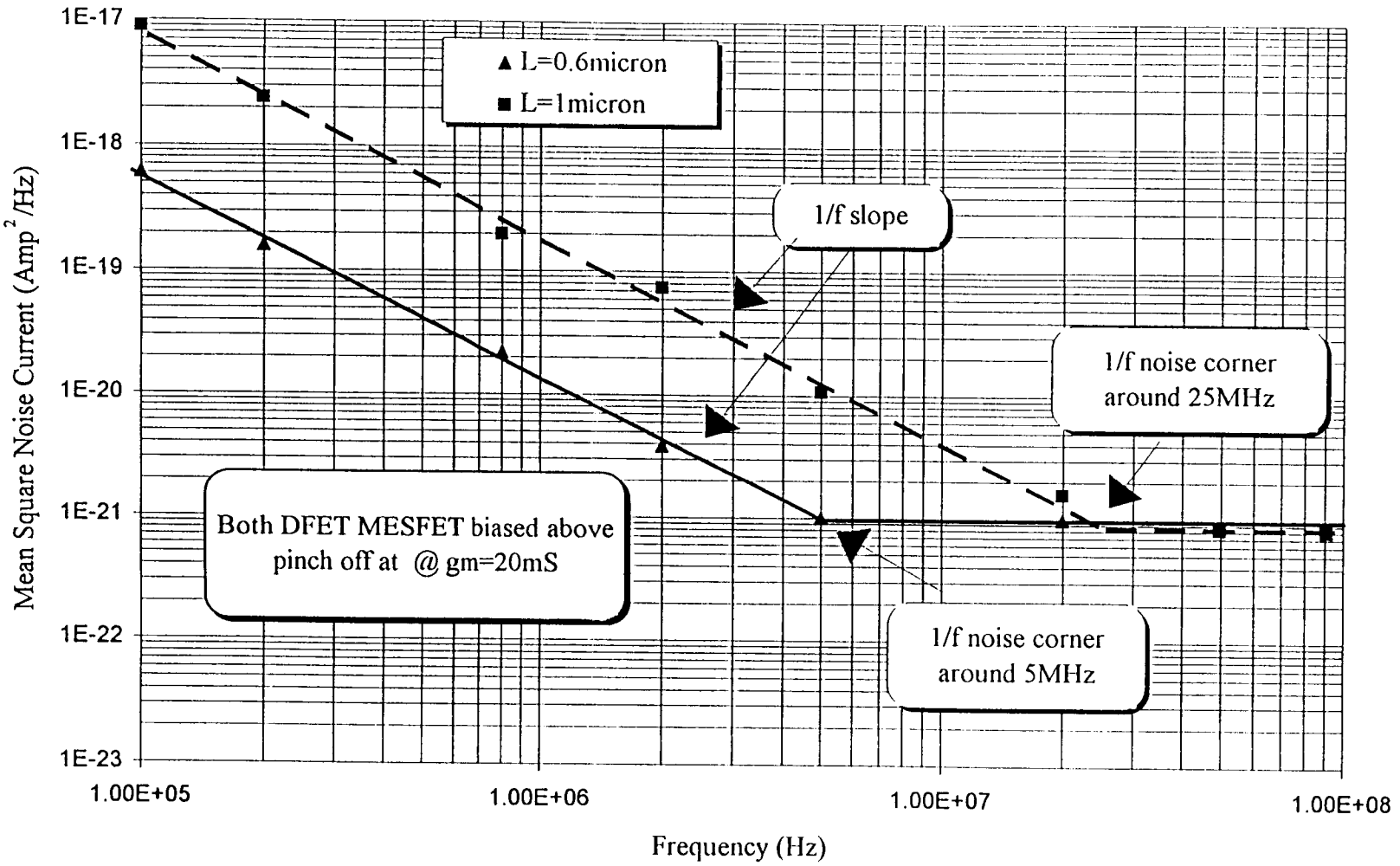


Figure 6.16 Mean square output noise spectrum comparison between L = 1μm and L = 0.6μm technology

6.6 Summary

The substrate resistance will vary from wafer to wafer and due to illumination. In addition, the backgate transconductance also varies with frequency. This needs to be modeled more accurately for a precise 1/f corner frequency determination, which is beyond the scope of this thesis. We can nonetheless predict based on the worst case variations in backgate transconductance and low frequency DC resistance of the substrate that the 1/f corner frequency is between 0.3MHz and 30MHz. We have demonstrated a consistency between the 1/f corner frequency predicted by this new theory and the measured noise spectrum. To the best of our knowledge no previous theory, which does not employ an empirical parameter, for example Hooge's parameter , has been able to show a correspondence between the theoretical and measured 1/f noise corner frequencies. One consequence of this model is that it predicts FET's with longer transit times for carriers across the backgate substrate and lower DC voltages across the substrate will have a lower 1/f noise corner frequency. Note that both the backgate substrate resistance, R, and backgate transconductance, g_{mbg}, depend on the substrate doping. In a simple model, the product $R(g_{mbg}^{2})$ is independent of doping. This theory predicts that devices with a low backgate substrate resistance and low substrate currents should be expected to have low 1/f noise, limited by other noise mechanisms. Devices on semi-insulating substrates, however, will have high 1/f noise corner frequencies determined by the semi-insulating substrate itself.

7. CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

7.1 Summary and Conclusion

A large investment has been made in time over three years and money in fabrication runs, development of accurate models, simulations, equipment and measurement techniques. We have available the latest relevant PSpice models, the TriQuint Own Model or TOM. As such there is a high degree of confidence in the results and techniques. Many of the older measurements in the literature are suspect and may for instance, not include corrections for differences in signal bandwidth and noise bandwidth of spectrum analyzers which was not appreciated until 1977 [65]. We have been able to determine the absolute value of Γ appropriate to long channel devices without hot electron effects. The channel noise coefficient, Γ, has then been obtained as a function of bias conditions for short channel MESFETs. To the best of our knowledge this has not been done previously for MESFETs, with hot electron effects.

The unique opportunity of industrial collaboration has also led to dedicated circuit designed specifically for the purpose of the accurate measurement of the thermal and 1/f noise characteristics of MESFETs. Physical theories for both the thermal and 1/f noise have been developed to analyze the measured data on state-of-art foundry service devices from TriQuint Semiconductor.

Thus new comprehensive noise models for MESFETs including 1/f and channel noise have been developed which constitutes a significant contribution to this particular technology. GaAs MESFETs are expected to become widely used in either fiber optic

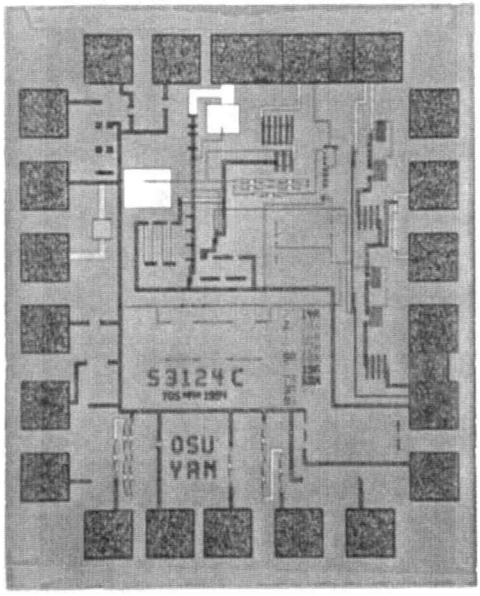


Figure 7.1 Die photo of L = 0.6μm transimpedance amplifier with integrated depletion mode resistors

systems or wireless communication systems, whichever prevails as the primary technology in the mass information media expansions.

The PSPICE models currently use the ideal value of "gamma" of 2/3 for the thermal noise and have two adjustable parameters for 1/f noise. By using the device equations option in PSPICE we should be able to incorporate alternative noise models into PSPICE.

7.2 Suggestion for Future Work

A natural extension of the present research work is to address the issue of how to better improve the process so as to exploit the new knowledge which has been obtained during the course of this research. The current trend to reduce the device gate length to attain higher speed and larger circuit density will eventually need to address the issue of more sophisticated device engineering to combat the effects of 1/f noise. So far preliminary results have shown that submicron devices manufactured using the P-well technology will helped to improve the 1/f noise performance [37]. The P-Well technology has undergone numerous changes and improvements. This technology has also been found to be useful for mixed-mode circuits [64].

Another research area which is worth addressing is the reduction of the backgate transconductance frequency dependence. This may help to explained the variation of 1/f corner frequency from device to device. In a 1μm technology, the 1/f noise corner frequency can vary by as much as a factor of 10 from 3MHz to 30MHz.

In addition, a transimpedance amplifier with integrated resistors has been fabricated as shown in the die photo in Fig. 7.1. This should be able to enhance the current knowledge of the 1/f noise performance of ion-implanted resistors [36].

Another area of study is in the field of noise characteristic of Metal-Semiconductor-Metal or MSM photodetectors made on semi-insulating GaAs. The ability to use the current theories of 1/f noise and thermal noise to design higher quality and lower noise photodetectors will be a great asset for a commercially proven MESFETs process. This will certainly help MESFETs technology dominate the low noise fiber optics interconnect market which is currently lacking a high performance front-end detector.

Another possible study is to quantify the tradeoffs in transimpedance amplifier bandwidth, noise performance and dynamic range and their relationship to the unity gain frequency, F_t in the GaAs MESFETs technology. This work is needed since little work has been done concerning this issue in the open literature. We need to review, extend and improve the circuit approaches for increasing the dynamic range of the transimpedance amplifier. A study of the different kind of circuit topologies available should be made, whether one stage, two stage or three stage using either differential or single ended transimpedance amplifiers.

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