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Abstract approved: _____

Shih-Lien Lu

A CMOS implementation of a True-Q Flip Flop is presented. It can perform either as an asynchronous storage element in micropipelines or a part of the synchronizer. It is capable of double-edge triggering which latches data at both the rising and the trailing edges. It is also free of the metastability state problem.

Some analog and digital circuits are incorporated with a true double-edge triggered Flip Flop (DETFF) making it a True-Q Flip Flop. A True-Q Flip Flop outputs an acknowledge signal only after the Q and NQ are stablized. Therefore, if the proceeding stages utilize this acknowledge signal as the triggering signal, then, the value of Q from the flip flop will not be received by the next stage if Q is in a metastable state.

The number of transistors used in this implementation of True-Q flip flop is 90. Due to the overhead of circuit complexity, the time delay from Request to Acknowledge signal is 6.5ns.

A Design of True-Q Flip Flop

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Henry Hui, Author

To my parents, sisters and brothers

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A Design of True-Q Flip Flop

Chapter 1
INTRODUCTION

1.1 Digital System Design

Synchronization is one of the important issues in designing a digital system. By the synchronization method, generally speaking, digital systems design can be classified as synchronous and asynchronous. As we look at the various current computer machines, globally clocked timing discipline has been the dominant design philosophy. The reasons are :

- Major components of a computer system, like the memory (DRAM) and the CPU, are built synchronously.

-The step by step nature of synchronous system makes design and trouble-shooting easier to perform by engineers.

-Usually, synchronous systems will require fewer transistors to implement them, thus lowering the cost of the system.

However, as the VLSI technology advances rapidly, the length of the gate channel is less than 1um. The global synchronization method of a digital system has become increasingly difficult because the clock periods are getting much smaller than the interconnect propagation delays within a single chip, PC Board factor is not taken into consideration yet. Moreover, the theory and methodology of asynchronous computing systems design have been maturing. Asynchronous systems possess many advantages.

-First, asynchronous designs are algorithmic instead of step by step in nature. It is easier to convert an algorithm to a wiring list for an asynchronous design than for asynchronous design.

-Second, systems designed asynchronously without a global clock will not have any problems with clock skew because of their event-driven nature.

-Third, it is not necessary to adjust the pulse width and the clock period to fit all modules' timing requirements. Therefore, an asynchronous design's maximum speed of execution will be as fast as the algorithm allows.

-Fourth, the interfacing among the asynchronous modules will not be a complicated task.

-Fifth, the individual asynchronous module on a single chip enables the testing and verification of each chip to be performed independently. So it saves testing time.

-Sixth, the asynchronous nature of a design allows slower peripherals to be replaced with faster peripherals without modification to the processor.

-Finally, asynchronous systems will not only have low power consumption but also produce less noise in the whole system. This is mainly due to the absence of the global clock. The low power consumption feature is especially useful when the portability of the application is important.

1.2 Transition Signaling

Transition signaling shown on Fig 1.1 is widely used in asynchronous system. The falling and rising transitions in transition signaling have the same meaning. The state, high or low, of the control signal is of no concern. Therefore, the control signal does not need to go back to an assigned state before next operation. This feature saves both time and

energy. This type of signaling is often called as the 2-phase signaling scheme. Another scheme, which is called 4-phase signaling scheme, triggers a particular state. Therefore, the control signal needs to return to the original state. Since the 2-phase transition signaling uses both rising and falling edges as trigger events, it offers twice the speed potential.

Fig.1.1 Transition signaling

1.3 The Two-Phase Bundled Data Convention

In asynchronous systems, Acknowledge and Request signals are incorporated so that data can pass from a sender to a receiver. Their operations are depicted in Fig 1.2 and briefly explained.

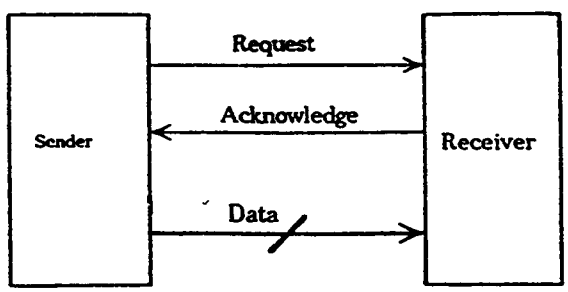


Fig.1.2 The control signals for Sender and Receiver

Once sender receives the acknowledge signal from receiver, then both request and data signal are released by the sender. A delay line may be added on the request signal for ensuring that only valid data are available for the receiver. The receiver starts to get the data when the request signal is received by it. After that, the acknowledge signal is released from receiver to the sender, while data and delayed request signals march forward to the next stage from the receiver. Now, the receiver becomes a sender.

1.4 Event Logic

Event logic is used by control circuit for transition signaling. For the sake of simplicity, only OR and AND events logic will be covered here. OR event logic can be implemented by an Exclusive Or circuit. Any state change in either input of the Xor circuit will produce a new state to output. A more complicated circuit, which is called Muller-C element, is applied to utilize the AND event logic. Its symbol and logic operation are shown in Fig. 1.3. Both circuits' transistors level implementation will be discussed further in Chapter 3.

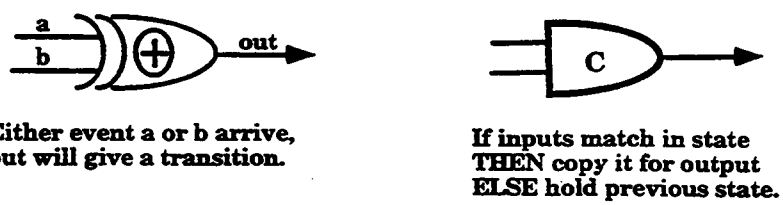


Fig.1.3 The OR and AND event logic symbols

1.5 Event-Controlled Storage Elements

A storage element for implementation of transition signaling control system is shown in Fig. 1.4. We will describe the detail in the following section.

This storage element is made up of three switches and two control signals. The operation of a switch is discussed first. Referring to Fig. 1.5, control signal *c* and its complement *nc* are used to select two events, which are *x* and *y* inputs. If *c* is low (high), the output *z* will be *y (x)* and vice versa. Now looking at Fig. 1.4 again, its operations can be explained by the relative states of two control signals. Assume that those switches will be in the position shown after master clear applied. If *Capture* and *Pass* signals are in the same state, then *In* will go through to *Out* directly. If *Capture* and *Pass* signals are in different states, then the coming *In* data cannot affect the value of *Out*, which will provide the previous *In* data to the next stage only. The table 1.1 summarizes all possible inputs and outputs.

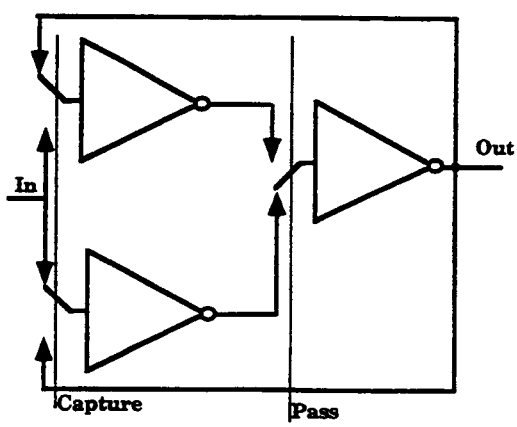


Fig. 1.4 The event storage element

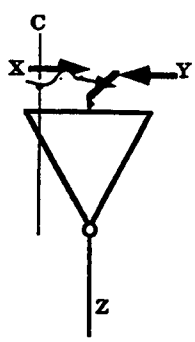


Fig.1.5 Switch

Capture/ Pass	In	Out	Actions done by storage element
0/0 and 1/1	new data	new data	transparent
0/1 and 1/0	new data	previous data	pass latched data

Table 1.1 The operations of event storage element

1.6 A 2-cycle FIFO Micropipelines

Sutherland describes an event-driven pipeline based on the transition-signaling framework as a micropipelines. In Fig 1.6 the pipeline without processing, that is FIFO, can be built with Muller-C and event storage elements. A set of event-controlled storage registers are connected in series so that they provide the mean to store data between stages. A string of Muller C-elements serve as the control logic. Each storage register has one Muller -C element adjacent to it. Pd and Cd are representing *Pass done* and *Capture done* used in event storage elements respectively. These two signals usually have been amplified for driving more paralleled registers. Capture done signal acts as a request signal for the next stage while pass done, which acts as acknowledge signal, will feedback to the Muller-C element of its own stage.

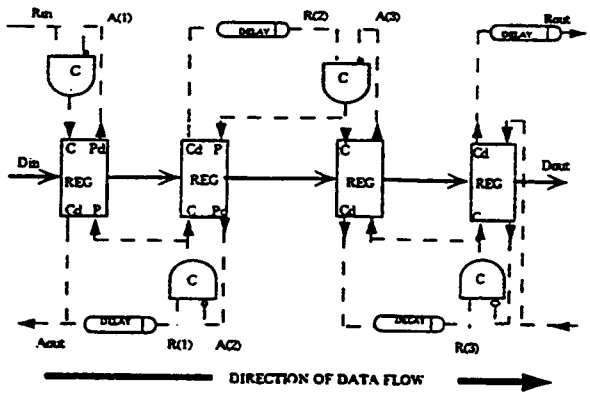


Fig.1.6 The FIFO Micropipelines

1.7 Summaries of the Thesis

This chapter has introduced the advantages of using asynchronous digital system design. The operation and construction of Micropipelines have discussed.

In the next chapter, we will discuss the relationship between bistable circuits and metastable state. In the third chapter, the design and applications of True -Q flip flops will be covered. In the fourth chapter, simulation results of our implementation of a True-Q flip flop will be presented. Finally, the chapter 5 will conclude what things had been done in this thesis.

Chapter 2

THE RELATIONSHIP BETWEEN BISTABLE CIRCUITS AND METASTABLE STATE

2.1 Latches and Registers

Both latches and registers are storage elements in digital systems. In a globally clocked system, their operations have to satisfy some timing constricts, which are represented by Fig 2.1 graphically. The timing waveforms in Fig. 2.1 describe the setup, hold and clock-to-Q delay time of a positive edge-triggered register. The time before the clock edge that the Data input has to be stable is called the setup time (Ts), and the time after the clock edge that the Data input has to remain stable is called the hold time (Th). The delay from the positive clock input to the new value of the Q output is called the clock-to-Q delay (Tq). The time between successive positive clock transitions is called the cycle time(Tc).

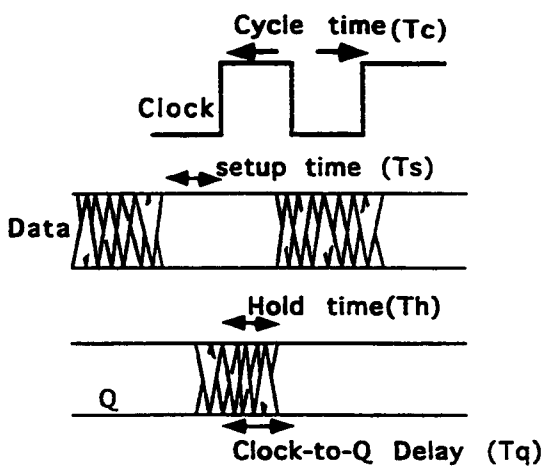


Fig 2.1 The timing constraints in latch

2.2 Level-Sensitive Latch

A latch can be built up by two inverters and a multiplexer. This structure shown in Fig.2.2 is a negative level-sensitive latch. The output follows the input when the clock is low. The D input must be stable for a short time before and after the positive transition.

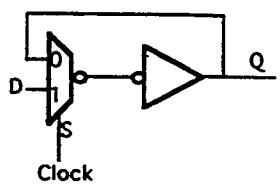


Fig.2.2 Negative level-sensitive latch

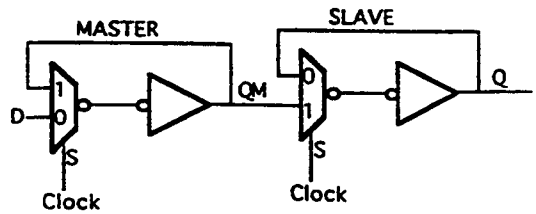


Fig.2.3 An edge trigger register

2.3 The Edge-Triggered Register

Basically, an edge-triggered register can be constructed by one negative level-sensitive latch and one positive level-sensitive latch as shown in Fig. 2.3. The first latch stage is called the master and the second is called the slave. The operations are described as below: When the clock is low, the master negative level-sensitive-latch output follows the D input while the slave positive keeps the previous data input. Considering transition of the clock from 1 to 0, the slave latch retains the master-latch output and the master starts sampling the input again. Therefore, this device is called a positive edge-triggered register because the input is sampled during rising edge of the clock.

2.4 Metastability

Latches can be used in both asynchronous and synchronous systems as a storage element. In synchronous system, if the data and clock do not satisfy the setup and hold-time constraints of a register, a synchronization failure may occur. This failure can result in the latch's output entering an indeterminate state between 0 and 1. Since both latches and registers are made up of inverters in CMOS circuit level, the sampled input must be close to the inverter threshold voltage. Therefore, the latch is balanced between making a decision to resolve 1 or 0. Even a slight noise (thermal) will push the latch output to 1 or 0. The delay caused by the metastability may allow the latch output to exhibit two different values within one or more clock cycle(s), thus the logic block interprets these two different values. The interpretation of this signal will cause a synchronization failure. The Fig.2.4 shows the conditions for metastability and is explained as follow. A fast-falling clock and a slow-rising data signals are shown on the top waveform. The data is delayed from 1.2ns to 1.4ns. At 1.2ns, the Q of latch changes from low to high. When the delay is 1.3ns, Q still makes a low-to-high transition, but there are some times spending at the transition point of the inverters. The 1.4ns delay makes the Q spend a significant time at metastable state and change to low arbitrarily. Similarly, the metastability in asynchronous systems can be described by Fig 2.4 when clock signal is substituted by request signal.

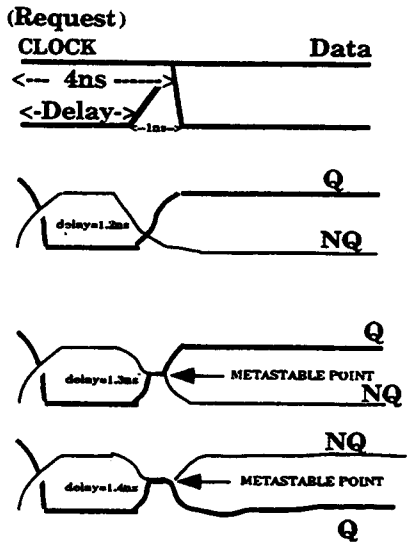


Fig. 2.4 The conditions for metastability in both asynchronous and synchronous system

2.5 The Interface between Synchronous and Asynchronous System

In clocked system, if the clock-to-Q delays are longer than the setup times (assume there is no clock skew and clock cycle is appropriate), then no metastability problem exists. However, it will happen with definite probability whenever there are two different clocked systems or a clocked system interfacing with a asynchronous input. There are some circuits called synchronizers, which are used to handle these asynchronous interfaces. The function of synchronizers is lowering the probability of synchronization failure. The typical synchronizer circuit is shown in Fig.2.5. There are two cascaded registers in the circuit. The first register interfacing with asynchronous input may enter metastable state under some conditions. By adding the second register, an extra clock cycle is provided to allow the output of the first register to resolve. More registers may be cascaded to decrease the probability of synchronization failure. Note that the probability of synchronization failure is never zero in this circuit.

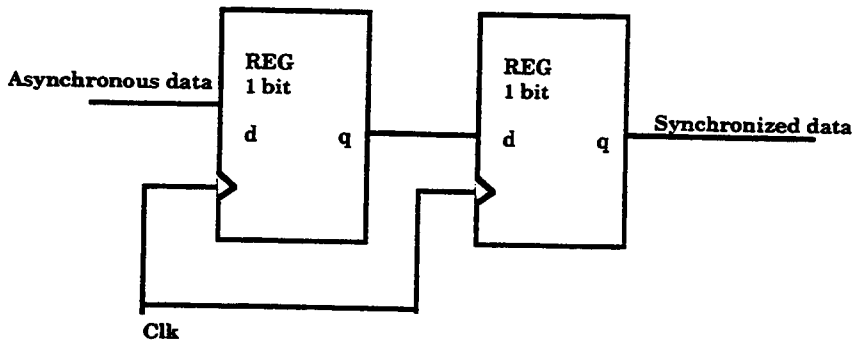


Fig 2.5 A typical register based synchronizer

2.6 The Metastability Problem in Asynchronous Systems

From section 2.4, the cause of metastability in asynchronous systems has been previewed. This section will further look at its effects in asynchronous systems. Referring to Fig.1.6, there are four stages in the FIFO micropipelines. If the first stage enters into the metastable state, then the Q from first to second stage will be delayed (typical 20ns) due to the metastability. Even though the second stage processes the data smoothly, the third stage has to wait the extra delayed time caused by the metastability in the first stage. Both the performances of latency and throughput rate of the micropipelines will decrease dramatically when one of those stages suffers from metastability.

2.7 Summary

This chapter has introduced the metastability of bistable circuits. Also, we notice that the metastability problem does exist whenever there is the interface between synchronous and asynchronous system or the data flowing in the stages of asynchronous systems.

Chapter 3

THE DESIGN OF TRUE-Q FLIP FLOP

3.1 The Introduction of Double-Edge Triggered Flip-Flop

The double-edge triggered flip flop [5. Lu 90] can be used as a storage element in 2-phase system, which has been described in chapter 1. The conventional edge-triggered flip-flop is for evaluating either the data within the rise time, or the data within the fall time. The double-edge triggered feature makes DETFF become a suitable storage element in Micropipelines.

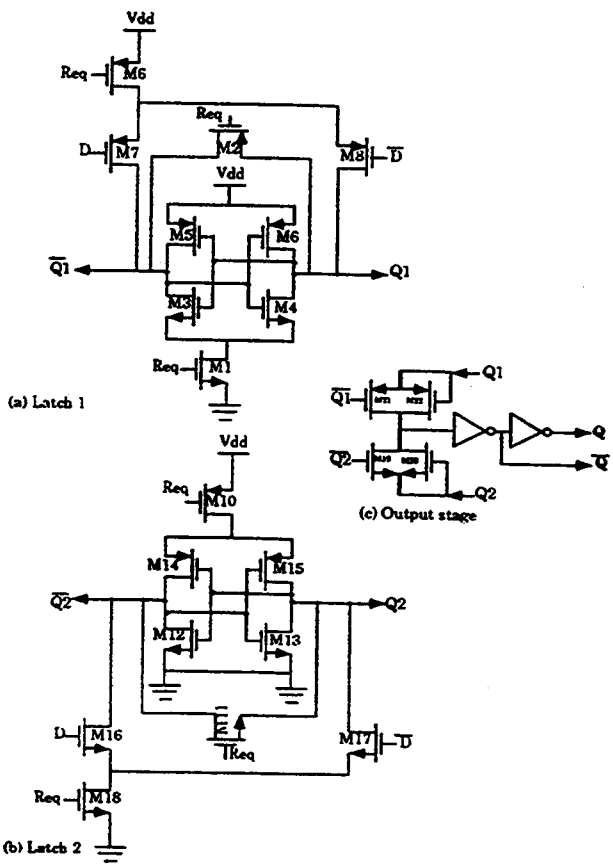


Fig.3.1 The Double -Edge triggered flip flop

3.1.1 The Operation of Double-Edge Triggered Flip-Flop

The hardware configuration of DETFF is shown on Fig.3.1. There are 26 transistors used to implement the DET flip flop which consists of two latches and an output stage. The first latch shown on Fig.3.1(a) and the second latch shown on Fig.3.1(b) are used to evaluate the input data during the rising and trailing edges respectively. Before the rising transition, M9 and M2 are enabled and thus q1 and nq1 are both at vdd. M3 and M4 are also on and thus Vx is equal to vdd-vtn. M1 will go to the saturation region once the request signal is greater than Vtn. Therefore, Vx is being discharged by M1 at that moment. Also, M3 and M4 will turn on and thus discharge q1 and nq1. Remember that the rise time of request signal is used to evaluate the D-input. If the D-input is high, q1 will be charged by M7. Similarly, if the D-input is low, nq1 will be charged by M8. Either case will result in the voltage or logic difference between q1 and nq1. Then, latch 1 finishes its process when Request signal reaches Vdd. Now latch 2 will take over the data evaluation job from latch 1, which keeps the values of q1 and nq1. M18 and M11 are on before trailing edge. Therefore, q2 and nq2 are at ground and latch 2 is said to be disabled before trailing edge. During the trailing transition, latch 2 is enabled once the request signal falls to Vdd-vth(p). M10 is on when request signal lies between Vdd-vth(p) and ground. M18 will go to off when the request signal is lower than vth(n). Either M16 or M17 will be on and thus either q2 or nq2 is discharged. So the trailing time between Vdd-vth(p) and Vth(n) must be large enough to let latch 2 evaluate data properly. The output stage is formed by two transmission gates and two inverters. The table 3.1 shows the logic truth table.

Request signal	Input q1 nq1	Input q2 nq2	Output q	Output nq
0v-->5v	5v 5v	q2 nq2	q2	nq2
5v-->0v	q1 nq1	0v 0v	q1	nq1

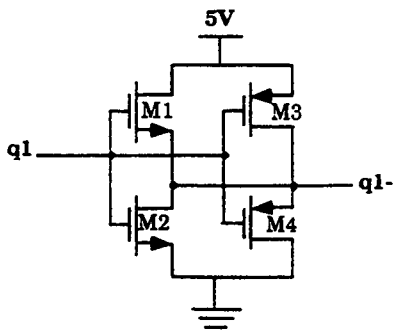
Table 3.1 Logic truth table of the final output

3.2 The Metastable Hazard on DETFF

Since DETFF is a bistable Flip Flop, so a metastable hazard will happen on it under some conditions. Those conditions are shown graphically on Fig.2.4. The "undesired digital" output , 2.5v, will probably stay on nq1 and q1 (or nq2 and q2) if request signal is rising (or falling). Actually, the metastability problem of DETFF can also be explained by section 2.4.

3.3 The Introduction of the Delta Voltage Circuit

The Delta Voltage circuit shown in Fig. 3.2 is to convert either the digital input (0v or 5v) or the metastable voltage (2.5v) to the desired voltages. The Table 3.2 and 3.3 tabulate the transistors' parameters and the voltage values of Delta Voltage circuit with the corresponding inputs respectively. The operation of this circuit will be explained according to the input voltage. When the input is 0v, M3 and M4 will operate on linear and saturation region respectively. The output voltage is 2.5v. If the input is 5v, then M1 will be on saturation while M2 will operate on linear region. The output voltage will give 2v, from which both Vds of M1 and M2 reach equal value under 5v input. Similarly, the 2.5v input will allow both M2 and M3 on saturation and M1 on linear region. The output voltage is 1v.



W1=20u L1=2u	W2=4u L2=2u
W3=4u L3=2u	W4=20u L4=2u

Fig.3.2 Delta Voltage Circuit

Table 3.2 The parameters of Delta Voltage

Input to Delta voltage circuit	Output from Delta voltage circuit
5V	2v
0V	2.5v
2.5V	1v

Table 3.3 The voltage inputs and outputs of Delta voltage circuit

3.4 The Introduction of Comparator Operation

A comparator is used to detect two large analog DC signals from the two inputs and figure out which input is larger. For non-inverting (inverting) comparators, if positive side input is greater (smaller) than the negative side input, then the DC signal output will go to Vdd (Vss) and vice versa.

3.4.1 The Characteristics of Comparator

The resolving capability, propagation delay, input common-mode range and offset voltage are the four main parameters for distinguishing the performance of a comparator.

Ideally, the gain of a comparator should be infinite and the resolving capability be unlimited too. In reality, a comparator always has a finite gain. The comparator's gain

can be improved by either adjusting the comparator design itself or sizing the transistors properly.

The propagation delay in a comparator indicates how fast is it can work. The propagation delay in a two stages comparator can be improved by either increasing the slew rate or decreasing the output swing in the output stage. If gain is not a critical factor, we can use as few stages as possible. A single differential stage comparator is always faster than a two stage comparator, which has an added output stage to the single stage differential pairs. Therefore, there is a tradeoff between propagation delay time and gain in a comparator. The performance requirement in a comparator is a critical factor for deciding how much gain and propagation delay are in a comparator.

The input common-mode range is defined by the input voltage range, over which both differential input pairs remain in saturation.

Ideally, the comparator will give Vss if both inputs are grounded. However, both input devices mismatch and systematic mismatch will contribute this abnormal output, above Vss. The added voltage, which is called offset voltage, is applied on one of the inputs to compensate for the mismatch problems so that the output comes back to Vss again.

3.4.2 The Design of the Comparator in True Q Flip Flop

There are four comparators used in True Q Flip Flop. Each comparator receives one analog and one digital input. The analog input of comparators comes from the Delta Voltage circuit, from which 5v and 0v input will give 2v and 2.5v out respectively. Considering DETFF under metastable state, Delta voltage circuit changes 2.5v input to 1v output which will give 1v out. Obviously, even a single stage of a differential operational amplifier can provide such resolving capability. So we should put more effort on the

improvement of propagation delay and the optimization of transistor numbers. The input common-mode range can be solved by appropriate sizing of those transistors parameter. The offset voltage is not a problem for True Q Flip Flop because there exists non zero input (greater than offset voltage) to the comparators at all time.

3.4.3 The Introduction of Differential Amplifier

Referring to the Fig. 3.3, the differential amplifier is a good choice to be used in True Q Flip Flop. It not only can provide sufficient gain to the circuit , but also can give high speed and low transistor count. M3 and M4 are current mirror and provide current source to the comparator. M5 is biased by Vbias so that it will give 200uA current sink to the comparator totally. M1 and M2 are sized so small that they provide small capacitor load to DETFF. Ibias is 200uA, which can provide a reasonable slew rate to the output. The detail parameters are summarized on table 3.4.

L1=L2=2um; W1=W2=5um	Ibias=200uA
L3=L4=2um; W3=W4=5um L5=2um; W5=10um	Vbias=1.98v

Table 3.4. The parameters for the single stage differential comparator

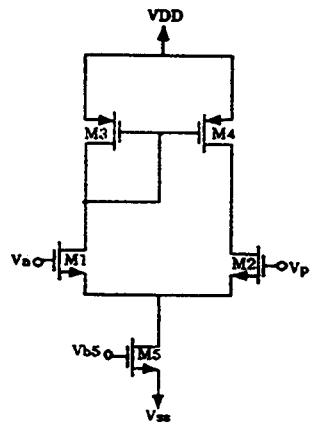


Fig. 3.3 The single stage differential comparator

3.5 The Introduction of Exclusive Or and Exclusive Nor Circuits

The Xor and Xnor circuit shown on Fig.3.4 use transmission gate implementation. The truth table for Xor and Xnor are tabulated on Table 3.5. Both Xor and Xnor use 8 transistors to implement. The Xor output will give 1, once q1 and nq1 from DETFF are firmed. While Xnor circuit is responsible for detecting whether q2 and nq2 have been processed by DETFF or not.

Input a	Input b	Xor output	Xnor output
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Table 3.5 The truth table of Xor and Xnor circuit

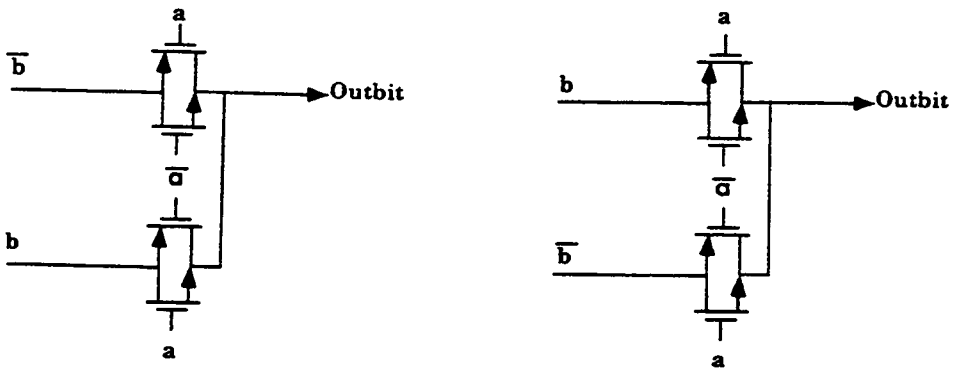


Fig.3.4 The implementation of Xor and Xnor gates by using CMOS transmission gate

3.6 The Introduction of Muller-C Element

The Muller-C element provides the AND function for events. The basic operation is for causing the output to follow the matched inputs only and will not change if both inputs are different values. It means that its output is latched under different inputs. Remember that, static CMOS AND gate does not have this data storage feature, which is the main difference between Muller-C and CMOS AND gate. The Fig. 3.5 shows its transistor level circuit. Also, Muller-C will change state only when two inputs or events have reached at it. This feature is necessary for asynchronous inputs.

The logic truth table and equation are shown on Table 3.6.

Input X	Input Y	Output Z
0	0	0
1	0	no change
0	1	no change
1	1	1
$Z=XY+(X+Y).Z^{(n-1)}$		

Table 3.6 The truth table of Muller-C Element

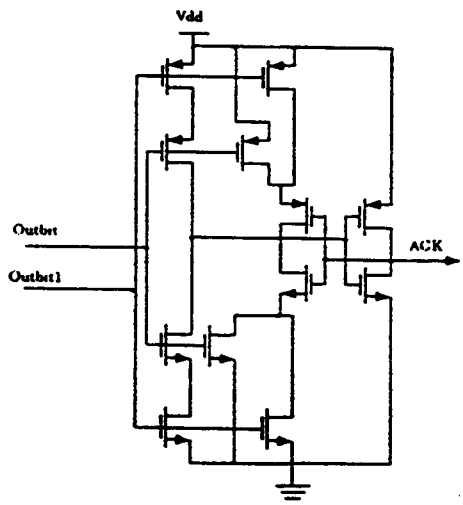


Fig. 3.5 The Muller-C element

3.7 The Introduction of True-Q Flip Flop

From the section 2.5 and 2.6, we know that the existence of metastability inside a bistable machine affects the performance of synchronization between two different clocked systems and the data flow of asynchronous system. This section suggests a solution to reduce the metastable hazard in DETFF. The block diagram shown in Fig.3.6 is an Asynchronous True-Q flip flop, which is made up of two Delta Voltage, four single stage

differential comparators, one Xor gate, one Xnor, a Muller-C element and a DETFF. Their operations will be explained in this chapter.

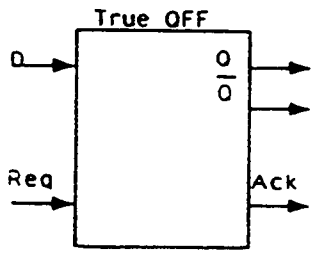


Fig. 3.6 An asynchronous True-Q Flip Flop

3.7.1 The Design Methodology of True-Q Flip Flop

Under metastable state, both q and nq stay on about 2.5v for a while and then resolve to either 0V or 5V. Some additional circuits are added to DETFF. They prevent the subsequent stage from using those defected digital signals. The basic operations of the circuit block shown on Fig. 3.7 are introduced briefly in here and discussed in detail in following sections. Firstly, there are two pairs of comparators. The first pair is used to test whether q1 and nq1 from DETFF had been completed or not during rising edge of the request signal. Once their values are normal (0 or 5v), a and b values will be either 01 or 10 such that the outbit will give 1. At the rising edge, both q2 and nq2 are at 0, so that outbit1 gives 1. The second pair works for evaluation of the validity of q2 and nq2 during the trailing edge of the request signal. If both q2 and nq2 are ready, the values of a1 and b1 will give either 01 or 10 and thus outbit1 is 0. If not, both a1 and b1 will be 0 or 1 such that outbit1 gives 1. At the trailing edge, both q1 and nq1 are at 5v such that outbit is 0. The purpose of using Delta-Voltage blocks is to create a desired voltage difference between the comparators' inputs under various values of q1, q2, nq1, and nq2. The

Muller-C element provides AND event logic function. It allows Acknowledge signal going to 5v if both its inputs are 5v. Similarly, the Acknowledge signal will fall down to 0v if both its inputs are 0v. Now, let us understand how this circuit can handle metastable state problems in DETFF. The Delta-Voltage, which does critical work under metastable state, alters 2.5v to 1v. Then, outbit and outbit1 will give 0 and 1 respectively. Therefore, the Acknowledge signal is unchanged until the metastable state is passed.

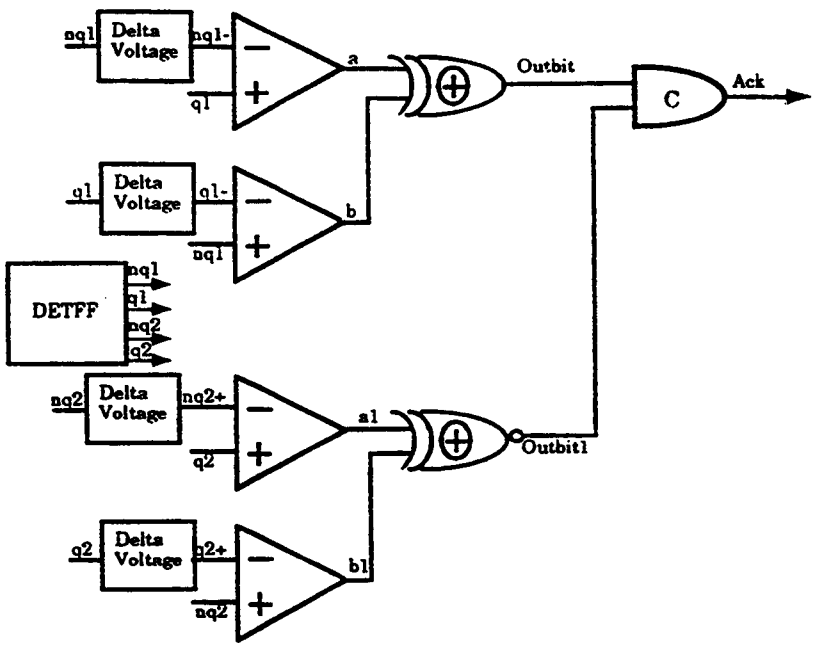


Fig. 3.7 The hardware architecture of Asynchronous True Q Flip Flop

3.7.2 The Solution to eliminate the Metastable Hazard from DETFF

The acknowledge signal shown on Fig 3.7 will not be given out by the True-Q flip flop unless the hardware conditions created by four comparators, a xor, a xnor and a Muller-C element are satisfied. The conditions, which will or will not allow a acknowledge signal out, are tabulated as shown on table 3.7.

inputs\outputs	q1-/nq1-	q2+/nq2+	a/b	a1/ b1	outbit	outbit1	Ack.
q1&nq1=5v q2=0v(5v) &nq2=5v(0v)	2v/2v	2.5v(2v)/ 2v(2.5v)	1/1	0/1 or 1/0	0	0	low
q2&nq2=0v q1=0v(5v) &nq1=5v(0v)	2.5v(2v)/ 2v(2.5v)	2.5v/2.5v	0/1 or 1/0	0/0	1	1	high
Metastable state: q2&nq2=2.5v q1&nq1=5v	2v/2v	1v/1v	1/1	1/1	0	1	same
Metastable state: q1&nq1=2.5v q2&nq2=0v	1v/1v	2.5v/2.5v	1/1	0/0	0	1	same

Table 3.7 The table for all possible inputs and outputs in True QFF

3.7.3 The Applications of True-Q Flip Flop

In section 2.5 and 2.6, metastability problems involved in synchronization failure in synchronizers and degraded performance in Micropipelines are investigated. This section suggests some solutions to ease those problems are caused by metastability. Fig. 3.8 shows that the synchronizer, which is made of a True-Q flip flop, a DETFF and a Muller-C element., is capable of giving 0% synchronization failure. Its operations are explained as follows. The Acknowledge signal is given from True-Q flip flop only when q is ready. The DETFF receives q from True-q flip flop when the conditioned clock signal from Muller-C element has arrived. The added True-Q flip flop provides the synchronizer processing data with 0% synchronization failure.

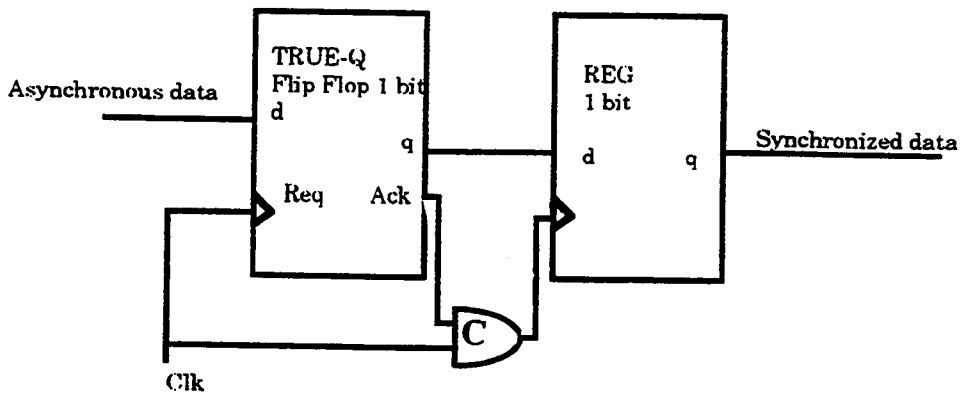


Fig. 3.8 Synchronizer installed with True-Q flip flop

The metastability problem in 2 cycle FIFO Micropipelines has been discussed in section 2.6. If those storage elements shown on Fig. 1.6 are substituted by True-Q flip flop, the delay time caused by metastability in any of the stages would not be cascaded to the following stages. Therefore, latency and throughput rate of Micropipelines are maintained almost the same.

3.7.4 The Overall Performances of True -Q Flip Flop

For digital circuits, time delay in a circuit mostly dictates its performance. Also, transistor count in a circuit should be kept as small as possible so as to save both area and cost of chip. However, the transistor count will increase when more features are added to the circuit. The added hardware in DETFF makes it become an Asynchronous True Q Flip Flop, which can improve the performance of synchronizer and keep the data flowing smoothly in Micropipelines. Unfortunately, it becomes rather expensive because more

transistors are used in the circuit. Nevertheless, it is worth paying more if the circuit's reliability is considered as a critical factor. That is the same reason why those motor car installed anti-lock brakes are more expensive than those installed regular brakes.

The total number of transistors used in True QFF are tabulated as shown below:

	DETFF	Delta voltage	Comp.	xor	xnor	Muller C	
no. of transistors per each	26	4	5	8	8	12	
no. of quantity	1	4	4	1	1	1	
Total of transistors used	26	16	20	8	8	12	Sum= 90

Table 3.8 The transistors used in various components

On the other hand, speed in a circuit will decrease to some extent by the additional hardware. The time delay from the Request to the Acknowledge signal is 6.5ns.

3.8 Summary

The hardware design of True-Q flip flop has been discussed in details. The applications and performances of True-Q flip flop are mentioned. The storage elements inside Micropipelines and synchronizer circuit created by True-Q flip flop, can suppress the metastability problem significantly and thus improve their performance dramatically.

Chapter 4

SIMULATION RESULTS

4.1 The Simulation Tools Used

HSPICE is used as a simulation tool in this paper. Transients and DC analysis are applied to test all circuits. The Level 3 CMOS transistor model is used throughout all the simulation in this paper. Only some transistors in DETFF are sized for giving same driving capability to the q1 and q2. All the other digital circuits use the minimum size, which are w=4u and l=2u. On the other hand, those analog circuits like Delta Voltage and Comparator are sized appropriately for getting the best performance. The simulation results will cover timing analysis, DC characteristics and transient analysis in each part of True-Q Flip Flop. All HSPICE files are shown in Appendix A. The device models are shown in Appendix B.

4.2 The Simulation Result of DETFF

The HSPICE simulation results for DETFF is shown in Fig. 4.1.

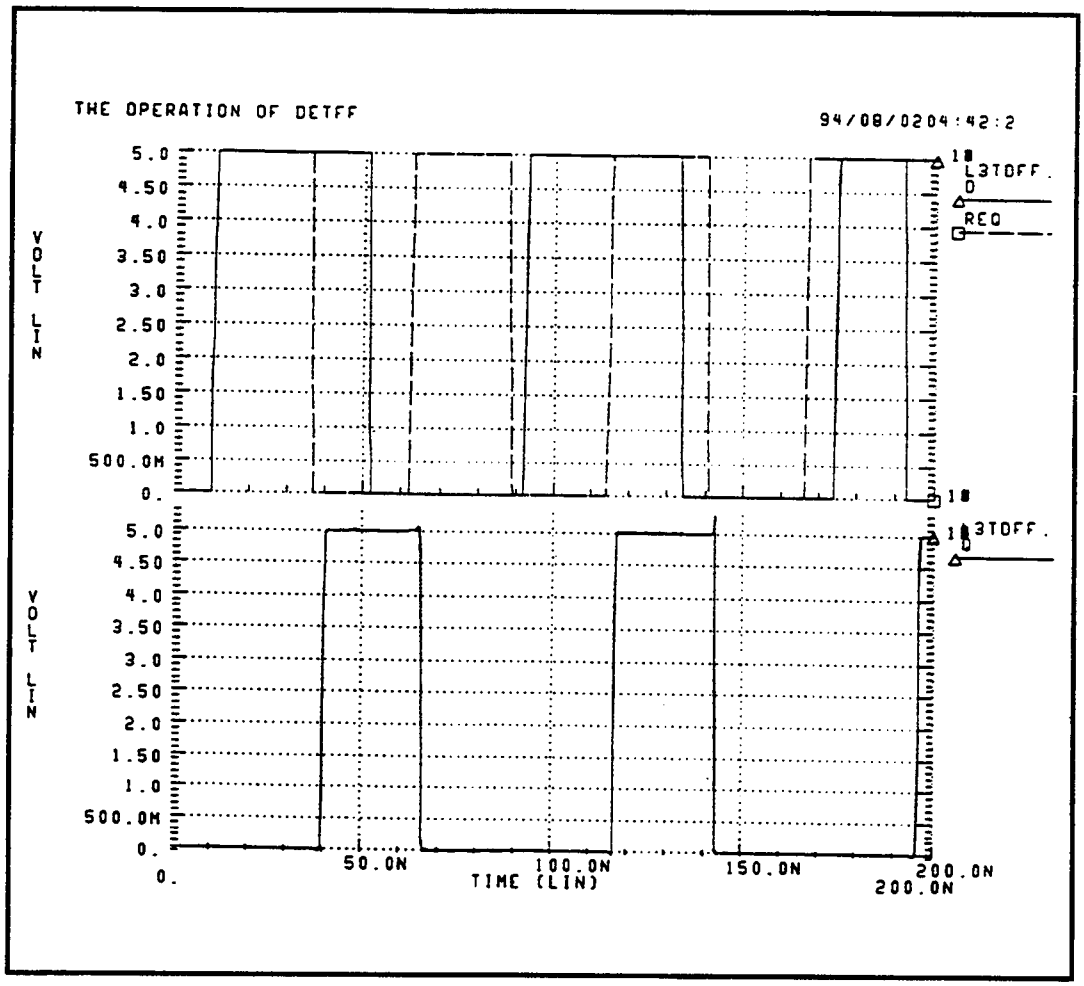


Fig 4.1 The transients analysis of DETFF

Notice that Latch 1 and Latch 2 are properly sized (referring to Appendix A pg.36) for requiring them to have the same driving capability on the next stage. Therefore, q1 and q2 have almost the same time delay, which is very important since the state of Muller-C AND will not change until both inputs are matched.

4.3 The Simulation Results for DC Analysis of Delta Voltage Circuit

Referring to Fig. 4.2, DC simulation result shows that the input and output voltage of Delta Voltage fellow the decided voltage closely. Sizing M1, M2, M3 and M4 is a short cut method to get and alter the DC characteristic in this circuit.

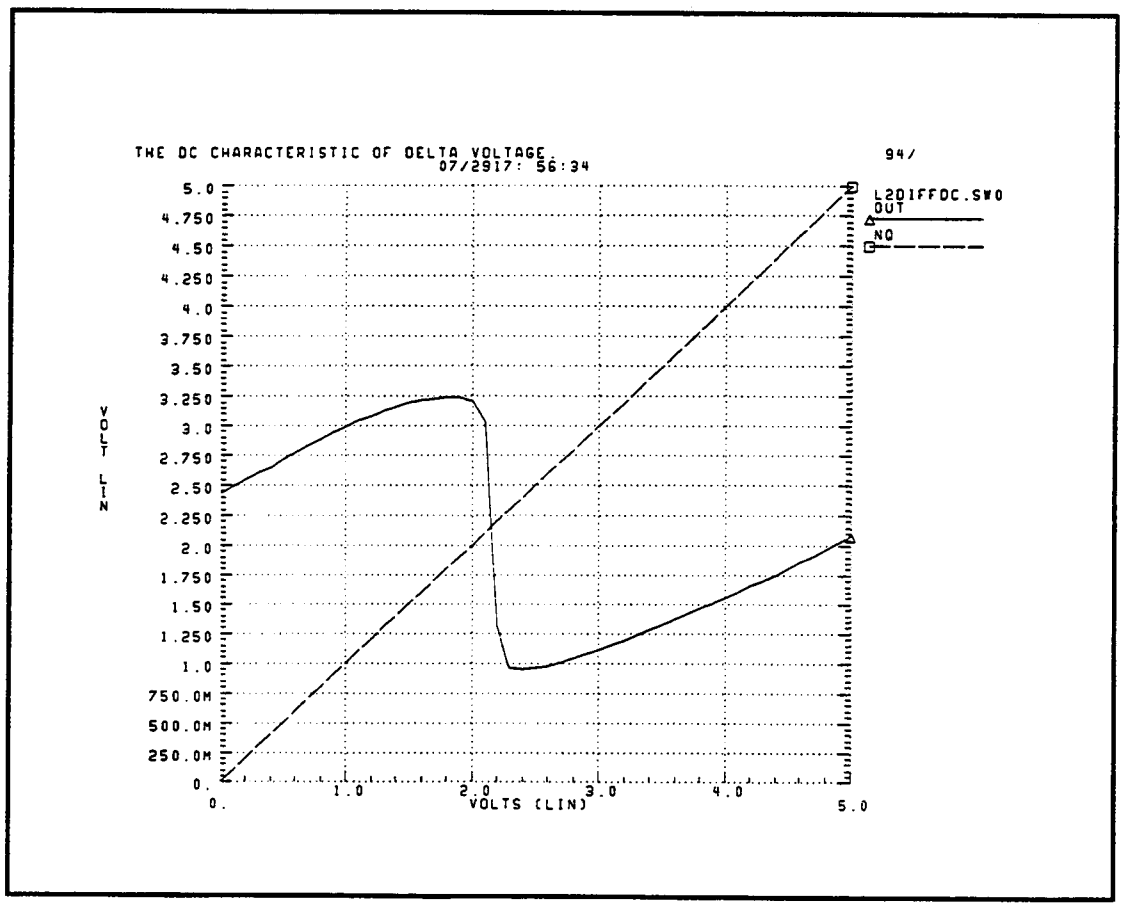


Fig 4.2 The DC characteristic of Delta Voltage

4.4 The Simulation Results of Single Stage Differential Comparator

Transient analysis of comparator is shown on Fig 4.3.

The Table 4.1 summarizes four main parameters of the comparator, from which we know its performances.

Gain	80
Propagation delay	Typical 1ns
Input Common Mode Range	3.1V
Offset Voltage	220mV

Table 4.1 The parameters of the comparator

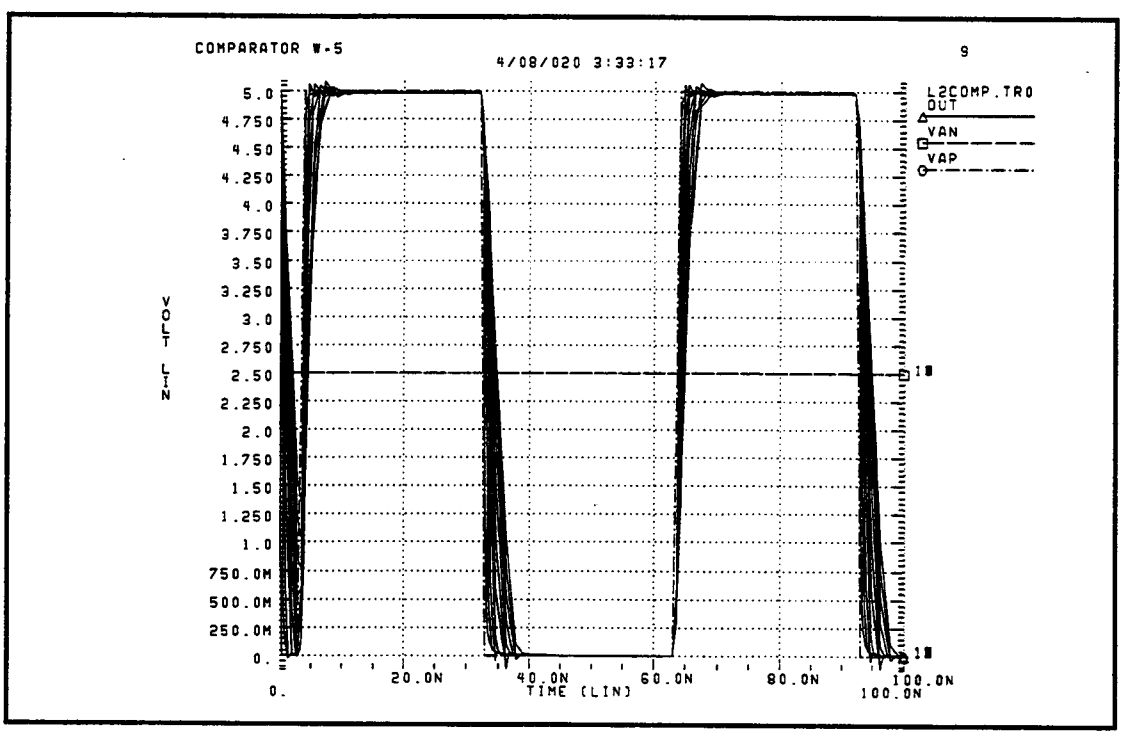


Fig. 4.3 The operation of the comparator

Gain is estimated by decreasing the voltage difference between two inputs until output has no response to the difference inputs. Then, gain can be calculated by gain = $5V/\Delta V$, which is found about 80. Typical propagation delay, which is about 1ns, can be read by Fig 4.4.

Cload(pf)	Rise time(ns)	Fall time(ns)
0	0.274	0.33632
0.01	0.40523	0.58225
0.02	0.51392	0.80511
0.03	0.64439	1.019
0.04	0.748	1.223
0.05	0.84748	1.4241
0.06	0.94794	1.6163
0.07	1.0492	1.8081
0.08	1.1691	2.0001
0.09	1.2547	2.1938
0.1	1.3601	2.3967

Table 4.2 Timing table for Comparator

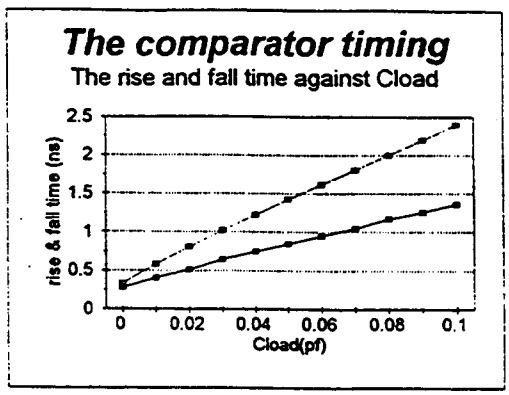


Fig. 4.4 The rise and fall time of the comparator

4.5 The Simulation Results of Xor and Xnor Gates

The transient analysis of Xor and Xnor are presented on Fig 4.5 and Fig 4.6 respectively.

Their rise and fall times are represented by Fig 4.7 and Fig 4.8 respectively. Those data are tabulated on Table 4.3 and Table 4.4 respectively.

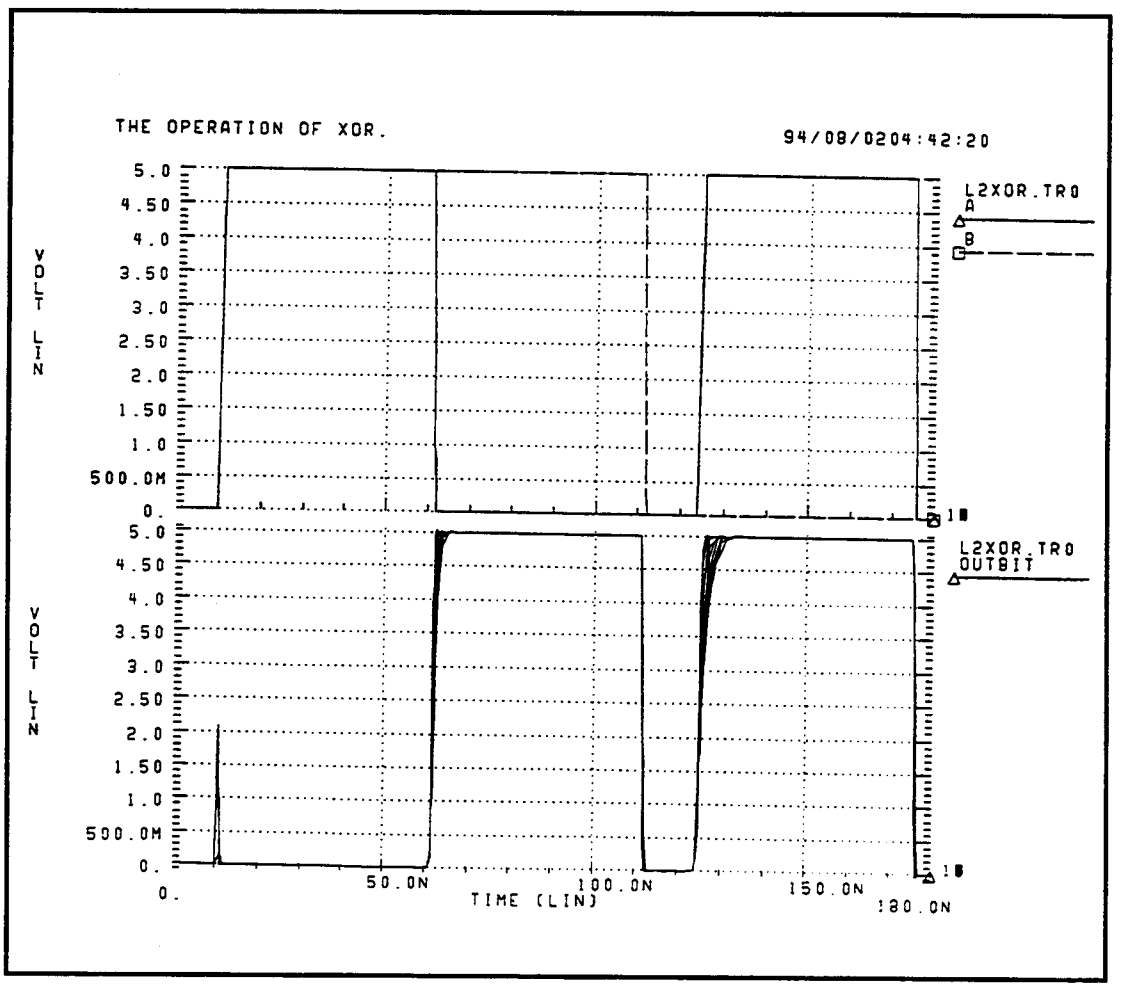


Fig 4.5 The transient analysis of Xor

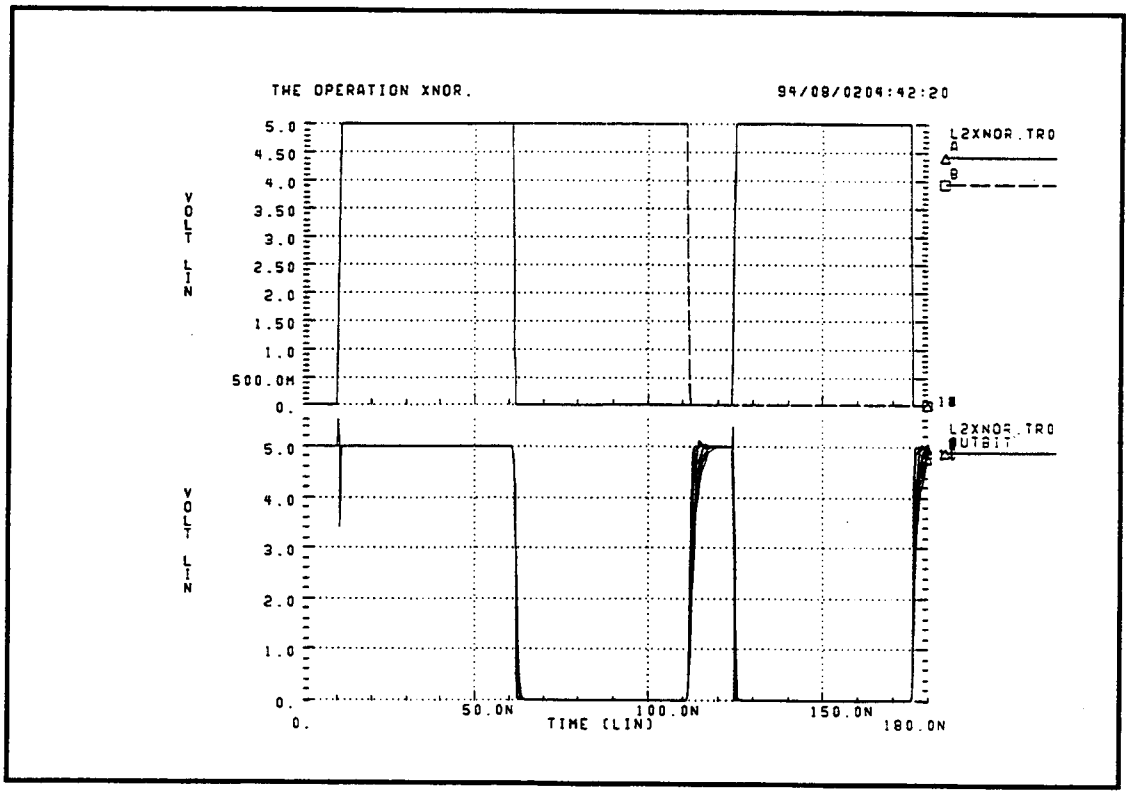


Fig. 4.6 The transient analysis of Xnor

Cload (pf)	Rise time(ns)	Fall time(ns)
0	0.78251	0.82245
0.01	0.97204	0.84723
0.02	1.1882	0.87338
0.03	1.3298	0.89717
0.04	1.5374	0.96256
0.05	1.6978	1.0182
0.06	1.8159	1.059
0.07	1.9922	1.1035
0.08	2.1148	1.151
0.09	2.2942	1.193
0.1	2.4673	1.2328

Table 4.3 Timing table for Xor

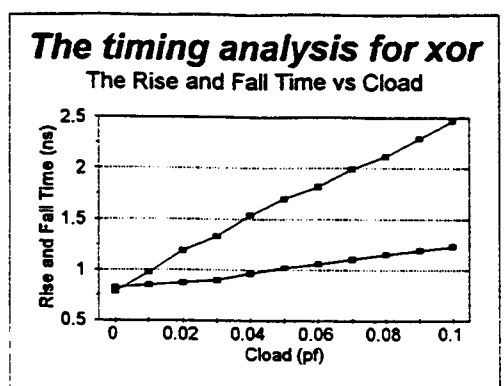


Fig. 4.7 The rise and fall time of Xor

Cload (pf)	Rise time(ns)	Fall time(ns)
0	0.4559	1.0443
0.01	0.78502	1.1669
0.02	1.051	1.2568
0.03	1.6169	1.4
0.04	1.838	1.4495
0.05	2.1253	1.5874
0.06	2.2693	1.6483
0.07	2.8	1.7685
0.08	3.0208	1.9051
0.09	3.2181	2.0594
0.1	3.4103	2.0535

Table 4.4 Timing table for Xnor

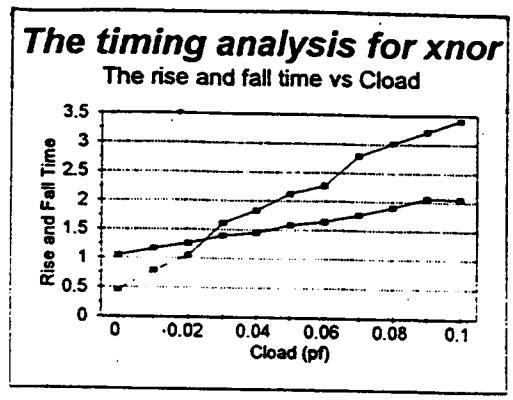


Fig. 4.8 The rise and fall time of Xnor

4.6 The Simulation Results of Muller-C Element

The transient analysis of Muller-C element shown on Fig 4.9. Also, its rise and fall time with varying capacitor load are shown on Fig. 4.10.

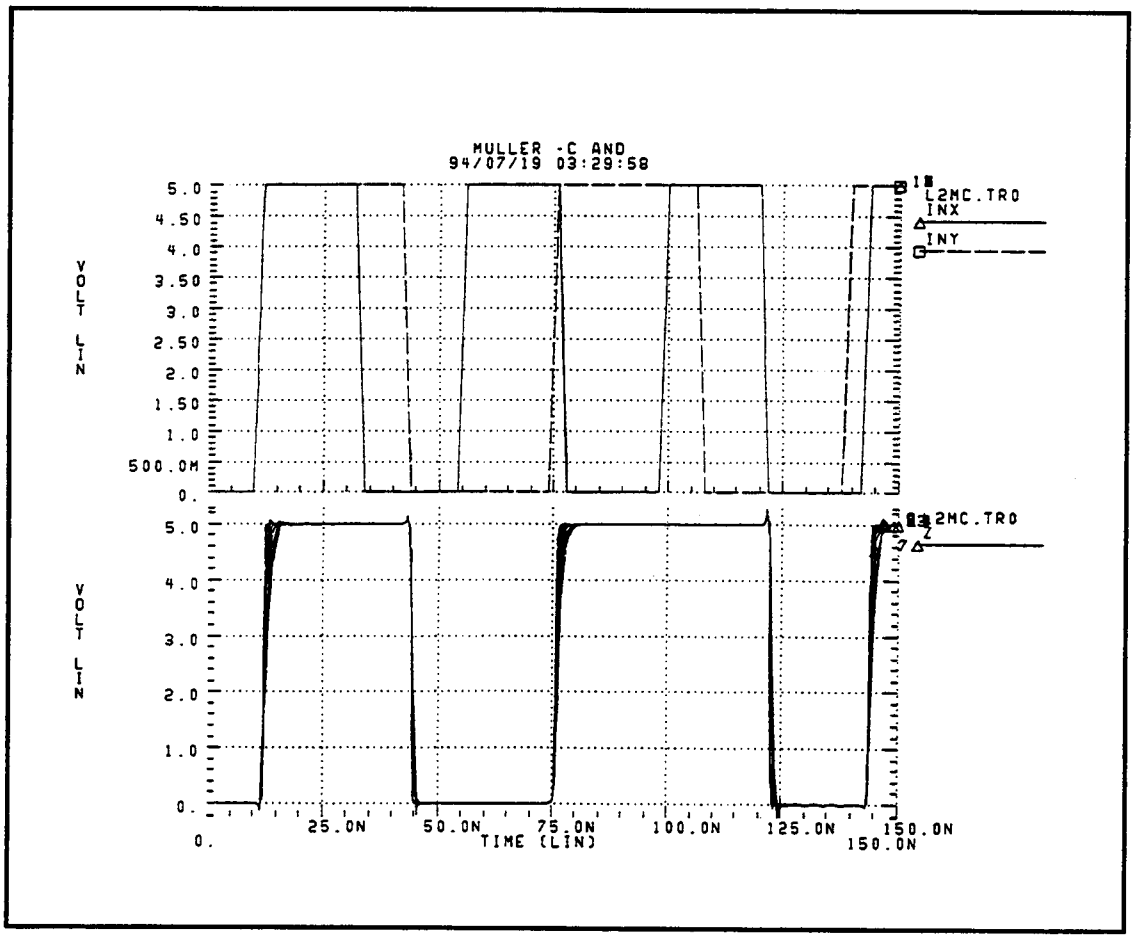


Fig. 4.9 The transient analysis of Muller-C element

Cload (pf)	Rise time(ns)	Fall time(ns)
0	1.7717	2.1778
0.01	2.0096	2.312
0.02	2.3006	2.4481
0.03	2.4644	2.5379
0.04	2.5766	2.7182
0.05	2.7492	2.8267
0.06	2.994	2.9018
0.07	3.1242	2.9601
0.08	3.3201	3.0304
0.09	3.476	3.081
0.1	3.672	3.1313

Table 4.5 Timing table for Muller-C element

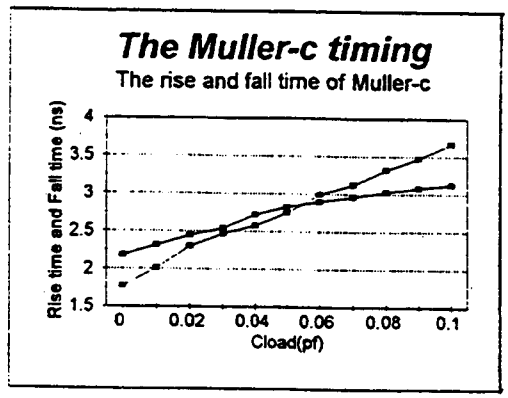


Fig. 4.10 The rise and fall time of Muller-C element

4.7 The Simulation Results of True-Q Flip Flop

The Fig. 4.11 demonstrates the operation of True-Q flip flop. The typical delay of True-Q Flip Flop is measured as 6.5ns.

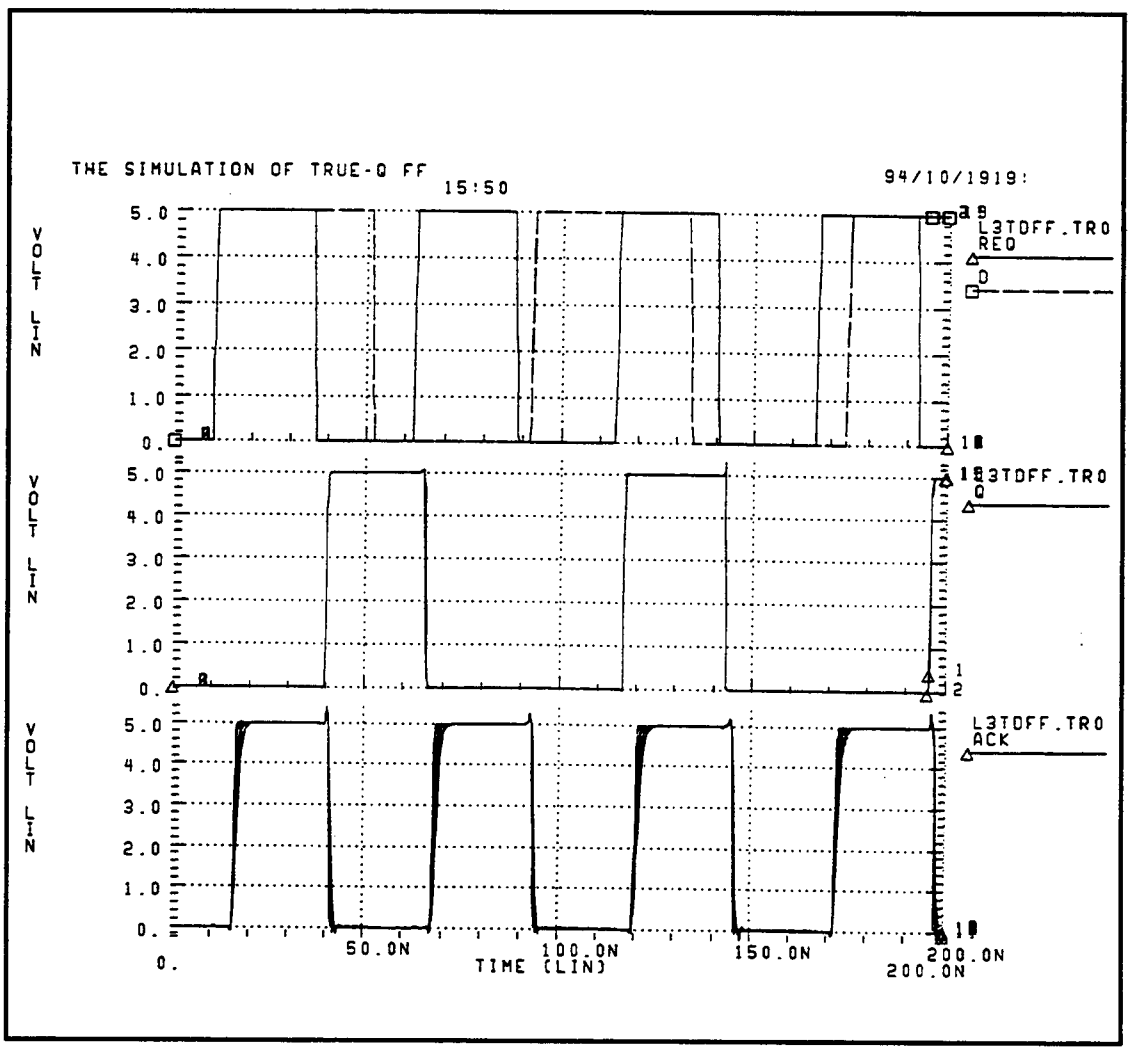


Fig 4.11 The operation of True-Q Flip Flop

The timing analysis of True-Q Flip Flop are represented by Table 4.6 and Fig. 4.12.

Cload(pf)	Rise time(ns)	Fall time(ns)
0	6.1605	5.5564
0.01	6.4304	5.6254
0.02	6.6304	5.571
0.03	6.7905	5.8717
0.04	7.0307	5.8808
0.05	7.2442	6.0247
0.06	7.3865	6.0646
0.07	7.5728	6.1219
0.08	7.9079	6.3012
0.09	8.1312	6.4409
0.1	8.2831	6.5176

Table 4.6. Timing table for True-Q Flip Flop

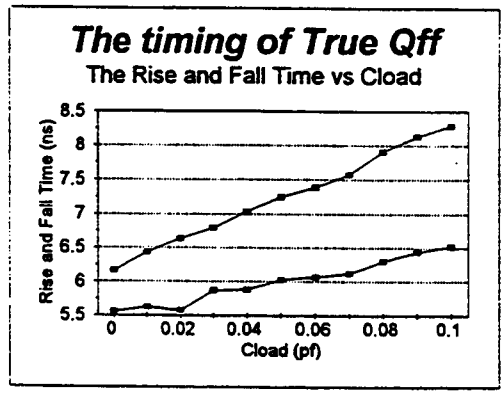


Fig. 4.12 The rise and fall time of True-Q Flip Flop

4.8 Simulation Of True-Q Flip Flop under Metastable State

In HSPICE, metastable state of Q and NQ cannot be created by adjusting time delay between Data and Request signals. In other words, simulation tools cannot create metastable state, but it actually does exist in some digital systems.

So the metastabled signals of q1, nq1, q2 and nq2 are created by PWL commands in HSPICE so that the circuit performance under metastable state still can be seen. PWL commands allow those signals staying at 2.5V for a certain time and then resolve to either 0V or 5V.

The Fig. 4.13 shows that True-Q Flip Flop does have the capability to handle those metastable inputs. Notice that acknowledge signal is still 'clean' under such 'unclean' inputs.

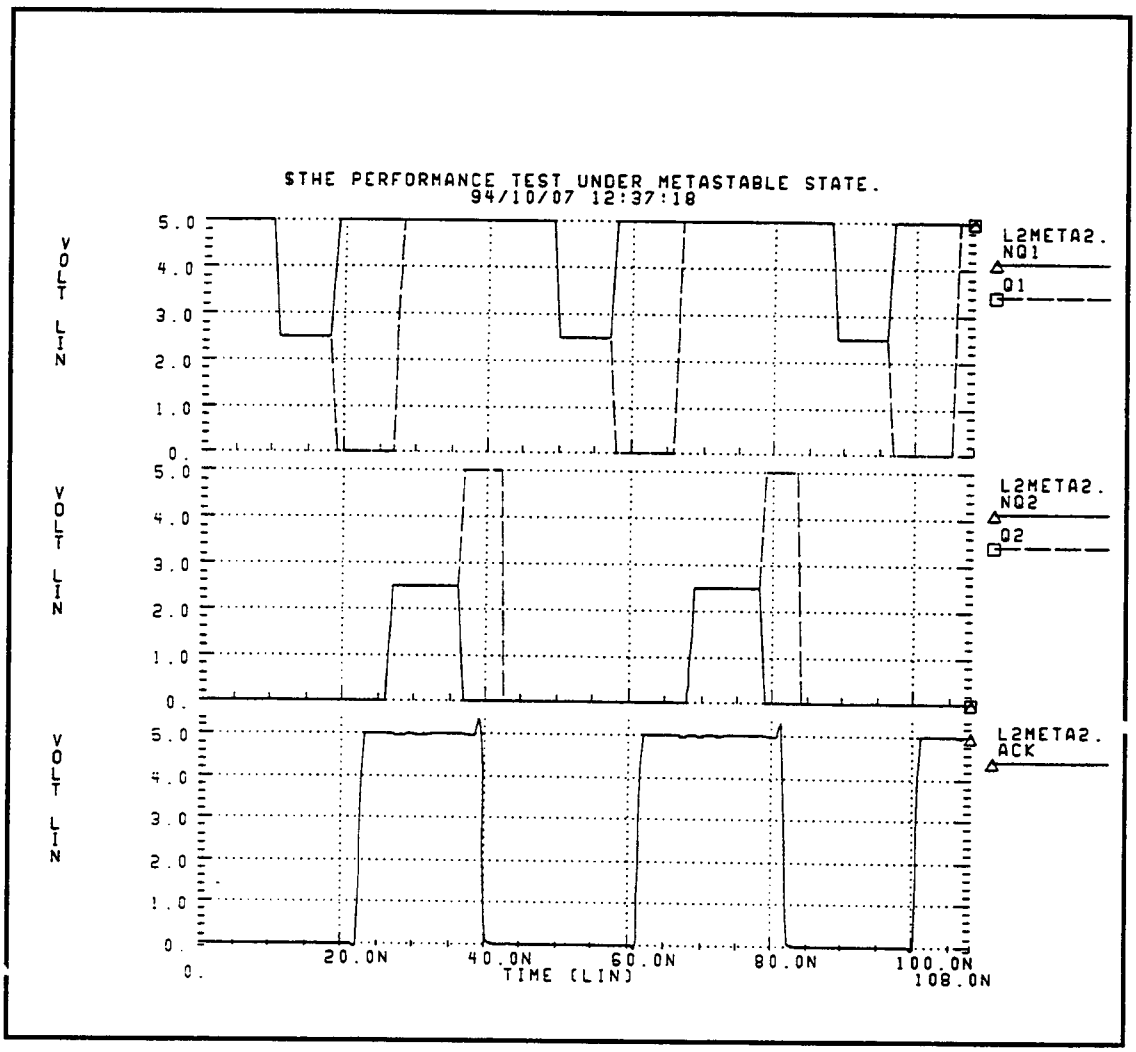


Fig. 4.13 The behaviors of True-Q flip flop under metastability

4.9 Summary

The HSPICE simulation results have been shown in this chapter. The simulation results cover timing analysis, DC characteristics and transient analysis in each part of the True-Q Flip Flop. Since those simulated results are matched to the expectation results, the design of True-Q Flip Flop is verified.

Chapter 5
CONCLUSIONS

5.1 Conclusions

Asynchronous system design is predicted to be more popular because of the advance of the VLSI technology. The 2-cycle FIFO Micropipelines is widely used as asynchronous pipeline. Metastability problems exist in the clocked systems interfacing with asynchronous inputs and the event storage elements in Micropipelines. The metastability problem affects the performances and reliability of the synchronizers and Micropipelines.

The True-Q Flip Flop is designed for suppressing the metastability problem in the Micropipelines and synchronizer. A synchronizer implemented by True-Q Flip Flop can have the performance of 0% synchronization failure. The True-Q Flip Flop can be used in a Micropipelines as storage elements so that the Micropipelines can maintain good performances even though one of its stages enters metastability.

Due to the complexity of the circuit in True-Q Flip Flop, 90 transistors are used for implementation of True-Q Flip Flop. The typical time delay is 6.5ns from the request to the acknowledge signal.

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APPENDICES

APPENDIX A

HSPICE FILES

A.1 The Hspice input file for DETFF

```
$The macro file of Double Edge Trigger Flip Flop.
.macro l2detffsize q nq q1 nq1 q2 nq2 d req
*First latch
M9 1 req vdd vdd P l=2 w=4
M7 nq1 d 1 vdd P l=2 w=4
M8 q1 nd 1 vdd P l=2 w=4
M2 q1 req nq1 vdd P l=2 w=4
M6 q1 nq1 vdd vdd  P l=2 w=8
M5 nq1 q1 vdd vdd P  l=2 w=8
M4 q1 nq1 vx gnd N l=2 w=4
M3 nq1 q1 vx gnd N l=2 w=4
M1 vx req gnd gnd N l=2 w=8
* Second latch
M10 vy req vdd vdd P l=2 w=16
M14 nq2 q2 vy vdd P l=2 w=8
M15 q2 nq2 vy vdd P l=2 w=8
M12 nq2 q2 gnd gnd N l=2 w=4
M13 q2 nq2 gnd gnd N l=2 w=4
M11 q2 req nq2 gnd N l=2 w=4
M16 nq2 d 2 gnd N l=2 w=4
M17 q2 nd  2 gnd N l=2 w=4
M18 2 req gnd gnd N l=2 w=4
```

```
*Output stage.
M19 q2 nq2 out gnd N l=2 w=4
M20 q2 q2 out gnd N l=2 w=4
M21 out nq1 q1 vdd P l=2 w=4
M22 out q1 q1 vdd P l=2 w=4
M23 nq out vdd vdd P l=2 w=4
M24 nq out gnd gnd N l=2 w=4
M25 q nq vdd vdd P l=2 w=4
M26 q nq gnd gnd N l=2 w=4
*inverter parts.
M27 nd d vdd vdd P l=2 w=4
M28 nd d gnd gnd N l=2 w=4
.oem
```

A.2 The Hspice input file for Delta Voltage.

```
Delta Voltage.
*using level2 MOSFET models.
.inc 'level2'
.option post
+ scale=1u
M1 vdd nq out gnd n l=2 w=20
M2 out nq gnd gnd n l=2 w=4
M3 out nq vdd vdd P l=2 w=4
M4 gnd nq out vdd P l=2 w=20
Vdd vdd gnd 5v
Vnq nq gnd
```

```
.DC Vnq 0 5 0.1
.end

$ The Single Stage Differential Comparator for q1 and nq1 inputs.

.macro l2comp out van vap

M1 1 vap 3 gnd N w=w1 l=l1

M2 out van 3 gnd N w=w1 l=l1

M3 1 1 vdd vdd P w=w1 l=l1

M4 out 1 vdd vdd P w=w3 l=l3

M5 3 vb5 gnd gnd N w=w1 l=l1 M=2

$ Biasing.

Mb5 vb5 vb5 gnd gnd N w=w1 l=l1 M=2

Ib vdd vb5 Ibias

.eom
```

A.3 The Hspice file for single stage comparator

```
$ The Single stage Differential Comparator for q2 and nq2 inputs.

.macro l2comp1 out vbn vbp

M1 1 vbp1 3 gnd n w=w1 l=l1

M2 out vbn 3 gnd n w=w1 l=l1

M3 1 1 vdd vdd P w=w3 l=l3

M4 out 1 vdd vdd P w=w3 l=l3

M5 3 vb5 gnd gnd N w=w1 l=l1 M=2

$Biasing.

Mb5 vb5 vb5 gnd gnd n w=w1 l=l1 M=2

Ib vdd vb5 Ibias

.eom
```

A.4 The Hspice files for Xor and Xnor gates.

```
$Two inputs OR logic gate using CMOS Transmission gate
implementation.
.macro xor outbit a b
M1 outbit  a b vdd P l=2 w=4
M2 outbit na nb gnd N l=2 w=4
M3 outbit na nb vdd P l=2 w=4
M4 outbit a nb gnd N l=2 w=4
$ Two inverters.
M5 nb b vdd vdd P l=2 w=4
M6 nb b gnd gnd N l=2 w=4
M7 na a vdd vdd P l=2 w=4
M8 na  a gnd gnd N l=2 w=4
.eom
$Two inputs XNOR logic gate
.macro l2xnor outbit1 a1 b1
M1 outbit1 a1 nb1 vdd P l=2 w=4
M2 outbit1 na1 nb1 gnd N l=2 w=4
M3 outbit1 na1 b1 vdd P l=2 w=4
M4 outbit1 a1 b1 gnd N l=2 w=4
$ Two inverters.
M5 nb1 b1 vdd vdd P l=2 w=4
M6 nb1 b1 gnd gnd N l=2 w=4
M7 na1 a1 vdd vdd P l=2 w=4
M8 na1 a1 gnd gnd N l=2 w=4
```

```
.eom
```

A.5 The Hspice file for Muller-C element

```
$Muller-C element for implementing AND events function.
.macro mc outbit outbit1 z
M1 d1 outbit vdd vdd P l=2 w=4
M2 d2 outbit1 d1 vdd P l=2 w=4
M3 d2 outbit1 s3 gnd N l=2 w=4
M4 s3 outibt  gnd gnd N l=2 w=4
M5 d5 outbit1 vdd vdd P l=2 w=4
M6 d6 outbit1 gnd gnd N l=2 w=4
M7 d5 outbit vdd vdd P l=2 w=4
M8 d2 z d5 vdd P l=2 w=4
M9 d2 z d6 gnd N l=2 w=4
M10 d6 outbit gnd gnd N l=2 w=4
M11 z d2 vdd vdd P l=2 w=4
M12 z d2 gnd gnd N l=2 w=4
.eom
```

A.6 The Hspice file for True Q-Flip Flop

```
$The True Q Flip Flop Simulation.
* Include those created Macro files.
.inc 'xor'
.inc 'mc'
```

```
.inc 'l2xnor'
.inc 'l2detffsize'
.inc 'l2comp'
.inc 'l2comp1'
$ Parameters of Differential Comparator.
.PARAM Ibias=200u
.PARAM L1=2 W1=5
.PARAM L3=2 W3=5
x1 outbit  a b xor
x2 outbit1 a1 b1 l2xnor
x3 outbit outbit1 ack mc
x4  a van vap l2comp
x5 b vbn vbp l2comp1
x6 a1 van1 vap1 l2comp
x7 b1 vbn1 vbp1 l2comp1
x8 q nq q1 nq1 q2 nq2 d req l2detffsize
*For change the signal names.
r1 vbn1 nq2 1
r2 vbp1 q2+ 1
r3 van1 q2 1
r4 vap1 nq2+ 1
*The Delta Voltage Block.
M1y vdd nq2 nq2+ gnd n l=2 w=20
M2y q2+ q2 gnd gnd n l=2 w=4
M3y q2+ q2 vdd vdd P l=2 w=4
M4y gnd q2 q2+ vdd P l=2 w=20
```

```
$For change signals' names
r5 nq1- van 1
r6 q1 vap 1
r7 q1- vbn 1
r8 nq1 vbp 1
$The Delta Voltage  Block for nq2.
M5y vdd nq2 nq2+ gnd n l=2 w=20
M6y nq2+ nq2 gnd gnd n l=2 w=4
M7y nq2+ nq2 vdd vdd P l=2 w=4
M8y gnd nq2 nq2+ vdd P l=2 w=20
$The Delta Voltage Block for q1
M9y vdd q1 q1- gnd n l=2 w=20
M10y q1- q1 gnd gnd n l=2 w=4
M11y q1- q1 vdd vdd P l=2 w=4
M12y gnd q1 q1-  vdd P l=2 w=20
$The Delta Voltage Block for nq1.
M13y vdd nq1 nq1- gnd n l=2 w=20
M14y nq1- nq1 gnd gnd n l=2 w=4
M15y nq1- nq1 vdd vdd P l=2 w=4
M16y gnd nq1 nq1- vdd P l=2 w=20

*Inputs for transients analysis.
Vreq req gnd pulse (0,5 10n,1n,1n,25n,52n)
Vd d gnd pulse (0,5 10n,1n,1n,40n,82n)
*Capacitor load added to ack output.
Cload ack gnd c1
```

```
* To measure the rise and fall times from request to acknowledge
signal in True Q Flip Flop
.meas tran trise trig v(req) val=0.5v td=2ns rise=2
+              targ v(ack) val=4.5v rise=2
.meas tran tfall trig v(req) val=4.5 td=2ns fall=2
+              targ v(ack) val=0.5v fall=2
*add plot and scale option.
 .option post
+scale=1
.global vdd
Vdd vdd gnd 5v
* CMOS level2 models are used.
.inc 'level2'
*varying the cload from 0pf to 0.1pf with the increment of 0.01pf.
.tran 1ns 200ns sweep cl 0pf 0.1pf 0.01pf
.end
```

A.7 The Hspice file for the metastability test on True-Q Flip Flop

```
$ The performance test under metastable state.
.inc 'xor'
.inc 'mc'
.inc 'l2xnor'
.inc 'l2comp'
.inc 'l2comp1'
$ Parameters of Differential Comparator.
```

```
.PARAM Ibias=200u

.PARAM L1=2 W1=5

.PARAM L3=2 W3=5

x1 outbit  a b xor

x2 outbit1 a1 b1 l2xnor

x3 outbit outbit1 ack mc

x4  a van vap l2comp

x5 b vbn vbp l2comp1

x6 a1 van1 vap1 l2comp

x7 b1 vbn1 vbp1 l2comp1

*For change the signal names.

r1 vbn1 nq2 1

r2 vbp1 q2+ 1

r3 van1 q2 1

r4 vap1 nq2+ 1

*The Delta Voltage Block.

M1y vdd nq2 nq2+ gnd n l=2 w=20

M2y q2+ q2 gnd gnd n l=2 w=4

M3y q2+ q2 vdd vdd P l=2 w=4

M4y gnd q2 q2+ vdd P l=2 w=20

$For change signals' names

r5 nq1- van 1

r6 q1 vap 1

r7 q1- vbn 1

r8 nq1 vbp 1

M5y vdd nq2 nq2+ gnd n l=2 w=20
```

```
M6y nq2+ nq2 gnd gnd n l=2 w=4
M7y nq2+ nq2 vdd vdd P l=2 w=4
M8y gnd nq2 nq2+ vdd P l=2 w=20
$The Delta Voltage Block for q1
M9y vdd q1 q1- gnd n l=2 w=20
M10y q1- q1 gnd gnd n l=2 w=4
M11y q1- q1 vdd vdd P l=2 w=4
M12y gnd q1 q1-  vdd P l=2 w=20
*The Delta Voltage Block for nq1.
M13y vdd nq1 nq1- gnd n l=2 w=20
M14y nq1- nq1 gnd gnd n l=2 w=4
M15y nq1- nq1 vdd vdd P l=2 w=4
M16y gnd nq1 nq1- vdd P l=2 w=20
* PWL inputs
Vq1 q1 gnd pwl 0ns  5 10ns 5, 11ns 2.5, 18ns 2.5, 19ns o, 27ns 0,28ns
+              5,39ns 5,R
Vnq1 nq1 gnd pwl  0ns 5, 10ns 5, 11ns 2.5, 18ns 2.5, 19ns 5, +
   27ns 5, 28ns 5, 39ns 5,R
Vq2 q2 gnd pwl 19ns 0, 26ns 0,27ns 2.5, 36ns 2.5, 37ns 5, 39ns 5, R
Vnq2 nq2 gnd pwl 19ns 0, 26ns 0, 27ns 2.5, 36ns 2.5, 37ns 0, 39ns
+              0,R
.option post
+ scale=1u
.GLOBAL vdd
Vdd vdd gnd 5v
.include 'level2'
```

```
.tran 3ns 100ns

.end
```

APPENDIX B

1.5UM CMOS/BULK LEVEL-2 SPICE PARAMETERS

B1. 1.5um CMOS/Bulk level-2 SPICE parameters

```
.MODEL n NMOS LEVEL=2 LD=0.458388u TOX=280E-10
+ NSUB=3.496105E+16 VTO=0.930261 KP=4.464000E-05
+ GAMMA=0.8759 PHI=0.6 UO=362.246 UEXP=9.499054E-02
+ UCRIT=130365 DELTA=1.00000E-06 VMAX=100000
+ XJ=0.250000U LAMBDA=1.44655E-02 NFS=1.245818E+12
+ NEFF=1  NSS=1.0000E+12 TPG=1.00000 RSH=20.580001
+ CGDO=5.65906E-10 CGSO=5.652906E-10 CGBO=4.291585E-10
+ CJ=4.015000E-04
+ MJ=0.445600 CJSW=5.023000E-10 MJSW=0.270500 PB=0.750000
* Weff = Wdrawn -Delta_w
* The suggested Delta_W is 0.35 um
.MODEL p PMOS LEVEL=2 LD=0.355084u TOX=280E-10
+ NSUB=1.443000E+16 VTO=-0.712799 KP=2.528866E-05
+ GAMMA=0.563231 PHI=0.6 UO=205.063 UEXP=0.357053
+ UCRIT=60449.2 DELTA=1.00000E-06 VMAX=23204.3
+ XJ=0.250000U LAMBDA=6.567991E-02 NFS=8.419363E+11
+ NEFF=1.001  NSS=1.0000E+12 TPG=-1.00000 RSH=77.339999
+ CGDO=4.378947E-10 CGSO=4.378947E-10 CGBO=4.68447E-10
+ CJ=2.156000E-04
+ MJ=0.396400 CJSW=2.663000E-10 MJSW=0.083900 PB=0.530000
* Weff = Wdrawn -Delta_w
* The suggested Delta_W is 0.38 um
```