AN ABSTRACT OF THE THESIS OF

ARTHUR GRAYSON ALBIN for the DOCTOR OF PHILOSOPHY
(Name) (Degree)

in OCEANOGRAPHY presented on March 14, 1968
(Major) (Date)

Title: THE ANALYSIS AND RECOMMENDED DESIGN OF A HIGH-RESOLUTION DIGITAL DATA ACQUISITION SYSTEM FOR THE IN SITU MEASUREMENT OF VARIOUS PHYSICAL AND CHEMICAL PARAMETERS OF SEA WATER

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Abstract approved: _____
Stephen J. Neshyba

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Harry Freund

The lack of availability of a single, complete paper on the analysis of a digital data acquisition system for in situ oceanographic measurements brought about the present work. In order to compile an accurate technical paper on such a complex system, it was necessary to design, construct, and calibrate a system for the in situ measurement of various physical and chemical properties of sea water.

A unique digital encoding circuit was developed which utilizes the basic principles of null balance, resistance ratio bridge and potentiometer measurements. The circuit is a uniquely loaded binary ladder resistance network. Variation of the loading allows resistance

ratio and potentiometric measurements to be made over different ranges with a constant high degree of resolution.

The developed system has the capability of measuring any parameter which can be converted into a varying voltage, current, or resistance. The range over which the measurement can be made is adjustable; and the resolution equals ± 0.006% of the full range value. The resolution is constant over the full range, as a result of the analog-to-digital converter linearity characteristics.

# The Analysis and Recommended Design of a High-Resolution Digital Data Acquisition System for the *in situ* Measurement of Various Physical and Chemical Parameters of Sea Water

by

Arthur Grayson Albin

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

June 1968

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Date thesis is presented March 14, 1968

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# ACKNOWLEDGMENTS

This research was performed under the joint direction of Dr. Harry Freund and Dr. Stephen J. Neshyba. I am grateful to Dr. Freund and Dr. Neshyba for their guidance and assistance throughout this work.

Professor Robert R. Michael and Dr. Kilho Park are to be thanked for their many valuable suggestions.

To the other members of the graduate committee, Dr. W. V. Burt, Dr. June G. Pattullo, Dr. R. L. Smith, and Dr. E. J. Dornfeld, I would like to extend my sincere appreciation.

To my wife, Inga, for her continued encouragement and assistance without which this thesis may never have been written, I am so grateful.

It is to be acknowledged that technical information supplied by Mr. Alec M. Dingee of the Geodyne Corporation has made this investigation possible.

This research was supported by the Navy Office of Naval Research under Contract NONR 1286(10).

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# THE ANALYSIS AND RECOMMENDED DESIGN OF A HIGH-RESOLUTION DIGITAL DATA ACQUISITION SYSTEM FOR THE IN SITU MEASUREMENT OF VARIOUS PHYSICAL AND CHEMICAL PARAMETERS OF SEA WATER

## INTRODUCTION

The many physical and chemical properties of each parcel of sea water in an ocean should be measured continuously and accurately if one is to completely understand the ocean environment. This requirement was almost impossible to attain until the recent advent of digital measuring systems capable of making numerous, highly accurate measurements at an extremely high rate. Oceanographers, unfortunately, have not been able to help in the development or improvement of such systems, as they have difficulties in communicating with the developers. In part, this has been due to the lack of availability of a complete analysis on a digital measuring system from which an oceanographer could attain a basic understanding of this type of data acquisition. An objective of this thesis is to make available, for general use, an analysis of such a system.

Oceanographic in situ measurements are made in a remote and hostile environment. To obtain accurate data at a sufficiently high sampling rate, the analog data is best converted into a digital format by an in situ measuring and encoding system. Invariably, the digital measuring system consists of a transducer to convert the parameter

being measured into an electrical signal, an analog-to-digital converter to encode the analog transducer signal into a digital form, and a display or recorder to monitor or store the digital data.

The analog-to-digital converter and its digital encoding circuitry are the heart of a digital measuring system. The accuracy and stability of the digital data are directly influenced by the characteristics of the analog-to-digital converter. The encoding circuitry and technique are determined, in part, by the type and magnitude of transducer signals to be encoded. This indicates that it is quite important to consider the transducer characteristics along with the analog-to-digital converter, when a digital measuring system is being analyzed or designed. Furthermore, encoding techniques require a finite amount of time to obtain a single measurement, thus making a digital measuring system inherently discontinuous in its method of measurement. To define all variables in both space and time, a digital measuring system should have a sufficiently high sampling rate. Measurements thus obtained are considered to be discretely continuous, as opposed to the continuous measurements obtained by an analog measuring system which does not utilize time-sharing multiplexing techniques.

Oceanographers need real-time information concerning ocean parameters, both at the surface and at depth. When the total expanse of an ocean is taken into consideration, only high speed digital

measuring, telemetering, and computing techniques are capable of performing such a feat. It is, therefore, quite important that oceanographers become proficient in the methods of digital data acquisition.

The availability of a complete analysis of a digital measuring system for oceanographic in situ measurements would allow an oceanographer to become familiar with this method of data acquisition and to interact productively with electronic instrument developers. The generation, analysis, and documentation of a digital measuring system is the purpose of this investigation.

# HISTORICAL

In 1948, Jacobson (14, p. 714) published a paper on an instrument for the continuous recording of salinity, temperature, and depth in sea water, which he developed at the Woods Hole Oceanographic Institute. His instrument did not require the use of any encoding or signal multiplexing techniques, as the resistive transducers were directly coupled through a nine conductor cable to separate shipboard servo-recorders. Pritchard (22, p. 146), Alexiou (1, p. 46), and LaFond (15, p. 137) similarly used a multiconductor cable and direct transducer coupling in their continuous in situ analog measuring systems.

This method of in situ data gathering is hampered by the need for an expensive multiconductor cable; and the accuracy of the data is less than that normally required, due to such factors as variable line resistance, slip-ring noise, and analog recorder inaccuracies (16, p. 36).

The following discretely continuous measuring systems were developed using time-sharing multiplexing and FM modulation techniques. Hamon (12, p. 72), in Australia, reported in 1955 on the use of a single conductor cable in connection with his temperature-salinity-depth recorder. He used a method of time-sharing multiplexing and FM telemetry to sequentially sample the transducers

and reference elements. The data, in the form of a single channel FM modulated carrier, was telemetered through a single conductor cable to a shipboard recording unit. Snodgrass (25, p. 142) reported in 1957 on the use of a single conductor cable in connection with the electronic bathythermometer, which he developed at Scripps Institution of Oceanography.

The following continuous measuring systems were developed using only FM modulation techniques. In 1962, Campbell (3, p. 53) and his associates at the Bendix/Pacific Corporation reported on a FM/FM modulation technique used in their multiple sensor acoustical telemetering system. Since 1963, the Hytech division of the Bissett-Berman Corporation, San Diego, California, has made available their FM modulated single-wire system for measuring "salinity", temperature, and depth in situ. The system is described by Brown (2, p. 26) in a paper discussing its application to the General Dynamics/Convair Monster Buoy Project (6, p. 8).

There are many advantages and disadvantages with regard to these last two FM methods of in situ data gathering and telemetry. The most important advantage lies in the continuity of the measurements and the relative simplicity of the system. The most important disadvantages are a low but acceptable accuracy and a long measuring time to obtain the required level of accuracy.

A completely digital data acquisition system for making in situ

oceanographic measurements was first introduced around 1962 by the Geodyne Corporation of Waltham, Massachusetts (7). Their system involves the use of analog-to-digital conversion and time-sharing multiplexing techniques to make numerous in situ temperature measurements. This system was described in a short article explaining its application to a Woods Hole buoy project (21, p. 41). Recently, the Geodyne Corporation has made available an expanded system using the same measuring techniques to measure in situ conductivity (salinity), temperature, pressure (depth), and other physical and chemical parameters (8). This newer system is capable of telemetering the digital data over a single conductor coaxial cable to surface vessel or land based digital processing equipment. During 1966, the Amecom division of Litton Systems Incorporated, in Silver Springs, Maryland, made available a digital system for measuring in situ conductivity, temperature, and pressure (18). The system was described, in general, by Murdock (20) in his paper presented at the 1966 Northeast Electronics Research and Engineering Meeting. This digital system is also capable of telemetering the digital data over a single conductor cable.

In both of the two digital systems referred to above, the technical details regarding them are proprietary in nature and are not readily available. One is left to assess the relative value of the systems and their similar digital measuring technique from company

supplied specifications. One cannot always rely upon such information, as pointed out by Daulphinee (5, p. 748). However, it seems that this method of in situ data retrieval offers the highest degree of accuracy, resolution, stability, and ease of data transmission of any method developed to date. The systems do have, however, the disadvantages of extreme complexity and lack of truly continuous measurements due to the use of digital encoding and time-sharing multiplexing techniques.

In the past, work has been confined to the measurement of temperature, salinity, and pressure, as these are the parameters which are most important to density calculations. More recently, the non-conservative, as well as the conservative parameters have become important in budget studies. In situ data acquisition systems, which have been developed to date, have been oriented toward the measurement of conductivity (salinity), which is best performed by alternating current measuring techniques. Unfortunately, these measuring systems are not easily adapted to the measurement of non-conservative parameters, which are best measured by direct current measuring techniques. A system analysis of a digital measuring system allows one to select or develop a more universal method of digitization, which will accomodate a larger variety of measurable parameters.

# METHOD OF APPROACH

## Typical Digital System

A typical digital measuring system consists of the following subsystems, as diagrammed in Figure 1: power supplies, sample control, analog-to-digital converter, storage and/or display, multipoint scanner, and transducers (some with signal conditioning amplifiers). The innerconnecting lines between the subsystems in the diagram are arrowed to indicate the path and direction of information flow.

The power supplies provide a set of stable voltages to each of the remaining subsystems. A sample control unit activates the analog-to-digital converter at a controllable rate, or at preset times, to start a sampling and measuring sequence. The storage and/or display section stores, records, and/or displays the digital data output of the analog-to-digital converter. Electrical analog signals, corresponding to the parameters being measured, are generated by the different transducers. The signals are sequentially fed to the analog-to-digital converter by a multipoint scanner. Once at the converter, an analog signal is encoded into a digital format. In any digital measuring system, it is important that the digital data be directly related to the analog data. It is desirable that this relationship be linear over the measuring range.

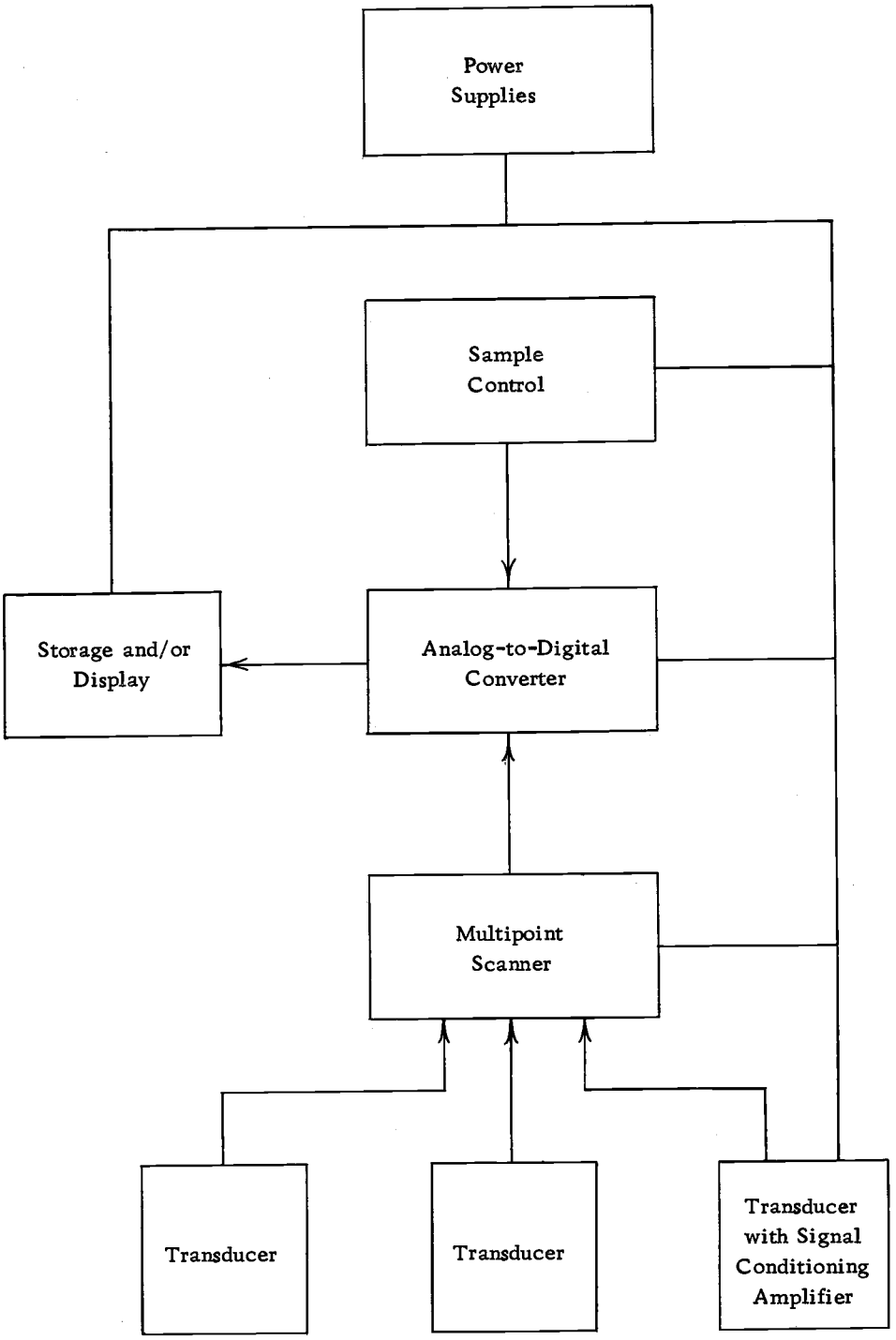



Figure 1. Block Diagram of a Typical Digital Measuring System.

## Need for System Analysis

A measuring system should be considered as a whole in order to attain the highest levels of measuring accuracy, stability, and reliability. In systems which are built up from standard subsystem units, the electrical connection between subsystems is often quite difficult to successfully make and match, and usually leads to total system degradation. When a measuring system can be analyzed and designed as a unit, the interfacing becomes quite natural; and total system performance is usually at its highest level.

By considering the measuring system as a whole, one can first look at the type and magnitude of transducer signals to be measured. When small signal variation transducers such as resistance thermometers and strain gauges are to be measured accurately, the transducer signal either should not be amplified before being encoded or a very stable amplifier must be used. If no amplification is used, the possible methods of encoding become limited. If the d. c. voltage and current outputs from electrochemical cells are to be measured also, the type of analog-to-digital conversion becomes even more restricted.

One approach in deciding upon the type of analog-to-digital conversion to be used would be to note the type of high accuracy laboratory measuring techniques which are ordinarily used in making

these measurements. Resistive transducers with small output variations are usually monitored by resistance ratio measuring techniques. Direct current voltage and current transducers are usually measured by potentiometric techniques. Both of these laboratory measuring techniques are null methods of measurement and utilize inherently accurate and stable resistive ratio networks. It is important to note that the highest degree of accuracy and stability of any standard laboratory method of measurement is attained through the use of direct comparison, null balance, ratio measurements. Therefore, an ideal analog-to-digital converter for making these measurements would be one which utilizes the direct comparison, null balance methods of resistance ratio bridge and potentiometer measurements.

## Selected Approach

The analog-to-digital (A/D) converter, which was designed for this purpose, is unique in that it can be combined with appropriate transducers to form a combination self-balancing resistance ratio bridge or potentiometer. In either case, blanace is attained through the digitally controlled adjustments of a precision resistive ladder network. In the case of operation as a resistance ratio bridge (Figure 2), the precision ladder network forms the equivalent of two adjacent legs in a bridge circuit. Both legs formed by the ladder

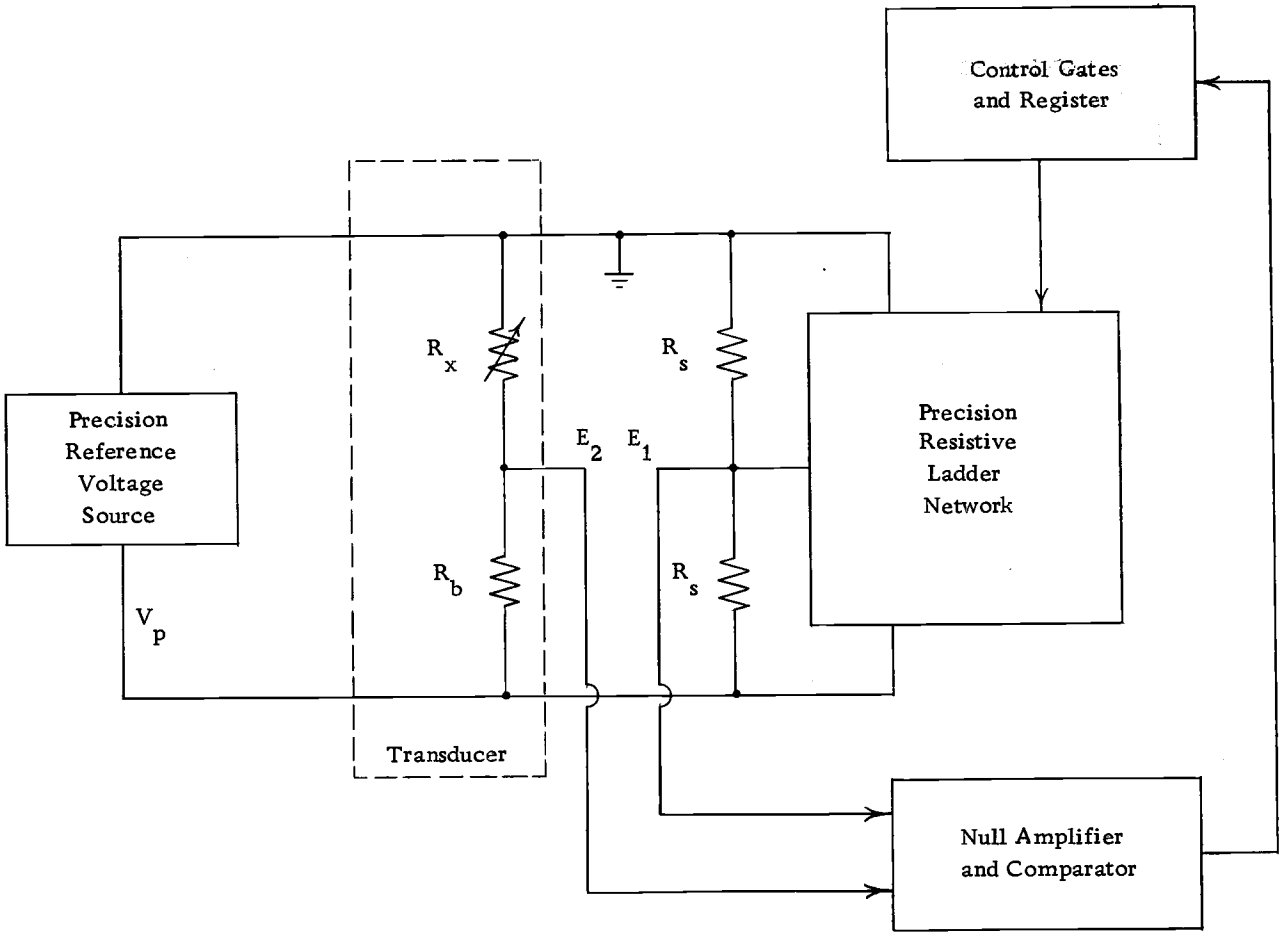



Figure 2. Basic Block Diagram of A/D Converter in Resistance Ratio Bridge Operating Mode.

network are simultaneously adjusted to obtain bridge balance. In the potentiometric operating mode (Figure 3), the ladder network can be looked upon as a precision linear voltage divider. The voltage across the ladder network is held at a constant known value by a precision reference voltage source. Balance is attained when the network output voltage, $E_1$, equals the unknown voltage, $E_2$.

A direct current (d. c. ) bridge circuit was chosen, contrary to the alternating current (a. c. ) bridges used by others (2, 8, 20). This decision was made in order to measure pure d. c. voltage and current outputs from electrochemical cells by a more direct method.

Converter Operation

The block diagrams in Figures 2 and 3 show the interconnection and information flow direction between the different units. The precision resistive ladder network is the most important part of the A/D converter. It is a set of precision resistors which are perfectly matched to assure maximum accuracy and stability. The precision reference voltage source maintains a constant voltage across the ladder network, which is important during the potentiometric mode of operation. The null amplifier compares the known voltage output of the ladder network with the unknown voltage being measured. The comparator, driven by the null amplifier, directs the control gates and register with "yes" or "no" logic signals, which

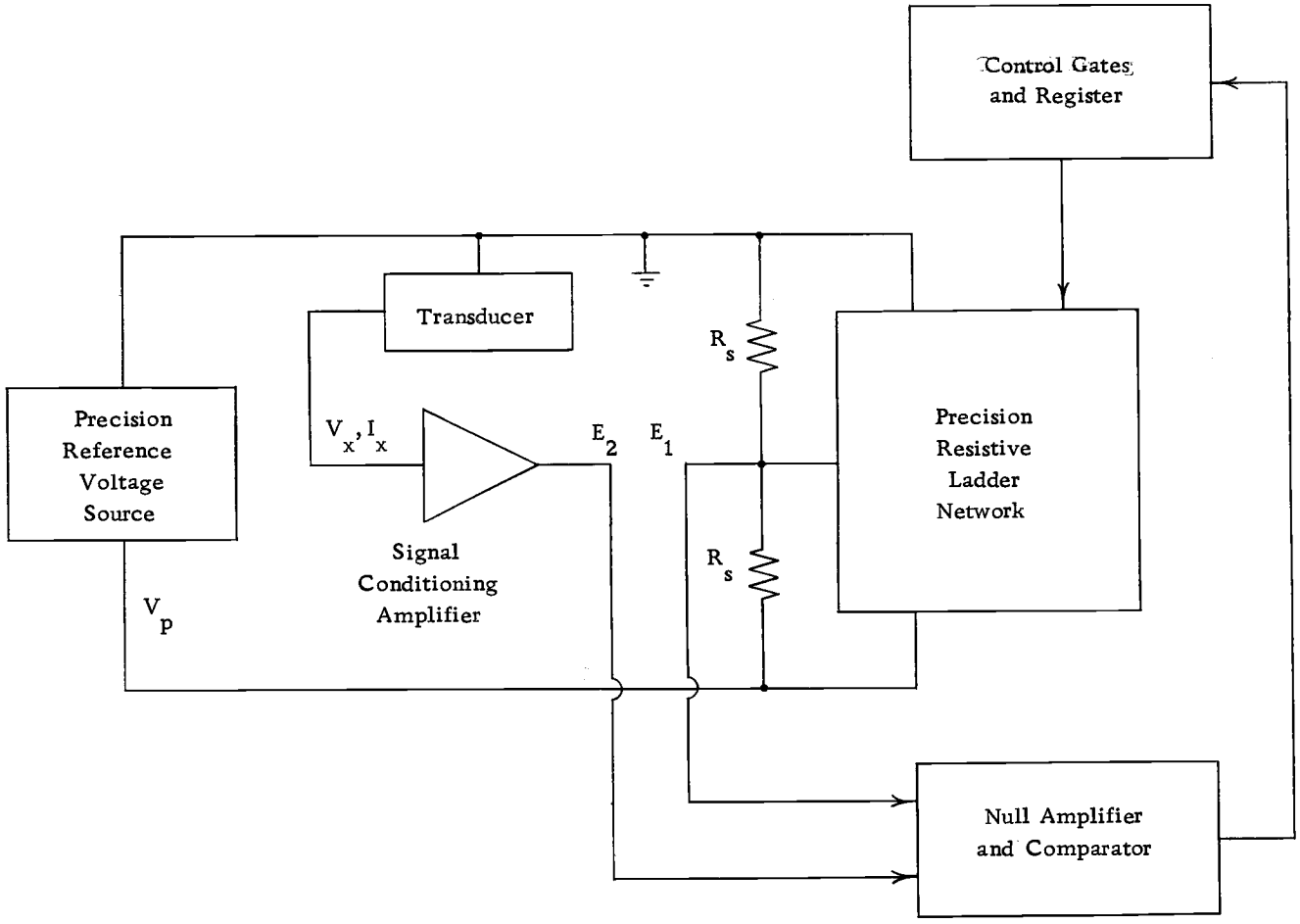



Figure 3. Basic Block Diagram of A/D Converter in Potentiometer Operating Mode.

in turn performs the necessary adjustments on the ladder network to bring about a null between the two voltages.

The converter uses the technique of successive approximation to obtain bridge or potentiometer balance. The following sequence of events is typical of a balancing cycle. The ladder network is first set to half-range by the control gates and register. The bridge or potentiometer output voltages are amplified and compared by the comparator to determine the overbalance or underbalance of the circuit. If the circuit is overbalanced ($E_1 > E_2$), the comparator generates a "yes" logic signal, which is fed back to the control register. This feedback signal then directs the second positioning of the ladder network to the one-quarter range position. If the circuit is underbalanced ($E_1 < E_2$), a "no" logic signal is developed; and the ladder network is set to the three-quarter range position. Continued comparison of the bridge or potentiometer voltages results in sequential adjustments of the ladder network by either plus or minus one-half of the preceding step until circuit balance is attained.

## Transducers Considered

The specific transducers to be considered in this investigation are a platinum resistance thermometer, a strain gauge pressure transducer, and a membrane polarographic oxygen cell. The first two fall into the category of resistive transducers with extremely

small output variations. The third is in the class of electrochemical cells with pure d. c. outputs.

As was pointed out earlier, a d. c. potentiometer is used to accomodate transducers similar to the oxygen cell. To measure the very small variations of transducers in the first category, a unique loaded ladder circuit was designed.

## Unique Loaded Ladder Circuit

This circuit is unique in that it utilizes two equal loading resistors, $R_s$, to set the voltage range over which the precision resistive ladder network output, $E_1$, will vary (Figure 2). The defining equation, which will be derived in a later section, relates the loaded ladder network output, $E_1$, with the analog-to-digital converter binary output, p. In its simplified form, the equation is: $E_1 = A_s p + B_s$, where $A_s$ and $B_s$ are constants. It is important that the equation is linear, as this will permit simplified data processing and assure constant sensitivity throughout the measuring range.

Since a direct comparison and null method of measurement is used, the binary output, p, which is the data in digital form, can be related to the parameter being measured by equating $E_1$ with the transducer output, $E_2$.

Resistance Conversion Equation

The exact equation for $E_1$ is:

$$E_1 = \frac{V_p}{2} \left[ 1 - \frac{R_o}{R} \left(1 - \frac{p}{2^{N-1}}\right) \right]$$

where: $p$ = Binary output

$R$ = Characteristic output resistance of ladder network

$R_s$ = Range setting load resistance

$R_o = \frac{RR_s}{R_s + 2R}$ = Constant for a particular range setting

$N$ = Number of stages in ladder network.

For a particular range setting where $R_s$ is fixed, the equation reduces to the basic form:

$$E_1 = \frac{V_p R_o}{2^N R} p + \frac{1}{2} \left(1 - \frac{R_o}{R}\right) V_p$$

$$E_1 = A_s p + B_s$$

or

$$\frac{E_1}{V_p} = C_s p + D_s$$

where: $A_s$, $B_s$, $C_s$ and $D_s$ are constants for a particular range setting.

In the case of temperature measurement with a resistance thermometer, the thermometer element, $R_x$, is a function of temperature, while $R_b$ as shown in Figure 2 is constant.

Therefore, the equation for $E_2$ becomes:

$$E_2 = \frac{R_x}{R_x + R_b} V_p$$

where: $R_x = f(T)$

$V_p$ = Constant voltage from voltage source.

Upon equating the equation for $E_2$ with that for $E_1$, $V_p$ cancels out and the conversion equation becomes:

$$\frac{R_x}{R_x + R_b} = C_T p + D_T$$

where: $C_T$ and $D_T$ are particular constants for the set temperature range.

Solving for $R_x$ in order to relate temperature with the binary output, p, gives:

$$R_x = R_b(C_T p + D_T) + R_x(C_T p + D_T)$$

$$R_x = f(T) = \frac{R_b(C_T p + D_T)}{1 - (C_T p + D_T)}$$

Voltage Conversion Equation

In the case of oxygen measurement with a polarographic cell, $E_2 = I_x R_f = V_x$, which is a function of the partial pressure of dissolved oxygen, $O_2$. $R_f$ is a constant known resistance in the signal conditioning amplifier (Appendix Ib).

Upon equating $E_1$ to $E_2$, the conversion equation becomes:

$$V_x = I_x R_f = f(O_2) = A_O p + B_O$$

where: $A_O$ and $B_O$ are particular constants for the set oxygen range.

The relationship between T and $R_x$, $O_2$ and $V_x$ are found by the calibration of the particular transducers. System calibration then gives the high resolution calibration between the digital data output, p, and T, $O_2$, or any other measurable parameter which can be converted into a resistance, current, or voltage.

Type of Circuits Used

The electronic circuitry of the digital control section in this system is the same as that used by the Geodyne Corporation in their Model 605 digitizer. The space requirements of the control section have been reduced to a minimum through the use of "cordwood" packaging techniques.

At the time the control section was assembled, digital integrated circuits were not available in low-cost units. The use of such units could reduce the space requirements even further. Linear integrated circuits have been used in the power supply voltage regulators,

voltage reference source, and null amplifier to give state-of-the-art sensitivity, stability, and size reduction.

# FOUR-BIT ANALOG-TO-DIGITAL CONVERTER PROTOTYPE

The diagram presented in Figure 4 shows the analog-to-digital converter in more detail. The figure is a block diagram of the four-bit A/D converter prototype. This prototype was designed and built to test the circuits and unique encoding technique which are to be used in the high resolution converter. A short description of the flow pattern between the individual blocks of Figure 4 is found below. A more detailed description of each block will then follow.

## General Description

The A-counter generates the signals $A_1$, $A_1'$, thru $A_4$, $A_4'$ by counting the pulses of the clock generator output, $K_1$. The pulses in the $K_1$ signal simultaneously activate the "set" gates in order to synchronize the operations of the two units.

The diode "set" gates produce the signals $a_1$-$a_5$ from the A-counter outputs, $A_1$, $A_1'$-$A_4$, $A_4'$. The signals $a_1$-$a_4$ are respectively fed to the "set" inputs of the four flip-flops in the D-register. The diode "clear" gates produce the signals $a_2'$-$a_5'$ from the comparator output, $d_0$, and the set gate outputs, $a_2$-$a_5$. Similarly, the signals $a_2'$-$a_5'$ are respectively fed to the "clear" inputs of the four flip-flops in the D-register.

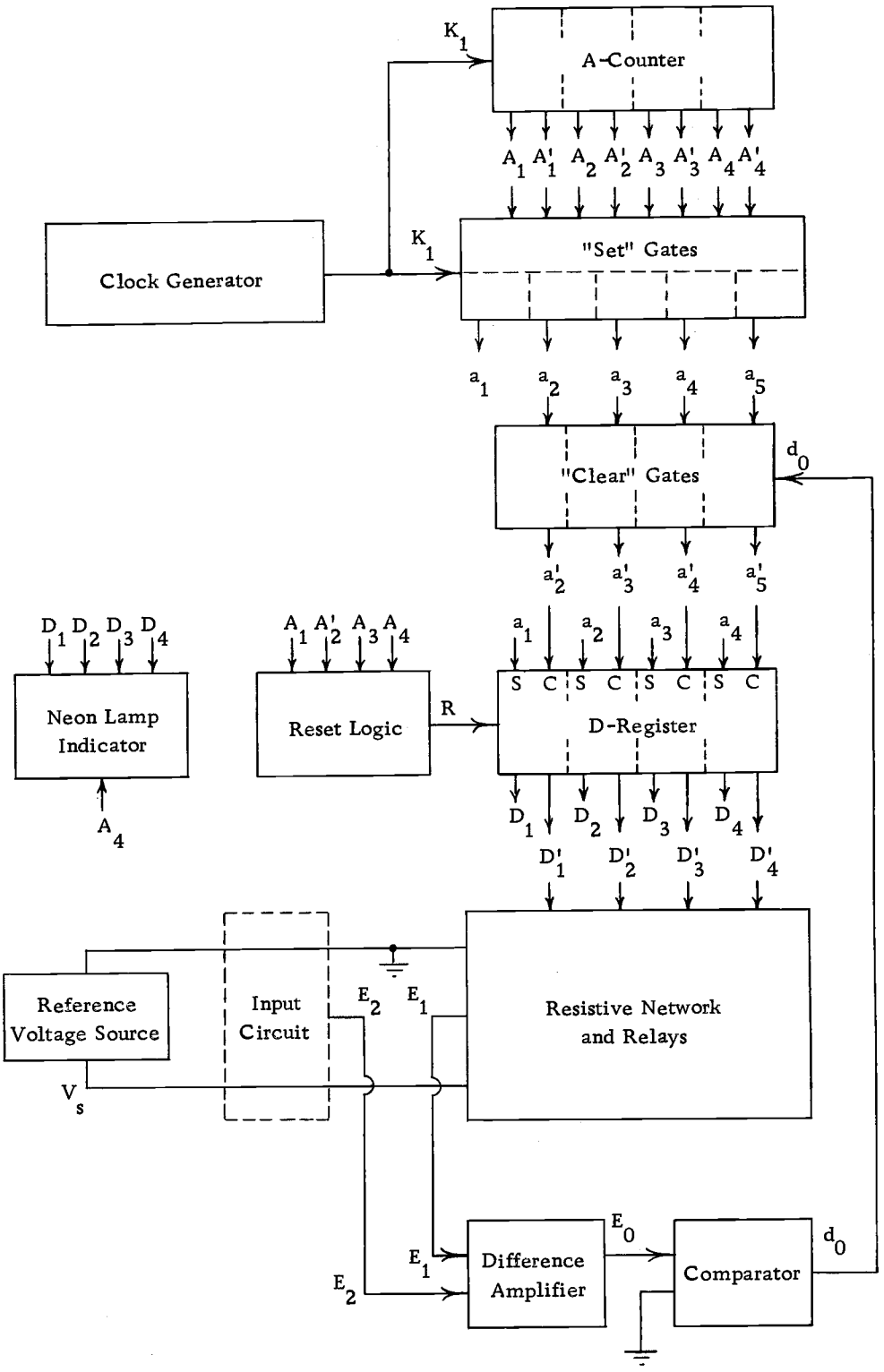



Figure 4. Block Diagram of Four-Bit Analog-to-Digital Converter Prototype.

The reset logic gate generates a reset signal, R, from the A-counter outputs, $A_1$, $A_2'$, $A_3$, and $A_4$ to reset all flip-flops in the D-register. A reset pulse is generated after every cycle of the A-counter, which is also a complete bridge or potentiometer measuring cycle.

The neon lamp indicator displays the state of each flip-flop in the D-register after every balancing part of the measuring cycle. The inputs $D_1$-$D_4$ respectively activate the four lamp drivers. To reduce lamp flickering, the $A_4$ input blanks all the lamps during the balancing sequence and displays the state of $D_1$-$D_4$ after the balancing part of the measuring cycle has taken place (Figure 13).

## Clock Generator

The prototype clock generator consists of an astable multivibrator, a counting flip-flop, and a three-input transistor "AND" gate (Figure 5). The astable multivibrator, MV-2, is a free running square wave generator (Figure 6), which determines the frequency of operation of the entire digitizer and sets the sampling rate at five samples per second. The output of the astable multivibrator, $K_0$, triggers the bistable multivibrator inputs, $T_1$ and $T_0$ (Figure 7). The bistable multivibrator is wired as a counting flip-flop. It, therefore, divides the $K_0$ input by two to produce the half frequency square wave output X, and its compliment X'. The three-input

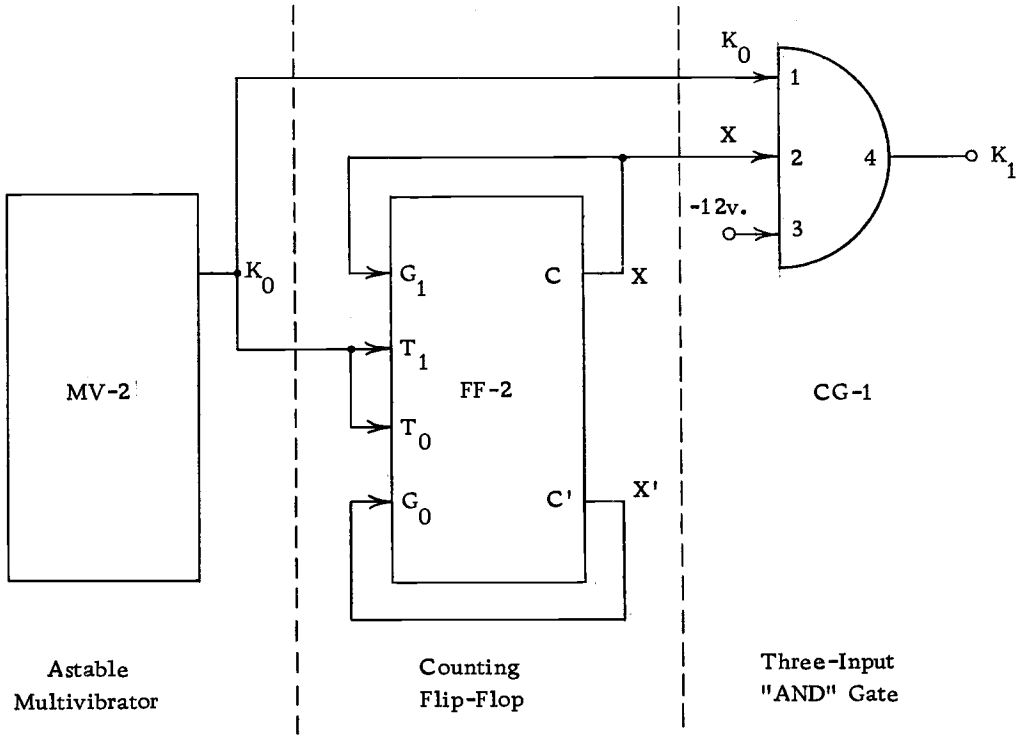



Figure 5. Prototype Clock Generator.

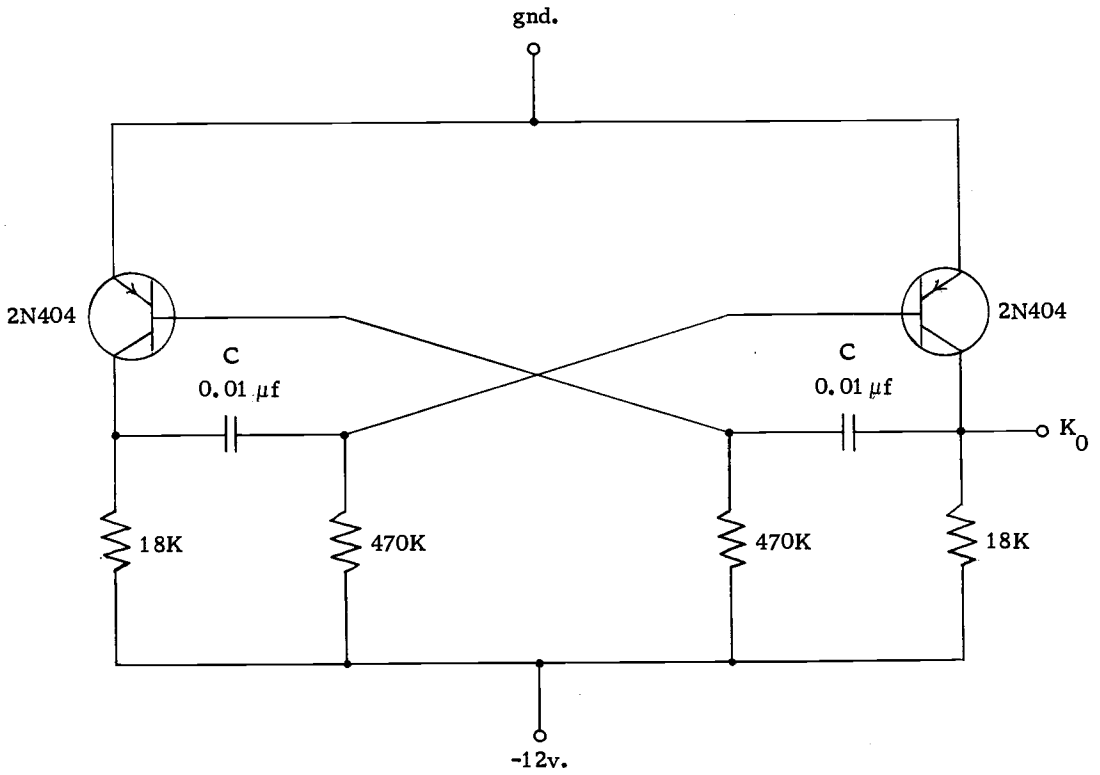



Figure 6. Astable Multivibrator Circuit, MV-2.

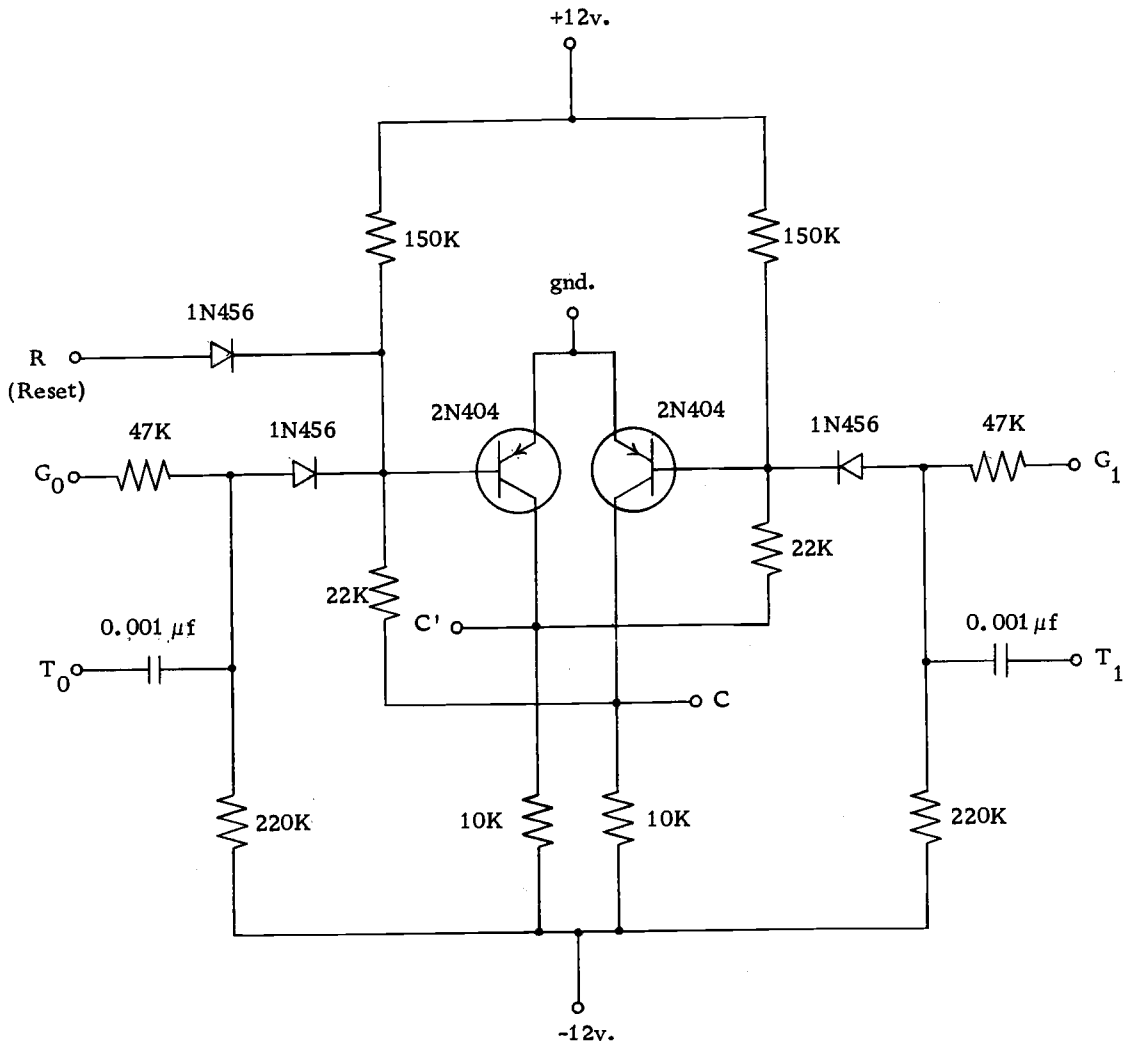



Figure 7. Bistable Multivibrator Circuit, FF-2.

transistor "AND" gate, Figure 8, then forms the waveform $K_1$ by the logical "AND" operation of $K_0 \cdot X$ (Appendix Ia). The pulses in the $K_1$ waveform simultaneously activate the A-counter and the diode "set" gates.

## A-Counter

The prototype A-counter is made up of four bistable multivibrators (Figure 7), which are individually wired as counting flip-flops. The four counting flip-flops are then interconnected to form a straight binary counter (Figure 9), with sixteen different possible states as indicated in Figure 10. The first counting flip-flop is triggered at its $T_1$ and $T_0$ inputs by each positive step in the clock pulse train, $K_1$. One of the outputs of this first flip-flop is labelled $A_1$ and the other, which is the compliment of $A_1$, is labelled $A_1'$. The unprimed output of each counting flip-flop in turn triggers the following flip-flop during the positive step of its waveform to generate the successive half frequency waveforms $A_2$, $A_3$, $A_4$, and their compliments (Figure 10).

## "Set" Gates

The prototype "set" gates (Figure 11), consist of five five-input diode "AND" gates. Each "set" gate (Figure 12), has the clock waveform $K_1$, as one input. The other four inputs are a

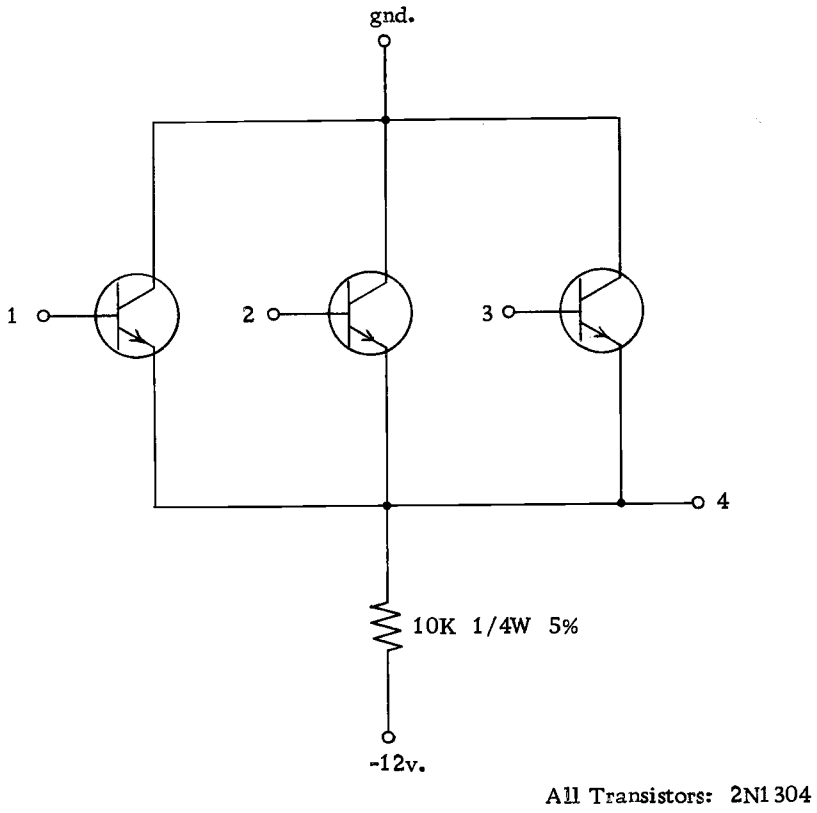



Figure 8. Three-Input Transistor "AND" Gate Circuit, CG-1.

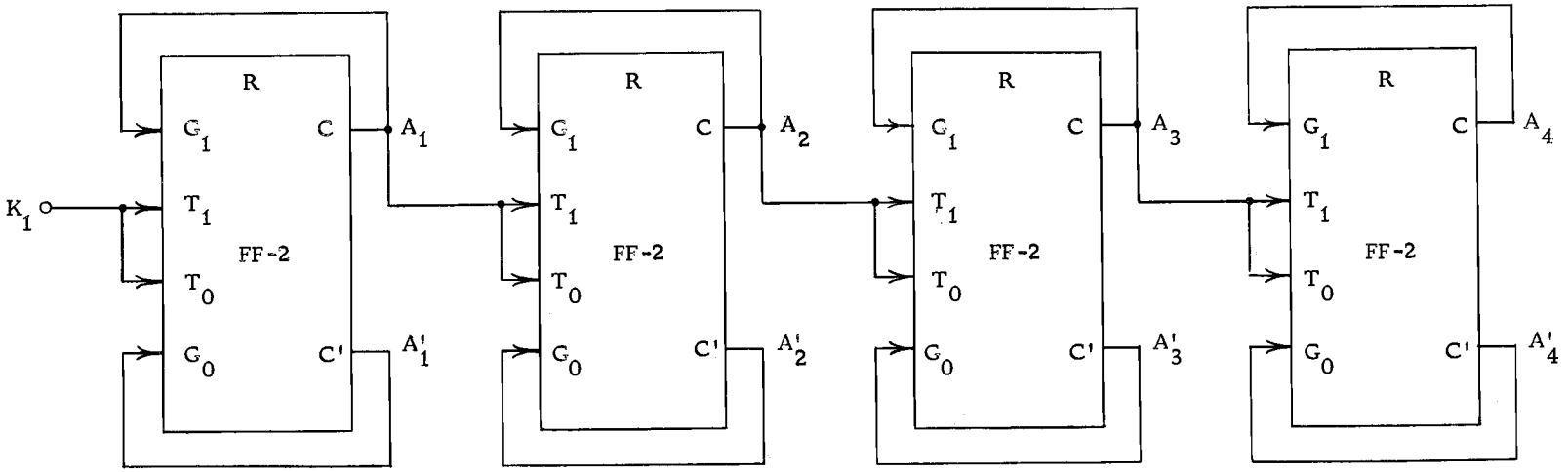



Figure 9. Prototype A-Counter.

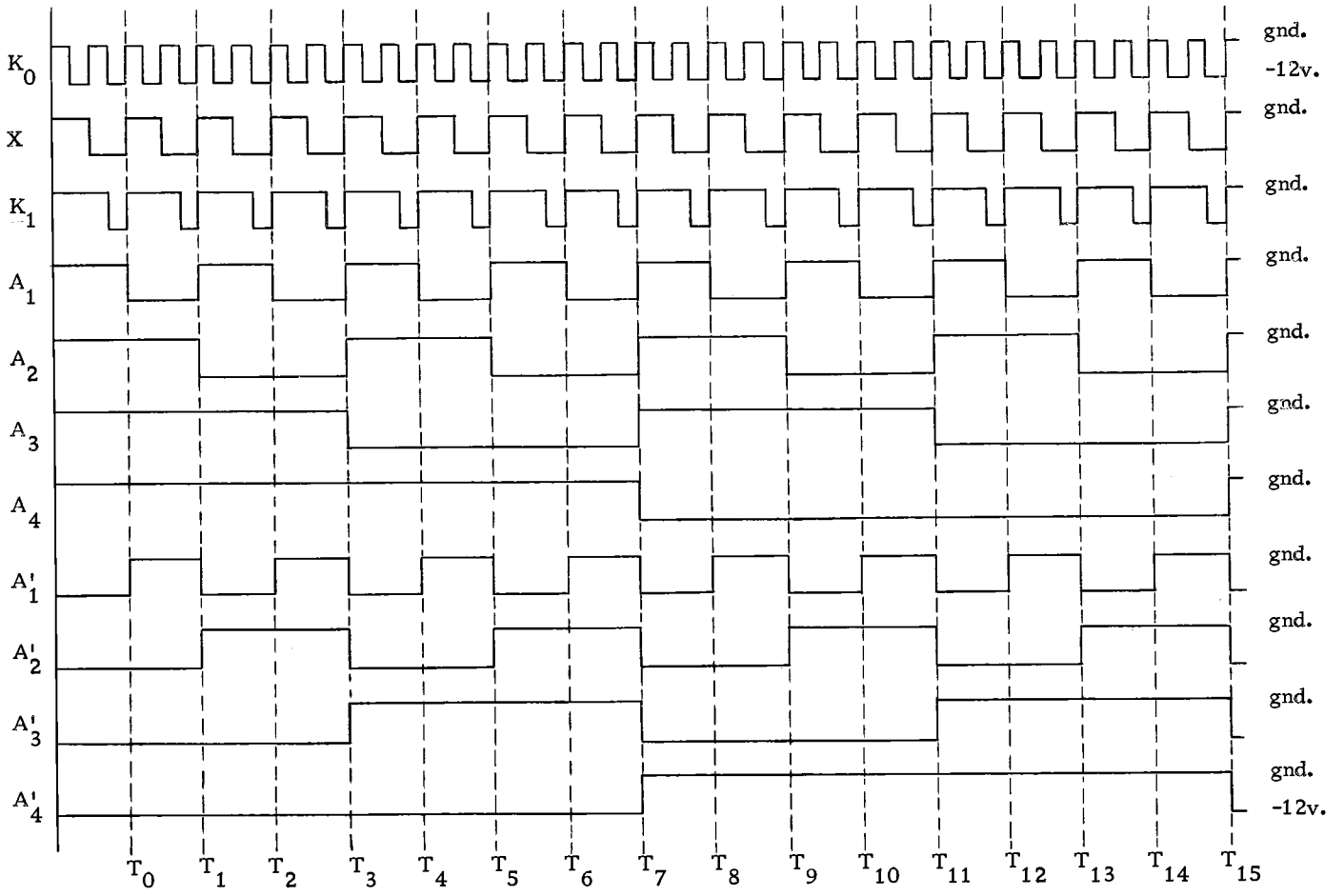



Figure 10. Prototype Clock Generator and A-Counter Timing Diagram.

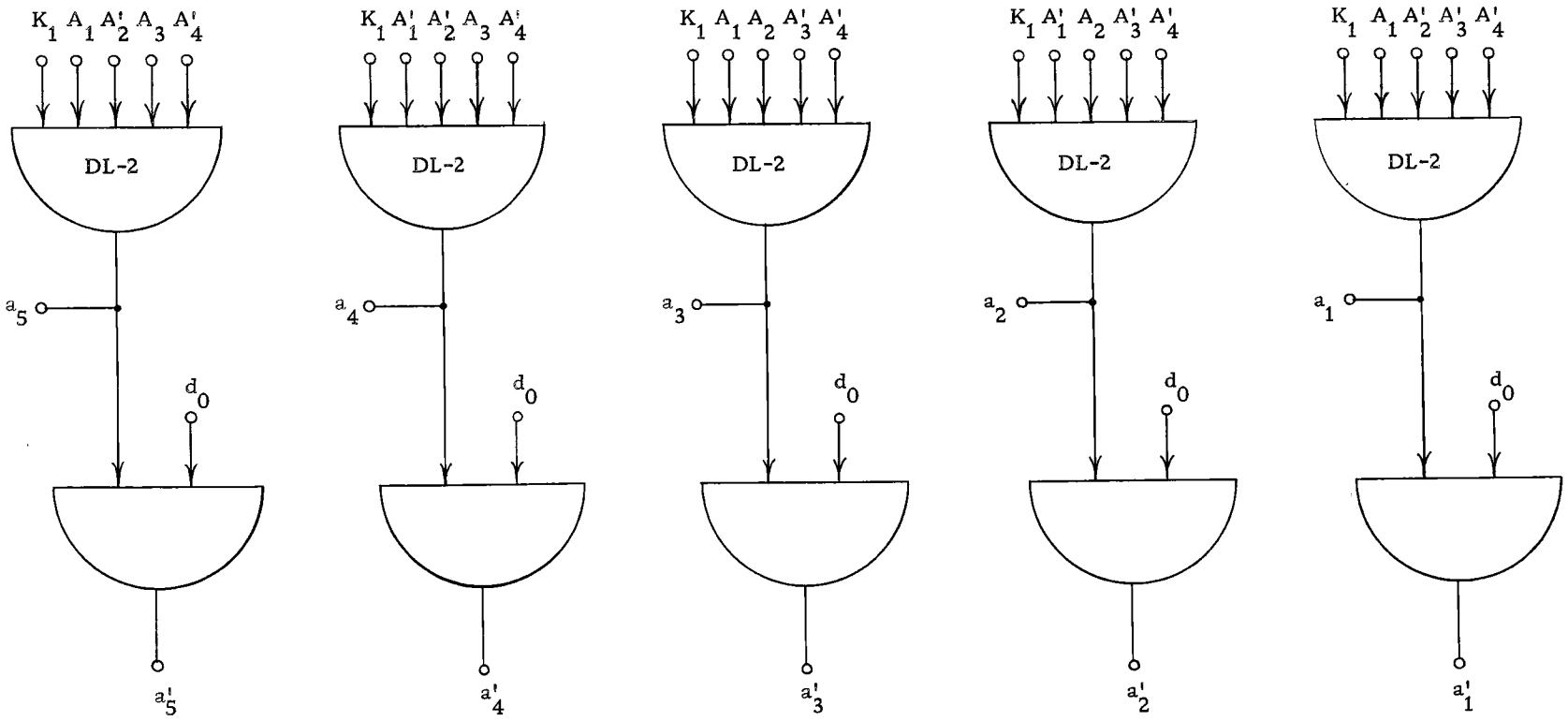



Figure 11. Diode "Set" and "Clear" Gates.

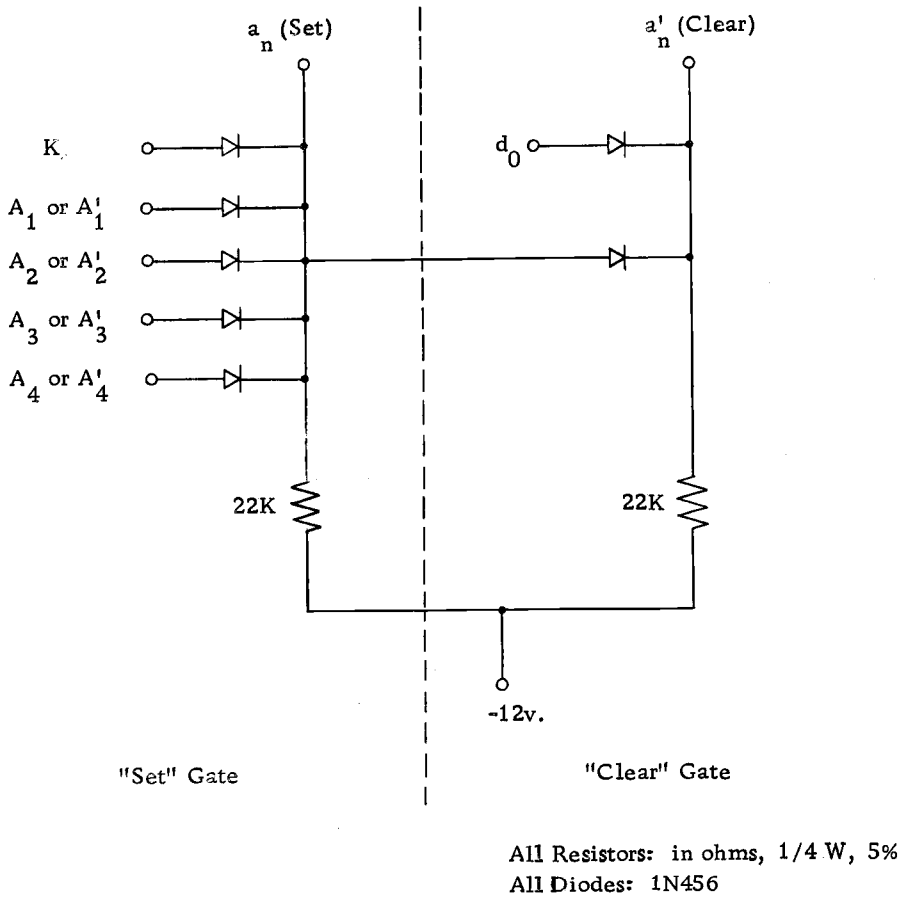



Figure 12. Diode "Set" and "Clear" Gate Circuit, DL-2.

combination of four of the eight A-counter outputs which correspond to one of the sixteen different states of the A-counter.

For example, the output of the first diode "set" gate, $a_1$, is generated by the logical "AND" operation of $K_1 \cdot A_1 \cdot A'_2 \cdot A'_3 \cdot A'_4$. Similarly, $a_2$ through $a_5$ are formed by the "AND" operation of $K_1$ and the outputs of the A-counter which correspond to the second through fifth state of the counter (Figure 13).

## "Clear" Gates

The prototype "clear" gates, Figure 11, consist of five two-input diode "AND" gates. Each "clear" gate, Figure 12, has the $d_0$ signal from the comparator as one input. The other input to each of the five "clear" gates is $a_1$ thru $a_5$, respectively. The $a'_1$ thru $a'_5$ outputs are formed by the logical "AND" operation of $d_0$ and $a_1$ thru $a_5$, respectively. The $a'_n$ output of each "clear" gate remains at ground level until both the $a_n$ and $d_0$ inputs become negative (-12 v.), at which time the $a'_n$ output will also become negative (-12 v.).

## Reset Logic

The prototype reset logic circuit (Figure 14) is made up of a single four-input diode "AND" gate and a differentiator. The gate output, R, becomes negative when the logical "AND" operation of

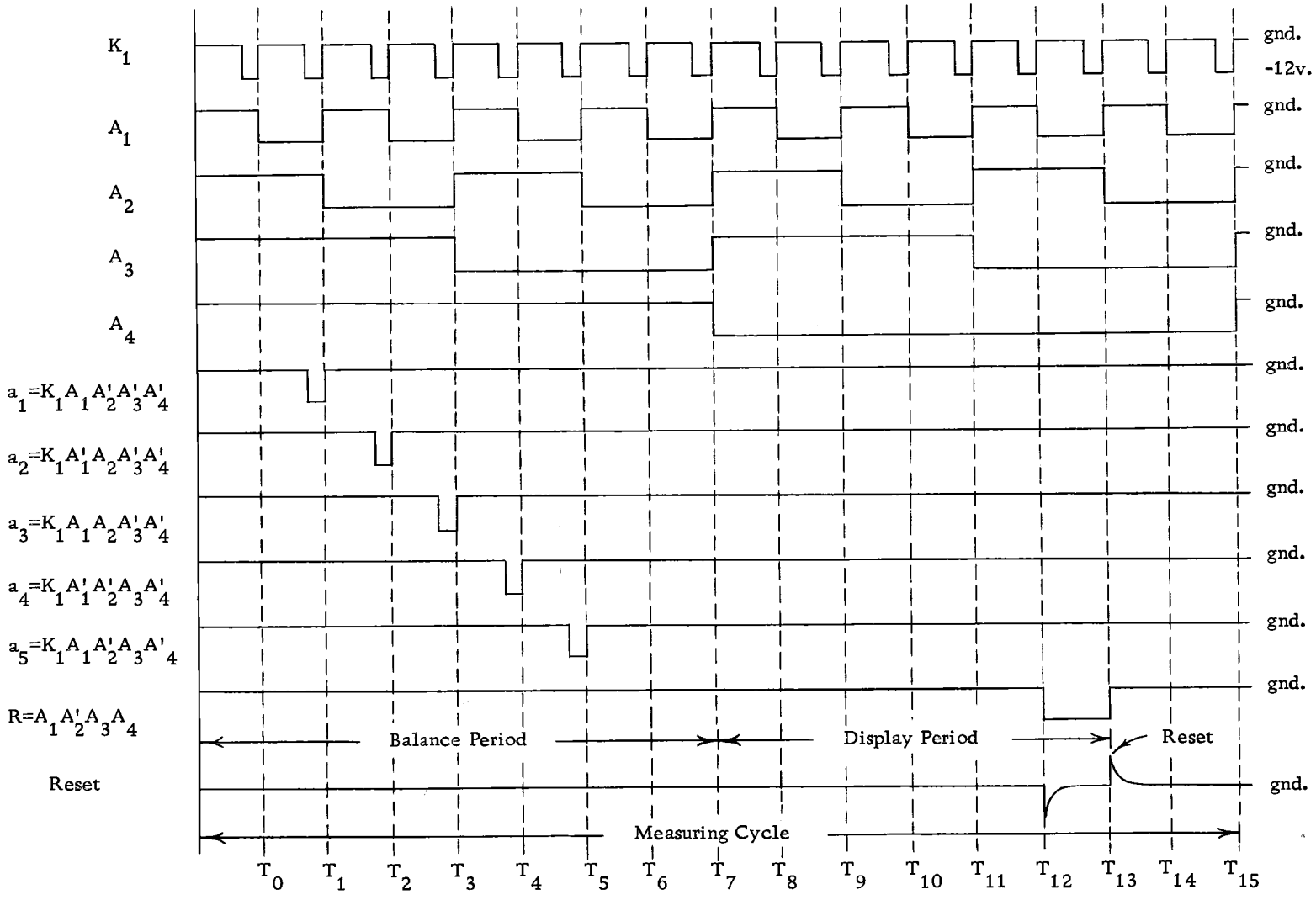
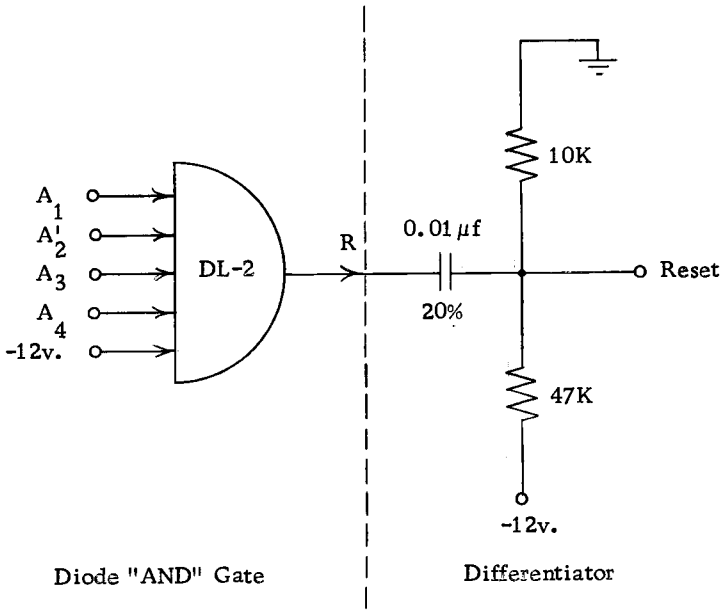



Figure 13. Prototype Diode "Set" and Reset Logic Timing Diagram.




All Resistors: in ohms, 1/4 W, 5%

Figure 14. Prototype Reset Logic Circuit.

$A_1 \cdot A_2' \cdot A_3 \cdot A_4$ is satisfied. The R output is then differentiated to generate a sharp negative and positive spiked waveform labelled reset (Figure 13). It is the positive spike of the reset waveform which simultaneously resets all the flip-flops in the D-register.

## D-Register

The prototype D-register (Figure 15), is composed of four bistable multivibrators, FF-2 (Figure 7), individually wired as set-clear flip-flops. A common line running between them carries the reset input. The trigger inputs $T_1$ and $T_0$ of the first set-clear flip-flop are connected to the diode "set" and "clear" outputs $a_1$ and $a_2'$, respectively. The outputs of the first set-clear flip-flop are labelled $D_1$ and $D_1'$.

The state of the first flip-flop output, $D_1'$, (either 0 v. or -12 v.), just before display is dependent upon whether or not a negative $a_2'$ "clear" pulse arrives after the negative $a_1$ "set" pulse. The $D_2$, $D_3$, and $D_4$ outputs and their compliments are similarly formed.

## Neon Lamp Indicator

The prototype neon lamp indicator, (Figure 16), is made up of four neon lamp drivers, ND-1, (Figure 17). Each neon lamp driver consists of a two-input "AND" gate and a transistor switch. $A_4$ is a

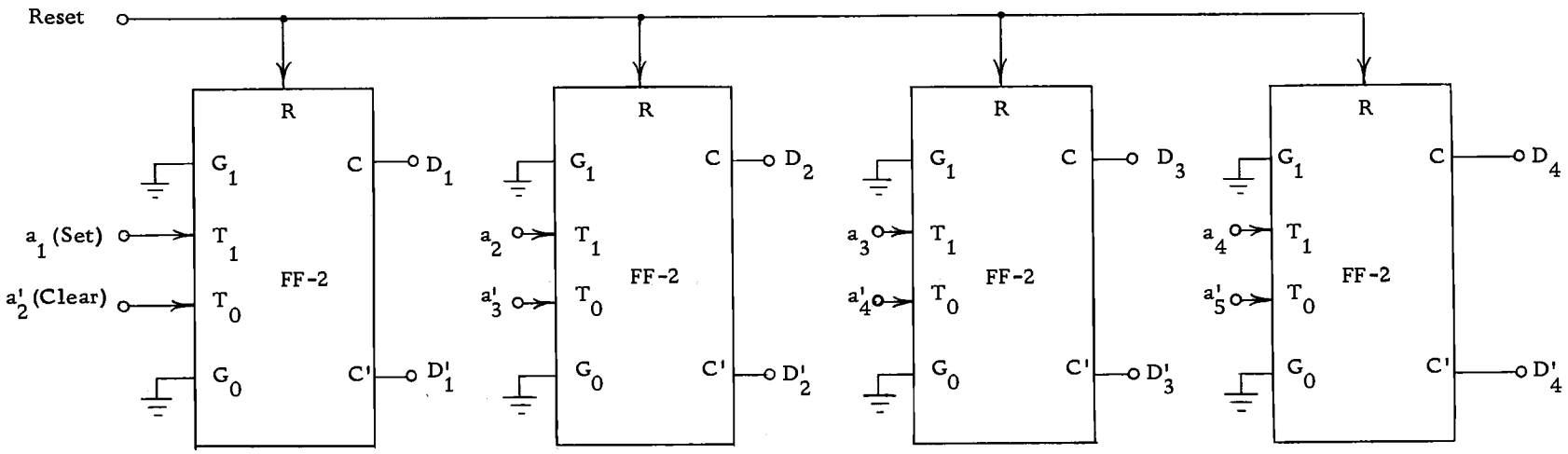



Figure 15. Prototype D-Register.

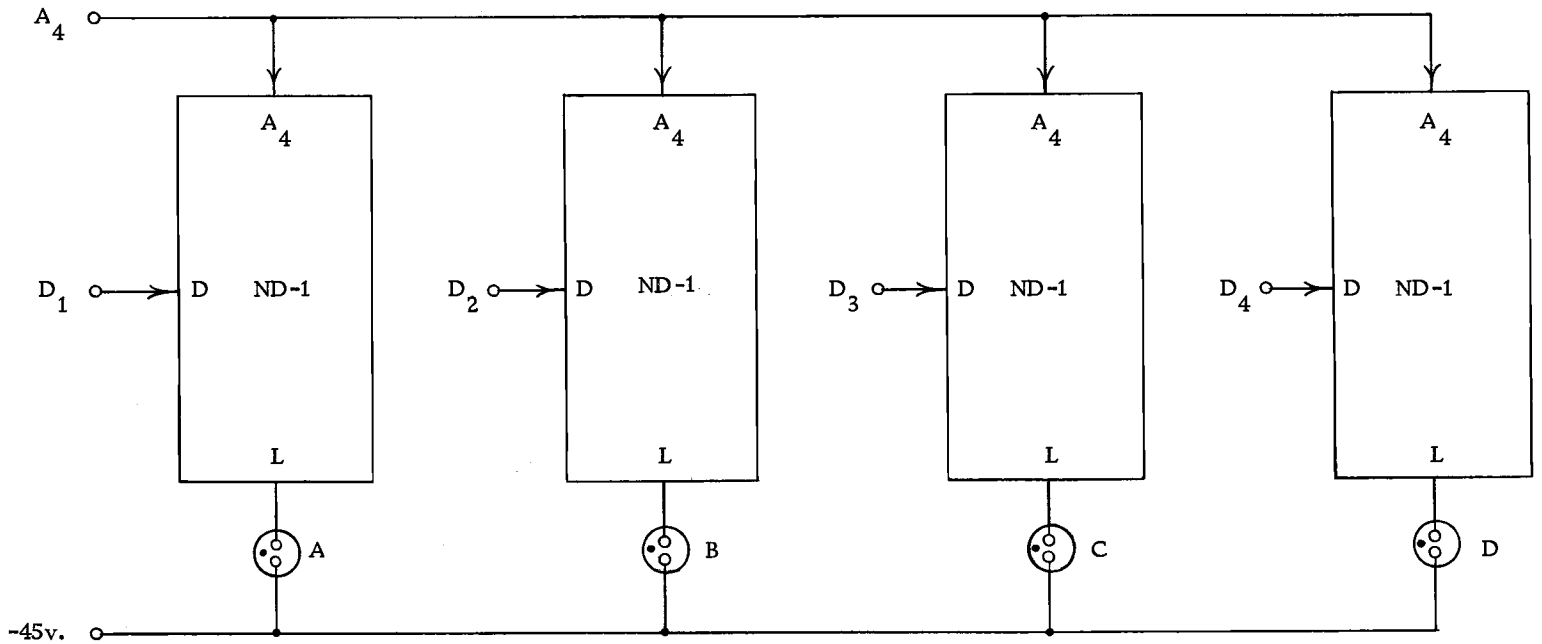



Figure 16. Prototype Neon Lamp Indicator.

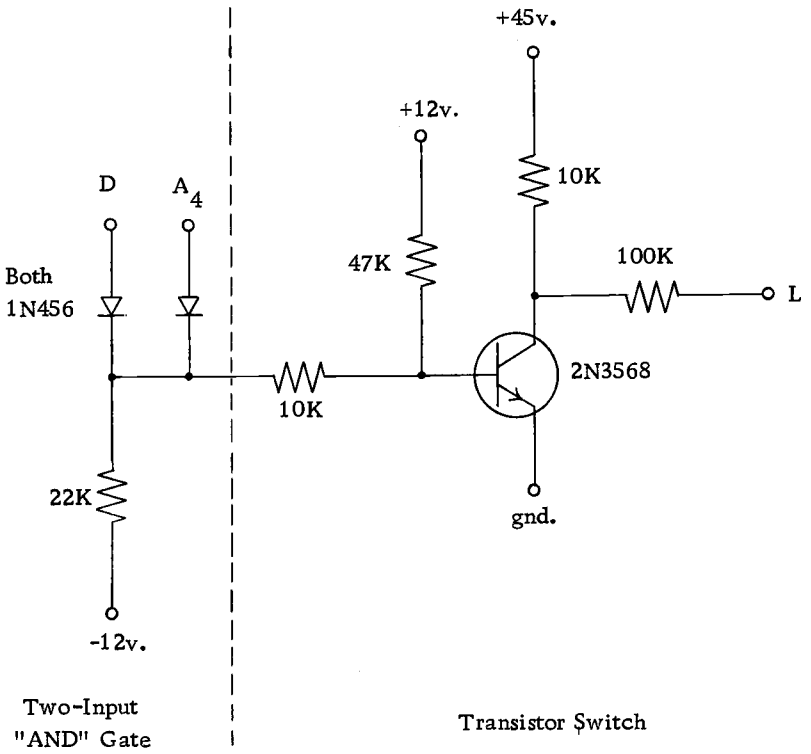
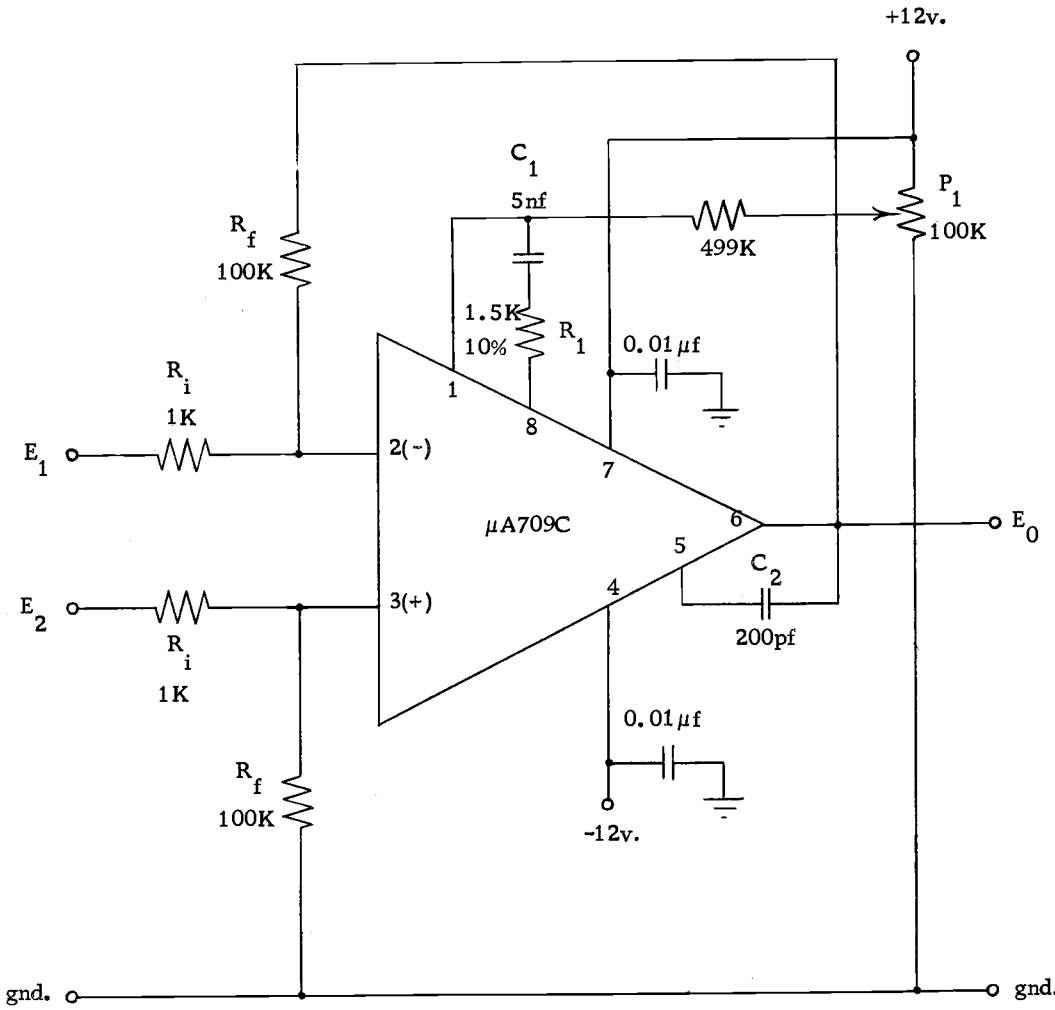



Figure 17. Neon Lamp Driver Circuit, ND-1.

common input to each "AND" gate. The other input is one of the four D-register outputs, $D_1$-$D_4$. When the logical "AND" operation of $A_4 \cdot D_1$ is satisfied, for example, the gate output becomes negative which turns the NPN transistor switch off. With the transistor off, the output voltage rises toward +45 volts turning on neon lamp A, which is connected between the output, L, and a -45 volt supply (in this way, a 50 v. transistor controls a 90 v. neon lamp). Similarly, the neon lamps B thru D are controlled by the "AND" operation of $A_4$ and $D_2$ thru $D_4$, respectively. The neon lamps are, therefore, kept from flickering during the balancing period by the common input $A_4$ (Figure 13).

## Difference Amplifier

The prototype difference amplifier, (Figure 18), is a Fairchild (Fairchild Semiconductor Company, Mountain View, California), μA709C integrated circuit (IC ) operational amplifier operating in the operational mode with a fixed differential gain of 100. The operational amplifier uses feed-back resistors of 100 KΩ and input resistors of 1kΩ to obtain the fixed differential gain of 100 or 40 db, (Appendix Ib). Through the use of current injection, amplifier input offset voltage is reduced to zero by adjusting the 100 KΩ potentiometer, $P_1$. The amplifier is frequency compensated by $C_2$, $C_1$, and $R_1$ to give a 20 db per decade roll-off starting at the upper frequency break point




All Resistors: in ohms, 1/4 W, 1%
100ppm/°C, unless
otherwise specified
All Capacitors: Disc Ceramic 20%

Figure 18. Prototype Difference Amplifier.

of 5 KHz. A unity gain bandwidth of 500 KHz is, therefore, obtained and assures amplifier stability for any resistive load.

## Comparator

The prototype comparator (Figure 19), consists of a limiting circuit, a Fairchild μA710C IC comparator, and a transistor inverting amplifier.

The difference amplifier output, $E_0$, is connected to the inverting input of the IC comparator through the 1 KΩ resistor of a resistor-diode limiting circuit. This circuit limits the voltage swing at the comparator input to ±0.7 v., thereby keeping the ±10 v. $E_0$ signal from exceeding the ±5 v. comparator input voltage range. The non-inverting input is connected to ground through another 1 KΩ resistor. A 500 pf capacitor between the two comparator inputs bypasses to ground any high frequency signal which may appear at the inverting input. The 100 KΩ positive feedback resistor connected from the output to the non-inverting input of the comparator decreases the possibility of self-induced oscillation. Oscillation is sometimes caused by a slight voltage drop induced across the input resistor when the comparator starts to draw input current upon switching. The use of a positive feedback resistor has the disadvantage of inducing a larger hystersis band into the comparator (10, p. 165).

The comparator amplifier inverts and amplifies the -0.5 v.

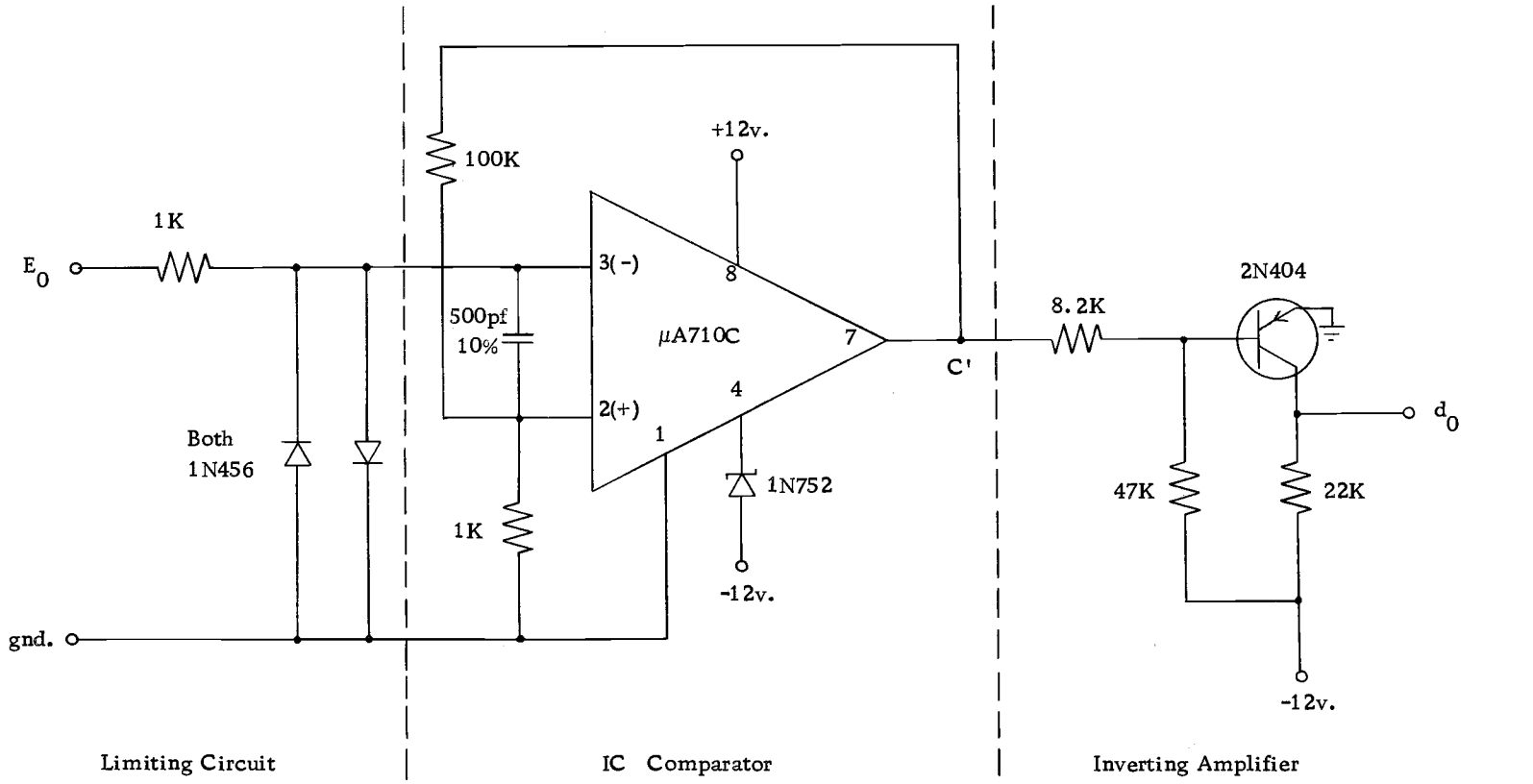


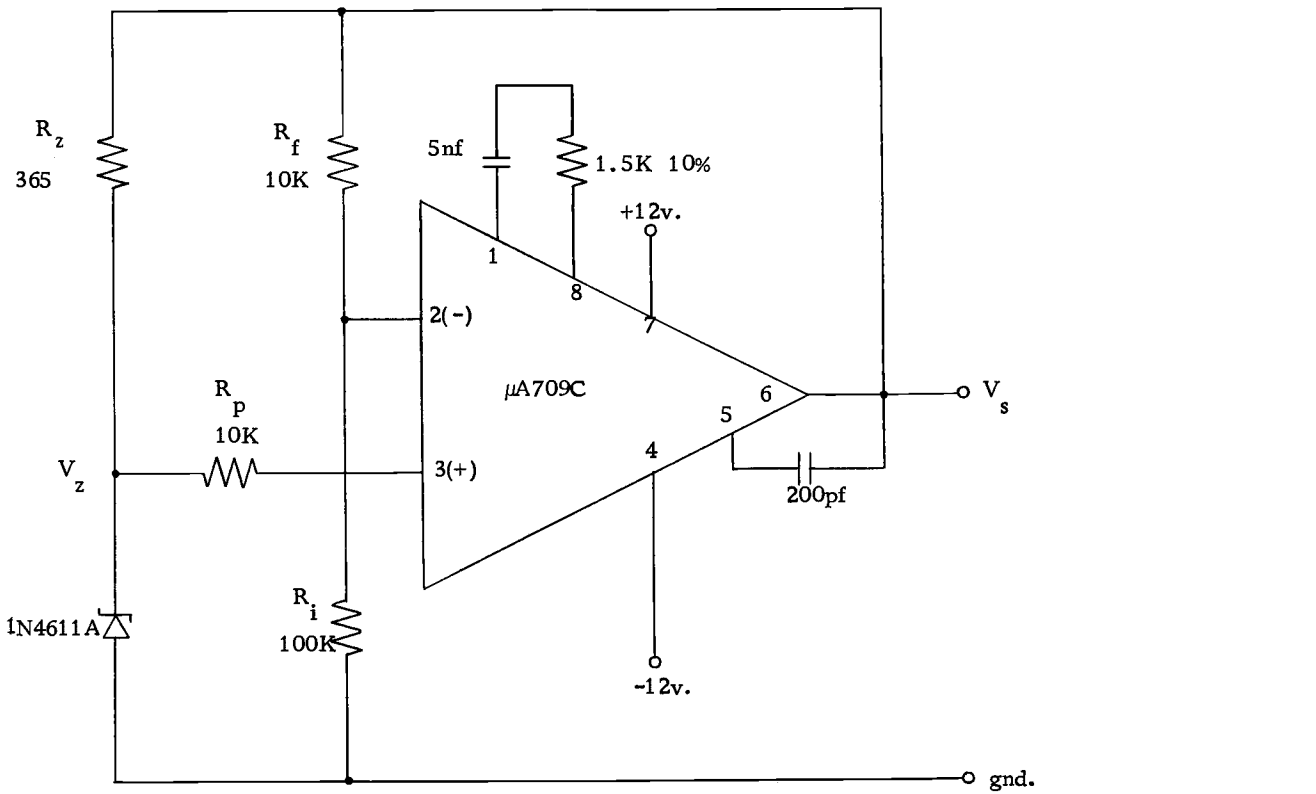

Figure 19. Prototype Comparator.

and +3.2 v. IC comparator output voltage levels. It produces at its output, $d_0$, the inverted and amplified voltages 0 v. and -12 v., respectively, which are compatible with the logic voltage levels of the other logic units.

## Reference Voltage Source

The prototype reference voltage source (Figure 20), uses a Fairchild temperature compensated (±0.002%/°C at 1-3 ma) silicon zener reference diode, 1N4611A, as a voltage reference element in the positive feedback loop of a Fairchild μA709C IC operational amplifier. The amplifier serves both as a high gain error amplifier and a current buffer amplifier, with a 10 ma current output capability. This circuit is a modification of the one described by Giles (10, p. 144). The modification involves placing the reference diode in the positive feedback loop. In this way, a constant diode current is drawn from the constant output voltage if the series resistor, $R_z$, is both time and temperature stable. This method greatly increases the voltage stability of the reference diode.

The amplifier is operated in the operational mode as a non-inverting amplifier (Appendix Ib). The inverting input of the amplifier is connected to the output through a 10 KΩ feedback resistor, $R_f$. The 100 KΩ input resistor, $R_i$, which is also connected to the inverting input, is returned to ground. This sets the gain of the




All Resistors: in ohms, 1/4 W, 1%, 100ppm/°C,
Unless Otherwise Specified
All Capacitors: Disc Ceramic 20%

Figure 20. Prototype Reference Voltage Source.

non-inverting amplifier to 1.1. The non-inverting input is connected to the cathode of the reference diode through a 10 KΩ resistor, $R_p$, while the anode is returned to ground. With a zener voltage, $V_z$ = 6.55 v., at a diode current of 2 ma, the output voltage, $V_s$, becomes 7.21 v. (6.55 v. x 1.1). By connecting the cathode of the reference diode to the non-inverting input of a non-inverting amplifier, the reference diode is negligibly loaded, since the input impedance to such an amplifier is in the tens of megohms (9, p. 84). The amplifier current output capability of 10 ma, therefore, allows up to 10 ma to be drawn by a load without any appreciable voltage variation being induced across the reference diode. The voltage regulation of the reference voltage source is extremely high and is only slightly affected by temperature drifts of the reference element and amplifier.

## Input Circuit

The prototype input circuit for the bridge operating mode is different from the circuit for the potentiometer mode. In the resistance ratio bridge operating mode, the input circuit is simply two resistors as indicated in Figure 2. The unknown resistance, $R_x$, is placed in series with the known resistance, $R_b$, to form two adjacent arms of the bridge circuit.

For measuring temperature, a platinum thermometer of

resistance $R_x$ is used along with a fixed series resistance, $R_b$. The value of $R_b$ is made equal to the mid-range value of $R_x$ to obtain maximum bridge output (4, p. 129).

For measuring pressure, both resistors are made variable. This is accomplished by using a two-element strain gauge pressure transducer with one element (serving as $R_x$) undergoing tension and the other (serving as $R_b$) undergoing compression. Both elements are equal in resistance at a gauge pressure of zero psig.

In the potentiometer operating mode, the input circuit is a current or voltage output transducer with its associated signal conditioning amplifier (Figure 3). For measuring the current output from an oxygen cell, the conditioning amplifier is an operational amplifier connected as a current-to-voltage converter (Appendix Ib). The value of the feedback resistor, $R_f$, is calculated from the current output of the cell and the desired amplifier output voltage.

For measuring the voltage output from an electrochemical cell, the conditioning amplifier is an operational amplifier operated as a non-inverting amplifier (Appendix Ib). The values of the feedback and input resistors are calculated from the voltage output of the electrode and the desired amplifier output voltage.

## Resistive Network and Relays

The prototype resistive network and relays consist of four Coto-Coil (Coto-Coil Co., Inc., Providence, Rhode Island) miniature SPDT reed relays, a four-bit binary ladder network, and a unique two-resistor loading circuit, Figure 21. The two-resistor loading circuit, $R_{s1}$ and $R_{s1'}$, loads the output of the binary ladder network and sets the voltage range over which the resistive network output voltage, $E_1$, can vary.

The four reed relays are activated sequentially by the D-register outputs $D'_1$ thru $D'_4$. The first reed relay, which is activated by $D'_1$ at time $T_1$, switches the most significant bit (MSB) switch, $S_1$, of the binary ladder network. The switching of $S_1$ to the "1" position places the $E_1$ output voltage at its half-range value. If $S_1$ is left in the "1" position and the second MSB switch, $S_2$, is switched to the "1" position by $D'_2$ at time $T_2$, the $E_1$ output is set to its three-quarter range value. But, if $S_1$ is switched back to the "0" position and $S_2$ is switched to the "1" position at time $T_2$, the $E_1$ output is set to its one-quarter range value. Similar adjustments of the next most significant bit switches, $S_3$ and $S_4$, at time $T_3$ and $T_4$ will vary the $E_1$ output around the preceding set value by plus or minus one-half of the preceding step. In this way, the resistive network produces an

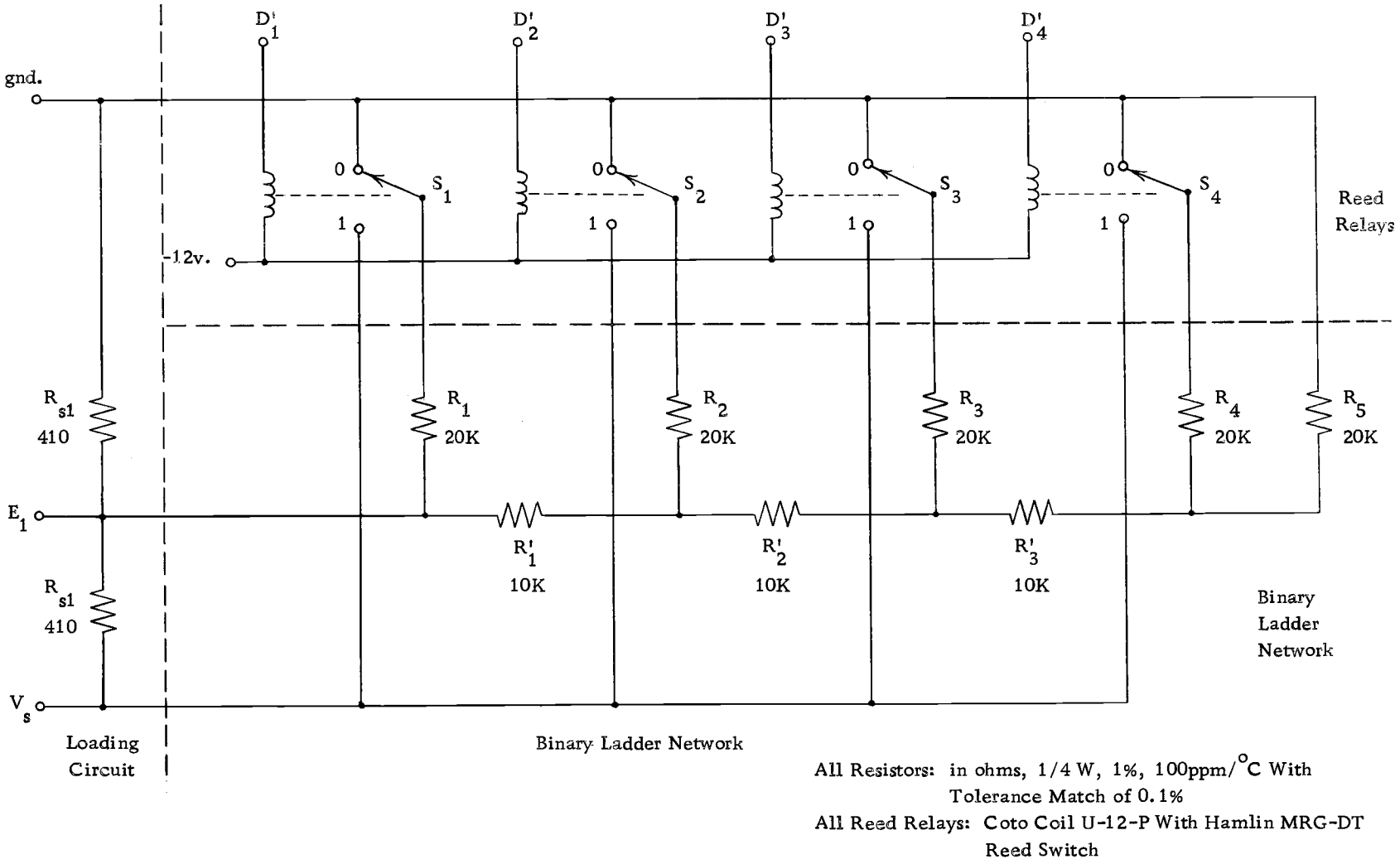



Figure 21. Prototype Resistive Network and Relays.

output voltage, $E_1$, which changes by equal steps from the middle, to any point between the top or bottom of the voltage range set by the loading circuit, $R_{s1}$ and $R_{s1}$.

## Balancing Sequence Example

Consider an example where both $R_{s1}$'s of the loading circuit are removed ($R_{s1} = \infty\Omega$), and an arbitrary value of transducer output, $E_2$, is $+11/32\ V_s$ (Figures 4 and 21). In this case, the range over which $E_1$ can vary is from ground to $+V_s$, and the number of equal steps from ground to $+V_s$ is 16 (i.e., $2^4$ from two possible states for each of the four ladder bits). The following will take place once a measuring cycle has started. We will assume that prior to this time a similar measuring cycle has taken place after which the reset signal has returned all reed switches, $S_1$ thru $S_4$, to the "0" position.

At time $T_1$, as shown in Figure 22, the positive step (-12 v. to 0 v.) of the negative pulse in the $a_1$ "set" waveform will set the first flip-flop in the D-register, thereby changing the $D_1'$ output from the reset level of -12 v. to 0 v. The most significant bit (MSB) switch, $S_1$, is then switched from its reset position, "0", to its activated position, "1", see Figure 21. At this time, $E_1$ will take on a value of $+1/2\ V_s$. This value is larger than that of $E_2$ ($+11/32\ V_s$), which will cause $E_0$ to become negative according to the

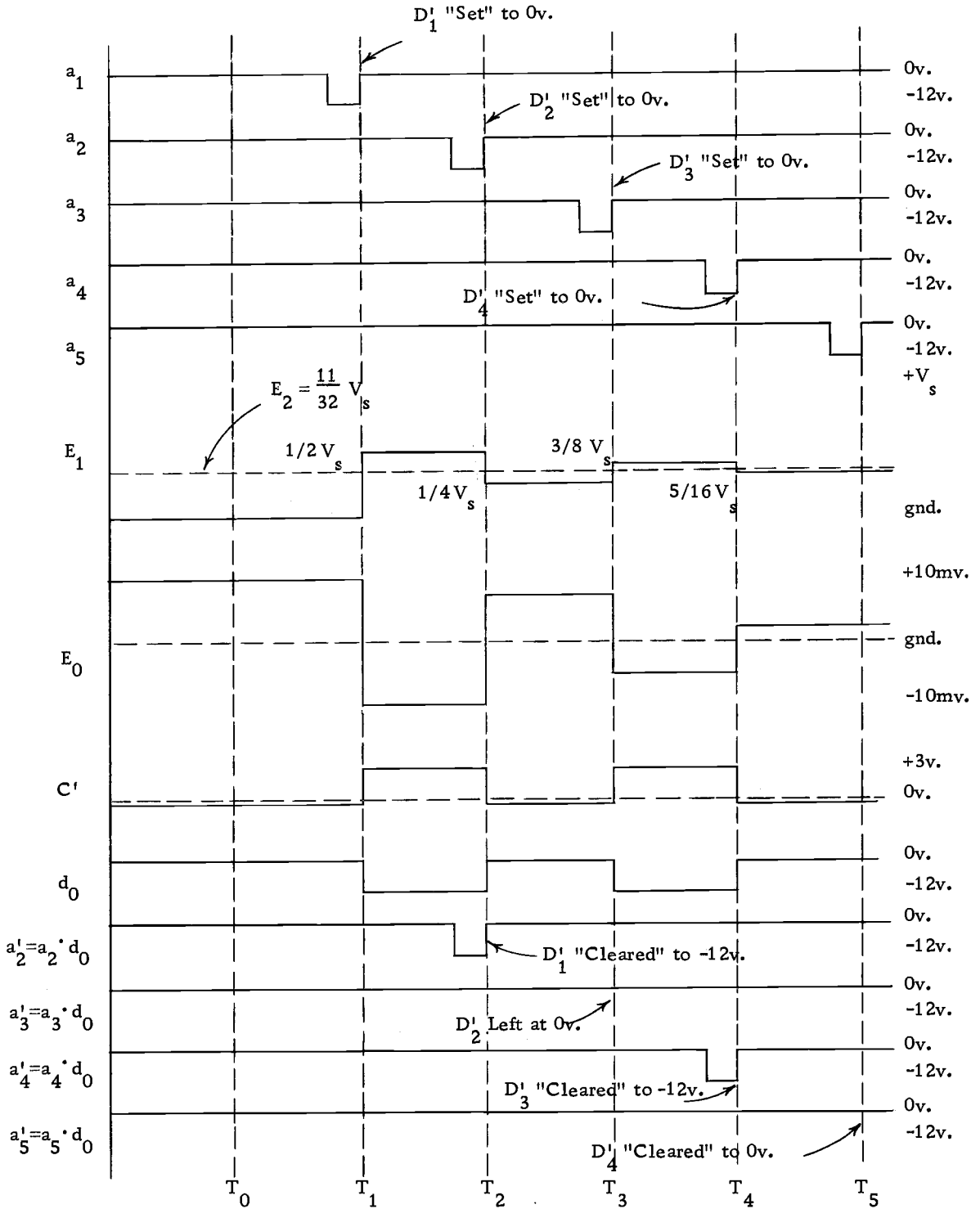



Figure 22. Prototype Balancing Sequence Timing Diagram.

transfer equation for the difference amplifier, $E_0 = 100\ (E_2 - E_1)$. The negative $E_0$ signal will cause the IC comparator to switch to its positive output state where $C'$ equals + 3.2 v. This logic level is inverted and amplified by the comparator inverter amplifier to produce the negative (-12 v.) output, $d_0$. The logical "AND" operation of $a_2' = a_2 \cdot d_0$ is performed by the first diode "clear" gate and in this case is satisfied, thereby generating a negative pulse in the $a_2'$ waveform. The positive step in the $a_2'$ waveform at time $T_2$ "clears" the first flip-flop in the D-register. The $D_1'$ output then returns to -12 v. and $S_1$ returns to the "0" position. Also, at time $T_2$, the positive step in the $a_2$ waveform sets the second D-register flip-flop, thereby positioning $S_2$ in the "1" position.

As a result of the simultaneous switchings of $S_1$ and $S_2$ at time $T_2$, $E_1$ takes on the value of + 1/4 $V_s$. This value of $E_1$ is less than $E_2$, which causes $E_0$ to go positive. The comparator output, $C'$, is switched to -0.5 v. and $d_0$ rises to ground level. The "AND" operation of $a_3' = a_3 \cdot d_0$ is not satisfied and no negative pulse is introduced into the $a_3'$ signal. $D_2'$ remains at zero volts at time $T_3$, and $S_2$ is also left in the "1" position. At time $T_3$, $a_4$ automatically sets $D_4'$ to ground level which activates $S_3$ to the "1" position.

As a result of no return switching action of $S_2$ and the

automatic switching of $S_3$ from "0" to "1" at time $T_3$, $E_1$ assumes the value of + 3/8 $V_s$. This value is larger than $E_1$ which causes $E_0$ to go negative. C' is then switched to +3.2 v. and $d_0$ to -12 v., which allows a negative pulse to be formed in the $a'_4$ signal prior to time $T_4$. The positive step of the $a'_4$ negative pulse "clears" $D'_3$ to the -12 v. level and returns $S_3$ to the "0" position. Also, at time $T_4$, $a_4$ automatically sets $D'_4$ to zero volts which activates $S_4$ to the "1" position.

Resulting from the above two switchings at time $T_4$, $E_1$ assumes the value of +5/16 $V_s$. This value is less than $E_1$ which causes $d_0$ to go to zero volts. The "AND" operation of $a'_5 = a_5 \cdot d_0$ is not satisfied and no negative pulse is developed in the $a'_5$ signal at time $T_5$. This then leaves $D'_4$ at ground level and $S_4$ in the "1" position.

Looking back, we note that $S_1$ is at "0", $S_2$ at "1", $S_3$ at "0", and $S_4$ at "1", giving the final digital output of 0101. This indicates that $E_2$ is between the value of + 5/16 $V_s$ and + 6/16 $V_s$ or equal to + 11/16 ± 1/16 $V_s$.

# FOURTEEN-BIT DIGITAL DATA ACQUISITION SYSTEM

The fourteen-bit digital data acquisition system was designed to automatically measure various physical and chemical properties of sea water. The digital data output is presented in both serial and parallel form for telemetry or direct readout and recording equipment. The system consists of a rechargeable battery supply and amplifier voltage regulators, a fourteen-bit analog-to-digital converter, a low-level scanner, and the transducers with their associated signal conditioning amplifiers, Figure 23.

## Rechargeable Battery Supply and Voltage Regulators

The rechargeable battery supply is a set of series connected "1/2 D" and "D" size Burgess (Burgess Battery Company, Freeport, Illinois) sealed nickel-cadmium rechargeable cells. Twelve "D" size cells (CD10L), having a ten hour discharge capacity of 4.0 ampere-hours, are connected in series to form the negative battery supply voltage $-V_b$. Twelve "1/2 D" size cells (CD13L), having a ten hour discharge capacity of 2.3 ampere-hours, are similarly connected in series to form the positive battery supply voltage, $+V_b$, (Figure 24). The lower positive and negative voltages ($\pm V_l$), to power the logic circuits, are tapped off between the eighth and ninth cell of each battery supply. The use of such high capacity cells gives

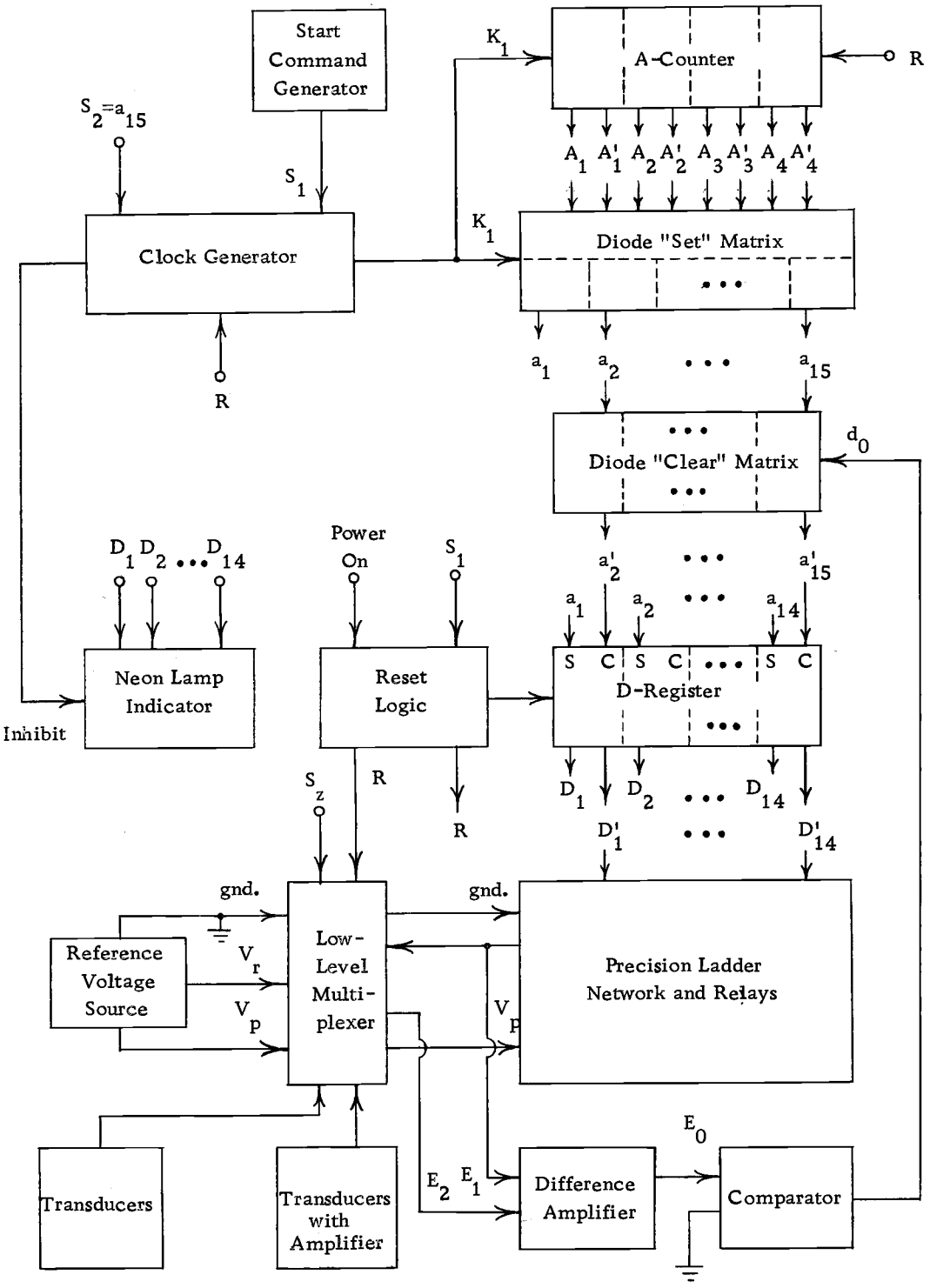



Figure 23. Block Diagram of Fourteen-Bit Digital Data Acquisition System.

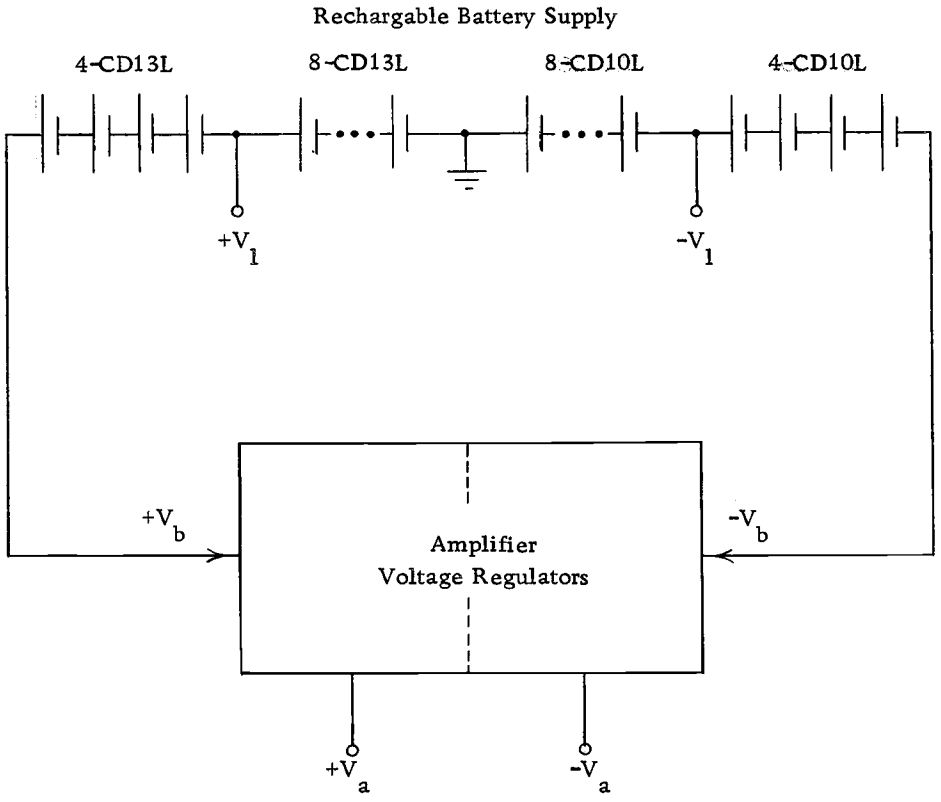



Figure 24. Block Diagram of Rechargable Battery Supply and Amplifier Voltage Regulators.

a battery life of approximately 12 hours between charges. In this way, having two battery packages available, allows the system to be operated continuously.

A μA709C IC operational amplifier is used as both an error amplifier and a current buffer in each of the two amplifier voltage regulators. A series voltage regulator transistor, driven by the error amplifier, increases the current capacity of each amplifier. The regulator circuit is drawn in Figure 25. To simplify the following circuit diagrams, the frequency compensating and supply voltage bypass components for each operational amplifier will be eliminated from the diagrams. It will be assumed, hereafter, that each μA709C IC operational amplifier is compensated and bypassed as described in the preceding section on the prototype difference amplifier (p. 40).

The circuit is unique in that it requires only one voltage reference element for the regulation of two voltages of opposite polarity. This is accomplished by using one operational amplifier as a non-inverting amplifier and the other as an inverting amplifier. The non-inverting amplifier, $NA_o$, amplifies the positive zener reference voltage, $+V_c = +6.56v$, to produce the positive amplifier supply voltage, $+V_a = +10.0v$. A constant zener current of 2ma is drawn from this stable positive voltage through the zener series resistor, $R_c$. The inverting amplifier, $IA_o$, inverts and

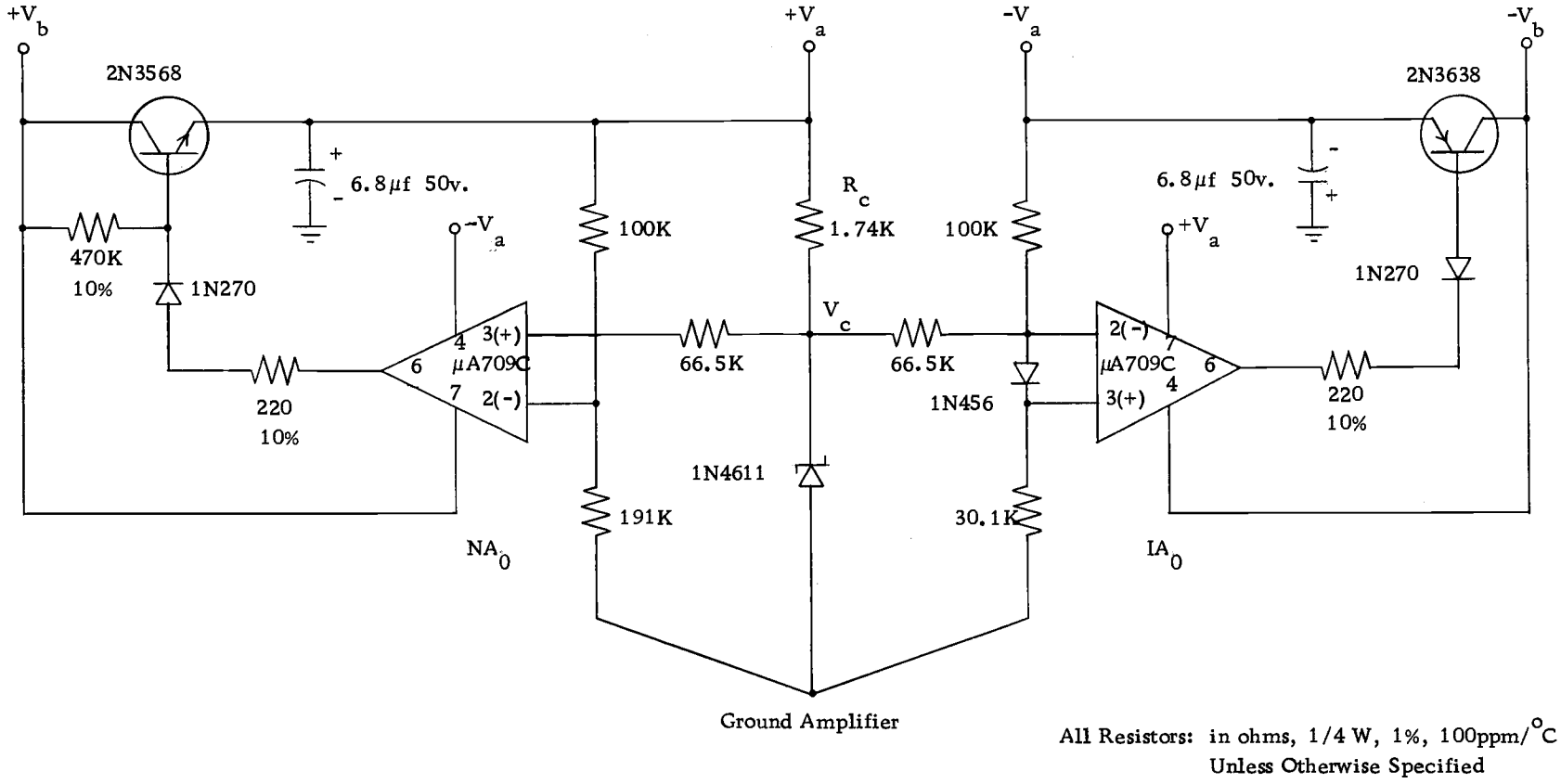



Figure 25. Amplifier Voltage Regulators.

amplifies the zener voltage to produce a negative amplifier supply voltage, $-V_a = -10.0$v. Cross coupling the two regulators, by connecting the negative supply terminal of $NA_o$ to $-V_a$ and the positive supply terminal of $IA_o$ to $+V_a$, increases the voltage regulation.

A high-speed silicon diode is placed across the inputs of $IA_o$, as a means of protecting the amplifier for the case where $+V_b$ might be connected before $-V_b$. In this situation, the voltage at pin 2 tends to rise toward $V_c = 6.56$ v., while the voltage at pin 3 is held at ground level. If the diode did not limit the voltage rise, the amplifier input voltage limitations would be exceeded; and the amplifier might be damaged. The 220Ω resistors perform the function of current limiting, while the 1N270 germanium diodes prevent latch-up. The 470K resistor provides a small bias current to the NPN voltage regulator transistor, thereby assuring reliable start-up.

## Fourteen-Bit Analog-to-Digital Converter

The fourteen-bit analog-to-digital converter uses, in general, the same logic units, basic circuitry, and balancing technique as were tested in the four-bit prototype. The larger converter is many times more complicated than the prototype, due to its ten additional bits of information. To obtain these additional bits, it was necessary not only to increase the digital control capacity, but also to increase the

sensitivity and stability of the precision reference voltage source, the precision resistive ladder network, and the difference amplifier. The clock generator was modified to include the features of starting upon the reception of a command pulse and stopping upon the completion of a balancing sequence. This, of course, starts and stops the converter, which allows the sampling rate to be determined by an external generator.

Figure 23 includes a block diagram of the fourteen-bit analog-to-digital converter; and the following is a block-by-block description to point out the similarities and differences between this converter and the prototype.

Start Command Generator

The generator is a low frequency (4 Hz.) free-running multivibrator, MV-1, followed by two three-input transistor "NAND" gates, AN-1, Figure 26. The $S_1$ output provides, simultaneously, a start command pulse to the clock generator and a reset pulse to the reset logic. The multivibrator differs from MV-2 (Figure 6), only in that the timing capacitors, C, have been increased to 0.5 μf in order to lower the frequency from 150 Hz. to 4 Hz. This frequency then determines the sampling rate of the system. By performing two "NAND" operations (Appendix Ia), AN-1, Figure 27, simply amplifies the multivibrator output $S_1$, to obtain the necessary drive

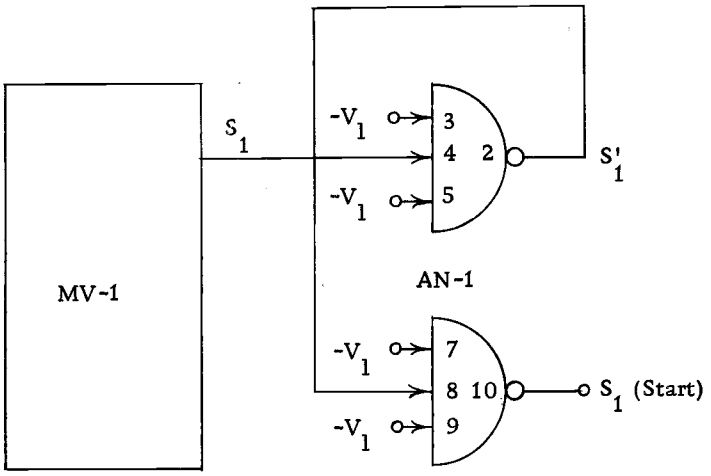



Figure 26. Start Command Generator.

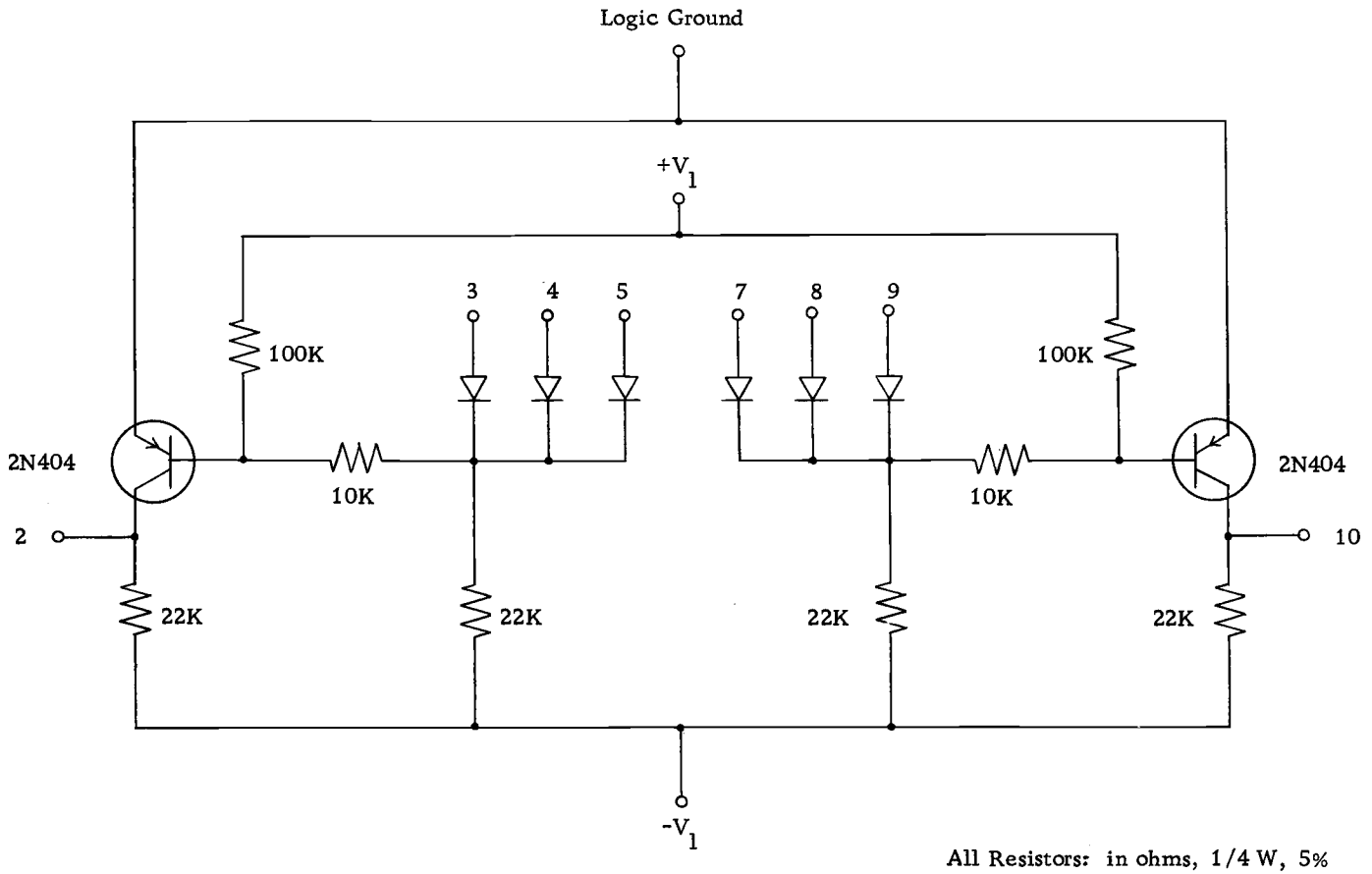



Figure 27. "NAND" Gate Circuit, AN-1.

capability for the $S_1$ (start) signal.

Clock Generator

The clock generator differs from the prototype clock generator (Figure 5), in that a start-stop flip-flop has been inserted between the counting flip-flop and the three-input "AND" gate to control the generator output $K_1$, Figure 28.

The start-stop flip-flop is a standard FF-2 connected in the set-clear mode. A positive step in the $S_1$ (start) input sets the flip-flop output, C, to ground level, thereby gating CG-1 open and allowing $K_1$ to flow. Upon reception of a positive step in the $S_2$ (stop) input, the output is cleared to $-V_1$ which closes CG-1 and stops the $K_1$ pulse train, Figure 29. The $S_2$ input signal is the same signal as the diode "set" matrix output, $a_{15}$.

Reset Logic

A circuit diagram of the reset logic is shown in Figure 30. The circuit consists of two differentiators and one two-input "AND" gate. The "AND" gate allows the output, $R_d$, to be the sum of the two differentiator outputs. As indicated in Figure 29, a positive step in the "power on" input produces a positive reset pulse in both R and $R_d$, thereby resetting all flip-flops in the converter when the power is first turned on. A positive step in the $S_1$ input produces

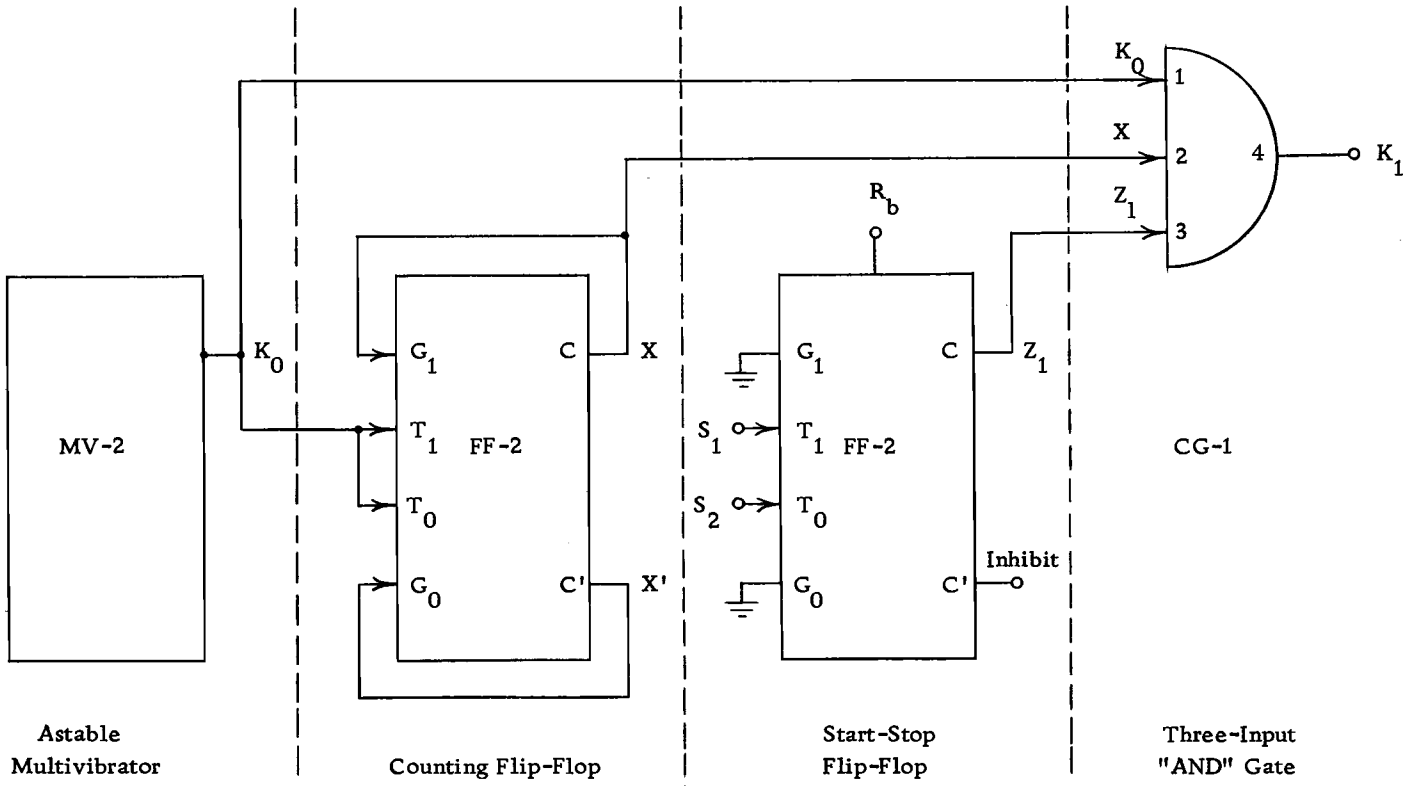



Figure 28. Clock Generator.

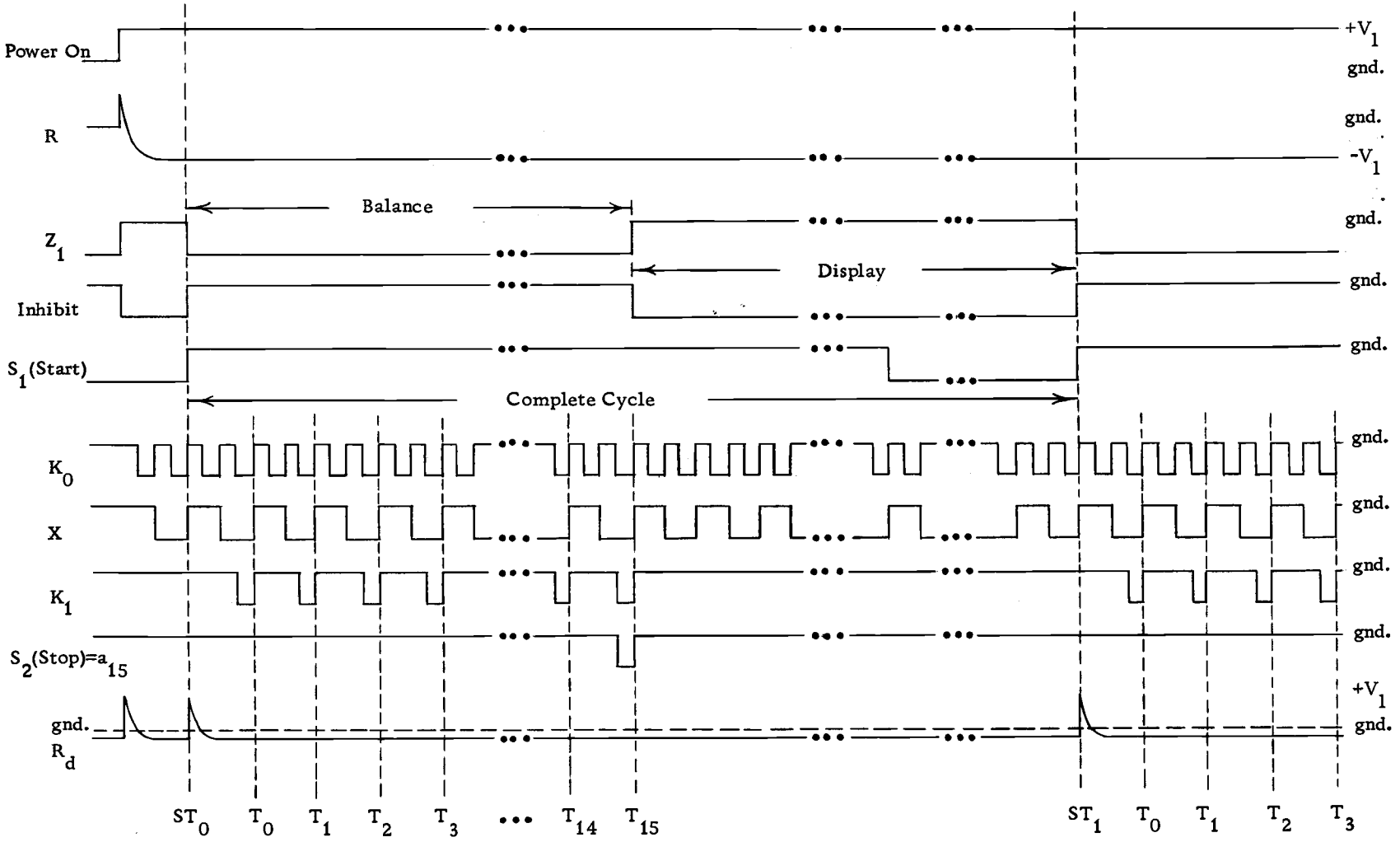



Figure 29. Clock Generator and Reset Logic Timing Diagram.

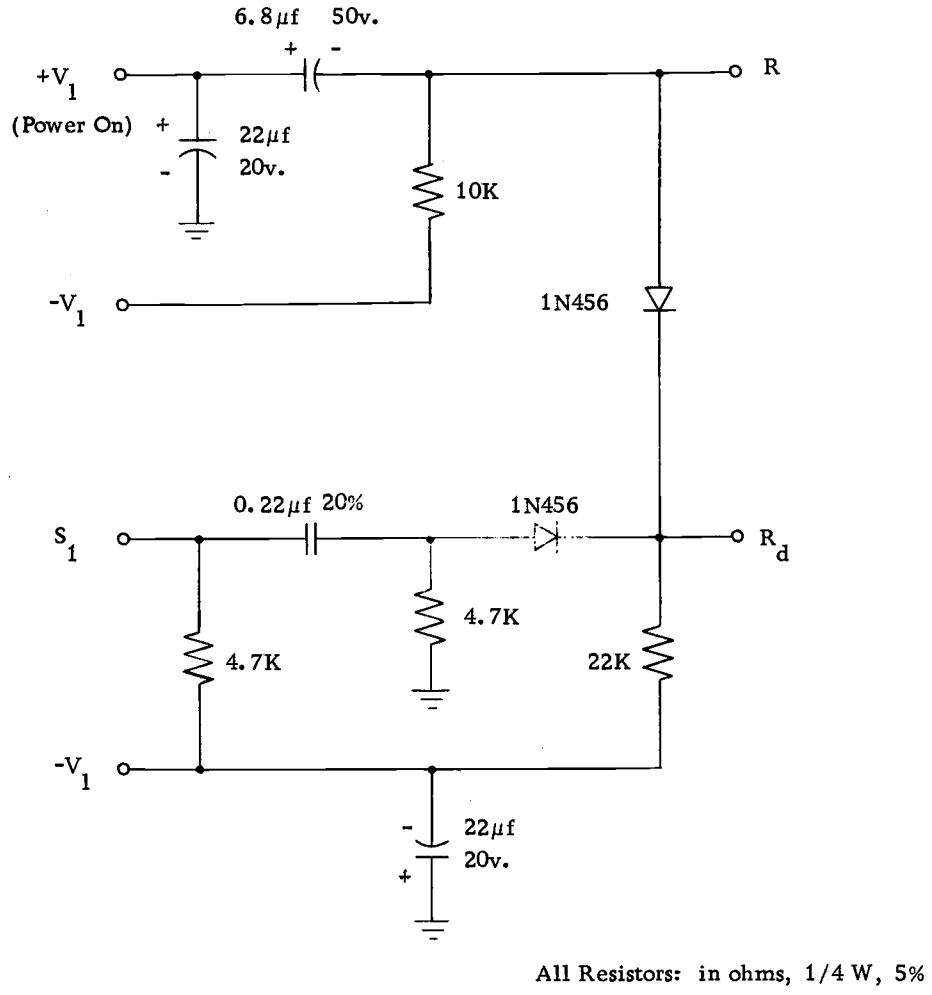



Figure 30. Reset Logic Circuit.

a positive reset pulse in $R_d$ only, thereby resetting the flip-flops in the D-register at the beginning of each balancing sequence.

A-Counter

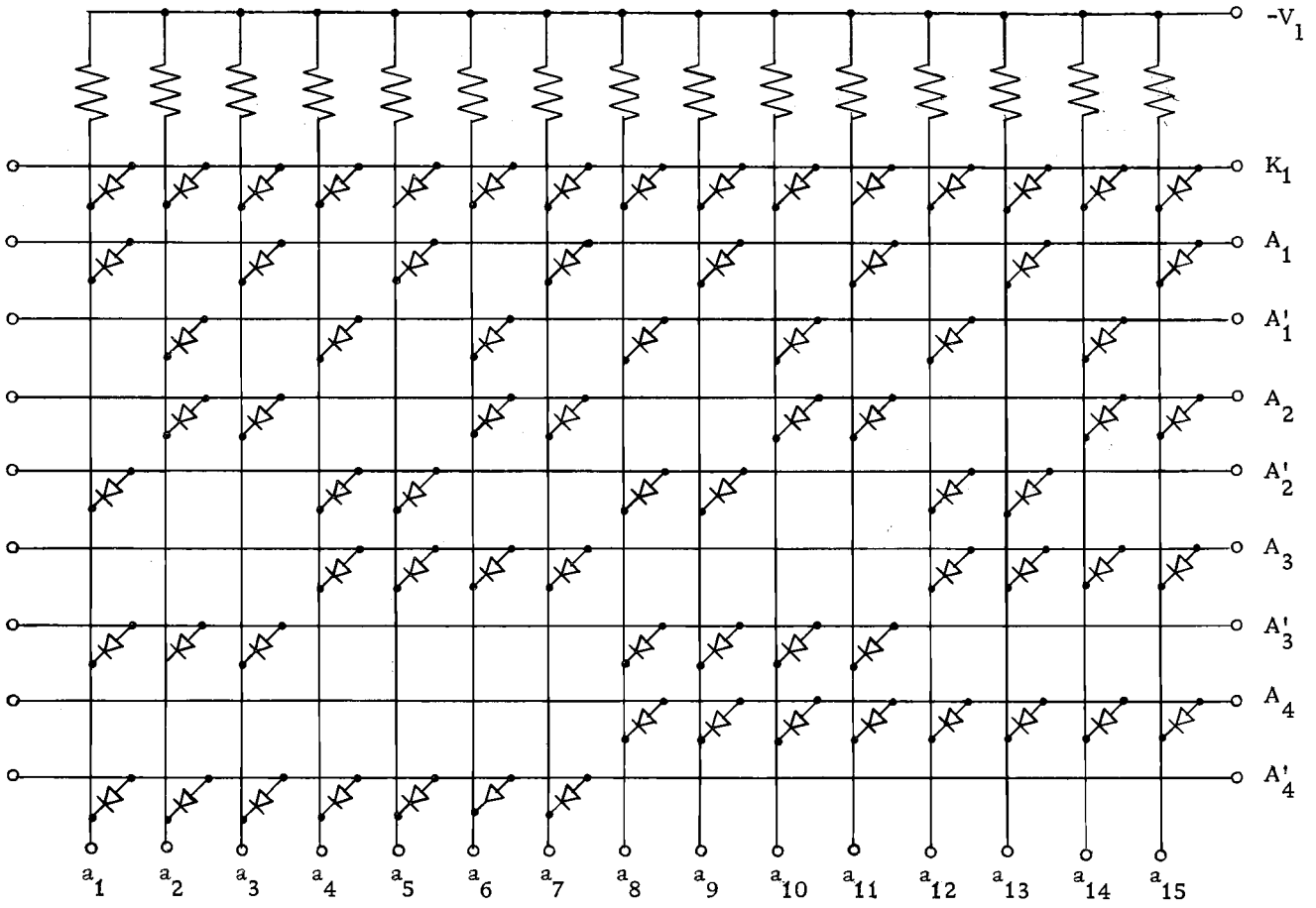
The A-counter is identical to the prototype A-counter (Figure 9), with the exception that a common reset input, R, is connected to the reset input of each flip-flop. The only time the A-counter is reset is when power is first turned on. After every sixteen cycles of the $K_1$ input, which constitutes one full counter cycle, the $K_1$ input is stopped by the start-stop flip-flop. This leaves the counter in its original reset state, ready for the next balancing cycle.

"Set" Decode Matrix

The diode "set" decode matrix is simply an extension of the prototype diode "set" gates. The diode matrix consists of fifteen five-input diode "AND" gates. A circuit diagram is drawn in Figure 31. As indicated in the diagram, the "set" outputs $a_1$ thru $a_{15}$ are derived from the A-counter outputs, which correspond to the second thru sixteenth count of the A-counter.

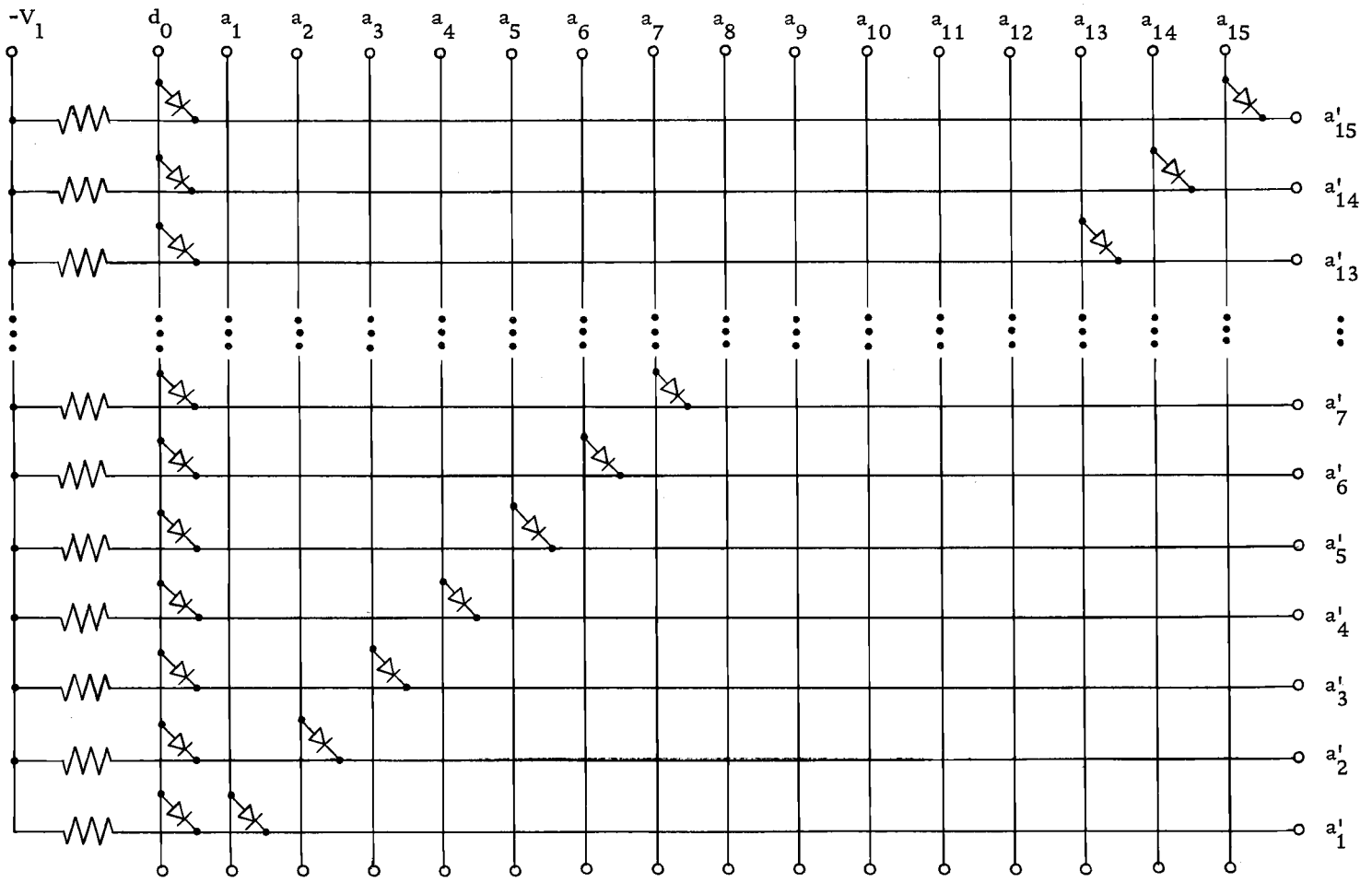
"Clear" Matrix

Similarly, the diode "clear" matrix is an extension of the prototype diode "clear" gates. Figure 32 is a circuit diagram of




All Resistors: 22KΩ, 1/4 W, 5%
All Diodes: 1N456

Figure 31. Diode "Set" Decode Matrix.




All Resistors: 22KΩ, 1/4 W, 5%
All Diodes: 1N456

Figure 32. Diode "Clear" Matrix.

the diode matrix, which consists of fifteen two-input diode "AND" gates. As indicated in the diagram, the outputs $a'_1$ thru $a'_{15}$ are derived from the common feedback input $d_0$ and the diode "set" matrix outputs $a_1$ thru $a_{15}$, respectively.

D-Register

The D register consists of fourteen flip-flops connected together exactly as the four in the prototype D-register. Its operation is identical to the prototype's. The only difference between the two is the ten additional flip-flops (Figure 33).

Neon Lamp Indicator

This is a complete reproduction of the prototype neon lamp indicator in both function and operation. Of course, ten additional driver units were added to increase the display capacity to fourteen bits (Figure 34). The indicator is essentially a straight binary weighted readout. An inhibit signal from the clock generator replaces the $A_4$ signal used in the prototype. Its function is still one of eliminating lamp flickering during the balancing period.

Difference Amplifier

The difference amplifier, however, is completely different from the prototype difference amplifier. Since the stability and

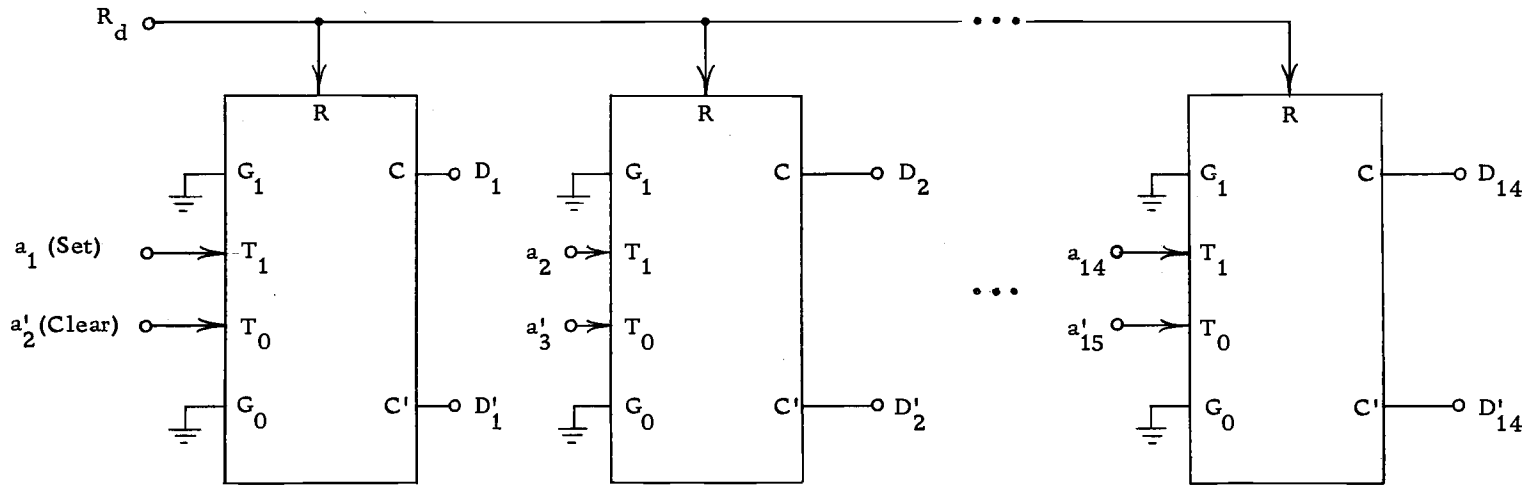



Figure 33. D-Register.

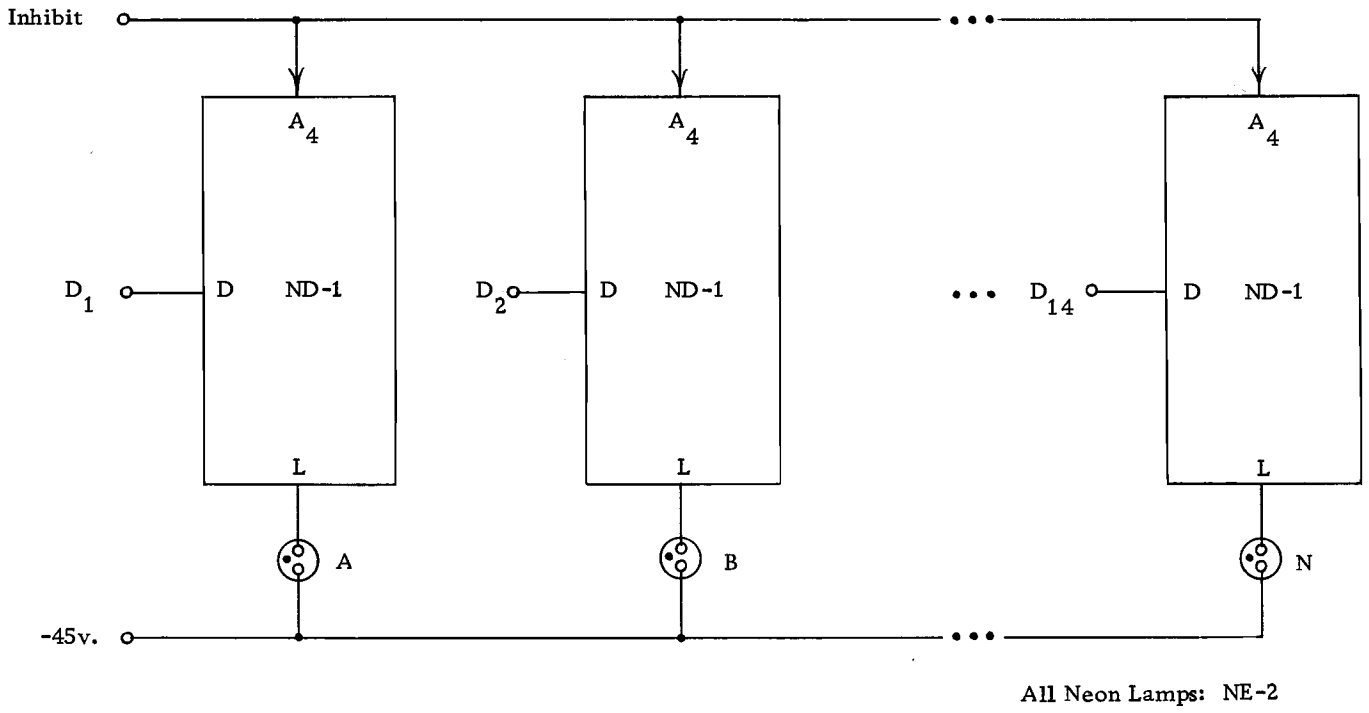



Figure 34. Neon Lamp Indicator.

accuracy of this amplifier directly influences the overall conversion accuracy, the amplifier stablity and accuracy must be made as high as possible. The difference amplifier chosen for this purpose is described by Giles (10, p. 137), as having an input offset voltage drift of only 0.2μv/°C and an open loop gain of three million (Appendix Ib). These characteristics are better than those of most chopper stabilized amplifiers available today. The closed loop gain accuracy and stability are dependent upon the accuracy and stability of the input and feedback resistors. For this reason, the resistors in the amplifier are matched for both resistance and temperature coefficient (Appendix III).

The amplifier consists of one Fairchild μA709C IC operational amplifier preceded by two Fairchild μA726C IC temperature stabilized matched silicon transistor pairs (Figure 35). One matched pair performs the function of a low current preamplifier, while the other performs the function of a voltage follower. Their characteristics and operation are described in the reference cited above. Two well matched 200 KΩ resistors are used as feedback resistors and two equally well matched 1 KΩ resistors are used as input resistors to set the differential gain of the amplifier to 200.

A highly stable differential voltage follower (Figure 36), is placed in front of the difference amplifier to decrease the effect of a changing transducer resistance on the differential gain of the

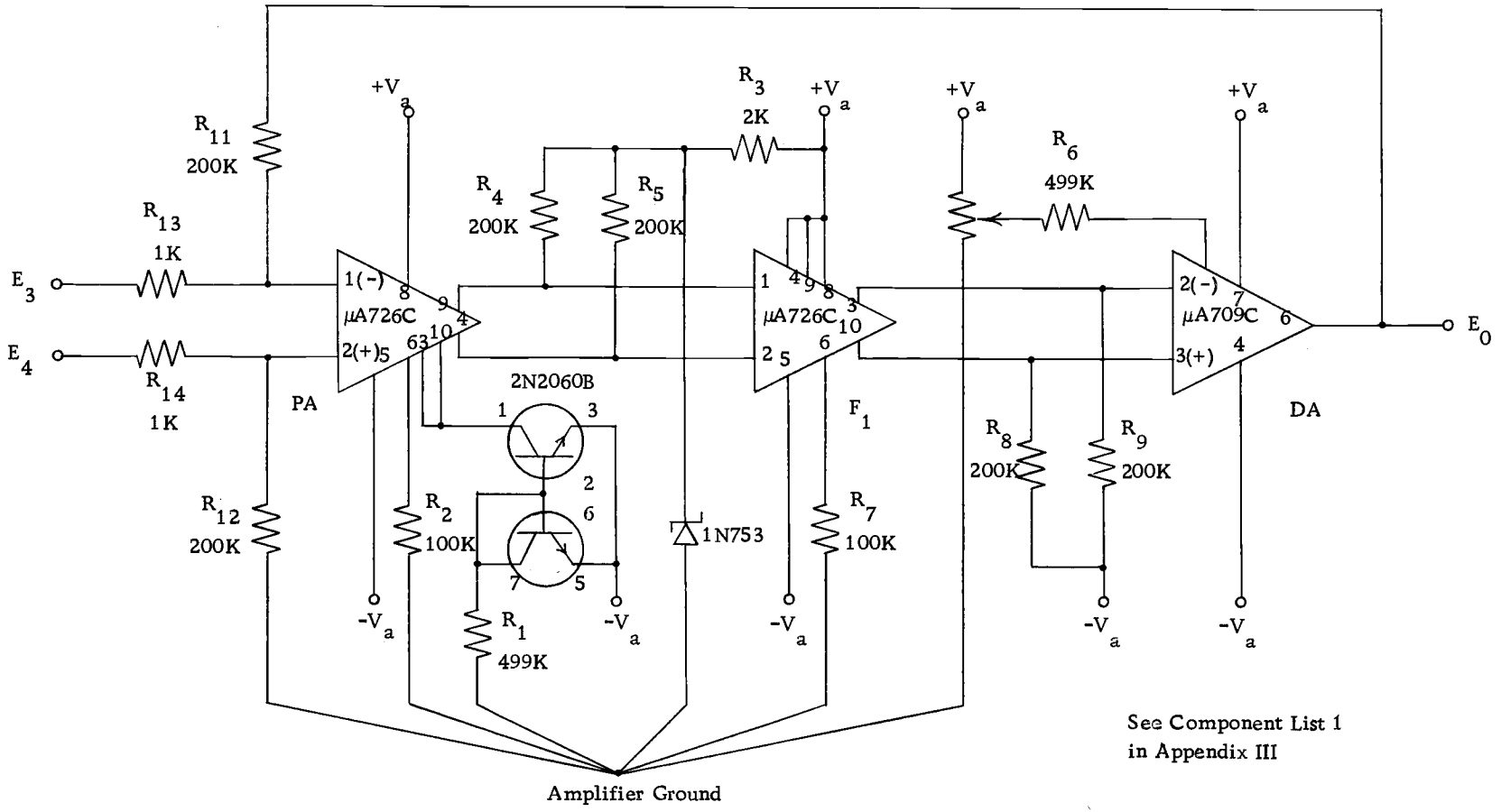



Figure 35. Temperature Stabilized Difference Amplifier.

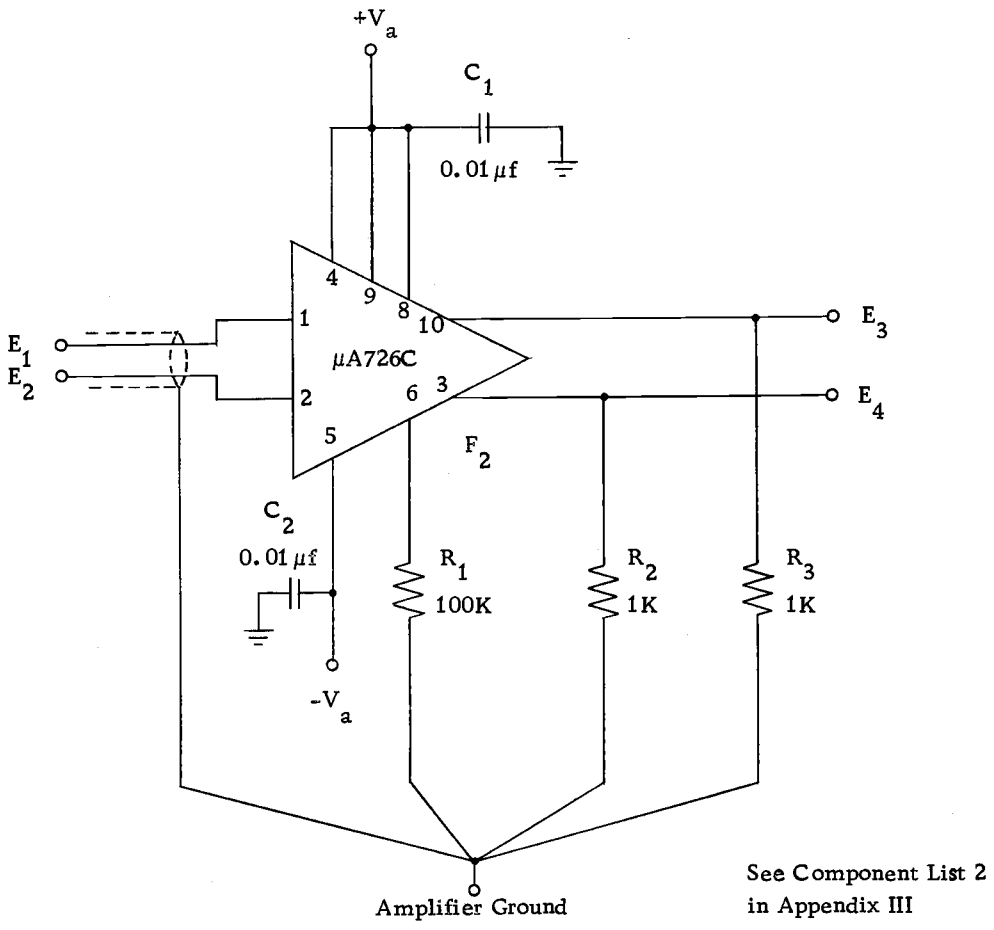



Figure 36. Temperature Stabilized Differential Follower.

amplifier. The follower effectively reduces the source resistance from a value of around 200 Ω to a value of less than one ohm. A disadvantage for the use of this follower is its added input offset voltage temperature drift of 0.2μv/°C. Since this value is equal to that of the difference amplifier's, it increases the total amplifier drift to 0.4μv/°C. As in the prototype difference amplifier, the output voltage, $E_0$, is balanced to zero by adjusting $P_1$ when the inputs are grounded. This is accomplished by removing the μA726C in the differential follower, $F_2$, and shorting pins 3 and 10 to amplifier ground. $P_1$ is then adjusted until $E_0$ equals zero.

Comparator

The μA710C IC comparator used in the prototype comparator has been replaced by two cascaded μA709C IC operational amplifiers to obtain a narrower hysteresis band (Figure 37). Each inverting amplifier has a gain of 100 and, as in the case of the prototype comparator, has its inputs protected by two voltage limiting diodes. The comparator amplifier is different from the prototype, but its function of amplification and voltage level shifting remains the same.

Precision Reference Voltage Source

The reference voltage source is basically the same as the one used in the prototype. However, since a lower excitation voltage is

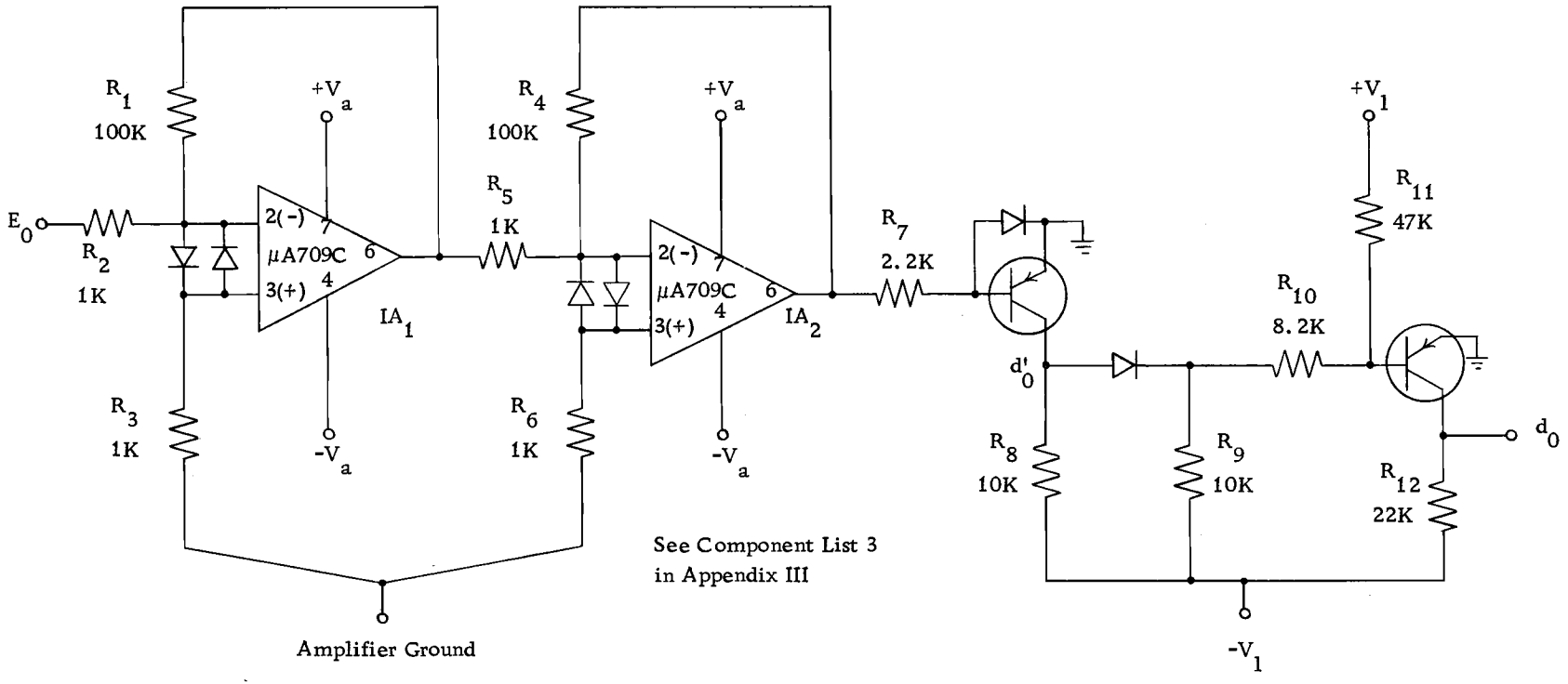



Figure 37. Comparator and Comparator Amplifier.

required for the high sensitivity transducers, a few additions and modifications were made. In the prototype reference voltage source, the functions of zener current regulation, voltage error amplification, and current buffering were performed by the same amplifier. In this reference voltage source, it is not possible to use only one amplifier since the required transducer excitation voltage is less than the voltage of the reference element. Therefore, as indicated in Figure 38, amplifier $NA_2$ performs the function of zener current regulation, while amplifier $NA_1$ operates as a voltage amplifier and current buffer.

The reference element is the same low temperature coefficient (± 20 ppm/°C) unit used in the prototype. The amplifier feedback resistors are low temperature coefficient (± 50 ppm/°C) components. Resistors $R_4$, $R_5$, and $R_6$, which are associated with the reference element, are lower temperature coefficient (± 20 ppm/°C) units in order to minimize any temperature effects on $V_r$ and $V_p$. Resistors $R_4$ and $R_5$ form a voltage divider to tap $V_r$ from $V_z$. $V_r$ is equal to $1/3V_z$ and is used as the reference voltage to measure the confidence level of conversion. The transducer excitation voltage, $V_p$, is set equal to $2V_r$ by amplifier $NA_1$. Therefore, both $V_r$ and $V_p$ are less than the reference element voltage, $V_z$. The resistors, capacitors, diodes, and transistor associated with the outputs of the amplifiers perform the same

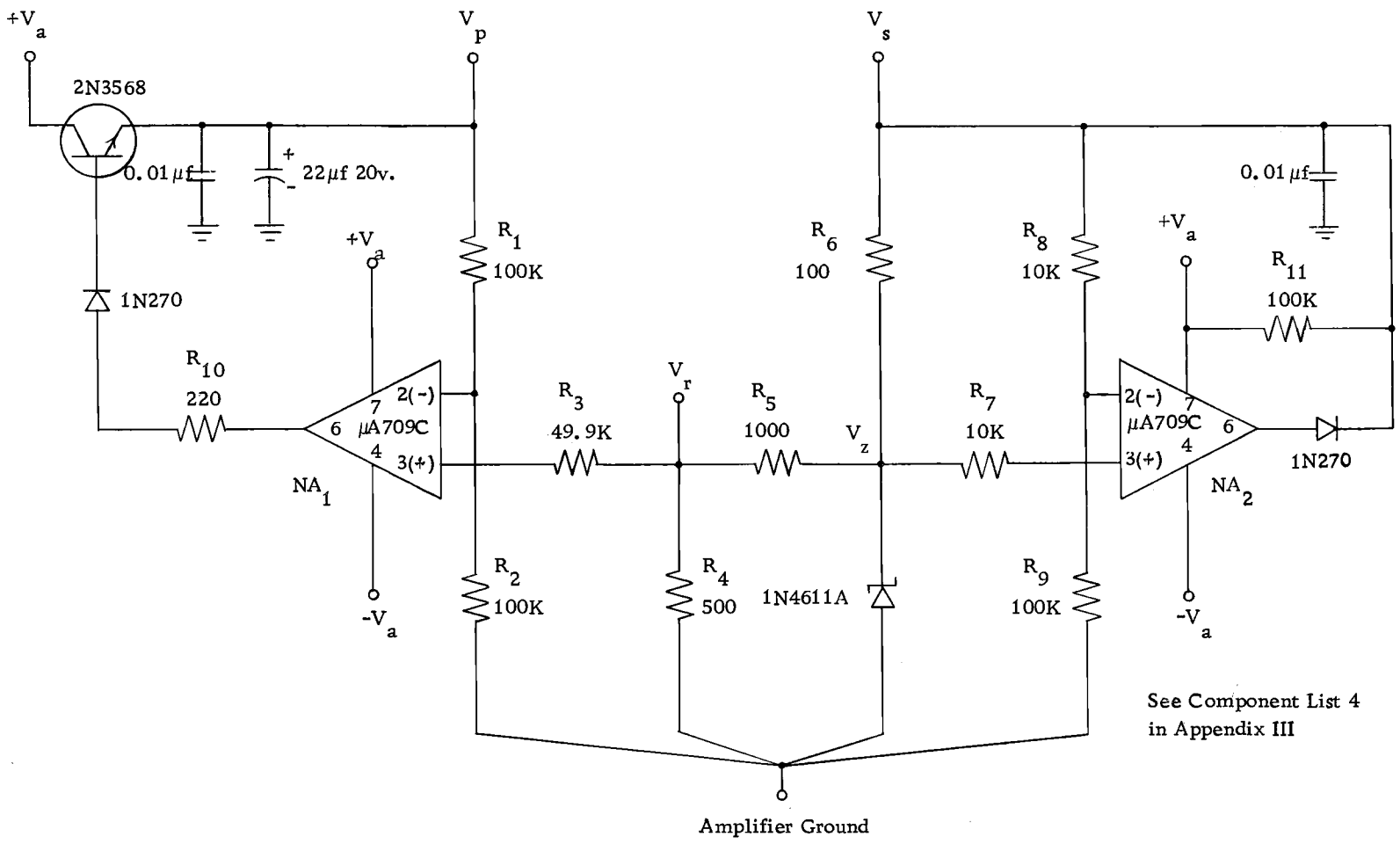
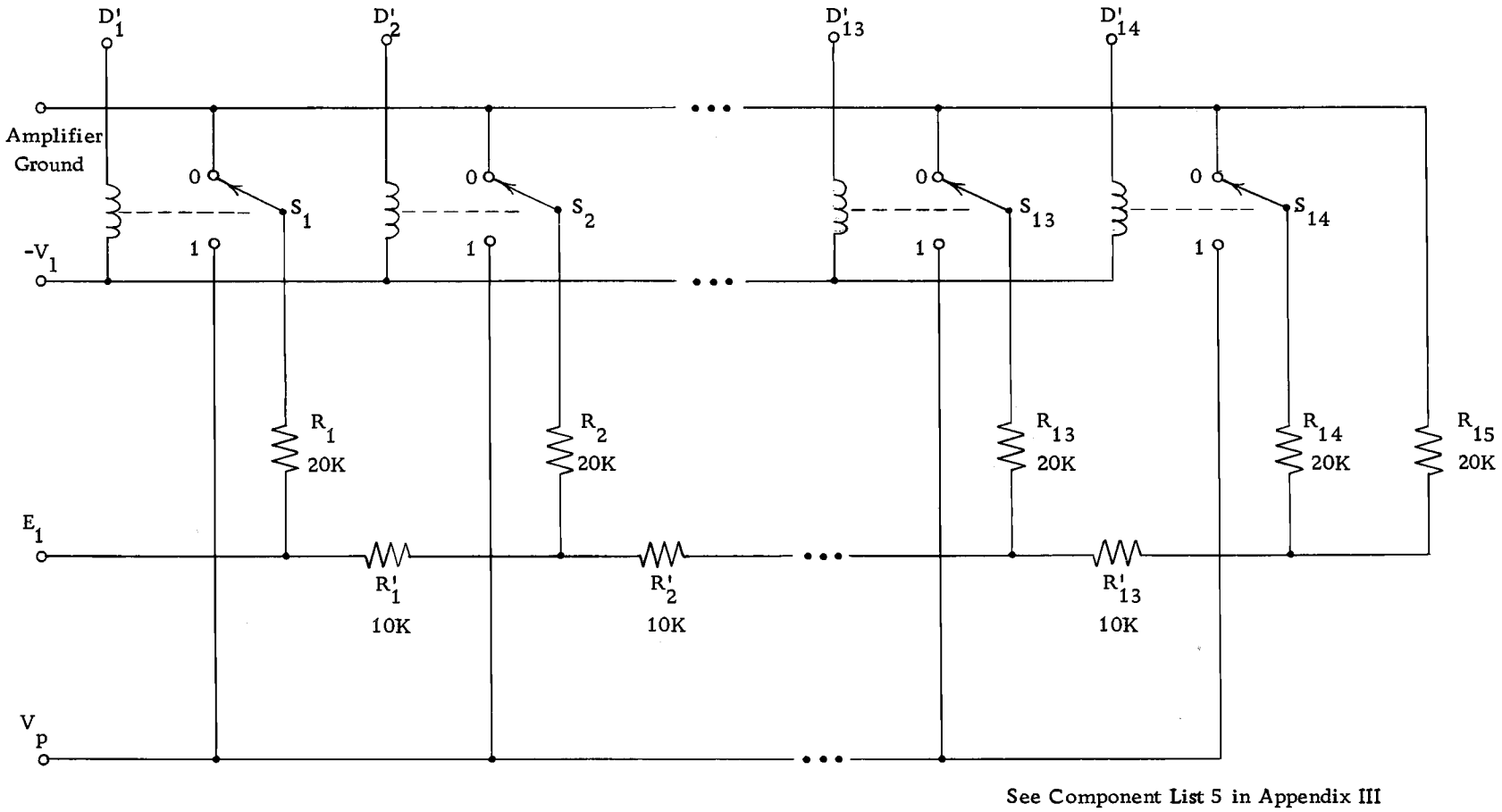



Figure 38. Precision Reference Voltage Source.

function as those used and described in the previous section on the amplifier voltage regulators.

Precision Binary Ladder Network and Relays

This section is essentially an extension of the four-bit prototype ladder network to include ten extra bits. The resistors making up the network are of much better quality, however, and are well matched for both initial resistance and temperature coefficient. The ladder network used is described and analyzed by Susskind (27, p. 5-35). It consists of fifteen 20 KΩ and thirteen 10 KΩ ESI (Electro Scientific Industries, Inc.; Portland, Oregon ) RF2R open-frame precision wirewound resistors (Figure 39). The initial resistance of the resistors was ± 0.01%, with a stability of ± 50 ppm/year. The temperature coefficient was 0 to -2 ppm/°C at 25°C; and temperature tracking is assured, since the resistors were all wound from the same spool of material. The resistors were matched for both resistance variation and temperature coefficient, as indicated in component List 5 of Appendix III. The above tight specifications and close matching were required, in order to assure a 14-bit ladder conversion accuracy of one-half of the least significant bit (± 1/2 LSB) over the anticipated environmental conditions. The resistors were spot-welded together with the same material as was used in making their leads. In this way, thermally generated EMF's, due to




See Component List 5 in Appendix III

Figure 39. Precision Binary Ladder Network and Relays.

dissimilar metal junctions, and contact resistances were held to a minimum.

The fourteen SPDT reed relays are the same as those used in the prototype. Since the reed switch material is a ferromagnetic alloy and the relay solenoid around the switch dissipates up to a quarter of a watt, every reed switch-to-resistor connection is a potential thermal EMF generator. This condition has been minimized by making the connection with a fine copper wire and insulating the switch-to-wire junction as described by Sommer (26, p. 86).

## Low-Level Scanner

The scanner performs the functions of programmable transducer sampling and range selection. Consisting of a binary counter and its associated decoding logic, it controls the sampling sequence. Since the scanner switches very low-level transducer signals, the programmer-controlled reed relays are extremely low-level units of special design. A pair of range setting load resistors are connected to line $E_1$ to select the proper ladder output voltage range for the transducer being sampled (Figure 40).

## Programmer

The programmer B-counter is similar in function and operation to the converter A-counter. It consists of only three counting

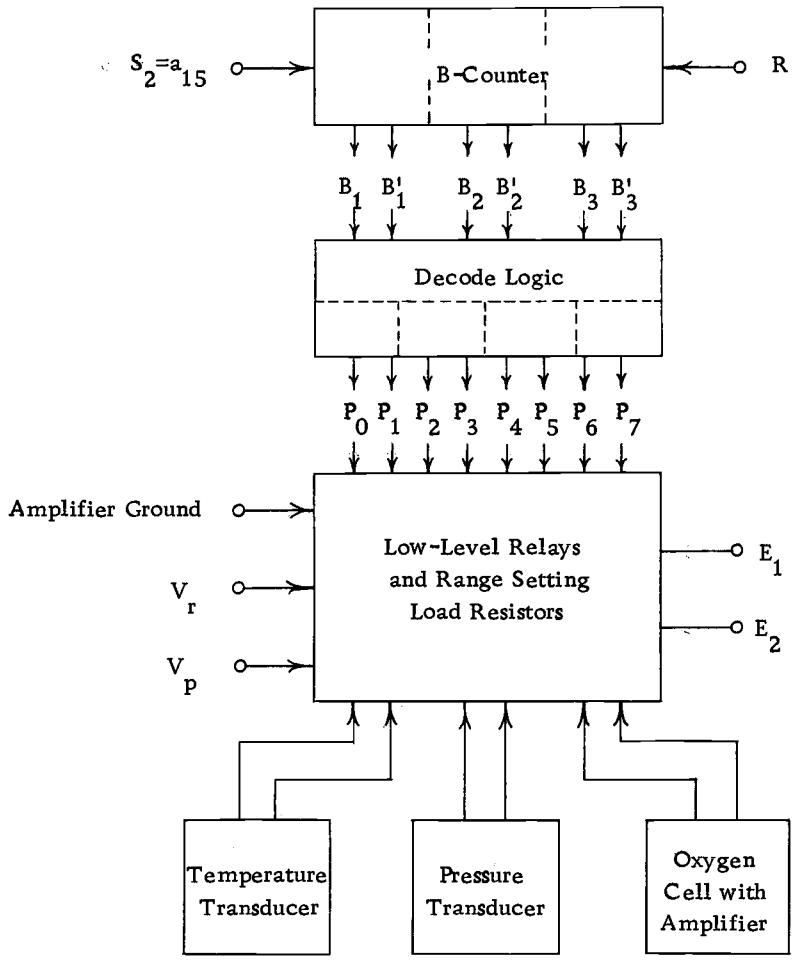



Figure 40. Low-Level Scanner.

flip-flops giving a total of eight ($2^3$) different decodable states per cycle (Figure 41). The counter is triggered by input $S_2$, which progresses the programmer by one step after every converter balancing sequence.

Decoding logic consisting of four AN-1's, (Figure 42), allows each state of the B counter to be decoded. The programmer outputs $P_0$ thru $P_7$ are thus generated to form a series of eight sequential sampling control pulses.

Low-Level Relays

The low-level relays are actuated by the programmer outputs, $P_0$-$P_7$. Upon connecting one or more outputs to a single relay, one can program the frequency and duration of operation of that relay. In order to sample each transducer, two relays are required. They are actuated simultaneously by the same programmer outputs (Figure 43). One relay connects the transducer to line $E_2$, while the other connects the appropriate range setting load resistors $R_s$ to $E_1$.

The relays were specially designed to minimize effects of contact resistance drift and thermally generated EMF. Two series-connected mercury wetted reed switches are used to minimize contact resistance drift, while matched pair and thermal blocking techniques are used to reduce the thermally generated EMF (Appendix IIa). The low-level relays have a constant contact resistance of approximately

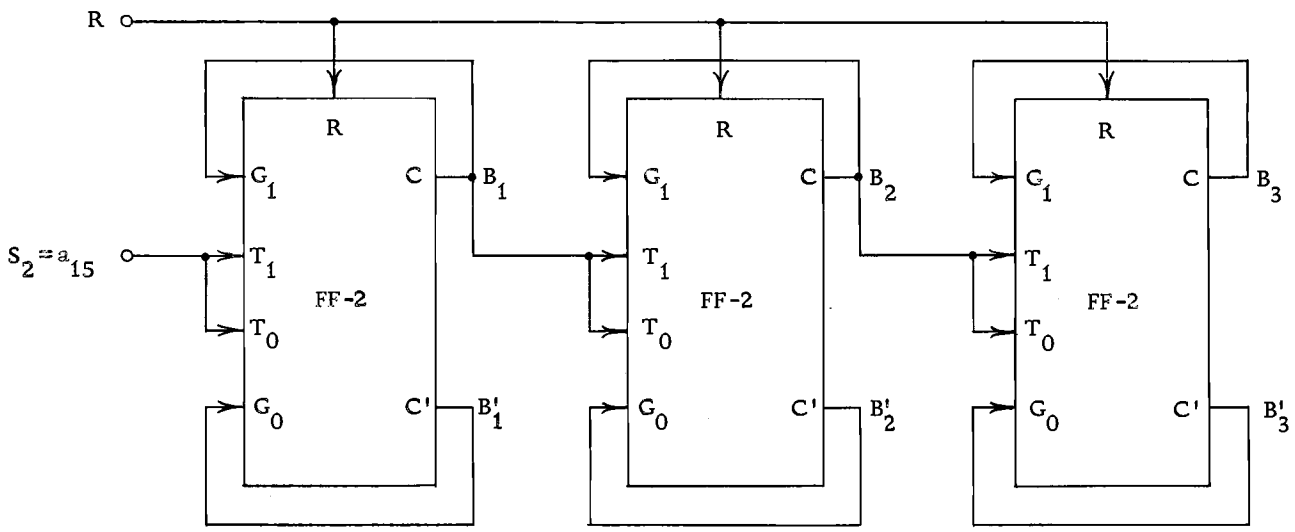



Figure 41. Programmer B-Counter.

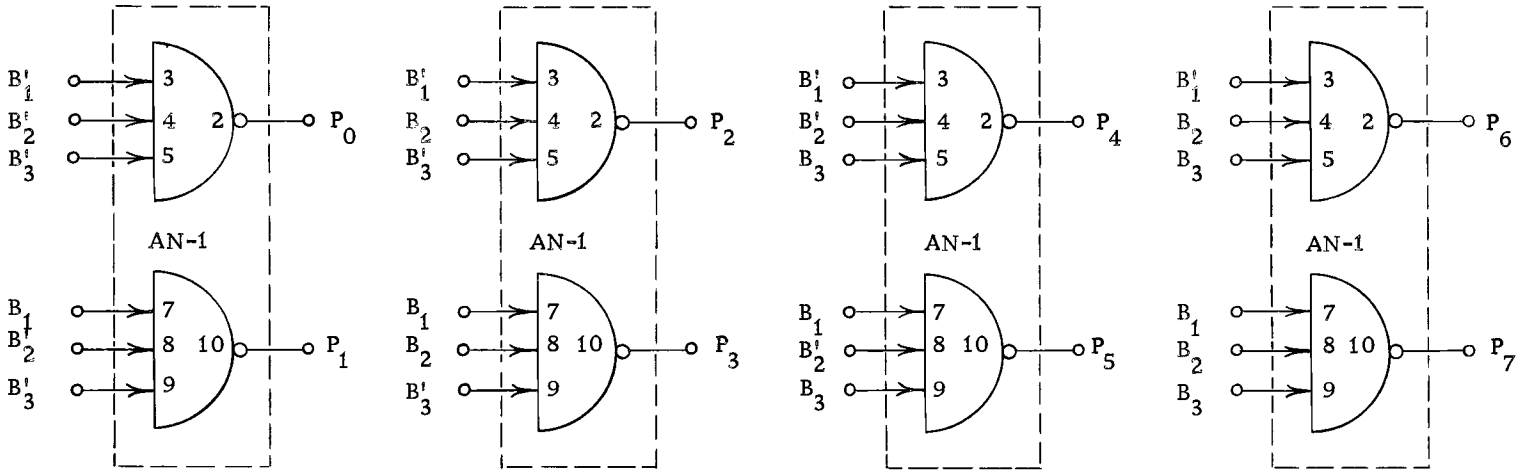



Figure 42. Programmer Decode Logic.

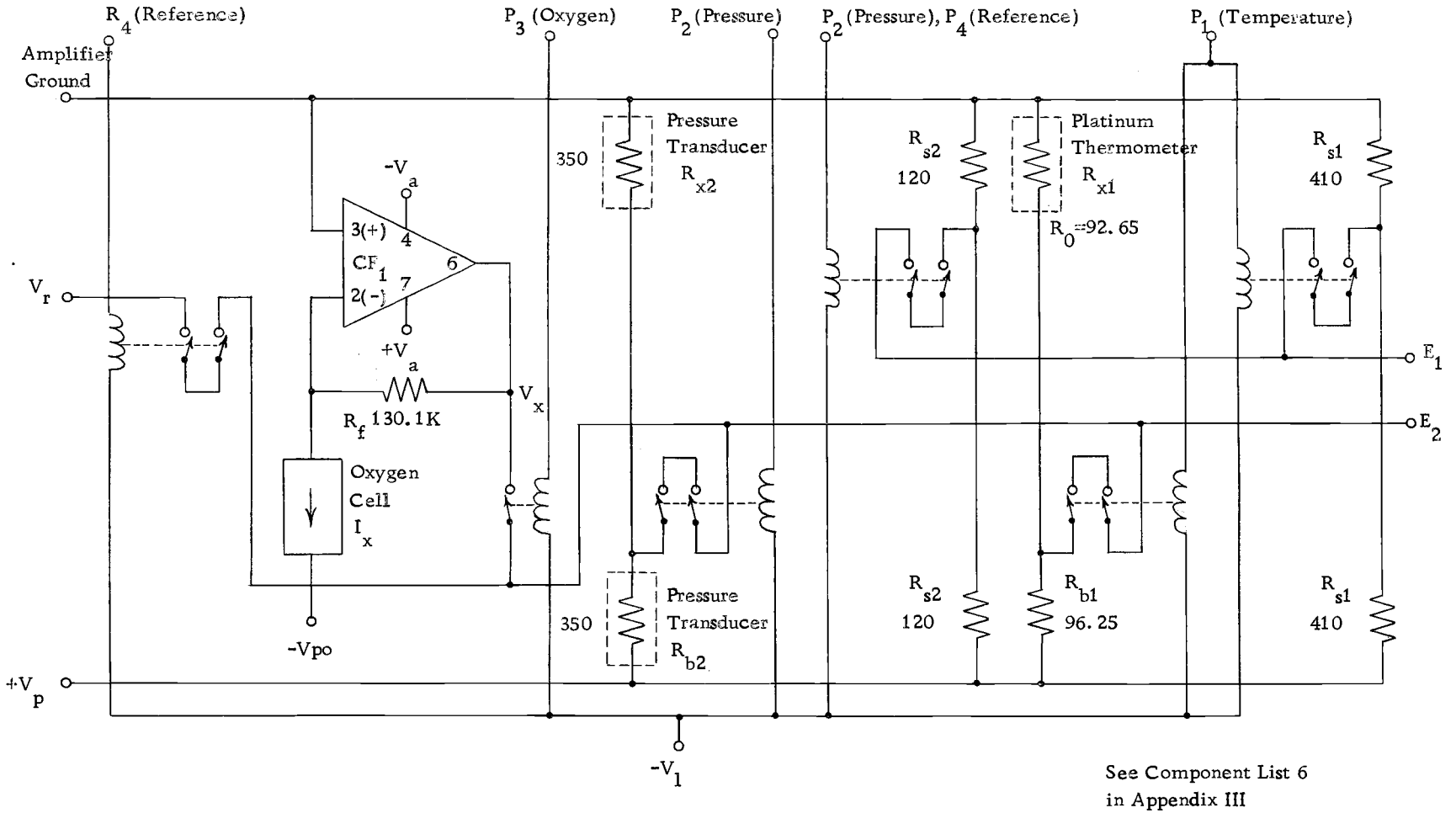


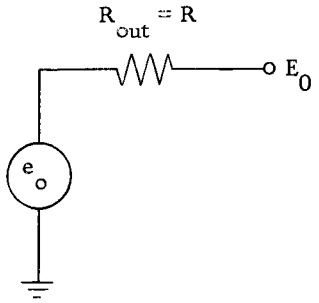

Figure 43. Low-Level Multiplexer and Transducers.

100 milliohms. A maximum EMF of 10 μv. was generated across the copper switch leads when a relay was operated continuously at a solenoid voltage of 14 v. in a 5°C air environment. This was approximately one-seventeenth of the EMF generated by a single, un-blocked mercury wetted reed switch operated under similar conditions.

Range-Setting Load Resistors

The circuit as drawn in Figure 43 shows the connections between the programmer outputs, low-level relays, range-setting load resistors, and transducers. The portion of the zero to $V_p$ voltage range over which the binary ladder output voltage, $E_1$, will vary is determined by the value of the range-setting load resistors, $R_s$. The following formulas were derived to relate the parameters $E_1$, $R_s$, and p.

The loaded ladder network in Figure 44 reduces to the following equivalent circuit of a straight binary ladder network derived by Smith (24, p. 1054) and Susskind (27, p. 5-35), when the range-setting load resistors are removed (i.e., $R_s = \infty$).



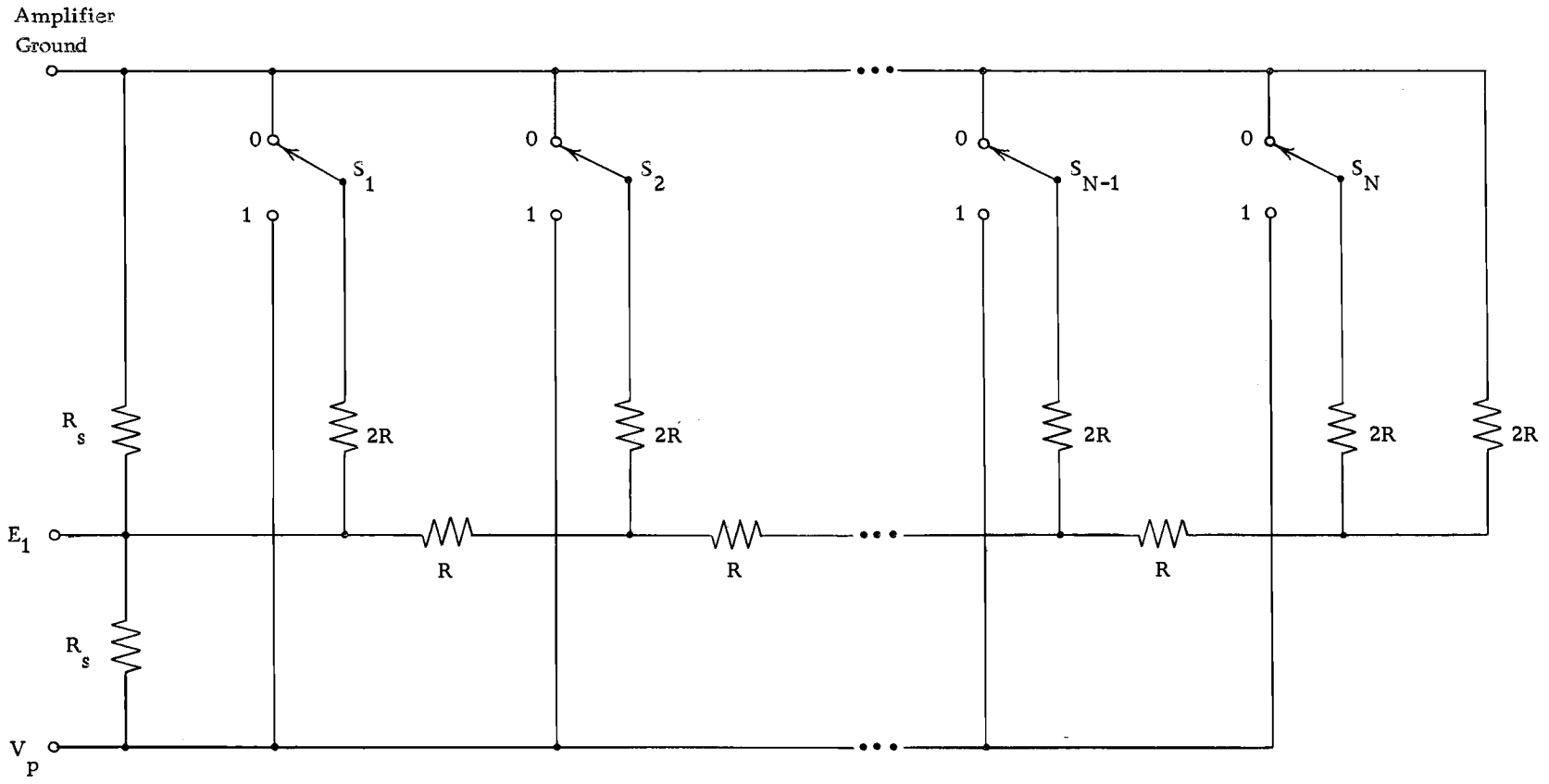



Figure 44. Binary Ladder Network with Range-Setting Load Resistors, $R_s$.

where: $R_{out}$ = Unloaded ladder output resistance = R

$e_o$ = Equivalent voltage source = $\frac{V_p}{2^N} p$

$V_p$ = Constant ladder excitation voltage

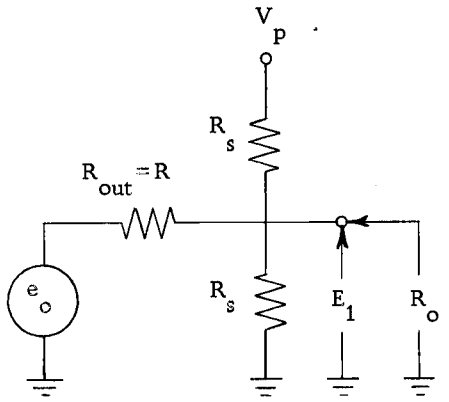
$p$ = Binary number, $S_1 S_2 \ldots S_N$

$$= \sum_{n=1}^{N} S_{N-n+1} 2^{n-1}$$

$N$ = Number of ladder stages

$S_{N-n+1}$ = Switch position = 0 or 1

Adding equal range-setting load resistors to the above equivalent circuit gives the following partial equivalent circuit for Figure 44.




When $S_1$ thru $S_N$ are all "0", $e_o$ is zero, $R_{out}$ is essentially connected to ground, and $E_1$ is at its minimum value as calculated from the voltage divider equations:

$$E_{1(min)} = \frac{V_p \, R \parallel R_s}{R_s + R \parallel R_s} \quad , \quad R \parallel R_s = \frac{R R_s}{R + R_s}$$

$$E_{1(min)} = \frac{V_p \left( \frac{RR_s}{R+R_s} \right)}{R_s + \frac{RR_s}{R+R_s}} = \frac{V_p RR_s}{RR_s + R_s(R+R_s)} = \frac{V_p R}{R_s + 2R}$$

$$E_{1(min)} = \frac{2V_p R}{2(R_s+2R)} = \frac{V_p(R_s + 2R - R_s)}{2(R_s+2R)}$$

$$E_1(min) = \frac{V_p}{2}\left(1 - \frac{R_s}{R_s+2R}\right) = \frac{V_p}{2}\left[1 - \frac{RR_s}{R(R_s+2R)}\right]$$

$$E_{1(min)} = \frac{V_p}{2}\left(1 - \frac{R_o}{R}\right) \qquad (1)$$

where: $R_o$ = loaded ladder output resistance

$$= R \parallel R_s \parallel R_s = \frac{RR_s}{R_s+2R} \quad .$$

Similarly, when $S_1$ thru $S_N$ are all "1" and N approaches infinity, $e_o$ equals $V_p$, $R_{out}$ is essentially connected to $V_p$, and $E_1$ is at its maximum value.

$$E_{1(max)} = \frac{V_p R_s}{R_s + R \parallel R_s} \quad , \quad R \parallel R_s = \frac{RR_s}{R+R_s}$$

$$E_{1(max)} = \frac{V_p R_s}{R_s + \frac{RR_s}{R+R_s}} = \frac{V_p R_s(R+R_s)}{R_s(R+R_s) + RR_s}$$

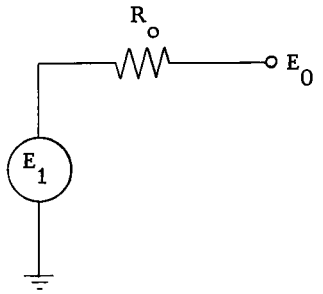
$$E_{1(max)} = \frac{V_p(R+R_s)}{(R+R_s)+R} = \frac{2V_p(R+R_s)}{2(R_s+2R)}$$

$$E_{1(max)} = \frac{V_p}{2}\left(\frac{R_s+2R+R_s}{R_s+2R}\right)$$

$$E_{1(max)} = \frac{V_p}{2}\left(1+\frac{R_s}{R_s+2R}\right) = \frac{V_p}{2}\left[1+\frac{RR_s}{R(R_s+2R)}\right]$$

$$E_{1(max)} = \frac{V_p}{2}\left(1+\frac{R_o}{R}\right) \qquad (2)$$

The equivalent circuit for the symmetrically loaded ladder network of Figure 44 then becomes:




where: $R_o$ = Loaded ladder output resistance = $\frac{RR_s}{R_s+2R}$

$E_1$ = Loaded ladder output voltage.

Through the use of network analysis, it has been proven that, as in the case of the unloaded ladder network, a ladder network symmetrically loaded with equal range-setting load resistors exhibits a linear output voltage variation from $E_{1(min)}$ to $E_{1(max)}$ in a direct relation to the ladder binary input, $p = S_1S_2 \ldots S_N$.

$E_1$ is then the summation of three terms. The first reflects the mid-range voltage value set by the two symmetrical load resistors. The second is the voltage deviation from mid-range when

the binary number, p, equals zero. The third is the incremental voltage variation as a function of p.

$$E_1 = \frac{V_p}{2} - \frac{R_o}{R}\,\frac{V_p}{2} + \frac{R_o}{R}\,\frac{V_p}{2^N}\,p$$

Upon collecting terms, the exact relationship between $E_1$, R, $R_s$, and p becomes:

$$E_1 = \frac{V_p}{2}\left[\,1 - \frac{R_o}{R}\left(1 - \frac{p}{2^{N-1}}\right)\,\right] \qquad (3)$$

where: $V_p$ = Constant ladder exciting voltage

$R$ = Unloaded ladder output resistance

$R_o$ = Loaded ladder output resistance = $\dfrac{RR_s}{R_s + 2R}$

p = Binary number, $S_1 S_2 \ldots S_N$

$$= \sum_{n=1}^{N} S_{N-n+1}\, 2^{n-1}$$

$R_s$ = Range-setting load resistance.

The factor $R_o/R$ is the fractional portion of the zero to $V_p$ voltage range, with center at $V_p/2$, over which $E_1$ will vary for a particular value of $R_s$.

A calculation of the value for the temperature range-setting load resistors, $R_{s1}$, (Figure 43), gives a practical application of the above loaded ladder equivalent circuit and equations (Appendix IIb).

## Transducers

The transducers which are considered in this system are a platinum resistance thermometer, strain gauge pressure transducer, and a polarographic oxygen cell. Any other transducer whose output is in the form of a resistance, voltage, or current variation could be used.

### Temperature

The temperature transducer could be a REC (Rosemount Engineering Company; Minneapolis, Minnesota) Type 171CE platinum resistance thermometer, which is specifically designed for oceanographic applications. It exhibits the outstanding features of ± 0.01°C repeatability and ± 0.01°C pressure error at 10,000 psia (23, p. 3).

### Pressure

For pressure measurement, a modified version of the Taber (Taber Instruments; North Tonawanda, New York) Model 2101 bonded strain gauge pressure transducer could be used. The standard model is a fully active four-arm Wheatstone bridge. The modification would involve the reduction in number of active arms to two, giving a half-bridge configuration. With a pressure range of 0 to 2,500 psig,

the transducer would produce a full scale output of approximately 1.8 mV. per volt of excitation (28). As indicated in Figure 43, the transducer is made up of two 350 Ω strain gauges. When pressure is applied to the transducer, one gauge ($R_{x2}$) undergoes tension while the other ($R_{b2}$) undergoes compression.

Oxygen

The oxygen transducer could be a modification of the polarographic oxygen cell as described by Grasshoff (11, p. 155). The cell is manufactured and can be modified by the Hydro-Bios Apparatebau GmbH; 23 Kiel-Holtenau, Am Jagersberg 7, West Germany. The modification would involve increasing the 500 meter depth range to 1,500 meters (13). The cell possesses the desirable features of ± 0.5% resolution over a dissolved oxygen range of 0 to 10 ml/L, and a long term drift of less than 0.8% per hundred hours of continuous operation (11, p. 159).

# DATA AND CALCULATIONS

Data has been gathered on the system in order to experimentally determine the relationship between the loaded binary ladder network output, $E_1$, and the binary number, p. This allows the determination of measured values for the constants $C_s$ and $D_s$ in the derived equation: $E_1/V_p = C_s p + D_s$, where $V_p$ is the ladder excitation voltage. By comparing these measured values with the calculated values, the validity of the equation can be verified.

Once this relationship has been determined from the data, the system is essentially calibrated for operation in either the resistance ratio bridge or potentiometer mode. This is possible since a null balance method of measurement is used in which $E_1 \cong E_2$ when the bridge or potentiometer is at balance.

The calibration data were obtained on the system while operating in the resistance ratio bridge mode (Figure 2) as stable precision resistance ratio references were readily available. The calibration data could equally well have been obtained on the system, operating in the potentiometer mode. A variable voltage reference source, of stability comparable to the resistance ratio references, would be required. A voltage source of such stability was not available.

For the resistance ratio laboratory calibration, precision

resistors and resistance decade boxes were used to obtain precision resistance ratio references. Tables 1 and 2 contain data for two calibrations, in which the range setting load resistor values were 410.012 Ω and 410.008 Ω.

Referring to Figure 2, the data in Table 1 was obtained by using a 100Ω±0.05% General Radio (General Radio Company; West Concord, Massachusetts) Type 500-D precision resistor as $R_b$ and a parallel combination of two 0.0 Ω to 1,111.0 Ω Gray (Gray Instrument Company; Andalusia, Pennsylvania) Model E-1042-S decade resistance boxes as $R_x$. One decade box was set to 200.0 Ω, while the other was varied from 190.0 Ω to 215.0 Ω in 5.0 Ω steps in order to obtain a varying resistance ratio reference.

In Table 2, the data was obtained by using a 500 Ω±0.05% General Radio Type 500-F precision resistor as $R_b$. $R_x$ was the parallel combination of a 1000 Ω±0.5% General Radio Type 500-H precision resistor and a 0.0 Ω to 1,111.0 Ω Gray Model E-1042-S decade resistance box. The decade box was varied from 940.0 Ω to 1080.0 Ω in 20.0 Ω steps in order to obtain a varying resistance ratio. In both tables, the high precision resistance ratio, $R_x/(R_x + R_b)$, was obtained by measuring the relative values of $R_b$ and $R_x$ on a five place Gray Model E-3207 Wheatstone bridge.

Table 1. Calibration Data for $R_b = 100.067\,\Omega$.

| Equivalent Decimal Number, p | $R_x$ (in $\Omega$) | $\frac{E_2}{V_p} = \frac{R_x}{R_x + R_b}$ | $\Delta p$ | $\Delta\left(\frac{E_2}{V_p}\right)$ | $C_{410} = \frac{\Delta(E_2/V_p)}{\Delta p}$ ($\times 10^6$) | $C_{410}$ Deviation from Average ($\times 10^9$) |
|---|---|---|---|---|---|---|
| 20 | 96.062 | 6.489790 | | | | |
| | | | 2,692 | 0.003316 | 1.2318 | +5.6 |
| 16,328 | 104.174 | 0.510054 | | | | |
| | | | 2,592 | 0.003178 | 1.2261 | -0.2 |
| 3,044 | 97.501 | 0.493506 | | | | |
| | | | 2,514 | 0.003066 | 1.2196 | -6.7 |
| 5,736 | 98.803 | 0.496822 | | | | |
| | | | 2,426 | 0.002956 | 1.2185 | -7.8 |
| 8,328 | 100.067 | 0.500000 | | | | |
| | | | 2,300 | 0.002841 | 1.2352 | +9.0 |
| 10,842 | 101.302 | 0.503066 | | | | |
| 13,268 | 102.507 | 0.506022 | | | | |
| 15,568 | 103.679 | 0.508863 | | | | |

Table 2. Calibration Data for $R_b = 500.15\,\Omega$.

| Equivalent Decimal Number, p | $R_x$ (in $\Omega$) | $\frac{E_2}{V_p} = \frac{R_x}{R_x + R_b}$ | $\Delta p$ | $\Delta\left(\frac{E_2}{V_p}\right)$ | $C_{410} = \frac{\Delta(E_2/V_p)}{\Delta p}$ ($\times 10^6$) | $C_{410}$ Deviation from Average ($\times 10^9$) |
|---|---|---|---|---|---|---|
| 3 | 481.09 | 0.49029 | | | | |
| 16,379 | 521.39 | 0.51040 | | | | |
| 1,567 | 484.80 | 0.49221 | | | | |
| | | | 2,195 | 0.002698 | 1.2292 | +1.1 |
| 3,762 | 490.06 | 0.49490 | | | | |
| | | | 2,134 | 0.002608 | 1.2221 | -6.0 |
| 5,896 | 495.20 | 0.49751 | | | | |
| | | | 2,075 | 0.002546 | 1.2270 | -1.1 |
| 7,971 | 500.27 | 0.50006 | | | | |
| | | | 1,991 | 0.002462 | 1.2366 | +8.5 |
| 9,962 | 505.22 | 0.50252 | | | | |
| | | | 1,948 | 0.002393 | 1.2284 | +0.3 |
| 11,910 | 510.08 | 0.50491 | | | | |
| | | | 1,896 | 0.002322 | 1.2247 | -3.4 |
| 13,806 | 514.84 | 0.50724 | | | | |
| | | | 1,844 | 0.002266 | 1.2288 | +0.7 |
| 15,650 | 519.53 | 0.50950 | | | | |

## Measured Values for $C_{s1}$

The calibration data gives values for the slope, $C_s$, and intercept, $D_s$, in the derived equation: $E_1/V_p = C_{sp} + D_s$. As $C_s$ and $D_s$ are different constants for different values of $R_s$, the constants corresponding to this calibration are $C_{410}$ and $D_{410}$.

The average value for $C_{410}$ from the data in Table 1 is $1.226 \times 10^{-6}$, while the average value for the data in Table 2 is $1.228 \times 10^{-6}$. The deviation of $C_{410}$ from the average within each table can be attributed almost entirely to the inaccuracies in the calibrated resistance ratio references. These inaccuracies are caused by the variation of contact resistances in the resistors making up the ratio references. It is important to note that, within the limits of calibration accuracy, the values for $C_{410}$ are constant and, therefore, the above equation is linear, as predicted in the derivation (Equation 3, p. 93).

## Measured Values for $D_{s1}$

An average value for $D_{410}$ can be obtained from the data by substituting one calibration point and the average value for $C_{410}$ from each table into the equation: $E_1/V_p = C_{sp} + D_s$. If the mid-range calibration point in Table 1 ($p = 8,328$ when $E_2/V_p = E_1/V_p =$

0.500000) along with the average value of $C_{410} = 1.226 \times 10^{-6}$ is substituted into the equation, an average value of $D_{410} = 0.4898$ is obtained.

If the mid-range calibration point in Table 2 (p = 7,971 when $E_2/V_p = E_1/V_p = 0.500059$) along with the average value of $C_{410} = 1.228 \times 10^{-6}$ is substituted into the equation, an average value of $D_{410} = 0.4903$ is obtained. The slight variation between the two values can also be attributed to the inaccuracies in the calibration ratio references due to varying contact resistances.

## Calculated Value for $C_{s1}$

A calculated value for $C_{s1}$ can be obtained by differentiating $E_1/V_p$ in Equation 3 with respect to p. This gives the slope, $C_{s1}$:

$$C_{s1} = \frac{d(E_1/V_p)}{dp} = \frac{R_o}{R} \times \frac{1}{2^N}$$

where: $R_o = \frac{RR_{s1}}{R_{s1} + 2R}$

N = 14 (for fourteen-bit converter)

Upon inserting the exact value for $R_{s1} = R_{410} = R10\,\Omega + 25$ ppm and $R = 10K\Omega + 7$ ppm into the above equation, a calculated value for $C_{410} = 1.226 \times 10^{-6}$ is obtained.

## Calculated Value for $D_{s1}$

A calculated value for $D_{s1}$ can be obtained by solving Equation 3 for $D_{s1}$ when $p$ equals zero. This value is equal to that derived in Equation 1, when the bridge is at balance.

$$D_{s1} = \frac{E_{1(min)}}{V_p} = \frac{E_2}{V_p}_{p=0} = \frac{1}{2}\left(1 - \frac{R_o}{R}\right)$$

Upon inserting the exact values for $R_{410}$ and $R$ into the above equation, a calculated value for $D_{410} = 0.4899$ is obtained.

# DISCUSSION AND CONCLUSION

Table 3 brings together the measured and calculated values of $C_{410}$ and $D_{410}$ for the system operating in the resistance ratio mode. The variation between the measured and calculated values is extremely small, and within the range of experimental error. Therefore, the unique digital encoding circuit and converter are linear throughout the measuring range as predicted by the derived equation.

Table 3. Measured and Calculated Values for $C_{410}$ and $D_{410}$.

| | Measured Table 1 | Measured Table 2 | Calculated |
|---|---|---|---|
| $C_{410} \times 10^6$ | 1.226 | 1.228 | 1.226 |
| $D_{410}$ | 0.4898 | 0.4903 | 0.4899 |

If the same high level of resolution could be maintained in the field as was obtained in the laboratory, temperature and pressure could be measured in situ to a degree of resolution almost one order of magnitude greater than that possible by any other system. By using a highly stable platinum thermometer, temperature could be measured over the range of 0 to 20°C with a resolution of ± 0.0012°C. By using a highly stable strain gauge pressure transducer, pressure (depth) could be measured over the range of 0 to 1,500 meters with

a resolution of ± 0.08 meter.

The system, therefore, has the capability of measuring any parameter which can be converted into a varying voltage, current, or resistance. The range over which the measurement can be made is adjustable; and the resolution with which the measurement is made equals ± 0.006% of the full range value. The resolution is constant over the full range as a result of the analog-to-digital converter linearity characteristics.

Future work should be directed toward preparing the laboratory tested system for field applications. This would involve packaging only the linear circuits on 2 1/2 inch in diameter cards, as the digital circuits are already on similar cards. A 2 1/2 inch inside diameter by approximately 48 inch long metal pressure housing would need to be constructed to contain the system and provide a mounting for the transducers. If such parameters as temperature, pressure, and oxygen are to be measured, the recommended transducers should be acquired. If digital data telemetering methods are to be used while the probe is lowered or towed by a surface vessel, a line amplifier should be constructed to amplify and telemeter the serial digital data output signal, $d_0$, along a single conductor cable.

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# APPENDICES

# APPENDIX I

## Equations and Symbols

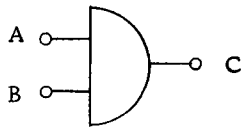
### a. Digital Logic

#### Logic Voltage Levels

In the analog-to-digital converter described in this dissertation, the logic voltage levels are zero (ground) and negative (-12v. or $-V_1$). The negative $(-V_1)$ level is considered the true state, while the ground level is considered the false state.

#### "AND" Operation

When the "AND" operation is indicated, the following symbol and equation are used:

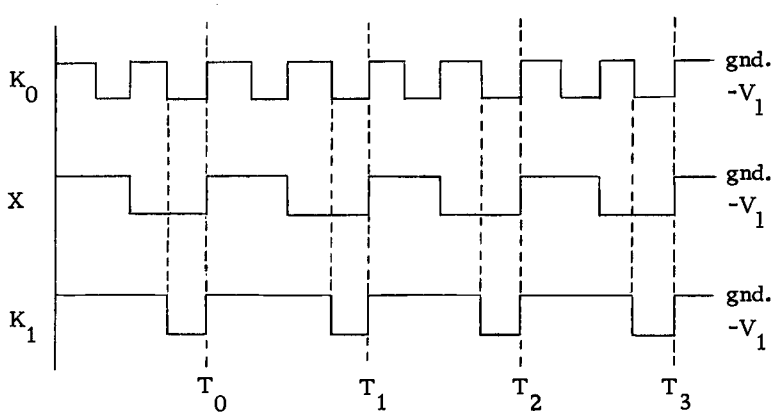



$$C = A \text{ "AND" } B = A \cdot B = AB$$

This means that C is true $(-V_1)$ when both A and B are true $(-V_1)$.

An example of the "AND" operation would be $K_1 = K_0$ "AND" $X = K_0X$. The following diagram, showing $K_1$, $K_0$, and

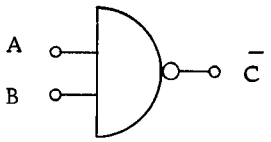
X waveforms, can be helpful in understanding the above "AND" operation.




Note: $K_1$ is negative ($-V_1$) only when both $K_0$ and X are negative ($-V_1$).

"NAND" Operation

The following symbol and equation are used when the "NAND" operation is indicated:



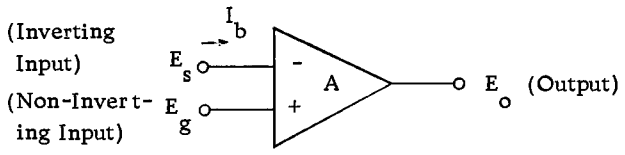

$$\overline{C} = A \text{ "AND" } B = A \cdot B = AB$$

This means C is false (ground) when both A and B are true $-(V_1)$.

b. Analog Operational Amplifiers

Theory and Notation

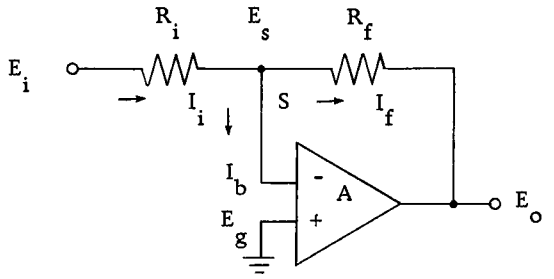
An operational amplifier is a universal amplifier with certain characteristics, which allows one to easily carry out analog operations. Its symbol and basic equation are:




$$E_o = A(E_g - E_s)$$

The characteristics are high open loop gain, $A$ ($10^4$ to $10^6$), and low input bias current, $I_b$ ($< 100\,\mu a$). A low input bias current is indicative of a high input resistance, $R_{in}$ ($> 1\,M\Omega$).

If the output of such an amplifier is connected to the inverting input by a feedback resistor, $R_f$ ($\geq R_{in}$), while the non-inverting input is connected to ground, and with an input resistor, $R_i$ ($\leq R_{in}$) then,




Kirchoff's Current Law gives for the summing point, S,

$$I_i = I_b + I_f$$

while Ohm's Law gives for the voltage drop across $R_i$ and $R_f$:

$$E_i - E_s = I_i R_i, \qquad E_s - E_o = I_f R_f$$

Upon combining the last three equations and solving for $E_o$, we get:

$$E_o = -E_i \frac{R_f}{R_i} + E_s \left(1 + \frac{R_f}{R_i}\right) + I_b R_f$$

This is the exact feedback equation for the operational amplifier. Remembering that $I_b$ is very small, the last term of the above equation will drop out if $R_i$ is such that $I_i >> I_b$. As this is usually the case, the equation becomes:

$$E_o = -E_i \frac{R_f}{R_i} + E_s \left(1 + \frac{R_f}{R_i}\right)$$

Referring to the basic operational amplifier equation, and solving for $E_s$:

$$E_s = E_g - \frac{E_o}{A} = -\frac{E_o}{A} \quad \text{since} \quad E_g = 0$$

Now upon substituting this value for $E_s$ into the above equation for $E_o$,

$$E_o = -E_i \frac{R_f}{R_i} - \frac{E_o}{A}\left(1 + \frac{R_f}{R_i}\right)$$

$$E_o\left[1 + \frac{1}{A}\left(1 + \frac{R_f}{R_i}\right)\right] = -E_i \frac{R_f}{R_i}$$

This is the feedback equation for the operational amplifier assuming only that $I_b \rightarrow 0$. If $A$ is very large, which is usually the case, the term $\frac{1}{A}\left(1 + \frac{R_f}{R_i}\right)$ approaches zero and can be dropped from the equation leaving:

$$E_o = -E_i \frac{R_f}{R_i}$$

This is the feedback equation assuming that $I_b \rightarrow 0$ and $A \rightarrow \infty$. It is important to note that the output voltage is directly related to the input voltage by a factor set by only the resistors $R_f$ and $R_i$

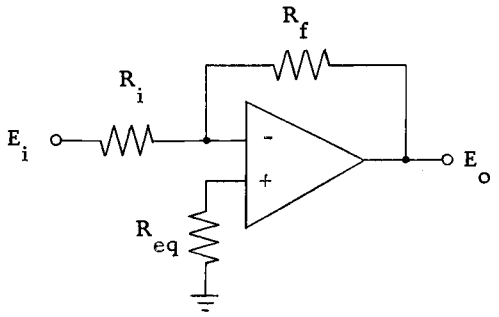
(19, p. 2).

The closed loop gain, $\frac{E_o}{E_i}$, can be expressed in decibels (db) by applying the following formula:

$$\text{Gain (db)} = 20 \text{ Log}_{10} \frac{E_o}{E_i}$$

The following is a set of circuits and related equations for a few of the more important configurations in which an operational amplifier can be used.

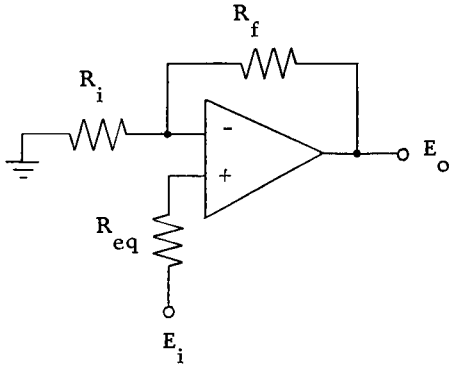
Inverting Amplifier




$$E_o = -E_i \frac{R_f}{R_i}$$

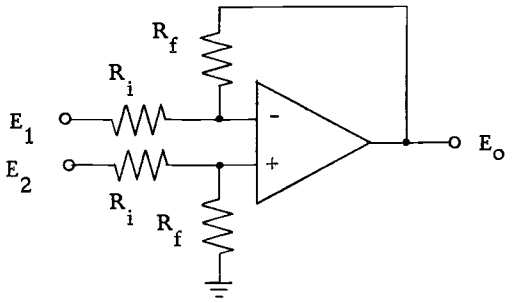
$$R_{eq} = \frac{R_f R_i}{R_f + R_i}$$

Non-Inverting Amplifier



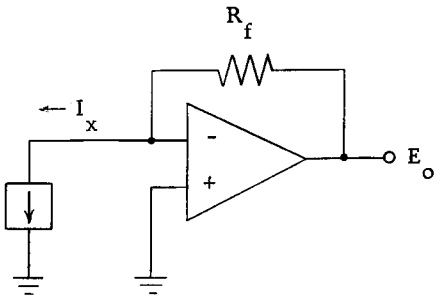

$$E_o = E_i \left( 1 + \frac{R_f}{R_i} \right)$$

Difference Amplifier




$$E_o = (E_2 - E_1) \frac{R_f}{R_i}$$

Current-to-Voltage Converter




$$E_o = I_x R_f$$

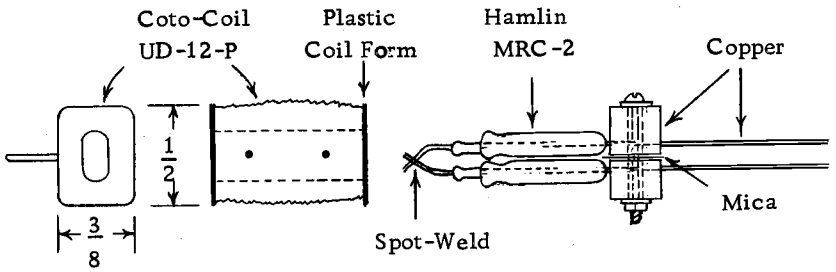
# APPENDIX II

## a. Low-level Reed Relay

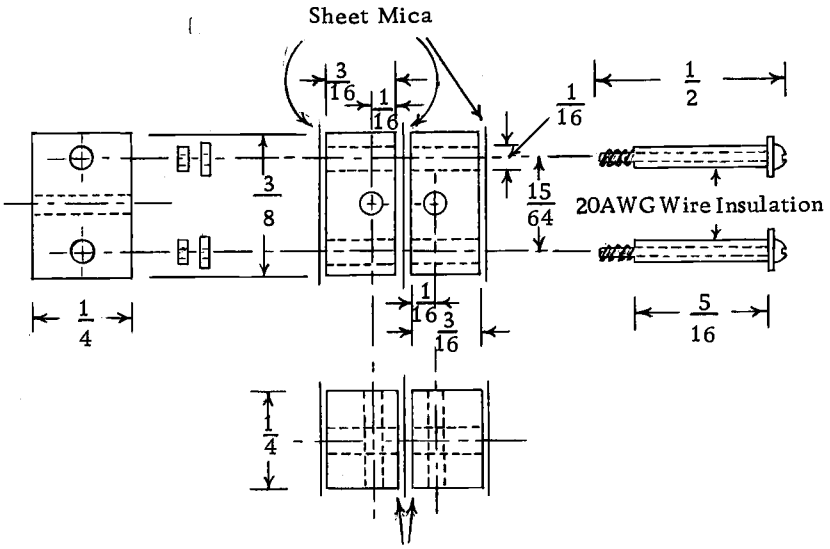
The relay consists of a solenoid, two mercury wetted reed switches, and a copper thermal block. Two Hamlin MRC-2 SPST mercury wetted reed switches are mounted side-by-side in a Coto-Coil UD-12-P solenoid in order to minimize their thermal EMF (Figure 45). The switches are connected in series by spot-welding their leads together at one end. At the other end, where the copper connecting leads are attached to the nickel-iron alloy reed switch leads, the two dissimilar metal connections are fastened together thermally but still electronically insulated from each other. This method of thermal blocking reduces the temperature differential between the two connections and assures that the thermal EMF generated at one will essentially be equal to that generated at the other. Since the two dissimilar metal junctions are in series, their EMF's add together to effectively cancel each other.

## b. Calculation of $R_{sl}$

It is desired that temperature be measured from 0 to 20° with a resolution of at least ±0.005°C and the temperature transducer be an inherently stable platinum thermometer. Since the




Scale Above: 1 in. = 1 in.
Scale Below: 1 in. = 2 in.




Materials: Copper Blocks
Brass Hardware (0-80)

Figure 45. Low-Level Reed Relay.

resistance-termperature coefficient of a platinum thermometer is approximately 0.4%/°C (Lion, 17, p. 155), a platinum thermometer, $R_x$, with an ice point resistance of $R_0$, will have a resistance of 1.08 $R_0$ at 20°C. This very slight resistance variation precludes the use of all measuring circuits involving a binary ladder network except a unity ratio resistance bridge, if the above desired resolution is to be attained. $R_b$ is chosen to be equal to the mid-range value of 1.04 $R_0$. The value of $E_2$ can be calculated to be:

$$E_{2\,(min)} = \frac{R_0 V_p}{R_0 + 1.04\,R_0} = \frac{V_p}{2.04} = 0.4902 \qquad (4)$$

and

$$E_{2\,(max)} = \frac{1.08\,R_0\,V_p}{1.08\,R_0 + 1.04\,R_0} = \frac{1.08}{2.12}\,V_p = 0.5094\,V_p \qquad (5)$$

By equating Equation (1) in the text to Equation (4) above and solving for $R_s = R_{s1}$, one can determine the value for $R_{s1}$ which will make the minimum value of $E_1$ equal to the minimum value of $E_2$.

$$E_{1(min)} = E_{2(min)} = \frac{V_p}{2}\left(1 - \frac{R_o}{R}\right) = 0.4902\,V_p$$

where:

$$R_o = \frac{R\,R_{s1}}{R_{s1} + 2R} \quad , \qquad R = 10K\Omega$$

$$R_o = (1 - 0.9804)R = (1 - 0.9804)10K\Omega = 1 - 0.9804 = \frac{R\,R_{s1}}{R(R_{s1} + 20K\Omega)}$$

$$R_{s1}(1 - 1 + 0.9804) = 0.398K\Omega$$

$$R_{s1} = \frac{0.398\,k\Omega}{0.984} = 406\Omega$$

# APPENDIX III

## Component Lists

All Resistors: in ohms, $\frac{1}{4}$W, 1% Metal film (IRC MEA), unless otherwise specified.

Resistor Temperature Coefficient: ± 100 ppm/ °C = T - 0,
± 50 ppm/ °C = T - 2

| | | | |
|---|---|---|---|
| $R_1$ | = 499 K | T-2 | |
| $R_2$ | = 100 K | T-0 | |
| $R_3$ | = 2 K | T-0 | |
| $R_4$ | = 200 K | T-2 | (199.2 K+ 11.2 ppm/ °C) |
| $R_5$ | = 200 K | T-2 | (199.8 K+ 12.3 ppm/ °C) |
| $R_6$ | = 499 K | T-2 | |
| $R_7$ | = 100 K | T-0 | |
| $R_8$ | = 200 K | T-2 | (200.8 K+ 15.7 ppm/ °C) |
| $R_9$ | = 200 K | T-2 | (200.0 K+ 6.7 ppm/ °C) |
| $R_{10}$ | = 1.5 K | 10%, Carbon | (IRC GBT-1/4) |
| $R_{11}$ | = 200 K | T-2 | (199.7 K+ 19.0 ppm/ °C) |
| $R_{12}$ | = 200 K | T-2 | (199.6 K+ 24.6 ppm/ °C) |
| $R_{13}$ | = 1 K | T-2 | (1005.4Ω + 5 ppm/ °C) |
| $R_{14}$ | = 1 K | T-2 | (1006.2Ω+ 6 ppm/ °C) |
| $P_1$ | = 100 K | T-0 | Beckman 77P |

List 1. Component list for temperature stabilized difference amplifier (Figure 35).

All Resistors: in ohms, $\frac{1}{4}$ W, 1%, Metal film (IRC MEA)

$R_1$ = 100 K T-0

$R_2$ = 1 K T-2 (1000.8Ω + 5 ppm/ °C)

$R_3$ = 1 K T-2 (1000.2Ω + 5 ppm/ °C)

List 2. Component list for temperature stabilized differential follower (Figure 36).

All Transistors: 2N404

All Diodes: 1N456

Resistors $R_1$ through $R_6$: in ohms, $\frac{1}{4}$ W, 1%, Metal film, ± 100 ppm/ °C (IRC MEA T-0)

Resistors $R_7$ through $R_{12}$: in ohms, $\frac{1}{4}$ W, 5%, Carbon (IRC GBT-$\frac{1}{4}$)

$R_1 = R_4$ = 100 K

$R_2 = R_3 = R_5 = R_6$ = 1 K

$R_7$ = 2.2 K

$R_8 = R_9$ = 10 K

$R_{10}$ = 8.2 K

$R_{11}$ = 47 K

$R_{12}$ = 22 K

List 3. Component list for comparator and comparator amplifier (Figure 37).

Reference Diode: 1N4611A

Diode Temperature Coefficient: ± 20 ppm/ °C

All Resistors: in ohms, $\frac{1}{4}$W, 1%, Metal film, ±50 ppm/ °C
(IRC MEA T-2), unless otherwise specified

$R_1 = R_2 = R_9 = 100$ K

$R_3 = 49.9$ K

$R_4 = 500\,\Omega$, $\frac{1}{4}$W, 1%, Wirewound, 20 ppm/ °C (IRC WW10J)

$R_5 = 1000\,\Omega$, $\frac{1}{4}$W, 1%, Wirewound, 20ppm/ °C (IRC WW10J)

$R_6 = 100\,\Omega$, $\frac{1}{4}$W, 1%, Wirewound, 20ppm/°C (IRC WW10J)

$R_7 = R_8 = 10$ K

$R_{10} = 220\,\Omega$, $\frac{1}{4}$W, 10%, Carbon, (IRC GBT - $\frac{1}{4}$)

$R_{11} = 100$ K, $\frac{1}{4}$W, 10%, Carbon, (IRC GBT - $\frac{1}{4}$)

List 4. Component list for precision reference voltage source (Figure 38).

All Relays: Coto-Coil U-12-P equipped with Hamlin MRG-DT

All Resistors: in ohms, ESI RF2R, initial resistance = ±0.01%, stability = ±50 ppm/year, temperature coefficient = 0 to -2 ppm/ ℃

| | |
|---|---|
| $R_1$ = 20 K+ 7 ppm, -0.8 ppm/°C | $R'_1$ = 10 K+ 7 ppm, -0.2 ppm/°C |
| $R_2$ = 20 K+ 7 ppm, -0.5 ppm/°C | $R'_2$ = 10 K+ 8 ppm, -1.1 ppm/°C |
| $R_3$ = 20 K+ 5 ppm, -0.9 ppm/°C | $R'_3$ = 10 K+ 9 ppm, -1.3 ppm/°C |
| $R_4$ = 20 K+ 8 ppm, -0.1 ppm/°C | $R'_4$ = 10 K+ 3 ppm, -0.1 ppm/°C |
| $R_5$ = 20 K+ 5 ppm, -0.3 ppm/°C | $R'_5$ = 10 K+ 2 ppm, -0.8 ppm/°C |
| $R_6$ = 20 K+ 8 ppm, -1.0 ppm/°C | $R'_6$ = 10 K- 2 ppm, -0.8 ppm/°C |
| $R_7$ = 20 K+ 9 ppm, -0.1 ppm/°C | $R'_7$ = 10 K- 5 ppm, -1.0 ppm/°C |
| $R_8$ = 20 K+ 3 ppm, -0.8 ppm/°C | $R'_8$ = 10 K- 7 ppm, -0.8 ppm/°C |
| $R_9$ = 20 K+ 9 ppm, -0.5 ppm/°C | $R'_9$ = 10 K- 7 ppm, -0.8 ppm/°C |
| $R_{10}$ = 20 K+ 3 ppm, -0.2 ppm/°C | $R'_{10}$ = 10 K- 8 ppm, -0.5 ppm/°C |
| $R_{11}$ = 20 K+ 1 ppm, -0.3 ppm/°C | $R'_{11}$ = 10 K-10 ppm, -0.3 ppm/°C |
| $R_{12}$ = 20 K- 1 ppm, -0.6 ppm/°C | $R'_{12}$ = 10 K-15 ppm, -0.6 ppm/°C |
| $R_{13}$ = 20 K- 3 ppm, -0.2 ppm/°C | $R'_{13}$ = 10 K-10 ppm, -0.8 ppm/°C |
| $R_{14}$ = 20 K- 15 ppm, -0.1 ppm/°C | |
| $R_{15}$ = 20 K+37 ppm, -0.8 ppm/°C | |

List 5. Component list for precision binary ladder network and relays (Figure 39).

$R_{x1}$ = Platinum resistance thermometer with ice point resistance of 92.65 ±0.2Ω (Rosemount 171 CE)

$R_{x2}, R_{b2}$ = 0 to 2500 psig bonded strain gauge pressure transducer with 350Ω elements (Taber instruments Model 2101 modified per text)

Oxygen cell = Oxygen probe acc. to Grasshoff (Hydro-bios Model 442 100 modified per text)

$R_{s1}$ = 410Ω + 30 ppm, -0.9 ppm/ °C

$R_{s1}$ = 410Ω + 20 ppm, -0.7 ppm/ °C

$R_{b1}$ = 96.25Ω ±0.01%, 0 to 2 ppm/ °C, 50 ppm/year (ESI RF2R)

$R_{s1}$ = 120Ω ±0.01%, 0 to 2 ppm/ °C, 50 ppm/year (ESI RF2R)

$R_f$ = 130KΩ, $\frac{1}{4}$W, ±1%, Wirewound, 20 ppm/ °C (IRC WW10J)

$CF_1$ = Transitron TOA8709 Low-input current IC operational amplifier

List 6. Component list for low-level multiplexer and transducers (Figure 43).